Design and Implementation of Energy Harvesting Powered Wireless Sensor Networks

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Summary (English)

The goal of the dissertation is to demonstrate a methodology for designing and implementing energy harvesting powered wireless sensor network (EH-WSN) nodes. The thesis first presents an overview of state of the art in wireless sensor networks and energy harvesting technologies. Then focuses on the solar and kinetic energy harvesting as a power source for ultra-low power wireless sensor nodes. The dissertation then addresses in detail different aspects of energy management issues in the EH-WSN nodes, when powered from low power sources. Here a number of power reduction techniques are proposed and tested. One of the focus points in this work was developing a concept that can be implemented using off the shelf components alone and allows for the use of the nanowatt and microwatt power sources.

After introducing the novel concepts and discussing all aspects of EH-WSN operation, a methodology is presented for guiding the design process of an EH-WSN node, using a system of well-defined steps. As a demonstration of the methodology two case studies realized by following the proposed guide are presented.

Summary (Danish)

Formålet med denne afhandling er at demonstrere en metodik for design og implementering af trådløse sensornetværksnoder, drevet af energihøst (EH-WSN). Afhandlingen giver et overblik over state of the art indenfor trådløse sensornetværk og energihøst. Den fokuserer dernæst på brugen af sol- og kinetisk energi til at drive ultra-laveffekts trådløse sensornoder. Afhandlingen fortsætter med en detaljeret behandling af forskellige aspekter af energihåndtering i forbindelse med EH-WSN noder, drevet af laveffekt kilder, hvor en række teknikker for at nedbringe effektforbruget skitseres og evalueres. Et af fokuspunkterne i dette arbejde er udviklingen af et koncept, der kan implementeres udelukkende ved brug af hyldevarekomponenter og muliggør udnyttelse af nanowatt og mikrowatt effektkilder.

Efter introduktionen af de grundlæggende koncepter og en diskussion af alle aspekter i driften af et EH-WSN, præsenteres en metodik for designprocessen af en EH-WSN node, der benytter sig af et system af veldefinerede trin. For at demonstrere metodikken gennemgås to case-studier, der er blevet gennemført i overensstemmelse med den foreslåede guide.

Preface

This thesis was prepared at the department of Informatics and Mathematical Modelling at the Technical University of Denmark in fulfilment of the requirements for acquiring a Ph.D. in Informatics.

The thesis deals with designing and implementing energy harvesting powered wireless sensor network nodes. Special accent was set on minimizing the power consumption and developing approaches for collecting energy from ultra-low power energy sources. The goal was to design circuits using commercially available off the shelf components. This approach was important in order to provide a solution to harvesting low power sources that could be implemented fast by small and medium sized companies and research groups who don't have resources to experiment with ASICs

The thesis consists of six main chapters and three appendixes.

In the first chapter a general introduction is made covering the background, motivation, research objectives and contributions of this dissertation.

The second chapter contains a survey of the current state of the art regarding wireless sensor networks. First the concept is explained and illustrated by an overview of different applications. Then the concept of energy harvesting is introduced. This chapter addresses components required for realization of a typical energy harvesting powered wireless sensor network (EH-WSN) node. The components addressed cover both the hardware and the software aspects of a node. The wireless connectivity between the nodes is addressed by describing different low power transceivers and network protocols. The chapter also addresses the concept of the energy aware design that is necessary for an energy efficient operation of the EH-WSN node.

The third chapter is presenting an overview of the different aspects of the design and the implementation of the energy transducers used to convert ambient energy into electrical power. The photovoltaics and kinetic energy harvesters are examined in detail, as the two of the most popular energy harvesting methods used in literature. The kinetic energy transducers examined are: piezoelectric, electromagnetic and electrostatic. The chapter is concluded by an examination of energy harvester interface circuits. An overview of the circuits used for adapting the harvester output to the rest of the circuit is presented together with the circuits used for maximizing the power output of the energy harvester.

The fourth chapter is the first of the two main contribution chapters. This chapter addresses the lack of discreet component based solutions for ultra-low power harvesting from high impedance sources. Backed up with the fact that applications with low sampling rates can be powered even by nanowatts, as the energy will be accumulated at rates down to nanowatts over long periods of time -- two novel circuits are proposed for collecting energy from nanowatt and microwatt power sources. The Nanowatt Voltage Monitor presented requires 2.83 nA while the novel, highly flexible ADC energy management, required 55 nA to operate.

The fifth chapter builds on top of the previous chapters and proposes a methodology for design and implementation of EH-WSN nodes. The presented methodology demonstrates a set of steps that could be followed in order to implement an energy harvesting powered node that would achieve energy neutrality. As a demonstration, the methodology was exercised on two case studies, each implementing a wireless sensor network application. Both case studies were aimed at building automation where one was powered by a photovoltaic and the other by a kinetic energy harvester.

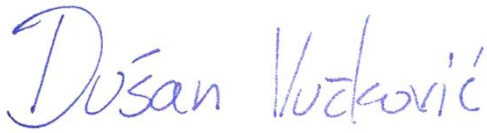
The chapter six is the overall conclusion chapter that summarizes the work done and draws general conclusions.

The Appendix A presents an in-depth analysis of the internal workings of the proposed Nanowatt Voltage Monitor. Here all signal propagations are described in detail.

The Appendix B presents a detailed schematic of the ultra-low power wireless sensor node realized in the first case study of Chapter 5.

The Appendix C presents a detailed explanation of the operation of the circuit used in Phase 2 of the second case study of Chapter 5. In this description the detailed schematic of the circuit is presented together with detailed explanation of all critical signal propagations inside the circuit.

Lyngby, 31-03-2014.



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I would like to thank Danish Electronics Light and Acoustics (DELTA) and Technical University of Denmark for an opportunity to work on the projects that ultimately lead to the writing of the dissertation. I would like to thank my supervisors for their support throughout the duration of the PhD studies.

I would especially like to thank all the people in the IdemoLab department of DELTA. They provided me with a perfect working environment, gave incredible support, and were there to help at every step of the way during the entire duration of the PhD. I can't be more grateful for that.

I would like to thank all the people from Center for Energy Harvesting Materials and Systems (CEHMS) at Virginia Tech for a wonderful 3 month period where I had an opportunity to collaborate with them. Some of the work the dissertation is based on, is coming directly from the joint research I did with them.

I would like to thank my family and all my friends for their limitless support throughout the past three years. Without their support this thesis would've never been completed.

Contents

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List of Acronyms

EH	Energy Harvesting
EH-WSN	Energy Harvesting powered Wireless Sensor Networks
ASIC	Application specific integrated circuit
ADC	Analogue to Digital Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
WSN	Wireless Sensor Networks
IoT	Internet of Things
MCU	Microcontroller Unit
RAM	Radom Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
MRAM	Magnetoresistive Random Access Memory
FRAM	Ferromagnetic Random Access Memory
PCM	Phase Change Memory

MAC	Medium Access Protocol
CSMA	Carrier Sense Multiple Access
SSHI	Synchronous Switch Harvesting on Inductor
SSPB	Single Supply Pre-Biasing
NVD	Nanowatt Voltage Detector
I/O	Input Output
PCB	Printed Circuit Board
AD	Analogue to Digital
RTC	Real Time Clock
SPI	Serial Peripheral Bus
I^2C	Inter-Integrated Circuit

Chapter 1

Introduction

1. Background and Motivation

The development of low power electronics allowed a fast growth of the market of portable electronics. These devices are relying on the amount of energy that they are carrying in batteries for operation. In some applications, such as mobile phone or portable music players, there are possibilities to recharge the battery. However, in some applications recharging or replacing of the batteries is not possible or very difficult. One example of such applications is a wireless sensor network.

Wireless sensor networks are becoming a very popular method for gathering information on various aspects of both human surroundings and industrial environments. Their strongest trait is the possibility for installing them into the existing systems without a need for introducing additional cabling or infrastructure change. A wireless sensor network consists of at least one collection point and a number of wireless sensor nodes that are performing the sensing and sending of data to the collection point(s). The nodes can only run as long as it has battery power available. Therefore, it is necessary to recharge or replace the batteries once they are depleted. However, this can be

very expensive, or even impossible, especially in the applications where the network is deployed in hard to reach places or hazardous environments. For example, the nodes could be placed inside of the walls of the buildings, laid under the pavement of the road, or placed inside an engine. Reduction of the power consumption of the node is not sufficient, as the amount of energy in a battery is finite and, in some applications, insufficient for the required lifetime of the deployment. Using large batteries cannot be an option in some situations. Furthermore, disposing of large quantities of batteries used by large sensor networks can have a major environmental impact. A new concept had to be introduced in order to make the operation of the node battery independent.

A potential solution, to the limitation of the finite amount of energy available in the battery, is powering the electronics from the energy available in the sensor node's immediate surroundings. The process known as energy harvesting (or energy scavenging), converts the energy available in the environment to electrical energy that can be used for powering the electronics. In the recent years a significant research effort has been put into developing different kinds of energy harvesting transducers, which can convert the ambient energy into electrical power, thus providing a stable source for a longer period of time than it was originally possible using a battery.

The most well studied energy harvesting transducers are converting the light energy (photovoltaics), thermal gradient (thermoelectric generators), and mechanical energy (piezoelectric, electrostatic or electromagnetic generators) into electricity. These transducers are rarely highly efficient, thus the amount of available power on their output is typically measured in the range of milliwatts, microwatts or even nanowatts. Such small amounts of available power are imposing challenges in the design and implementation of EH powered systems. Furthermore, compared to batteries, availability of power is going to be varying depending on the amount of energy available for harvesting. In the case of solar harvesting, the light is not available during the night. Therefore, the electronics attached to the transducer needs to able to cope with the uncertainty of the power availability, unpredictable changes of the power levels and often the inability to predict the power levels even in the near future.

It should be stressed that energy harvesters are not a simple drop-in replacement for batteries. First of all, the output of the energy harvester can seldom be directly used by the off-the-shelf electronics. Therefore, a power management stage is required to convert the output of the harvester to a more appropriate form. The output of the power management stage is often insufficient to power the attached electronics, for example, a wireless sensor node, continuously. Therefore, the average power consumption of the node has to be reduced. The reduction of the power consumption of the node can be achieved by implementing low power modes of operation. If the power

consumption in the low power mode is lower than the power generated by the harvester, the excess energy can be stored in buffer storage. Once sufficient energy is accumulated, the node can be reactivated in order to perform the application specified task. As a result, the nodes operation has to be energy aware, meaning that it should adapt the execution based on the amount of the energy available. Therefore, the design and implementation of an energy harvesting powered system can be a very challenging task, especially in the cases where energy sources are scarce.

One aspect of the motivation behind the thesis was to develop an approach that would be used as a guide for navigating the complex design space of energy harvesting systems by pointing out different tradeoffs that need to be considered and steps that are required, in order to successfully implement an energy harvesting powered wireless sensor network node. Main focus has been on combining the currently available energy harvesting technologies with available off-the-shelf components into a working system.

Second aspect of this thesis was aimed at designing batteryless environmental monitoring systems that can operate with very low amounts of energy. The motivation for this work lies in the fact that slow changing parameters of the environment will not benefit from large number of measurements. For example, the indoor temperature of a typical building is not going to change in the matter of seconds. Therefore, measuring the temperature every second would only generate excess data. Similar can be argued for the changes of the outdoor and the indoor light levels, humidity levels, air pressure levels and similar environmental data. Other examples of slow changing parameters are temperature of lakes or other large water surfaces, corrosion development, and many more applications that exhibit changes in periods of minutes, hours, days or even weeks. Due to long periods between the measurements, even a scarce energy source, in the range of nanowatts and microwatts, would over time provide sufficient energy to perform the measurement and transmit the data. The question of why to use the energy harvester in such application can be raised. If the average discharge current of a battery is, for example, 100 nA, a typical CR2032 coin cell battery would, in theory, last for 262 years. However, this isn't practically feasible as their capacity and usability degrade after 5-10 years. Furthermore, the batteries capacity will vary with temperature and can be challenging to use in extreme conditions.

In order to overcome battery limitations, energy harvesting power source can be used instead. As only a small amount of power is required, a small or inefficient harvester can be used to power the system. The challenge in the designing such a low power system lies in utilizing the few microwatts and nanowatts of generated power because this power level is below the minimum operating power requirement of the majority of available off-the-shelf

components. The lack of available circuits for such a task motivated part of the research done in the thesis. As a result two circuits have been developed that allow the use of the harvesters that have a power output which was previously deemed insufficient to power environmental monitoring applications.

2. Context

This thesis is a result of a research project granted by the Danish Ministry of Science, Technology and Innovation. The project has been done as collaboration between the Technical University of Denmark and the company Danish Electronic Light and Acoustics DELTA (www.delata.dk). DELTA is a GTS institute[1] and a technology consultancy company. One of DELTA's roles in the market is to facilitate the transition of knowledge from the universities to the industry. Therefore, a part of the research was aimed at developing competences in the energy harvesting field that could be used by Danish small and medium sized companies as a basis for designing and implementing energy harvesting powered wireless sensor networks.

The targeted scenarios were wireless sensor network applications that require measurements to be performed once a minute or less frequent. These applications can be related to environmental monitoring tasks of slowly evolving phenomena. For example, humidity, temperature and light levels required in for building. Monitoring of greenhouses, soil humidity, CO and CO_2 levels, and other applications where high data rates are not required. Another possibility lies in the applications where the system is waiting for an event for longer periods of time allowing it to accumulate sufficient energy to be able to act promptly when the event occurs.

3. Research Objective

During this project I had two primary objectives. The first objective was to develop a guideline for designing energy harvesting powered wireless sensor nodes only using off-the-shelf components. As the energy harvesting systems are complex in nature, due to tight energy constrains a methodology is needed to guide the designer through all the stages of the wireless sensor node design. In the literature, there currently isn't an established methodology for performing this task using off-the-shelf components. The limitation to the use of off-the-shelf components was imposed due to the fact that manufacturing of application specific integrated circuits (ASIC) is expensive and tied with a need for larger production volumes. This is seldom the case with small and medium sized companies developing a product in a new, commercially unproven field,

[1] This is a type of private company that is awarded contracts by the Ministry of Science, Technology and Innovation to perform research and disseminate the resulting knowledge.

as was the case with the energy harvesting filed at the time of writing this thesis.

The second objective was to develop energy management circuits for energy harvesting that are capable of operating in nanowatt and microwatt ranges. This was important for three reasons. First, it would allow for the use of energy harvesters that are operating in conditions previously outside the useable range. Second, the design and implementation of an efficient transducer can be a complex task requiring large expertise in that field. Using circuits that can harvest even the smallest amounts of generated power allows the use of off-the-shelf energy harvesting transducers, with minimal modification, even outside their optimal operational envelope. Third, the size of the energy harvester can be reduced. The reduction of the minimum required power for the circuit to run would directly mean that a smaller energy harvester could be used.

The circuits developed during the fulfillment of the second objective are used as one of the building blocks that can be used when the applying the methodology developed as the first objective of the thesis.

4. Contribution

The contribution of the thesis can be divided into four parts. The first part is the methodology for designing and implementing the energy harvesting powered wireless sensor networks. The proposed methodology allows a systematic approach to designing and implementing an energy harvesting systems using off-the-shelf components. The methodology has been tested through applying it on two case studies. Chapter 5 reports on this methodology.

The second part of the contribution is design and implementation of circuits capable of collecting energy from nanowatt and microwatt power sources using off-the-shelf components. In order to reduce the energy management circuit's power consumption a novel approach has been suggested. The energy management realized using the proposed approach resulted in lower average current consumption compared to all reported state-of-the-art circuits realized using off-the-shelf components. Chapter 4 reports on the circuits.

The third part consists of general optimization techniques for reducing the power consumption of circuits in order to meet the tight energy budgets of energy harvesting applications. These techniques are covered in Chapter 5.

The fourth contribution lies in the comprehensive overview of different aspects of wireless sensor network nodes, done in Chapter 2 and energy harvesting transducers done in Chapter 3.

5. Publications

The following section will address the publications made during the course of the PhD studies. For each publication a short description of the contribution is presented

5.1. Published Journal Papers

- Dragan Avirovik, Ravi A. Kishore, Dushan Vuckovic, and Shashank Priya "Miniature Shape Memory Alloy Heat Engine for Powering Wireless Sensor Nodes", Journal of Energy Harvesting and Systems 2014.

  My contribution in this work was in designing and implementing an interface for collecting energy from a shape memory alloy based harvester.

- Journal paper: Ravi Anant Kishore, Dusan Vuckovic and Shashank Priya, "*Ultra-Low Wind Speed Piezoelectric Windmill*"

  My contribution in this work is with a method to improve the efficiency of the off the shelf power management circuit in order to efficiently harvest energy from a piezoelectric windmill.

5.2. Conferences

- Vuckovic D. "*Microcontroller-based Power Management for Nanowatt and Microwatt Energy Harvesters*", IEEE Sensors conference, November 2013, Baltimore, Maryland, USA

  The main contribution of this conference paper is in the description of the methodology behind the ADC energy management circuit presented in the Chapter 4.4. Also this paper addresses the implementation of the ultra-low power wireless sensor node used as a part of the first case study presented in Chapter 5.

- Vuckovic. D, "*Low Leakage Power Management Module For Sub-microwatt Energy Harvesting Applications*", 7th Annual Energy Harvesting Workshop / 2nd Annual CEHMS Conference, August 2012, Blacksburg, Virginia, USA

  Main contribution of this work was design and implementation of the Nanowatt Voltage Detector circuit presented in Chapter 4.3.

- Vuckovic, D. "*Microwatt energy harvesting and use of environmental trigger for wireless sensor node activation*", IWPMA 2012 Conference, April 2012, Hirosaki, Japan

  Main contribution of this work lied in design and implementation of the early version of the nanowatt energy harvesting energy management circuit. This work evolved into the circuit described in Chapter 4.3. This work also demonstrated early ideas of utilizing environmental events, rain in this instance, for activation of the communication in the wireless sensor network.

- Henckel, J.T.; Sørensen, T, Vuckovic, D.,"*Powering Sensor Node using Macro Fiber Composite*", IWPMA 2011 Conference and the 6th Annual Energy Harvesting Workshop, August 2011, Virginia

  Main contribution in this work was on designing and implementing a piezoelectric energy harvester for collecting the energy of wind using a cantilever structure. This work evaluated the possibilities of using a Macro Fiber Composite material for harvesting irregular oscillations induced by the wind.

5.3. Workshops and Poster Presentations

- Fafoutis, Xenofon and Vuckovic, Dusan and Di Mauro, Alessio and Dragoni, Nicola and Madsen, Jan,"*Energy-Harvesting Wireless Sensor*", *9th European Conference on Wireless Sensor Networks EWSN 2012,* February 2012, Trento, Italy

  My contribution in this poster was providing an overview of the field of energy harvesting wireless sensor networks

5.4. Papers in Review

- Journal paper: Anthony Marin,, Ravi Kishore,, Darian A. Schaab, Dusan Vuckovic and Shashank Priya,"*Micro Wind Turbine for Powering Wireless Sensor Nodes*"

  My contribution is in this paper is in novel energy management circuit designed for fast activation of the load using a small primary buffer capacitor, followed by mechanics for efficient storing of excess energy in a secondary buffer capacitor. The knowledge gained from work on this project was used in realizing the energy management for the second case study presented in Chapter 5.

6. Structure

The thesis is laid out in a way that follows a top down approach to system design. After the introduction the wireless sensor network concepts is examined in Chapter 2. This chapter is covering all major parts of an energy harvesting powered wireless sensor node: microcontrollers, sensors, memory, radio and communication. A short review of different programming techniques is also presented. Chapter 3 is aimed at introducing the different types of energy harvesters as well as methods for interfacing the harvesters to the rest of the circuitry, maximizing the power output of the harvester and storing the generated energy. Chapter 4 is covering the design and implementation of nanowatt and microwatt harvesting circuits and is the first of the two main contribution chapters. Chapter 5 is aimed at rounding up all the parts and concepts discussed in previous chapters and propose a design methodology for combining them in a sustainable energy harvesting powered wireless sensor node. Two case studies are examined in the chapter, which are utilizing the proposed methodology. During the design and implementation of the case studies several novel circuits for energy management have been designed and implemented which could be extended for use in other applications. Finally, Chapter 6 gives a general conclusion and directions for future work.

Chapter 2

Wireless Sensor Networks

1. Introduction

The autonomous wireless devices used for collecting information on various physical phenomena are usually referred to as wireless sensor networks (WSN). A wireless sensor network is consisting of one or more data collectors (sinks, base stations) and a number of measurement units that collect the data (nodes). The nodes can communicate over the wireless link among themselves and the base station. The goal of the network is to generate the data of interest and propagate the data to the collection point.

The possibility to communicate wirelessly, hence removing the need for wires, makes WSNs an attractive solution for a variety of monitoring tasks. With the advancements in low power electronics the WSNs could, for a wide variety of applications, be deployed for long periods of time without a need for any type of maintenance and on-site intervention. The WSN has a distinct advantage over a data logger that the system can be left deployed removing the need for revisiting the deployment site.

In [108] a survey of wireless sensor networks was performed demonstrating the various possibilities in environmental monitoring. Various research groups have demonstrated the advantages of using the WSN's for monitoring climate changes, changes of the indoor environment, greenhouses, monitoring of domesticated animals and wildlife [97]. Pollution monitoring is rising in interest especially for use in developing countries. There has also been reported research in the field of forest fire detection and monitoring. WSNs could be beneficial for use in hostile conditions, for example, in a volcano or glacier monitoring [177]. In agriculture, WSNs can be used for monitoring the soil moisture and temperature as an input for an automated irrigation system [105]. Monitoring of environmental conditions in underground mines has been explored in [91] where the goal was collecting environmental data and detecting collapses inside a mine shaft.

The need for optimized use of energy in buildings has led to increased interest in home automation and monitoring. Analysis done in [38] indicates that if current trends of power consumption continue by 2025., buildings will be consuming more than transportation and industry sector combined. It stresses out the requirement for smart power metering and proposes a wireless solution for easy installation and use.

Besides environmental monitoring, a large interest in recent years has been in the structural health and system usage monitoring. Structural and system usage monitoring provide a possibility to detect defects before they lead to failures. For an example, in [111] a 64 battery powered sensor node network was deployed on the Golden Gate Bridge to monitor the stress and vibrations. Furthermore, structural monitoring provides information on the health of the devices hence avoiding the need for scheduled maintenance if there is no need for it, thus reducing the maintenance costs.

Wireless sensor networks have found their application also in the domain of tracking of goods. In [128] a WSN was developed to monitor the change of conditions in transport of fruits in the cold chain supply. In the domain of tracking and detection, the WSNs have found an application in border control. In [11] a WSN has been envisioned that will monitor the border between the USA and Mexico by detecting and identifying object that are moving through the area.

Development of WSNs has also a major impact on the implementation of the "Internet of Things" paradigm [12]. The "Internet of Things" is based around a concept that various objects can be uniquely addressed in a way that will allow them to interact with one another in order to reach a common goal. It is easy to see that a WSN will have a major role in this paradigm as it will provide means for wireless connectivity of various objects.

However, the major limiting factor of the WSN implementation is the available energy for its operation when it is powered from batteries. Therefore,

their lifetime is limited by the available energy stored in the batteries. In order to expand the potential of the WSNs it was necessary to extend the lifetime of batteries. One solution was introducing energy harvesting.

The energy harvesting is aimed at collecting available energy in the environment such as waste heat, radio waves, diffused indoor light, vibrations, into an electric power source capable of running low power electronics. The advancements in low power electronics, developments of new transducer materials and approaches to convert energy to electrical power, allowed for fast rise in number of applications that are energy harvesting powered.

In [109, 103] various structural monitoring energy harvesting concepts have been demonstrated. These concepts are relying on harvesting the energy from vibration induced by the structure monitored, or fluid flow, in order to generate electric power. The power is then used for the electronics that is measuring the condition of the structure and wirelessly reporting on it. In [131] it was argued that a potential to predict maintenance on the windmill farms could potentially save approximately \$2 - 3 billion dollars annually in the USA alone. The authors of this work demonstrated an energy harvester that uses the vibrations of the windmill wing to power the wireless sensor node. Their approach is based on a network of wireless sensor nodes located on critical points on a wing blade monitoring for irregularities in the structure.

Another example of monitoring materials under high stress is monitoring the rotor head of the helicopter. This application was implemented by the company MicroStrain using ceramic PZT patches as energy harvesting elements [10]. In buildings it is possible to monitor the corrosion of the reinforcement inside concrete blocks using environmental energy as demonstrated in [147].

With the development of new materials, new energy harvesting approaches continue to emerge. In [164] magnetic shape memory alloys had been used to transduce the vibrations of the bridge into electrical energy used by a sensor node to monitoring the structural integrity of the bridge.

Beside structural monitoring and industrial applications, the solar powered systems have found an implementation potential in agriculture. A wireless sensor network for monitoring olive trees has been designed and implemented in [76], while a sensor network monitoring soil moisture is presented in [104]. Another application of solar powered node was found in monitoring of aquatic wild life [8].

The implementation of all these applications is based on realization of energy harvesting powered wireless sensor network (EH-WSN) nodes. The rest of this chapter will focus on the structure of a wireless sensor node and different technologies required for its realization. First the structure of the sensor node is explained in detail followed by sections covering critical parts of the structure. The focus will be on overview of different technologies and

components that will allow a successful implementation of an energy harvesting powered wireless sensor node (EH-WSN).

2. Structure of a Wireless Sensor Node

The WSN node is aimed at performing a measurement of physical phenomena using one or more sensors and relaying the information to the base station at an application defined sampling rate. The wireless sensor network node consists of four main blocks: the power supply, the sensor, the controller and the communication block. In a case of energy harvesting powered wireless sensor network node (EH-WSN) the power supply block can be divided into smaller segments: the energy harvester, the power management, the energy management and the storage. The block diagram of a typical energy harvesting powered wireless sensor node is presented in Fig. 2.1.

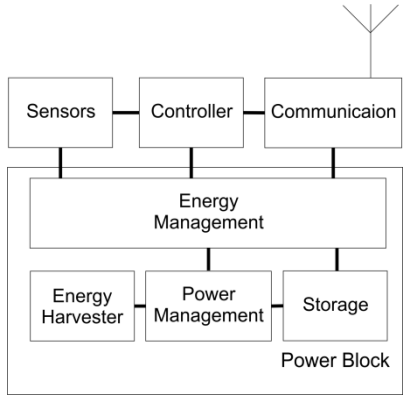


Fig. 2.1 The block diagram of an EH-WSN node

Typically energy harvesting power sources cannot provide sufficient power for continuous operation of all components on the node. Therefore, it is necessary to select low power components and control the activity of these components as well. By disabling the elements of the node that are not used and utilizing low power features of the controller and the sensor blocks, it is possible to reduce the power consumption of the entire node below the average power produced by the energy harvester.

While the components are kept in low power regime the energy is being accumulated from the energy harvester. Upon collecting enough energy to perform the task required by the application, the components are activated.

Following subsections will define each block's function in detail following the low power requirements imposed by the nature of the node's operation in mind.

2.1. The Energy Harvester Block

This block consists of one or more energy harvesting transducers. The aim of this block is to convert the environmental energy into electrical energy.

The energy harvesting transducers that have gotten the most research attention so far are the ones converting light energy, kinetic energy and waste heat energy to electrical energy. Photovoltaics have been the most typical approach to converting the light energy to electrical energy. In the case of kinetic energy harvesters the field has been dominated by piezoelectric, electromagnetic and electrostatic harvesters. The waste heat can be converted to electrical energy using thermoelectric generators. The development of new materials and approaches in energy conversion is constantly increasing the number of possible harvesting approaches extending the field of applications. Different types of energy harvesting transducers are going to be covered in Chapter 3.

2.2. The Power Management

The power management stage has two main tasks. The first is to maximize the power output of the harvester and second is adjusting the output of the energy harvester to meet the input requirements of the system powered by the harvester.

The output of different energy harvesters can vary in both voltage and current levels. For example, the output of a thermoelectric generator exposed to thermal differences of several degrees has a DC output with a voltage level in the order of millivolts. On the other hand, the output of the piezoelectric generator is an AC signal that can be in the order of volts or even tens of volts while the impedance of the output is in kilo-ohms or mega-ohms. Therefore, the power management stage has to convert the output signal of the harvester to a DC voltage in the range of 1.8V to 3.6V, which is the voltage typically used by the off the shelf sensors, microcontrollers and transceivers.

It is important to maximize of the available output of the harvester as the amount of power available is already limited. This can be done by matching the input impedance of the power management stage with the output impedance of the harvester. When this is achieved maximum energy is being transferred from the harvester to the power management stage. This operating point of the maximum power transfer is commonly referred to as maximum power point (MPP).

The impedance matching is typically done by implementing a switch based DC/DC converter which can be either capacitor or inductor based. By changing the operating characteristics of the DC/DC converter it is possible to adjust the input impedance of the power management stage, hence match it to the output of the harvester [151]. It should be pointed out that the output

power of the energy harvester is varying together with the availability of the energy in the environment. The change of the energy output is followed by a change in the maximum power point location. Therefore, in order to continue operating at the maximum power point the operation of the power management needs to be adjusted. The operation of adjusting the input impedance of the power management so it follows the maximum power point of the harvester is referred to as Maximum Power Point Tracking (MPPT).

However, controlling the power management stage to operate at the maximum power point and subsequent tracking of its change comes at an increased power consumption of the power management stage. This is very important to be aware of, as in ultra-low power applications the power required by the MPPT might be higher than the power gain obtained by using the MPPT [28].

The implementation of MPP and MPPT, as well as maximizing the power output of the harvester, depend on the type of harvester used. Chapter 3 will address the most common circuits used with different energy harvesters.

2.3. The Storage Block

The power output of the majority of energy harvesters can't provide sufficient power for a continuous operation of the wireless sensor node. Therefore, it is necessary to buffer the energy in an intermediate storage and run the node once sufficient energy is accumulated. This allows compensation for the varying power output of the harvester and provide a stable energy source for the rest of the circuitry to use.

Typically storages used are capacitors and batteries. The benefits and drawbacks of different storage types will be addressed in more detail in Section 3.5 of this chapter. The choice of the storage is going to be primarily driven by the application parameters such as the energy availability, the level of activity, the operating temperature conditions, size, lifetime, price, etc. The choice of the storage for a specific application is described in Chapter 5.

2.4. The Energy Management Stage

The goal of the energy management stage is to manage the output of the power management stage and provide mechanics for efficient use of the energy stored in the buffer storage. The energy management can be divided into software and a hardware part.

In battery storage systems the hardware aspect of energy management stage is usually reduced to battery management. This includes the battery under-voltage and over-voltage protection and interface between the battery and the rest of the electronics it is supposed to power [73, 28].

In the case of capacitor based systems the most important task of the energy management block is to prevent the elements outside the power block from activating until the capacitor has accumulated sufficient energy. This is necessary as integrated circuits can have unpredicted behavior when operated at voltage levels under their minimum specified voltage level. Then they demonstrate an increased power consumption that could potentially be larger than the power generated by the harvester [138].

In systems where both storage elements are present the energy management has a more complex task. It needs to select which storage should be used based on the actual output of the harvester, state of the battery and state of the buffer capacitors. It also needs to arbitrate the charging process of the battery in order to extend its lifetime [78].

Besides the hardware part of the energy management, special algorithms are usually realized inside of the controller section in order to optimize the use of the available energy. The software is designed to be energy aware, in other words, its operation is driven by the amount of energy available [16]. The energy-aware operation is discussed in Section 5. of this chapter.

2.5. The Controller

The controller block is used to manage all sensor and communication related tasks. Typically for this purpose a low power microcontroller is used. This thesis will be focused on wireless sensor nodes that are controlled by microcontrollers. However, there are implementations that are not based around the microcontroller.

In [79] the data transmitted is generated by an oscillator that is changing its frequency depending on the change of the sensor's capacitance. The change of frequency of the oscillator is then transmitted as a measurement value by modulating the signal. Similar approach was used in [138]. These wireless sensor nodes are simpler and cheaper compared to devices that are based around a microcontroller hence making them attractive for mass production. However, implementations without microcontrollers are application specific, inflexible, and have a limited amount of sensors that can be used.

2.6. The Communication

The biggest difference between the data logging and a wireless sensor node is the nodes capability of relaying the collected data to a remote location without the need of visiting the measurement site. The data transfer is typically performed using radio waves. This has been a predominant way of the data transfer due to low energy requirement, early standardization and low cost. Furthermore there are various receiver, transmitter and transceiver integrated circuits and modules available on the market allowing a fast and

easy implementation of wireless communication into applications. Some modules remove a need for any in depth knowledge of the physical concepts of wireless communication hence allowing the designer to focus on higher levels of communication.

Apart from using radio waves for communication different communication options are also possible in WSN. Optical communication has been demonstrated as an option in energy harvesting wireless sensor networks [165]. Research has been done in the field of ultrasonic communication as well. Ultrasonic communication brings several advantages over radio based communication. It doesn't interfere with other electronic devices and it has better security for indoor networks as the signal would be hard to detect outside a room preventing long range eavesdropping [77]. Furthermore, it can be used in underwater wireless sensor networks [20].

2.7. The Sensor

The sensor block has the task of translating the information from the monitored environmental phenomena or events into electrical signals that can be interpreted by the rest of the electronics, processed and sent over the wireless link. Recent developments in low power sensing techniques are the one of the main enabling parameters for implementation of WSNs beside the radio and the controller. Different sensor types are going to be discussed in the Section 3.4.

3. Devices and Peripherals for Low Power EH-WSN Nodes

In order to realize an energy harvesting powered wireless sensor node it is necessary to choose components that would operate efficiently in the regime that is expected from the node. As mentioned earlier, the microcontroller and sensors are going to spend majority of the time in low power sleep mode while the energy is being accumulated. They will be activated periodically, or whenever there is sufficient energy to perform the required task. This section will focus on review of available technologies and off the shelf components for implementing energy harvesting powered wireless sensor networks.

3.1. The Microcontroller

The microcontroller represents the main control unit of the wireless sensor node. It controls the activity periods, the data collection from the sensor and wireless data transmission, and other application specific tasks. The most important characteristics of the microcontroller that is aimed at EH-WSN node applications are:

- The characteristics of the low power regimes
- Availability of the peripheral modules on the MCU

These main characteristics are going to be addressed in detail followed by an overview of microcontrollers typically used in WSN applications.

As the microcontroller is typically powered throughout the operation of the node it is important that the MCU features a low power "sleep" mode in which the core of the MCU is not running and some peripherals are unpowered. The microcontrollers used for wireless sensors networks are low power microcontrollers that feature sleep currents in the order of $<1\mu A$. The main contributor of the sleep power consumption is RAM memory of the microcontroller. The RAM is maintained so the MCU can continue execution once the wake-up signal is received. There are some microcontrollers, for example, the EFM32 series of microcontrollers from SiliconLabs [86], that can remove the power from the RAM. However, after receiving a signal for returning to operating mode these microcontrollers start software execution from the first instruction, similar result to restating the MCU. Recent studies have shown a new approach to designing non-volatile microcontrollers that are not losing the RAM content when the supply is removed, thus reducing the sleep current close to 0A [15]. This type of microcontroller would be attractive for use in energy harvesting systems as its state wouldn't be lost due to loss of power.

The next important feature of a microcontroller are the different power modes it could potentially enter in order to reduce the power consumption during execution. The goal of the low power mode is to disable the MCU core hence providing large energy savings while keeping peripherals active. In this way the core can set a task to a peripheral and then be turned off while waiting for the peripheral to complete the task. The Texas Instruments MSP430 series of microcontrollers have five low-power modes [74]; SiliconLabs EFM32 [86] series of microcontrollers have 4 low power energy modes available. The power modes are selected depending on which peripheral is required.

An important characteristic of a microcontroller used in WSNs is the number of peripheral modules that are available on the MCU and their characteristics. Two most important peripherals for the WSN applications are the Analogue to Digital converter (ADC) and hardware support for different types of serial communication. These two peripheral modules are mainly responsible for interfacing the MCU to the radio and various sensors sensor.

A careful selection of a microcontroller can potentially simplify the entire node design. For example, instead of implementing an amplifier section between an analogue sensor output and a microcontroller ADC input it is possible to use a microcontroller that has a higher resolution ADC converter. The MSP430AFE series of microcontrollers by Texas Instruments [72] are

ultra-low power microcontrollers with an integrated 24-bit sigma delta ADC with selectable gain. This means that ideally at 3 V supply the maximum resolution of the ADC would be 60 nV while in case of 10-bit and 12-bit ADCs, which that is more common among MCUs, the maximum resolution would be 3 mV and 0.732 mV respectively. As a result voltage levels that are 50 000 times smaller could be detected by MSP430AFE compared to a microcontroller with 10-bit resolution.

In cases where there are multiple peripherals that are required to interface over serial communication it is beneficial to select a microcontroller with a larger number of serial hardware modules. It should be noted here that different manufactures have a different approach to realizing serial communication modules. In the case of MSP430 the serial communication hardware module can be switched between I^2C, SPI and UART operation, while on PIC microcontrollers SPI and I^2C are shared by the same module while the UART has a dedicated hardware module.

Typical microcontrollers found in literature are mainly 8-bit and 16-bit architectures coming from the PIC series of Microchip microcontrollers, TI's MSP430 series and AVR's ATMega series. The TI MSP430 series has been mostly predominant in the research communities mainly due to the popularity of several platforms that have been built around it, for example, Telos motes. Different platforms will be discussed in more details later in the chapter.

The advancements in microcontroller manufacturing have allowed for development of low power 32-bit platforms that are targeted as a replacement for 8-bit and 16-bit MCUs. In [115] it was demonstrated that the new ARM Cortex M series processors are executing code more efficient, have smaller code and are overall more power efficient compared to ARM7, MSP430 and ATMega128 microcontrollers.

However, as the cores are running at higher frequency they require higher power consumption when operating, therefore, it is necessary to keep the core of the MCU, which is the main contributor to the power consumption, disabled as long as possible while relying mainly on the onboard peripherals to perform the tasks. The EFM32 series of 32-bit microcontrollers has been specially designed with that in mind. These microcontrollers can, for example, perform analogue to digital conversions with storing the data in the RAM using the onboard DMA at regular time intervals without activating core at any point. This is done using a proprietary Peripheral Reflex System (PRS) [86] that allows the peripherals to signal beginning and end of tasks among themselves allowing the system to operate without starting the core. Similar peripheral interconnecting mechanism has been demonstrated in the nRF51 microcontroller from Nordic Semiconductor [133] that is built around an ARM-Cortex M0 core as well as Cortex M series of microcontrollers by AVR.

The structure of an EFM32 Tiny Gecko series of microcontrollers is shown in Fig. 2.2. This figure also demonstrates the peripherals available on the chip and their interconnections.

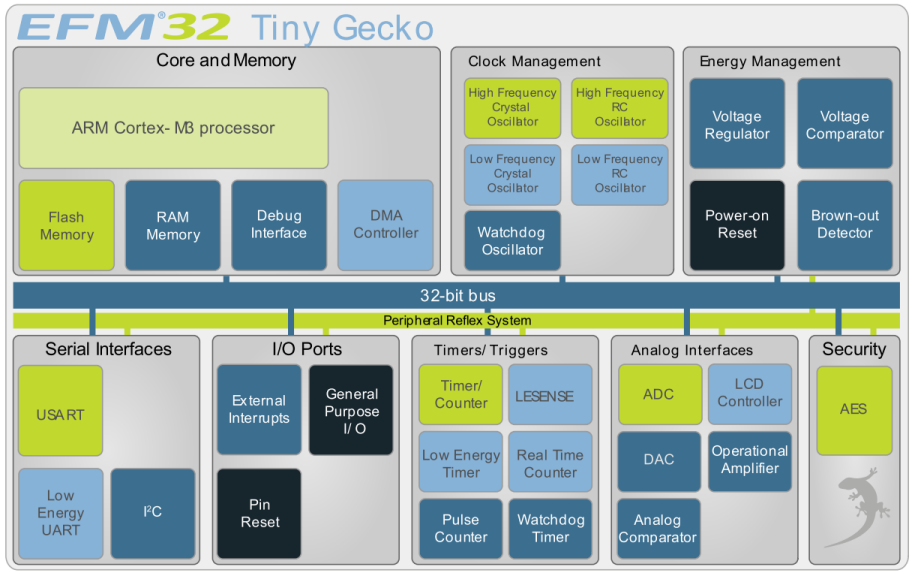


Fig. 2.2 Block diagram of an EFM32TG microcontroller [86]

Almost all big microcontroller manufacturers have come forward with their version of 32-bit microcontrollers targeted for potentially replacing 8-bit and 16-bit microcontrollers. The NXPs LPC Cortex M0+ and M3 series of microcontrollers and Freescale Semiconductor Kinetis series are some of the examples. However, for some applications the 8-bit and 16-bit microcontrollers can still be more energy efficient. This has been demonstrated in the microcontroller profiling section in Chapter 4.

3.2. The Transceiver

The second key element of a wireless sensor node is the radio. Currently on the market there is a large array of wireless modules that are designed to be interfaced with a microcontroller typically over an SPI bus. The availability of the radio modules and integrated solutions that only require filtering capacitors and an antenna matching network are drastically simplifying the design process of the wireless section of a WSN node. The company Johanson Semiconductors is manufacturing complete solutions for antenna matching networks as a single passive component further simplifying the wireless section and reducing the overall PCB footprint.

Depending on the carrier frequency of the radio signal that is used for communication the radio modules can be divided into two main categories:

- Sub-gigahertz radio modules (sub-GHz)
- 2.4GHz radio modules

3.2.1. Sub-gigahertz Radio Modules

The modules in the sub-gigahertz range are typically used for low bandwidth communication on baud rates of up to 500 kbps. Although not rated at the smallest energy consumption per bit of transmitted data, these modules have range that is several times longer than 2.4 GHz radios for the same power output due to lower frequency of operation. The superior range is a direct consequence of longer wavelength of the sub-GHz wave. However, this comes at a price of larger antenna requirement.

The extended range makes the sub-GHz range attractive for networks that are supposed to cover larger areas fewer number of hops. With a range of 100 m this frequency is better suited for outdoor environmental monitoring compared to 2.4 GHz networks that have a range of up to 30 m for the same wireless link budget. In the applications aimed at outdoor environmental monitoring longer range of sub-GHz radios is beneficial. Furthermore, there is less interference in sub-GHz range due to fewer devices currently operating in that frequency band.

The biggest drawback of operating in sub-GHz range is the lack of worldwide standard. Different countries have different standards about which frequency band in the sub-GHz range can be used for unlicensed communication. Another drawback of the sub-GHz radios is data rate compared to the 2.4 GHz radios.

In the EU, following the decision numbered 2005/928/EU, the frequency of 169 MHz band was relocated to the ISM band, hence becoming available for unlicensed use. This will allow achieving even longer ranges on the same energy budget due to lower frequency. The increased penetration properties of longer waves are especially important in industries where large machinery might be in the way of signal propagation.

Some of the most popular sub-GHz radio modules found in literature and their power consumption are summarized in Table 2.1.

Table 2.1 Properties of sub-GHz transceivers used in literature. The characteristics are obtained from devices' datasheets

Device Name	*Manufacturer*	*Operating frequency range*	*TX current*	*Rx current*	*Max. data rate*
CC1200	Texas Instruments	164 – 190 MHz 410 – 475 MHz 820 – 850 MHz	36 mA@ +10dBm	23.5 mA 2 mA – wake on radio	1250 kbps
CC1101	Texas Instruments	300 – 348 MHz 387 – 464 MHz 779 – 928 MHz	15 mA @ 0dBm	14.7mA	500 kBaud
Si4421	Silicon Labs	430 – 439 MHz 860 – 879 MHz 900 – 929 MHz	16 mA @ 0dBm	14 mA	256 kbps
MRF89XA	Microchip	863–870 MHZ 902–928 MHz 950–960 MHz	16 mA @ +1dBm	3 mA	200 kbps
SX1211	Semtech	863–870 MHZ 902–928 MHz 950–960 MHz	16 mA @ +1dBm	3 mA	100 kbps

3.2.2. 2.4 GHz Radio Modules

The worldwide availability of the 2.4 GHz frequency made it possible to build worldwide standards on it. This lead to the production of dedicated integrated circuits that would support that frequency and even incorporate entire protocol stacks inside. Standards will be discussed later in this chapter. The focus of this section will be on the radio modules. Besides worldwide availability the advantage of the 2.4 GHz frequency radio over the sub-GHz one is the high throughput. At 2.4 GHz the WiFi can stream data at rates of up to 11 MBps. Even low power radios can reach bit rates of 2 MBps drastically reducing the time transmitter and receivers are active and thus reducing the overall energy consumption per transmitted bit.

One of the drawbacks of 2.4 GHz radios is reduced range due to high absorption of the waves in indoor environments and by human body.

Another drawback is the fact that there are a lot of devices operating in this frequency range resulting in possible interferences between systems when they are operating in close proximity. In order to overcome this problem some standards are using spread spectrum techniques in order to spread the energy of the signal over a larger frequency range hence making it more immune to noise and interference. Other approaches use frequency hopping where the communication is continuously changing the channel it is operating at. In this scenario if one channel is occupied the operating frequency will change with the next hop reestablishing the communication.

Some of the most popular radio integrated circuits found in literature with their power consumptions are summarized in the Table 2.2.

Table 2.2 Characteristics of commonly used radio modules in literature. Characteristics were obtained from the devices' datasheets

Device Name	*Manufacturer*	*TX current*	*Rx current*	*Data rate*	*Supported Standard*
CC2420	Texas Instruments	17.4 mA @ 0dBm	18.8mA	250 kbps	ZigBee/IEEE 802.15.4
CC2541s	Texas Instruments	17.9 mA @ 0dBm	18.2mA	1 Mbps	Proprietary Bluetooth LE
Nrf24L01+	Nordic Semiconductor	11.3mA @ 0dBm	12.3mA	2 Mbps	Proprietary
CC2500	Texas Instruments	21.2mA @ 0dBm	13.3mA	500 kbps	Proprietary
CC2520	Texas Instruments	25.8 mA @ 0dBm 33.6 mA @ 5dBm	18.5mA	250 kbps	ZigBee/IEEE 802.15.4

From the Table 2.2 it can be seen that some modules are noted to support different standards. This means that the radio modules have integrated controllers that are taking care of the protocol stack hence simplifying the operation of the main controller in the system. Different standards and protocols are going to be addressed in wireless section of this chapter.

It should be noted that the nRF24L01+ module has demonstrated the most power efficient operation. It was measured that the energy required for transmission of an 8 byte packet using 2 Mbps data link followed by an acknowledgement of the packet required only 10 µJ of energy. This feature makes the nRF24L01+ a good candidate for short range energy harvesting applications that are energy constrained.

3.3. System on Chip – Microcontroller and Transceiver

In order to minimize the size of the system, power consumption and reduce the overall price some manufacturers have stated combining the radio and a microcontroller together on a chip. In majority of cases these are hybrid chips that have the radio core and a microcontroller core on the same die connected using a bus.

Typically the MCU and the radio are two separate hardware blocks with their own separate memories. This means that the communication between the MCU and the radio is very similar to having an external radio module. From a software development stand point this is beneficial as changing from a system with external radio to an internal one is just the matter of writing to different communication registers. However, from the hardware optimization stand point the gain can be marginal and depends on the system implementation. In order

to achieve higher performance and lower power consumption the radio module and the MCU should share the same memory space. In this way there is no need for transferring packets between the radio and the MCU over the bus hence increasing the efficiency of the system.

A survey of different systems on chips is given in Table 2.3.

Table 2.3. Typical characteristics of commonly used System-On-Chip microcontrollers. Characteristics are obtained from the devices' datasheets

Device Name	*Manufacturer*	*Embedded MCU*	*Radio freq.*	*TX current*	*Rx current*	*Data rate*	*Supported standard*
CC2538	Texas Instruments	ARM Cortex M3	2.4 GHz	24mA @ 0dBm	24mA	250kbps	IEEE 802.15.4, ZigBee, 6LoWPAN
CC2533	Texas Instruments	8051	2.4 GHz	28mA@ 0dBm	25mA	250kbps	IEEE 802.15.4, ZigBee, RF4CE
CC430Fx1xx	Texas Instruments	MSP430	Same as CC1101	16mA	15mA	500kBaud	Proprietary
CC2540/1	Texas Instruments	8051	2.4 GHz	18.2 mA @ 0dBm	17.9mA	2 Mbps	Proprietary Bluetooth LE
Nrf51422	Nordic Semiconductors	ARM Cortex M0	2.4 GHz	10 mA	13 mA	2 Mbps	Proprietary ANT
Nrf51822	Nordic Semiconductors	ARM Cortex M0	2.4 GHz	10.5mA	13mA	2 Mbps	Bluetooth LE Proprietary
LTC5800-IPM	Linear Technology	ARM Cortex M3	2.4 GHz	5.4mA @ 0dBm	4.5mA	250kbps	6LoWPAN IEEE 802.15.4e
STM300	EnOcean	8051	868 MHz 315 MHZ 902 MHz	24mA @ +6dBm	27.4mA	125 kbps	Proprietary
EM35x	Silicon Labs	ARM Cortex M3	2.4GHz	31mA @ +3dBm	25mA	250kbps	IEEE 802.15.4
Si1000/1/2/3/4 /5	Silicon Labs	8051	240-960 MHz	18mA @ +1dBm	18.5mA	256kbps	Proprietary

A distinctively lower current consumption of the LTC5800 module from Linear Technology can be observed from the Table 2.2. This is the first product that is utilizing a new, lower power, generation of radios that were entering the market during the writing of the thesis. This advancement in radio module technology would reduce the power consumption of the radio stage by at least 50% making a significant impact on the average power consumption of the entire wireless sensor node.

The STM300 system-on-chip module from EnOcean was the first commercially available module build specifically for energy harvesting powered wireless sensor networks. The module incorporates specially designed energy and power management hardware that allows the system to be powered from different types of energy harvesting power sources [55].

3.4. Sensors and Peripherals

The third most important part aspect of the wireless sensor node is selection of sensors and other onboard peripherals. The peripherals are usually additional ADCs, memories, low power Real Time Clocks (RTCs) or other application specific components. The most critical elements are the sensors. Memories are usually used in order to buffer the data before transmission and provide a mechanic for data logging where there isn't sufficient energy for transmitting the data.

3.4.1. Nonvolatile Memories for EH-WSNs

An external non-volatile memory is used on a sensor node for storing various calibration data, different node specific settings and measurement data between transmissions. The most widespread types of nonvolatile memories used are the flash and EEPROM memories. The flash memories are dominant on the market due to their high endurance high speed and large capacitance at low price. The flash memory is considered a block write memory. It is designed to be written in block rather than addressing every individual byte. This can be considered a drawback if the data that needs to be written is aimed at overwriting only a few bytes. For data logging features, where every next measurement is written in next memory space updating the flash isn't a problem. The issue arises when the same memory location needs to be updated. In flash memories this means moving all data from the block into a temporary buffer, erasing the entire block, updating the value and writing the block back into the memory. Furthermore there is a delay between the writing command is issued and the writing is done. For example, in the case of AT45DB011D this delay can be up to 4ms for 256 bytes [152].

Due to its drawbacks the energy requirement for writing to the flash can be too high for energy harvesting powered devices. The new nonvolatile memory technologies like Magnetoresistive RAM (MRAM), Ferromagnetic RAM (FRAM) could be a solution to this problem. These memories are smaller in capacity and come at a higher price point. However, they have lower power consumption. At the time of writing currently available FRAM memories on the market are in the range of 4Kb to 8Mb, while MRAM memories are in the range of 256kb to 16Mb, which is considerably smaller compared to flash chips that were available with memory capacity in orders of 100 GB. However, the biggest advantage of MRAM and FRAM memories is possibility to write to single bytes in memory, hence no need for block erases. Another important parameter is lack of delay when performing writing of data to the memory.

The second important benefit of MRAM and FRAM is high endurance. The FRAM chips are rated to 10^{14} erase/write cycles while MRAM supports an unlimited number of erase/write cycles. This is a substantial advancement over the current commercial flash chips that can withstand 10^5 erase/write cycles.

Another technology that is falls in between the MRAM, FRAM and flash is the phase change memory (PCM). This technology allows larger storage capacities compared to MRAM and FRAM, however, it can endure a significantly lower number of write cycles. The data is stored by changing the structure of the chalcogenide glass from amorphous to crystalline and hence changing its resistive properties. The write time of PCM is significantly shorter than of the flash memory, however, comes with a higher current requirement. The benefit of PCM is that is byte addressable. These memories are new on the market and have a large potential for substituting flash memory in the future [26].

The comparison of different off the shelf nonvolatile memory integrated circuits are presented in Table 2.4.

Table 2.4. Comparison of different off the shelf nonvolatile memory chips

Device Name	*Manufacturer*	*Memory type*	*Capacity*	*Write Current max. (mA)*	*Read Current max. (mA)*	*Write delay*	*Write Endurance*	*Price per unit*[1]
M25P10-A	Numonyx	Flash	1Mb	15	4 @ 20MHz	5ms	$10^4 - 10^5$	0.6
AT45DB011	Adesto Technologies	Flash	1Mb	20	10@ 20MHz	4ms	10^5	0.6
FM24V10	Cypress	FRAM	1Mb	0.3 @ 1MHz 1.3 @ 40 MHz	0.3 @ 1MHz 1.3@ 40MHz	0ms	10^{14}	10
MR25H10	Everspin Technologies	MRAM	1Mb	13@1MHz 27@40MHz	3@1MHz 10@40MHz	0ms	Unlimited	9
NP5Q128A	Micron Technologies	PCM	128M	50	7@33MHz 16@66MHz	360µs	10^6	5

[1]) USD price for a single unit obtained from Digi-Key website (www.digikey.com) at the time of writing
Note: values are obtained from the devices' datasheets

3.4.2. Sensors for EH-WSN

Wireless sensor networks are deployed with a goal to monitor and detect some phenomena and produce an electronic signal that will correspondent to the state or change of the sensed object or phenomena. The sensors can be divided based on their output and the approach of performing the measurement. The output of sensors the sensors can be analogue or digital, while the measurement techniques they can be divided into active and passive sensors.

Analogue vs Digital Output

Analogue sensors have a varying voltage output that is correlated to the physical properties of the sensed characteristic. These sensors can consist only of a transducer element, for example, a photodiode, thermistor or thermocouple. In some cases they incorporate some additional electronics to

condition the signal coming from the transducer. For example, accelerometers with analogue outputs, the Hall effect sensors etc.

Digital sensors are usually analogue transducers coupled with additional electronics that processes the output signal of the transducer and transmits it over a communication line of some sort. These sensors are usually equipped with high resolution analogue to digital converters reducing the need for a high resolution ADC outside the sensor. Embedding the processing electronics close to the transducer reduces the noise pick up and interference, thus providing better precision and accuracy. Some sensors have integrated controllers allowing different types of calibration, self-calibration, and self-monitoring, special modules for improving the linearity of the output and any other necessary processing of the transducer output.

The motion processing algorithms processing the data from accelerometer, gyroscope and compass are computationally heavy when performed on a general purpose microcontroller. In order to keep the power consumption of the system low, the company IvenSense developed a 9 degree of freedom motion sensor, MPU-9250 [64], that is equipped with a Digital Motion Processor which processes the measured data instead of the host controller. This offloads the computational tasks from the host controller, where it would be done less efficiently, thus allowing reduction of the overall power consumption.

The choice of digital or analogue sensor is dependent on the targeted price, precision and complexity of the node to be designed. The digital sensors do not necessarily consume less power than their analogue counterparts. This is mainly due to the fact that the digital sensor having additional circuitry that it needs to be powered. In some cases digital sensors might require longer initialization times (self-calibrations, on-board controller startup, internal reference stabilization) compared to analogue sensors hence consuming more energy. From the implementation side digital sensors require implementation of the communication protocol between the MCU and the sensor. However, all these drawbacks are in some applications overshadowed by the gain in accuracy, precision and potential processing done on the sensor itself.

An analogue sensor requires a microcontroller with an analogue-to-digital converter and in cases where the supply voltage is not stable, a voltage reference for the MCU's ADC. The precision and accuracy of the reading are mainly dependent on the circuitry interfacing the sensor and the resolution of the ADC on the microcontroller

Active vs Passive Measurements

Depending on the mechanic of the sensor transducer operation, sensors can be divided into passive and active sensors. The passive sensors are defined

as sensors that "listen" to the environment [16] and their change reflect the change of properties in the environment. Active sensors, on the other hand, interact with the environment and measure the response [16].

Typically the passive sensors are low power or even self-powered. Piezoresistive strain gauges are an example of low power passive sensor that changes its resistance with the variation of the strain. Change of resistance can be easily measured using a potential divider or Wheatstone bridge. It should be noted here that resistive based sensors are dissipating power when measured due to voltage being applied over their terminals. Therefore, the values in the voltage divider and bridge should be considered in order to reduce the power consumption.

There are sensors that don't dissipate power when operated. For example, sensors that change their capacitance with the change of the parameter that they are monitoring. An example of a capacitive sensor is a humidity sensor HCH-1000 by Honeywell [59] that changes its capacitance between 310pF and 355pF for a change of relative humidity between 20% and 90%. However, the power consumption of using the capacitive sensors is coming from the interfacing circuit. Typically these sensors are read out using a change of frequency of an oscillator with the change of the capacitance. Consequently running an oscillator will introduce power losses. One other alternative in reading the capacitance value is by measuring the time constant of the capacitor by charging it using a known voltage and resistance during a set amount of time.

Passive sensors can as well generate electric signals on their terminals without applying power to them. Some chemical and gas sensors, for example, CO sensor [52] are producing output without applying the power supply. The material used in the sensor is generating current potential when in contact with CO in the air.

Under some conditions self-powered sensors can produce enough power on their output to be used both as generators and as sensors. Piezoelectric devices produce a charge when subjected to pressure hence generating power on their output that can be correlated to the pressure applied. A piezoelectric based generator/sensor for human movement detection has been developed in Chapter 5.

Another example is using the magnetic field produced by the current running through a cable as a power source and as an indication on how much current is flowing through the cable. A wireless system for sensing power consumption of household utilities has been realized in [38] using this approach.

It should be noted that not all passive sensors are low power. For example, sensors designed for picking up the signals emitted from global positioning satellites have power consumption in order of tens of milliwatts. The high current consumption is coming from the amplification of the received

signal and its processing. For example, during signal acquisition phase MAX-7 GPS receiver from u-blox consumes approximately 60mW of power [159].

Active sensors, as defined earlier, need to interact with the environment in order to generate an output signal. The majority of gas and vapor sensors need to warm up the sensing element. This process consumes a significant amount of energy due to the operation of the heater. New generations of chemical sensors are using optical methods for identifying gas presence, thus significantly reducing the power consumption. One example of such sensors is an infrared CO_2 sensor GC-0010/1/2 by COZIR. Using light significantly reduces the energy consumption of the sensor compared to the traditional approach. For comparison, Telaire T6615 CO_2 (General Electric) [31] sensor that uses a traditional approach requires an average 16 5mW of power with 2 minute warm up time, while the COZIR solution is operating at 3.5 mW average with $<$10 s start-up time.

Light can be used as well for detecting particles in the air and even identifying them. This has been demonstrated by the PS2 pollen sensor by Shinyei technology [155] which can distinguish pollen from dust in the air using light scattering and change of the polarization of the reflected light.

Due to the high power consumption of the gas sensors, an approach to reducing the power per measurement has been demonstrated in [125]. This approach is aimed at the applications where the exact gas concentration is not important but knowledge of an exceeded threshold is. The concentration of the monitored gas can be assessed by extrapolating the data from the slope of the gas sensor's output change during a fraction of a second after the sensor is activated. In this way significant power reduction can be achieved.

The detailed analysis of possible sensors for use in wireless sensor networks and optimal sensor choice for give application is beyond the scope of the thesis.

3.5. Energy Storage

In the beginning of the chapter the requirement for storing energy from the energy harvester has been described in detail. This section will compare the characteristics of the two mainly used storage techniques: the capacitors and the batteries.

With the advancement of materials for capacitors, their capacitance has reached values of tens of Farads while maintaining relatively small size. The amount of energy that can be stored in such supercapacitors is sufficient to provide buffer storage for sensor node's operation in some applications. The number of charging discharging cycles of a capacitor can be in order of 10^5 or more. This is one of the biggest advantages of capacitor-based storage over the

battery-based storage. Furthermore, supercapacitors are exhibiting less temperature dependence compared to batteries.

On the other hand, current supercapacitors have high leakage currents that are sometimes larger than the sleep current of the entire sensor node. In Fig. 2.3 self-discharge of three different seized capacitors has been presented. It can be seen that the leakage current of the 50 F capacitor is initially so high that it discharges the supercapacitors below the minimum operating voltage of the node [78] faster than the node operating from 22 F capacitor.

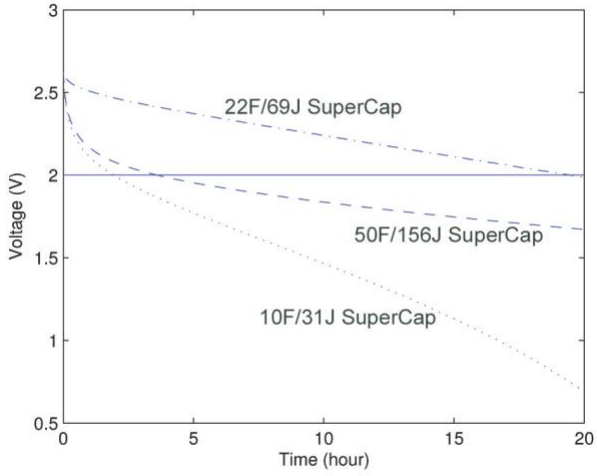


Fig. 2.3 Discharge of the supercapacitor under load Taken from [78]. The 2V line indicates the minimum operating voltage of a sensor node

Another issue with some supercapacitors is that sometimes require prolonged time to be connected to the supply voltage in order to fully charge [32]. However, this isn't always possible in energy harvesting as the power source may vary depending on the availability of energy.

The supercapacitors have the drawback when it comes to size compared to the lithium ion batteries. However, recent work in the new generation of supercapacitors, based on carbon nanotubes and graphene, is promising capacitors that will reach energy densities in the order of 100 Wh/L. Which is comparable to the energy density of some lithium ion batteries [169, 172]. The comparison of the two proposed supercapacitor technologies with current supercapacitors and lithium batteries is shown in Fig. 2.4.

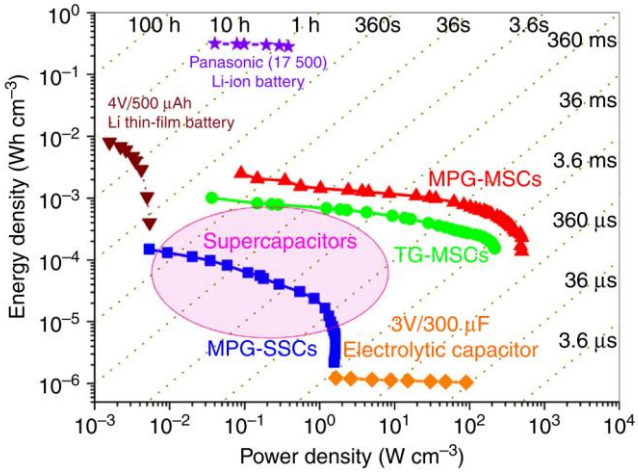


Fig. 2.4 The comparison of energy and power density of new proposed supercapacitors technologies, MPG and TG with commercially available electrolytic capacitors, lithium thin-film batteries, Panasonic Li-ion battery and conventional supercapacitors (indicated by the pink region) [52]

Hybrid combinations of lithium battery electrodes inside supercapacitors have been researched. This approach combines the large number of recharge cycles with high energy storage density of lithium ion batteries. A hybrid capacitor with energy densities in order of 95 Wh/kg has been shown in [90].

Primary batteries have been a prime source of power for wireless sensor networks for years. However, they deplete over time. Energy harvesting generators could potentially be used to recharge the secondary battery in the system.

Secondary batteries allow for smaller buffer storages compared to supercapacitors due to their significantly higher energy density as shown in Fig. 2.6. However, due to the nature of the chemical processes used in storing the energy, the battery degrades with each charge/discharge cycle [78]. In order to prologue the life of the battery it should be discharged as shallow as possible. Fig. 2.5 demonstrates that the number of recharge cycles is an exponential function of the number of depth of discharge.

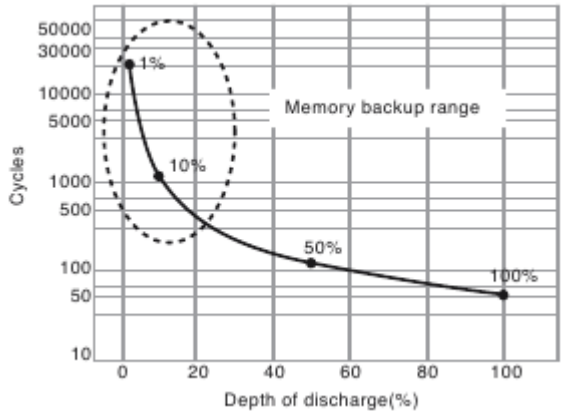


Fig. 2.5 Cycle life of a vanadium rechargeable lithium battery [33]

To extend the batteries lifetime in some energy harvesting applications batteries are used in conjunction with supercapacitors in order to reduce the number of change/discharge cycles of the battery [78].

The batteries, similar to supercapacitors, suffer from loss of charge over time. The self-discharge of the batteries depends on the type of battery chemistry used. The comparison of different battery technologies is presented in Table 2.5. The data is obtained from [160] with addition of thin film batteries from [143] and Lithium Manganese batteries from [33].

The introduction of small low power system-on-chip modules that combine the microcontroller with a radio require only a few external components. This has turned the attention of system designers to coin cells batteries as a power source. The WSN nodes implementing Bluetooth 4.0 low power protocol could potentially run on a single coin cell battery for months. The use of coin cell batteries is, however, limited mainly to their internal resistance as these batters can only source 15 mA of current without damage. Demanding 30 mA peak currents reduces the capacity of a battery by 10% [141]. These batteries were originally designed to be used as memory backups with typical discharge currents of $<$2mA. In order to avoid a potential large voltage drop when sourcing currents in the range of tens of milliamperes in short periods of time, a possible approach is to use a capacitor as a buffer. In this scenario the energy required during high current bursts is supplied from the capacitor which is then recharged from the battery.

Table 2.5 Comparison of different battery technologies based on [160, 143, 33]

	NiCd	*NiMH*	*Lead Acid*	*Li-ion*	*LiPo*	*Reusable Alkaline*	*Li-Mn*	*Li - Thinfilm*
Gravimetric Energy Density(Wh/kg)	45-80	60-120	30-50	110-160	100-130	80 (initial)		
Internal Resistance (includes peripheral circuits) in Ω	0.100 to 0.200 6V pack	0.2 to 0.3 6V pack	<0.1 12V pack	0.15 to 0.25 7.2V pack	0.2 to 0.3 7.2V pack	0.2 to 2 6V pack	>100	210 to 360
Cycle Life (to 80% of initial capacity)	1500	300 to 500	200 to 300	500 to 1000	300 to 500	50 (to 50%)	1000 (to 90%)	100 000 (to 90%)
Fast Charge Time	1h typical	2-4h	8-16h	2-4h	2-4h	2-3h		15min
Self-discharge / Month (room temperature)	20%	30%	5%	10%	~10%	0.3%	2%	1%
Cell Voltage(nominal)	1.25V	1.25V	2V	3.6V	3.6V	1.5V	3	3.6
Load Current - peak - best result	 20C 1C	 5C 0.5C or lower	 5C 0.2C	 >2C 1C or lower	 >2C 1C or lower	 0.5C 0.2C or lower	 >1C	 38C (7mA)
Operating Temperature(discharge only)	-40 to 60°C	-20 to 60°C	-20 to 60°C	-20 to 60°C	0 to 60°C	0 to 65°C	-20 to 60 °C	-40 to +85 °C

The new generation of the thin film batteries are demonstrating charge/discharge cycle numbers in the range of 100 000 iterations. This makes them comparable to supercapacitors, while still having a high energy density. Furthermore these batteries have a leakage current in the order of nanoamperes, which is also beneficial for low power systems. These batteries, at the time of writing, have output impedances in the order of 100 Ω, thus reducing the amount of available current. Similarly to using the coin cell batteries, adding a capacitor parallel to the battery can provide the required energy for the short bursts of high power demand.

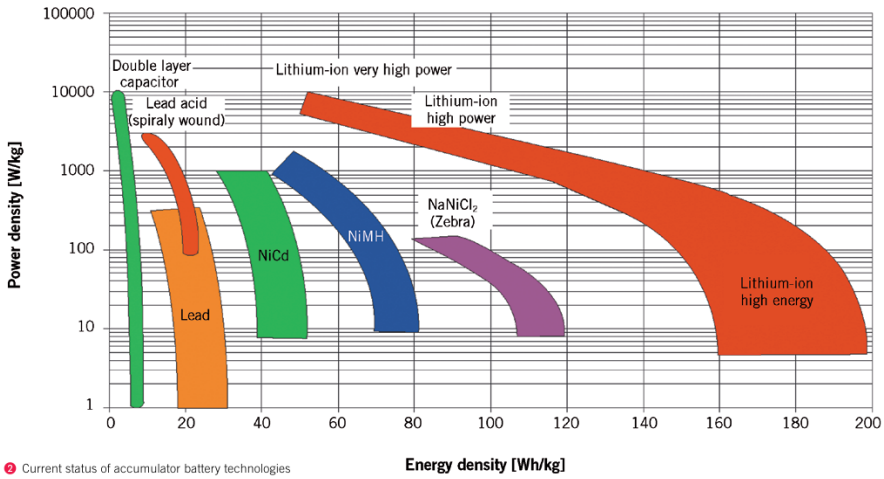


Fig. 2.6 Rechargeable storage energy and power densities [102]

The research in battery technology is aimed at making smaller batteries capable of storing more energy while being able to provide high power densities. Based on review done in [102] one of the current research focus, in the field of rechargeable batteries, is on Lithium-Air batteries that have a theoretical energy density of 11 000 Wh/kg. In practice it is expected that 10% is realistically achievable which would be still an order of magnitude higher density than currently available solutions. However, this technology is far from commercial availability at this point. A possible step between current Lithium technologies and Lithium-Air batteries might be Lithium-sulfur batteries that have a theoretical density of 2550 Wh/kg. The company SionPower in collaboration with BASF has demonstrated a battery that has energy density of 350 Wh/kg which is 50% more than current top of the line Li-ion batteries. The drawback of this battery is that currently it supports only 50 recharge cycles.

The final choice on the storage to be implemented in the system comes down to the application, design, size, cost and application's performance and lifetime requirements. Detailed analysis in storage selection for a given application is done in Chapter 5. A comparison between the batteries and supercapacitors is summarized in Table 2.6.

Table 2.6 Comparison between batteries and supercapacitors

	Advantages	*Disadvantages*
Capacitors	• Long lifetime • Large number of charge cycles • High power density • Safer for use and disposal • Better for use in harsh environments	• Self-discharge • Low energy density • Energy management issue: Empty capacitor
Batteries	• High energy density • Easier to implement • Cheaper per Joule stored • Power availability	• Shorter lifetime (although new generations have long lifetimes) • Safety • Temperature range

3.6. Wireless Sensor Network Platforms

Design and implementation of a low power sensor node is not a trivial task, resulting in research groups often obtaining hardware that has been developed for some other purpose and then adapting it. In order to simplify the design and implementation of wireless sensor network a number of research groups have come forward with their solutions for wireless sensor nodes.

Most of the platforms found in literature are complex nodes with flexible hardware options and multiple interfaces in order to connect to various sensors. One of the first platforms that got widespread use in the research society were nodes produced by UCB Telos [118], and Crossbow, mica class of nodes [5]. These nodes were designed with low power in mind and were aimed at using TinyOS [36] as the operating system.

Some research groups have focused on minimizing the size of the node under 1 cm^3 using commercially available off the shelf components. University of California came forward with its ECO platform [112] that packed the entire functionality of a sensor node into 648 mm^3.

In 2001. the researchers from UCB have introduced an idea of deployments of 1 mm^3 wireless sensor nodes in large numbers that could communicate and perform various sensing tasks. This research group has demonstrated a complete sensor node in 138 mm^3 [165]. Researchers have demonstrated an 8.75 mm^3 [53] wireless sensor node for temperature measurements. A more recent addition to this family of nodes is the 0.56 cm^3 wireless sensor node from UCB [136].

In order to increase the flexibility of node and realize a multipurpose platform, some researchers have investigated into modular platforms. In [132] a modular platform is demonstrated that can be adjusted for an application at hand by simply adding or removing hardware modules. Different hardware modules are being connected to the rest of the system over a specially designed

power and communication bus. Another approach of modular sensor node systems was presented by the company Libelium that has launched a wireless sensor platform with a wide array of sensors and supported wireless communication technologies [92].

It should be noted that almost all of these platforms are designed to mainly be run on batteries. The energy harvesting is typically added by attaching the energy harvesting modules to the power supply input of the sensor node. An example of this approach is the Texas Instruments solar harvesting module that can be combined with the ez430 series of wireless sensor node platforms [69]. However, these platforms are not aimed at utilizing the EH power source to its full potential.

In order to achieve better control over the energy harvesting process some research groups have designed wireless sensor network platforms especially for use with energy harvesting sources. An example is the Prometheus node [78] that is designed to operate powered by a solar panel. The company EnOcean has designed a series of energy harvesting powered wireless solutions that can be easily implemented in wireless sensor networks [48]. Research has been made in the field of multimodal harvesters for wireless sensing applications in order to provide power for the sensor node from several power sources [131].

Another benefit of using a well-established platform for rapid deployments is the software support that most platforms come with. Some platforms are running specially designed low power operating systems in order to reduce the task of energy management and ease the peripheral use for the software designer. Low power operating systems and microcontroller programming will be discussed in more detail in the later section of the chapter.

4. Wireless Communication

The main task of the wireless sensor network is to collect data from the environment and relay it to the collection point (base station). The radio module on the node consumes a significant amount of power when operating. Therefore, it is necessary to develop a communication scheme that will provide energy efficient way of utilizing the wireless communication channel. The communication protocol defines all communication parameters in the wireless sensor network. The selection of the communication protocol used will have a considerable impact on the power consumption, performance, dependability, scalability and adaptation of the wireless sensor network [150].

One of the main characteristics of the protocol is the type of network topology it supports. The type of the topology is going to play a major role in the later implementation of routing and handling the traffic through the

network. Depending on the way connections among the nodes of the network are laid out, three main common types of topologies can be identified:

- Star topology network
- Tree topology
- Mesh topology

The three topologies are graphically illustrated in Fig. 2.7.

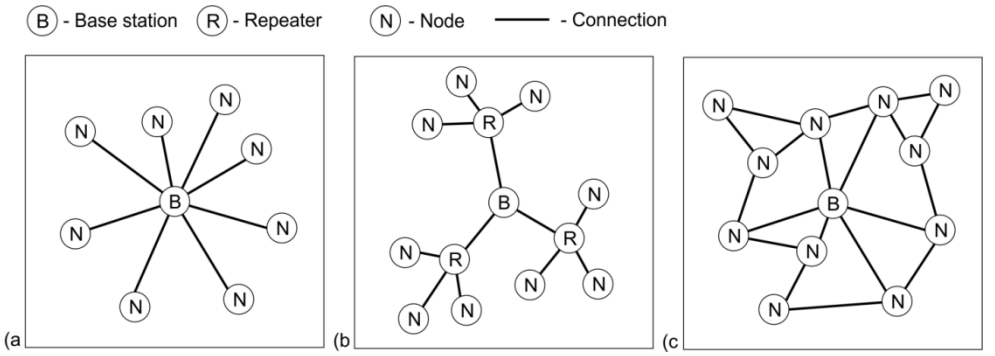


Fig. 2.7 Common network topologies for sensor network (a) star, (b) tree (c) mesh

The star topology is the most straight forward topology where all the nodes can communicate with the base station. In a tree topology repeater nodes are forwarding the data from other nodes to the base. On the other hand, in a mesh network scenario the nodes can communicate with their neighbors. Therefore, there is a possibility to forward the data using different routes depending on the routing algorithm. The existence of alternative routes in the network allows for increased reliability as the packet can reach the base station using an alternative route.

Each step the data takes through the network is referred to as a "hop". Star topology networks are singlehop networks while tree and mesh networks are multihop networks. The multihop networks are very attractive as they provide a possibility to extend the range of the network beyond the range of the single node's radio. When the network has to cover a larger area then there are two options; (i) increase the power of the radio transmission or (ii) design a multihop network. The addition of new nodes increases the complexity of the communication protocol and introduces a need for routing the data; however, it could potentially reduce the power required. The generalized version of Friis free space model can be used to theoretically assess the potential benefit of using a multi-hop network [16]. The power that will reach the receiver P_{RX} is proportional to the power emitted from the transmitter multiplied by the factor that defines the path loss where d is the distance between the two nodes communicating, λ is the wavelength, and η is the path loss exponent. The

formula is given in (2.1). In case of a multi-hop network H denotes the number of hops that need to be performed:

$$P_{rx}^{singlehop} = P_{tx}\left(\frac{d}{\lambda}\right)^{\eta} \tag{2.1}$$

$$P_{rx}^{multihop} = HP_{tx}\left(\frac{d}{H\lambda}\right)^{\eta} \tag{2.2}$$

Combing the equations (2.1) and (2.2) a factor describing the power reduction can be obtained:

$$\frac{P_{rx}^{singlehop}}{P_{rx}^{multihop}} = H^{\eta-1} \tag{2.3}$$

By varying the path loss factor and the number of hops it is possible to make, a theoretical estimation of the potential power reduction in communication of a multi-hop network over a single-hop network. This is shown in Fig. 2.8.

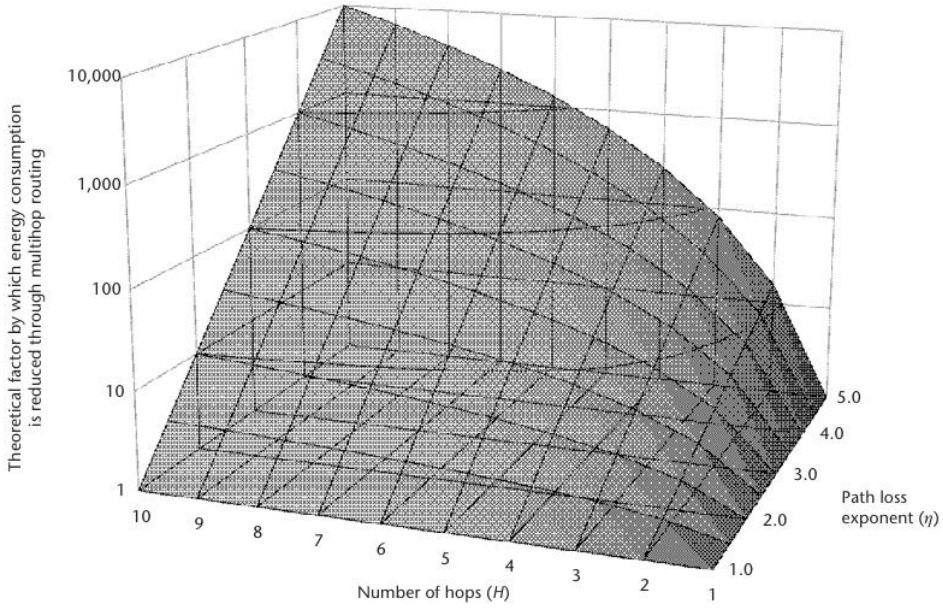


Fig. 2.8 Theoretical power reduction of communication power in case of multihop network as the function of number of hops and path loss exponent [16]

From Fig. 2.8 it can be seen that in case of environments with high path loss factors, such are indoor environments, a multi-hop network has a

significant advantage. However, this model is not capturing the power required for operation of the radio hardware, the starting up and operation of high frequency crystals, packet assembling, and other processes involved in the radio's operation (which can sometimes be larger than the power required for transmitting the packet [16].) Furthermore, it doesn't account for the potential packet collisions and the overhead in receiver's radio being active waiting for the packet from the transmitter as well as all the calculations required by the routing protocol. It also doesn't account for the necessary overhead in order to establish and maintain a multihop network, update the routing schemes, and adapt the transmission power to match the distance. The multihop approach can further give raise to the issues of data latency, accumulation of data in nodes and end-to-end reliability. However, the multihop approach is useful in cases of hostile environments with high path losses and cases where the power of the transmitter can't be increased further due to regulatory limitations.

As a conclusion, a definitive answer cannot be given whether to implement a multihop network or a single hop network by altering the radio properties. The decision is going to depend on the specific application scenario and the environmental conditions which approach will be the most optimal.

4.1. Protocols for Wireless Sensor Networks

Designing a communication protocol is not a trivial task, especially in resource constrained systems. If the routing requires too many control packets, chooses sub-optimal routes, or requires significant computation resources to determine the routes it might reduce the lifetime of the node and hence the network. In industry and academia there has been a significant research interest in developing low power wireless protocols that would allow for optimal use of the stored energy. Furthermore, standardization of protocols has provided a stable foundation for component manufacturers to produce more efficient integrated circuits that embed the protocol stacks reducing the complexity of the software running on the MCU. A variety of modules that support different standards have been presented in Section 3.4.

In recent years several protocols have been in the focus of research and industry. The summary of different popular wireless protocols is given in the

Table 2.7 [122].

The majority of standardized protocols, and a number of proprietary protocols, are designed to operate in the 2.4GHz ISM band. This was mainly driven by the possibility of worldwide unlicensed use and high data rates allowing fast transmission and reception hence reducing power per transmitted bit of data.

Table 2.7. Summary of different poplar WSN protocols used in literature [122]

Protocol	Zigbee	Z-Wave	EnOcean	UWB	Bluetooth	Wi-Fi	6LoWPN
IEEE Standard	IEEE 802.15.4	-	-	IEEE 802.15.3a	IEEE 802.15.1	IEEE 802.11a/b/g	IEEE 802.15.4
Frequency Band	2.4 GHz, 915 MHz, 868 MHz	868/915 MHz, 2.4 GHz (400 series only)	868 MHz	3.1 – 10.6 GHz	2.4 GHz	2.5 GHz	2.4 GHz, 868 MHz, 915 MHz
Data Rate	20/40/250 kbps	9.6/40/200 kbps	125 kbps	110 Mbps	1 Mbps	54 Mbps	20/40/250 kbps
Modulation	/BPSK / BPSK / O-QPSK	FSK / GFSK	ASK	BPSK, QPSK	GFSK	B/QPSK, COFDM, QAM	BPSK / O-QPSK
Spreading	DSSS	No	No	DS-UWB, MB-OFDM	FHSS	DSSS, CCK, OFDM	DSSS
Communication Range	10-100	30 (in) – 100 (out)	30 (in) – 300 (out)	10	10	100	10-100
Security	AES	AES-128	Basic	AES	E0 Stream AES-128	RC4 Stream / AES block	AES
Error Control / Reliability	16-bit CRC, ACK, CSMA-CA	8-bit CRC, ACK, CSMA-CA	-	32-bit CRC, CSMA-CA	16-CRC	32-bit CRC	16-bit CRC, ACK, CSMA-CA
Network Size	64000	232	2^{32}	8	8	2007	2^{64}
Internet Connection	Gateway Required	Gateway Required	Gateway Required	Gateway Required	Gateway Required	Gateway Required	Gateway Required
Logistics	Standard	Proprietary	Proprietary	Standard	Standard	Standard	Standard

One of the most widely used standards in the 2.4GHz range in wireless sensor networks is the IEEE 802.15.4 standard. This standard defines the physical and network layer in the communication. The physical layer defines the physical characteristics of the radio (modulation, frequency band, over the air data rate, etc.) and the network layer defines the mechanic for accessing the wireless link through the MAC (medium access control).

The MAC defines how the packets of data will be transported between the two communicating parties by controlling the access of the individual nodes to the transfer medium. However, this is enough only in the case of star topology networks. In case of more complex networks it is necessary to design an additional layer that will take care of the routing of the packets from any node to the base station and vice versa. The ZigBee protocol is one of the most popular routing protocols based on IEEE 802.15.4, however, it has been demonstrated that is too power demanding for some low power wireless sensor network applications [16]. The 6LoWPN protocol that is built on top of IEEE 802.15.4 standard is aimed at supporting the "Internet of Things" [12] applications. Similarly to ZigBee it can be too power consuming for some ultra-

low power applications due to the communication overhead required in order to be compatible with the IPv6. WirelessHART is another protocol based on IEEE 802.15.4 standard. It is primarily aimed at process measurement and control applications [142].

Two low popular low power protocols not mentioned in the Table 2.8. These are the Bluetooth Low Energy (BLE) and ANT. They have been specially aimed at battery powered devices and are operating in 2.4GHz rage. The BLE is supporting only star shaped network topology limiting its use only to sensors that are within unit's radio range, while ANT supports mesh networks.

The analysis done in [141] demonstrates that the power consumption of the Bluetooth LE is lower than ANT. Measured sleep interval of 120s between transmissions the BLE achieved lower power consumption (10.1 µA), then both ZigBee (15.7 µA) and ANT (28.2 µA) [39]. A more detailed investigation of the power consumption of different protocols was done in [141]. The results are summarized in Table 2.8.

Table 2.8. Comparison of different low power protocol characteristics based on results from [141]

	ANT	*BLE*	*ZigBee*	*WiFi*	*Nike+*
Protocol efficiency	47%	66%			
Energy efficiency	0.71µW/bit	0.153µW/bit	185.9µW/bit	5µW/bit	2.48µW/bit
Latency	0s	2.5ms	20ms	1.5ms	1s
Payload Throughput	20kbps	305kbps	100kbps	6Mbps(lowest power mode)	272bps

From the power efficiency stand point the most efficient protocol is the Wi-Fi, due to its high data rate. This isn't visible in Table 2.8, as the table is showing the lowest power setting of the Wi-Fi. If full speed of Wi-Fi is utilized, energy consumption per bit will be lower than any other wireless technology. However, seldom is the case in low power energy harvesting networks that accumulate large amounts of data in order to justify the use of high speed Wi-Fi. Even if the system logs the data and transfers it in a single burst of activity, this kind of operation would require a significant storage in order to supply the Wi-Fi module with sufficient energy.

Next most power efficient protocol is the BLE followed by ANT. However, it should be noted that the actual power consumption of the communication in the end is going to depend also on the hardware being used, the amount of data transferred, the duty cycle of the operation and environmental conditions.

In the case of applications where longer distances between nodes need to be covered, radios operating at lower frequencies are used due to better

propagation characteristics of longer wave lengths. Z-Wave and EnOcean are two wireless proprietary protocols aimed primarily at home and building automation markets. EnOcean's protocol has been specially designed to operate with energy harvesting buttons and solar powered sensors [48]

The ultra-wideband (UWB) radios have gain momentum in research community because they promise high data rates at low energy using the unlicensed frequency range of 3.1GHz to 10.1 GHz. These radios are operating using short, high frequency pulses with low duty cycles, hence providing low average power consumption. At the time of writing, the receiver modules had relatively high power consumption due to the complexity of decoding the signal. However, advancements in the field are leading to ultra-low power radios. In [25] a 1mW radio has been demonstrated operating at 1Mbps.

4.2. Energy Aware Communication Protocols

All aforementioned protocols have been aimed at wireless sensor nodes with stable power supply (e.g. battery operated). However, in the case of energy harvesting systems there is a need for a paradigm shift from minimizing power to maximizing energy utilization because the energy availability is going to change depending on the environment. Therefore, the MAC and routing protocols have to account for the change in available power. Energy harvesting is introducing a dependency on energy availability into the MAC and routing protocol. For example, in the case of a solar powered network some of the nodes might be temporarily located in a shade. A routing protocol can be implemented that would avoid shaded nodes and route using the nodes that have larger amount of power at their disposal [175, 95]

Beside optimization of the routing in the network, it is also necessary to optimize the way the radio accesses the wireless link through optimization of the MAC protocol. As the access to the wireless link is controlled through the MAC, effective use of the communication medium will have major impact on the power consumption. The MAC protocol has to address the following issues:

- Overheads – additional information that has to be transmitted with every packet that allows identification of the origin, destination and additional information required by the network
- Collisions – when two nodes transmit the data at the same time hence requiring that the packet gets retransmitted.
- Over-emitting – when the packet is sent but the reception node wasn't receiving the data,
- Idle listening – time the node spends in reception before it receives a packet,
- Overhearing – energy used by the nodes to decode a packet that is not intended for them

One approach is to allocate fixed time (TDMA), spectrum (FDMA) or coding (CDMA) to different nodes in order to control when and how each node accesses the medium to perform communication. These protocols provide answers to the majority of the issues of the MAC. However, they require good time synchronization either using stable onboard time keeping modules, or implementing time synchronization using the network itself [21]. In [170] authors demonstrate the challenges of implementing a time slotted MAC on an energy harvesting powered system indicating that even after several optimizations the time slotted MAC layer still required more energy than the harvester was capable of providing in the given application scenario.

An alternative to MAC layer that allocates fixed slots for accessing communication medium are random access protocols. In a random access MAC protocol the node transmits the data when available. In these protocols nodes usually use one communication channel and usually check if the cannel is available by listening before transmitting in order to avoid collision with ongoing communication (Carrier Sense Multiple Access - CSMA).

Between transmissions, the nodes spend time in low power modes where the receiving section is turned off. This leads to a challenge of activating the receiver of one node and transmitter of the other at the same time, otherwise, the packet transmitted might get lost. Therefore, it is necessary to develop an approach to synchronize the two nodes.

The timekeeping is a challenge on the nodes therefore, it is expected that there will be some temporal distance between the receiver activating and sending, hence leading to waste of energy. The challenge of designing the MAC protocol is to minimize the loss of energy.

A number of different protocols have been demonstrated that are aimed at low power operation while minimizing the wasted energy. The Berkeley MAC (B-MAC) [117] protocol is built on top of the IEEE 802.15.4 physical layer and is utilizing a technique called low power listening. The idea behind this concept is that the receiver periodically wakes up and listens for a short period of time if there is a preamble signal coming from the transmitter. The node that has data to transmit wakes up periodically and transmits a preamble signal for a period of time Δt_p followed by the data packet. If the receiving node detects the preamble signal the receiver stays active and receives the packet sent from the transmitter that is following the preamble signal. This MAC protocol is beneficial for networks where data is not sent frequently. Operation of B-MAC protocol is depicted in Fig. 2.9.

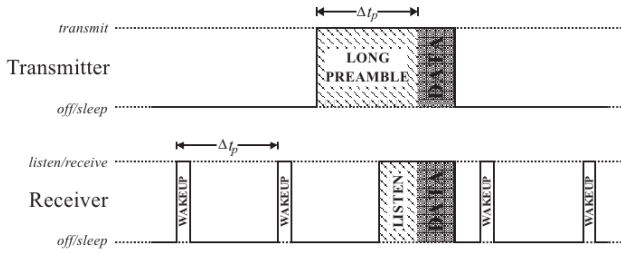


Fig. 2.9 Operation of the B-MAC protocol [16]

The shortcomings of this protocol have been addressed in later X-MAC protocol [174]. This protocol is repeating the destination address instead of a preamble hence all nodes that aren't the intendant recipient of the packet can go back to sleep instead of waiting for reception of the packet to determine it wasn't addressed to them. Second improvement lies in the fact that after each transmitted destination address the transmitted waits for a response for a fixed duration of time before retransmitting. During this delay the transmitter is waiting for an acknowledge packet from the receiver that it has received the destination address. In this way there is no need for waiting for the entire period of Δt_p before sending the packet. As a result the throughput of the network in increased.

Recently more advanced protocols have been presented that are further optimizing the MAC protocol by making the protocol energy aware. The ODMAC protocol proposed in [50], which is an on demand MAC protocol, aimed at supporting nodes with individual duty cycles. The duty cycle of the node is dependent on the available energy. Therefore, by adjusting the duty cycle the average power consumption can be reduced before the storage gets depleted and the node drops out of the network.

A common feature of all proposed protocols is periodic waking up of the node in order to sense if there is a signal from surrounding nodes that they have data to transmit. In case of networks that have low duty cycles measured in minutes continuous transmission of beacons, or activations to sense if some node has data to forward is a waste of energy. Therefore, some researches are proposing wireless wake-up approach where a specially designed receiver is kept active all the time.

This receiver activates the node only once it receives a signal of characteristic shape [148, 96]. These receivers are designed to consume nanoamperes of current which is typically similar or even smaller than the nodes sleeping current consumption. Another proposed approach is based on sending an infrared pulse from the transmitter to the receiver that will signal the node to active its radio. In [161] a zero power infrared detector has been realized that would activate the node once an infrared signal has been received.

5. Energy Awareness in Embedded Software

The main task of the algorithm running on the microcontroller is to adjust the operation of the system to reach energy neutral operation. In order to do so the node's operation should be based on the energy availability. The amount of available energy can be easily determined in the case of a single storage on the node. However, in the case when there are several different storages the task of determining the available energy level can become more complex. Based on the information on the available energy the microcontroller can decide on the task it can perform without depleting the buffer energy storage. An example of an energy aware algorithm is presented in [137]. Here an energy aware lazy scheduling algorithm is presented. This algorithm is scheduling tasks in a way to maximize the accumulation of energy in the storage.

Some algorithms for task scheduling are relying on the climate and environmental data in order to forecast the energy availability. Using the result of the forecast the scheduling, the algorithm selects which tasks are going to be executed. When forecasting is used it is possible to activate the tasks for which execution there isn't enough energy, however, the energy will be accumulated during the tasks execution hence leading to sustainable operation [123, 166].

5.1. Operating Systems and Software Implementation

Fulfilling all energy management related tasks while utilizing the microcontroller as efficient as possible and keeping the code modular is a big challenge in programming the WSNs. A number of operating systems have been developed to aid the developer when designing the software for use with the WSNs. These operating systems are taking care of peripheral use and keeping the microcontroller in the lower power mode of operation for as long as possible. Some of commonly used microcontroller operating systems are TinyOS [36]. Contiki, MANTIS [16]. For example TinyOS operating system doesn't provide typical operations of operating systems like parallel task execution, memory management, but provides a very lightweight environment that is event driven and optimized to keep the MCU in low power mode as often as possible. TinyOS is programed in the NesC language and has implemented hardware abstraction layers hence making it possible to cross compile the same software on different platforms. TinyOS consists of services and abstractions that are aimed at easy implementation of wireless sensor network synchronization, radio operation and interface to the hardware [36]. These features are making the TinyOS a very flexible programming solution allowing easier implementation of wireless sensor networks.

However current operating systems don't have support for performing energy management through selecting which task should be executed based on

current energy level and predicting how much energy is required for the tasks execution. In case of EH-WSN being able to automatically select tasks for execution depending on the energy level can lead to more efficient use of energy without the need to specifically program that behavior. The Eon programming language [144] has a feature to select which tasks are going to be executed based on the task's energy requirement, priority and current available energy budget. The Eon compiled programs are Linux and TinyOS compatible allowing the language to be used with a wide variety of commercially available platforms.

If the sensor node requires the most optimal operation it is necessary to program the microcontroller without the use of the operating system. This process yields the best performance, but it is time consuming. In order to achieve as power efficient operation as possible the MCU should be programed to delegate the tasks to the onboard peripherals as much as possible and be placed in the low power mode while these tasks are being processed. When the task is done the peripheral will activate the MCU core that will continue algorithm operation. Implementation of such schemes of operation can be a challenging task especially if the microcontroller is supposed to perform complex algorithms interfacing multiple sensors and relying on excessive use of peripherals on the node.

6. Conclusion

This chapter introduced and described the main concepts of the energy harvesting wireless sensor node. Typical components and approaches to realizing different parts of the system have been covered with the focus on the microcontroller, the radio, the memory and the sensing systems. In the second part of the chapter the focus was on the wireless communication and basic of low power communication protocols. In the end software development for low power applications was covered.

Chapter 3

Energy Harvesting Technologies

1. Introduction

An energy harvesting transducer is a specially designed system that is aimed at converting the ambient energy into electrical power. The main aim is to replace or supplement batteries as the power source for low power electronics. Typically in the devices immediate surrounding there are numerous potential energy sources. The challenge is to identify them and design energy harvesting transducers (generators) that will extract sufficient amount of energy from the ambient sources.

Typical sources for energy harvesting are: light, vibrations, RF energy, and thermal gradient. The amount of power collected by the harvester will depend on the availability of the selected power source, the harvester's size, construction, conditions and technologies available. A summary of estimated power output of different types of energy harvesting power sources is given in

Fig. 3.1. The availability of power sources can vary in the given environment and sometimes it is necessary to combine more than one power source [88].

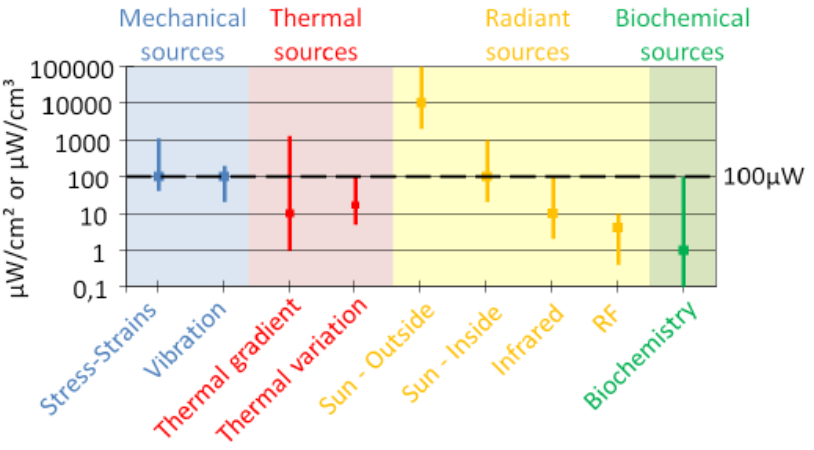


Fig. 3.1 Summary of estimated power output for different power sources [88]

The light's high energy potential makes solar one of the prime energy harvesting sources, especially in the outdoor applications. For example, a soil monitoring application [104] or olive tree farm monitoring [76] can be easily solar powered. However, light isn't always available. In industrial applications the use of vibration energy might be a better choice, especially in the domain of condition monitoring applications [110]. Monitoring of properties of vehicles can be also of interest [22]. A research area that got significant attention recently, in regard of vehicle monitoring, is tire pressure monitoring [163].

Harvesting energy from human body motion in order to power hand held devices and sensors located on the human body, or inside it, has been a popular research topic as well [30, 129]. Various approaches have been implemented in this field. An example is harvesting the energy of a human gait by using specially designed backpacks [57, 173], or special shoe inserts [84].

This chapter will be focused on technologies required to implement an energy harvesting transducer. The scope of this chapter will be limited to solar and kinetic energy harvesting. These two transducer mechanisms are among the most common in research beside the thermal and radio frequency harvesting transducer technologies. Beside these technologies, it should be noted that energy harvesting isn't limited only to these approaches. There is a vast design space of energy harvesters that are based on various phenomena such as the pH difference between the tree and the soil [157], or an energy harvesting system stimulated by β-emitting radioisotopes [7]. A very interesting approach to thermal harvesting was presented in [171] where sufficient energy

was harvested, from the energy of the ionic thermal motion, to drive a commercial off the shelf LED.

The rest of this chapter is structured as follows: first the concepts of solar and kinetic energy harvesting are described in detail. Then power management circuits for use with energy harvesting transducers are described. In the end three applications will be described that were realized and published. In the end a conclusion is presented.

2. Solar Energy Harvesting

One of the things most associated with alternative energy sources is solar energy. The amount of solar energy that reaches the Earth each day is sufficient to cover the total energy needs of the Earth for one year [24]. The solar energy has been used in many fields ranging from residential (for both heating and electricity), through powering vehicles, space and naval applications, to powering small-scale electronics and recharging batteries.

The use of solar energy dates back to ancient civilizations. The main use of solar power was heating and lightning applications. In the 19 century, Europeans started using solar-heated greenhouses and conservatories. In 1883. Charles Fritts described the first solar cells made from selenium, achieving efficiency of 1 %. The first silicon solar cells were developed in 1954. by researchers Calvin Fuller, Daryl Chaplin, and Gerald Pearson at RCA. These first solar cells were 4.5 % efficient and were raised to 6 % during the next months. In 1955. early successful products powered by solar cells emerged: solar cell powered dollar bill changers and devices that decoded computer punch cards and tape. At that point the cost of energy was \$1500/W using 2% commercially available solar cells. In the following years the price per watt dropped as the efficiencies rose and solar cell availability increased. Ultimately the price reached the 0.74\$/W mark at the beginning of 2013. according to National Renewable Energy Laboratory (NREL) report [51].

2.1. Structure and Physics Behind a Solar Cell

When a material is exposed to light there are three possible effects that can occur:

- Absorption: Incoming light is absorbed by the material
- Reflection: Material reflects the incoming light
- Transmission: The light passes through the material

The first two effects are most common while some materials also exhibit the transmission property, thus allowing the light of a given frequency range to pass through. This section will focus on the effects absorption has on the material.

A photon is the carrier of light energy. The light energy is equal to the product of Planck constant and the frequency of the light wave. When absorbed by a material, a photon delivers the energy it is carrying to either electrons or phonons. The phonons in the material determine its temperature; hence absorption of the photon by the phonon would increase the temperature of the material. In the case of some semiconductor devices, if the photon is absorbed by an electron, under the circumstance that the photon was carrying a sufficient amount of energy, the election might break free from the atom, thus moving into the conductance band of the semiconductor, allowing it to move freely inside the material. On the other hand, the vacancy it left behind can be filled by electrons from one of the surrounding atoms hence making the vacancy appear to move from the atom that lost the initial electron. This vacancy is referred to as "hole". Electrons and holes are considered free charges that can move around the material, thus forming an electric current. The effect of generating free charges in the material by light is called the photoelectric effect.

It can be said that in certain types of semiconductors photon absorption generates a hole-electron pair. However, the lifetime of generated electrons and holes in a bulk material is short as they recombine fast with other electrons and holes, keeping the material electro-neutral. In order to make electric current it is necessary to separate the electrons and holes and then provide a path through the external circuit where electrons could flow before being recombined with holes. The separation of electrons and holes can be achieved by combining two, or more, different semiconductor materials.

If a semiconductor is designed in such a way that that it has excess of electrons it is called n-type of semiconductor. If, on the other hand, the semiconductor is designed so that it has an excess of holes, it is considered a p-type of semiconductor. When these two types of semiconductors are joined they form a p-n junction. A characteristic of the p-n junctions is that a depletion region is formed between the two semiconductor types. The depletion region is a consequence of holes on the borderline of p-side of junction recombining with electrons in n-region. As they recombine this area of the junction it becomes free of all carriers leaving electrically charged atoms. The charge of the atoms generates an electric field that acts as a barrier stopping any more free carriers moving from p-type semiconductor to n-type semiconductor. A p-n junction is shown in Fig. 3.2

When a photon gets absorbed in the depletion region it forms an electron-hole pair as described before. As soon as it is formed, the electron gets "picked up" by the electric field of the depletion region and transported to the n-type of the semiconductor. Similar is happening to the hole that moves to the p-type side of the junction. This excess electron will make the n type slightly more negative and similarly the hole is making the p-type slightly more

positive. By connecting this semiconductor inside a circuit current will flow in order to balance the number of electrons and holes in the semiconductor, hence generating current.

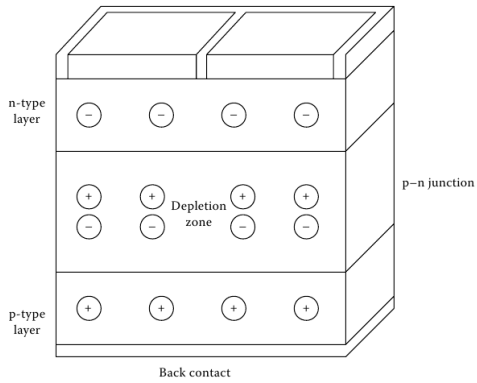


Fig. 3.2 The p-n junction of the photovoltaic cell [80]

The energy required for the electron to be formed is going to depend on the characteristic of the material used. This energy is defined by the "bandgap" of the material, i.e. the energy required for the electron to be moved from the valence band, over the potential gap, into the conductive band where it can contribute to the electric current. As the energy is correlated to the wavelength of the light, different materials will require different wavelengths in order to produce photoelectric currents.

2.2. Solar Cell Technologies

The solar cells can be made from different types of materials, deposited and arranged in various structures. The main types of materials used are silicon, polycrystalline thin films, single-crystalline thin films and organic materials.

The silicon based cells were the first type of cells used. In the beginning they were mainly based on a single crystalline structure, also known as single-crystalline solar cells. With advancement of material science new types of solar cells got introduced: semi-crystalline silicon, multi-crystalline silicon, thin film cells, amorphous silicon cell and organic based solar cells. In order to increase the efficiency of the solar cells they are in some cases build using several layers of material. These cells are then referred to as multijunction cells compared to single junction cells that use only one material for generating electric current.

The single-crystalline silicon has a uniform crystalline structure. This uniformity allows for efficient transport of electrons through the material, making it a good semiconductor material. This type of silicon can be easily

altered in order to make it p-type or n-type. However, while providing high efficiency cells, it has the highest price compared to other silicon based materials [80].

The semi-crystalline silicon consists of several smaller crystals (grains) of silicon. As the crystal isn't uniform boundaries are formed between different grains leading to increased loses as boundaries are places with increased recombination of electrons and holes. Due to higher recombination, these cells are less efficient than single-crystalline cells. On the other hand, the price of these cells are significantly lower compared to single-crystalline silicon, hence increased interest by researches on removing the effects of the grain boundaries and increasing the efficiency of the cells while keeping the price low.

Poly-crystalline thin film solar cells are based on CIS, CdTe and thin-film silicon. The thin film term comes from the method used for depositing the material. These types of solar cells are made by depositing thin layers of semiconductor material. Therefore, realization of this type of cells uses much less material. The active area of the cell is only 1-10 µm thick, while in a conventional thick solar, the active area is 100-300 µm thick. Thin-film cells can be easily produced for large areas and can be deposited on flexible materials.

Single-crystalline thin films solar cells are based around high efficiency materials such as GaAs and other multiple compound semiconductors. Gallium is rarer than gold and is obtained as a by-product of smelting of other materials, mainly aluminum and zinc. Therefore, it is necessary to utilize it efficiently and in low quantities in order to make the cells an economically viable option.

The GaAs is especially suitable for use in singlejunction and high efficiency solar cells for several reasons: first the band gap of GaAs 1.43V making it nearly ideal for single junction solar cells. Second, GaAs has a very high absorptivity requiring only few micrometers thick layer compared to silicon based cells that require 100 µm or more. Third, GaAs is less sensitive to heat, making it a good candidate for concentrator applications. Alloys made from GaAs, aluminum, indium, phosphorus antimony have complimentary characteristics allowing great flexibility in design of cells by stacking these materials in layers.

By combining GaAs with other materials into a multijunction cell, it is possible to precisely set the bandgap of each layer, hence making each layer absorb one part of the spectrum. By combining layers of different materials it is possible to cover the entire visible range of light using layers that are highly efficient each in its own range of wavelengths ultimately allowing for a highly efficient overall cell design. Fig. 3.3 demonstrates an example of the suggested stack of different materials that promises to deliver efficiencies above 50% [89].

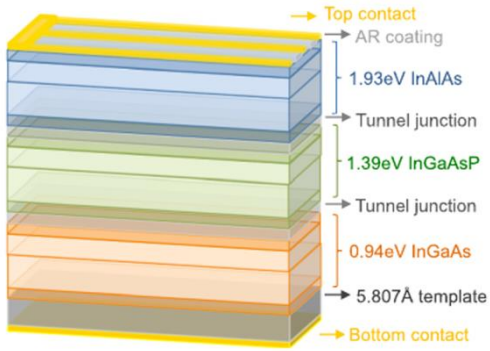


Fig. 3.3 A schematic of a three junction solar cell [89]

Amorphous silicon or amorphous hydrogenated silicon is a disordered network of silicon and hydrogen atoms. This material demonstrates a strong absorption of short-wavelength light making it a good candidate for both indoor and outdoor applications. The efficiency of these devices is quite low with the best modules initially being 8%-10% efficient. These cells degrade over time due to Staebler-Wronski effect and can lose up to 10% of their efficiency after a few months [5]. Solar cells used in calculators are typically 5% efficient.

The efficiency of these solar cells is unlikely going to rise to levels seen in other types of silicon based cells; however, their cost per watt is low, making them an important technology for low-power indoor applications [16].

Organic solar cells are a result of developments in the area of semiconductor organic materials, mainly the development of conductive plastics that are being applied to flat screens. These materials have demonstrated photoelectric properties and can be used as generators. The production of organic solar cells is still in the research phase. Some research groups have reported efficiencies of up to 8.7% [59] with projections to pass the 10% mark.

2.3. Concentrated Photovoltaic

The theoretical limit of single junction solar cells is defined by the Shockley–Queisser limit to 33.7% [140]. The maximum theoretical limit for multijunction solar cells is 86.8% [61]. These efficiencies are rated at the light levels equal to one sun. Higher efficiencies can be achieved by concentrating the light energy onto a solar cell [85]. The fact that GaAs based cells have a higher temperature tolerance makes it is possible to use optics to concentrate more light energy onto a smaller surface. The increasing of the solar cell's temperature beyond 100°C can reduce the overall efficiency of the solar cells in the order of 7% [106].

Beside increased efficiency, using concentrated solar approach requires smaller sized cells, hence reducing the use of expensive materials required in the manufacturing of the high efficiency multijunction solar cells [85].

In order to provide maximum utilization of the light source the light needs to be focused on the solar cell. However, for solar cells deployed in the outdoors, the relative movement of the Sun is going to change the angle at which the light falls onto the cell. In case of optics that have low concentration <3x, tracking is not required as lenses are capable of concentrating enough light even when the angle is not optimal. However, in case where medium (3x-100x) and high concentrations (>400x) are used tracking of the light source becomes imperative.

Using luminescent concentrators is another option to increase the amount of collected light. In this approach the solar cell is placed on the side of a waveguide that is coated with the material designed to absorb the incoming light and reemit it inside the waveguide. In this case it is possible to have large area of luminescent material that concentrates its output onto a single solar cell [85].

2.4. Solar Cell Properties

This section will be dedicated to the solar cell electrical characteristics. The solar cell properties, such as the efficiency of the solar cell, fill factor, open circuit voltage, short circuit voltage, spectral response of the cell are going to be covered in this section. Additionally a single diode model of a solar cell will be presented in the end.

2.4.1. Solar Cell Efficiency

One of the most important parameters of a solar cell is its electrical efficiency and the output power. By sweeping the load resistance attached to the solar cell and measuring its voltage it is possible to determine the point where the solar cell has the maximal output. Typical solar cell output characteristics are shown in Fig. 3.4.

The maximum power point is usually located after the 'knee' in the I-V characteristic of the solar module. The characteristic of a solar cell power output is that when the voltage crosses, the maximum power point the available power drops fast. This can be seen in Fig. 3.4.

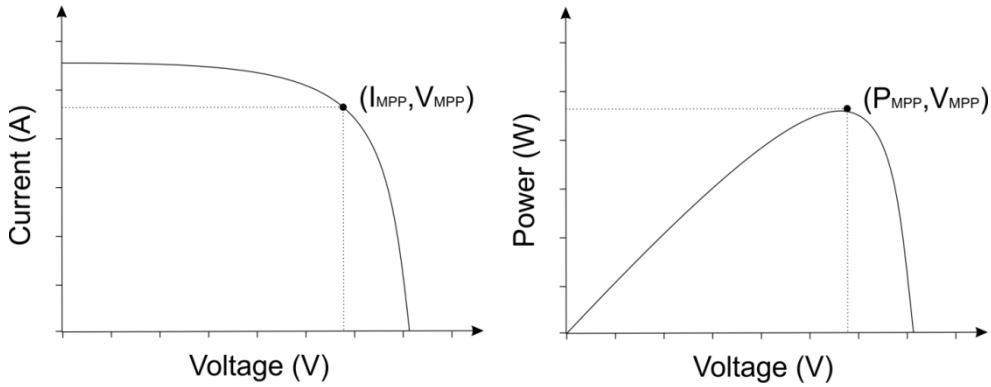


Fig. 3.4 Solar cell typical current-voltage and output power-voltage characteristic with maximum power point indicated on the graph

The value of power at the maximum power point (MPP) can be used to calculate the overall efficiency of the cell as the ratio of output power and input power:

$$\eta = V_M I_M / P_I \tag{3.1}$$

where η is the calculated efficiency, V_M and I_M are the voltage and the current of the solar cell at the maximum power point, while P_I is the input power to the cell.

Fig. 3.5 illustrates the efficiencies of different solar cell technologies and demonstrates the trend in the efficiency changes.

2.4.1. The Fill Factor

Beside the efficiency metric, another factor is used that is based on MPP. This is the fill factor (FF) and represents the ratio of the area covered by $V_{MPP} \times I_{MPP}$, and area covered by $V_{OC} \times I_{SC}$, where V_{OC} are I_{SC} the open circuit voltage and short circuit voltage of the solar cell, respectively. The graphical representation of the fill factor is given in Fig. 3.6.

The formula for FF calculation is straightforward:

$$FF = \frac{V_M I_M}{V_{OC} I_{SC}} \tag{3.2}$$

The overall efficiency of the solar cell is dependent on the fill factor, open circuit voltage and the short circuit current.

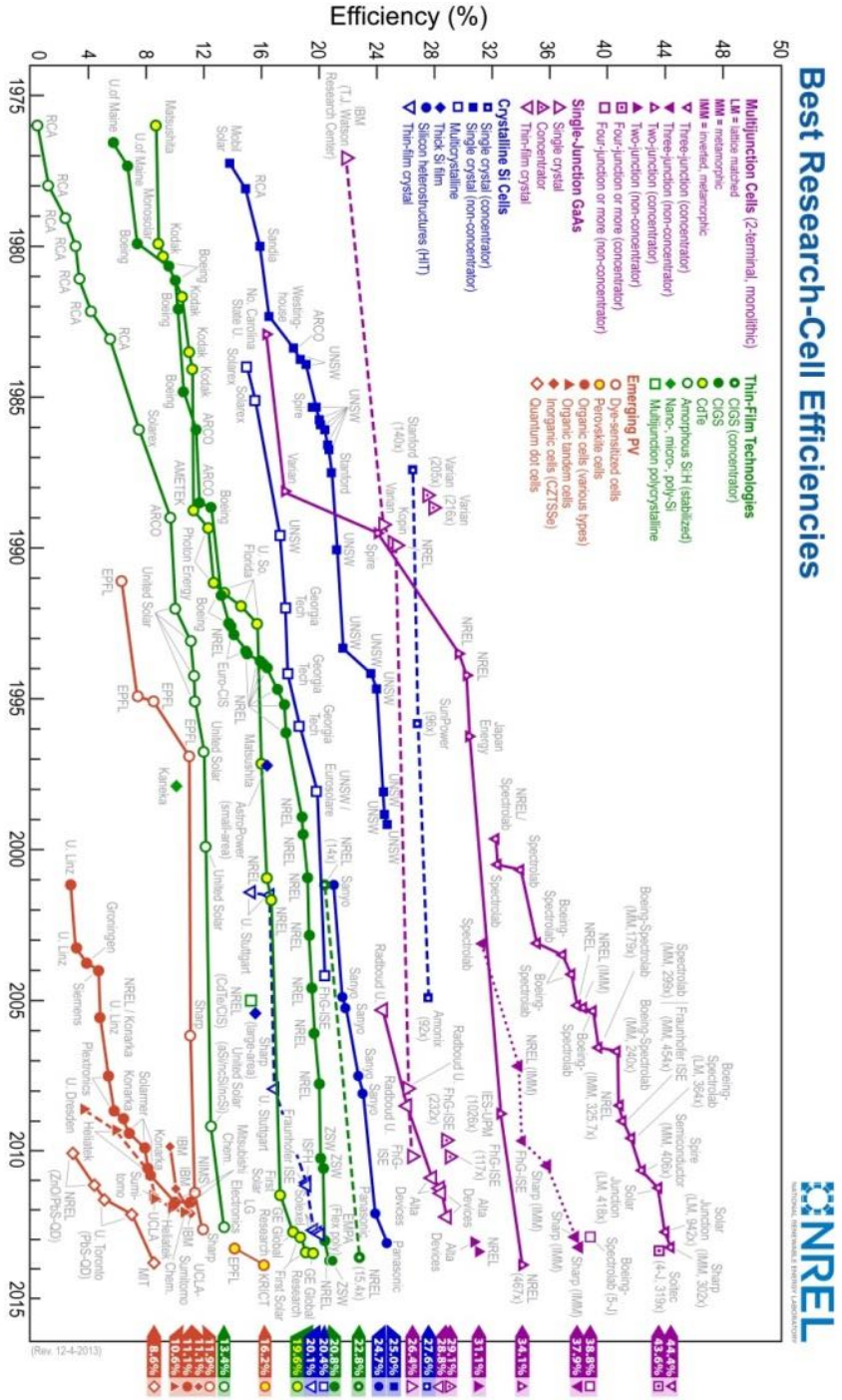


Fig. 3.5 Change of the efficiency of different photovoltaics thought the years [85]

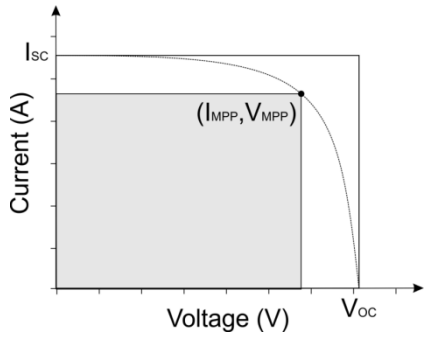


Fig. 3.6 The Fill Factor of a solar cell

2.5. The Solar Cell Modeling

In order to better understand losses that occur in solar cells a simple, one diode model will be introduced [121]. Although there are more precise solar cells models [80, 16, 121] this model is capturing enough details to model the basic operation of a solar cell. The schematic of the electrical model is shown in Fig. 3.7. The equations used for describing the model are [121]:

$$I_D = I_0 \left[e^{\frac{V_{PV}}{\alpha V_T}} - 1 \right] \tag{3.3}$$

$$I_{PV} = I_{SC} - I_D \tag{3.4}$$

$$V_{PV} = \alpha V_T \ln \left[\frac{I_{SC} - I_{PV}}{I_0} + 1 \right] \tag{3.5}$$

where V_{PV} is the voltage on the output of the solar cell, I_{PV} is the current output of the cell, I_0 is the reverse saturation current of the diode, I_D is the diode current, V_T is thermal voltage expressed as kt/q which is 25.85 mV at 25 °C, the factor α represents the ideality factor and varies between 1 and 5.

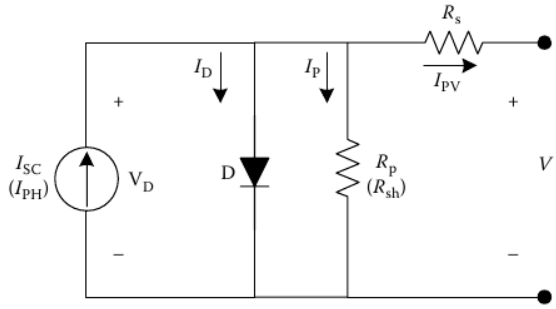


Fig. 3.7 The single diode electrical model of a solar cell [121]

The solar cell series resistance, R_S, is originating from bulk resistance and metal contacts. The parallel resistance R_P is caused by the leakage on the cell edge or defects in the material. These defects can include grain boundaries, dislocation and large precipitates. The resistive losses are the ones having the largest impact in the fill factor.

In the cases of high efficiency photovoltaic modules R_S and R_P can be neglected leaving only the current source and the diode in the model.

2.6. Spectral Response of Solar Cells

The losses in solar cells originate from three mechanisms:

- Optical issues – spectral mismatch and shadow induced by the electrical contact of the top electrode
- Material quality issues
- Parasitic resistance

The majority of solar cell losses (>50 %) are coming from the spectral mismatch [121]. The spectral mismatch occurs when the incident photon has more or less energy than required to cross the band gap. As spectral losses are the predominant losses it is important to select solar cells that are going to be operating in the environment where they are the most efficient. Typical spectral response, for different solar cell technologies, are presented in Fig. 3.8.

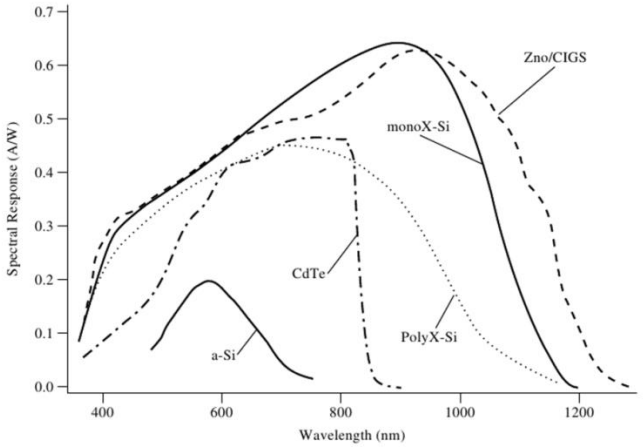


Fig. 3.8 Typical spectral response for solar cell technologies: a-Si = amorphous silicon; CdTe = cadmium telluride; Poly-Si = polycrystalline silicon; monoX-Si = monocrystalline silicon; ZnO = zinc oxide; CIGS = copper indium gallium diselenide [121]

Based on the knowledge of the typical spectral responses, a proper solar cell technology can be selected when the wavelengths of the light sources are known. In Fig. 3.9 typical spectral response of indoor amorphous solar cells has

been shown together with the wavelengths of typical light sources [121]. In order to use the cells efficiently the spectral response of the cell has to match the wavelengths of the light sources.

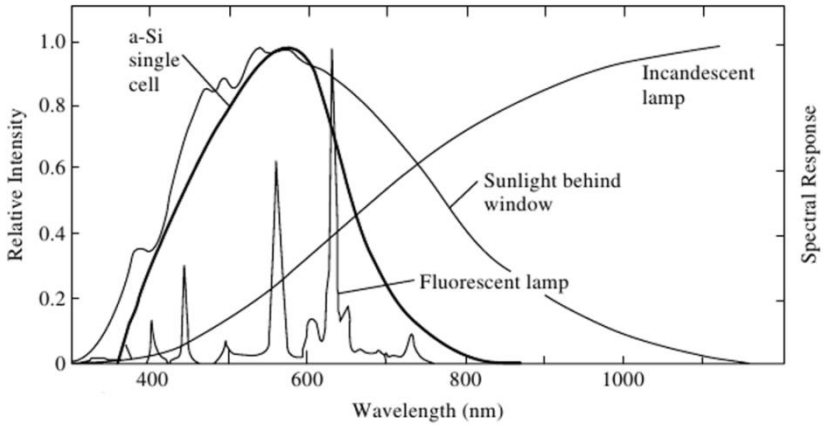


Fig. 3.9 Qualitative comparison of light source spectra and an amorphous silicon (a-Si) single cell [121]

The highest interest is matching the high frequency part of the spectrum to the solar cell's spectral response. This is necessary because they represent the shorter wavelengths which carry higher energy photons and thus hold the potential to generate higher levels of power.

2.7. Shading Effect on Solar Cells

In case of large solar cell modules, shading can become an issue in the system. Shading occurs when one part of the solar cell module is receiving less light due to some obstructions. In case of the energy harvesting wireless sensor applications, shading can occur due to parts of solar cell being covered by leaves, debris, dirt, residue after precipitation etc. There are two typical shading scenarios: (i) The shading is severe and the solar cell stops acting as a generator and start behaving like a regular diode; (ii) under the circumstances that the solar cell is only partially shaded the output characteristic of the solar cell array can get the shape shown in Fig. 3.10. One or more local maximum could be formed and which could potentially interfere with the electronics attempting to localize the MPP.

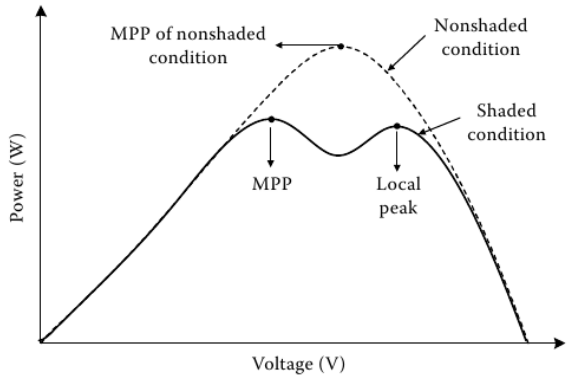


Fig. 3.10 MPP relocation under shaded condition [80]

2.8. Light Energy Harvesting Summary

The research is driven by the requirements for a cheap and efficient solar power. With the increase of efficiency of solar cells, more power will be available for the low power system, without changing the size of the cell. This in turn means that the cell's size could be reduced while maintaining the output characteristics needed by the original application

This section has provided an overview of currently available technologies and trends in solar energy harvesting. The main characteristics of solar cells were addressed together with examining the main contributors to the cell losses.

3. Kinetic Energy Harvesting

The energy harvested from the light sources can be sufficient to power small electronics in some of applications. However, there is a large number of applications that require operation in low light conditions, or without access to any light sources. Additionally, in the case of low light conditions, the surface area of the solar cell required to produce sufficient power for running the electronics, can be impractically large. Furthermore, there are a lot of applications where dust and other obstacles could cover the solar cell, thus reducing its power output. All these shortcomings can be a limiting factor for viability of light energy use in some applications. Example applications can be found in an industrial environment where the position of the mounted sensor node would make the solar cell exposed to both low light and unclean conditions.

A possible alternative to powering electronics from photovoltaics could lie in converting the energy of movement into electrical energy. The conversion of the kinetic energy to electrical power has been used as a primary source of electrical power generation. Power plants, dams, windmills, use this principle in large generators to provide electrical energy for the mains supply.

Kinetic energy harvesting was the first energy harvesting principle to be used with low power devices. The first self-winding pocket watch was patented in 1770. by Swiss watch manufacturer Abraham-Louis Perrelt. Later throughout the twentieth century the concept was further refined. Watches that had a self–winding mechanism used a rotating inertial mass that moved with the movement of the user's arm. The motion of the inertial mass was then used to wind the clock. In modern versions, using a series of connected gears, the inertial mass would drive a small micro-generator that would in turn charge a battery. The company Kinetron (http://www.kinetron.nl/) is one of the manufacturers of micro-generators which are as small as 4mm in diameter while generating 10mW of power.

The kinetic energy is present in various forms: vibrations, human movement, air/water flow, changes of pressure, etc. Vibrations are present in a wide variety of applications from industrial equipment, through household appliances, moving structures such as cars, airplanes, to civil structures such as buildings and bridges.

4. Linear Oscillating Systems

The majority of vibrating sources oscillate in one direction. Therefore, the harvesters used to convert those oscillations to electrical energy can be modeled as a spring-mass damping system [16]. An important characteristic of the spring-mass damping system is its resonant frequency. At this frequency the amplitude is magnified by the quality factor of the circuit. This in turn means that a higher amount of mechanical energy is being transferred from the environment to the harvester, hence increasing the available energy output of the harvester.

The spring-mass damping system can be modeled using a seismic mass m, on a spring of the stiffness, k. The energy loss of the system is represented by the damping coefficient, c_T, which combines the damping coefficient of the extracted electrical energy, c_e and the parasitic losses c_P. These components are connected to the inertial frame that is excited by an external sinusoidal vibration with the amplitude Y and the frequency ω. The external vibration is out of phase with the inertial mass when the structure is vibrated at resonance. The model of spring-mass damping system is shown in picture Fig. 3.11.

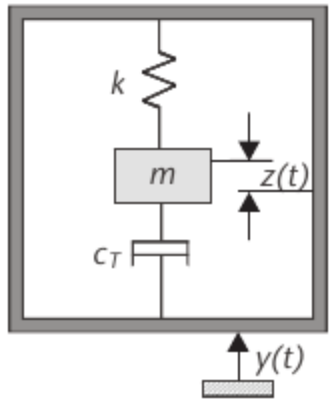


Fig. 3.11. Model of a linear, inertial generator [16]

The average power available for the vibration energy harvester, including the power delivered to the electrical loads and the power wasted in the parasitic damping, was defined by [178] as:

$$P(\omega) = \frac{m\zeta_T Y^2 \left(\frac{\omega}{\omega_n}\right)^3 \omega^3}{\left[1-\left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \left[2\zeta_T \frac{\omega}{\omega_n}\right]^2} \tag{3.6}$$

where ζ_T is the total damping ratio ($\zeta_T = c_T / 2m\omega_n$), Y is the amplitude of the vibration and ω_n is the natural frequency of the device, while the ω is the frequency of oscillation. Based on the formula (3.6) the maximum power is generated when the device is driven at its natural frequency, ω_n. The output power at this point can be described using the following equation:

$$P_d = \frac{mY^2\omega_n^3}{4\zeta_T} \tag{3.7}$$

By analyzing the equation (3.7) it can be deduced that the power would reach infinity as the damping ratio is decreased to near zero. This, however, is not the case. The maximum power, which can be extracted by the transducer, is going to depend on the parasitic and the transducer damping ratio as shown in:

$$P_e = \frac{m\zeta_e A^2}{4\omega_n\left(\zeta_p + \zeta_e\right)^2} \tag{3.8}$$

where $A=\omega_n^2 Y$ is the excitation acceleration level, ζ_p is the damping ratio of the parasitic elements and ζ_e is the damping ratio of the transducer. The maximum power generated is obtained for $\zeta_e = \zeta_p$. The parasitic damping is unavoidable in practical implementations. In order to maximize the power

output both the resonant frequency and the damping level should be designed to match the specific application requirements.

Another important conclusion that can be drawn from the formula (3.8) is that the power output is inversely proportional to the natural frequency of the generator. Therefore, it is preferable to operate at the lowest available fundamental frequency of the source. Before selecting a frequency, at which the generator should operate, a careful study of the sources vibration spectra should be performed. This is done in order to determine the most appropriate frequency in regard of the acceleration, the generator size and the maximum permissible displacement. An example of acceleration and frequency content of different example vibrations is shown in Fig. 3.12 [145].

When analyzing the vibration spectra it is beneficial to convert the acceleration measurements from the time to the frequency domain using the Furrier transformation. This will allow an easier identification of the natural frequencies of the vibrating object that the energy harvester should be tuned to.

The molding machine is an example of a typical rotating machine powered by the mains supply. As the frequency of the main AC line is 50Hz the rotating parts of the machine are typically going to have larger acceleration levels at 50 Hz.

On the other hand, a car and a tunnel boring machine are demonstrating a wide array of frequencies with different peak accelerations. In these applications further analysis is required in order to determine an optimal frequency for harvesting energy.

5. Kinetic Energy Harvesting Mechanisms

The kinetic energy is typically converted into electrical energy using electromagnetic, piezoelectric and the electrostatic mechanisms. These mechanisms are exploiting different physical effects to convert the mechanical energy into electrical current. The piezoelectric generators use the piezoelectric effect to generate a charge when strained. The electromagnetic harvesters are based on the fact that a coil, when subjected to a changing magnetic field, is generating electric current following the law of electromagnetic induction. The electrostatic harvesters are based on converting the energy required to perform capacitance change of a structure, induced by moving its electrodes, to electrical power.

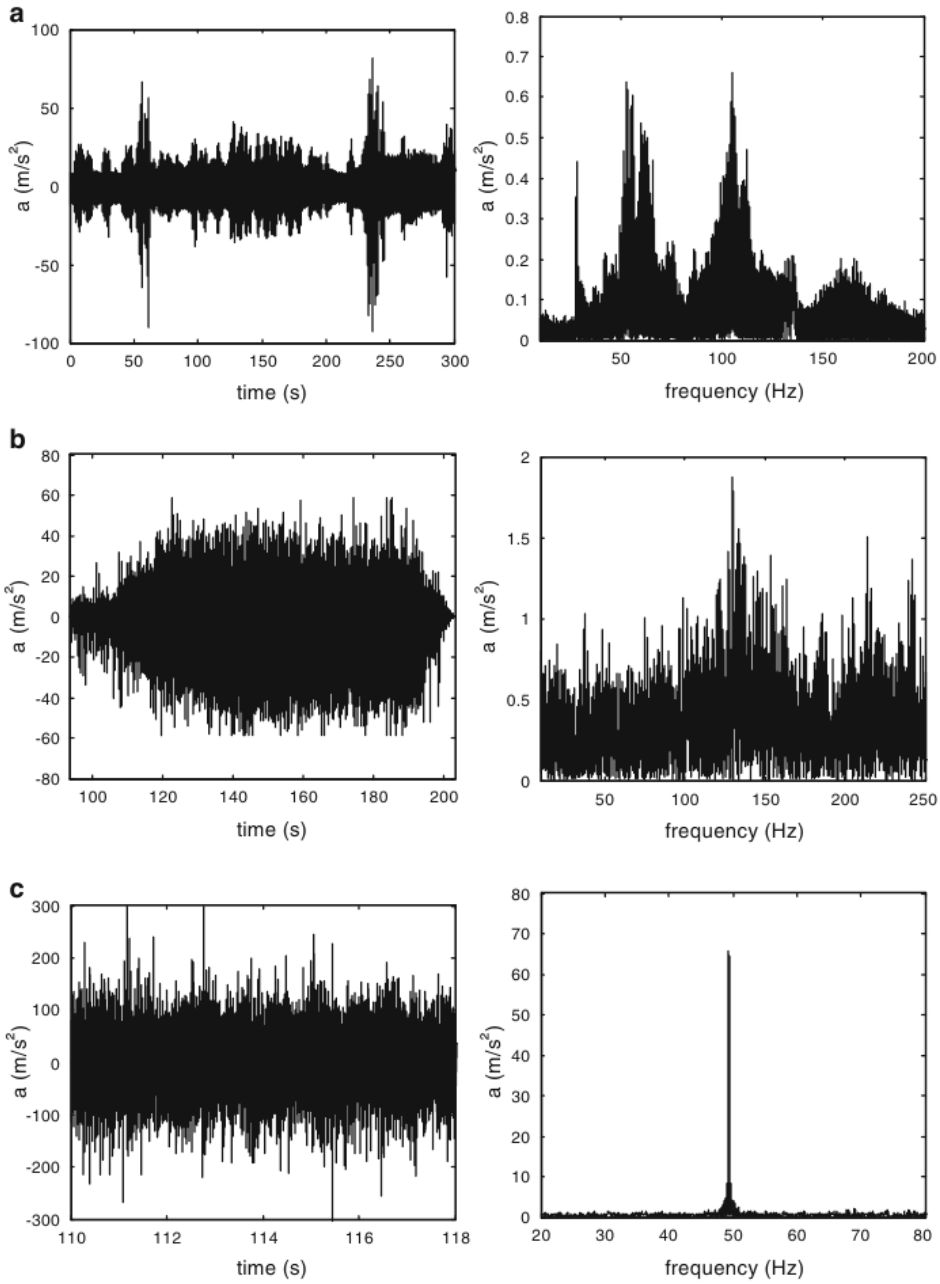


Fig. 3.12 The acceleration (left) and the frequency (right) of different example vibration sources: (a) air-filter housing of a car engine during country driving route, (b) tunnel boring machine close to the chisel and (c) mold for fabrication of concrete products [145]

Every approach to converting the energy from the mechanical to the electrical domain has its advantages and drawbacks. The piezoelectric elements typically produce voltages in order of volts or tens of volts, therefore, the output of the harvester could be used directly with off the shelf components, without a need for a complicated power management. However, the piezoelectric generators often have high output impedances which lead to very low output currents. On the other hand, the output of the electromagnetic energy harvesters is low impedance, but has a voltage level that is typically lower than required for the rest of the circuit to operate. As a result there is in a need for an additional power stage to adapt the output voltage levels to the requirements of the circuits attached. Both of these methods can operate without a need for pre-charging. In contrast, the electrostatic harvesting approach requires that the harvester has a voltage applied before the each cycle of vibration begins. This implies a need for a more sophisticated control circuitry. On the plus side, the electrostatic harvesters are very convenient for implementation in microelectromechanical (MEMS) system applications, as they are compatible with the standard MEMS manufacturing process. The possibility to have a power source manufactured together with the sensor and the control electronics, on a single chip are making the electrostatic harvesting an interesting research topic. The other two approaches to kinetic energy harvesting, previously discussed, are not as promising when it comes to micro-scale implementations. Piezoelectric harvesters can be scaled down due to advancements in thin film production technologies. However, their power density drops 50% compared to their bulk implementations [16]. In case of electromagnetic harvesters the poor properties of planar magnets, in conjunction with a limited number of coil turns that can be implemented, are severely limiting their practical applications in micro-scale [49, 16]. A summary of some main advantages and disadvantages of kinetic energy harvesting mechanisms are presented in Table 3.1 [88].

In the following sections the piezoelectric, the electromagnetic and the electrostatic harvesters will be reviewed in detail. The main focus will be on their principle of operation and optimizing the power output.

Table 3.1 Advantages and drawbacks of kinetic transducers [88]

	Piezoelectric devices	*Electromagnetic devices*	*Electrostatic devices*
Advantages	-high output voltages -high capacitances -no need to control any gap	-high output currents -long lifetime proven -robustness	-high output voltages -possibility to build low-cost systems -coupling coefficient easy to adjust -high coupling coefficients -size reduction increases capacitances
Drawbacks	-expensive (material) -coupling coefficient linked to material properties	-low output voltages -hard to develop MEMS devices -may be expensive (material) -low efficiency in low frequencies and small sizes	-low capacitances -high impact of parasitic capacitances -need to control µm dimensions -no direct mechanical-to-electrical conversion for electret-free converters

6. Piezoelectric Energy Harvesting

Piezoelectric materials exhibit the direct and the converse piezoelectric effect. The direct piezoelectric effect is the characteristic of the material to produce an electric polarization proportional to the applied mechanical strain. The converse piezoelectric effect is the reverse effect from the direct piezoelectric effect. When the material is subjected to an electric polarization it mechanically strains proportional to the applied polarization. The piezoelectric effect is found in variety of materials, such as single crystal materials, ceramics (piezoceramics), thin film materials, screen printable thick films based upon piezoceramic powders and polymer materials. The typical examples of piezoelectric materials are the PZT (lead zirconate titanate), signal crystal PMN-PT (lead magnesium niobate-lead tinanate) or semi-crystaline polyimer, such as polyvinylidene fluoride (PVDF)

The piezoelectric properties of a material are characterized by a series of constants that have been summarized in [16] and are presented in the Table 3.2. The piezoelectric materials demonstrate an anisotropic behavior consequently the constants will have different values based on the directions of the applied strain and the orientation of the polarization. The subscripts of constants are defined by direction of the applied stress and polarization in reference to the axes of the material. The 3 direction indicates that the piezoelectric material has been polarized along their thickness, i.e. the electrodes are placed on the top and the bottom surfaces. If the mechanical strain is applied in the same direction (through the thickness of the material) then the constants are denoted with subscript 33. In the case where the strain is applied perpendicular to the thickness of the material, this is referred to as 1

direction and similarly the constants related to this mode of operation have subscript 31.

Table 3.2 Piezoelectric Material Properties [16]

Property	*Constant*	*Definition*	*Units*
Electromechanical coupling coefficient	k	√(mechanical energy stored ÷ electrical energy applied) √(electrical energy stored ÷ mechanical energy applied)	
		strain ÷ applied field	m/V
Piezoelectric constant	d	short circuit charge density ÷ applied stress	C/N
		open circuit field ÷ applied stress	V/N
Piezoelectric constant	g	strain developed ÷ applied charge density	m/C

In the most cases the piezoelectric harvesters operate in the lateral 31 mode. This is a result of typically bonding the piezo element to a surface of a cantilever that converts the vertical displacement into the lateral strain across the piezoelectric element. Some designs operate in the compressive 33 mode that is typically more efficient than 31 mode. However, the strains induced by compressing the structure are often lower than the lateral strains. The two approaches of applying strain to the piezoelectric element are shown in Fig. 3.13. The coefficients of common piezoelectric materials are obtained from [16] and presented in Table 3.3.

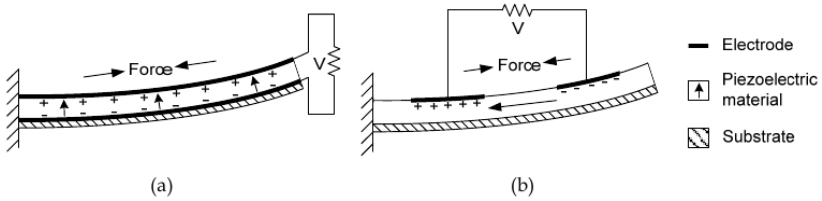


Fig. 3.13. Two types of piezoelectric harvesters (a) d_{31} mode (b) d_{33} mode [150]

Table 3.3 Coefficients of Common Piezoelectric Materials [16]

Property	*Quartz*	*PZT-5H*	*PZT-5A*	*$BaTiO_3$*	*PVDF*
Material type	Single crystal	Piezoceramic	Piezoceramic	Piezoceramic	Polymer
d_{33} (10^{12} C/N)	-2.3 (d_{11})	593	375	149	-33
d_{31} (10^{12} C/N)	-0.93 (d_{13})	-274	-171	78	23
g_{33} (10^{3} Vm/N)	-58	19.7	24.8	14.1	330
g_{31} (10^{3} Vm/N)	-	-9.1	-11.4	5	216
k_{33}	0.07	0.75	0.71	0.48	0.15
k_{31}	-	0.39	0.31	0.21	0.12
Relative permittivity ($\varepsilon/\varepsilon_0$)	4.4	3400	1700	1700	15
Curie temperature (C)	573	195	365	120	150

The typical approaches to realizing the piezoelectric energy harvesters have been summarized in Fig. 3.14 obtained from [47].

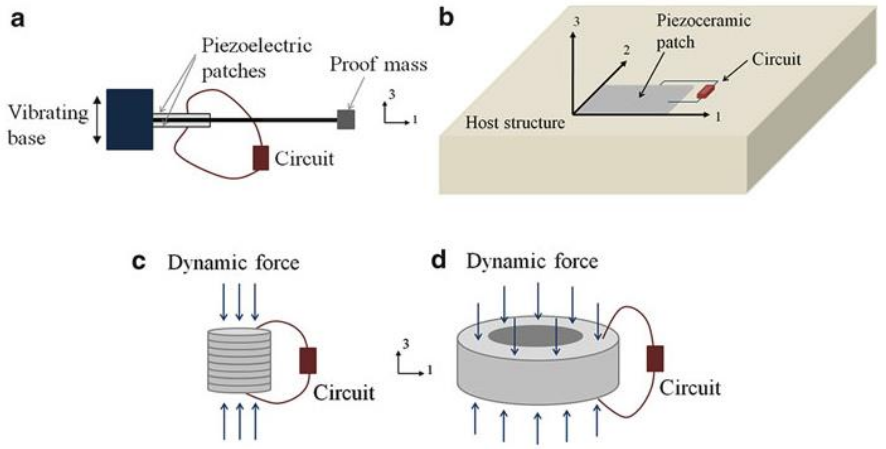


Fig. 3.14 Typical piezoelectric energy harvester configurations: (a) bimorph piezoelectric cantilever under base excitation, (b) piezoelectric patch harvesting surface strain energy (c) multilayer piezoelectric stack and (d) monolithic element under compressive loading [47]

The cantilever harvester is an example of inertial based system that can be described using the model presented in Section 4. This harvester type is a good choice for applications that have well defined natural frequencies. Regarding the other examples: the mechanical quality factor has little or no effect on the performance of a patch attached to a large structure (Fig. 3.14-b) or a compressed stack at low frequencies (Fig. 3.14-b and c). These configurations are better suited for the off-resonant applications such as the scavenging from shoes during walking [47].

Based on the maximum power transfer theory, the load will receive the maximum power from the generator only when the load is matched to the generator. In order to determine the optimum load for a piezoelectric generator it is necessary to determine the damping coefficient first. This coefficient has been determined in [126]:

$$C_e = \frac{2m\omega_n^2 k^2}{2\sqrt{\omega_n^2 + {}^1/_{(R_{load}C_{load})^2}}} \tag{3.9}$$

where k is the electromechanical coupling factor of the piezoelectric material and C_{load} is the load capacitance, m is the inertial mass and ω_n is the natural frequency of the cantilever. The value of the resistive load can be calculated to determine the optimum electrical damping ratio, thus maximizing the

generated power. The optimum value for R_{load} occurs when the mechanical damping ratio ζ_p is equal to electrical damping ratio, thus resulting in:

$$R_{opt} = \frac{1}{\omega_n C} \frac{2\zeta_p}{\sqrt{4\zeta_p^2 + k^4}} \tag{3.10}$$

By connecting the optimal load to the piezoelectric generator maximum power will be transferred from the mechanical to the electrical domain, hence increasing the efficiency of the harvester.

7. Electromagnetic Induction Harvesting

The majority of the modern generators are based on the electromagnetic induction to convert the mechanical rotational energy to the electric energy. When not constrained in size, the electromagnetic harvesters can be very efficient in converting the rotational energy to the electric power. The principle of the electromagnetic induction is based on Faraday's Law, which states that "*an electrical current will be induced in any closed circuit when the magnetic flux through a surface bounded by the conductor changes*". The voltage induced in the conductor (V) is proportional to the rate of change of the magnetic flux (ϕ) in time through the conductor. In a practical implementation of a generator the conductor is typically a multi-turn coil (consisting of N turns) and the magnetic field is created by permanent magnets. The formula for generated voltage potential is:

$$V = -N\frac{d\phi}{dt} \tag{3.11}$$

When the circuit is closed using a load, induced current runs through it. As the current flows through the coil it is generating a magnetic field around it that opposes the filed that is inducing the current. This action is generating a force that dampens the movement of the generator. The external mechanical energy is used to act against this opposing force, hence keeping the generator moving, thus continuing to generate electrical energy.

The dampening coefficient of induced current was defined in [45] as:

$$c_e = \frac{(NlB)^2}{R_{load} + R_{coil} + j\omega L_{coil}} \tag{3.12}$$

where N is the number of the turns in the generator coil, l is the side length of the coil and B is the magnetic flux density the coil is exposed to. The R_{load} is the load resistance and R_{coil} and L_{coil} represent the coils resistance and inductance, respectively. The formula (3.12) is an approximation and only suitable for cases where the coil moves from a high magnetic field region B to a zero field region. In other cases it is very hard to analytically deduce the dampening coefficient due to complex nature of the magnetic field. Therefore, for these cases a value can be determined using a finite element analysis (FEA) on the system. The factor NlB is the electromechanical coupling factor and is denoted as K [146].

The maximum output power of an inertial oscillator is generated when the mechanical dampening ratio is equal to the electrical dampening ratio. Therefore, by adjusting the load resistance attached to the circuit, it is possible to achieve the maximum power output. The optimum value for the R_{load} was calculated in [146] as:

$$R_{load} = R_{coil} + \frac{K^2}{c_m} \tag{3.13}$$

where c_m represents the mechanical (parasitic) dampening of the system. Based on the equation of the maximum power output of the linear oscillator (3.8) the maximum average power can be calculated as [146]:

$$P_{eloadmax} = \frac{mA^2}{16\zeta_p\omega_n}\left(1 - \frac{R_{coil}}{R_{load}}\right) \tag{3.14}$$

From the expression (3.14) it can be easily concluded that the internal resistance of the coil should be minimized while maximizing the electromechanical coupling K, which will in turn, maximize the optimal load resistance, ultimately leading to maximizing the power delivered to the electrical load.

8. Electromagnetic Coupling Architectures

In order to provide the maximum power output for a given application it is necessary to select an appropriate electromagnetic coupling method between the coil and the magnet. The coupling effect is largely going to depend on the geometric properties of the magnet and the coil. The biggest challenge in designing the harvester lies in the magnetic field analysis, which is rather complicated and often requires using the finite element modeling.

In the literature there are a lot of proposed configurations of magnets and coils. Based on the relative position of the coil and the magnet, majority of the architectures can be placed into one of the two categories [145]:

- The "Magnet In-Line Coil" architecture
- The "Magnet Across Coil" architecture

Both of these architectures can be realized with or without the back iron. The back iron is added ferromagnetic material that is used to concentrate the magnetic field hence increasing the magnetic flux. Some of the different possible architectures for the both categories are shown in Fig. 3.15.

8.1. The "Magnet In-Line Coil" Architecture

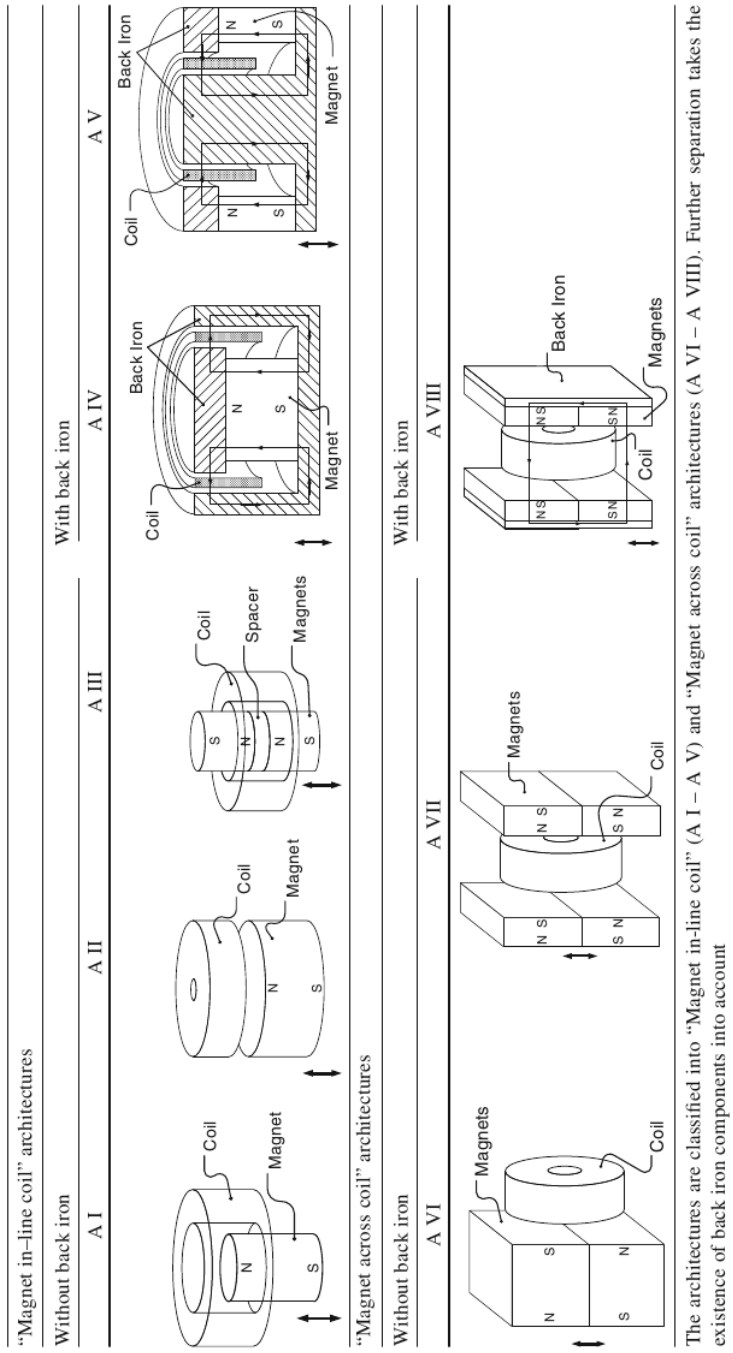
In the "Magnet in-line coil" architecture the coil's and the magnet's center axis is in line with the oscillation. These architectures, with and without the back iron, are marked as first architecture (*A I)* to fifth architecture (*A V)* in Fig. 3.15

A special characteristic of the structure *A I*, where a cylindrical magnet oscillates inside the coil, is that the optimal resting position of the magnet is not directly apparent. When the magnet travels through the structure, at some point, the transduction reaches the maximum point. For this architecture this is the optimal resting position for the magnet. In the architecture *A II* the magnet oscillates above the coil without immersion. The optimal resting place for this architecture is at maximum inner displacement of the magnet. For architecture *III* the optimal resting place is in the middle of the coil as the structure is symmetrical.

The architectures *IV* and *V* are derived from the magnetic circuits typically used for the electroacoustic loudspeakers. The only difference in these two architectures is the placement of the magnet. In one, the magnet is located in the center of the structure while in the other the magnet is ring-shaped and placed on the outer rim of the structure.

8.2. The "Magnet Across Coil" Architecture

In cases where the center axis of the magnet and the coil are orthogonal to the oscillation direction, the architecture is referred to as the "Magnet Across Coil". These architectures are also shown in Fig. 3.15. In architecture *VI* two rectangular magnets are oscillating across a cylindrical coil. Architecture *VII* is a variation of architecture *VI* where magnets are placed on both sides of the coil. The advantage of this architecture is that the magnetic field is going to be somewhat homogenized. However, this architecture has two gaps between the magnets and the coil instead of one in the architecture *VI*. Architecture *VIII* is based on architecture *VII* with the addition of the back iron in order to channel the magnetic field.

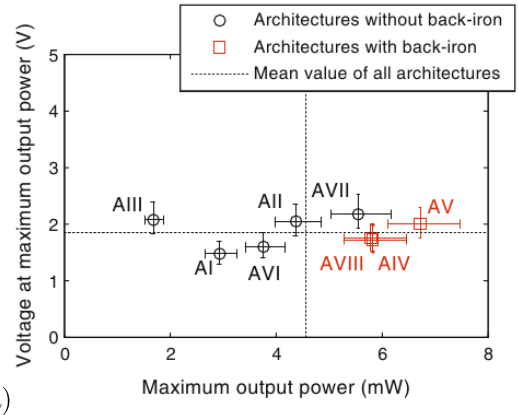


The architectures are classified into "Magnet in-line coil" (A I – A V) and "Magnet across coil" architectures (A VI – A VIII). Further separation takes the existence of back iron components into account

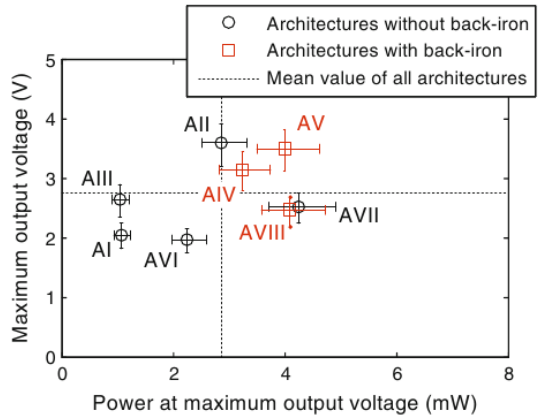
Fig. 3.15 Typically used electromagnetic coupling architectures [145]

A detailed explanation of the different architectures and how they can be optimized for a given application can be found in [145].

A comparison has been made between the proposed architectures in [145]. The design used for comparison was a harvester with the size constrain of $1cm^3$ that will be excited using a pure harmonic vibration with 10 m/s^2 at 100 Hz. The back iron used by architectures was standard low carbon steel 1010. The comparison was done for two different cases. In the first case the architectures were optimized for the maximum power output, while in the second case the architectures were optimized for maximizing the output voltage. The results of the architecture comparison for both cases are presented in Fig. 3.16.



a)



b)

Fig. 3.16 Comparison of the architectures with the optimized dimensions for the maximum power a) and the maximum voltage output b) at the maximum power points. The dashed curve indicates the mean value of all architectures. The errorbars indicate a variance of ±10% of the parasitic damping [145]

For each architecture there is a set of optimal geometrical parameters that leads to the maximum output power while another set leads to the maximum output voltage. In regard to the power generation, the top three architectures are *V*, *IV* and *VIII*. It should be noted that all top three architectures are ones that use the back iron in their realization, although it reduced the volume of the magnetic material.

In the case of rotary generators and generally architectures that rely on arrays of magnets with opposing poles located one next to the other (architectures *VI*, *VII*, *VIII*) it is possible to use a Halbach array of magnets in order to increase the magnetic flux density. The improvement of using this configuration instead of a magnetic element array has been demonstrated in [163]. It should be noted that although the magnetic segments are smaller in the case of the Halbach array, the fact that every second magnet is rotated is increasing the overall strength of the magnetic field, thus making it stronger than in the case of a standard multipolar magnetic disk. This is illustrated in Fig. 3.17.

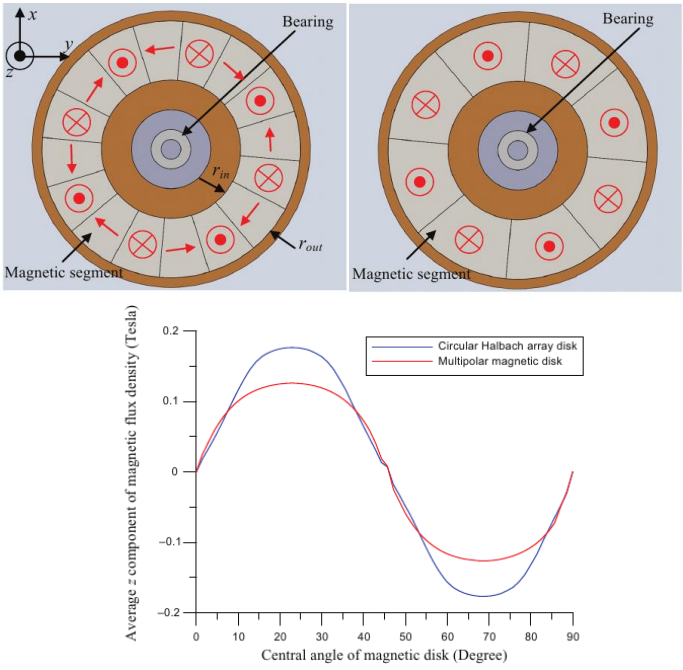


Fig. 3.17 Increasing the flux density of the magnetic disk using the Halbach array of magnets [163]

9. Electrostatic Energy Harvesting

The electrostatic transducers for energy harvesting are based on variable capacitors. A relative movement between two plates of a capacitor generates a capacitance variation that changes the level of stored energy in the capacitor. The increase of the energy can be then collected and stored. Depending on the method of operation these devices can be divided into two categories:

- Electret-free electrostatic transducers that use conversion cycles based on charging and discharging a capacitor. These devices require an active electronic circuit to apply the charge to the capacitive structure and this circuit must be synchronized with the capacitance variation.
- Electret-based electrostatic transducers are based on electrets hence are able to directly convert mechanical power into electricity without a need for an external supply

9.1. Electret-free Electrostatic Transducers

These devices are passive structures that require an external power source in order to operate. The operation of the harvester is based on charging the capacitance of the structure at the point where the capacitance is maximal. Then the mechanical force is being applied to the capacitor's plates working against the electrostatic forces inside the capacitor. This increases the energy of the capacitor. When the capacitance reaches the minimal value, the energy transfer from the mechanical to the electrical domain is complete and the cycle can repeat. The most commonly used approaches in harvesting are the charge constrained cycle and the energy constrained cycle. The following sections will address them in more detail.

9.1.1. Charge-constrained Cycle

The charge constrained cycle is depicted Fig. 3.18. The cycle starts when the capacitance has reached its maximal value (Q_1). At this point the external voltage is applied which changers the capacitor. After the charging is done the source is removed (Q_2). Following is the application of the external mechanical force that separates the electrodes of the capacitor. This results in work being done against the electrostatic forces, hence increasing the energy stored in the capacitor. As the charge on the plates is constant the increase of energy is manifested through the increase of the voltage across the capacitor (Q_3). When the application of mechanical force stops, the maximum voltage is reached and the accumulated energy can be used or stored (Q_4).

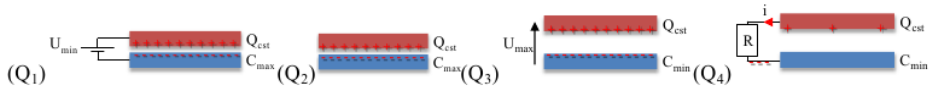


Fig. 3.18 The charge-constrained cycle [88]

The total energy gain using this structure is:

$$E_{Q=cte} = \frac{1}{2} Q_{cst}^2 \left(\frac{1}{C_{min}} - \frac{1}{C_{max}} \right) \tag{3.15}$$

where Q_{cst} is the amount of charge stored in the structure during operation and the C_{min} and C_{max} are the minimum and maximum capacitances realized on the structure during the conversion process.

9.1.2. Voltage-constrained Cycle

This cycle starts as well when the capacitance of the structure is maximized. The charge is placed in the capacitive structure (V_1). In comparison to previous cycle, as the mechanical force separating the two plates is applied, the voltage across the capacitor is kept constant. As the capacitance decreases, the charges increases, generating a current that is collected (V_2). When the capacitor reaches its minimum value, the charge is completely removed and stored (V_3). The operation of the voltage-constrained cycle is shown in the Fig. 3.18.

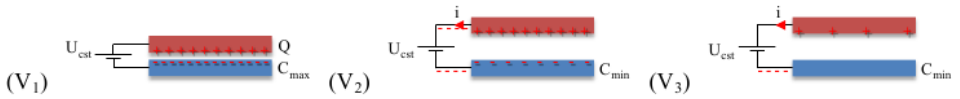


Fig. 3.19 The voltage-constrained cycle [88]

The total energy gain from using this type of harvester is:

$$E_{U=cte} = U_{cst}^2 (C_{max} - C_{min}) \tag{3.16}$$

where U_{cst} is the constant voltage applied during the process of harvesting while the C_{min} and C_{max} are the maximal and the minimal capacitances acheved during one cycle of operaion.

The constant voltage cycle produces higher energy levels compared to the constant charge cycle, however, it requires the electronics to provide a charging voltage that is typically different from the operating voltage of the rest of the electronics [16]. The charge constrained system requires simpler electronics but produces less energy. A hybrid approach has been proposed in [98] where the generator operates in the charge-constrained mode with placing a fixed capacitance in parallel. The drawback of this system is that higher amount of initial precharge is required before the conversion begins.

The common drawback of both cycles is the requirement for an external supply source that is used on the beginning of the each cycle to polarize the

structure. Furthermore, in order to maximize the efficiency of the structures, while keeping them small, high voltages are typically needed for polarization (>100V) and generating such voltages can be inefficient.

9.2. Electret-based Transducers

In order to avoid the need for external power source and high voltages, an electret can be used. The electrets are electrically charged dielectrics that are able to polarize the electrostatic energy harvesters avoiding the need for the external power source. The modern electrostatic energy harvesters are employing them extensively allowing them to perform direct mechanical to electrical conversion.

The basic principle of operation of these transducers is similar to the operation of the electret-free devices. It is also based on the capacitance change. The difference is in an added layer of electret material on one, or both, plates of the variable capacitor structure.

The electrets are dielectric materials that are in quasi-permanent electric polarization state. The key parameter of these materials is their lifetime. Electrets, as being dielectrics aren't perfect insulators, therefore, the free charges will recombine over time, thus reducing the electric field around the electret. Therefore, the choosing a stable electret during the development of an electret based kinetic energy harvesters is essential. Examples of electret materials are Teflon, SiO_2, CYTOP. Their characteristics are reviewed in [88].

The conversion principle of mechanical into electrical energy, as stated earlier, is similar to the conversion principle of the electret-free transducers. The structure of the electret based energy harvester is shown in Fig. 3.20. The electret is typically placed on one of the electrode plates, which leads to charging of electrodes due to the charge of the electret. During the charging process the charge is going to move through the load, hence producing useable electric energy. The total charge of the electret is Q_i, therefore, the charge available on the electrodes Q_1 and Q_2 is going to be Q_i=Q_1+Q_2 (Fig. 3.20a). When the capacitor geometry changes, this leads to redistribution of the charges on the electrodes, which in turn leads to flow of the charge through the attached circuit (Fig. 3.20b).

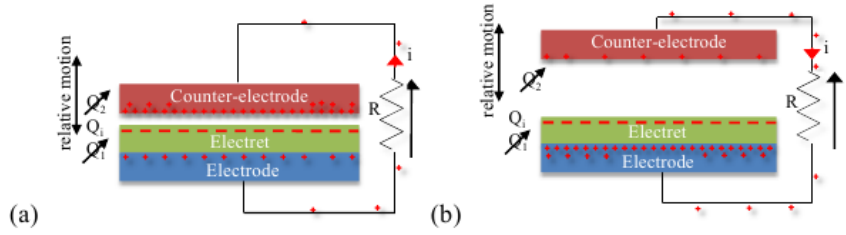


Fig. 3.20 Electret-based electrostatic energy harvesting operation princile [88]

The power harvested from the electret-based electrostatic harvester is dependent on the electret's surface voltage and the capacitance variation. The dependence has been determined in [19]. The output power approximation can be stated as:

$$P \propto V_s^2 \frac{dC}{dt} \tag{3.17}$$

It can be concluded that the generated power output is going to be primarily driven by the electret's surface voltage, *Vs.* This stresses the importance of selecting a stable electret, as the device's lifetime is going to be defined by the electret's lifetime.

An example of electret based system is demonstrated in [149] where a miniature harvester has been implemented that produced 3-33μW of power at 0.65G acceleration in the frequency range of 10-24Hz.

9.3. Construction of Electrostatic Energy Harvester

Three types of varying geometries are typically used for implementing electrostatic energy harvesters are:

a) In-Plane Overlap – the capacitance is changed by changing the overlapped surface area of the electrodes

b) In-Plane Gap Closing – the capacitance is changed by changing the distance between the electrodes

c) Out-of-Plane Gap Closing

The three approaches are depicted in Fig. 3.21 [150].

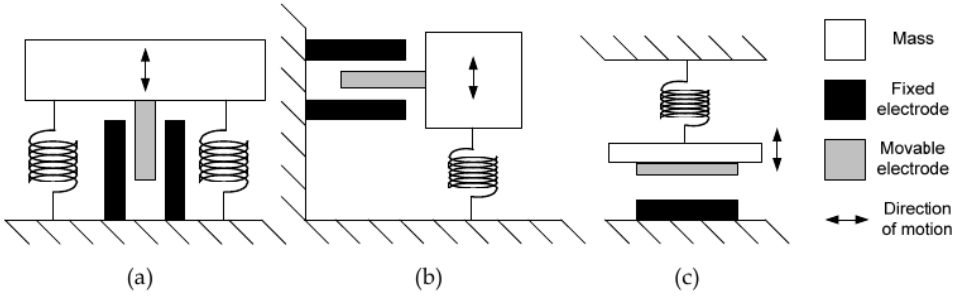


Fig. 3.21 Three types of electrostatic energy harvesters (a) In-Plane Overlap (b) In-Plane Gap Closing (c) Out-of-Plane Gap Closing [150]

In order to increase the surface area of the capacitor, hence its capacitance, the electrostatic generators are usually designed in a comb like structures as shown in Fig. 3.22 [15]

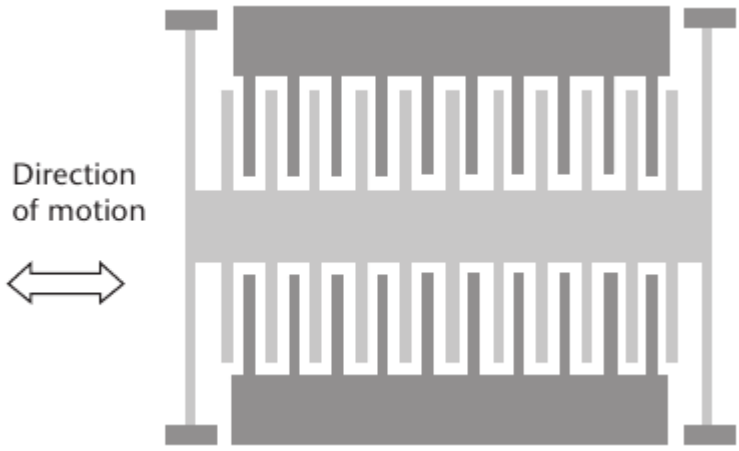


Fig. 3.22. Example of the in plane gap varying comb like structure used to increase the overall capacitance [16]

10. Optimizing Harvester's Frequency Response

In a real world scenario the objects that are vibrating seldom have a stable oscillating frequency, and even if they do, this frequency can drift over time due to the temperature variations, changes of the properties of the object and other external impacts. Furthermore, the resonant frequency of the harvester might be impacted by the manufacturing process, the temperature or aging, hence resulting in a mismatch between the frequency of the external vibration and the resonant frequency of the harvester. In the case of the resonant frequency harvesters, which are typically tuned with a high quality factor to a single frequency, this would result in a significant decrease of the output power. This limitation of operating at a single frequency is severely restricting the widespread implementation of linear energy harvesters. In [176] two approaches have been presented to solve this problem: the approach is to tune the energy harvester to a single frequency and then change it periodically when the ambient frequency changes. The second approach is to design harvesters with a wide bandwidth. A detailed review of broadband harvesters is available in [158]; some of these approaches will be addressed in more detail in the following sub-sections.

10.1. Frequency Tuning

The resonant frequency tuning can be achieved either in the mechanical or the electrical domain. In the mechanical domain the frequency of the system can be altered by altering the physical characteristics of the system such as: changing the dimension of the structure, moving the center of gravity of the

proof mass and changing the spring stiffness. In the electrical domain the tuning is performed by adjusting the electrical load attached to the generator.

10.1.1. Mechanical Tuning

The mechanical tuning is based on altering the construction of the harvester. The changes to the mechanic construction of the harvester can be employed continuously or intermittently. Continuous tuning is applied throughout the device's operation regardless if it is operating at the resonant frequency or not. On the other hand, intermittently tuning means that the system will be tuned occasionally based on the natural frequency of the exciting force. It should be noted that extra circuits and energy are typically required for the tuning task. Therefore, the tuning mechanism has to be carefully designed in order not to consume more energy than is gained by applying the tuning to the harvester.

In the case of a cantilever with a mass at the free end, the resonant frequency is given by [17]:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{Y\omega h^3}{4l^3(m + 0.24m_c)}} \tag{3.18}$$

where Y is the Yuong's modulus of the cantilever material; w, h and l are the width, thickness and length of the cantilever. The internal mass is denoted with m and m_c is the mass of the cantilever. The resonant frequency can be adjusted by changing any of these parameters, however, in practice it is challenging to change the width and the thickness of the cantilever. Changing of the length is the most suitable and a good option for intermittent tuning. The change of the length allows for a significant change in the resonant frequency as it is inversely proportional to $l^{3/2}$.

Although it is possible to change the resonant frequency by changing the mass attached to the cantilever, practical realization of such approach is difficult. However, it is possible to alter the resonant frequency by moving the center of the mass. In [168] such a system was demonstrated where two masses were used on the cantilever. One mass was fixed and the other mass could be moved in regard to the fixed mass. In this way the center of gravity of the cantilever could be altered resulting in an adjustable resonant frequency. This implementation allowed successful tuning of the energy harvester in the range of 130 Hz to 180 Hz.

Another possible approach is based on changing the stiffness of the cantilever. This can be done by adding an adjustable spring in parallel with the mechanical spring. The effective spring constant of such device will be equal to

the combined value of the two springs [16]. The piezoelectric tuning can be utilized as well to alter the stiffness of the cantilever. This was demonstrated in [44] where a piezo actuator was used to axially preload the cantilever. By adjusting the amount of the preload it was possible to adjust the resonant frequency in the range of 150 Hz to 190 Hz. The illustration of the device is shown in Fig. 3.23.

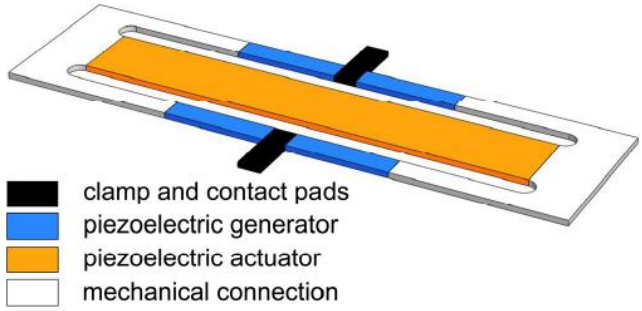


Fig. 3.23 The scheme of the tunable generator [44]

It should be noted that this device is capable of self-tuning and the energy required for tuning is provided by the harvester energy making this device self-sufficient.

Magnetic force can be used as well to provide tuning of resonant frequency as reported in [176]. The tuning in this case was performed by applying an axial tensile magnetic force to the cantilever as sown in Fig. 3.24.

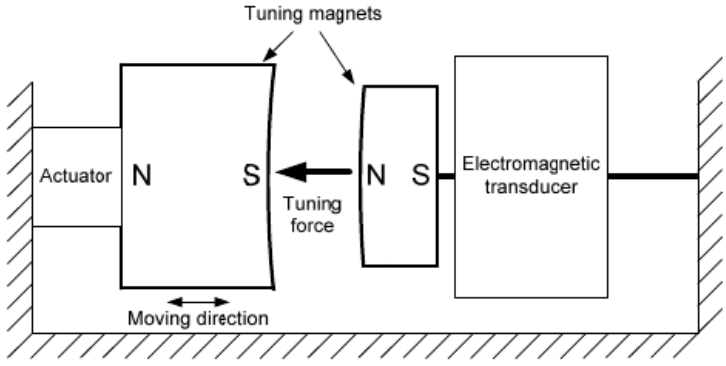


Fig. 3.24 Frequency tuning by applying magnetic force [176]

One magnet was fixed to an end of the cantilever while the other magnet was set to be moved by an actuator. The change of distance between magnets resulted in the change of resonance frequency. For this device the tuning range was from 67.6 Hz to 98 Hz while changing the distance between the magnets

from 5 to 1.2mm. The control system for this harvester was realized in [13] where the energy for the control and the operation of the actuator was provided by the harvester, thus allowing for a self-sufficient self-tuning energy harvester.

10.1.2. Electrical tuning

All previous approaches were based on mechanical tuning. Mechanical tuning has a drawback that it requires additional mechanical structures to be implemented on the harvester (piezoelectric elements, magnets, additional masses). Although they provide large tuning range possibilities, they also require significant energy to operate.

Another possibility to tune the harvester is by using the variation of the electric load connected to the transducer. It can be observed that the deflection of a cantilever, with a piezoelectric material attached, is higher when it is placed in a short circuit compared to an open circuit configuration. This means that the stiffness is lower in the case of short circuit condition than in the open circuit condition. Hence by varying the electric load the stiffness of the cantilever can be altered, resulting in a change of the resonant frequency.

It should be noted that by regulating the load by using a resistive element the quality factor of the oscillator would be reduced due to energy dissipation. Therefore, it is necessary to implement a varying a non-dissipative element such as capacitor or inductor. Several topologies of switched mode converters are able to emulate variable reactive loads. An example circuit that emulated a variable capacitor on the output of the generator was demonstrated in [6]. A tuning ratio of 13%-15% was reported for this circuit. Another approach was presented in [101] where a specially designed AC-DC converter was used to control the real and the reactive power exchange between electrical and the mechanical domains. This circuit allowed a tuning ratio of $\pm 10\%$.

10.2. Bandwidth Widening

Instead of applying a mechanism to adjust the resonant frequency when the frequencies of the exciting force and the resonant frequency don't match, another approach is to design the harvester with a wide bandwidth. There are several ways to implement this. This section is going to focus on approaches that include oversizing the system, combining an array of narrow bandwidth harvesters, use of bi-stable harvesters and implementation of nonlinear structures.

A direct approach to widen the bandwidth is to have a heavily damped inertial generator. In this case the power output is sacrificed for a wider bandwidth of operation. Increasing the size of the inertial mass can partially

compensate for the power reduction. If the design isn't size constrained this is a simple approach to broaden the bandwidth.

Second approach is to design the harvester as an array of narrow bandwidth harvesters that have their individual resonant frequencies in close proximity. In this way the bandwidth of the device will be the sum of bandwidths of individual harvesters. The response of such a harvester and individual elements of the harvester are shown in Fig. 3.25.

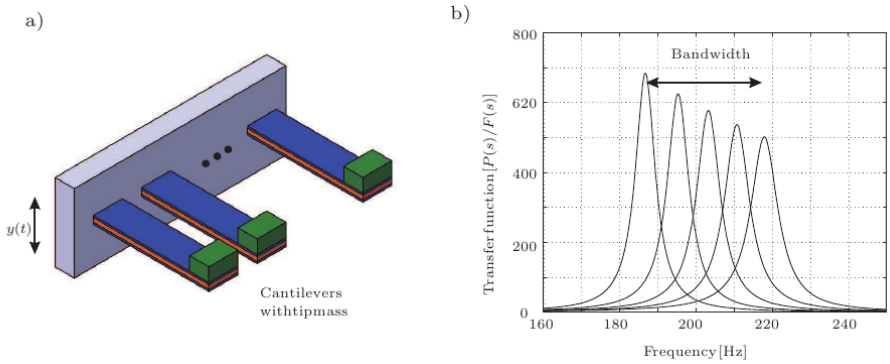


Fig. 3.25 Schematic view of the generator array (a) and transfer function of single generators [158]

This approach can be used to great extent in the micromachined energy harvesters where it is easy to produce a large number of different sized cantilevers. The biggest drawback of such approach is increased size of the system and a need for a potentially large number of cantilevers in order to meet the required bandwidth.

Another possible approach to broaden the frequency is to use a nonlinear structure. The bandwidth of these systems depends on the damping ratio, the nonlinearity and the acceleration [150]. In the nonlinear systems the output power and bandwidth depend on the approaching direction of the vibrating frequency to the resonant frequency. There are two types of nonlinearity: hard nonlinearity and soft nonlinearity. In the case of the hard nonlinearity an improvement of bandwidth can be observed only when the oscillation frequency is rising to the resonant frequency, the opposite is true for the soft nonlinearities. This is shown in Fig. 3.26

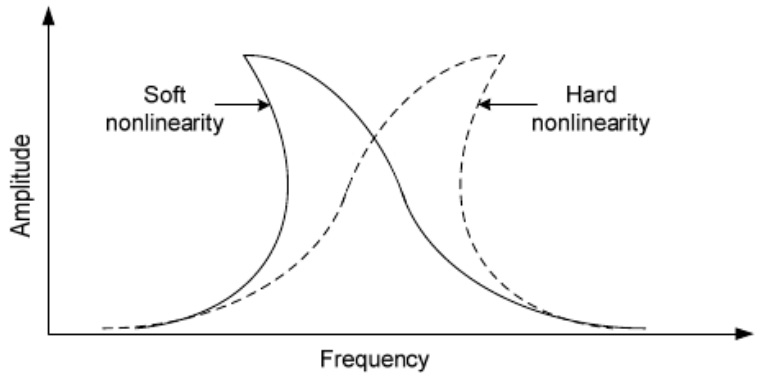


Fig. 3.26 Soft and hard nonlinearities [150]

The use of a magnetic spring in an energy harvesting system leads to nonlinear behavior of a vibrational energy harvester. Here the nonlinearity is achieved by magnetic reluctance forces [34, 29].

Use of the bi-stable harvesters is another option for broadening the frequency response. These structures have two stable positions where, upon being excited, the harvester switches state from one stable position to the other. The energy is being harvested with every change of the state. Analysis done in [114] concluded on the bi-stable devices having a power output higher than the linear oscillators in the broadband range of operation. However, in the case where the energy is converted from a single frequency excitation, the harvesters based on a linear oscillation approaches are more efficient. As a conclusion, the bi-stable structures can't be universally used.

An example of a self-tuning energy harvester that is not using any of previously mentioned approaches is presented in [58]. Authors of this work have demonstrated a method to extend the bandwidth of a rotating harvester using the centrifugal force. In this approach the change of the centrifugal force is changing the length of the element that is used to excite the cantilever hence extending the bandwidth of the harvester.

11. Power Management for Energy Harvesting Circuits

The power management stage has the objective to interface the output of the energy harvesting generator with the rest of the circuit while maximizing the amount of extracted energy from the generator. The power management stage can have one or more of the following tasks:

- Rectification of the output of the energy harvester generator

- Providing optimal load to the output of the generator – matching the impedance of the generator with the input impedance of the power management, thus maximizing the power transfer
- Providing voltage required by the storage and the rest of the electronics that are powered by the harvester
- Maintaining the generator at the optimal operating point ensuring optimal use of the energy source

Each of these points is going to be addressed in more detail in the following subsections.

11.1. Rectification

Several different types of energy harvesters are producing alternating current on their output. These harvesters belong to the family of piezoelectric, electromagnetic and electret-based electrostatic harvesters. In order to provide power to the rest of the electronic, which require typically DC voltage to operate, it is necessary to rectify the output of the generator.

11.2. Passive Rectifiers

The simplest approach to rectification is to use passive rectifiers. The most popular rectifier is the standard diode bridge which consists of four diodes as shown in Fig. 3.27.

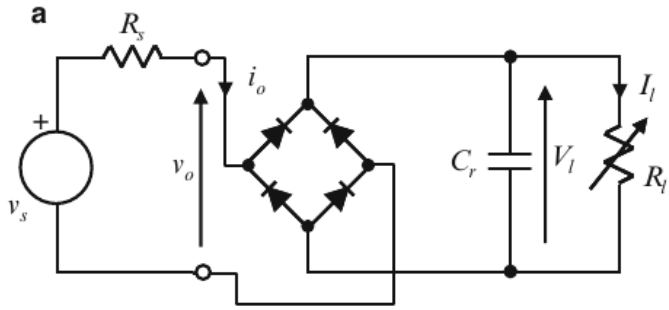


Fig. 3.27 Standard diode bridge rectifier [16]

However this method of rectification has a major drawback that it introduces a voltage drop between the input and the output equal to two diode voltage drops. This typically isn't a problem in the case of high voltage sources, such as piezoelectric generators. In these cases the ratio of input voltage to diode voltage drop is high hence the losses on the bridge can be often ignored. However, in cases where the generator output voltage levels are in the order of several volts, the power loss on the diode bridge can't be ignored. In those cases instead of diodes, MOSFET transistors can be used. In

this way the energy loss is limited to the loss in the MOSFETs and the threshold voltage of the MOSFET. Typical topologies of the MOSFET based bridges are shown in Fig. 3.28.

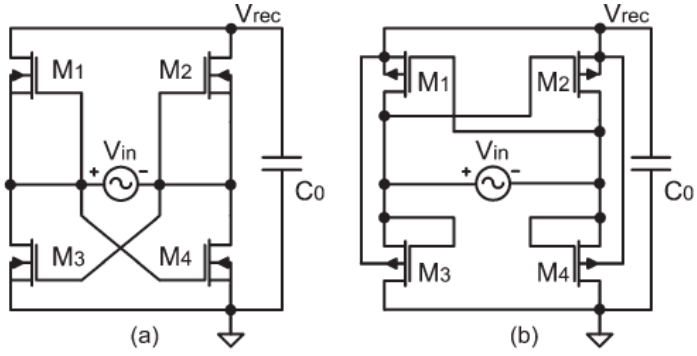


Fig. 3.28 (a) NMOS (b) PMOS full-wave rectifiers

Introduction of the near zero volt threshold (EPAD) transistors by Advanced Linear Devices [40] allowed for the construction of an almost ideal rectifier due to MOSFET threshold voltages close to 0V. However, these devices have high channel resistance (around 25Ω) hence limiting their use only to low power applications where the internal resistance of the generator is much higher than the resistance of the MOSFET's channel.

Another possibility is to utilize the fact that in some energy harvesting applications (mainly RF harvesting applications) the input signal has high frequency. This can be used in conjunction with inductors to overcome the shortcomings of a standard MOSFET bridge. In [94] a MOSFET based LC oscillator structure has been presented as an improved rectifier circuit.

11.3. Active Rectifiers

In applications where it is critical to reduce the power loss of the rectifier section an active rectifier can be used. These rectifiers are typically based on the MOSFET transistors that are driven by a comparator. The comparators are implemented in a way that they sense when the voltage on the input of the bridge is higher than the voltage on the output and then activate the MOSFET. An example of such rectifier is demonstrated in [151].

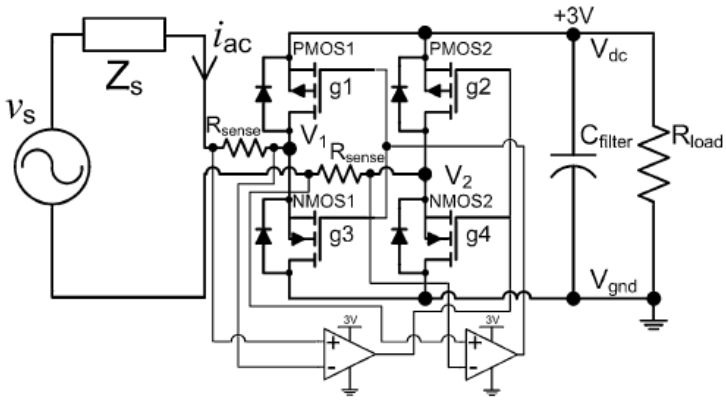


Fig. 3.29 Active rectifier example from [151]

Presented rectifier achieved an improvement of 40%-20% over a passive diode bridge for input power levels in the range of 10-100mW.

Active rectifiers are often used in the field of RF harvesting in order to minimize the losses and for rectification of low voltage signals [18].

11.4. Direct AC-DC Converters

In the kinetic harvesting by adapting the reactive load on the output of the generator it was possible to adjust the resonant frequency of the system. For these applications AC-DC converters are can be used [47]. These converters have an advantage that they don't require a separate rectification stage and they provide a DC voltage on their outputs. Furthermore, they can set the output voltage level, thus adapting it for the use by the rest of the circuit. Typical topologies of AC-DC converters are summarized in Fig. 3.30 [47].

The reported efficiency of AC-DC circuitry found in literature is in the 40 % - 61% range [43, 47].

11.5. Voltage Multipliers

The electromagnetic harvesters typically have the voltage levels that are under the minimum operating voltage level of the electronics that they need to power. Therefore, it is necessary to increase the output voltage of the harvester. As the voltage output of the electromagnetic harvester is AC the increase can be done using a voltage doubler or Villard multiplier and the Dickson multiplier. The number of stages in the multipliers is going to be dependent on the required voltage amplification.

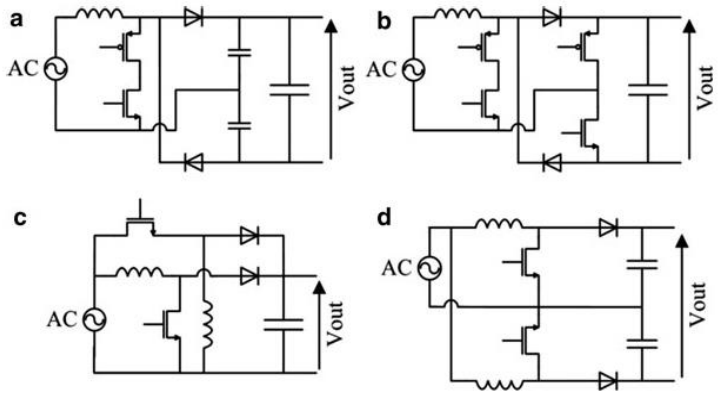


Fig. 3.30 AC-DC converter topologies: (a) single inductor with split capacitor (b) single inductor with secondary side switch (c) combined boost-buck-boost and (d) dual-boost converter [47]

The advantage of using a voltage doubler instead of a diode bridge is the fact that during one half-cycle of the input AC signal, only one diode is conducting hence reducing the overall losses in the rectification stage. An advantage of using a cascade voltage multiplier is no need for switching converters and additional electronic circuitry. However, implementation of voltage multipliers prevents implementation of an impedance matching circuit hence reduces the possibility for further power optimizations [16].

11.6. Advanced Rectification Techniques for Piezoelectric Generators

In order to be able to explain the more advanced rectification techniques it is necessary to first introduce the electrical model of the piezoelectric generator. After the model is being introduced a family of advanced rectification topologies will be explained that increases the potential power output of the piezo element for an order of magnitude or mode compared to the output obtained using the standard diode bridge rectifier.

11.6.1. Modeling of the Piezoelectric Generator

A model of a piezoelectric generator has been developed that is based on a second-order lumped model circuit with structural and piezoelectric coupling parameters included. The model was introduced in [83]. The schematic of the model is shown in Fig. 3.31. The lumped parameters M_{11}, K_{11} and D_{11} are the effective mass, the stiffness and the parasitic damping of the energy harvester. The voltage source output is the function of the mass and acceleration. The transformer turns ratio n is related to the piezoelectric coupling. C_P is the

clamped capacitance of the piezoelectric generator. An important effect of this capacitance is to limit the maximum damping that can be achieved regardless of the external load resistance applied. This implies that the harvesting system is always under damped.

Due to the typically poor coupling between the mechanical and electrical domain of the piezoelectric generator, at resonance the mechanical motion is influenced almost entirely by the mechanical parasitic damping on the primary side of the transformer. This leads to the conclusion that the electrical damping of the system is being neglectable from the mechanical side's point of view. This in turn allows use of a simplified model for the piezoelectric generator. In this model the generator is modeled by a current source, that has the same frequency as the mechanical vibration and the magnitude is set by the properties of the piezoelectric material. A shunt capacitance is used to model the parasitic damping.

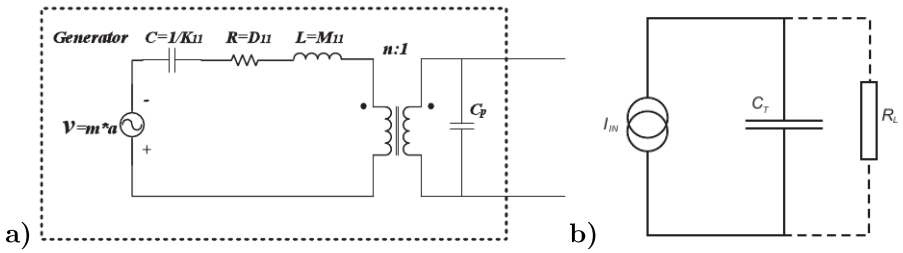


Fig. 3.31. a) Second order circuit model of a piezoelectric generator [83] b) simplified model of a piezoelectric generator [16]

11.6.2. Synchronous Switch Harvesting on an Inductor

The existence of the shunt capacitance in conjunction with the fact that the electrical and mechanical domains are poorly coupled results in the load resistance not being able to influence the motion of the harvester. As a result a power loss can be identified at the end-stops of the harvester. In order to increase the output power of the piezoelectric generator two steps can be taken [16]:

1. Pre-biasing the piezoelectric material before mechanical work is done against it;
2. Synchronously extracting the charge from the piezoelectric element instead of continuous extracting into a linear resistive circuit.

When a piezoelectric element is strained in one direction, using external force, while not connected to a load, the generated charge causes a force that tries to move the material back to the rest state. If a charge is placed onto the element before the force is being applied (pre-biasing the piezoelectric element) more work needs to be placed into moving the element as the pre-charge will oppose the applied force. In this way more mechanical power is used hence

more electric power is generated. First research group to apply this technique on a low power energy-harvesting domain was led by Guyomar [60]. This technique of charge extraction was named synchronous switch harvesting on inductor (SSHI). The circuit schematic is shown in Fig. 3.32.

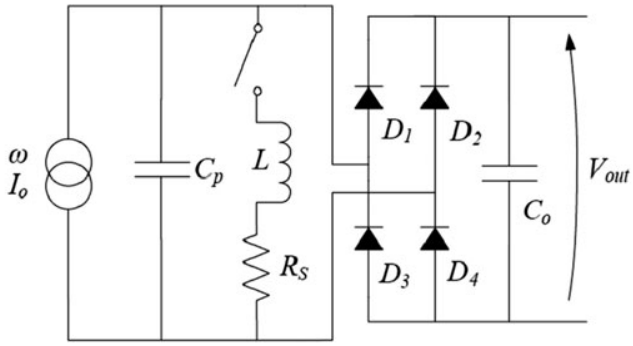


Fig. 3.32 Original SSHI circuit with DC output [60]

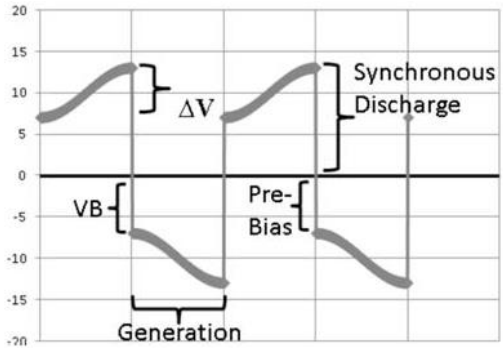


Fig. 3.33 Piezoelectric voltage when operated with the pre-bias and the synchronous discharge [16].

The SSHI operation can be best explained on one operation cycle of the circuit. The analysis will start with the piezoelectric element at the maximum displacement point. At this stage the mechanical force changes direction. In order to achieve maximum utilization of the external force it is necessary to charge the piezoelectric element with the voltage of opposite sign of what is currently measured over the piezo element. In order to do so, the inductor is closed, which forces a current flow through the circuit effectively reversing the voltage on the internal capacitance of the piezo element. In this way the charges have been removed (synchronous discharge in Fig. 3.33) and the piezoelectric element has been pre-biased. As the mechanical force is being applied now the absolute voltage of the piezo element will continue to increase, until the maximum displacement is reached once again, leading to repetition of the process. In this way the output voltage on the piezoelectric element is

much higher than in the case of the diode bridge, hence increasing the energy output.

The review of the literature done in [49] suggests that the power output of the piezoelectric generator can be increased 250% to 900% compared to approach using only a diode bridge. Therefore, this technique has gained a lot of attention and various circuits have been based on this approach.

The newest addition to the SSHI family of the circuits is a circuit which besides increasing the power output further is aimed at extending the usability of the piezoelectric element [46]. The schematic of the circuit is shown in Fig. 3.34. This circuit represents an improvement over the single supply pre-biasing (SSPB) topology [41]. The theoretical power output of the proposed approach is [46]:

$$P_{SSPB_{FRTZ}} = 2fC_pV_{po}^2\frac{(1+\gamma)}{(1-\gamma)} \tag{3.19}$$

where Cp is the shunt resistance of the piezoelectric element, Vpo is the voltage induced on the piezo element and γ is a tangent loss coefficeint in the rage of 0 to 1, where 0 is the maximum loss and 1 is the lossless system. At the beginning of the lifetime the circuit will perfomr in the same way as SSPB, which will provide a gain in extraceted power of $8Q/\pi$ compared to the maximum power that could be extracted using a standard diode bridge rectifier, and a factor of two greater than the original SSHI technique. As the piezo element deteriorates, the proposed circuit would outperform the original SSPB because of its forced return to zero approach, that makes certain that the piezo element is discharged before applying pre-bias to it.

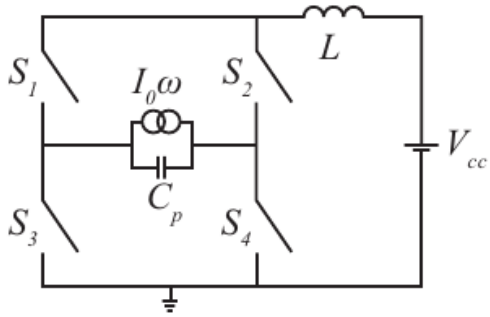


Fig. 3.34 Forced Return to Zero SSPB circuit Topology [46]

It should be noted that the proposed circuits, although they increase the power output of the piezoelectric harvester, they don't address the issue of optimal load matching. This has been addressed in [54]. In this circuit a magnetic rectifier has been used, therefore, eliminating the need for load

matching as the load circuit is completely insulated from the piezo element. The schematic of this circuit is shown in Fig. 3.35.

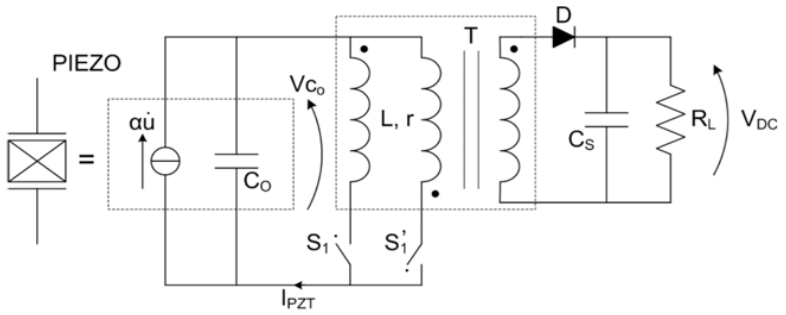


Fig. 3.35 Synchronized switch harvesting on inductor (SSHI) with magnetic rectifier circuit [54]

The circuits provide an optimal operation of the piezo element by ensuring the proper pre-biasing and removing of any influence of the load to the piezo element. In this way an increase of 56 times in the power output of the piezoelectric element has been reported by the authors of the circuit.

12. Maximum Power Point Operation and Tracking

In order to maximize the available power output the energy harvester the harvester should be operated at the maximum power point. At the maximum power point the input impedance of the power management circuit is matched to the output impedance of the generator, thus providing the maximum power transfer. The circuits used for emulating the impedance are switched based converters. These converters can be capacitor or inductor based. The emulation of the impedance is realized by altering the operating condition of the converter.

There are three common approaches to emulating resistance. The first is by altering the duty cycle of operation of the converter [83, 151]. The second is by altering the switching frequency of the converter [27]. Third is by activating the converter for a brief period of time, using a predefined frequency and duty cycle, around the maximum power point, thus making the input oscillate around the maximum power point [93, 167].

It should be noted that the implementation of impedance matching is consuming power. Therefore, it is necessary to assess if the power gained by implementing the circuitry for impedance matching is larger than the power consumed by the said circuitry.

The fact that the operating condition of the converter can be altered easily leads to a possibility to dynamically adapt the input resistance of the converter. This is useful in the case of environments where the amount of available energy is changing. For example, with the change of the wind speed the power output of a small scale wind turbine will change. This is demonstrated in Fig. 3.36. In order to continue providing optimal load for the generator the input impedance of the power management needs to be dynamically changed. The constant adaptation of the operating point of the converter to meet the maximum power point of the generator is typically referred to as maximum power point tracking.

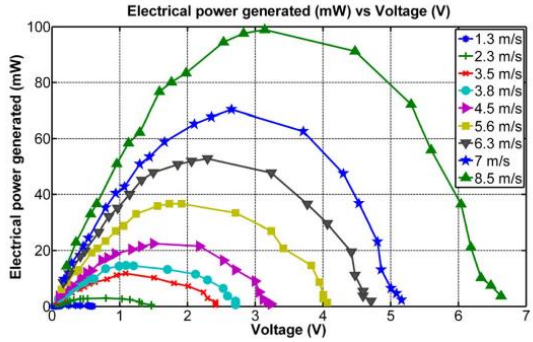


Fig. 3.36 Power harvested by wind turbine generator as a function of voltage at different wind speeds [151]

The maximum power point tracking techniques are widely used in large scale photovoltaic systems in order to optimize the power generation. The reviews of literature done in [113, 130] list 20 different maximum power point tracking algorithms that are typically used in the case of relatively high powered PV cells. However, the majority of those approaches are either too complex, or too power demanding to be implemented in a low power energy harvesting system [37, 62].

By analyzing the literature two maximum power point approaches have been found dominant for low power systems: the open circuit voltage method and the "perturb and observe" (hill climbing) method. These two methods will be described in detail, followed by two additional methods for determining the maximum power point.

12.1. Open Circuit Voltage MPP Method

The open circuit voltage method is based on the observation that the maximum power point can be determined as a function of the open circuit voltage [9]:

$$V_{MPP} = k \cdot V_{OC} \tag{3.20}$$

where V_{MPP} is the maximum power point voltage, V_{OC} is the open circuit voltage and k is the factor of proportionality that typically falls in the range between 0.7 and 0.8 for solar cells. The exact value of the factor depends on the photovoltaic used and should be determined experimentally. For other types of generators k is typically at 0.5 [62]. Therefore, the operation principle of this maximum power point tracking algorithm is to disconnect the generator for a brief period of time, asses the open circuit voltage, followed by setting the operating point of the converter based on the obtained results. A low power implementation of this approach can be found in [167].

The major drawback of open circuit voltage approach is the need to disconnect the generator from the power converter during maximum power point assessment. This leads to the energy loss. Furthermore, this method requires experimental determination of the factor k which can be impractical in the case of large volumes of energy transducers.

12.2. Perturb and Observe MPP Method

The issue of the power loss due to frequent connecting and disconnecting of the generator and the converter is addressed in the second most common used technique for maximum power point tracing, the "Perturb and Observe" (P&O) method [130]. This is an iterative method based on varying the input power of the converter and observing the change. At the maximum power point the variation of the power with the change of the voltage should be 0.

The operating voltage point of the PV generator is perturbed for a small increment of ΔP_{PV} and the change in the output power of the panel is measured. If the power change is positive the next perturbation of the voltage should have the same direction. On the other hand, if the change of the output power is negative, this would mean that the voltage is moving away from the maximum power point and that the perturbation should change direction. Examples of low power implementations of the P&O method can be found in [82, 37, 27].

The drawbacks of this approach are the delay until the maximum power point is reached which is dictated by the size of the perturbations, the complexity of the algorithm used for determining the change of the power and the requirement for continuous measurement of the input power.

12.3. Other MPPT Methods

Several other approaches to maximum power point tracking have been reported in literature as well. One of the popular approaches for maximum

power point tracking for solar cells is using a "pilot" cell to assess the light intensity level and based on that, provide a control signal for the switching converter [16].

Work done in [93] is determining the maximum power point by evaluating the average power used to charge the capacitor placed on the input of the power management stage. This method is based on the fact that when the operating point V_m is under the MPP voltage, the average power measured during the charging of the capacitor from a voltage level V_m-ΔV_H to V_m is going to be smaller than the average power in the voltage region V_m+ΔV_H. In the case where the operating point is beyond the maximum power point the average powers in these two sections will have a different relationship. This is demonstrated shown in Fig. 3.37.

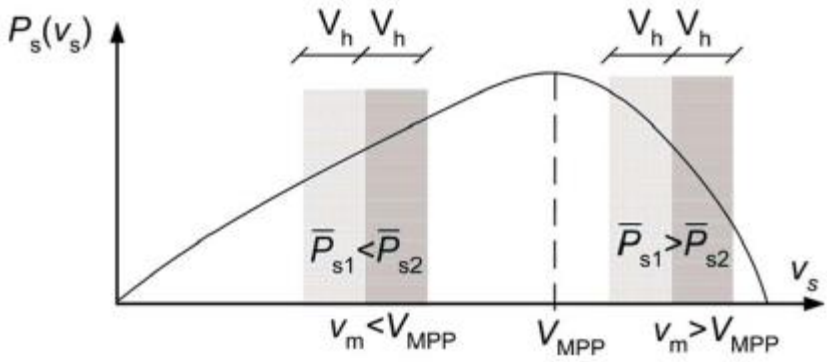


Fig. 3.37 Evaluation of the operating point (Vm) with respect to the MPP (V_{MPP}) [93]

It should be noted that in some cases it is possible to design a system to cope with the change of the energy levels in the environment without employing any additional electronic circuits. This will be discussed in more detail in Chapter 5.

13. Conclusions

This chapter was aimed at introducing the basic principles of operation of energy harvesting transducers. The main focus was on the photovoltaics and the kinetic energy harvesting.

The photovoltaics have been addressed first. Their structure has been examined as well as their properties. A basic single diode model of a solar cell has been presented as well. An accent has been placed on optimal use of the solar cells with stress on the selection of proper solar cell depending on the light source it will be harvesting.

The kinetic energy harvesting was examined in detail with accent on piezoelectric, electromagnetic and electrostatic transducers. Each transducer

type was examined in detail with discussions on optimal transducer use. An accent had been made on overcoming the typical problem of narrow bandwidth of linear vibration harvesters.

After introducing the energy harvesting transducers the circuits that are used as interfaces between the energy harvester and the rest of the circuits have been examined. The issues of optimal power transfer, rectification and increasing of the power output of different types of harvesters have been addressed.

It can be concluded that the recent advancements in materials and in low power circuit design and implementation are definitely providing the means for powering the low power electronics from the environmental power sources.

Chapter 4

Ultra-Low Power Energy Management

1. Introduction

In a typical energy harvesting powered wireless sensor network (EH-WSN) node application, the power source is not capable of delivering sufficient power to run all the node elements at full power. Therefore, the energy harvesting system can be divided into two segments: the first, that is always powered, which controls the collection of the energy and harvester's operation and the second, that is active only when sufficient energy has been collected in the buffer storage. The second part is typically in charge of performing measurements and transmitting the data wirelessly. Depending on the system realization these segments can include different elements of the system.

Typically the energy management and power management sections are active throughout the system operation as they are managing the power source and the energy buffer storage. Therefore, in order to collect the energy for

running the application task, the harvester has to provide more power than it is required by the sections that are always running.

The discussions done in the previous chapters showed that the power management's task is to provide optimal energy extraction. However, in case of the ultra-low power sources, aimed at nanowatt and microwatt harvesting, the energy consumption of an advanced power management stage can be greater than the potential gain in the power output. By adapting the harvester, it is sometimes possible to have a harvester that will operate in the optimal range without a power conditioning circuit, hence increasing the efficiency of the overall system. This will be demonstrated in the first case study in Chapter 5.

The energy management stage, in contrast to the power management, stage typically cannot be removed from the EH-WSN node. The monitoring of the storage has to be implemented in some way; otherwise, the unpowered part of the system would never be activated. Therefore, it can be stated that the minimal required power generated by the harvester needs to meet the power consumption of the energy management stage. By minimizing the energy management's power consumption it would be possible to power the wireless sensor nodes from power sources that were previously deemed unfit to power the application.

This chapter is aimed at energy management circuits designed to operate with generated power levels in the nanowatt and microwatt range. This amount of energy can sometimes be perceived as too small to be useful.

Experiments done during the course of the writing of the thesis have shown that the energy requirement for performing an operation consisting of starting up the node, performing an ADC conversion that resulted in reading of the ambient temperature and sending the measured value using a wireless link, can be as low as 10µJ even on 1 dBm radio output power setting. In such a case, a 1µW power source could potentially provide sufficient power to perform one wireless transmission every 10s, or once every minute and a half using a 100nW source. This might seem like a long period between two transmissions for some applications, however, there are applications that don't require fast sampling. For example, indoor air quality monitoring and structural monitoring such as: strain monitoring of beams in a building, bridge monitoring, stress monitoring, fatigue monitoring. Further examples include various indoor or outdoor temperature monitoring tasks and other environment monitoring tasks that are tied to slow changing physical phenomena.

The harvester will provide nanowatt or microwatt output power levels under three scenarios. The first scenario covers the cases where the harvester is placed in an environment with a small amount of available energy to convert from. One example are solar cells exposed to $<$20 lux light sources. These power levels can be expected in hallways, rooms in residential buildings, rooms with dimmed light sources, etc.

The second scenario covers harvesters that by design generate an output in the nanowatt and microwatt range. For example, MEMS scale harvesters [88] or an array of solar cells that have the surface area of several square millimeters [3]. One more example of microwatt power generators are harvesters based on electric field harvesting [23].

The third scenario is covering the harvesters operating outside their optimal conditions or using low efficiency harvesters in order to reduce the complexity or the cost of the system.

Typically, the power management for ultra-low power applications in literature is almost exclusively done by applications specific integrated circuits (ASIC) [14, 139, 27]. The possibility to closely control the leakage currents and precisely trim the operation of analogue components makes ASICs well suited for such a task. However, this technology is limited only to research groups that have access to ASIC manufacturing. ASICs are also expensive to produce and their design and manufacturing can take a significant amount of time.

Additional challenge for the energy management stage is applications where a capacitor is used as storage instead of a battery. In these applications the energy management has to provide stable operation when the charging begins with the buffer capacitor empty. Also, it is a well-known fact that the majority of off the shelf integrated circuits are not performing inside their specification for voltages under the minimum operating voltage.

The aim of this chapter is to demonstrate two approaches to implementing an energy management stage aimed at applications that utilize capacitors as buffer storage. These circuits are aimed at power sources in the range of nanowatts to microwatts, hence providing an alternative to using ASICs in developing ultra-low power energy harvesting applications.

The rest of the chapter is structured as follows: first, state-of-the-art in off-the-shelf component based energy management circuits are presented, which operate in nanowatt range. Following is a section on ultra-low power voltage monitoring where a "Nanowatt Voltage Detector" (NVD) is designed and implemented. After this, a section on microcontroller based power management is presented referred to as the "ADC energy management" In the end the conclusions are presented.

2. State of the Art in Nanowatt and Microwatt Energy Management

Ideally, the power consumption of the energy management stage should be 0 A, however, this is currently not feasible. Until a technology capable of 0A voltage monitoring is available, the total power consumption of the energy management stage should account to as small part of the harvested power as possible.

The simplest control of activating a load when a voltage threshold has been reached can be achieved using a window comparator. These circuits are well known and are based on two operational amplifiers in combination with a voltage reference. At the time of writing of the thesis, the lowest power comparator with integrated reference was LTC1540 from Linear Technology [153]. The power consumption of this device was typically 840 nW with the reference active at 3 V. This would potentially consume all of the generated power in case of a 1 µW power source. At the time of writing of the thesis, an operational amplifier was marketed with 100 nA typical power consumption NPS1101 by nanowatt power solutions [67]. However, it was not commercially available and it requires an additional external voltage reference to operate, increasing the overall power consumption of such approach.

The literature review has yielded a small number of energy management circuits designed for operation with power consumption in nanowatt range [23, 138, 107]. One of the most commonly used circuits is shown in Fig. 4.1.

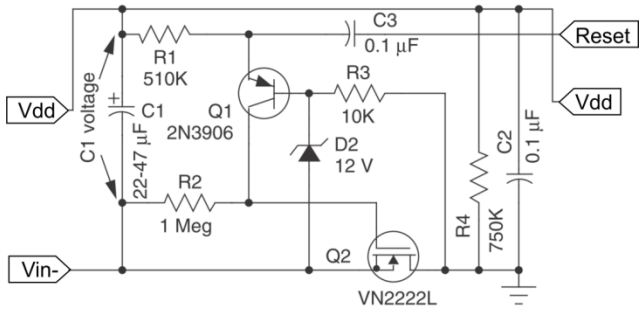


Fig. 4.1 The most commonly used circuit for high impedance power sources [23, 138]

In the circuit shown in Fig. 4.1, a Zener diode is used as a voltage reference in combination with bipolar transistors. The circuit operates as follows: once the voltage on the buffer capacitor, marked C_1, reaches the threshold voltage of the Zener diode, the diode conducts allowing the attached bipolar transistor to conduct. This in turn latches up the Q2 transistor allowing the connection of load to the negative terminal of the buffer capacitor, hence allowing the flow of charge. When the energy is used for the application specified task, by applying low voltage level on the RESET signal, the Q2 would stop conducting, hence deactivating the load. The input capacitor is now being recharged by the power source and the process repeats itself. The input impedance of this circuit is reported to be in order of $10^7\ \Omega$ [138].

This circuit has a limitation in that the threshold voltages are limited to available Zener diode threshold voltages. However, not all Zener diodes can be used. The circuits implemented had a threshold voltage of 12 V. This was

chosen because the Zener diodes with threshold voltages above 10V have near ideal transition from non-conductive to conductive stage [2]. On the other hand, if the voltage output of the harvester was in the range of 2 V to 3.6 V, low voltage Zener diodes couldn't be used with the same efficiency. Low threshold voltage Zener diodes have higher reverse currents, hence increasing the static power consumption of the monitoring circuit.

The second circuit found in the literature is called "Novotill circuit" [107] and it removes the limitation of the Zener diode by using a LED instead. This circuit was simulated using SPICE simulator LTSpiceIV and the results have shown a current requirement of 32 nA in order to perform the voltage monitoring successfully. However, the drawback of the "Novotill circuit" was its high current consumption once the threshold was reached. Simulations have shown a consumption reaching 55 mA on 3.6 V while the load was connected to the buffer storage. This current consumption is exceeding the current consumption of a radio operating at full power. Such high current consumption reduces the possible applications of this circuit only to applications where the load would be active for a very brief period of time, thus preventing the energy management circuit from consuming most of the collected energy. However, in scenarios where sensors require long times to activate and where is a need for processing the signal, this circuit would introduce major energy losses.

3. The Nanowatt Voltage Detector

The "Novotill" circuit has a great potential for being used for harvesting from nanowatt power outputs as it has very high input impedance. However, it was necessary to overcome the issue of the increased current consumption once the circuit is active. The following section will address this challenge and will also aim at further reduction of the current consumption of the circuit before it activates. The improved circuit is then used as a building block for the circuit that will be referred to as the Nanowatt Voltage Detector (NVD).

The NVD was aimed at having lower input impedance of the state of the art circuits and having a lower current consumption while the load is powered from the buffer capacitor.

3.1. Theory of Operation

The full circuit schematic is presented in Fig. 4.2.

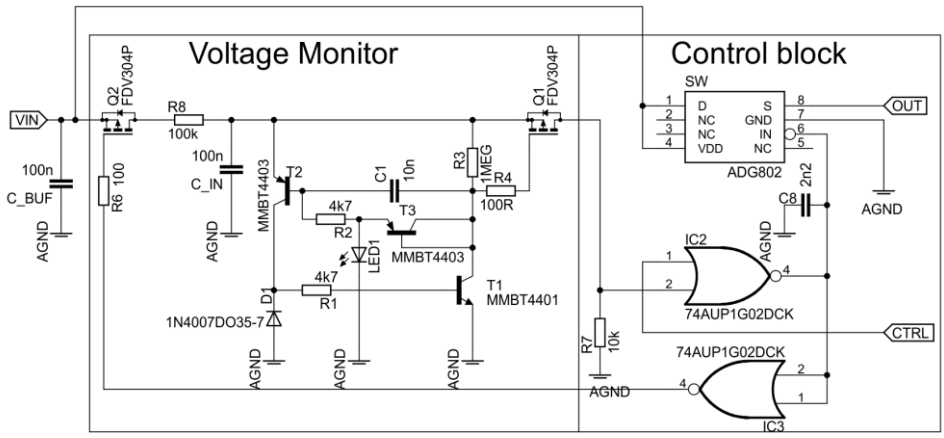


Fig. 4.2 Schematic of the proposed nanowatt voltage detector

The circuit is aimed at being connected directly to the input buffer capacitor that is accumulating the energy collected by the harvester. The circuit consists of two main parts: the voltage monitoring stage and the control block.

The main function of the voltage monitoring stage is to signal the control block once the threshold voltage of the buffer capacitor has been reached. The adapted circuit from [107] is used as the main building block of the voltage monitoring stage. The changes done to the circuit presented in [107] are the following: in the original circuit the Q1 was a bipolar transistor, here a MOSFET is used in order to reduce the power consumption during operation. Furthermore the resistor values in the circuit were modified in order to reduce the power consumption. The resistor values have been selected experimentally.

The control block is used to activate the switch connecting the load and the input buffer capacitor once a signal from the voltage monitoring stage is received. Furthermore, it is used to disable the voltage monitoring stage in order to reduce the power consumption while the load is connected to the input buffer capacitor. This also provides a way to disconnect the load from the buffer capacitor when needed. The last function of the control block is reactivation of the voltage monitoring once the load is disconnected, allowing the voltage monitor to observe the buffer capacitor voltage again.

The circuit operation is depicted using block diagrams in Fig. 4.3.

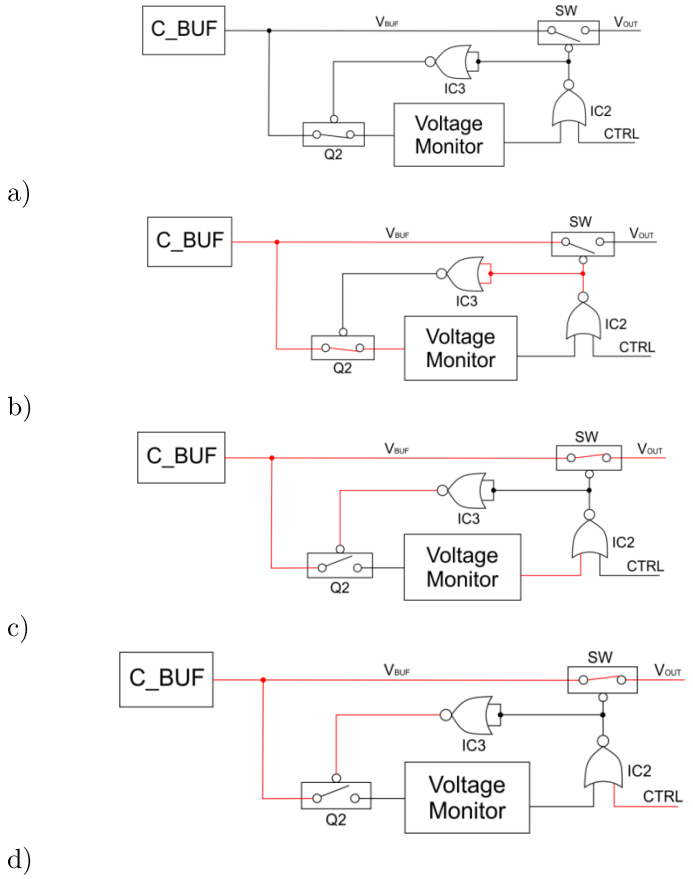


Fig. 4.3 The operation sequence of the Nanowatt Voltage Detector – a) initial state; b) buffer capacitor charging; c) the voltage monitor threshold is reached; d) The voltage monitor is disconnected while the control of the SW is done via external circuit. Red lines indicate V_{BUF} voltage level while black lines indicate ground potential

At the beginning of the operation, all signals in the NVD are on 0V. When the power becomes available, from the energy harvester's output, it starts charging the C_BUF. Once the threshold voltage of the Q2 is reached it activates, and the Voltage Monitor block starts monitoring the voltage level on the C_BUF.

During this phase, the IC2 and IC3 circuits are operating under the minimum specified operating conditions. Therefore, special care needs to be taken when choosing them. This is explained in more detail in the implementation section.

When the threshold voltage of the voltage monitoring stage is reached its output would change, activating the NOR circuit IC2. The change in signal on the output of the IC2 will change the output of the IC3 leading to disabling of

the Q2 transistor. This will disconnect the voltage monitor from the C_BUF, preventing further energy loss by the voltage monitoring circuit. This is necessary due to high current consumption of this circuit once the threshold voltage of the voltage detector is reached as explained earlier. During the time the voltage monitor block discharges its internal capacitances, the voltage on the CTRL line should reach the V_{BUF} voltage level using external circuitry that is connected to V_{OUT}. In this way, when the capacitances inside the voltage monitoring block get depleted, the output of the IC2 NOR is going to be controller by the CTRL line, allowing the load to control for how long it will stay connected to the input capacitor.

During the operation of the load it can be said that the Nanowatt Voltage Detector circuit is in "by-pass" mode where it has minimum power consumption as the only elements active are the logic gates.

When the circuitry powered from V_{OUT} needs to be disconnected from the C_BUF, in order to allow the buffer capacitor to recharge, the CTRL line is connected to the ground potential, which results in the IC2 output changing to the low voltage level. This leads to SW opening, hence disconnecting the C_BUF from V_{OUT}. At the same time, via IC3, the Q2 is re-enabled allowing the voltage monitor to start monitoring the C_BUF again and the activation cycle repeats once the threshold voltage is reached again.

The detailed explanation of the all the signals inside the circuit and the detailed explanation of the behavior of the circuit is presented in Appendix A.

The next section will focus on the implementation of the circuit and give details on the design choices made during the circuit implementation.

3.2. Analysis and Implementation

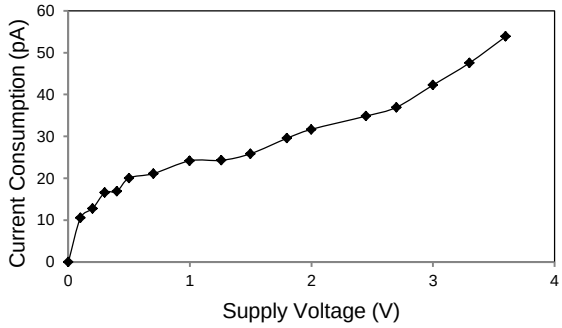
The circuit operation can be divided into four characteristic operating stages. The stages are divided based on the buffer capacitor voltage and state of the switch SW. The voltages used in defining the stages are V_{BUF} – the voltage on the buffer capacitor and V_{THR} – threshold voltage of the voltage monitor. Based on these voltages the stages are:

- Low voltage stage ($V_{BUF} < 0.5$ V)
- Triggering stage ($V_{BUF} >= V_{THR}$)
- Load active stage
- Disconnecting stage

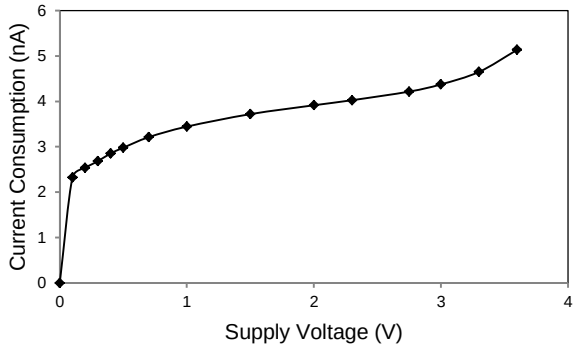
3.2.1. Low Voltage Stage $V_{BUF} < 0.5$ V:

This can be considered the most critical stage of the circuit operation, as the components are operating under the specified low voltage limit. As can be seen from the schematic, the components that were being powered directly

from the buffer capacitor continuously are: SW (ADG802 [1]), IC2 and IC3 (74AUP1G02 [156]). IC2 and IC3 are specified for operation from 0.8V while SW was specified to operate from 1.8V. Therefore, individual profiling of these components was necessary in order to determine their power consumption for supply voltages under the voltage specified from their datasheets. The current consumption of evaluated circuits is presented in Fig. 4.4 .



a)



b)

Fig. 4.4 Current consumption of critical circuits under the entire expected operating voltage range; a) ADG802 analogue switch, b) 74AUP1G02 NOR logic gate

The current consumption of the NOR gate is higher compared to the ADG802. Investigation has shown that lower power consumption can be expected from the AUC series of integrated circuits as shown in Fig. 4.5. However, the AUC circuits are designed for operation from 0.8 V to 2.7 V, hence they should be used only in applications where the buffer capacitor is not going to be charged above this limit.

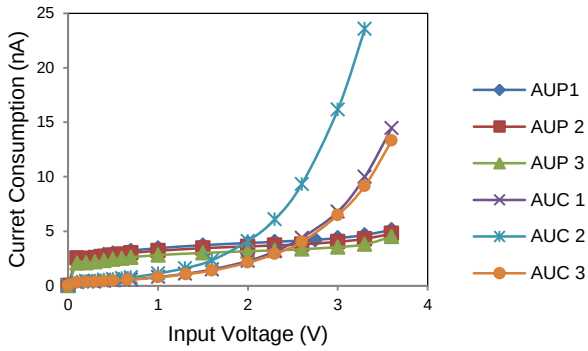


Fig. 4.5 A comparison between logic gate AUC and AUP series current consumption. Three units of each type have been characterized. It can be seen that AUP series of gates demonstrated smaller differences between units tested. It should also be noted that the AUC series is rated only to 2.7 V

It was experimentally determined that NOR gates in the LVC and HC logic families exhibit even lower current consumption compared to AUC and AUP series, however, it was necessary for the NOR gate to start operating as soon as possible, and these series have a higher minimal operating voltage. The need for stating at a low voltage is necessary for the following reason. The output of the IC2 NOR gate is connected to the gate of the ADG802 (SW) while the CTRL pin is connected to external circuitry. During the low voltage stage, the output of the NOR gate is disconnected as the output driver inside the integrated circuit can't provide a conducting path to either ground or supply due to the low voltage condition. Therefore, the output of the NOR gate can't be immediately established to high level as is expected when both of its inputs are being on a ground voltage level. During this period the NOR gate has undefined output and the voltage level on the signal line will be defined by the parasitic elements of the output of the NOT gate. This, in turn, means that undefined voltage might appear on the gate of SW. The SW has to be chosen in such a way that until the NOR starts operating, there is minimal leakage from the input buffer capacitor to the V_{OUT} regardless of the voltage on the input.

The critical amount of leakage is defined by the impedance connected to the V_{OUT}. If the impedance of the load is in order of gigaohms, even a leakage current in order of parts of nanoampere could potentially provide sufficient voltage drop of several hundreds of millivolts. This voltage drop could possibly lead to CTRL line reaching the voltage IC2 would interpret as a high logic level, thus activating the SW before the buffer voltage has reached the threshold.

It has been experimentally verified that both the AUP and AUC series of logic gates will provide a stable output at 0.3 V supply voltage when their

output is driving a high impedance load. If the NOR gate is stable at 0.3 V that means the switch should be kept disabled in case of voltage difference of 0.3 V between the gate and the supply voltage. It should be noted here that use of a resistor, that would connect the gate and the source of the circuit, which is commonly used in these situations, isn't an option as the current loss it would introduce would be too large. For example, even a 100MΩ resistor at 2 V drains 20 nA which is significantly higher than other components in the circuit.

The first choice for SW was a transistor. However, transistors exhibit subthreshold leakage currents that are more than sufficient to cause the previously explained preemptive activation. In order to minimize the subthreshold leakage, a transistor with high threshold voltage could be used. On the other hand, the transistor should enter the saturation region at 2 V allowing low loss connection between the input buffer capacitor and the load. The typical heuristic for determining the subthreshold leakage current is to assume a drop of one order of magnitude per 0.1 V under the threshold [127] which is shown in Fig. 4.6. For an IRLML6401 transistor, this current was measured to be 20 nA at 0.3 V and for the transistor FDV304P 10 nA at 0.3 V. These currents were sufficient to cause a change on the output voltage of the NOR gate, thus activating the switch before the buffer capacitor reached the desired voltage level.

After investigation of available analogue switches, the ADG802 series of switches by Analogue Devices [1] has been found to have almost no measurable leakage using the equipment that was on disposal, until the supply voltage reaches 0.5 V. The leakage current as a function of the supply voltage when the gate is held on the ground potential is shown in the Fig. 4.7. It should be noted that the switch used was active low so keeping the gate at low level would make the switch conduct. The goal of this experiment was to determine the minimum voltage difference between the gate and the source that would lead to the switch conducting.

Based on the results of the ADG802 measurements, combined with the fact that the selected NOR gate will provide a stable output at 0.3V, there will be a margin of 0.2 V left before the ADG802 would start conducting. This margin will provide a stable operation of the circuit preventing the load from being powered until the threshold voltage has been reached.

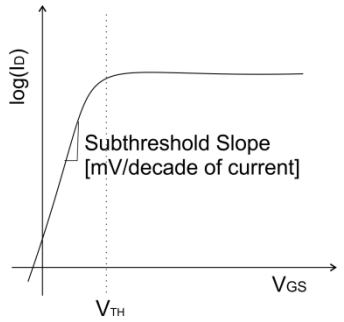


Fig. 4.6 Estimation of the subthreshold current based on the difference between the gate voltage and source voltage

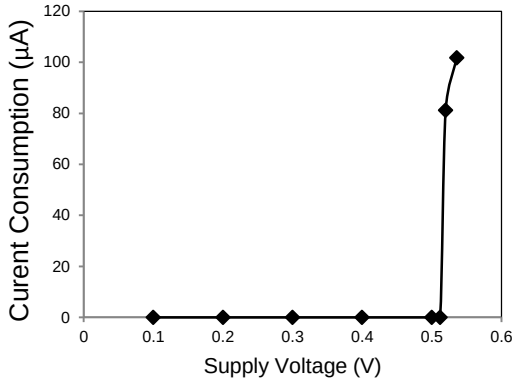


Fig. 4.7 Leakage of ADG802 with gate tied to ground. Up until 0.5 V supply voltage the leakage is neglectable suggesting that the gate driver should have stable output before the supply voltage reaches 0.5 V.

After the supply voltage reaches 0.5 V, all circuits are opening stable until the threshold voltage of the voltage monitoring stage is reached. When the threshold voltage is reached the voltage monitor activates its output leading the circuit into the next stage of operation.

3.2.2. Triggering Stage $V_{BUF} >= V_{THR}$:

When the voltage reaches the forward conduction voltage of the diode used as a reference, the LED starts to conduct. This leads to the activation of the transistor Q1, hence signaling the control stage that the voltage has been reached. The key aspect of the circuit is the behavior of the LED as a reference.

The LEDs are subject to photoelectric effect. Although small, the generated current is sufficient to increase the threshold voltage. The increase of the threshold voltage is coming as a consequence of the forward biasing current

having to overcome the photoelectric generated one. The shift in threshold voltage of the circuit is a function of the photoelectric effect and dependent on the light intensity. In order to avoid the uncertainty of the threshold voltage, the LEDs were shielded thus providing a stable threshold voltage for a given rate of charge of the buffer capacitor.

The rate of charge of the buffer capacitor is also going to have a major impact on the threshold voltage. The voltage detector is going to activate when the transistor Q1 starts conducting. In order for this to occur the voltage on the LED needs to be 0.4 V under the voltage of the transistor's emitter voltage. The voltage on the LED is, on the other hand, defined by the current running through the LED. By analyzing the circuit, the current running through the diode is dependent on the capacitor C_IN value as:

$$I \sim \frac{1}{C\_IN} \frac{dU}{dt} \tag{4.1}$$

From the formula (4.1) it can be seen that the current is going to be dependent on the rate of change of the voltage and the rate of charge of the buffer capacitor. The higher the rate of charge, the higher the voltage across the LED will be. This in turn means a higher threshold voltage. This behavior was experimentally verified.

Setting the threshold voltage is done by selecting an appropriate LED. The previously explained effect of the dynamics of the voltage change has to be taken into account when selecting the threshold. At this point the LED is being selected experimentally. Fig. 4.8 shows different threshold voltages depending on the combination of LEDs used. Test was performed using 47 kΩ input resistance attached to a 5 V power source with 50 μF input buffer capacitance. As a comparison, in the case of a blue LED with 50 nA current source, the threshold voltage was reduced to 1.92 V.

In this circuit, the diode D1 is placed instead of a "pull down" resistor. This isn't a common practice; however, this approach has an advantage over the approach of using a resistor [107]. A diode is a nonlinear element and the current running through it, in reverse polarization, will depend on the voltage across the diode. The diode used is 1N4007 which has a breakdown voltage of 1000 V. The maximum expected change of voltage on the buffer is 3.6 V. This change of voltage has no impact on the reverse current as can be seen from Fig. 4.9 [135]. On the other hand, current flow through the resistor is following the Ohm's law and will vary over the expected voltage range. Using a reverse diode, therefore, provides polarization of the collector of the transistor that is almost unaffected by the applied voltage and is more power efficient compared to resistor use.

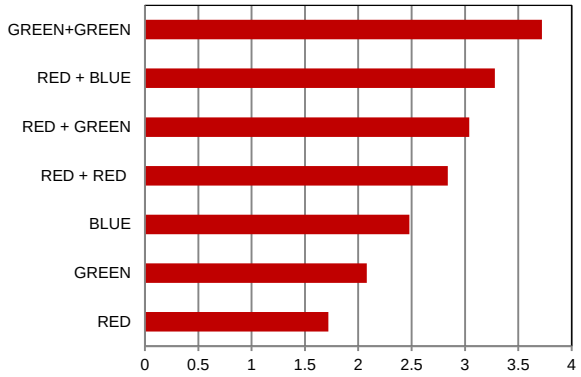


Fig. 4.8 Triggering voltage based on the combinations of LEDs used as the voltage reference

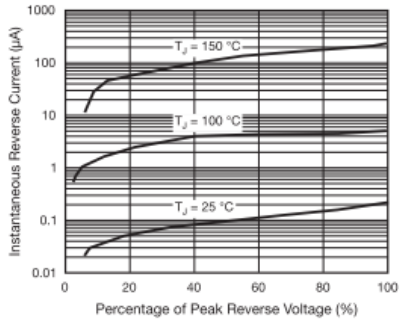


Fig. 4.9 Typical Reverse characteristics of 1N4007 diode [135]

3.2.3. Load Active Stage

Once the buffer capacitor is connected to the load, the voltage detection stage is disabled, thus reducing the overall power consumption of the energy management circuit to the consumption of the logic gates.

When the task is completed or the voltage of the buffer capacitor is approaching a predefined threshold limit, the connection between the load and the buffer capacitor should be broken. This is done by pulling the CTLR line low. The next subsection will address the requirements for disabling the connection.

3.2.4. Disconnecting the Load

When the buffer capacitor voltage level drops below a predefined threshold voltage, the connection between the load and the input buffer capacitor is interrupted in order to prevent over-discharging of the input

capacitor. The threshold voltage is usually selected to be the minimum operating voltage of the component with highest minimum operating voltage. This is typically 1.8 V for most modern microcontrollers, however, some sensors can operate only down to 2.3 V or 2.7 V, and hence these voltage levels would be selected as disabling thresholds.

In order to disable the switch, the ground potential should be applied to the control input CTRL. This can be done using a dedicated analogue voltage monitor that will monitor the voltage across the load. Another option is to simply disable the switch by using a pin from the microcontroller that is powered from the buffer capacitor when the task is done. In either case, it is imperative that upon disconnecting the output voltage, the CTRL pin is kept close to the ground potential until all capacitances in the load circuit get depleted.

In case of some microcontrollers, when the voltage drops below 1.6V they will enter a state known as "brown-out-reset" (BOR) [74]. In this condition, the microcontroller is kept in reset by internal circuitry, thus preventing any uncontrolled behavior due to insufficient voltage for stable operation. In reset condition, the power consumption of the microcontroller is in order of microamperes. Another consequence of placing the MCU in a reset condition is the change in the direction of the I/O pin settings. If the CTRL pin was controlled directly from the microcontroller, the NOR gate might get activated due to the change of pin settings during BOR. As the discharge of the output capacitances takes time due to low current draw of the MCU in reset state, the voltage on the CTRL pin can rise due to leakages in the output driver of the I/O pin of the MCU. The rise of voltage on this pin will reactivate the switch SW. This kind of behavior is undesirable. Therefore, special care needs to be taken when designing the CTRL control circuit. In Chapter 5, an example of an interface circuit between CTRL signal line and a microcontroller is explained in detail.

The circuit has been realized on a PCB with special care taken to minimize the possible leakage currents on the PCB. This has been done by removing the copper pour from the top layer of the PCB, thus removing the potential leakage from the tracks to the copper pours. The clearance between tracks, with a few exceptions was kept over 0.762 mm.

3.3. Measurements

The expected power consumption level of the circuit was in order of nanowatts, therefore, the measuring approach selected was to monitor the charging and discharging a capacitor of known value in order to determine the power consumption. This approach was also selected because it was close to the expected operating conditions of the circuit, as the circuit is designed to operate with a buffer capacitor attached. Furthermore, this approach avoided

the use of a high value resistance for current sensing. It also allowed the circuit to activate properly using energy stored in the buffer capacitor which wouldn't be possible if high values of sensing resistances were used. Having a capacitor in the input also allowed filtering of the high frequency noise that could be coming from the supply and from the environment.

The setup for measuring the power consumption is given in Fig. 4.10. The buffer capacitor used for the measurement was a ceramic X7R 914nF 50V capacitor. The resistor used was 1GΩ +/-10%. The power supply voltage was set to 20 V resulting in a 20 nA maximum input current. The measurements of the buffer storage voltage were performed using an oscilloscope with a voltage follower placed between the circuit and the probes of the oscilloscope. This was done in order to increase the input impedance of the measuring equipment, thus minimizing the impact of the measuring equipment on the circuit. A block diagram of the setup used for measuring power consumption is given in Fig. 4.10.

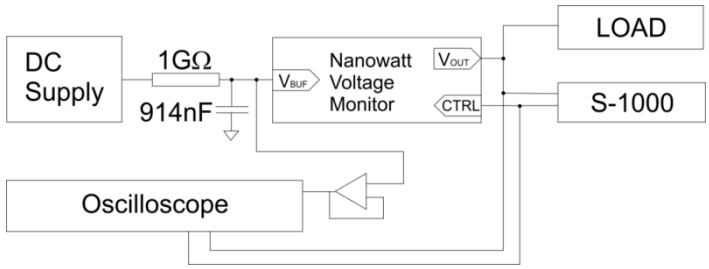


Fig. 4.10 Block diagram of the setup used for demonstrating the circuit operation

The threshold voltage of the low current voltage monitor was set to be around 2.5V using a green LED in combination with a red LED. As earlier stated, the low current voltage monitor requires some control mechanism to disable the connection between the input buffer and the load. For this purpose, a Seiko S-1000 voltage monitor was used [68]. The threshold voltage of the voltage detector was selected to be 1.9V. This can be considered a safe turn off voltage for most microcontrollers and radio modules on the market today.

In the beginning of the measurement all capacitors in the circuit were emptied. Then the power was applied and the voltages in the circuit were monitored. The graph of the changing voltage on the buffer capacitor can be seen in Fig. 4.11.

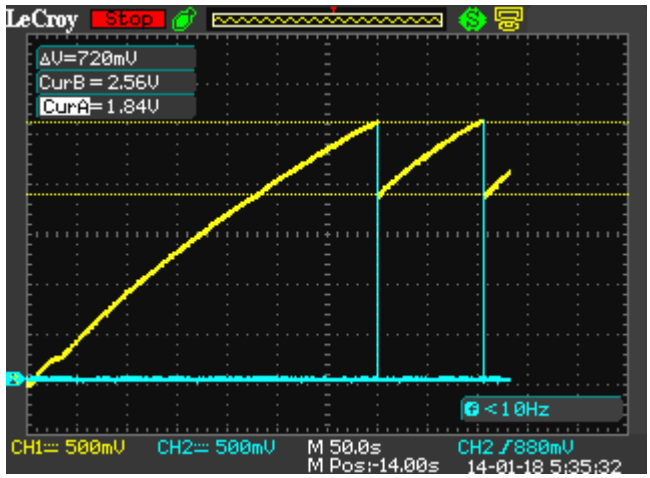


Fig. 4.11 Input buffer voltage (yellow) and output voltage of the voltage monitoring circuit (blue) when supplied from 20V power supply through 1GΩ resistor with 914nF buffer capacitance

In the beginning of the charging process, a small plateau can be observed on the buffer voltage. This is the moment where the voltage monitoring stage gets connected as the transistor separating the input buffer from the voltage monitoring stage starts to conduct. The charging of the buffer continues once the C_IN capacitor on the input of the voltage monitor gets charged.

The slope of the charge was almost linear, indicating a small change in the total power consumption of the circuit throughout the charging process. Based on the average slope of the voltage on the input buffer capacitor during charging, it was easy to determine the current consumption of the circuit. The average current from the supply was 18.72 nA. The current consumption was calculated for the change of input voltage from 0.5V to triggering voltage in order to avoid the impact of the C_IN capacitor charging. The formula used for calculating the average current consumption was:

$$\Delta I = \frac{C\Delta U}{\Delta t} \tag{4.2}$$

,where C is the total capacitance attached to the input of the circuit, ΔU is the change of the input voltage, while the Δt is the time it took for the input voltage to change. Therefore, a 914 nF capacitor was charged in 290 s from 0.5 V to 2.56 V resulting in average charging current of 6.49 nA. Therefore, as the average supply current was 18.72 nA the average current consumption of the NVD was 12.23 nA.

In the implementation section, the activation of the load was explained as a two-step process. First, the voltage monitoring stage would activate, and remain activated until the circuitry attached provided a stable supply voltage level on the CTRR input of the NOR gate. During this time, the output voltage of the voltage monitoring stage is dropping as it is disconnected from the buffer capacitor and is consuming the energy stored in C_IN capacitor, connected to the input of the voltage monitor. This operation can be seen in Fig. 4.12.

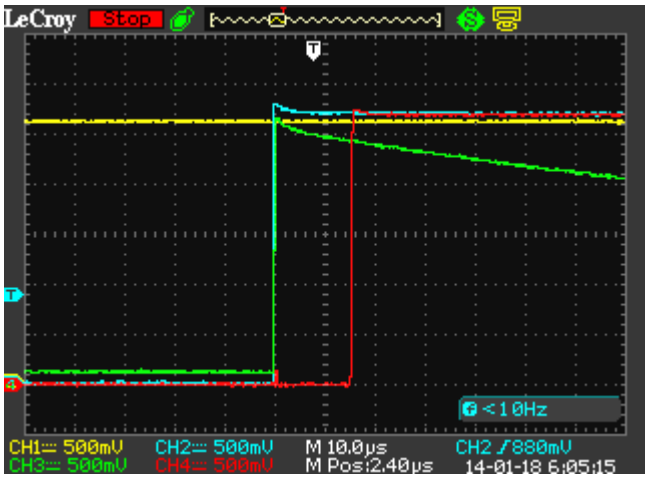


Fig. 4.12 Connection of the load to the buffer capacitor. Output voltage level (blue), output of the voltage monitor stage (green), control line voltage (red)

In this demonstration, an S-1000 voltage monitor circuit was used for controlling the CTRL line. The S-1000 circuit has a 12 µs propagation delay. This, in turn, means that the voltage monitor has to keep the SW active for the duration of the propagation delay before the S-1000 takes over the control of the SW. This can be seen in Fig. 4.12 as the red signal line.

Based on the propagation delay of the S-1000 it is possible to optimize the values of C_IN in order to reduce the energy loss in C_IN. In Fig. 4.13 the waveform of the voltage on the output of the voltage detection stage is shown. It can be seen here that there is an increase in power consumption as the C_IN discharges. This is coming from the fact that the voltage on the input of the NOR gate transitions between logic one and logic zero, hence increasing the power consumption. The measurements have shown that its current consumption reached 500 µA during this transition.

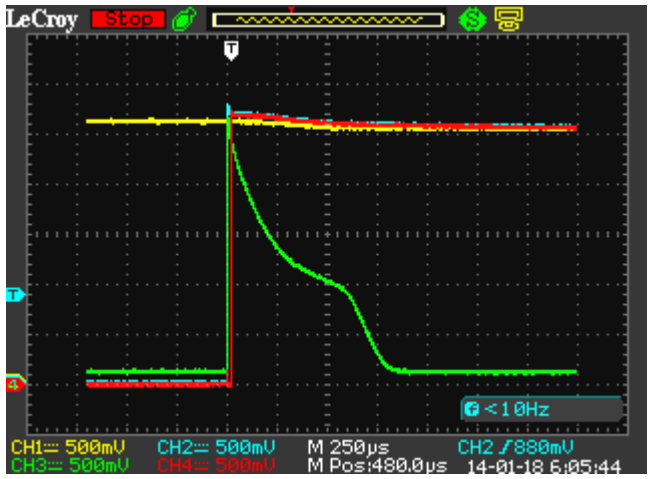


Fig. 4.13 Impact of the discharging of C_IN during disabling of the voltage detection stage

The discharge time of C_IN defines the minimum time the load should operate before attempting to close the main SW. In this case the discharge time was 750µs. If the external circuitry sets CTRL line to low logic level before this time elapsed, the second input to the NOR gate, connected to the voltage detector output stage, might still be interpreted by the NOR gate as logic one. This occurs as C_IN didn't have sufficient time to get emptied. This would lead to extended activation of the switch, thus discharging the input capacitor further and wasting energy.

After the input buffer capacitor dropped below 1.9V, the S1000 circuit changed its output to low forcing the SW to close allowing the input buffer capacitor to recharge.

Analysis of the current consumption of the NVD between two activation cycles showed that the average current consumption of the circuit in this stage was 11.54 nA.

The second set of measurements was done on a modified version of the circuit that was aimed at a slightly higher current consumption once it is activated. This variation is aimed at applications where it isn't required for the load to continue operation for longer periods of time after being activated by the voltage monitoring circuit.

For example, sensing a sensor value and sending the result wirelessly. In this case a 1MΩ resistor was placed between the gate of the SW and the buffer capacitor. The switch was also substituted, so a P-type MOSFET it was used instead of an analogue switch ADG802. This change made this variant of the circuit cheaper than the first implementation and easier to assemble. By placing a resistor in the gate of the MOSFET, the MOSFET would be

polarized from the buffer capacitor and the problem of having unstable output during the startup stage of operation on the NOR gate is removed. The second difference was using 74LVC02 circuit instead of 74AUP02, as this circuit has demonstrated lower current consumption.

The circuit was connected to a 10V power supply through the 1GΩ resistor, as used in previous setup, and the same buffer 914nF capacitor. Using the same technique to determine the average power consumption as before, the average charging current was determined to be 5.89nA while the average supplied current was 8.72nA resulting in an average current consumption by the NVD of 2.83nA.

However, this circuit has increased power consumption during operation. The increase of the power consumption is coming from the resistor used to initially polarize the gate of the SW. The increase of the consumption was several microamperes, depending on the voltage. However, in some applications this isn't an issue if the load is active only during several milliseconds, thus making the energy loss on the resistor during the operation neglectable.

The ultra-low current consumption of the modified NVD was demonstrated by using this variant of a circuit as an energy management for a wireless sensor node that was powered with a solar cell in low light conditions. In this setup a 4.5cm2 solar cell ECS300 from EnOcean [56] was used in 1 lux light conditions. There was no instrumentation attached to the wireless sensor node in order to avoid any potential antenna affects and possible charge injections into the circuit as the current levels were in nanoampere range.

Under the light conditions of 1 lux the circuit was able to operate and leave enough power to charge the buffer capacitor. A wireless reading of temperature occurred every 3.5 minutes under these light conditions.

3.4. Discussion

The discussion first addresses the limitations of the proposed circuits, followed by discussion on possible external control circuitry.

The limitations of this circuit are multiple. Most of them are coming from the fact that the main voltage reference in the circuit is an LED. The selection of threshold voltages is limited to available combinations among LEDs. Furthermore, as shown in the implementation section, the threshold of the system is dependent on the rate of charge of the buffer capacitor. This can result in varying threshold voltages depending on the variations in the power output from the harvester, leading to varying operating conditions for the load attached. Additionally, as the LED is a semiconductor device, the threshold will be prone to temperature and humidity changes.

It was repeatedly stressed that the circuit requires an external circuit in order to disable the main switch connecting the load and the buffer capacitor.

There are several possible options that can fulfill this task. One is the use of a dedicated voltage detector/monitor or an operational amplifier in the voltage monitoring configuration. The second option is the use of a microcontroller that is usually present in most modern wireless sensor node applications.

The use of an analogue voltage detector or an operational amplifier is advised only if their power consumption, during the operation of the load, is neglectable compared to the total energy used by the load. If that is not the case, the load should disable the voltage monitor when the task is done. For example, in an application where an energy harvesting powered sensor is programmed to perform a wireless measurement task, the microcontroller could signal the SW to open when it has completed the task. In such application scenario, there is no need for additional monitoring of the buffer voltage level. Doing so would only increase the power consumption, complexity, and the price of the circuit.

During the testing it has been observed that the voltage threshold circuit would become very sensitive around the triggering voltage. The changes in its immediate surroundings, for example, people moving could trigger the circuit. Further investigation might show the potential of using this circuit as a sensor.

One possible use of this circuit would be as a timing circuit, or a voltage controlled oscillator. As a timing circuit, it could be used to start a microcontroller after a predefined time set by a RC network that is monitored by the voltage monitoring stage. In this way, by using a small capacitance and a large resistor, long time delays can be generated with minimal power consumption.

3.5. Summary

In order to interface energy harvesters with high output impendences it is necessary to design circuits that are capable of operating using only nanoamperes of current, leaving the rest of generated current for being collected in a buffer capacitor. The measured current consumption of the Nanowatt Voltage Detector circuit suggests that it can be used for such applications.

The measured total power consumption, of proposed Nanowatt Voltage Detector circuit demonstrated that it can be effectively used for monitoring the charging process of the buffer capacitor even in cases of very high output impedances of energy harvesters. This circuit can be used in combination with a standalone voltage monitor for controlling the connection between the load and the buffer capacitor, or as a part of a more complex system where disconnecting the load from the buffer capacitor is done in a more advanced way, allowing greater power efficiency. An example of such a system is shown in Chapter 5.

4. ADC Power Management

When the sensor node has only a single predefined task, for example, sensing a single sensor and transmitting the measurement, then the energy management stage can be rather simple. In this scenario, as the task is always the same, the amount of required energy to perform it is fixed. Therefore, the energy management stage will only be required to wait until the buffer storage reaches a predefined threshold. After the threshold has been reached the storage is being connected to the rest of the circuitry and the task is executed. Then the recharging process begins again. This simple energy management operation has been addressed in the previous section.

However, if a more complex wireless sensor node is at hand, this simple approach to energy management doesn't provide enough flexibility. Let's assume that the application performs two tasks T_1 and T_2, sensing from sensors S_1 and S_2. Both tasks have different individual energy requirements E_1 and E_2, where $E_2 > E_1$. Also let's assume a scenario where task execution of T_2 is dependent on the result of measurements done in T_1. Under these conditions there can be a number of N times T_1 measurements are done before T_2 is performed.

If an approach to energy harvesting presented in previous section is used, there is only one available threshold in the circuit. Therefore, it is necessary to select the threshold that would correspond to the energy required by the T_2 task. This means that every time there was sufficient energy for the T_1 to run, the system wouldn't be activated, but would wait for E_2 level of energy to be accumulated before activating. If the energy requirement for T_2 is much larger than the energy requirement for T_1, this would introduce a significant delay during activation, and a long start delay can be a critical factor in some applications.

Another scenario that would require a more flexible approach to energy management are the applications deployed in an environment where the energy availability is changing and tasks should be coordinated based on the available energy. Using the previously introduced tasks and their energy requirements, let's consider a scenario where the energy harvester isn't able to charge the buffer storage to the energy level required for E_2 to run, but it is possible to charge it to activate task T_1 instead. The approach with a single threshold voltage would limit the operation to only activate when there is sufficient energy to run T_2, missing on the opportunity to run T_1 tasks.

Further issues a single threshold system can encounter if the system has deadlines on executing the tasks, and the tasks have different repetition rates. The delay introduced by waiting for the buffer to charge enough so the task with maximum energy requirement could be executed could potentially violate a deadline of a task with low energy requirement.

In the end, it would be beneficial to have a possibility to select which tasks are going to be run based on the incoming power from the generator. An advanced energy management should be able to react to the change in the power output of the harvester, adjust the threshold voltage and the task execution.

These are only some of the shortcomings of simple energy management circuits. In conclusion, there is a need for a more flexible energy management system that would operate in nanowatt range using off the shelf components. In this range, the increased flexibility will allow a better utilization of the scarce energy source.

To the author's knowledge, there haven't been reports on energy management circuits that had a possibility to dynamically change the threshold, while operating on the capacitor buffer storage, utilizing nanowatt energy levels.

Monitoring of the voltage level is usually done using ultra low power operational amplifiers, comparators or using a circuit similar to one proposed in Section 3. However, these circuits have one major drawback either stability, in case of the circuit described in Section 3., or the current consumption that is in order of hundreds of nanoamperes.

Overview of the lowest power consuming commercial off the shelf voltage monitoring circuits is presented in Table 4.1.

Table 4.1 The commercially available off the shelf nanowatt comparators and monitors

Manufacturer	*Part Name*	*Current consumption (nA)*	*Operating Voltage Range (V)*
Seiko	S-1000[1]	350	0.95 – 5.5
Linear Technologies	LTC2935	500	0 – 5.5
Linear Technologies	LTC1540	280	2 – 11
Torex Semiconductors	XC61	700	0.8 – 6
Texas Insturments	LPV7215	580	1.8 – 5.5
NanoPowerSolutions	NPS1101[2]	100	2.4-5.5

[1]) This product was discontinued at the time of writing the thesis
[2]) Data was based on preliminary datasheet from the manufacturer

The power consumption of the circuitry used for monitoring the voltage level of the buffer defines the minimum power output required by the harvester in order for the system to collect energy. In order to reduce the power consumption, a new approach has been introduced. The idea is to remove the static power consumption of an operational amplifier and replace it with timed analogue to digital conversions performed by the microcontroller. In this approach, the microcontroller would actively make decisions on the course of action depending on the measurement value of the current voltage on the buffer capacitor, hence increasing the flexibility.

In the case of nanowatt and microwatt power sources the amount of time required by the source to charge the buffer capacitor is measured in seconds, minutes or even hours. Therefore, it could only be necessary to activate the circuitry and measure the voltage in predefined interval and not waste energy on the continuous monitoring of the buffer voltage that is slowly changing, as is currently done with comparators. Furthermore, as the measurement is done by the microcontroller, it is possible to immediately act based on the measured buffer energy level. For example, based on the voltage of the buffer, the MCU can decide whether to continue charging the buffer or execute the pending task. Another possibility is to calculate the priorities of the tasks based on the changing in the harvester power output which can be deduced from the change in the buffer voltage between two measurements.

This section will address the theory of operation of the proposed approach followed by modeling the circuit. The modeling section consists of profiling different microcontrollers in order to obtain measurements for building the model. Following the modeling section is the implementation section that is going to address the techniques for reducing the power consumption of the circuitry with special accent to the frequent power cycling of the MCU. Finally, measurement results are presented followed by the discussion section.

4.1. Theory of Operation

The ADC energy management circuit is based around a real time clock (RTC) with low power consumption AB1814 from Abracon [63] that is connected to a microcontroller. After initial powering up of the circuit, the RTC is programmed with the period until the next analogue to digital (AD) conversion. The MCU then finishes the application specific tasks and is deactivated. The deactivation can be either placing the processor into low power regime of operation, commonly referred to as “sleep”, or completely removing the power of the microcontroller. The choice of the deactivation method is dependent on the application and target power consumption.

The RTC activates (wakes-up) the MCU after the previously set period expires. The goal of the next step is to determine the energy available in the buffer. This can be done either by directly measuring the buffer storage voltage level or the MCU’s supply voltage level. In cases where the MCU is powered directly from the buffer storage, the MCU calculates its power supply voltage by measuring the voltage output of a known voltage reference. In the case where there is a DC/DC stage, or some other circuit between the buffer storage and the MCU that provides the MCU with a stable supply voltage, it is only necessary to measure the buffer voltage level. If the MCU is neither directly connected to the buffer storage nor a stable power supply, the ADC of the

MCU should be provided with a known reference while performing the measurement of the buffer voltage level.

After performing the measurement of the voltage level of the buffer storage, the MCU can decide its next step. If there is sufficient energy for the application specific tasks to be performed, the MCU can immediately start execution of the task. Upon finishing the task, or tasks, required by the application, the MCU has two choices: (i) waking up next time after the same time interval as previously used; (ii) to set up new time interval by programming the new wakeup time in the RTC. By using a fixed interval between measurements there is no need to communicate the new time to the RTC, hence reducing the energy consumption. After all tasks have been done, or the initial measurement shows that there was no time to perform any tasks, the MCU is disabled, thus allowing the continuation of charging the buffer storage.

Based on the state of the MCU power supply between two consecutive AD conversions, two scenarios can be identified:

- Scenario 1 (S1) – The microcontroller is powered and waiting in low power mode (sleep) for the wake up signal from RTC
- Scenario 2 (S2) – The microcontroller is unpowered and will have its power supply restored by the RTC

The MCU will be free to select which scenario it will use based on the available power, pending tasks and application requirements. The differences between operating scenarios will be addressed now in detail.

4.1.1. Scenario 1

In this operating scenario, the MCU is being kept in low power mode. In this mode, the RAM inside the MCU is being maintained and the MCU continues operation upon receiving a signal from the RTC. This scenario has increased power consumption due to RAM retention and all leakage currents coming from/to pins of the microcontroller, as well as the other peripherals MCU is connected to. On the other hand, the MCU will continue the operation in the matter of microseconds after the activation signal has been received [86, 74]. It would also return fast to low power mode of operation after its tasks are performed, and there will be no losses in charging capacitances connected to the supply of the MCU. This scenario should be used in the cases of frequent activation of the MCU.

4.1.2. Scenario 2

This is the lowest power scenario, where the MCU is powered off and all leakage currents associated with the MCU are thus removed. However, in this scenario, every waking up of the MCU is an energy expensive process. When

the power is applied to the MCU block, all capacitances that MCU is connected to need to be charged, followed by the process of the MCU initialization. Only then, the AD conversion can be performed. When the process is done, and the MCU needs to be disabled, the turning off procedure needs to be performed carefully, as the I/O pins of the MCU are likely to change state during this process. This issue has been addressed in the implementation section. However, even with all of the mentioned losses, in case of long delays between measurements, this scenario is still more power efficient than Scenario 1. This will be later demonstrated in both modeling and measurement sections. If the application requires the data to be retained between two measurements this can be implemented using memory that is located outside the MCU.

4.2. Microcontroller Selection

From the theory of operation, it can be concluded that the system is dependent on the operating characteristics of the microcontroller. The entire approach of the proposed energy management is based on the efficiency of performing three tasks: first, performing the AD conversion, second processing the data, and in the end, communicating with the RTC unit.

In order to select a low power platform to implement the ADC based energy management, three different microcontrollers were evaluated. The microcontrollers have been selected from different manufacturers, represent different architectures and have different operating modes. The objective of this comparison was to determine the most power efficient platform for performing the AD conversion based energy management (ADC energy management). Furthermore, the goal of this profiling was to determine the behavior of different MCUs when exposed to frequent power cycling which would be necessary in the case of Scenario 2 implementation. Additionally, the detailed measurements of the microcontroller operation were performed in order to provide an in-depth understanding of power consumption of different stages of operation.

The MCUs selected have been chosen as representatives of low power families from different manufacturers. The choice was made after searching for the lowest power advertised microcontrollers. The MCUs tested were: PIC18LF14K22 by Microchip [66], MSP430G2553 by Texas Instruments [74] and EFM32TG222 [86] by EnergyMicro (now SiliconLabs). Evaluation of each platform will be done in a separate subsection. In the end, all platforms will be compared in both operating scenarios of interest.

All measurements presented in the following subsections were done using an oscilloscope and a shunt resistance. The MCUs have been tested without anything attached to them except the decoupling capacitors required by the datasheets. This will produce slightly more favorable results compared to real

life scenarios where the MCUs would be surrounded by additional peripherals. However, the measurements will provide a good starting point for modeling.

The existence of the decoupling capacitors on the boards will influence the measurements. Tasks with low energy footprint, such as performing the AD conversion or sending one byte of data over SPI, consume energy in order of nanojoules, therefore, the majority of this energy is going to initially be delivered from the decoupling capacitor. After the task is performed the decoupling capacitor would slowly recharge from the power source. When the power consumption was measured this recharging of the decoupling capacitor was taken into account.

In order to model the behavior of the two operating scenarios, the power consumption the following operations was profiled: active power consumption, energy consumption during the AD conversion and the energy consumption during the data transfer over the SPI bus. The SPI power consumption is important because setting up of the RTC, as well as storing data in an external memory in case of the Scenario 2 is done over the SPI. The SPI has been chosen over I^2C due to its higher speed and lower overall power consumption.

Besides measuring individual operations, entire expected operation for each scenario was performed and the energy consumption was measured. An assumption was made that the MCU will be powered directly from the buffer storage, hence it is necessary to measure a known voltage reference in order to determine the supply voltage.

For the Scenario 1, the energy consumption was measured while the MCU was performing the following tasks: activating the MCU from the low power state, waiting for the reference to stabilize, performing a single ADC followed by returning to low power state.

For the Scenario 2, energy consumption was measured from applying power to the MCU, through its startup, activating of reference followed by performing an ADC, concluding with the disabling of the MCU.

Throughout the profiling sections, instead of presenting energy consumption, the charge consumption is often presented. This is done to demonstrate that for certain tasks the voltage has no or little impact on the current consumption of the circuit. Therefore, the increase of the voltage is only going to result in increased thermal dissipation of the circuit. For the tasks that have increased current consumption as the result of increased supply voltage, the power consumption is presented instead.

4.2.1. Profiling of the PIC18LF14K22

The microcontroller PIC18LF14K22 is an 8-bit microcontroller by Microchip. It is a representative of the Microchips XLP series of

microcontrollers that have been designed and developed specially for ultra-low power applications.

Active and Sleep Power Consumption

This microcontroller was specially designed to have a low "sleeping" current. Based on the datasheet, the RAM retention on this microcontroller requires only 32nA at 2V, hence making it a very good choice for the applications of the ADC energy management that favors Scenario 1 mode of operation. The sleeping current consumption has been verified through measurements, and the results are presented in Fig. 4.14.

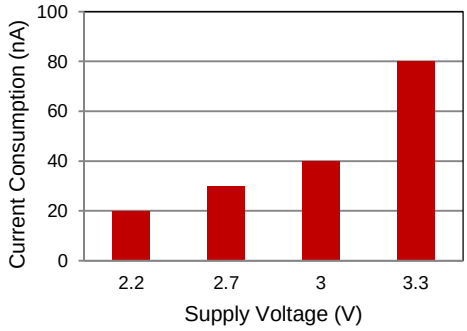


Fig. 4.14 Current consumption in the lowest power mode of the PIC18LF14K22

The second step in the profiling was determining the power consumption during the operation of the microcontroller. The current consumption of the core running an empty loop executed from flash is presented in Fig. 4.15.

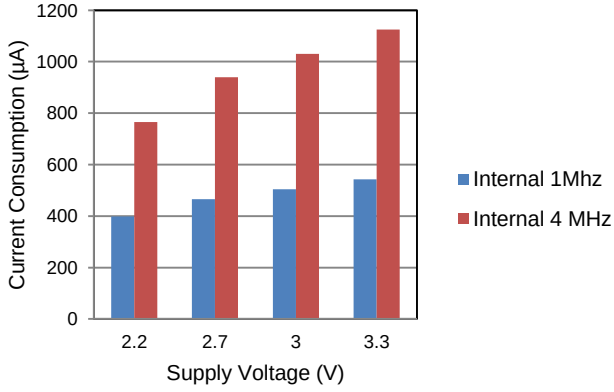


Fig. 4.15 Power consumption of PIC14LF14K22 under different operating voltages and clock speeds

From Fig. 4.15 it can be concluded that the current consumption doesn't scale linearly with the clock. Hence the most power efficient approach to code execution would be to run the core as fast as possible, and sleep when waiting for the peripherals to complete the given task.

A note should be given here that on the PIC microcontroller, each instruction requires 4 clock cycles to complete, and therefore, one should be cautious when comparing the power consumption for different platforms based on the clock frequency. For example, the MSP430 performs one instruction per instruction cycle, so a PIC18LF14K22 running on 16MHz is executing the same number of instructions per second as a MSP430 running on 4 MHz This is a reason why in measurements were also performed at 4 MHz, allowing a direct comparison with the MSP430 platform and the EFM32 platform when running close to 1MHz.

A characteristic feature of the PIC microcontrollers is their ability to start code execution before the oscillator stabilizes. This allows for power saving in cases where the core should be turned on for just a brief period of time. For example: to start a new conversion, or toggle a pin. For such operations to be executed, it is not necessary to wait for the core to reach the set high frequency, instead, the code can be executed while the frequency is changing. This is demonstrated in the can be seen on the power consumption measurement shown in Fig. 4.16.

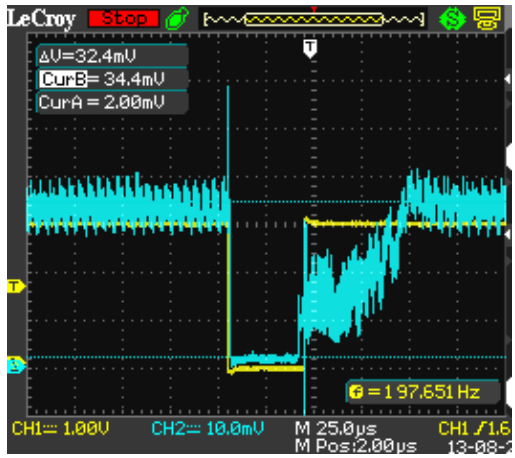


Fig. 4.16 The current consumption of the PIC microcontroller. After sleep, during which it performed and ADC, The PIC's power consumption increases as the core switches to higher operating frequencies

The blue signal line in Fig. 4.16 shows the current, consumption while the yellow signal line indicates the beginning and the end of the ADC. The rise of the current consumption, after the rising edge of the yellow signal line, demonstrates the increase of the current consumption due to increasing

operating frequency of the MCU from 1MHz to 16MHz. During the change of frequency the code is being executed.

Analog to Digital Conversion

After measuring the active power consumption, the next test was aimed at measuring the power consumption of the ADC (Analogue to Digital Converter). The ADC on PIC has a lot of options for setting up the AD conversion. Some of the options are selecting different clock source for the AD conversion, sampling time and the references used. In order to find the most optimal configuration, two sets of measurements were performed. The goal was to determine the difference between the states when the core is put to low power sleep regime during AD conversion and when keeping the core active while the ADC is in progress.

The first set of experiments was performed aimed at keeping the MCU core disabled hence reducing the power consumption. As the main clock is disabled it was necessary to use an internal 500 kHz clock for the ADC. However, the MCU needs to be activated in order to setup the ADC and perform the evaluation of the result once the measurement is done. Therefore, it was necessary to determine which MCU frequency of the operation was more power efficient. The first set of measurements was performed on the 16MHz core clock, followed by measurements done on the 4MHz core clock. The results are shown in Fig. 4.17.

The second set of measurements was done while the core was active while waiting for the ADC to finish the conversion. This approach is referred to as "polling", because the software is constantly checking the status flag in order to determine if the AD conversion has completed. In this way the delay required for the core to activate from low power regime is avoided, however, the core is running all the time hence increasing the power consumption. The results of the measurement are shown Fig. 4.17.

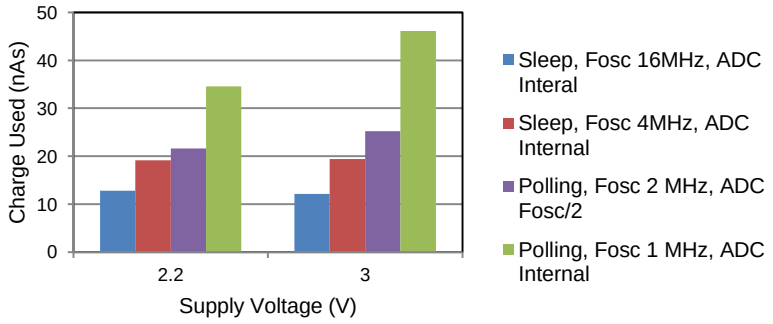


Fig. 4.17 Charge consumption of performing a single ADC measurement under different operating conditions; F_{OSC} was the MCU operating frequency while ADC Internal refers to the internal 500 kHz RC oscillator

In conclusion, polling for the end of the AD conversion is less power efficient than placing the MCU to low power mode.

Serial Peripheral Interface

The last important parameter was the energy consumption of the MCU during SPI operation. On the PIC microcontrollers the maximum frequency of the SPI, when the PIC is the master device in communication, is Fosc/4, where Fosc is the frequency of the core clock. It is also important to note that the core can't be put to lowest power mode during the SPI operation, but only to the IDLE mode where only the core of the MCU is disabled. The power consumption in IDLE is still significantly lower compared to the active power consumption. It should be noted that the power consumption in IDLE is dependent on the set frequency of the oscillator.

Fig 4.18. demonstrates the power consumption of the MCU running the SPI communication under different scenarios. The main focus of measurements is on the low packet lengths due to the nature of the communication between the MCU and the RTC.

Similar to the ADC profiling two methods have been examined. First, where the core of the MCU was put to low power mode and second, where the MCU was active while waiting for the SPI to finish the transmission.

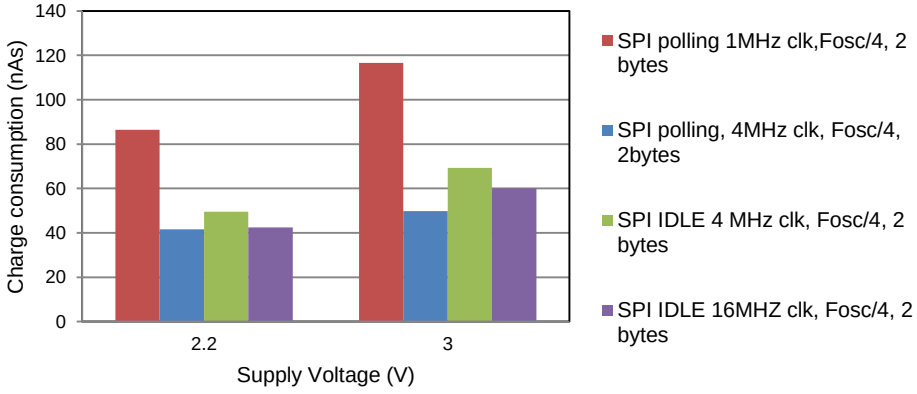


Fig. 4.18 The charge consumption of different operating configurations of SPI on PIC microcontroller

In Fig. 4.18 the SPI polling refers to checking in software for completion of the SPI transfer, while SPI IDLE refers to interrupt based operation with the core placed to IDLE during transmission of each byte. Fosc/4 indicates the SPI clock speed while the last parameter is the packet length.

From the charge consumption it can be seen that the polling method, where the MCU was run at 4MHz, was the most power efficient. However, the

methods utilizing placing the core to IDLE during transmission didn't fall far behind. Further increase of the MCU clock speed would lead to further reduction of the charge consumption, however, the RTC that the MCU is mainly communicating with in this application couldn't support higher SPI clock speeds.

The charge consumption for transmission of longer packets was determined using the polling method. The measurement results are shown in Fig. 4.19.

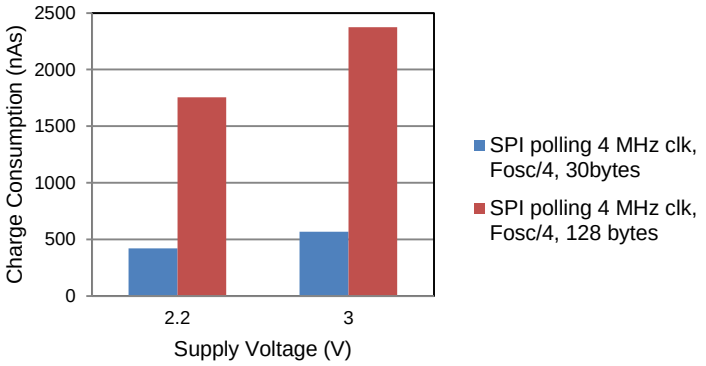


Fig. 4.19 Charge consumption required for transmission of different packet lengths over SPI

There is a fixed overhead associated with every SPI operation and the dynamic overhead associated with the variable packet length, hence a simple linear equation can be set. By solving this linear equation it is possible to model the expected energy requirement for arbitrary SPI communication packet length on this operating speed of the SPI.

Profiling the Energy Consumption for the two Operating Scenarios

The most efficient modes of operation for the PIC microcontroller were on 4MHz and 16 MHz with use of internal RC oscillator for driving the ADC. Before going into profiling the two operating scenarios of the ADC energy management explained in the theory of operation, the operation of the voltage reference needed to be included in the model.

The reference selected was MAX6018 by Maxim Integrated Products [119]. This reference was selected because it had the lowest energy consumption before the output of the reference became stable. This was important because the reference was only powered when the measurement needed to take place. This reference has a startup delay of 200 µs before the output of the reference can be used. In order to reduce the power consumption while waiting for the voltage reference to stabilize, the core was disabled and the timer was set to

run at 250 kHz clock speed. These things were done in order to reduce the power consumption during the waiting period.

The summary of energy consumption for two operating scenarios is shown in the

Table 4.2 .

Table 4.2 Energy consumption of PIC18LF14K22 under different operating conditions and scenarios

Operating scenario	*Voltage*	*Charge used (As)*	*Energy used (J)**
Scenario 2, clk = 4MHz	2.2	9.23E-07	2.03E-06
Scenario 1, clk = 4MHz	2.2	1.59E-07	350.4E-9
Scenario 1, clk = 16MHz	2.2	216.4E-9	476.0E-9
Scenario 2, clk = 16MHz	2.2	5.95E-08	1.03E-06
Scenario 2, clk = 16MHz, worst case	2.2	7.34E-07	2.52E-06

*) energy measurement has been done without accounting for the energy needed to charge the decoupling capacitors

A detailed current consumption can be seen in Fig. 4.20.

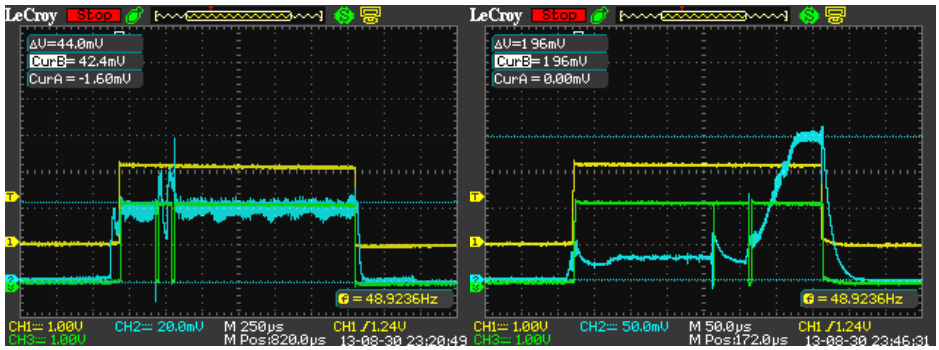


Fig. 4.20 The detailed current consumption on a) 4MHz and b) 16MHz for PIC microcontroller

In Fig. 4.20 the blue signal indicates the voltage drop across 100Ω shunt resistor. The green signal indicates the output from the MCU used to indicate different stages of operation. The interval between the first rising edge and the first falling edge of the green signal indicates starting up of the reference followed by a second high period that correspondent to the ADC conversion. The processing of the result follows. As it can be seen, the processing of the read result demonstrates a major impact on the current consumption. This isn't surprising as the platform selected is an 8-bit microcontroller, hence operating on a 10-bit ADC result requires a significant amount of cycles. This

can be improved by using only the higher 8-bits of the results at the cost of reduced precision.

During the 16MHz testing the microcontroller didn't have the same power consumption every time. By looking at the current consumption it became obvious that the microcontroller sometimes didn't reach the 16MHz operating frequency which meant that the processor wasn't operating as efficient as possible. This had a major impact on the power consumption as can be seen in

Table 4.2. This indicates that PIC18LF14K22 wouldn't perform stable in case of frequent power up cycles if the frequency used was 16MHz.

The collected results in this profiling section were used for modeling the behavior and comparison with other proposed microcontrollers done later in this section.

4.2.2. Profiling of the MSP430G2553

The profiling of MSP430 will follow the same process as the profiling done for the PIC microcontroller. An accent will be placed on the features of this MCU that were of special interest for ADC based energy management. The microcontroller selected for testing is a representative from the "value line" of Texas Instrument's microcontrollers that are designed for ultra-low power applications. This MCU has a wide variety of peripherals and 4 low power modes of operation allowing easy adjustment of operation in order to meet the low power requirements of the application.

Active and sleep power consumption

The most critical aspect in an application where the processor is required to be inactive most of the time is the sleep current consumption. The current consumption of MSP430G2553 in these two low power modes of interest is presented in Fig. 4.21. The active operation is referring to power consumption of the microcontroller when operating at 1MHz clock frequency while executing a while loop. The LMP0 is a power mode where the processor is not providing the clock to the core of the microcontroller, however, peripherals are clocked using a peripheral clock. This mode of operation is used when operating high speed peripherals, for example, the serial communication hardware blocks. The LPM4 is the lowest power mode available where the entire chip is powered down with the RAM retained. The processor resumes operation when activated from LPM4.

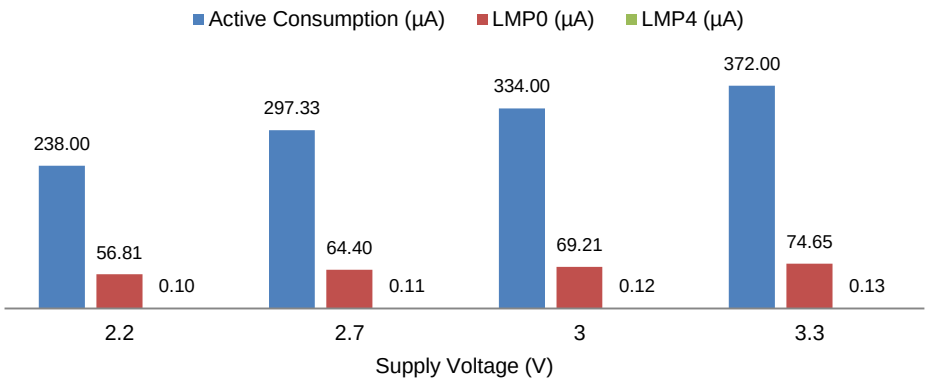


Fig. 4.21 The current consumption under different voltage levels for the required power modes

From Fig. 4.21 it can be easily concluded that stopping the core is advisable whenever possible, as the savings in current consumption are significant. Also the operating voltage has a major impact on current consumption in the case of MSP430G2553.

A characteristic of the MSP430G2xxx Value Line of MCU's is that their power consumption scales almost linearly with the increase of frequency. This means that the processor demonstrates only a small increase in efficiency as the frequency is increased. The frequency to power consumption graph is shown in Fig. 4.22. Therefore, I have selected to keep the MCU running on the same frequency as it has upon startup, which is 1 MHz. The potential saving in case of 2.2V power supply is around 15% if the processor is run on 8MHz instead. However, due to the fact that the system is activated and deactivated often, starting up the core at a higher frequency will consume more energy than will be saved by running the core at a higher speed.

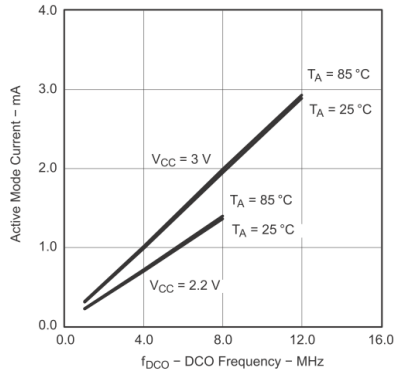


Fig. 4.22 Typical power consumption in active mode depending on the frequency of internal oscillator [74]

Analog to digital conversion

The MSP430G2553 has a 10-bit 200kbps Analogue to Digital Converter. This converter has a large variety of possible operating modes. As the basic process for the ADC energy management is performing the AD conversion, determining the most power efficient approach was important.

The ADC module on this MCU is equipped with an internal 5MHz clock that allows the MSP to perform AD conversion while in low power mode. A typical 10-bit conversion, in case where sampling is done in 4 cycles, requires 17 cycles of the AD clock [74]. When the AD oscillator is run on 5 MHz the AD conversion is executed in 3.4µs. On the other hand, the MCU is executing one instruction per microsecond when operating at 1MHz, meaning that the core will only be idle for a few cycles before the result is ready. The question that arises from this fact is: whether or not it is advisable, from the energy standpoint, to put the processor to low power mode during this interval.

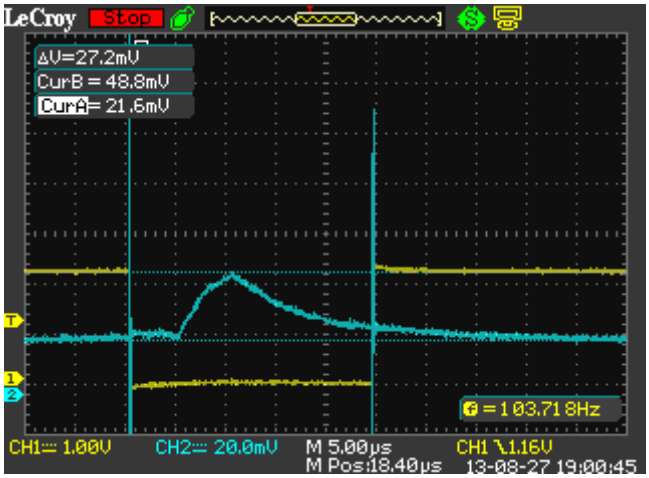


Fig. 4.23 Measured current consumption during AD conversion without placing the core to low power mode

In Fig. 4.23 the blue signal is the voltage drop across 100Ω resistor while the yellow signal is used to indicate the beginning and end of the AD conversion. It can be seen that setting up the AD conversion took 5µs followed by the conversion that lasted <5µs. The execution of the AD conversion can be seen as the increase of the current consumption. After the conversion is done, the software polls for the flag for AD conversion competition, retrieves the result from the AD converter and returns from the ADC function. The return from the AD conversion function is shown with rising edge of the yellow signal.

The two spikes in the current consumption were originating from charging/discharging the capacitance of the oscilloscope probe during change of the output on the I/O pin the probe was connected to.

Another approach to the AD conversion was measured as well. Instead of polling for the flag indicating the competition of the AD conversion, interrupt based solution was implemented that placed the core to low power regime during ADC operation. The comparison between the polling approach and interrupt based approach is shown in Fig. 4.24.

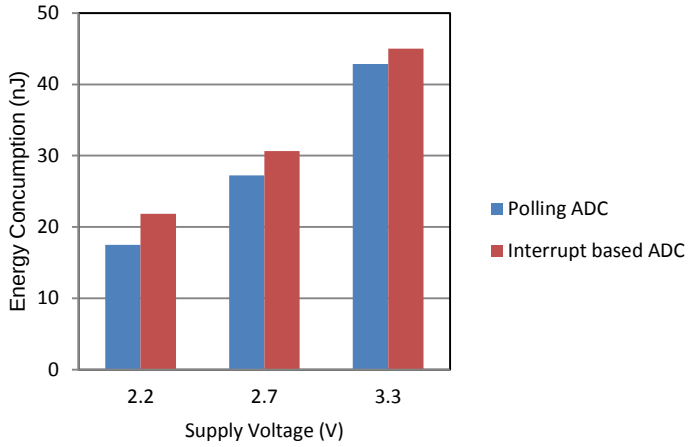


Fig. 4.24 Energy consumption of polling and interrupt based operation of ADC

Based on the measurements from Fig. 4.24 a conclusion can be drawn that both approaches of performing AD conversion yield similar results. The polling approach has shown marginally better results and will be used when modeling the ADC energy management operation.

Serial Peripheral Interface

The MSP430G2553 has a dedicated hardware block for serial communication. This module has serial peripheral interface support. One of the features of this module is that it can provide a SPI clock signal that is at the same frequency as the core frequency. As a consequence, the operation of the MCU can be optimized to have minimal delay between sending consecutive bytes.

Transferring each byte over the SPI takes 8 clock cycles plus an overhead to start the transmission and signal that the transmission has been completed. Therefore, as soon as the buffer for transmission is filled with the byte, the hardware of the SPI begins transmission. In the next 8 clock cycles the transmission will be done, during this time the MCU can perform a check if

the byte being sent is the last byte to be sent. After this check is performed there are only 3 clock cycles remaining before the SPI hardware is ready to accept next byte. Therefore, similar to the case with ADC, such a short delay is not convenient for putting the processor to sleep. It has been measured that interrupt based approach requires 20µs to transmit a single byte. During this transmission no reduction in power consumption was observed hence leading to a conclusion that interrupt based solution would only increase the time required to perform the data transmission and hence the power consumption.

The energy consumption required to transmit different packet sizes is measured at two voltage levels and results are presented in Fig. 4.25.

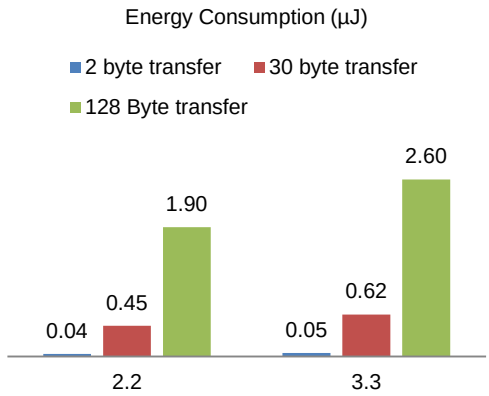


Fig. 4.25 Energy consumption during transmission of various packet sizes on MSP430G2553

Profiling the energy consumption for the two operating scenarios:

The next step in profiling the energy consumption was performing the actions required by the two scenarios of operation on the MCU that are going to be used in the ADC energy management. The software used was performing the same tasks as described in profiling of the PIC18LF14K22. The current consumption profiles during the Scenario 1 and the Scenario 2 are given in Fig. 4.26.

In Fig. 4.26 for the Scenario 2, a large initial spike can be identified. This current spike was coming from the decoupling capacitor being charged. It should be noted that the decoupling capacitor used was 100nF, which is specified as the minimum decoupling value that should be used with the microcontroller. The issue of energy loss on decoupling capacitor will be addressed in the implementation section.

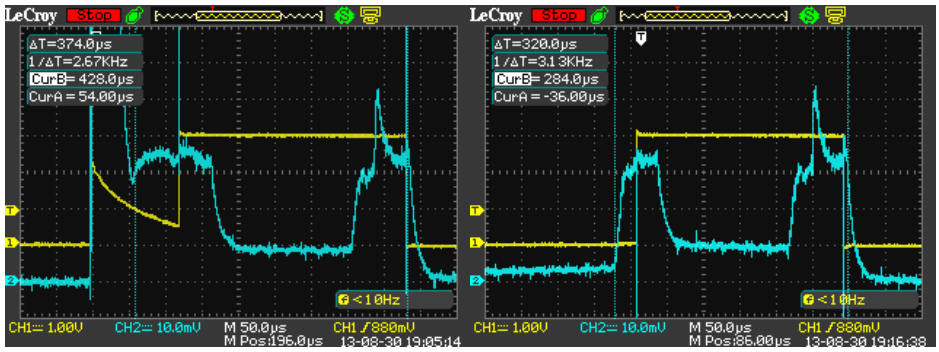


Fig. 4.26 Starting up and performing an ADC at 3V while executing Scenario 2 (left) and Scenario 1 (right)

Following the initial spike, the core is starting up and the code beginning execution begins on the rising edge of the yellow signal. After initialization has been completed the core goes into low power mode while waiting for the voltage reference to stabilize. After the stabilization of the reference was completed, the next spike in current consumption came from the AD conversion. Total energy consumption under different power supply voltage levels and different operating scenarios of ADC energy management are given in Fig. 4.27.

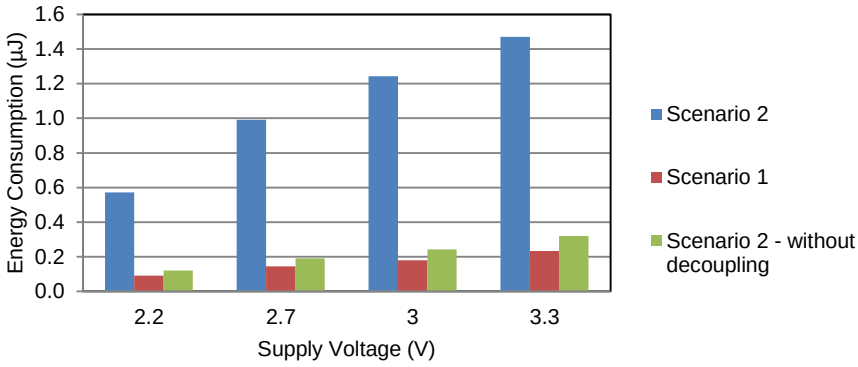


Fig. 4.27 Energy consumption of two operating scenarios when ran on various voltage levels. The impact of charging the decoupling capacitor when operating in second scenario is evident

4.2.3. Profiling of the EFM32TG222

In recent years manufacturers have started introducing 32-bit microcontrollers to the market of ultra-low power devices. With the advancement of VLSI it became possible to incorporate a 32-bit architecture

together with an extensive set of peripherals onto a single chip while keeping the low power consumption.

One of the lowest power consuming 32-bit Cortex M3 ARM microcontrollers was the Gecko series of microcontrollers from SiliconLabs (former EnergyMicro). One of the entry level microcontrollers has been selected for profiling. The EFM32TG222 [86] was selected as being one of the cheapest and smallest processors available at the time of testing. The TinyGecko series became available at the time of writing of the thesis. This series was aimed at selling at <1$/piece making it a direct competitor to cheap 8-bit and 16-bit MCUs.

Following the same procedure as done with the PIC and the MSP microcontrollers, this microcontroller was profiled for the power consumption in aspects required by the ADC based energy management.

Active and Sleep Power Consumption

The EFM32TG222 (EFM32 in the rest of the text) provides several low power modes of operation and the possibility to change the operating frequency. However, compared to the MPS430 and the PIC, the EFM32 is specifically designed to operate at higher frequencies. The default core frequency of the EFM32 is 14 MHz. The EFM32 is designed to perform tasks fast and spend the majority of the time in one of the low power modes. The current consumption of the core running on 14MHz is presented in Fig. 4.28.

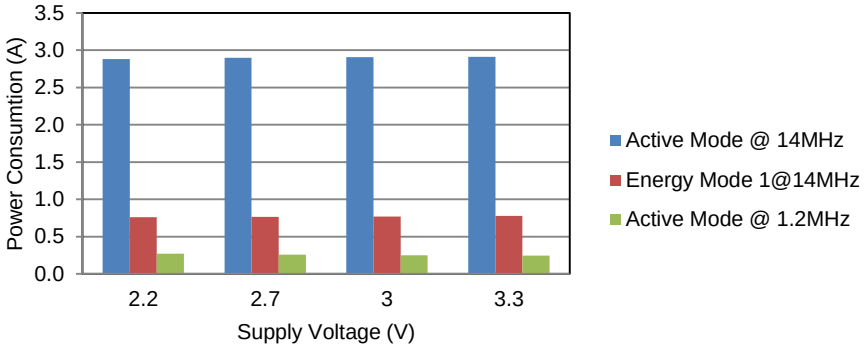


Fig. 4.28 Measured Current consumption of EFM32TG222 at different supply voltages

It should be noted that there is almost no variation in the supply current with the change of the supply voltage. It is interesting to note that in the Energy Mode 1 (EM1), the first low power, the core is unpowered but the peripherals are still running on the 14MHz clock. At this clock speed the MCU is consuming almost three times more current than the MCU executing code on 1.2MHz clock. This would mean that in case of a slow SPI communication it

would be beneficial to reduce the clock speed instead of going to EM1 while transmitting data.

The energy required for the transfer between different core frequencies is shown in Fig. 4.29. The frequencies used in the test have been specifically chosen. The initial frequency of the MCU is 14 MHz. The 11 MHz frequency allows for the most efficient AD conversion [87]. The 1.2 MHz frequency is the slowest operating frequency and will be used when communicating over long periods of time with peripherals that can't support SPI speeds over 1 MHz.

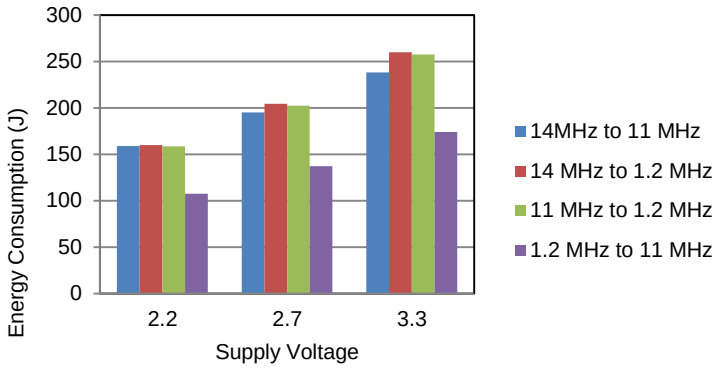


Fig. 4.29 Energy consumption required to perform core frequency switch on EFM32TG222

The EFM32TG222 supports several low power sleep modes. The lowest energy mode that supports RAM retention is referred to as Energy Mode 3 (EM3) and the current consumption in this mode is 590nA based on the information from the datasheet. In the lowest energy mode (Energy Mode 4) only some peripherals are operating and the current was measured to be an average of 15nA over the entire supply range. However, upon starting from this power mode the MCU goes through a reset procedure and all RAM data is lost. Therefore, this mode of operation resembles the second scenario for the ADC energy management and will be evaluated as such.

Analog to Digital Conversion: This MCU has been designed with a very versatile ADC in mind. The amount of features combined with up to 5V voltage tolerable inputs, high speed high precision internal voltage reference and a large variety of possible operation regimes makes it a good platform for sensing analogue signals. However, compared to two previous platforms, the AD converter doesn't have its own oscillator hence the peripheral clock can't be turned off. On the other hand, the AD converter on EFM32TG222 is 1Msps making it five times faster than the one on the MSP. The results of charge consumption requirements for performing a single AD conversion on different voltage levels and clock frequencies are shown in Fig. 4.30.

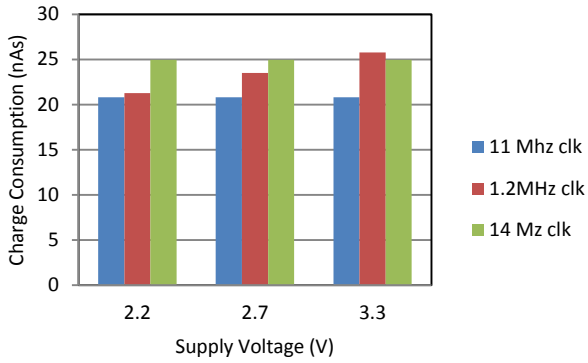


Fig. 4.30 The charge consumption of single AD conversion performed on different voltage levels and different clock speeds

The results of the single ADC measurement indicate that the most energy efficient operation is achieved when operating at 11MHz. However, operating on other two frequencies doesn't fall behind much in the energy consumption. In case of performing a single ADC there is no need to switch the operating frequency as the gain in energy consumption of 5nJ when operating on 11MHz instead of 14MHz is not justifying the cost of the 150nJ required to perform the switch of frequencies.

Serial Peripheral Interface

Similar to the other two platforms the EFM32TG222 is equipped with an SPI hardware module. This module is operating from the peripheral clock of the device therefore, the power consumption of the board can't be lowered further than the Energy Mode 1. As shown in the part about power consumption, it is more beneficial to reduce the clock frequency and perform the transfer of data than to spend time in low power EM1 on high frequency.

It should be noted here that the hardware of SPI was build assuming the first scenario, where the core is operating at high frequency and the peripheral is operating at low frequency. This is manifesting as the hardware module not being able to properly control the chip select on the SPI lines. This was observed as termination of the transmission even though there were more bytes to send, followed shortly by re-enabling the communication with the arrival of the next byte. This can result in bad framing of messages being sent to the peripheral, ultimately leading to communication errors.

The main difference of the EFM32 compared to the PIC and the MSP is the direct memory access (DMA) module available on the EFM32 allowing the microcontroller to perform memory transfers without activating the core of the microcontroller. The DMA is used in order to reduce the overall power

consumption when moving the data in the RAM. However, the cost of setting up the DMA on each start up makes its use limited. Fig. 4.31 demonstrates the power consumption for sending different amounts of data using SPI polling on one hand and the DMA transfer on the other. For data transfers longer than 30 bytes, the DMA approach becomes a more efficient way of data transfer. The measurements were done on 1.2 MHz clock frequency.

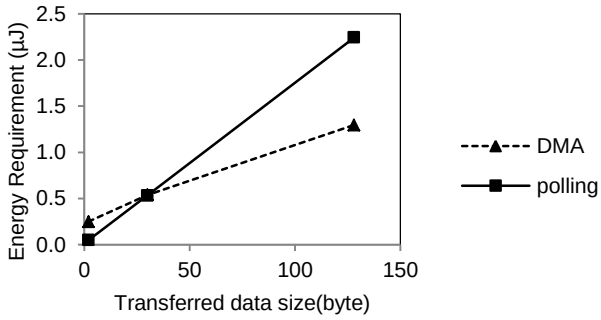


Fig. 4.31 The energy requirement for different packet sizes sent using DMA or polling for the end of transmission.

The results of experimental comparison of the different MCU operating frequencies and SPI communication methods are summarized in Fig 4.32. It can be clearly seen that use of low sending frequency is beneficial, however, depending on the length of the packet that needs to be sent, the penalty of switching frequencies might be higher than the gain in energy saved.

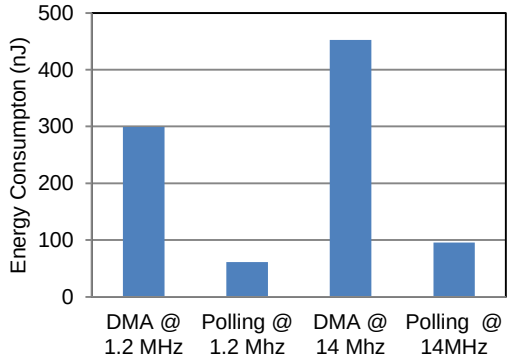


Fig. 4.32 Transmission of 2 bytes over SPI using different approaches at two main clock frequencies

Profiling the Energy Consumption for the two Operating Scenarios

The static power consumption of the EFM32TG222 while in RAM retention mode is five times higher than the other two platforms, therefore, Scenario 1 of the ADC energy management won't be evaluated for this platform. Two types of Scenario 2 regimes for EFM32TG222 will be evaluated. One where the core was being turned off and second, where the core was placed in Energy Mode 4 reducing its current consumption to 15nA. The results are summarized in Table 4.3

Table 4.3 Measured energy requirement for executing Scenario 2 under different conditions

Profile	*Voltage (V)*	*Energy (μJ)*
Scenario 2 from disabled power supply, 14MHz	3	11.0
Scenario 2 from Energy Mode 4, 14MHz	3	10.9
Scenario 2 from disabled power supply, 14MHz	2.2	5.94

From Table 4.3 it can be seen that both approaches to performing the Scenario 2 have similar energy requirements. This is coming from the fact that upon entering Energy Mode 4 the decoupling capacitor of the core connected to the microcontroller is being discharged. This means that every time the core needs to be activated, this 1μF capacitor needs to be charged resulting in an energy loss.

4.3. Modeling of ADC Energy Management

By combining all results obtained during the profiling of different microcontrollers it was possible to model the expected ADC energy management power consumption. After analyzing the modeling results a decision will be made on which MCU will be used for system implementation.

The model was built around the following assumptions: there is no impact to the energy consumption from other elements of the system, the supply voltage is at stable 2.2 V, and the loss in decoupling capacitors is neglected. The RTC's power consumption during SPI communication was neglected as it is much smaller compared to MCU power consumption.

The model is aimed at demonstrating the average power consumption for different operating scenarios of ADC energy management. The power consumption is going to be mainly driven by the static power consumption in low power modes and the period between performing two consecutive AD conversions. For the Scenario 1 the formula used to calculate the average power consumption is:

$$P_{S1}(T_{WAIT}) = P_{RTC} + P_{MCU\_SLEEP} + \frac{E_{WAS}}{T_{WAIT}} \quad (4.3)$$

where P_{S1} is the average sleep power consumption, P_{RTC} is the average power consumption of the RTC and T_{WAIT} is the period between two measurements. The P_{MCU_SLEEP} is the power consumption of the microcontroller in sleep while retaining the RAM. The E_{WAS} is the measured value of energy required to perform the staring up from the low power mode, performing the AD conversion, processing the result and placing the MCU back to low power mode.

In case of Scenario 2 the formula for average power consumption is similar to (4.3):

$$P_{S2}(T_{WAIT}) = P_{RTC} + \frac{E_{SAS}}{T_{WAIT}} \quad (4.4)$$

where E_{SAS} element corresponds to the energy required to perform the powering up of the microcontroller, performing the AD conversion, processing the result and disabling the MCU.

Both P_{S1} and P_{S2} are dependent on the sleeping interval as other two parameters are constant for given microcontroller implementation. The PIC and the MSP microcontrollers had both Scenario 1 and Scenario 2 modeled, while the EFM32 had only Scenario 2 modeled due to much higher RAM data retention current consumption compared to other two MCUs.

As a comparison to the ADC energy management, an energy management implementation consisting of an operational amplifier with a reconfigurable resistor network was modeled. By using a reconfigurable resistor network, a voltage comparator with multiple thresholds can be implemented. In this approach, by attaching and detaching resistors connected to one of the input pins of the operation amplifier, it is possible to select the threshold voltage at which the output of the operational amplifier would change its value. Other input pin of the operational amplifier is connected to a voltage reference. For modeling purposes the power consumption of the resistor network was neglected. The power consumption of the circuits providing signal to MOSFETs used for selecting the voltage level was neglected as well. The only contributor to the power consumption of such a circuit was the operational amplifier. The power consumption of the comparator based approaches has been modeled very close to ideal in order to stress out the potential savings introduced by the proposed ADC energy management. The lowest power comparators available on the market at the time of writing of the

thesis were the NPS1101 from NanoPower Solutions and LTC1540 from Linear Technology.

The result of the modeling of the Scenario 1 and the Scenario 2 at 2.2 V supply voltage for all platforms, together with the power consumption of the reference comparators, is demonstrated in Fig. 4.33.

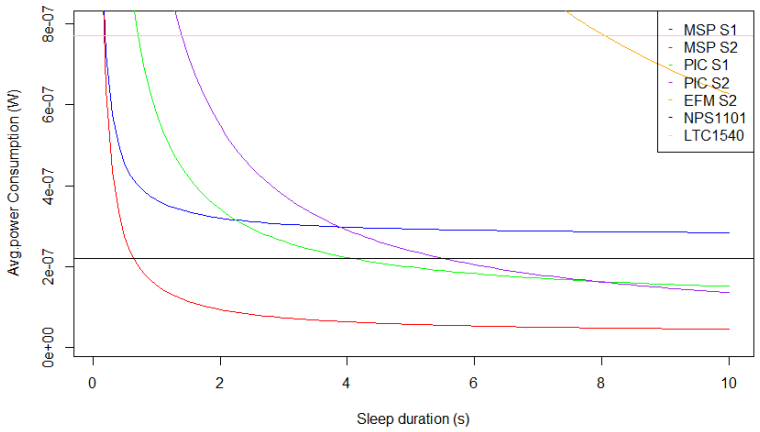


Fig. 4.33 The result of modeling expected power consumption under different scenarios at 2.2 V

The result from the modeling suggests that the MSP430 implementation of the ADC energy management required only half of the power of NPS1101 implementation with interval of 2s between two AD conversions. It should be stressed that this energy saving has been achieved even with all the assumptions for the NPS1101 bases circuit. It can be also seen that with extension of sleep duration the average power consumption of the MSP implementation is slowly reducing. From the result of modeling, delays longer than 5s provide only marginal gain in power reduction.

The power consumption of the EFM32 is significantly larger than the other two platforms and will not be looked into any further.

The power consumption of the Scenario 1 using the MSP never becomes more efficient than by using analogue circuitry. Therefore, in case of the MSP, it should be used primarily in the Scenario 2 in order to gain power savings. However, this approach has a shortcoming in that it requires disabling the MCU power supply hence losing all stored data. On the other hand, PIC's low current with RAM retention allows the PIC to maintain the RAM making the Scenario 1 a viable option for short sleep durations. This advantage is particularly beneficial in the case where keeping track of the harvester output is of interest as the MCU has to keep the data from the previous measurement.

In order to compensate the loss of data during the power cycle, the MSP has to store the data outside the MCU.

The fastest way to store and retrieve data would be through parallel interface to a non-volatile memory, for example, the parallel low power FRAM. One more option is storing the data inside the RTC's RAM using serial communication lines.

In order to compare the MSP's Scenario 2 with the PIC's Scenario 1 operation, the Scenario 2 model for MSP was extended to include SPI communication overhead. According to the measurements done for the MSP, a model of energy required to transfer data over SPI was built. The energy consumption was approximated with the following linear function:

$$E_{SPI} = Nk + E_{SPI\_OFFSET} \tag{4.5}$$

where k is the slope of the linear function and was calculated to be 14.71nJ/byte while the E_{SPI_OFFSET} is the fixed overhead of the communication and was calculated to be 8.57nJ, N represents the number of bytes that are transmitted over SPI. The supply voltage was 2.2V.

The new Scenario 2 model is given with the formula:

$$P_{S2}(T_{WAIT}) = P_{RTC} + \frac{E_{SAS} + E_{SPI}}{T_{WAIT}} \tag{4.6}$$

Using the modified Scenario 2 power consumption formula for the MSP power consumption, a new comparison was made to PIC's Scenario 1 operation. The result is shown in Fig. 4.34.

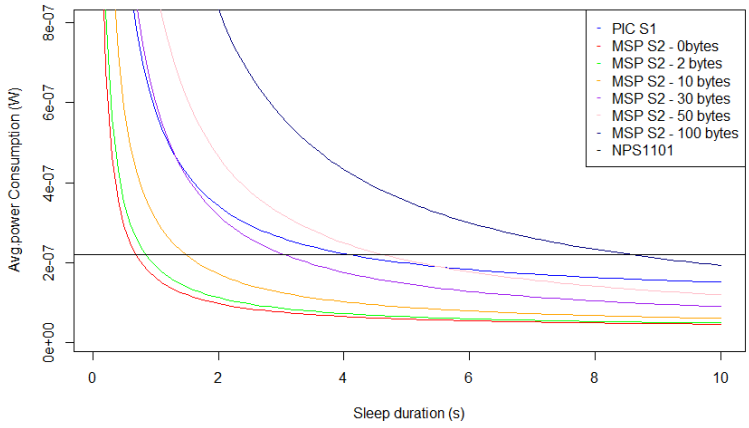


Fig. 4.34 The comparison of storing various amounts of data in external memory while operating the MSP430 in Scenario 2, to power consumption of PIC in Scenario 1 with varying amount of data stored

According to the modeling results, the average power consumption of storing up to 50 bytes in the external memory is comparable to the PIC running in Scenario 1. The results suggest that even transferring 100 bytes of data on every startup was more power efficient than using an analogue approach for sleep intervals longer than 10s.

In the case of the applications where the output power from the harvester is varying in nanowatt range, it would be beneficial to adjust the time intervals between two measurements of the buffer voltage in order to save power. However, adjusting the time interval requires calculation based on a previously measured point hence introducing the need for recovering the measurement data from the RTC RAM and processing the data. The behavior of the system under these circumstances has been modeled.

When building the model, I assumed the simplest scenario where the power generated by the harvester is assessed based on the previous measurement point and current data point. The calculation for next measurement moment was done under the assumption that the time interval between two measurements was short enough to assume the output of the harvester, although varying, can be considered constant. Based on this assumption, the following formula was used for calculating the next wake up time:

$$T_{NEXT} = \frac{T_{OLD}(V_{END} - V_{CURRENT})}{\alpha(V_{CURREN} - V_{START})} \tag{4.7}$$

where T_{NEXT} is calculated duration for the next sleep period, V_{END} is the projected voltage the buffer should reach during the next sleeping period, $V_{CURRENT}$ is the current voltage and V_{START} is the voltage of the previous measurement. The factor α is introduced to accommodate for the varying harvester output. As previously mentioned this formula holds true only if the charging current between two measurement points can be considered constant. The time interval for the next measurement calculated using this formula could potentially be too long for this premises to hold. Therefore, it is necessary to reduce the interval of waiting between two measurements. The factor α can be preprogrammed based on the expected behavior of the output energy of the harvesting source.

The average time required for the MCU to calculate the delay between measurements using the formula (4.7) has been simulated to be 280µs. Using the simulated results the energy consumption for the calculation totaled to 147 nJ under the assumption of 2.2V supply voltage and 238 µA supply current required by the MCU.

In order to perform the calculation for the sleeping interval it is necessary to read the data of the previous measurement. For modeling

purposes I have assumed that the data is available in the RAM of RTC. In order to retrieve the previous measurement point, based on the datasheet of the RTC, the reading procedure requires 4 bytes to be transferred over the SPI. Two of these 4 bytes were the address and command to the RTC and two bytes were required to read out the 10-bit measurement value stored in two consecutive bytes. Using the results from the profiling section the required energy for performing this task was 78 nJ. In total the energy requirement for calculating the sleeping interval was 225 nJ.

In conclusion, the amount of energy required to perform the calculation of the next sleep interval was determined to be larger than the measured energy consumption of the entire Scenario 2 operation. This indicates that if the sleeping interval estimation can save at least one starting up it would be advantageous to adjust the sleeping period.

However, the gain in the power consumption reduction has its limits. The power consumption of the RTC running for intervals longer than 100s becomes the dominant factor in the average power consumption. As a result the potential saving in power consumption for sleeping periods longer than 100s are marginal. This is shown in Fig. 4.35.

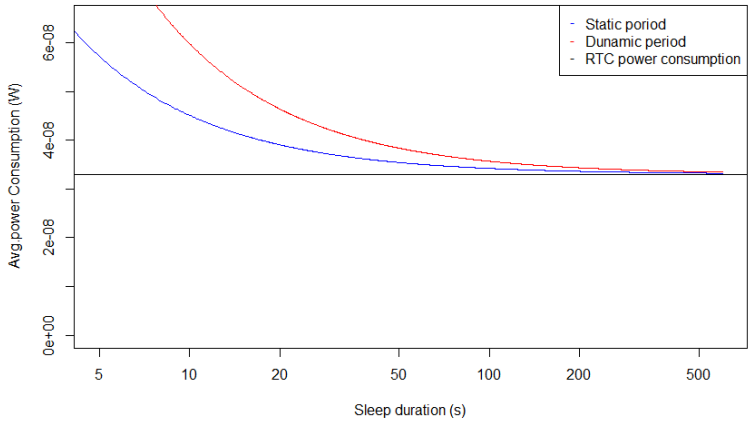


Fig. 4.35 The average power consumption as a function of delay between AD conversions of the approach with static interval between measurements, dynamic period that is changed to accommodate the change of input power and the RTC power consumption

In conclusion, it can be said that the estimation of the sleeping period in the proposed implementation is beneficial if the periods between activations are estimated to be shorter than 100s based on the expected energy harvesting output in the application environment.

After evaluating the results of different MCU performance under both operating scenarios of ADC energy management, it was decided to implement the system based around the MSP430G2553 MCU. The following section will address in detail the implementation of the system.

4.4. Implementation

The implementation section will first focus on meeting the assumptions used in modeling in order to keep the average power consumption of the system as close as possible to the modeled version. The main focus will be on removing the energy loss due to charging and discharging of the decoupling capacitors. Next, the explanation of the need for a specialized power supply control block for the MCU is presented. This is followed by the theory of operation of the entire circuit. In the end, the software algorithm running on the MCU is presented.

4.4.1. Minimizing Decoupling Capacitor Energy Loss

In the modeling section the energy required for charging the MCU's decoupling capacitor during the powering up has been ignored. This, however, can't be done when the system is implemented due to excessive noise that would be inserted into the power supply lines by the core of the MCU if the decoupling was to be removed.

The energy required to charge the 100 nF capacitor in case of the Scenario 2 is significant when compared to the energy required by the MSP to perform all the tasks required by the Scenario 2. It was measured that the power consumption of the Scenario 2 was 120nJ at 2.2, on the other hand charging a 100 nF capacitor to the same voltage through a MOSFET would require 484 nJ. This means that the process of charging the decoupling capacitor will consume four times more energy than was used by the MCU to perform all the tasks required by the Scenario 2.

The proposed solution for reducing the impact of the decoupling capacitors is to divide the decoupling capacitor into two stages. The second stage is a 1nF capacitor placed as close as possible to the MCU supply pins. The first stage is a larger 100 nF capacitor connected to the supply of the electronics controlling the activation of the MOSFET. The schematic representation is given in Fig. 4.36.

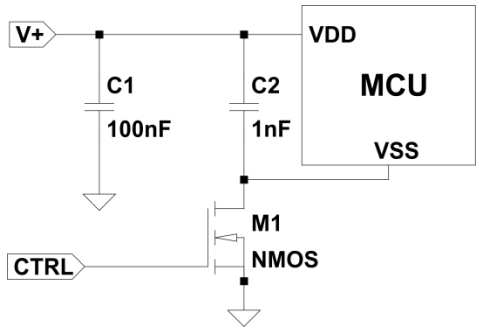


Fig. 4.36 Removing the influence of energy loss on decoupling capacitor on each MCU power cycle

The input voltage, V+, is present all the time and is equal to the supply voltage the MCU is going to be powered with. When the CTRL line activates the supply to the MCU by connecting the ground of the MCU to the circuit ground, only the 1nF capacitor will be charged.

It should be noted that when implementing this approach, the placement of the MOSFET and the first and the second stage capacitors is critical. Therefore, when routing and placing components, special care should be taken in order to maintain the decoupling functionality. If the two stages are electrically far apart or, in other words, there is a long trace between them, the C1 capacitor would not be able to provide proper decoupling.

4.4.2. The Power Supply Control of the MCU

The RTC used for the time keeping in this application comes with an integrated switch that can be used to control the power supply of the MCU or any other load attached to it. The internal controlling circuitry of the RTC can be set to power off the load for a set amount of time. When the set time elapses the power is restored to the load. In this way, the power consumption during sleep is equal to the power consumption of the RTC. An example implementation of such a system is shown in Fig. 4.37.

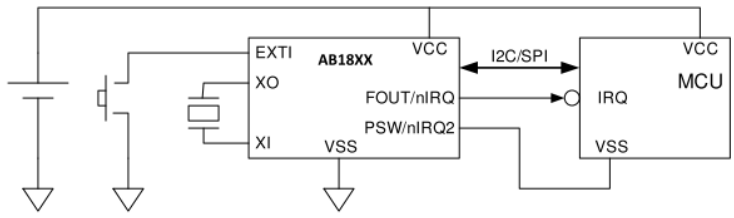


Fig. 4.37 An example of typical implementation of an AB1814 RTC as a power management circuit [63]

The hardware support for activation and deactivation of the attached MCU makes this RTC a very convenient choice for implementing the Scenario 2 of ADC energy management. However, it has two drawbacks:

- Every time the MCU is started the new wake up time needs to be programmed to the RTC and the sleep process needs to be reactivated. This would require SPI communication between the RTC and the MCU to take place, thus increasing the power consumption;
- The implemented switch feature would limit the implementation to this specific RTC not making it a more general approach.

The majority of currently available RTCs have an interrupt pin that is available for signaling the expiration of the sleep interval, therefore, it was beneficial if a circuitry had been built that would support both operating scenarios (Scenario 1 and Scenario 2) using only the change on the signal pin of the RTC. This would also reduce the required SPI communication between the RTC and the MCU as the RTC will continue to produce an output at a given frequency and wake up the MCU again on the next interval.

The circuit proposed in this section was designed to be able to support both the Scenario 1 and the Scenario 2 mode of operation while introducing minimal power consumption overhead. The schematic of the control circuit for enabling the power to the MCU is given in Fig. 4.38.

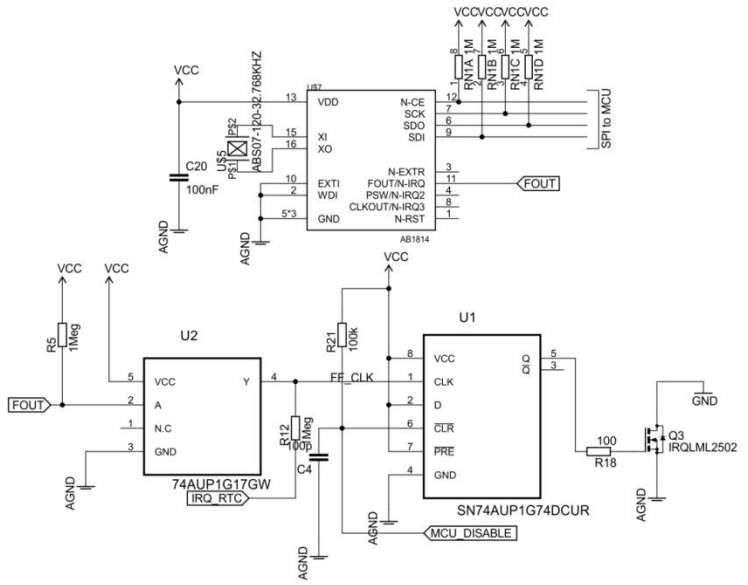


Fig. 4.38 The schematic for control of the power supply of the MCU

The U2 is a buffer with Schmitt trigger input that is used to provide a proper rising edge for driving the clock line of a D type Flip-Flop as the interrupt line from the RTC is an open collector and its rising time will be defined by the resistor R5. The operation of this part of the circuit will be explained in conjunction with the rest of the circuit in the following section.

4.5. The Circuit Operation

The circuit operation can be divided into two stages: The first stage is powering up stage, when the supply is applied for the first time to the circuit. The second stage is the operating stage, where the circuit is activating the MCU depending on the predefined mode of operation. The software algorithm of the MCU is shown in Fig. 4.39 .

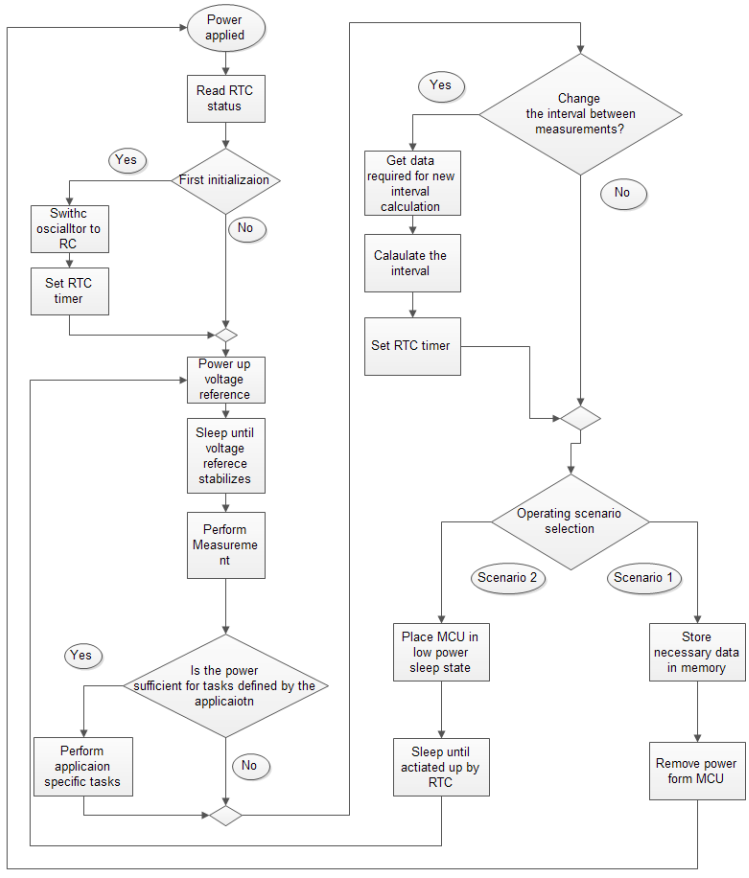


Fig. 4.39 The software algorithm used in the MCU

The operation of the circuit will be described using an operation cycle from powering up until the system starts performing timed AD conversions.

During the initial powering of the circuit the RTC requires 300ms delay before it becomes operational. During this time the interrupt line is on low logic level. This logic level is transmitted through the buffer and keeps the clock line of the D type flip-flop on the low logic level. A low pass filter consisting of R21 and C4 is introducing a sufficient delay on the clear pin of the flip-flop providing a reset mechanic. As the flip-flop is reset the output is on low logic level hence the Q3 is not conducting. The transistor Q3 is connecting the ground of the supply to the ground of the MCU and the rest of the load. In this way the MCU is kept disabled until there is a change on the output of the flip-flop.

While disabled, due to the fact that there is no ground connection on MCU, all electronics connected to the MCU will be on the supply potential. This feature is used to stabilize the MCU_DISABLE line as there is a connection between supply and the MCU pin through the R21. Similarly the resistors on the SPI communication lines prevent the lines from floating when the MCU is disabled. However, during the starting up there is a conduction path between the MCU and the output of the buffer, the IRQ_RTC line. This line is directly connected to an input-output pin of the MCU. This allows the current to flow through the MCU supply pin, then through the protection diode connected inside the microcontroller between the pin and the supply. This in turn allows the circuit to get closed through the R12 and the output of the buffer U2 that is connected to the ground. The resistor R12 is chosen to be 10MΩ in order to minimize the current going through it.

The main reason why low side switching[2] of the load was used was the fact that the SPI communication lines are idle when CS is on high voltage. Furthermore the flip-flop asynchronous reset is also active low. Therefore, in order to avoid any additional circuitry by disconnecting the ground of the MCU, the pins could be connected to the supply voltage through a resistor without any energy loss during inactive periods. The use of low side switching will also allow the use of I^2C communication bus as the bus, when idle, has its line connected to the supply potential. This opens up opportunities to use the RTCs that do not support the SPI interface.

After the 300ms delay required by the RTC to start up, the state of the FOUT line changes to logic one which produces, through the buffer, a rising edge on the clock line of the flip-flop. With the rising edge the logic level on the input of the flip-flop, which is connected to the supply voltage, gets propagated to flip-flops output activating the NMOS transistor. The activation

[2] Disconnecting the power by disconnecting the ground pin of the device from the circuit ground pin

of the transistor closes the circuit of the load, thus activating the MCU and other connected circuits.

After the MCU has been powered up it is necessary to determine if this was the initial powering up after the supply has been applied for the first time to the RTC. If this was the case, it is necessary to set up the RTC through setting the oscillator and the interval between measurements. The MCU is determining if the initial startup has occurred by reading the status byte from RTC. If the RTC is running on internal RC oscillator this is an indication that the setup has been already performed.

Following evaluation if the initial power up of the system has occurred, the MCU can perform tasks required by the application and then set the interval at which the measurements of the supply should be taken. Depending on the application and energy harvester attached to the supply, this interval can vary. The interval length will be discussed in the discussion section later in this chapter. After setting the wake up interval, based on the application requirements, the MCU begins operation under the Scenario 1 or the Scenario 2 depending on the application. Both Scenarios will be described in detail.

In the case of Scenario 1 the MCU sets an input pin to be the interrupt pin and goes into low power mode. This interrupt pin is connected to the RTC_IRQ line. When the timer inside the RTC expires, the RTC will send a short pulse to the RTC_IRQ line through the buffer U2. On the rising edge of the RTC_IRQ the processor starts up and continues execution. In the meantime the rising edge of the RTC_IRQ also activates the flip-flop. However, as the output of the flip-flop is already on logic one, there are no changes.

In the case of Scenario 2, the MCU sends a short low logic level pulse on MCU_DISABLE pin. This short pulse will trigger an asynchronous reset of the flip-flop disabling the Q3 and hence disconnecting the power to the MCU and the load. Now the circuit is in the lowest power state where the only power consumed is coming from the RTC and the two logic circuits totaling to around 20nA depending on the supply voltage. After the timer inside the RTC expires, a short pulse is sent through the buffer to the clock line of the flip-flop. The flip-flop was previously reset by the MCU so its output was on low logic level. With the arrival of the pulse on the clock line, the state of the input of the flip flop, which is connected to logic one, will be propagated to its output, thus activating the Q3 transistor leading to powering up the MCU.

The software algorithm implemented in the MCU in order to perform the ADC energy management operation is depicted in an algorithm in Fig. 4.39.

4.6. Startup Power Losses

During the startup procedure of the MCU, between the powering up and the start of the execution of the software the boot section of software is being run. During this period the MCU resets followed by the global variable initialization to zero. Although this time is in order of a fraction of a millisecond, during this time the I/O pins on the microcontroller are set to high impedance, which can increase the energy consumption during startup as these pins can be connected to other high impedance inputs. In Fig. 4.40 the difference between the MCU powering up with and without the pull up resistor on the serial output line of the RTC is shown.

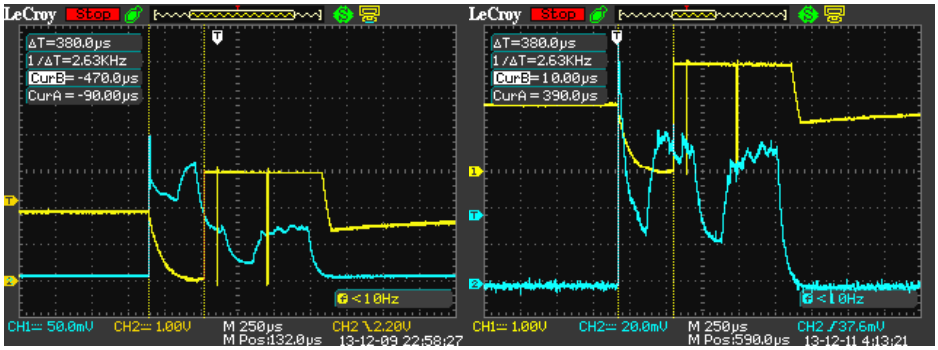


Fig. 4.40 The impact of floating communication pin during initialization of the MCU. The current consumption (blue) on the left picture is with the pin not connected to the supply with the resistor, while on the right it is connected. The yellow signal line indicated different stages of MCU operation.

In Fig. 4.40 the initialization phase was highlighted using the vertical bars. The total duration of the startup stage was 380 µs. The total energy consumed during powering up with the serial communication line left floating was 629 nJ more than the implementation with the line connected with a resistor to the supply voltage. The total power consumption with the pin connected was measured to be 412 nJ. As a conclusion, leaving the pin floating, even for such a short period, before the MCU starts, has increased the total energy requirement for performing the startup 152%.

The next section will focus on measurements of the actual energy requirements of the ADC energy management implemented using the components and processes described in this section.

4.6.1. Measurements

The system was realized on a PCB together with a radio module attached. Attaching of radio modules was done in order to provide the

implementation that is close to a typical wireless sensor node application. The entire sensor node operation using this energy management in an application is described in Chapter 5.

The most critical characteristic of the implemented system is the average current consumption. However, due to expected long times between the MCU operations measuring, the average current consumption was challenging, and therefore, the power consumption was calculated using the same formulas used when modeling.

First, the measurement of the average energy consumption for two ADC energy management scenarios on different supply levels has been performed. The results are shown in the Fig. 4.41.

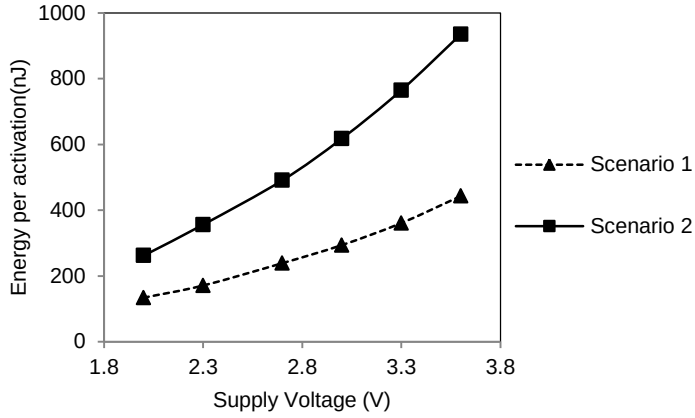


Fig. 4.41 The energy consumption per single buffer voltage evaluation at different supply levels

It can be seen that on 2.3 V the measured energy consumption during Scenario 1 operation of the entire circuit is 171 nJ, while the modeled energy consumption was 90 nJ. The increase of the power consumption is coming from the added complexity of the circuit, additional processing done by the MCU and the leakage currents. In case of Scenario 2 the additional increase of energy consumption is coming from the added SPI communication compared to the modeled system. Here the difference is 356 nJ compared to 121 nJ that was modeled. Further work on optimizing the circuit will reduce the energy required for operation under both Scenario 1 and Scenario 2.

The average power consumption as a function of the sleep interval is calculated and shown in Fig. 4.42. The calculations were based on the

measured results for the energy consumption of the realized ADC energy management during operation in the Scenario 1 and the Scenario 2. From Fig. 4.42 it can be seen that even without a highly optimized circuit, it was possible to realize the energy managing system that has lower average power consumption than using a state of the art operational amplifier approach even for sleep periods as short as several seconds.

The final measurements done are addressing the energy requirement for the ADC energy management circuit to start. This is an important factor as the buffer storage has to be large enough to store sufficient energy for the activation of the ADC energy management. This energy can, in some applications, be larger than the energy requirement for the tasks the application has to perform. The energy required to activate the entire energy management block, as the function of voltage, is given in Fig. 4.43.

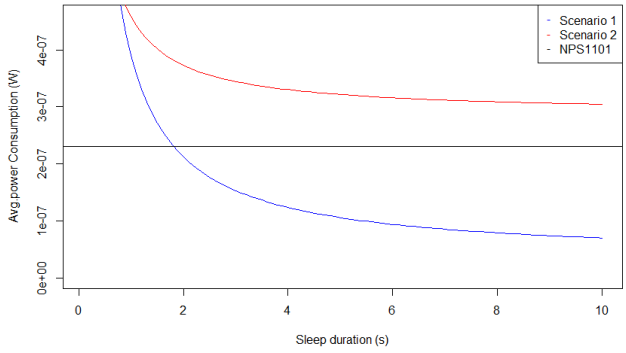


Fig. 4.42 The average power consumption as the function of the interval between the AD conversions on 2.2 V

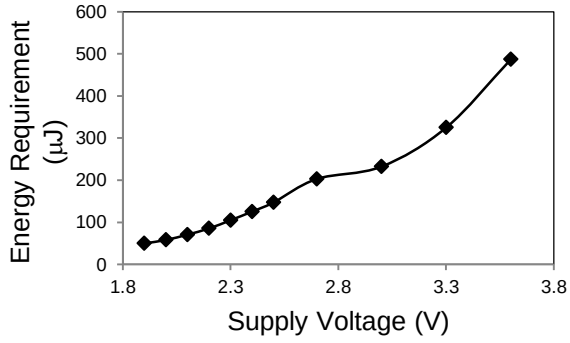


Fig. 4.43 The energy requirement for starting the ADC energy management stage

The largest contributor to the startup energy consumption is the RTC. It can be seen that with the increase of the input voltage, the current consumption of the RTC rises fast, therefore, the ADC energy management should be initially started at the lowest possible voltage level. This will be discussed in more detail in the first case study in the Chapter 5.

4.7. Discussion

The proposed approach has demonstrated a great potential for reducing the energy management power consumption while increasing the flexibility of the system as the threshold voltages can be adapted based on the system's needs. Furthermore the entire system is realized using commercially available off the shelf components.

An advantage of the ADC energy management lies in the higher immunity to the environmental impacts such as temperature and humidity. The environmental impact hasn't been tested before the writing of the dissertation; however, the following argument can be made: in case of ADC energy management the only active element during the sleeping period is the RTC, hence all the critical current paths are located inside the integrated chip. This is protecting the sensitive circuitry from the impacts of humidity and pollution. On the other hand, in the case of an approach where operational amplifier is used, the critical current paths are located mostly outside integrated circuits. This means that the critical paths are spread out on a significantly larger area of the PCB compared to the ADC energy management approach. The signal paths are going through high value resistors, tens or hundreds of megaohms or even gigaohms. The high value resistors are susceptible to humidity and possible pollutions from the environment [73]. It is also known that the high impedance inputs of operational amplifiers are prone to picking up the noise from the environment. All these shortcomings can be avoided by implementing the ADC energy management approach.

In case of temperature fluctuations the RTC interval oscillator will drift, however, that can be adjusted in the software by simply adjusting the wake up interval to compensate for the temperature drift. In case of operational amplifiers, the impact of temperature can be also compensated, however, compensation requires use of external circuitry. Furthermore, the compensation has to be determined based on the environmental conditions expected and implemented during the circuit design stage. On the other hand, the ADC energy management could potentially adapt when deployed, hence allowing a more robust system.

One more major advantage of the ADC energy management is that the evaluation of the amount of energy stored in the buffer storage is performed by the MCU and not by the peripheral module. As the information of the buffer management is readily available, this can be used as an additional input

parameter to the algorithm providing the task management for the system. In this way a more efficient task management could be potentially realized, hence increasing the utilization of the collected energy.

The drawback of this approach is its limitation to microwatt and nanowatt energy harvesting sources. The proposed energy management is aimed at applications with delays between active states that are measured in tens of seconds, minutes or longer. In the case of applications where the monitoring of the buffer storage capacitor should be performed every second or more often, the conventional approach using the operational amplifier would be more energy efficient.

Another potential drawback of this approach is the potential overshot that might occur if the interval between two consecutive buffer storage measurements is not set accurately. If there is a significant change in the charging current during the interval between measurements, the buffer storage capacitor might get charged over the minimum energy amount required for the task, hence introducing the delay in performing the task. This issue is, to some extent, addressed by α factor in formula (4.7) used for calculating the expected duration between the measurements.

Further limitation of the circuit is that it has increased power consumption under 1.2V, hence preventing nanowatt operation when the ADC energy management is coupled with a capacitor in a circuit that is supposed to start operation with the capacitor empty. This limitation was addressed by combining the ADC energy management with the Nanowatt Voltage Detector described in Section 4.2. Implementation of an energy management consisting of both of these circuits is demonstrated in Chapter 5.

4.8. Future Work

The future work on this circuit will be focused on removing the losses in the ADC energy management and further optimization of both hardware and software. One of optimizations is removing the leakage current going through the resistor that is connecting the MCU to the RTC interrupt line. This can be done by introducing an additional buffer stage between them.

The optimizations of the sleeping period are subject to future work in this field. The calculation of the next sleeping interval could include, beside the change in the measured voltage, the difference between the voltage measured and the expected voltage level after the sleeping interval expires. By comparing these two values it is possible to determine if the averaged input current is changing from one delay interval to the other, hence allowing for a more advanced sleeping time prediction. Such an algorithm is the subject of the future work.

One more topic for further work is introducing this approach as an enhancement to the task scheduling algorithms, hence potentially improving the efficiency of the task management.

4.9. Summary

This section has demonstrated a novel approach to implementing an energy management system using commercially available off-the-shelf components. The proposed approach is aimed at nanowatt and microwatt power sources. It is based on the fact that monitoring the buffer storage using a series of an analogue to digital conversions inside the MCU is more power efficient than continuous monitoring of buffer using even the most power efficient commercially available operational amplifiers and comparators. This approach has a great potential of increasing the efficiency of utilization of the nanowatt and microwatt power sources by allowing a more flexible energy management system compared to energy management systems that have only one hardware fixed threshold voltage.

5. Conclusions

This chapter has presented some novel concepts in utilizing off the shelf components for design and implementation of ultra-low power circuits. A nanowatt energy management circuit with a fixed threshold was presented. This Nanowatt Voltage Detector could be potentially used with power sources that have the output impedance in order of gigaohms.

Beside the NVD circuit, a novel approach for reducing the overall power consumption has been presented. This approach is based on sampling the storage buffer periodically instead of continuously monitoring the voltage level on it. This allowed for removal of operational amplifiers and comparators from the circuit and moving all energy management related tasks into the microcontroller. This, in turn, allowed increased flexibility of the energy management while reducing the overall power consumption.

Throughout the chapter, additional techniques for reducing the power consumption of microcontroller systems have been presented together with in depth analysis of three different microcontrollers that are used in energy harvesting systems.

Chapter 5

Design of EH-WSN nodes

1. Introduction

The energy harvesting powered applications, in order to operate, need to achieve energy neutrality. In other words, the amount of power required by the application has to be less or equal to the power generated by the energy harvester. Only then the application can, in theory, achieve the perpetual operation. However, due to low energy generating potential of energy harvester generators, in order of microwatts and milliwatts, sometimes even nanowatts, achieving the energy neutrality in energy harvesting powered applications can pose a significant challenge.

In the case of wireless sensor nodes, that are the main objective of this thesis, the main challenge lies in implementing "energy aware" operation of all elements of the system. This means that every aspect of the hardware and the software on the node has to take into account the energy level that is on the node's disposal and incorporate the fact that the energy will be replenished in time. The energy aware operation adds a new layer of complexity compared to battery powered systems, where the average power consumption was the most

important parameter and the main objective was to extend the lifetime of the battery as much as possible.

The fact that the energy levels are being replenished in time adds a requirement for a more advanced power and energy management systems as well. The energy collected from the energy harvesting source needs to be stored until a sufficient level has been reached. The storing process needs to be performed as efficient as possible in order to leave the majority of the collected energy for performing the application related tasks. Efficient storing of energy with low losses is challenging in ultra-low power systems. For example, an 80% efficient energy management circuit, when operated at the power level of 100 µW, has only 20 µW on its disposal to power its control circuitry and incorporate all of component losses and the leakage currents. As a comparison a 100 kΩ resistor, the resistance value that is typically used to prevent high impedance lines from having undetermined voltage levels, will dissipate as heat 90µW of power when 3V are applied to it. It should be noted that in most conventional systems the power consumption of these resistors is not even considered, and yet in an energy harvesting system the total available power for the entire system's operation is in that order of magnitude.

An additional research challenge is placed here: to design and implement the power management and energy management using only off-the-shelf components. Achieving nanowatt power consumption can be achieved using specially designed integrated circuits. However, manufacturing of these circuits is costly and takes time. By being able to come close to the power consumption of these circuits for specific applications, using off the shelf components, allows easy implementation of the required circuitry and hence the entire energy harvesting powered wireless sensor node.

The added layer of complexity in the design originating from the need for the energy aware operation, and highly efficient energy management, is making the already not trivial task of designing a low power wireless sensor node, even more challenging. Therefore, a need for a methodology arises that will address the issue of how to design an energy harvesting powered wireless sensor node using off the shelf components that will meet the energy constrains imposed by the harvester while fulfilling the application requirements. The objective of this chapter is to propose a methodology that can provide a basic framework required for successful design and implementation of a wireless sensor node.

The approach is presented on a high abstraction level and it doesn't provide detailed implementation methods due to the high complexity of the EH-WSN node implementation task as EH-WSNs are very application specific. The methodology is presenting general questions and guidelines that could be used when designing the EH-WSN node. The methodology proposes a set of steps that would guide the system designer through the design and

implementation of the different elements of EH-WSN node allowing easier navigation through the design space where elements are typically tightly interconnected.

Two case studies are used to show how following the proposed methodology guides and questions can lead to implementing an EH powered node. The two case studies are presented in the following order: first, an ultra-low power platform is presented followed by the low light level energy harvesting application. After the second case study on occupancy detection is presented. This case study is broken into two parts as it was a two stage project. In the end the summary of the chapter is presented

The first case study was aimed at ultra-low power energy harvesting power sources with the power output in the range of 1 µW. In this case study a wireless sensor node platform was developed that operated on the required power level. The target application was a solar powered batteryless environmental monitoring system intended for the indoor use in 10-30 lux conditions. The second case study was aimed at an occupancy detection applications used for a building automation application.

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2. Designing an Energy Harvesting Powered Node

The sensing applications are driven by the need to acquire data about a process or an event. This data can be used for obtaining a better understanding of the environment, process or a system and its properties. A wireless sensor network is a good candidate for this task as explained in Chapter 2. When desiring the wireless sensor network the first element that is designed is the wireless node of the network. The node performs the measurements and forwards the data to a collection point. As the node needs to be deployed for extended periods of time powering it using energy harvesting can enable long lifetime of the sensor node. A typical energy harvested powered wireless sensor node consists of 5 blocks:

- The energy harvester
- The power management stage
- The energy management stage
- The control block
- The sensor
- The communication block

In order to design the EH-WSN node every block needs to be addressed. The flexibility of individual block design process is going to be determined by the applications requirements. In some applications not all blocks are going to be present, while in the other the same component might perform multiple

functions. Furthermore, these blocks are typically tightly interconnected leading to a challenging task of selecting in which order these blocks should be addressed and which aspects of the blocks should be addressed first. Therefore a methodology was designed that would guide the implementation engineer through the process of designing the blocks.

The methodology is built around an iterative process during which the energy harvester's power output is matched to the power consumption of the rest of the circuit. The design flow is depicted in Fig. 5.1.

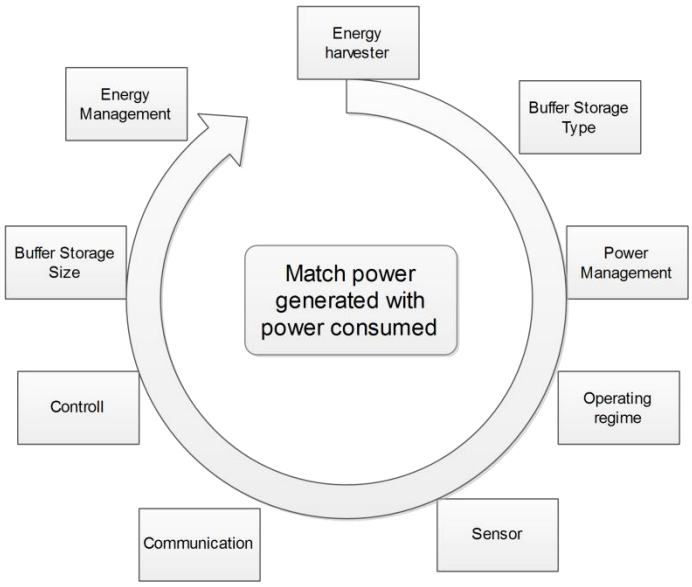

Fig. 5.1 Design flow of an energy harvesting powered system

By analyzing Fig. 5.1 it can be seen that there are a lot of different segments of the circuit that need to be addressed, furthermore it should be noted that all these blocks are going to be using the same energy storage and often the operation of one block is going to depend on the operation of other. This interconnection of the blocks is the main reason why the design process is iterative. It is necessary to verify that a change in one block will not jeopardize the system's overall operation.

The implementation of these blocks is mainly going to be driven by the application requirements. The application requirements will influence the complexity of individual blocks, components used and the targeted efficiency.

The design process starts from the selection of the type of the energy source that is going to be used for powering the electronics and choosing an appropriate energy transducer technology for the selected energy source. Following this the storage type is selected. It should be noted that only the

targeted type of storage is selected, not its parameters such as the storage capability, operating conditions etc. Selection of the type of the storage will have a major role on the selection of the power management block. After selecting a power management circuit it is necessary to determine the operating regime of the node. The possible operating regimes of nodes will be addressed in more detail in a separate section. Following is the selection of sensors, control units and communication method for the node. Once the most critical components for application implementation are selected, together with the communication protocol and the operating regime of the node it is possible to determine the size of the energy storage. The next step is to select the energy management block that will provide the control and distribution of the stored energy to the rest of the circuit. The final step is determining if the energy neutrality has been achieved. If this is not the case it is necessary to revisit the steps that are not constrained by the application requirements, and optimize them. Which blocks are going to be optimized are dependent on the application parameters as: size, cost, efficiency, time required to implement it, etc.

The following sections address steps required for designing the EH-WSN node and explain in more detail the design steps required for their implementation. It should be noted that these are general guides and that the actual component and methods used for their implementation are going to be application specific.

2.1. The Energy Harvester Selection

The design process begins with the selection of the environmental power source to be used. Any change in the environment represents a change in the energy and hence a possibility to harvest a part of that energy and convert it to electrical energy. Vibrations, light sources, thermal differences between objects, flow of fluids are just some of the possible energy sources. The energy harvesting power sources are covered in more detail in Chapter 3.

The designer must be aware of the harvester's influence on the surrounding environment as well. As the harvester interacts with the surrounding, collecting the available energy, the original functionality of the system can get influenced. In case of solar energy there is no influence of the photovoltaic to the light source, however, in the case of mechanical harvesting that isn't always the case. In situations where unwanted vibrations are being harvested, the harvester is acting as a damper reducing the vibrations; hence have a beneficial effect to the system. However, in a case of harvesting human motion it is important to consider the interaction of the harvester with the user. For example, harvesting the power of the human gait by using a harvester that is attached to a human knee yields a high power output [42], however, it can result in discomfort for the wearer. Similar issue was recorded

when people were using energy harvesting shoe soles that were deforming so much that they gave an impression of "walking on sand" [124].

In the given application environment it is usually possible to determine several potential energy harvesting sources. The issues that should be answered when selecting a power source are [16]:

- Is the source always available?
- Does it vary in intensity?
- How many different sources can be exploited?
- Is it a cost-effective solution?
- To what extent does the harvesting process affect the primary energy source?

Depending on the selected power source an appropriate harvester can be chosen. Different energy harvesting approaches are coming at a different implementation costs and complexities. The cost of the harvester and the interface circuit should also be taken into account when designing a system.

The system doesn't have to be limited to only one energy harvesting source. Multimodal harvesting system have been presented that combine several energy inputs in order to meet the energy requirement of the system [116, 131].

2.2. Buffer Storage Type Selection

After selecting one, or more, potential power sources next step is to determine the type of the buffer storage used. The choice of the storage will have a huge impact on the design and implementation of the power management and other subsequent stages.

There are two most common storage types used. One is the capacitor and other is the battery. The characteristics of different capacitors and batteries were covered in detail in Chapter 2.

From the application point of view it can be stated that capacitor based storage has an advantage in the lifetime and the current sourcing capability, however, the capacitors require a larger volume to store the same amount of energy compared to a battery solution. One more advantage of a capacitor based system is the fact that it can be used in harsh environments and is less prone to the environmental impact compared to the batteries. Furthermore, capacitors are safer to use compared to the batteries and have a smaller environmental impact when disposed.

The capacitors are a preferred buffer storage element in the cases of applications where the system is activated only when sufficient energy is accumulated. In these applications the buffer is charged and discharged with every startup of the system. The limited amount of charge/discharge cycles of

a battery will severely shorten the lifetime of the system in this kind of applications.

A major advantage of the battery approach is that when a battery is used the system has energy on its disposal immediately and this can be used for powering the electronics ensuring that all components are operating inside their specified operating range. Beside limited number of charge cycles another drawback of a battery buffer is requirement for a precise battery management [33].

On the other hand in case of a single capacitor based buffer storage there is no need for complex management circuitry, however, the circuit has to be able to demonstrate stable operation even with the voltages below 1V. This requirement is increasing the circuit's complexity and can be a limiting factor in some situations.

There is also an option of using both the capacitor and the battery for storage where the capacitor is primarily used and battery is used only when the energy source is not available. The battery is then replenished when excess energy is available [78].

While making the choice for the type of the storage that will be used, one should take into account the benefits and drawbacks of the both storage approaches and in conjunction with the application requirements select an appropriate storage technology.

2.3. Power Management

After selecting the storage type the power management stage should be evaluated. The operation of the power management stage has been described in detail in Chapter 2. The implementations of different power management stages for several different energy harvesters have been presented in Chapter 3.

When selecting the power management stage the key factors that need to be kept in mind are: (i) the type of the energy harvester, (ii) type of the storage buffer used (iii) the efficiency; (iv) the application specific requirements as: allowed circuit complexity, the operating conditions of the system, cost, size, etc.

Depending on the type of the harvester selected and the target efficiency of the power management stage, the choice of the circuit to be implemented can be driven by the following questions:

- Is there a need for rectification of the harvester's output?
- Is the storage connected to the power management circuit requiring different voltage level than what is produced by the harvester?
- Is there a need for matching the impedance of the harvester output to the input impedance of the power management circuit? Is the gain of

implementing the impedance matching going to justify the increased power consumption of the stage and added complexity?

- Is there a need for the maximum power point tracking of the generator output? What are the gains of using the circuit, and what are the costs both in power consumption and in circuit complexity?

A very important fact that needs to be kept in mind, when designing the power management stage, is that this stage is typically always active. Therefore, it is directly making an impact to the amount of power stored ultimately defining how long time would be required to collect the energy required by the application.

The use of advanced power management circuits, the impedance matching and maximum power point tracking can increase the power output of the harvester several orders of magnitude depending on the harvester used. This is especially true for the piezoelectric harvesters as demonstrated in the Chapter 3. However, in some applications it is possible, by selecting an appropriate energy harvester, to remove the power management stage entirely from the system while increasing the overall efficiency. This approach has been demonstrated in the first case study.

2.4. Operating Regime of the Wireless Sensor Node

A feature, often present in energy harvesting wireless sensor nodes, is the harvester's incapability of sufficient power supply to run continually all the circuits located on the node. Therefore, the system has to accumulate energy in a storage and then use it in short bursts of activity. Based on the way this energy is utilized we can distinguish two sensor node operation scenarios:

- The "One-shot" operation scenario
- The interval based operation scenario

The "One-shot" operation scenario can be defined as a scenario where the buffer is charged until the required energy for performing the required application task is reached after which the buffer capacitor is depleted and the process repeats itself. This approach is used in systems where the frequency of measurements isn't of high importance and the energy harvester should transmit as often as the energy allows. For example, in [38] a measurement of the power consumption of a household appliance is deduced from the frequency of received packets from the node. The harvester powering the node is designed to have a power output proportional to the current going through the cable.

Similar case with performing a transmission as soon as the energy is available can be seen in [138]. Here the harvester is located in the shoe and as the person is stepping the buffer is being charged ultimately reaching the voltage that allows the system to transmit the data.

In the interval based scenario the sampling frequency is determined by the application. The biggest difference to the previous scenario of operation is that the energy management is designed in a way that provides a mechanic to store excess energy for later use allowing the system to continue operation when the energy is not available any more. Typical examples are solar cell powered systems where a buffer is used to store the energy allowing the system to continue operation in conditions with low or no light sources.

Two different operating scenarios are demonstrated in Fig. 5.2. These are results of a simulation where both operating scenarios were using the same varying power source while running the same task.

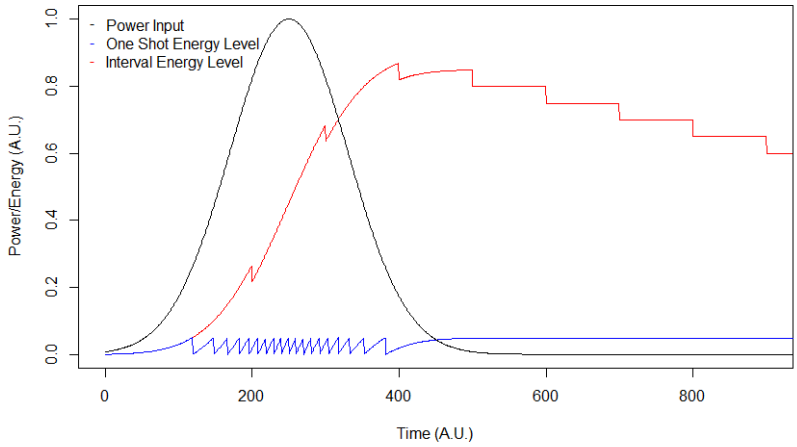

Fig. 5.2 The comparison of operation of "one-shot" system and interval based system.

From Fig. 5.2 it can be easily seen how the one shot operation has activated more often when there was more power available. The interval based scenario stores the excess power allowing it to continue operation even when the environmental energy is not available any more.

Based on the application requirements the operation scenario can be selected. The selection of the application scenario is going to have a major impact on the sizing of the buffer storage and energy management. In the case of "one-shot" systems the buffer storage can be rather small as it only requires keeping the energy for performing one measurement followed by a transmission. On the other hand, if the interval based system is needed, the storage has to be able to supply sufficient power for the node until the energy source is available again.

In the case of applications that have a requirement for the maximum allowed time between two activations of the system it is possible to determine

how long the system can spend accumulating the energy. For example, an application could require that the radio should be turned on every second for a defined period of time to transmit a beacon, or that the application requires at least 5 samples of the sensor per minute.

Once the duration of the sleeping interval is known, it is possible to calculate the expected energy budget for the application, i.e. the maximum amount of energy that is going to be on the node's disposal before violating the task deadline. This energy budget estimation can be used throughout the process of component selection as it gives a target average power consumption of the entire node. The energy budget per activation can be approximated using the following formula:

$$E_{PBO} = P_{EH}\eta_{PM}(T_{SLEEP} - T_{ACTIVE}) \tag{5.1}$$

,where E_{PBO} is the energy budget for activation, P_{EH} is the power generated by the energy harvester, T_{ACTIVE} is the time the sensor, radio and controller are active while T_{SLEEP} is time the system spend accumulating energy. In low duty cycle systems T_{ACTIVE} can be neglected as it is typically orders of magnitude shorter than the sleeping period, η_{PM} is the efficiency of the power management stage. This formula holds under the assumption that the static power consumption of the circuit during energy collection phase can be neglected.

2.5. The Selection of the Sensors, Controller and Communication Technology

The selection of the controller, communication and sensors are going to be heavily influenced by the application requirements. The critical aspects that need to be addressed in this step are:

- What is being sensed and what sensors should be used?
- What are the requirements for the data processing?
- How is the data going to be transported to the collection point?

These aspects are going to define the energy required for each activation cycle of the sensor node. The first step is determining the energy required to perform the measurements required by the application. The choice of the sensor and its optimal operation is of the highest importance. The sensor technologies have been briefly addressed in Chapter 3. together with some power reduction techniques.

Second step is based on determining the level of data processing on the data and how is the data going to be transported to the collection point. Performing the processing of the data on the sensor node will lead to reduction in data size that is going to be transmitted over the air. As the radio is

typically the most power consuming element of the system reduction of the time radio is active is going to decrease the overall power requirement for the node. An example of such approach is structural health monitoring. These systems are often relying on measuring the vibration of the structure at high sampling rates in order to determine the health status of the structure. These measurements can consist of thousands of measurement points and transmitting all of them would require a lot of energy. Instead the sensor node performs the processing of the data and only transmits a signal if there is something out of order with the structure. This approach was demonstrated in [162].

Another consideration that can be made is if the data should be sent as soon as it is available or collected over a period of time and only then transmitted. At first it might be seem obvious that collecting a large amount of data and transmitting it at once is going to be more energy efficient as the radio is being used more efficiently, however, that is not always the case and is dependent on the application and the components as shown in [110].

Last critical aspect of the design in this stage is selecting an appropriate communication technology. A review of different wireless communication methods has been presented in Chapter 2.

The selection of the communication method and protocol for communication is going to be mainly driven by the following application requirements: the required data rate, the expected range, the reliability, the power consumption, the compatibility with other devices and networks and finally the regulatory approvals.

Once all three aspects of the sensor node operation are known it is possible to determine the required energy consumption per activation:

$$E_{op} = E_{sensor} + E_{proc} + E_{comm} \tag{5.2}$$

where the E_{op} represents the total energy required for performing the application required task when the energy has been accumulated, E_{proc} is the energy consumed by the node for processing the data and managing the sensor interface and communication interface, E_{sensor} is the total energy required for performing the required measurements and the E_{comm} is the energy required for transmitting the data or storing, depending on the systems design.

Depending on the amount of tasks the node needs to perform, and the operating conditions, the node can have different energy requirements based on the tasks it needs to perform when activated. The goal of this stage is to determine the maximum energy required for completing the application specified tasks during one active period. This will define the worst case scenario energy consumption which is necessary for sizing the buffer storage element.

2.6. Buffer Storage Size

The size of the buffer storage depends on the type of storage used, the operation scenario, power output of the harvester and energy required for performing measurement and transmission tasks. The sizing of the storage is mainly going to be driven by the operation scenario. First step in determining the size of the storage is to determine the amount of energy it is required to store.

2.6.1. Interval Based Operating Scenario

If the interval based scenario is required by the application the storage has to be able to maintain enough energy for the node to run between the periods of reduced energy input from the environment. For example, operating a solar powered node on the stored energy during the night. The approximation of the energy budget required for such operation can be done using the following equation:

$$E_{stor} = N\left(E_{op} + P_{sleep}T\right) + P_{leak}NT \tag{5.3}$$

where E_{STOR} is the amount of energy that should be stored during the period when the harvester is producing energy. E_{op} is the estimated amount required for performing the application task. P_{sleep} is the static power consumption of the system in the lowest power mode that can be measured during the changing of the storage. T is the period between executions of two consecutive application tasks. N is the number of times the node should be activated before the energy source is available again. P_{leak} represents the power loss due to the fact that storage element isn't ideal. For batteries P_{leak} is small, however, for supercapacitors the power lost can be sometimes larger than the power used by the node [78]. The formula (5.3) assumes that the time node is active is neglectable compared to the charging time as is typically the case in low duty cycle systems.

2.6.2. One-Shot Operating Scenario:

In applications that are required to operate in "One-Shot" regime the buffer needs to be only as large as needed to provide sufficient energy for completing the required application task.

2.6.3. Determining the Size of the Storage:

Once the required amount energy to be stored is determined it is necessary to select the size of the storage to be used.

In the case of the capacitor buffer storage the required capacitance is going to depend on the voltage levels at which the energy is going to be stored. The capacitor based energy harvesting systems typically have minimum and maximum voltage levels at which they will operate. This means that the buffer will be charged to a high threshold and then discharged to a low threshold. The energy stored in the capacitor between these two thresholds should match the calculated energy requirement.

The amount of energy stored is proportional to the square of the voltage hence it is possible to reduce the size of the capacitor by storing the energy at a higher voltage. However, this is coming at a cost of increased capacitor leakage currents as the leakage currents are a function of applied voltage across the capacitor. In case of storing the energy at voltage levels that are above the maximum voltage level required by the rest of the circuitry that is powered from the storage it is necessary to convert the voltage, which is in turn coming with an energy loss. Furthermore, the energy management stage would require more power to run at higher voltages. The effect of storing energy at higher voltages and impacts on the circuit are going to be discussed in the first case study.

In the case of battery storage the size of the battery should be selected in a way that the discharge of the battery is as "shallow" as possible. This is necessary as the number of charge/discharge cycles supported by a battery is typically exponentially dependent to the percentage of discharge before recharging the battery. For an example, in a case of a solar powered system that is required to operate over night if a battery is sized so it gets discharged 3% of its nominal capacity during the night, the battery could be used for over 10 years before it degrades [120]. This effect was addressed in Chapter 2. Section 3.5.

2.7. Energy Management

Once the storage has been selected and the voltage levels on the buffer storage are known the last element of the system can be addressed. The energy management block has the goal of arbitrating the charging process of the storage and routing the energy to different parts of the node when needed.

The complexity of the energy management stage is mainly dependent on the type of the storage used and the mode of operation of the node. For example, in "one-shot" operating scenarios the energy management section has the task of monitoring the buffer energy level. Once sufficient amount of energy has been collected the energy management would activate the node which will process to utilize the stored energy. Therefore, it is easy to conclude that the harvester needs to provide enough power to run the energy management section and have excess power to charge the buffer capacitor.

The break-even point of the harvester is considered the point where the harvester provides only enough power for the energy management and power management section of the circuit. As a result the buffer cannot be charged any further [28]. In the battery driven applications it is important to prevent discharging of the battery once the output power of the harvester drops below the break-even point, otherwise, the circuit might attempt to charge the battery but actually discharging while attempting to utilize the insufficient power output of the harvester.

2.8. Optimization and the Energy Neutrality

After the first run thought the design process is completed, the next step is to evaluate if the power demand of the node is met by the power delivered by the harvester. The generated power can be depicted as a circle with its radius representing the power level. The various parts of the system can be depicted as sectors with their areas representing their respective power requirement. Once the graph is designed is easy to determine the major contributors to the power consumption and select which parts should be optimized.

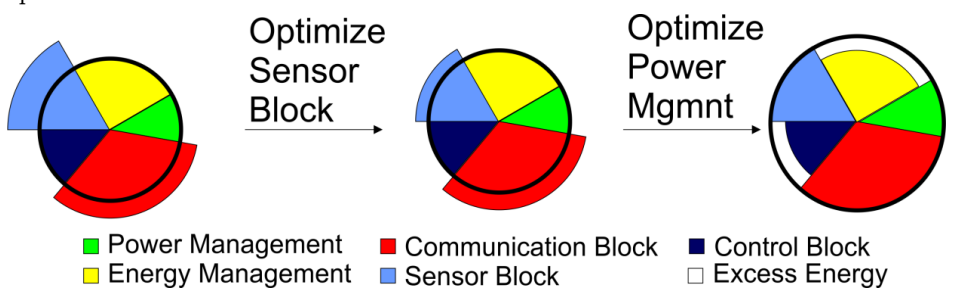

Fig. 5.3 Using energy pie chart to determine impact of different elements on the energy budget

An example of an optimization process is shown in Fig. 5.3. After the component selection was performed it was determined that the system couldn't be realized, as the required power was larger than the power available. After analyzing the components used, it was decided to reduce the sampling interval of the sensor, hence reducing the power consumption of the sensor block. Next step was optimizing the power management. It can be seen that the total power requirement of the power management was increased. On the other hand the energy generated by the harvester has also increased. This is a typical example of adding a maximum power point tracking for a photovoltaic system, or substituting a diode bridge with a SSHI rectifier in a piezoelectric generator case. As a result, the power requirement is met and the system can be realized.

It should be pointed out here that in some applications using the highest efficiency harvester in conjunction with the highest efficiency power management for this type of harvester doesn't always result in an optimal operation of the node. It might occur that for the given application the highest efficiency harvester will have an output that could be interfaced only to a low efficiency power management. Therefore, in some cases it is beneficial to sacrifice the efficiency of the harvester in order to gain in the efficiency of the power management stage, hence making the overall generated power higher than with the optimal harvester. As a result when evaluating the system, the energy harvester and the power management stage should be evaluated together.

3. Summary

This section has introduced a methodology for designing an energy harvesting powered wireless sensor node consisting of nine steps. The process described in the methodology will lead the designer through all the steps needed in order to realize an energy harvesting powered wireless sensor node. The goal of this section was to make an introduction to each step of the design process and define some key questions that need to be addressed when designing the energy harvesting powered application.

4. Introduction to the Case Studies

The research done in [38] has shown that the majority of the energy consumption in the near future is going to come from the commercial buildings. Therefore, there is an initiative to automate the buildings in order to conserve energy without reducing the comfort of the people using them. Through this initiative the concept of smart houses and smart living was developed. In order to optimize the building's power consumption heating and air conditioning system are one of the main candidates for optimization. In order to do so, it is necessary to obtain information on the temperature and humidity as well as the occupancy of the space. Therefore, two case studies have been made around gathering the required information.

The first case study will focus on use of small amounts of energy available in low light conditions for powering environmental sensors. For example, restaurants, cafes, living rooms in residential houses, hallways, all these places have light levels that are under 100 lux sometimes even as low as 10 lux. This case study was aimed at providing a method for utilizing these low light levels for powering environmental sensors. A wireless sensor node was

designed and implemented that was capable of operating at power levels as low as 1μW.

The second case study is aimed at determining human presence in an area. Information on human presence can be used to control the air conditioning in the room, temperature and lightning. This case study is using the energy generated by a person stepping on the floor to power the occupancy sensor. When a person steps on the floor, a tile equipped with the energy harvester compresses under the weight of the person and an amount of electrical energy is generated from the compression. The electrical energy generated is used to transmit a signal wirelessly. In this way the presence of a person is detected. Additionally it is possible to detect the direction of the person stepping onto the tile. Based on the movement direction information more advanced possibilities for automation arise. For example, turning lights and air-conditioning off when a person exits the room, or opening the door as a person approaches.

Bothe case studies are going to be implemented following the methodology laid out in the beginning of the chapter.

5. Case study: Low Light Level Building Automation

5.1. Application Requirements

The aim of the case study is to provide information on temperature and humidity indoors using solar power. The frequency of measurements should be no less than 15min and there is no requirement for continuing operation during the night. The humidity sensor that should be used is SHT11 by Sensirion [4]. The goal was also to minimize the active solar cell area and to use a capacitor as the buffer storage source in order to maximize the lifetime of the system.

The main challenge of this work was designing the energy management stage that would have minimal impact on energy collection. This was important as the expected amount of generated power by the harvester was in microwatt range.

5.2. Profiling the Potential Energy Harvesting Source

First step in designing the energy harvesting system was determining the power source for the system. From the application requirements the wireless sensor node was aimed to be deployed in a common area inside the office building placed on a wall and powered used a solar cell.

The measurement of available light level was done at noon and in the evening when only artificial lightning was available. The highest measured

light intensity was 42 lux at noon while the light intensity when only the artificial lights were active was 10 lux.

For this application a solar cell ECS300 [56] from EnOcean was selected because of its size, price and availability. This solar cell has an area of 4.5cm^2. Based on the datasheet of this solar cell its output is rated at 200 lux to be 4µA at 3 V when operating at the maximum power point. The solar cell has been profiled at the minimum and maximum expected light levels based on the measurements done in the deployment environment. The output power, as a function of the cell voltage is given in Fig. 5.4.

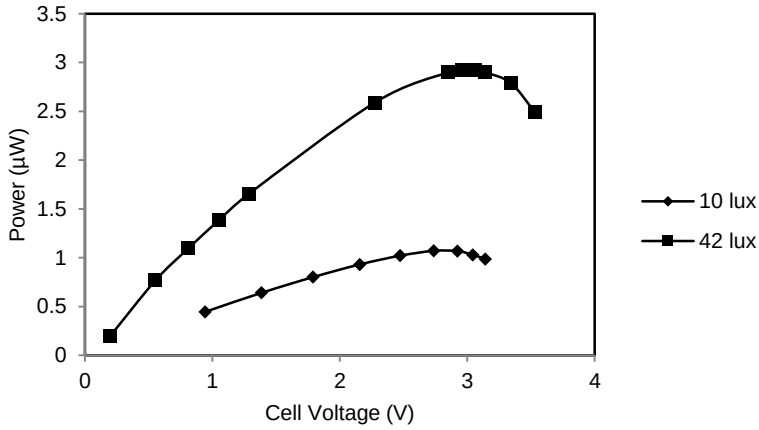

Fig. 5.4 The power output of a single ECS300 solar cell in expected indoor light conditions. The maximum and minimum light levels measured were 10 lux and 42 lux.

Following the methodology laid out in the beginning of the chapter after determining the power output of the energy harvester, the step was determining the type of energy buffer storage.

5.3. Selecting Storage Type

This application was aimed at a long deployment life, possibly as long as the building itself, therefore, it was necessary to use a capacitor as the buffer storage element. One additional reason for the utilization of a buffer capacitor was the fact that the node was only supposed to be active when there was power available. Furthermore, the time delays between measurements weren't supposed to be fixed so the system was free to transmit as often as it had energy to do so.

5.4. The Power Management

The power management section of an energy harvesting system has two main objectives. The primary objective is to convert the output of the harvester to match the input required by the storage. The secondary objective is to operate the harvester at a maximum power point.

The solar cell chosen has a voltage output that is around 3V when operating at the maximum power point, therefore, it is possible to directly interface it to the rest of the circuitry without a need for voltage level manipulation. Therefore, the power management stage was not needed for voltage level conditioning.

The next step was evaluating a need for a circuit that would keep the cell at the maximum power point and evaluate if there is a need for maximum power point tracking.

In order to be able to examine different operating scenarios of the power generation the output efficiency of the cell will be considered as the ratio of the output power and the power at the maximum power point.

In the range of expected light levels the maximum power point exhibits a 0.2V shift between the minimum and maximum light level. This means that areas where the solar cell has efficiency over 90% overlap regardless of the applied light intensity level. In Fig. 5.5 the area marked with >95% represents the range of cell voltages where the generated output will be more than 95% of the power generated at the maximum power point regardless of the light level. It should be noted that the area of >90% is has only slightly wider cell voltages than the >95% area indicating that the efficiency drops fast as the voltage of the cell moves further from the maximum power point voltage.

A question can be raised if the MPPT circuit is going to be able to provide higher efficiency than directly coupled system. If the cell is set to operate at a fixed voltage level, in the range of voltages that guarantee over >95% output efficiency, it would result in a total loss of 53 nW at 10 lux and 145 nW at 42 lux. Therefore, the MPPT circuit needs to be able to operate using less than 145 nW, in the case of highest losses, in order to be more efficient than a system operating at a fixed voltage. To my knowledge there are no MPPT circuits currently available capable of operating at this power level at 3V supply voltage.

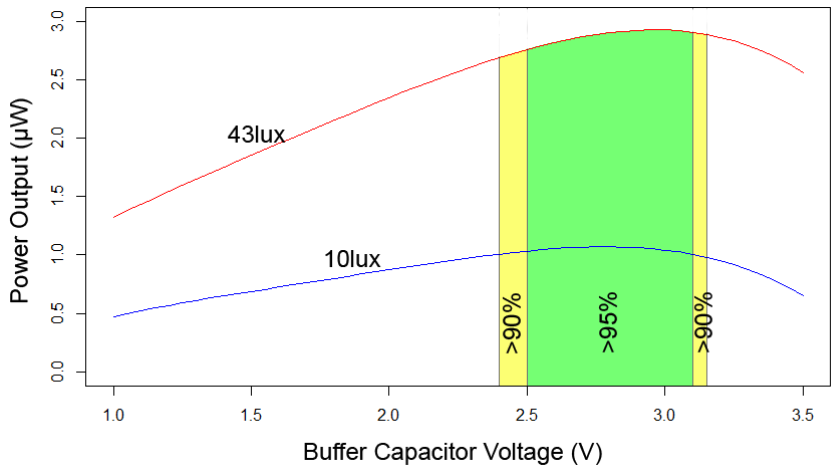

Fig. 5.5 The output efficiency of an ECS300 solar cell depending on the voltage on the buffer capacitor

As a conclusion a MPPT circuit is not going to be used. The voltage on the solar cell could be controlled in the voltage range that provides high harvesting efficiency.

5.5. Defining the Operating Regime of the Energy Harvesting Node

The delay between measurements is defined by application requirements to be less than 15min. This system was aimed to operate following the "One-Shot" operating scenario. This kind of energy harvesting operation has been previously explained in Section 2.6 of this chapter. The most important aspect of the "One-Shot" operating scenario is that there is no storage of excess energy and that the system operates as often as it has energy.

Due to the fact that there is a requirement for how often the measurements need to be taken, next step was determining the energy budget. In the power management section was determined that it is possible to operate the solar cell at the maximum efficiency of >95%. Combining this information with the application requirement for transmitting the measurement once every 15 min the energy budget for the system can be approximated using the equation (5.1). In this particular case the $T_{SLEEP} >> T_{ACTIVE}$ so T_{ACTIVE} can be neglected. P_{EH} in the worst case scenario is 1.07µW at 10 lux and η_{PM} is 95%. When all these parameters are substituted in the equation (5.1) the resulted energy budget is 914µJ in the worst case scenario. In other words, without altering the energy harvester the rest of the electronics needs to be able to operate with no more than 914µJ per transmission interval.

5.6. The Sensor, the Communication and the Controller Selection

The sensor is predefined by the application. The SHT11 was profiled and it requires around 600 µJ of energy at 2.7 V supply in order to perform a humidity measurement. The approximated energy budget was 914 µJ leaving still an overhead that could be used for powering the rest of the system.

For the communication the radio nRF24L01+ from Nordic semiconductor was selected [134]. This choice was made as this is one of the lowest power radios available on the market, at the time of writing the thesis. This radio module was measured to require only 10 µJ of energy to perform a wireless transmission with acknowledgment of the received packet.

The controller selected was MSP430G2553 by Texas Instruments [74]. This choice was made as the system had to run for a very brief period of time and this microcontroller has performed the best based on the results in Chapter 4.

The temperature measurement was performed using a thermistor instead of using the sensor that is located onboard SHT11. This was done in order to optimize the power consumption, otherwise, the approximated energy budget wouldn't be able to cover the energy requirement for performing both temperature and humidity measurement using the SHT11 sensor. The total of 3 µJ has been measured to be required to perform a temperature measurement using a thermistor as a sensing element.

5.7. Determining the Storage Size

This section will focus on explaining the capacitor sizing process followed by a demonstration of how to reduce the power consumption of the circuit by selecting proper operating voltage.

Based on the information on estimated energy requirement of individual components it is possible to calculate the total energy requirement per activation of the system. In this case the energy consumption of the radio and the temperature measurement are neglectable compared to the energy requirement of the SHT11 humidity sensor. Therefore, the storage size calculation is going to be done for an approximate energy requirement of 600 µJ. This is an approximation because the actual energy consumption of the node can only be determined experimentally. The precise analytical calculation of the energy requirement can't be done due to observed nonlinear relationship between the current consumption and the applied voltage on the SHT11 sensor. As the system is powered from a capacitor the voltage will change as the system operates hence leading to changing energy consumption as the device operates.

The system is operating out of the capacitor storage. Therefore, it was necessary to select a threshold voltage at which the system would activate and perform the measurement and transmission of the data. From the output characteristic of the solar cell (Fig. 5.5) it can be seen that if the activation and deactivation voltages are kept in the range of 2.4 to 3.15V the solar cell would be over 90% efficient for all light conditions between 10 lux and 43 lux. Therefore, the most obvious step would be to design a system that would operate from 3.1V down to 2.5V. Experimentally was determined that under these voltage operating conditions the energy required by the SHT11 sensor to perform one measurement would be 664 µJ. As a result, the capacitance required to store this amount of energy using the upper and lower threshold levels suggested, was calculated to be 384µF.

By narrowing down the voltage limits under which the buffer capacitor operates it is possible to increase the efficiency of the system at a cost of prolonged startup time. Prolonged stating time is coming from the fact that a larger capacitance is needed when the voltage range on the capacitor is reduced.

If the startup time isn't a limiting factor, by activating the system at 2.89V and discharging to 2.5V the same efficiency of the solar cell will be maintained while the overall energy consumption of the system will be reduced. The reduction of the energy requirement is coming from the fact that at 2.89V the system has lower energy consumption due to lower operating voltage. The energy required to perform a measurement at 3.1V while discharging the capacitor to 2.5V was 664µJ. On the other hand starting the measurement at 2.9V and discharging a larger capacitor of 510µF to 2.5V resulted in 550 µJ of used energy. Therefore, by using a larger capacitor, longer charge time during initial startup will be compensated by more frequent transmissions once the system reaches the solar cells operating voltage. The increase in frequency of transmission is coming from the fact that a smaller amount of energy needs to be replenished between two consecutive measurement operations.

It is possible to achieve even lower energy consumption while keeping the smaller capacitor when the startup time is critical factor. This can be achieved by placing a DC/DC power converter stage between the buffer and the load [75]. Based on measurements done during profiling of the SHT11, it was calculated by interpolation of data, that the power consumption for performing a measurement at 2.4V would be 3.7 mW over a course of 80ms resulting in 240µJ. In theory, using a low power high efficiency switching DC/DC converter, for example, the TPS62730 by Texas Instruments [75], it would be possible to achieve efficiency of 90%. However, the efficiency graphs in the technical documentation of the component don't state the energy required to start the DC/DC converter. As these losses are not documented estimating the actual efficiency is not possible. Furthermore the addition of a

DC/DC stage would further increase the complexity of the board and at this point there is still no need for optimization of power consumption.

In the end for the approach with longer initial charging time was selected as it will provide a higher frequency in sampling.

The total input current is in order of nanoamperes, therefore, it is necessary to choose a low leakage capacitor. The capacitor selected was 560µF/6.3V Panasonic FM series. Some of the other low leakage electrolytic capacitors are 013 RLC series from VISHAY, RLB series from ELNA, the HE/M series from Nichicon. When selecting capacitors that are required to have low leakage currents it is important to select capacitors with low rated voltages as the leakage current of the capacitor is proportional to the product of the rated voltage and the rated capacitance.

5.8. The Energy Management

The examination of the energy budget and the total energy requirement for performing a single measurement and transmission so far suggests that this system can be realized. The last piece of the circuit is the energy management stage that will connect the buffer capacitor to the rest of the circuit.

In the operating condition section it was explained that this is an application that operates following the "One-Shot" scenario. From the energy management's point this means that it should provide a mechanic for monitoring the voltage of the buffer capacitor and activate the sensor and radio once sufficient energy has been accumulated. In the storage size determination section the threshold voltage for activation selected was to be 2.89 V.

In order to make a choice on an energy management an approximation of the required power consumption of the energy management is made. At this point total energy requirement is 600 µJ for performing the task of measurement and transmission, while available energy budget during the required period of 15 minutes between the measurements is 914 µJ. By using a simple formula (5.4) it can be calculated how much power is left for the energy management section before optimizations should take place:

$$P_{EM} = \frac{\left(E_{PBO} - E_{op}\right)}{T} \tag{5.4}$$

where P_{EM} is the power consumption of the energy management, E_{PBO} represents the available energy budget and E_{op} represents the energy required the node to perform the measurement and transmission. Using formula (5.4)

the maximum allowed power consumption was calculated to be 333nW. As the solar cell is already operating at maximum efficiency the main challenges in realizing this system becomes the energy management stage that would meet the calculated power constrain.

A comparator in combination with voltage references is typically used for the voltage monitoring task. However, even top of the line off the shelf comparators, at the time of writing this thesis, require at least 840 nW to operate [153]. This power requirement was close to the power generated by the solar cell. Therefore, the energy management was required to have at least an order of magnitude lower power consumption. This power consumption was reached by using the energy management circuits described in Chapter 4.3 and Chapter 4.4.

The circuitry performing the task of monitoring the buffer capacitor should be able to start operation with storage buffer empty. A circuit capable of performing voltage monitoring at required power level is Nanowatt Voltage Detector (NVD) presented in Chapter 4.3. However, the NVD circuit has a limited selection of the threshold voltages and its activation voltage will depend on the output power of the harvester. These factors limit the circuits operation, especially if tight control of the threshold voltage is required in order to achieve operation in the range of maximum power output of the solar cell and minimize the power consumption.

On the other hand, the ADC energy management circuit, presented in Chapter 4.3, can adjust the threshold voltage level easily in software, however, it cannot be powered from a high impedance source before the voltage reaches 1.8V.

The idea was to combine these two approaches in one solution for complete nanowatt energy management. In this solution the system would operate with NVD performing the buffer voltage monitoring until the buffer reaches 2V. After this the ADC energy management circuit would take over the task of the buffer monitoring until the buffer reaches the desired threshold voltage. Based on the measurements done in Chapter 4.3 and Chapter 4.4, the expected power consumption of the ADC energy harvesting block was 50nW at 2.7V while the NVD has a power consumption of 15nW at 2V.

5.9. Evaluating the Energy Neutrality

The goal of this step is to determine if the available energy budget from the harvester is equal or larger than the energy requirement of the system. First the power output of the harvester is reevaluated. The energy harvester is directly coupled to the buffer capacitor and the minimum and maximum operating voltages for the buffer have been set so the output efficiency of the solar cell is above 95%. This means that the system will have at least 1µW of power in the worst case scenario of 10 lux illumination.

The estimated power consumption of the energy management stage is based on the estimated power consumption of the ADC energy management. The ADC energy management power consumption was profiled in Chapter 4.4. Based on the measurements 900 nW are left for the capacitor charging when the power consumption of the ADC energy is subtracted.

The total energy requirement for performing sampling and transmission was measured to be 560 µJ. The output power of the solar cell is 900nW, therefore, the time required to accumulate required amount of energy for one measurement and transmission cycle would be 622s or 10.5min. As the requirement of the application was a wireless transmission once every 15 min it can be concluded that the system would fulfill the requirements.

5.10. Circuit Theory of Operation

After selecting all components and verifying that the energy neutrality can be met, the next step was implementing the system. Before the entire system was implemented the interaction of all components needs to be evaluated followed by implementing interfaces between them where necessary. This section will be dedicated to explaining the interaction between different blocks of the system and describe the theory of operation of the entire circuit.

The block diagram of the circuit is shown in Fig. 5.6. The full circuit schematic is available in Appendix B.

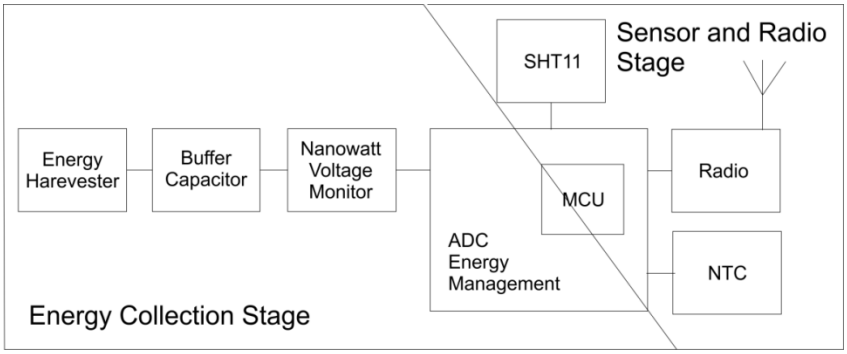

Fig. 5.6 The block diagram of the low light level powered humidity and temperature sensing wireless sensor node

The circuit can be split into two distinct parts. The division is made based on how long the part of the circuit is powered. The "energy collection" stage is active all the time and has a goal to monitor the voltage of the buffer capacitor. The "sensor and radio" stage is unpowered most of the time and is activated only when the buffer capacitor has collected required amount of energy. In Fig. 5.6 it can be seen that the ADC energy management is placed in both stages as the MCU inside the ADC energy management block is being

used for both monitoring of the buffer capacitor storage and for performing operations related to the measuring and wireless transmission of obtained results.

The circuit operation will be explained on one cycle of operation starting from an empty buffer capacitor until the humidity and temperature are measured data is transmitted. The operation of the circuit can easily explained by examining the change of the buffer capacitor voltage in time. The graph of expected buffer capacitor change in time is shown in Fig. 5.7.

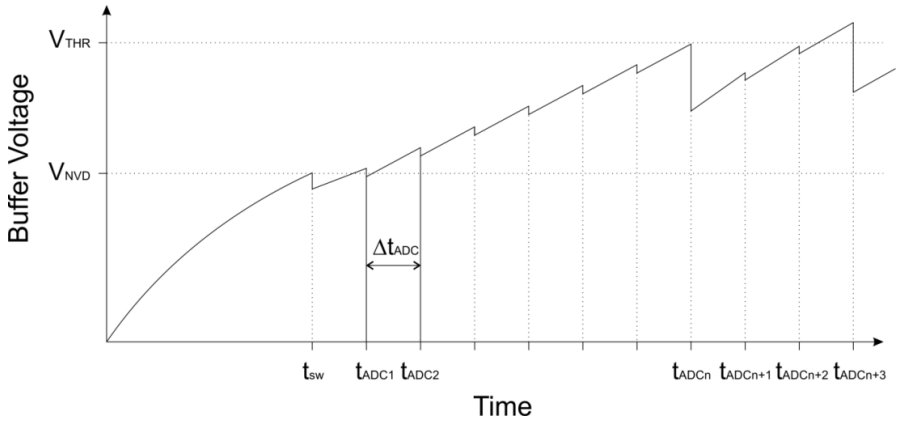

Fig. 5.7 The expected change of the buffer capacitor voltage over time as the circuit operates

In the beginning the buffer capacitor is empty. At this point only the Nanowatt Voltage Detector (NVD) is connected to the buffer storage. The buffer capacitor is being charged by the solar cell until it reaches the threshold voltage of the NVD, V_{NVD}, at the time t_{SW}. When the buffer voltage reaches the threshold of the NVD it would activate and connect the Buffer Capacitor to the ADC energy management section. From this moment the NVD is in "by-pass" mode where its contribution to the power consumption is only coming from two digital logic gates as explained in Chapter 4.2.

As soon as the NVD activates the ADC energy management, this module takes over the task of monitoring the buffer voltage. The operation of the ADC energy management is based on the MCU performing Analogue to Digital (AD) conversion in timed intervals in order to monitor the change of the voltage of the buffer capacitor. This process can be seen in Fig. 5.7 as small voltage drops of the buffer storage capacitor at times t_{ADC1}, t_{ADC2} etc. This is a result of the MCU being activated to perform the AD conversion every Δt_{ADC} seconds. By changing the time between AD conversions the average power consumption of the ADC energy management is reduced. Detailed operation of the ADC energy management is described in Chapter 4.3.

Depended on the result of the AD conversion the MCU will select which action it will perform, either continue waiting for the capacitor to charge

further, or use the stored energy. In the example from Fig. 5.7, up until the moment t_{ADCn} the amount of stored energy was not sufficient to activate the sensor and radio section. However, once the result of the AD conversion shows that the threshold voltage was reached, the MCU activates the "sensor and radio" stage, performs the required measurements followed by transmission of the collected data.

In Fig. 5.7 it can be seen that the threshold voltage has been surpassed before the time t_{ADCn+3} is reached. This indicates that if the sampling period is too long, depending on the power output of the source, the buffer might get charged more than required leading to sub optimal use of the energy collected. The delay issues of the circuit have been discussed in detail in Chapter 4.4 and will be addressed in the implementation section.

Upon successful transmission the "sensing and radio" stage is unpowered once again. The MCU goes back to the task of monitoring the buffer capacitor voltage, until the threshold voltage is reached once again and the process repeats.

Next section will address specifics around the implementation of the entire sensor node. The implementations of the Nanowatt Voltage Detector and the ADC energy management stage have been discussed in detail in Chapter 4.3.

5.11. Implementation

The implementation section will focus on the critical aspects of the circuit. First determining the threshold voltage of the NVD is done, followed by design of the interface circuit between the ADC energy management and the NVD. The last step in the implementation section will be focused on determining the period between sampling of the buffer capacitor voltage by the MCU.

After examining the theory of operation and the block diagram, the first unknown parameter in the circuit was the threshold voltage of the NVD. This threshold voltage needs to correspondent to a stored energy level that is sufficient for the ADC energy management to start, without discharging the buffer capacitor under the minimum operating voltage level of the ADC energy management. If opposite is the case, the system would never start as the ADC energy management would keep on attempting to start followed by disabling itself due to under voltage condition. When the ADC energy management gets disabled the NVD is reactivated and the buffer is charged once again to the threshold voltage of the NDV. This cyclic operation is shown in Fig. 5.8. At time moments t_{SWn} the ADC energy management attempts to start, however, is unable to, due to insufficient energy.

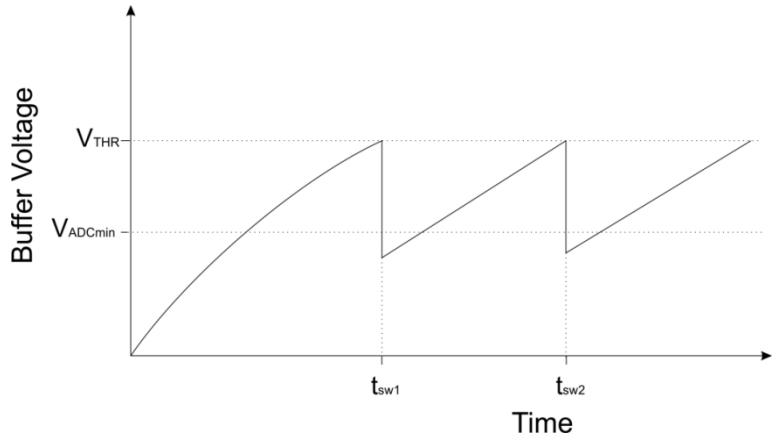

Fig. 5.8 Failure to start the ADC energy management stage due to insufficient energy

The energy required for activating the ADC energy management is strongly dependent on the supply voltage. As a result activating it at 2V would be the most beneficial from the energy stand point. Limited number of LED combinations required for threshold selection of the NVD resulted in using a blue LED as it provides a threshold voltage around 2 V. Testing has shown that the threshold voltage of NVD using a blue led was 1.93 V when supervising a buffer capacitor charged using a 50 nA current source. In this scenario the maximum allowed voltage drop on the capacitor would be 0.13V before the system reached the minimum operating voltage of the ADC energy management. In order to store 71 µJ of energy, required by the ADC energy management to start up, at this voltage the required input buffer capacitance is 292 µF. As the buffer capacitor selected was 560 µF, the V_{THD} could be set to around 2 V.

In cases where the input buffer capacitance is lower than 293 µF it is possible to use a combination of two red LEDs in order to raise the threshold voltage to 2.3 V. At this voltage level the activation energy for the ADC energy management is 105 µJ. However, the minimum required capacitance size for starting the system is reduced to 112 µF. The energy requirement for starting the ADC energy management on different voltage levels can be found in Chapter 4.3.

Next step in the implementation was providing a mechanism for disabling the NVD. As stated in Chapter 4.2 the Nanowatt Voltage Detector requires and external signal that will initiate disconnection procedure of the buffer capacitor from the ADC energy management. The connection between the ADC energy management and the NVD circuit is shown in Fig 5.9.

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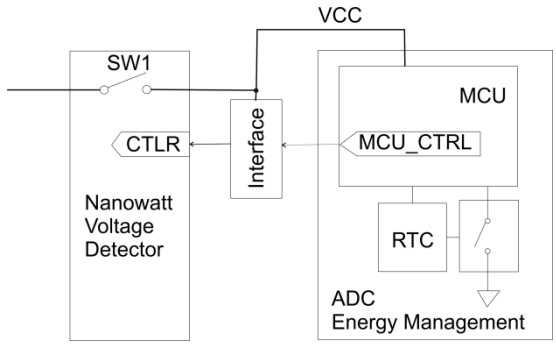

Fig. 5.9 Interface between the Nanowatt Voltage Detector and the ADC energy management

There were three requirements for the interface circuit: (i) the signal on the CTRL pin had to reach high voltage level as quick as possible when switch SW1 was closed. This was necessary as the CTRL signal is keeping the switch active. The NVD is designed only to provide a short pulse activation of SW1 after which the voltage level on CTLR line would control the SW1 operation. (ii) the MCU, when inactive, would have its ground pin disconnected. Hence CTRL line has to remain on high voltage level under these conditions as well. (iii) when the signal for disconnection is sent from the MCU, the CTRL line should remain stable even though the pins of the MCU are placed in high impedance state once the supply voltage on the MCU falls below 1.6V.

The interface circuit that fulfills all set requirements is shown in Fig. 5.10.

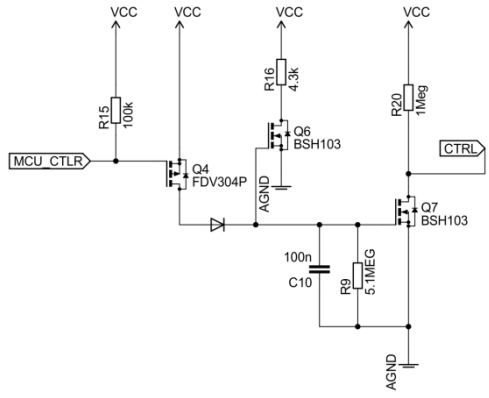

Fig. 5.10 Interface circuit between the ADC energy management and the Nanowatt Voltage Monitor

By analyzing the schematic in Fig. 5.10 it can be seen that CTRL line is connected to VCC line via a resistor. The VCC is in turn connected to the

output of the Nanowatt Voltage Detector. This provides a rise on the CTLR line once the VCC is connected to the buffer capacitor hence addressing the first requirement.

During operation the MCU_CTRL line, which is connected to the MCU general purpose I/O pin, is on a high voltage level regardless of the supply state of the MCU. This is the consequence of disabling the MCU by removing its ground connection to the common ground. During transition between inactive and active state of the MCU, its I/O pins are in high impedance state, hence there will be no change of the voltage potential on line as the line is connected to the VCC through a resistor. This has been experimentally verified on MSP430G2553.

When it becomes necessary to deactivate the SW1, thus disconnecting the ADC energy management from the buffer supply, the MCU connects the gate of the Q4 transistor to the ground potential. When this occurs, the capacitor C10 is charged, thus activating transistors Q6 and Q7. For this task BSH103 transistors have been chosen as the lowest threshold voltage transistors available through major distributors (RS, Farnell and DigiKey) in SMD packages with leads. The transistor Q7 connects the CTRL line to the ground potential hence disconnecting the output of the Nanowatt Voltage Monitor (the VCC line) from the buffer capacitor. The transistor Q6 has a goal to discharge any capacitance connected to the VCC. This is important as the voltage at the output of the NVD has to be lower than voltage on its input when the SW1 is disabled in order to ensure stable operation of the NVD.

The diode is placed in order to prevent backflow from the capacitor C10 into the VCC line through the body diode of the Q4 device. This was necessary in order to keep gate to source potential on the gates of Q7 and Q6 above threshold voltage, even when the voltage of the VCC line drops below the threshold voltage of the transistors. This provides a method to completely deplete the capacitances connected to the VCC line. When the transistors, inside the integrated circuits, stop conducting the voltage level is around 0.5V and this voltage is slowly being reduced by leakage current flowing through the integrated circuit. Therefore, a way for discharging the capacitors connected to the VCC line was necessary.

The ADC energy management continues operation as long as the voltage on the buffer capacitor stays above 1.8 V. If the MCU measures a voltage level below 1.8 V it will disable the ADC energy management by sending a signal to the NVD. The threshold voltage level for disconnection is set in software but it cannot be less than 1.8V.

After disconnection of the ADC energy management from the buffer capacitor, the capacitor needs to be recharged. Once the buffer voltage recharges to the threshold of the NVD, the ADC energy management stage will be repowered.

The next step in implementation was determining the period between two consecutive buffer capacitor voltage measurements done by the ADC energy management. The sleeping period influences the average power consumption of the ADC energy management and the efficiency of storing the energy produced by the harvester. The time required for accumulating sufficient energy for performing the measurement and transmitting the data was calculated to be 622 s. A delay period of 30 s between the measurements has been selected empirically in order to keep the average power consumption of buffer voltage monitoring low. This delay of in packet reception wouldn't play a major role in the overall system operation as the measurements were expected at least once in 15min.

The ADC energy management delay wasn't set for 600 seconds in ordered to compensate for variations in solar cell output energy. In cases when there is more light the buffer capacitor would change faster hence a long delay between sampling the buffer capacitor would result in overshooting the threshold voltage. This would in turn lead to suboptimal use of the collected energy as the circuit would be run at a higher voltage level than necessary, leading to increased energy consumption.

5.12. Measurements and Discussion

Although the theoretical evaluation of the energy management stage demonstrated that it should operate using nanowatts of energy the first steps in the testing and measurement were done in order to verify the design of the energy management stage. This stage is the most critical stage in this wireless sensor node, as the increased power consumption of this stage would prevent the node from sampling at the required rate.

5.12.1. Testing the Energy Management Stage

The first measurements were focused verifying the power consumption of the energy management stage. The current consumption of the Nanowatt Voltage Monitor is only dependent on its supply, in this case the voltage of the buffer capacitor. On the other hand the ADC energy management's power consumption depends on the frequency of the sampling of the buffer and the applied supply voltage.

For the initial test the total energy management static power consumption was measured. This was done in order to determine the baseline power consumption on different voltage levels. The results are shown in Fig. 5.11. The measurements were done with Agilent A34408 voltmeter with a 9.467MΩ shunt resistance. The threshold of the ADC energy management was set to 3.6V while the NVD threshold voltage was 2V.

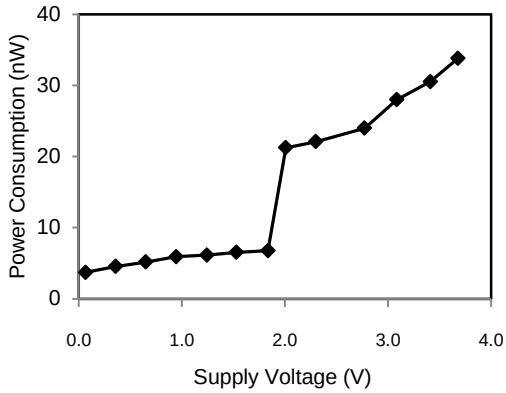

Fig. 5.11 Static power consumption of the energy management stage as a function of the rising supply voltage

In the power consumption figure shown in Fig. 5.11 a sharp change in power consumption can be identified at 2V. This jump is explained by the switch between two energy management approaches. Until 2 V the buffer capacitor was monitored by the nanowatt voltage monitor. After the 2 V mark, the management was carried on by the more flexible ADC energy management, which has higher power consumption.

When the value of the static power consumption is known, it is easy to determine the average power consumption of the system by simply adding the energy required for sampling the supply voltage divided by the interval between the measurements:

$$P_{avgEM} = P_{statEM} + E_{ADC}/T \tag{5.5}$$

where P_{statEM} is the static power consumption, E_{ADC} is the energy required for performing a buffer voltage measurement and P_{avgEM} is the total power consumption of the energy management when operating. Interval T is the period between measurements. The power consumption is the highest right before the threshold voltage is reached which is 2.89V. At this voltage it was calculated that the power consumption of the energy monitoring stage would be 74.5nW together with 570nJ per AD conversion every 30s totaling to 93.5nW of average power consumption. This power consumption would represent only 9.1% of the generated power by the solar cell at 2.9V on 10lux demonstrating that energy, even at this power level, will be collected efficiently.

5.12.2. The Full System Test

The full system test consisted of charging an empty buffer capacitor to the 2.89V threshold after which the measurement of temperature and humidity was done followed by a wireless transmission. After the transmission was completed the system was to go back to low power mode and remain there until the buffer was recharged to 2.89V.

The system has been tested indoors, in a room that had artificial light sources and a large window. The solar cell was placed vertical on the wall. The measured light level at solar cell location at the time of testing was 10-12lux due to presence of only artificial light sources. The voltage on the buffer capacitor was monitored using an AVR microcontroller with a voltage follower placed between the input of the AD converter of the microcontroller and the buffer capacitor in order to minimize the impact of the measuring equipment to the experiment. The results of the measurement are shown in Fig. 5.12.

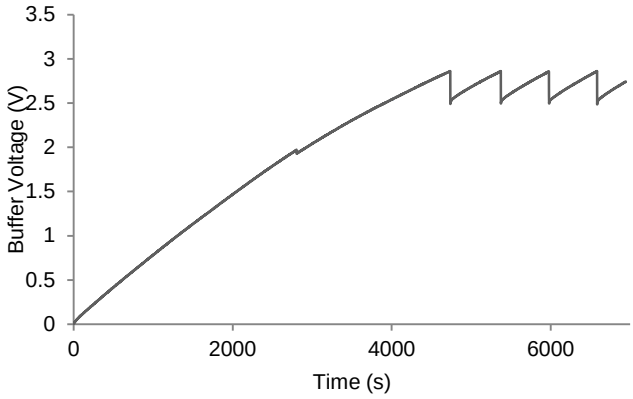

Fig. 5.12 Measured voltage on 560 µF capacitor when connected to a solar cell exposed to 12 lux light level demonstrating the circuit operation

First the energy consumption of the each temperature and humidity measurement followed by a transmission was calculated. Based on the voltage drop on the 560 µF capacitor it could be concluded that the energy consumption for startup, sampling of humidity and temperature followed by the transmission of data was 556 µF.

The charging of the capacitor began with the storage empty. It can be seen that there is a small voltage drop of buffer voltage at 2 V. The voltage drop is a result of the switch between the NVD and the ADC energy management. After the storage had reached 2.86 V a packet was sent. It can be seen that the threshold voltage is almost constant even though the measurement of the buffer capacitor voltage is taking place every 30s. The measurement has shown only a ±5mV variation between the activation voltages.

The average charging current before the first transmission was calculated to be 338 nA, while the charging current between transmissions was 334 nA. According to the measurements of the solar cell output at 10 lux at 2.7V the average current output of the cell was 389 nA indicating that the ADC energy management, together with all the leakage currents on the board, was consuming in average 55 nA verifying that the energy management was operating as assumed in the design.

The delay between the measurements was 602s ±30s. This is in line with projected time interval under low light conditions. The variation of 30s between the measurements is coming from the ADC energy management interval as the measurements and transmission can only occur at predefined time intervals.

Starting from an empty capacitor, until the first packet was sent, the time interval was 4737.38s or 78min. The energy management current consumption, which is the only power consumption during the startup stage, is neglectable compared to the power output of the harvester, so the time before the first packet was sent was mainly driven by the size of the buffer capacitor. In applications where the startup delay time is critical a smaller capacitor can be chosen as explained in the storage selection section.

The system was left to work over a course of five work days collecting information on humidity and temperature. Fig. 5.13 displays the delay between measurements through the day.

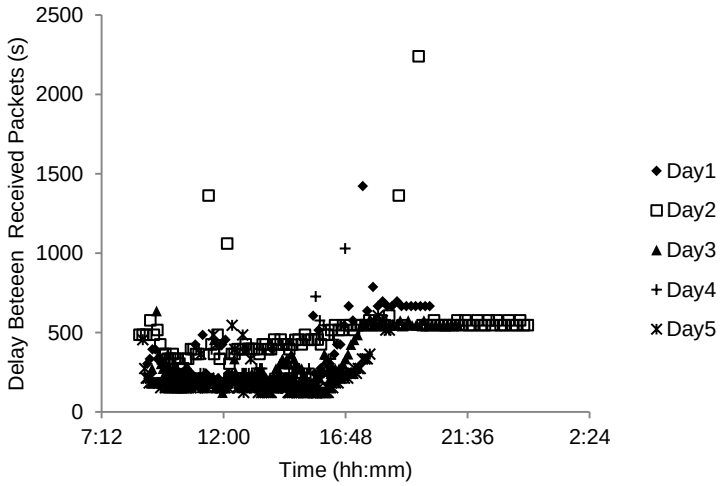

Fig. 5.13 Delay between received packets from the wireless sensor node throughout the day

It can be easily concluded based on the data that that almost all packets were received with de the delay shorter than required 900s. Several

measurements that arrived later than 900s were the result of dropped packets in the communication between the sensor node and the base station receiving the information.

During the testing, the system showed a capability of transmitting a packet even at the light level of 2 lux, however, the delays between packets in these light conditions were 3.5h. This indicated that even on such a low light level, a single ECS300 was capable of providing sufficient energy for powering ADC energy management and charge the buffer capacitor. The average current generated by the solar cell was calculated to be 46nW at 2 lux. Taken into account that the activation of the "sensing and radio stage" is defined by software it would be easy to implement a simple condition statement in the algorithm running on MCU that would trace the change of capacitor buffer storage over time. When this change is small, like in case of 2 lux, the system could switch to only performing temperature measurement instead of performing both temperature and humidity measurements. Under this scenario the power budget required for measurement of temperature and transmission would be 15 µJ. With available power of 46 nW time required to accumulate required energy would be 326 s. This demonstrates that the wireless sensor node is capable of measuring temperature in an environment that has light levels of 2 lux using a single 4.5 cm^2 solar cell.

5.13. Future Work

The system was designed to operate as frequent as possible, however, as the energy management is MCU based, it would be possible to reroute the power from the solar cell when excess power is available. At this point a transmission is possible every 10 min at 10 lux and the transmission interval dropping to 3 minutes in case of 40 lux light levels. This means that there will be excess energy if the system would operate with 15 minute delay between measurements. The excess energy could be stored in a secondary, larger, buffer capacitor that would be used when there is no more light available. The implementation of a backup storing system together with further optimization of the buffer storage capacitors are left for future work.

A part of future work is also aimed at examination of more advanced control of the timing between two consequent AD conversions of the ADC energy management. In this way a more efficient use of stored energy would be possible allowing the system to operate with a larger dynamic of input power levels.

5.14. Summary

The suggested methodology given in the beginning of the chapter was utilized to design and implement an ultra-low power environmental monitoring

wireless sensor node. The node was aimed at operating from a small solar cell at low light levels that can be expected in hallways and residential buildings. It was shown that it was possible to implement a temperature and humidity monitoring system for smart home operation using power that is until recently considered too low to be useable by the commercially available off the shelf components.. The proposed wireless sensor node has demonstrated that a wireless sensing of temperature and humidity was possible every 10 minutes in 10 lux light conditions using a 90% efficient energy management circuit.

6. Case study: Occupancy Detection Powered by Human Motion

In order to detect human presence typically PIR or ultrasonic detectors are used. These detectors require constant power source and require a clear line of sight in order to detect human presence. Another possible approach to detecting human presence is detection of the person's interaction with its surrounding. The motion of person walking could be potentially used to detect the movement by detecting the force that a person applies onto the floor as they walk. Generating energy from the people stepping on specially designed floor tiles is a known concept and has been utilized earlier as a power source [35]. By extending this approach of power generation with stepping direction detection and wireless transmission of the collected stepping direction data, the central system receiving the data can use the information for advanced building control.

The proposed system, in contrast to PIR and ultrasonic occupancy detection systems, wouldn't require any external power source as it will generate the power from the stepping motion. The biggest challenge in collecting energy from the stepping motion was generating as much energy as possible with minimal vertical displacement of the floor tile as a person is stepping on it. A displacement of even several millimeters, although would produce large amount of power, would be make an impression of sinking into the floor.

In order to address the issue of the vertical displacement a novel of harvester was designed at the Virginia Polytechnic Institute. This harvester minimizes the displacement to parts of the millimeter while providing sufficient energy to transmit wirelessly the information on stepping on the floor tile.

The work on the energy harvesting floor tile (EH tile) was divided into two phases. In the first phase, the first prototype had a task of collecting the energy generated by a step and using the energy to perform a wireless transmission. In the second phase, that was still ongoing during the writing of

the thesis, the tile is used for both generating power and stepping direction detection. This additional information of the stepping direction will extend the range of applicants of the tile providing more precise occupancy information. For example, it would allow the system monitoring the movement to know if a person is entering a room or exiting. It could potentially be used as an input for automated door control where the doors would only open if a person is walking towards them.

The two phases in development are going to be addressed separately and the methodology proposed in the beginning of the chapter will be used in order to complete the first phase. The second phase has similar hardware with the only difference laying in the energy management stage, therefore, not all design steps are going to be repeated.

7. Phase 1

7.1. Application Requirements

The application requirement for Phase 1 of the project was designing an electronic circuit that was going to collect the energy generated by a person stepping on the energy harvesting (EH) tile and storing it in a buffer capacitor. As soon as there is sufficient energy for performing a wireless transmission the radio would be turned on and a packet would be transmitted to a base station.

The requirement for the system was to be build using off the shelf components and modules in order to reduce the development time and keep the cost of system low. Following the design methodology laid out in the beginning of the chapter first step was selecting a harvester.

7.2. Profiling the Energy Harvester

The energy harvesting tile used in Phase 1 of the project was consisting of five specially designed piezoelectric structures. The piezoelectric structures used are known as cymbals [81]. The cymbal structures are used as they provide mechanical amplification hence increasing the strain of the piezoelectric element and thus, the power output.

In Fig. 5.14 the interior of the energy harvesting tile is shown with five cymbal structures clearly visible, four units located in the corners and one in the center of the tile. When a person steps on the top cover of the tile, the force from the step will induce pressure on the cymbals thus generating energy.

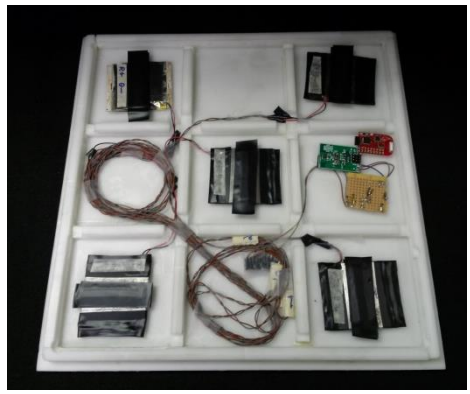

Fig. 5.14. Floor tile without the cover showing the electronics and five cymbals (courtesy of VirginaTech)

The initial power output test performed on the tile has been done by having a 71 kg person stepping on the center of the tile. The resulted output waveform of the cymbals is shown in Fig. 5.15. It was expected that the output waveform of different cymbals was going to have different shapes for every single step. From the measurements it can be observed that there are two dominant spikes coming from the motion of stepping on and stepping off the tile. During the transition period between stepping on and stepping off, the duration a person is standing on the tile, no power is being generated.

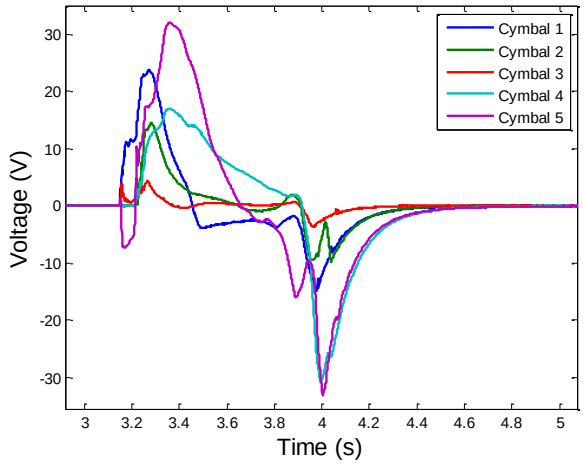

Fig. 5.15. Individual response of cymbals when being stepped on (courtesy of VirginiaTech)

After the initial power output measurement the terminals of the cymbals were connected in parallel and through a voltage bridge connected to a buffer capacitor. Depending on the capacitor size the amount of collected energy varied. This was expected because the cymbals would charge small

capacitance values fast leading to only cymbals that are generating higher voltage than currently available in buffer to continue charging the capacitor. On the other hand, large capacitances would introduce large stress onto the cymbals resulting in low efficiency as the voltage on the storage was significantly under the maximum power point voltage. The summary of energy collected depending on the capacitance value is given in Table 5.1.

Table 5.1 Energy collected per step as a function of input capacitance (courtesy of VirginiaTech)

Input capacitance (μF)	*Voltage reached (V)*	*Energy Collected (μJ)*
1	25	315
2.2	21	485
10	14	980
47	2	94

7.3. Selecting the Storage Type

The floor harvesting tile is aimed at a long deployment life as it will be a permanently placed in the floor during the construction of the building. Therefore, the use of batteries wasn't an option as any battery exchange wouldn't be possible. Furthermore, the use of batteries would limit the possibilities for operation in low temperatures would be more prone to other environmental impacts.

7.4. The Power Management Stage

The section on the power management will address the utilization of the maximum power point and describe theory behind the way cymbals were connected inside the EH tile.

First step in collecting generated power was connecting the cymbals together to a common buffer capacitor. However, the output of the cymbals is an AC signal, therefore, it is necessary to rectify the output before it can be stored.

In Chapter 4 several different approaches have been demonstrated for piezoelectric output rectification. However, these circuits have been made to operate with stable periodic oscillations and not designed for a single pulse operation with an irregular shape. Furthermore, the amount of available energy after one step is performed is in order of millijoule so any potential rectification circuit used would have to be very efficient in order not to consume more energy than it will produce. Furthermore, the buffer capacitor

can be considered empty before each step occurs hence and advanced rectifier requires power for the control circuitry. All these challenges made use of the advanced rectification a very challenging task, therefore, a standard diode bridge was selected. This decision would've been revised if the application couldn't be implemented due to lack of energy.

The next step was determining the approach to connect the cymbal together, in order to charge a single storage capacitor, using a standard diode bridge, as efficient as possible. The following subsection will address this issue.

7.4.1. Connecting Cymbals – Serial vs Parallel

After performing the measurements on the power output of cymbals it can be seen that the output open circuit voltage of the cymbals is in range of 20 to 30V. Therefore, it can be expected that the maximum power point (MPP) will be on one half of the open circuit voltage. This means that the buffer capacitor should be kept as close as possible to the maximum power point voltage in order to maximize the power output.

If we consider connecting the cymbals in series, this would yield the maximum power point voltage of approximately 75V in the case of having 5 cymbals. This was derived under the assumption that all cymbals were the same, and that their maximum power point voltage was 15V for each cymbal. In this case, the energy management stage had to be designed to convert the 75V stored on the capacitor to 3V which is the voltage typically used by sensors and wireless modules. After searching for high efficiency DC/DC converters with the required input voltage rating, it can be easily concluded that conversion from 75V to 3V would be very inefficient. Furthermore, at the time of writing, there weren't any available integrated solutions for low power switching DC/DC converters capable of performing the task. Therefore, connecting the cymbals in series wasn't an option.

On the other hand, connecting them in parallel would result in approximately 15V maximum power point. At this voltage level it was possible to use off the shelf converters while providing high efficiency in energy transfer from the buffer capacitor to the rest of the circuitry. Therefore, it was selected to arrange the cymbals in parallel.

7.5. Defining the Operating Regime

The electronics in the first phase of the development had a simple task of collecting the energy and transmitting a packet once the sufficient amount of energy has been collected during the stepping motion. This is another example of "One-Shot" operation scenario of an energy harvesting system, where the energy management has a task of waiting until there is required energy collected in the buffer. When the required energy level had been reached the

energy management activated the microcontroller and the radio. After transmission was performed the buffer capacitor was depleted and the system was ready for the next step.

There is no low power periods between transmissions hence all generated energy by the step is being used as soon as it is available. Therefore, it can be stated that all energy generated by a person stepping on the tile can be used by the radio. In case of a 71kg person this would be in the range of 0.9mJ.

7.6. The Sensor, Controller and the Communication

Following the energy budget determination the next step was selecting the platform that would be able to perform a wireless transmission using the available power budget. The platform selected was ez430-RF2500 by Texas Instruments [71]. This choice was made because of its low power features, easy availably of the platform and a good software support allowing fast implementation of the system.

The energy consumption required for transmitting one byte packet at 0dBm output power using this platform was measured to be 101.3µJ at 3V. This is in line with the energy requirement for the platform found in literature [100]. With the expected budget of around 1mJ, when a 71kg person is stepping on the tile, it can be assumed that it would be possible to transmit a packet when a step is performed by a lighter person.

7.7. The Capacitor Size Selection

In this application, as stated earlier, there is no need for accumulating energy between transmissions. Therefore, the capacitor buffer size is selected based on the value that would produce the most optimal power output from the cymbals. Based on the measurements done in the energy harvester profiling section of this case study, the buffer capacitor selected was a 10µF ceramic X7R capacitor rated for 25V. This capacitor was chosen due to temperature stability and long lifetime.

7.8. Energy Management

Analysis of the power output of the cymbals, with the 10 µF capacitor used as storage, showed that it was not possible to perform a transmission using the energy available during the stepping on the tile. With the selected 10µF capacitor the amount of stored energy when a 71kg person stepped onto the tile was 100µJ which is border line sufficient for the transmission. Furthermore by waiting to harvest the energy when the stepping off occurs, before the transmission took place, more energy would be collected hence allowing a lighter person to generate enough power for transmission when walking over the tile.

When the step is performed the buffer capacitor could charge to a voltage level that would be outside the operating range of the most MCUs and radios. As a result it was necessary to convert the voltage on the buffer capacitor to the range of 1.8V to 3.6V, which is the common operating voltage range of off the shelf radio modules and MCUs. Typically the conversion is done either by using a linear regulator or a switching DC/DC regulator

The current required by the most microcontrollers and radios isn't affected much by the applied voltage, as was shown in [100] and in the profiling done of the chapter 4. Therefore, the energy required for the MCU and the radio to perform the wireless transmission, with a LDO used for changing the voltage level of the capacitor, can be approximated by the equation:

$$E_{LDO} = tV_{BUF}\left(I_{REQ} + I_{LDO}\right) \tag{5.6}$$

where V_{BUF} is the voltage on the input of the voltage regulator, I_{REQ} – current consumption of the circuit and t – time the circuit is active. E_{LDO} is the amount of energy that will be used from the input storage buffer. The approximation of the energy requirement to perform the task lies in the fact that the change of the current and the voltage as the capacitor is being discharged isn't taken into account. On the other hand, the energy required when a DC/DC converter is used can be expressed as:

$$E_{SW} = \frac{I_{REQ}V_{OUT}t}{\eta} \tag{5.7}$$

where V_{OUT} is the output voltage of the switching converter and η is its efficiency. E_{SW} is the amount of energy that will be used from the storage buffer to perform the task. By dividing E_{SW} and E_{LDO}, under the assumption that the I_{LDO} can be neglected, it can be concluded that the energy requirement of the circuit using a LDO is going to be larger than in the case of using the DC/DC converter. The relation can be expressed using:

$$\frac{E_{LDO}}{E_{SW}} = \frac{V_{BUF}}{V_{OUT}}\eta \tag{5.8}$$

For example, in the case of 14V voltage on the buffer and 80% switching converter efficiency, with 2.5V switching converter output, the implementation with LDO would require 4.5 times more energy compared to switching

converter implementation. Considering the application is very energy restricted such energy loss is unacceptable.

We have decided to use a LTC3129-1 nanowatt buck boost DC/DC converter for the energy management [154]. This was done for two reasons. First the circuit is rated for the voltage range expected on the input buffer capacitor; second this converter has analogue control which can be used for selecting a threshold voltage at which the converter should activate. By applying a voltage level above 1.22V on the analogue control pin, the converter would activate. Therefore, by providing the voltage from the input using a simple resistor divider it was possible to set the activation voltage at a desired input buffer voltage level.

However, this circuit has a narrow input hysteresis so it was necessary to extend it in order to allow the output to use as much energy as possible before the DC/DC converter turns off. This was implemented by connecting a diode and a capacitor to the RUN input of the LTC3129 as show in Fig. 5.16.

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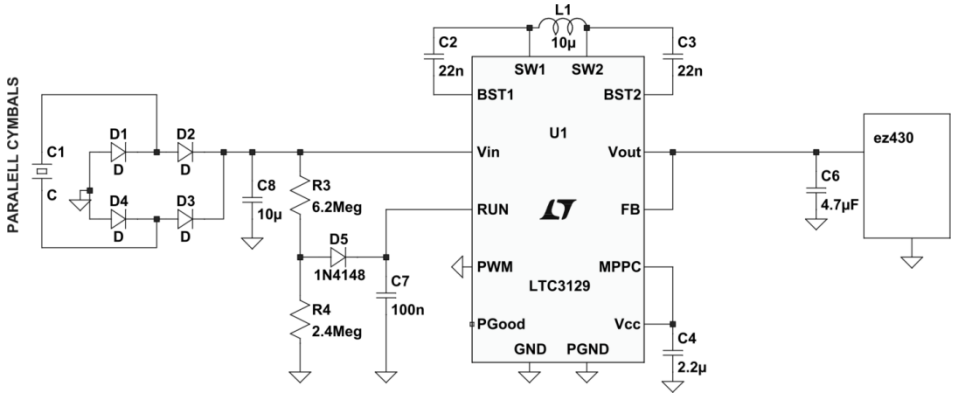

Fig. 5.16 The schematic of the proposed circuitry for transmitting a single packet upon stepping on an energy harvesting tile

The circuit operates as follows: as the voltage on the input capacitor rises, the voltage on the capacitor connected to the RUN pin would also rise, at a rate defined by the voltage divider and the diode voltage drop. When the voltage on the capacitor reaches the threshold voltage of the converter, 1.22V, the converter starts operation. As soon as the converter starts operating the voltage on the input will drop, as the harvester is not capable of supplying sufficient power to prevent this. With the drop of input buffer voltage, if it weren't for the diode D5, the voltage on the RUN pin would reflect the voltage change on the input, leading to disabling the converter once the voltage on this pin reaches 1.11V. However, as the diode is preventing the discharge of the capacitor, the LTC3129-1 continues operation, draining the input capacitor

until it reaches 1.9V, when the LTC3129 enters under-voltage condition and stops powering the output.

Introduction of the diode and the capacitor to the circuitry had a drawback of realizing a low pass filter on the RUN pin. This in turn introduced a delay in response to the changing input. The value of the resistance divider is in megaohm range, in order to reduce the losses during charging. This in turn means that the time constant of the RC network would be in second range, depending on the values of the resistors and capacitor used. This delay could be potentially used to the advantage of the circuit.

Let $V_{THR\text{-}DC/DC}$ be the voltage level required for the input buffer capacitor to reach in order to provide sufficient energy to perform a wireless transmission. This voltage level will be reached, as explained earlier, during the stepping off from the tile. If a person's weight is the same as the minimum weight required for the system to operate, after the person has stepped off, the buffer would reach the required voltage $V_{THR\text{-}DC/DC}$ after the delay introduced by the RC circuit. However, if a person is heavier, the voltage on the input buffer capacitor would continue to rise because of the said delay. In this way more energy will be accumulated in the buffer capacitor before the circuit is activated, hence providing energy for a potential retransmission if the initial transmission were to fail.

7.9. Evaluation of the Energy Neutrality

In the case of one-shot operations that don't have restrictions on the time between transmissions energy neutrality doesn't need to be evaluated as the circuits is going to be activated every time there is sufficient energy.

7.10. Implementation

The output of the LTC3129-1 was selected to be 2.5 V, which was the lowest output voltage setting possible on this converter. It was necessary to select the lowest power output in order to reduce the energy requirement for transmission of data. The required energy for transmission of the packet using ez430-RF2500 at 2.5V was measured to be 77.5 µJ.

Beside the collecting energy required for transmitting the data, is was also necessary to produce energy to for the operation of the LTC3129-1. The DC/DC converter requires energy to start up and charge the capacitors connected to its output before it can power the output circuit. Having that in mind the DC/DC converter's output capacitance was minimized to 4.7 µF. This capacitance was selected as it is the minimum recommended value for the output capacitance based on the datasheet.

The energy required for activation of the DC/DC converter was not specified by the datasheet. Therefore, the minimal energy required for the

circuits operation couldn't be theoretically determined. Therefore, we have selected a threshold voltage of 4.7V, which in current setup can be only reached when a person is stepping off the tile. The delay circuit will provide enough time for the stepping off to finish before the DC/DC converter gets activated, allowing the capacitor to reach the maximum voltage before the transmission takes place.

7.11. Measurements and Discussion

Fig. 5.17 demonstrates the change of the voltage on the input buffer capacitor while performing simulation of a step using a press. The step has been simulated by applying a square pressure using a pneumatic piston.

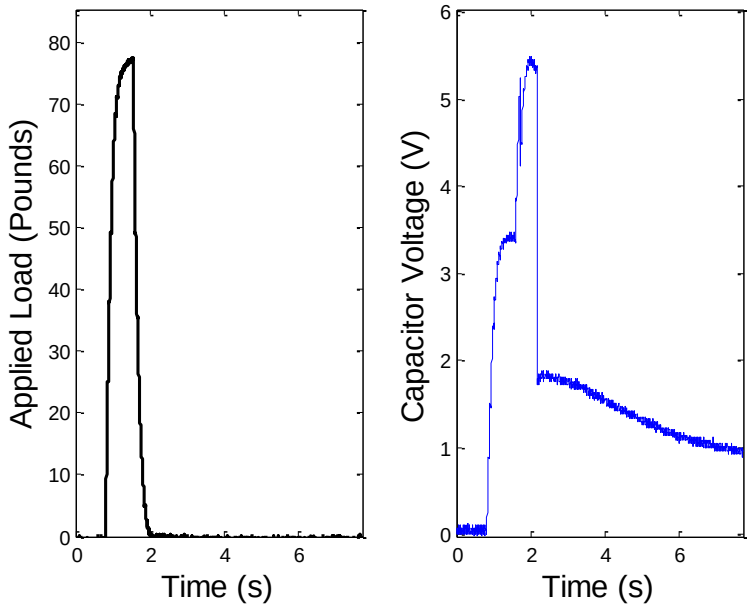

Fig. 5.17 The applied force on the tile and the buffer capacitor voltage as the function of time (courtesy of VirginaTech)

In Fig. 5.17 it can be seen that the transmission has occurred at 5.4V, after the maximum voltage has been reached. During the stepping onto the tile, the buffer capacitor reached 3.4V. When stepping off the tile was performed, the voltage on the buffer capacitor rose above the threshold activating the LTC3129 which then powered the radio transmitted that sent the data out.

The first smaller drop of voltage is coming from the LTC3129 activating procedure. It can be seen that the system didn't get activated when the maximum voltage was reached but after a time delay. The delay is coming

from the RC network connected to the RUN pin. Only when the RUN pin has reached the activation voltage of the DC/DC converter, the transfer of energy from the buffer capacitor to the ez430-RF2500 begins.

The minimum weight required to perform a successful transmission at maximum power output of the radio of 0dBm was 36.8kg. From the measurement it was determined that the actual energy budget required for performing the wireless transmission was 127µJ instead of 77.546µJ This indicates that the DC/DC stage was less than 80% efficient. The actual measured efficiency of the DC/DC converter was 64%.

This circuit has a limitation that it cannot detect the direction of the stepping onto the tile as the ez430 is unpowered until the step is almost over. Furthermore, an issue with repeated steps has been observed, where the circuit would not operate properly if the input buffer wasn't discharged before the next step occurred. It was imperative to discharge the input buffer between steps and hence restart the microcontroller located on the EZ430 board. In the cases where the microcontroller didn't get restarted, and the next step occurred, there was no mechanic to signal to the microcontroller that a new step has occurred hence MCU didn't send a new packet indicating the new step.

These limitations have been removed in Phase 2 of the project by introducing new circuitry to the design. The next section will address this phase in detail.

8. Phase 2

Phase two of the project was aimed at expanding the functionality of the circuit in order to perform step direction detection and remove the shortcomings of the circuit explained in Phase 1.

Although Phase 2 was not completed at the time of writing the thesis, it was included as it demonstrates two novel approaches to managing the energy in low power piezoelectric powered systems. First approach was managing the power output of the piezoelectric floor harvester in a way that allows direction sensing and collecting energy for transmission of collected data during a single step on the floor tile. Second approach was reducing the static power consumption of a stage required for retaining the measured data between the stepping onto the tile and stepping off the tile, when the transmission of the data takes place.

The description of Phase 2 will be focused on changes implemented to Phase 1 circuit. The stepping direction detection and the energy management part will be explained in detail. The last difference in hardware design was the change of the radio used for communication. The ez430 platform was

abandoned in order to increase the flexibility and the range of the system. The design choice to change the radio will be explained in a separate subsection.

8.1. The Stepping Direction Detection

The application requires the device to be able to detect the direction of a person stepping onto it. The idea was to use the cymbals as both sensors and generators hence removing a need for any additional sensing elements.

In order to determine the best solution for step detection, a set of measurements had been performed with a person stepping on the EH tile from four different directions. The results from stepping on the tile from four directions by a 71kg person are shown in Fig. 5.18.

The measurements were taken using DAQ is NI9221, with all cymbals connected to a common ground. It was expected that stepping motion was going to produce a varying response from the EH tile, as a step cannot be replicated in the exact same way when a person was walking. The response would depend on the weight of the person, their speed of walking, the magnitude of impact on the floor and where exactly the person stepped on the EH tile.

Performing analysis of the shape of the output signal of individual cymbals would provide the most accurate information on the stepping direction. However, performing such a task would require a significant amount of energy in order to digitalize the signal and process it. This approach couldn't be implemented mainly because the amount of energy available from a single step.

As a solution we have turned to measuring the delay that occurs between the heel contacts the EH tile until the foot comes to a rest on the surface of the tile. The tile has cymbals placed in the corners so there was a delay in the activation of the cymbals closer to the heel compared to activating and the cymbals closer to the toes. The average time delay between activations was 53ms, with the shortest measured time of 40ms. This delay was occurring on every step making it a good candidate for stepping direction detection.

Detecting which cymbals got activated when the foot made first contact with the floor was made by measuring the voltage on the output of individual cymbals. In order to prevent the mutual influence of the cymbals, each cymbal has a separated bridge used for rectification of its output. The diode bridge would prevent activated cymbals from charging the output capacitance of the inactive ones.

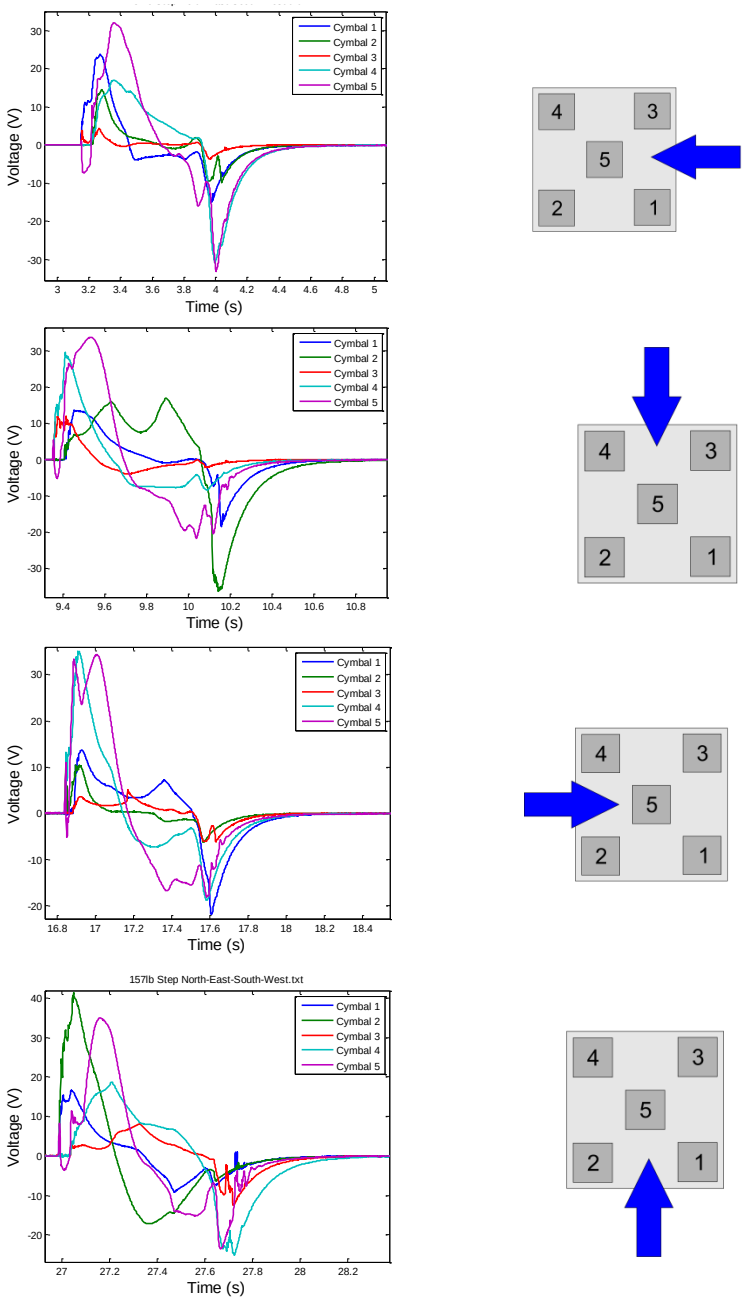

Fig. 5.18 The response of the individual cymbals when stepping from four different directions on the floor tile. Stepping direction indicated by the blue arrow (courtesy of VirginiaTech)

8.2. The Energy Management

The proposed approach to determining the stepping direction based on the initial delay between the heel contacting the floor and the rest of the foot imposes two challenges on the energy management circuit:

(i) Providing sufficient power for performing the measurement of cymbal output voltages as soon as the foot contacts the ground

(ii) Storing the data until the stepping off the tile is performed leading to transmission of the data

These two challenges are contradictory. The first challenge would benefit from as small buffer capacitor as possible in order to provide a fast start-up of the microcontroller due to the fact that on the beginning of the step the input capacitor is empty. The second challenge, on the other hand requires a larger capacitor in order to provide sufficient energy for keeping the information on the direction before a transmission of the data can take place upon stepping off the tile. A large capacitor would require a longer amount of time to reach the minimum operating voltage for the microcontroller. This would result in the microcontroller failing to start in time to detect which cymbals got activated and in turn sense the stepping direction.

An optimal capacitance was selected by choosing the value that will allow the capacitor to charge to 3.6V in under 40ms. This was the time measured between activation of the closer and further pair of the cymbals. The value was determined based on the power output measurements of the cymbals in Phase 1. This resulted in a 1µF capacitor.

In order to verify the feasibility of the approach cymbals were connected to a 1µF capacitor and voltage was monitored on every cymbal individually. The measurements were made by having a person walk over the tile. The results from the measurements are shown in Fig. 5.19.

Analysis of Fig. 5.19 indicate that it can be easily determined that the two cymbals that got activated first were the pair of cymbals closest to spot where the foot made first contact with the floor. The further pair of cymbals was, in this case, activated 80ms later. Furthermore this experiment has demonstrated that by connecting a 1µF capacitor to the output of the cymbals, it was possible to reach the operating voltage of a microcontroller in less than 15ms.

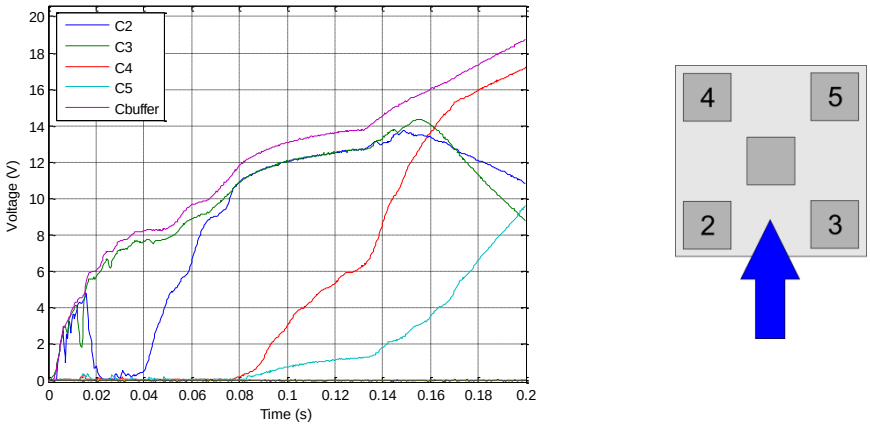

Fig. 5.19 The output of the cymbals and voltage on a buffer capacitor as a result of stepping onto the tile (courtesy of VirginiaTech)

Once the set threshold of 3.6V was reached the microcontroller could perform the measurement of the voltages on the cymbals. The energy required for performing 4 AD conversions on the MSP430G2553 used in this application was measured to be 314nJ at 3.6V. At this point in time the useable energy stored in a capacitor was 4.86µJ. Under useable energy is considered energy on the disposal of the MCU between the voltage levels of 3.6V and 1.8V. The limitation is coming from the fact that under 1.8V the MCU will stop operating and the measurement data would be lost. The residual energy in the buffer capacitor is used to maintain the RAM of the MCU, thus keeping the measurement data.

After the direction measurement was performed it was necessary to store the rest of the energy in a larger capacitor as the 1µF would fast charge beyond the maximum power point and cannot store sufficient energy for performing a transmission. As explained in the Phase 1 energy harvester profiling section, the optimal capacitance to be used was 10µF. Therefore, it was necessary to connect an additional capacitance to in parallel the buffer, once the measurement was performed, in order to maximize the amount of collected energy.

The detailed operation of the entire circuit operation is explained in the theory of operation section.

8.3. Transceiver Choice

The original transceiver used in phase 1 was a CC2500 by Texas Instruments [70] which is the transceiver located on the ez430-RF2500 board. However, this radio is operating at 2.4GHz radio and at 0dBm power it wasn't able to cover the area required by the application. In order to extend the range of the transmission we have chosen to use a sub-GHz radio instead. The radio chosen was MRF89X by Microchip [65], as it is low power, has a good link budget and was available as a module reducing the cost and time for implementation

8.4. Theory of Operation

The block diagram of the circuit is presented in Fig. 5.20. The block diagram is presented in order to demonstrate the interconnection between different parts of the schematic. The full schematic is shown in Appendix C

The behavior of the circuit will be explained on one full operation cycle performed during one step onto the tile. The operation of the circuit is summarized in the flowchart shown in Fig. 5.21.

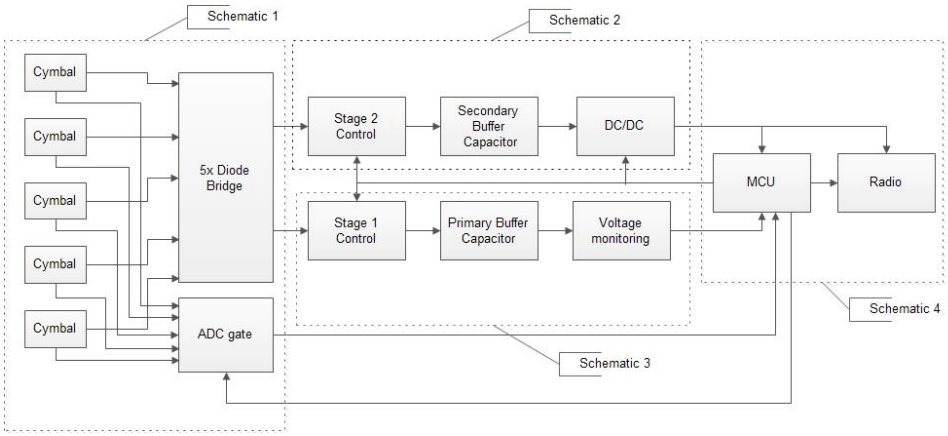

Fig. 5.20 The block diagram of Phase 2 floor tile harvester

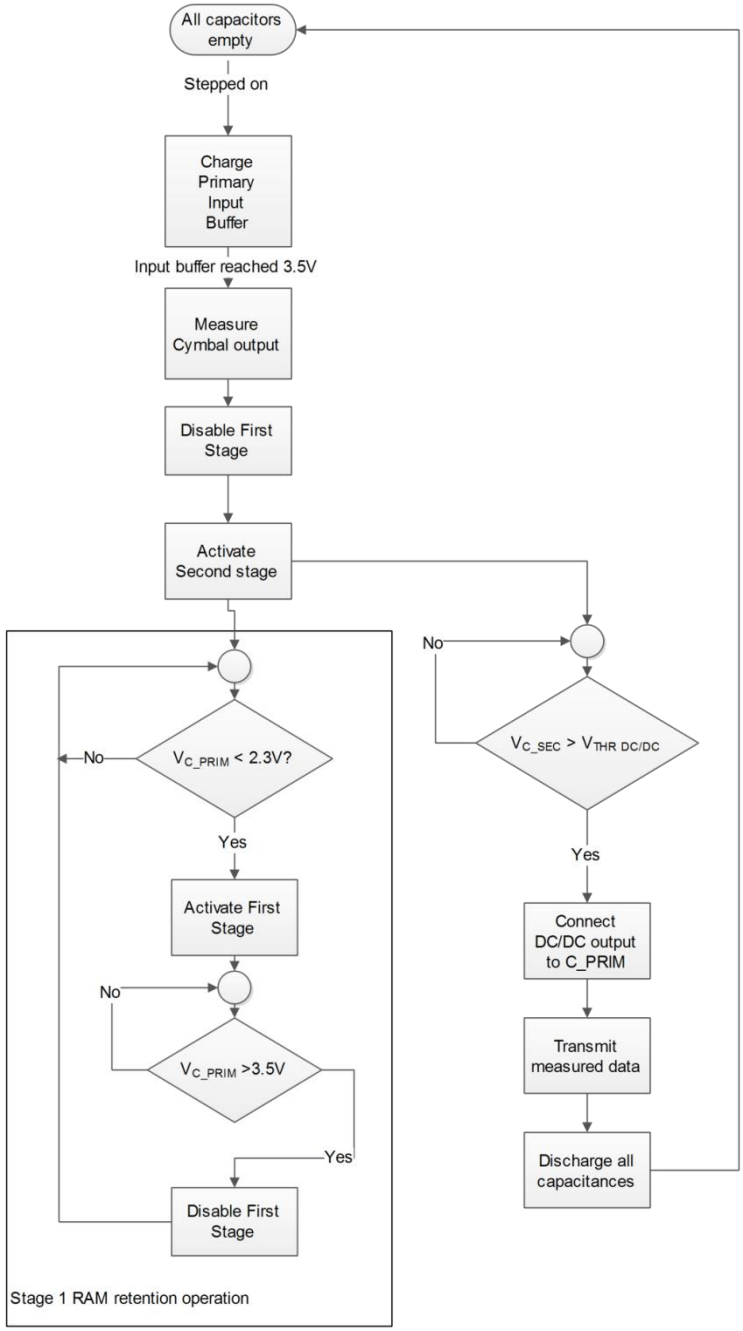

Fig. 5.21 The flowchart of the energy harvesting tile Phase 2 electronics operation

The circuit operation can be divided into three separate stages:

- Stepping on stage
- Waiting stage
- Stepping off stage

The behavior of the circuit throughout the stages can be explained by analyzing the voltage level change on the primary and the secondary buffer capacitors, as well as on the output of the cymbals.

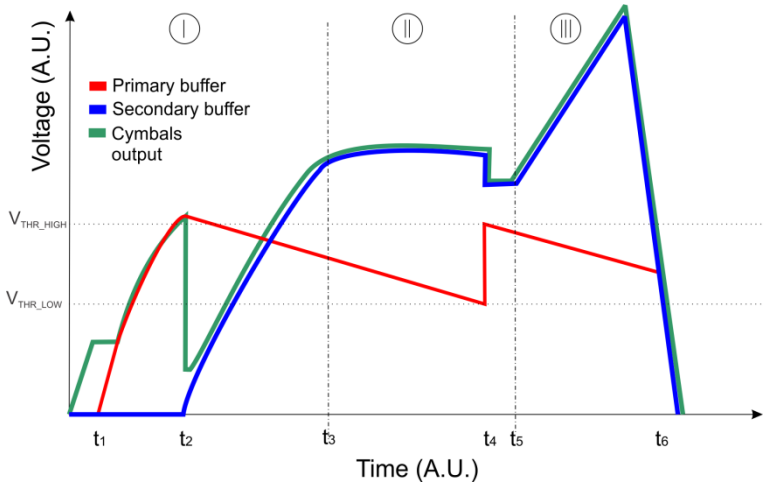

Fig. 5.22 The three stages of the EH tile circuit operation depicted through the voltages on the primary buffer capacitor, secondary buffer capacitor and cymbal output. The three operation stages are marked with numbers: I – stepping on stage, II – waiting stage and III – stepping off stage

8.4.1. First Stage – Stepping on the EH Tile

The first stage begins with all capacitors in the circuit empty. All cymbals are connected to their respective diode voltage bridges in a way that all of them, when strained, produce output voltage in the same phase. As the stepping begins, the voltage output of the two cymbals that are stepped on first rises. This action charges the output capacitance of the cymbals leading to powering up the stage one control circuit and stage two control circuits. In the beginning the stage two is disconnected while the stage one circuitry is connected. This leads to beginning of the charging process of the primary buffer at time t_1. In the next period the primary buffer capacitor is being charged to time t_2 when the voltage on the primary capacitor reaches V_{THR_HIGH}. At this point the microcontroller gets activated.

Upon activation the MCU is performing the measurement of the voltage levels on the outputs of cymbals. Based on the fact that all cymbals are

strained in phase the two cymbals that have the voltage close to the supply voltage of the MCU are the two that got activated first. This data is stored in the MCU's RAM and then the primary buffer gets disconnected from the cymbals' output. Next step is to reroute the power output of the cymbals to the secondary buffer capacitor. This can be seen in Fig. 5.22 as a sharp voltage drop on the output of the cymbals followed by the rise of the secondary buffer's voltage. During the charging process of the secondary buffer, the MCU is using the energy stored in the primary buffer to retain the content of the RAM, hence storing the values of the measurements until sufficient energy for the transmission is stored in the primary capacitor.

Once the process of stepping onto the tile is finished, the system enters the next stage where the system is waiting for the person to step off the tile.

8.4.2. Second Stage – Waiting for Stepping off the EH Tile

During this stage no power is being generated from the cymbals and the system is waiting for the person to step off the tile. While waiting for this to occur the MCU is consuming the power stored in the primary buffer storage to maintain its RAM content. This is necessary as the information of the stepping direction is kept inside the RAM.

If the person is standing for an extended period of time on the tile the primary buffer capacitor is going to get depleted by the electronics it is supplying mainly due to its small size. If this occurs it is necessary to recharge the primary buffer storage in order to avoid data loss from the MCU's RAM. Therefore, a voltage monitoring circuit is supervising the voltage on the primary buffer capacitor. Once the voltage on the primary buffer capacitor reaches the V_{THR_LOW} level, a connection between the primary buffer capacitor and the secondary buffer capacitor is established. The primary buffer capacitor is then recharged from the secondary buffer capacitor. Once the primary buffer capacitor reaches the V_{THR_HIGH} the recharging is complete and done the primary buffer capacitor gets disconnected.

The system remains in this stage until either both the primary and secondary buffer capacitors get discharged, or the person begins to step off the tile, thus transitioning the system into the third stage of operation.

8.4.3. Third Stage – Stepping off the EH Tile

As the stepping off begins the power is generated by the cymbals. Therefore, the charging continues leading to activation of the DC/DC converter when its threshold is reached. The DC/DC converter is the same as used in the Phase 1 of the project, therefore, its operation is not going to be discussed in detail. The only difference is in the fact that the output of the DC/DC converter isn't directly connected to the MCU. There is a transistor in between.

The transistor is placed in order to prevent the charging of the output capacitance of the DC/DC converter during the stepping on stage of the circuit operation. The minimal recommended output capacitance of the used DC/DC converter is 4.7µF which is significantly larger than the 1µF primary buffer capacitor.

Once the DC/DC converter is active, it signals the MCU when the output is stable. Then the MCU activates the MOSFET that connects the primary input buffer to the output of the DC/DC stage and transmits the measured voltage levels of cymbals wirelessly to the base station.

After the transmission is done, all capacitances in the circuit are being depleted in order to bring the circuit to a stable, known state before the next step occurs.

8.5. Reduction of the Static Power Consumption

The most critical aspect of the implementation was reducing the power consumption of the primary stage during the delay between stepping on and stepping off hence prolonging the amount of time RAM of the MCU could be retained and with it the cymbal measurement results. The static power consumption was reduced by implementing multiple functionalities on the same hardware and by removing the resistors used for stabilization of high impedance lines.

The components powered from the primary buffer capacitor during the waiting stage are: the MCU and the primary buffer voltage monitoring circuit. The MCU is measured to consume about 120-150 nA, depending on the supply voltage, when operated in data retention power saving mode. On the other hand the voltage monitoring required analogue circuits and resistor networks that increased the power consumption of the stage. Furthermore the voltage monitoring circuit required two thresholds, one for activating the MCU and one for detecting when the primary buffer capacitor was being depleted.

The threshold voltage is controlled by the MCU through control of the value of the resistor network on the input of the comparator. Simply by activating and deactivating a switch realized using ADG802 it was possible to connect an additional resistor, thus changing the voltage level on the positive input pin of the LTC1540. This is shown in Fig. 5.23.

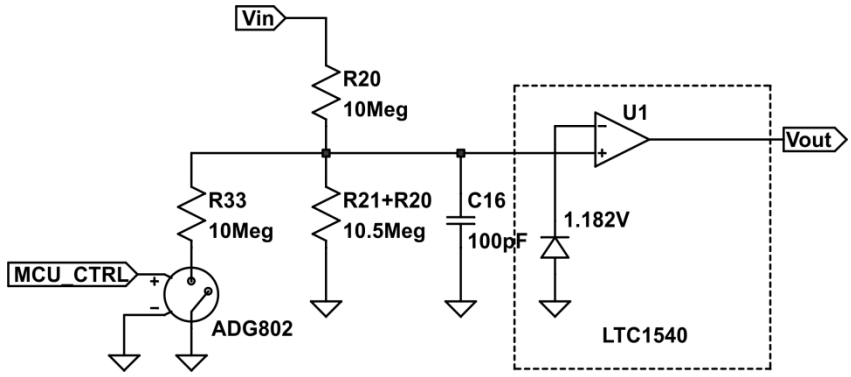

Fig. 5.23 Control circuitry for threshold voltage selection in the voltage monitoring block

During the startup the MCU_CTLR line is at ground level allowing the ADG802 to conduct, thus setting the input voltage to 3.5V. When the MCU_CTLR line is driven to the supply voltage level, the resistor R33 gets disconnected and the threshold voltage becomes 2.3V.

The upper threshold voltage is set to 3.5V in order to prevent overshooting the 3.6V, which is the maximum operating voltage level, during the recharging of the primary buffer capacitor in the waiting stage. The potential overshoot might come from the delay of the LTC1540 introduced by the R_1C_1 circuit connected to the input of the comparator.

Although there is a series connection between the ADG802 and the resistance their placement is important. This is coming from the fact that the input capacitance of the ADG802 circuit will change when the circuit changes the state of the internal switch from active to inactive. As the capacitance changes it needs to be recharged. This is happening at the expense of the energy stored in the filtering 100pF capacitor attached to the pin. This would result in an immediate reduction of the voltage on the line, followed by the comparator changing its output state. Increasing the value of C_1 wasn't an option because that would increase the delay between the V_{in} reaching the threshold voltage and the actual change of the LTC1540 output state leading to an overshoot on the monitored voltage line.

There was one more additional aspect that contributed significantly to the overall current consumption. Those were the resistors used to prevent the transistors' gates and other high impedance inputs from having unknown voltage level during the period the MCU was unpowered. The most critical were two transistors controlling the connection between the cymbals and the two buffer capacitors. Even if a 22MΩ resistor were to be used for connecting the signal lines to the ground potential, at 3.6V, the current consumption

would be 160nA per resistor. This block requires in total four resistors for all critical lines to be stabilized, hence the current running through the resistors alone would be 640nA. This current consumption is higher than the current consumption of the MCU in low power mode of operation and LTC1540 combined.

In order to eliminate the resistors I am proposing use of small value capacitors instead. In power electronics it is a well-known fact that use of capacitors in gate of MOSFET transistor can prevent them from activating due to dV/dt effects.

The size of the capacitance that is required to stabilize the high impedance line depends on the size of the parasitic capacitances of the transistor used. For the FDV301 transistors and on the input of ADG802 a value of 1nF has been experimentally chosen. The total energy required for charging a 1nF capacitor to 3.5V was 12.25nJ. Let's assume that a period between stepping on and stepping off from the tile lasts 0.3s. It can be calculated that the equivalent resistance, which would dissipate the same amount of energy in this period of time, as needs to be stored in the capacitor, would be close to 300MΩ. This resistance value didn't provide stable operation of the circuit when used in the gate circuit. This demonstrated that the use of the capacitors instead of resistors would be beneficial, especially in the case of long periods between stepping on and stepping off the floor tile.

Furthermore, in this application, during startup the MCU is connected to the power source so the energy used to charge the capacitors is coming from the source, not from the primary buffer capacitor as is in the case with the resistor realization. Thus the capacitor approach has this additional benefit of not using energy during the waiting stage of operation.

8.6. Measurements and Discussion

At the moment of designing and testing the circuits the actual tile wasn't available for testing therefore, the output of the tile was simulated. The stepping motion on the tile results in a complex response of the cymbal elements depending on the speed of the step, direction, the way force is distributed, etc. Therefore, exact simulation of the output would require a complex setup. For this test the output of the tile was approximated with a voltage source that was controlled using two MOSFET switches. The setup is shown in Fig. 5.24.

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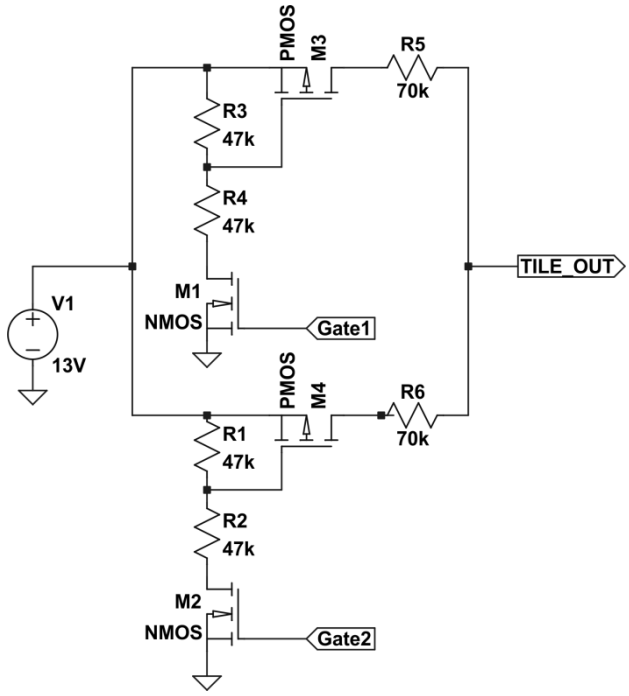

Fig. 5.24 The setup used for simulating the step response of the floor tile

Each gate represents a pair of cymbals. In this way it was possible to simulate the delay in stepping onto the tile. First gate would be activated 50ms before the second gate hence simulating the stepping delay. The total duration of the stepping on signal was 150 ms, followed by the idle time, which correspondents to the foot resting on the floor, in duration of 300 ms. The stepping off was simulated with a 150 ms pulse as well.

The values for the power supply and the resistances have been chosen to simulate the output of the cymbal in case of a 43 kg of applied to the tile. The supply was chosen to be 13V while the resistance values were 70 kΩ.

The control signals as well as the voltage change on a 1 0µF capacitor using the setup discussed are shown in Fig. 5.25.

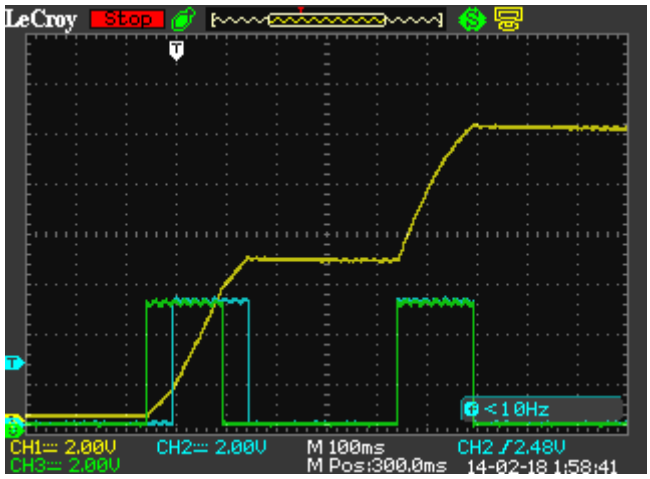

Fig. 5.25 Simulated response of the energy harvesting tile; gate control signals (blue and green) voltage on the 10µF capacitor

After the tile simulation hardware was realized the series of the suggested hardware for Phase 2 was tested. Fig. 5.26 demonstrates change of voltage levels in the circuit during one simulated stepping action.

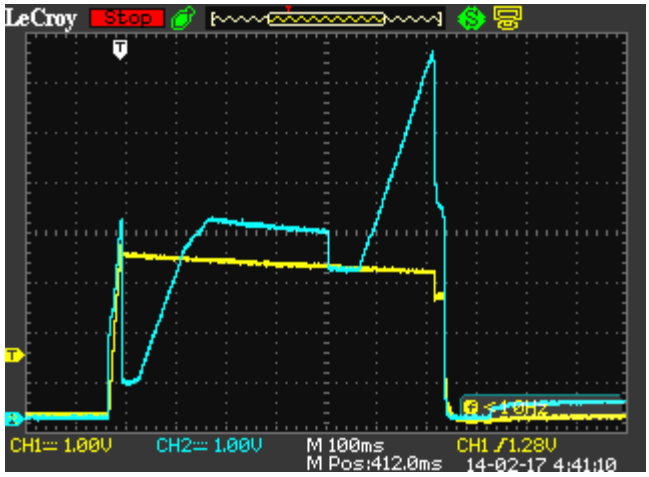

Fig. 5.26 The voltage levels on the combined output of cymbals (blue) and voltage on the primary buffer (yellow)

In the same way as explained in the theory of operation section of the circuit, three stages can be identified in the overall circuit operation. The first, stepping on stage, stage can be easily identified by a spike followed by the

charging of the primary buffer. The second stage is following where the circuitry is waiting for the stepping off motion. The drop in voltage that can be seen during the second stage is coming from the DC/DC stage powering up the control circuit. The third stage begins with continuation of the charging of secondary buffer capacitor and ends with the sharp voltage drop that is the result of the MCU activating and performing a wireless transmission. The operation of all stages will be now explained in more detail.

The startup phase begins when the force applied to the tile. As there is no additional capacitive load on the output of the cymbals the output voltage rises fast as can be seen in Fig. 5.27.

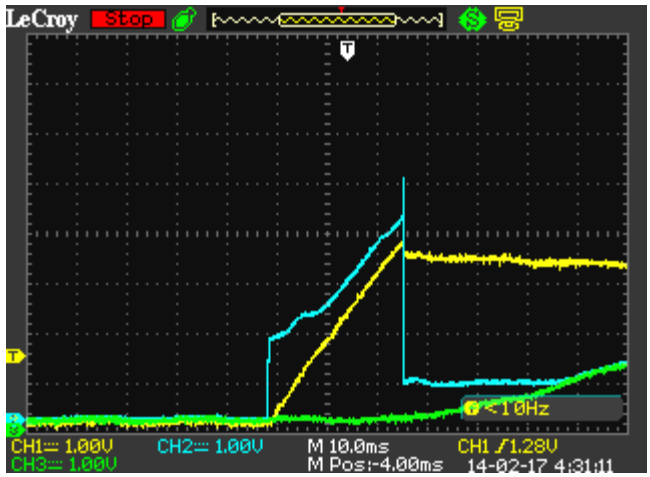

Fig. 5.27 The startup stage of the circuit; The combined output of the cymbals (blue), voltage on the primary buffer capacitor (yellow), voltage on the secondary buffer capacitor (green)

The threshold voltage of the LTC1540 of 3.5V was reached in 32ms. This was important to demonstrate as the stepping direction detection has to be performed before the second pair of cymbals is activated. Upon reaching the threshold voltage the MCU performed the ADC measurement and stores the information in its RAM. The energy required for this operation was measured to be 618nJ.

After the measurement was performed the primary stage was disconnected, which can be seen as a spike on the combined output of the cymbals. Following disconnection of the primary stage the secondary stage was activated resulting in the sharp voltage drop of the combined cymbal line to approximately 1V, which is equal to the threshold voltage of the PMOS gate used to connect the secondary stage to the output of the cymbals. From this

moment on, the secondary stage is being charged from the cymbal output and the system enters the waiting stage.

The static power consumption was minimized using the optimization techniques presented earlier in this section. The current consumption of the elements powered by the primary buffer capacitor is summarized in the Table 5.2. The values have been obtained based on the datasheets of the components and expected average voltage level of 2.9V. This voltage level was selected as the average voltage between the two thresholds of the primary buffer voltage monitoring circuit.

Table 5.2 The current consumption breakdown of the primary stage

Element	*Contributor*	*Average Current Consumption (nA)*
Comparator Threshold	20.5 MΩ	141.46
Comparator Hysteresis	4.6 MΩ	256.96
MCU in data retention	MSP430	120*
Comparator	LTC1540	280*
Sum of Current Consumption		798.42

*) Typical current consumption at 3V from component's datasheet

During the waiting stage, based on Fig. 5.26, the primary buffer capacitor of 910nF got discharged from 3.3V down to 2.95V. From the graph it can be seen that the voltage was changing linearly indicating a near constant current discharge, therefore, the average current was calculated using equation:

$$C = \frac{I\Delta t}{\Delta U} \tag{5.9}$$

,where C is the primary buffer capacitance, Δt – duration of the waiting phase and ΔU the change of the voltage on the primary buffer capacitor. The average current consumption was calculated to be 511nA. The difference between the predicted average current consumption from the Table 5.2 and the measured current consumption is mainly attributed to the use of typical values for current consumption estimation in the table and nominal resistor values.

During the waiting stage the MCU must retain the content of its RAM until the person steppes off the EH tile, even if the step takes longer than predicted 0.6s. based on typical human gait. This is done by recharging the primary stage from the secondary stage when the voltage on the primary buffer drops below 2.3V. The process of recharging can be seen in the Fig. 5.28 where a 1MΩ oscilloscope probe was attached to the primary buffer. This resulted in an increased rate of discharge and the primary buffer had to be recharged.

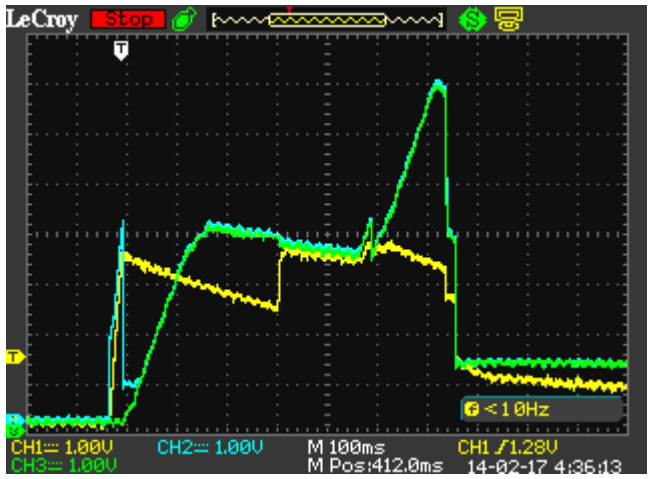

Fig. 5.28 Behavior of the circuit under the increased load condition on the primary buffer; combined output of the cymbals (blue); secondary buffer (green), primary buffer (yellow)

Due to increased load applied to the primary buffer, it depletes to 2.3V before the stepping off occured. In order to prevent the buffer from falling under the MCU's RAM retention voltage, the MCU activates connects the primary buffer capacitor to the secondary buffer capacitor.

If the secondary buffer did not reach the 3.5V level during the stepping on phase, then two buffers remain connected allowing the MCU to utilize the power from the secondary buffer in order to maintain the RAM content. As soon as the stepping off begins, the primary buffer is recharged to 3.5V followed by the disconnection of the primary buffer capacitor from the secondary buffer capacitor. The secondary buffer capacitor then charges further, using the energy generated by the stepping off from the tile. When the threshold of the DC/DC converter is reached, the DC/DC converter is activated and the MCU transmits the data wirelessly.

The voltage level waveform of buffer capacitors during transmission and output voltage of the DC/DC converter are shown in Fig. 5.29.

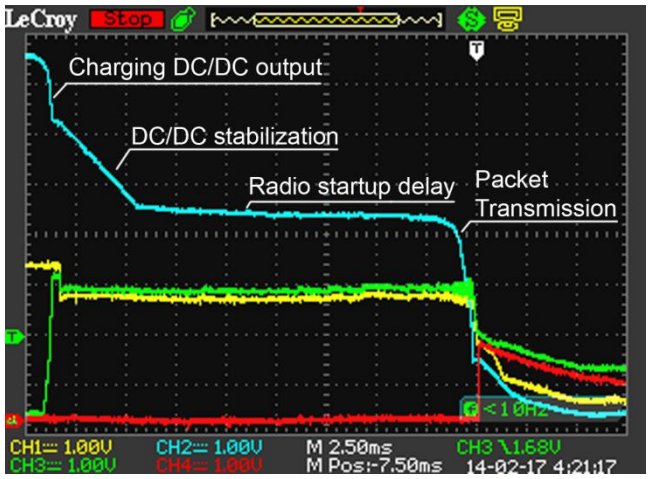

Fig. 5.29 Voltage levels in the circuit during the transmission – the secondary buffer capacitor voltage (blue), the primary buffer voltage (yellow), the output of the DC/DC converter (green)

From the operation of the circuit during transmission of the packet the efficiency of the DC/DC converter can be determined. When the threshold voltage required for activation of the DC/DC converter has been reached, far left side in Fig. 5.29, the DC/DC converter is charging its output capacitance to 2.5V. While charging the 4.7µF output capacitance, the secondary buffer capacitor of 9.3µF discharges from 7.3V down to 5.98V. This results in 81µJ of invested energy in order to store 14.69µJ in the DC/DC output capacitor. This yielded an efficiency of 18.1%. Such low efficiency can be explained by the starting up of the internal circuitry of the DC/DC converter and having a capacitive load connected to its output.

When the output voltage of the DC/DC converter stabilizes at 2.5V the DC/DC converter sets its power good output to high voltage level indicating to the microcontroller that the DC/DC convertor is ready. The primary buffer capacitor is then connected to the output of the DC/DC converter. This can be seen in Fig. 5.29 as an abrupt change of voltage on the yellow signal line, following the rise of the voltage on the green line, which is the output of the DC/DC converter.

After 4.3ms since the starting of the DC/DC converter it had been stabilized. Energy required by the DC/DC to finish the startup was measured to be 84.26 µJ. This stabilization time was not documented and didn't show up in the simulation. However, it was observed even when a circuit only had the DC/DC converter running, indicating that the DC/DC converter was the cause of the energy consumption.

After the DC/DC converter has reached a stable mode of operation, following was waiting for the radio module and start up. After the startup, the data on cymbal voltage during stepping on was transmitted wirelessly. Total energy requirement for transmitting the 8 bytes of data at 200kbs with 1dBm power output was measured to be 52.5μJ. From the measurements it can be seen that the secondary buffer capacitor got discharged from 4.2V down to 1.9V resulting in 65.23μJ energy input to the DC/DC converter. Based on this result the efficiency of the DC/DC conversion was calculated to be 80.5% during stable operation. This value is in line with the expected efficiency of the LTC3129-1 based on its datasheet.

After the transmission was completed the signal for discharging the input capacitances was sent from the microcontroller. This can be seen in Fig. 5.29 as the red signal line.

By analyzing the energy consumption it is easy to realize that the majority of energy has been used by the DC/DC converter to start up. The power consumption distribution is shown as a chart in Fig. 5.30.

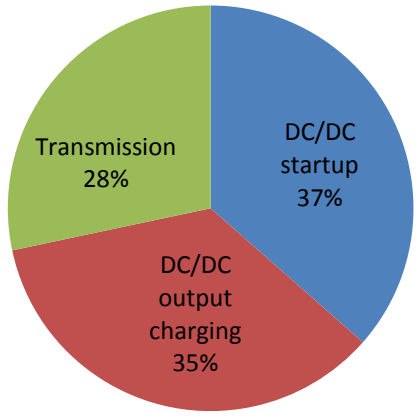

Fig. 5.30 The distribution of the energy use during one activation in order to transmit the data

It can be easily concluded that the operation of the DC/DC stage needs to be optimized in order to increase the overall system efficiency. Current configuration is utilizing only 28% of the collected energy for performing the transmission.

A comparison can be made to Phase 1 circuitry that was aimed to be activated only when there was sufficient energy. The same DC/DC converter was used, however, in Phase 1 the entire process of starting up and sending the

data took only 3.8ms. Consequently, the DC/DC stage didn't have time to finish the startup phase hence reducing the energy consumption of the DC/DC.

The measurement of the circuit performance on the actual energy harvesting tile is ongoing during the wiring of the thesis and will be included in future publications.

8.7. Future Work

First and foremost is the verification of the circuit operation on the energy harvesting floor tile. Next step is aimed at optimization of the DC/DC converter. Primary focus would be on the losses occurring during the DC/DC starting up.

One possible approach to increase the efficiency of the startup would be to charge the output capacitor of the DC/DC converter using the primary buffer capacitor by attaching a high value resistor between them. By using this approach it will be possible to pre-charge the output of the DC/DC stage hence allowing more efficient activation. The higher efficiency of activation in such case is coming from the fact that the difference of voltage between the input and the output would be smaller hence reducing the startup energy consumption.

Another approach that will be looked into is using FRAM to store the data between stepping on and stepping off. The FRAM is a nonvolatile memory element with a number of write cycles in the order of 10^{14}. If we assume a typical lifetime of a piezoelectric element is 10^{10} [99] the FRAM module would be able to operate through the entire lifetime of the piezoelectric element with even several read-write cycles per step. Use of the FRAM would eliminate the problem of data retention during the time a person is standing on the tile. Stepping on could be potentially distinguished from stepping off by the fact that during stepping off all sampling capacitors would be on -0.3V. Hence after the sampling is done when he MCU gets reactivated during the stepping off it would be easy to determine that the FRAM should be read and data transmitted.

8.8. Summary

In this section occupancy detection system has been developed that was aimed at collecting energy from the force a person induces on the floor when walking. The energy collected was used to wirelessly transmit information on the direction of the person walking. The energy generating element used in the floor tile was used for both energy generation and as a sensing element. This section has demonstrated an approach to dynamically change the storage attached to the generator in order to maximize the power output and perform

a fast start up. Also a concept for minimizing the static power consumption of the energy management stage has also been investigated.

9. Conclusion

The main goal of this chapter was to introduce a design methodology for implementing energy harvesting powered wireless senor nodes. In the beginning of the chapter an iterative design process was described that took the designer from selecting the energy harvesting sources through all steps required to design and implement an energy harvesting powered wireless sensor node on a high abstraction level.

The proposed methodology was used in realization of two case studies aimed at building automation.

In the first case study, following the methodology described, a solar powered wireless sensor node for temperature and humidity sensing was realized. The current consumption of the realized node while operating at 2.7V was 55 nA. Such low operating current would allow the system to operate at light levels down to 2 lux.

The second case study was separated into two phases. In the first phase the occupancy detection was performed by detecting a person stepping on a specially designed energy harvesting floor tile. Every time a person would step on the tile a wireless signal was transmitted indicating the step to the base station receiving the signal. In the second phase of the case study the functionality of the energy harvesting tile was extended by adding direction sensing. In this way the functionality of the system got extended as the information of the direction would allow more advanced automation algorithms to be employed.

As a final result it can be concluded that the proposed methodology successfully guided the design process for both case studies from the application requirement to the system implementation.

Chapter 6

Conclusions

The need for sensing applications has increased in a broad range of fields, spanning from personal health monitoring to industrial process monitoring. This has created opportunities for wireless sensor network (WSN) applications. WSNs carry the potential for easy deployment without the need for additional cabling, low cost and low maintenance. This makes them a very attractive for implementing solution for monitoring tasks. Typically the wireless sensor nodes are powered by batteries. However, the batteries have a limited amount of energy available, thus putting a hard limit on the lifetime of the node. When the batteries deplete, the task of replacing them can be difficult, especially if the nodes are deployed in hard to reach or hazardous environments. Furthermore, in the case of large scale deployments, disposing of batteries can have a major environmental impact. Therefore, a new approach was needed to extend the lifetime of the sensor network. This dissertation addressed the challenges of designing and implementing wireless sensor nodes that are powered by the energy available in the nodes immediate surroundings, by describing a structured methodology which can aid in node's realization.

The advancements in low power electronics have reduced the energy requirement for performing a task of sensing and transmitting the data to millijoule and microjoule levels. This has been verified through the profiling of several types of microcontrollers in Chapter 4. and through the review of low power communication protocols in Chapter 2. The advancements in sensor technologies are also allowing for low power sensing to take place.

With the power consumption reduced, it becomes possible to power the wireless sensor nodes using the energy collected from the environment. The energy harvesting technologies presented in Chapter 3. can be used for converting solar and kinetic energy into electrical power that can be used by the wireless sensor node. In order to improve the power output of the harvester and adjust its output to meet the requirements of the rest of the circuit additional circuitry is often needed. These circuits have been presented in Chapter 3.

In applications involving slowly evolving phenomena, such as some cases of the environmental monitoring, high data rates aren't necessary. Therefore, the time intervals between individual measurements can be raised to minutes, hours or days. If the energy requirement for a single measurement is in millijoule range, with a long delay between measurements, then the average power requirement would be in nanowatt range. In order to utilize such low power levels, a new method has been developed and presented in Chapter 4. This method dramatically reduces the static power consumption which is crucial when the power sources are in the range of nanowatt and microwatt. The power levels achieved using this method have surpassed all previously reported work in the domain of discreet component based energy management.

In order to reduce the complexity of the design and implementation task of an EH-WSN, a design methodology was proposed in Chapter 5. This methodology describes a process to realize an EH-WSN node.

Two case studies in the field of building automation have been realized by following the suggested design methodology. These case studies, besides illustrating the use of the methodology, were also used to demonstrate novel power reduction techniques that ultimately played a key role in the realization of each of the case studies.

In conclusion this dissertation demonstrates that energy harvesting is a viable power source for wireless sensor networks. Although energy harvesting adds complexity to the wireless sensor network design, it removes the need for batteries, thus opening new application possibilities.

The future work in the field of nanowatt energy management, based on proposed ADC energy management, is aimed at developing algorithms for adapting the duration of the interval between evaluations of the buffer voltage. In this way, it will become possible to adapt the wake up period in order to

reach lower power requirements for the energy management stage, without influencing the monitoring efficiency.

The future work in the methodology could consist of developing methods for optimal implementation of sensor nodes powered by a specific type of harvester or using a specific type of storage.

In the case of the second case study, the future work is aimed at improving the harvesting efficiency of the floor tile. Advances in this field could lead to more efficient methods for harvesting the energy from low intensity impacts.

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Appendix A

Detailed Description of the Nanowatt Voltage Detection Circuit

This section is aimed at detailed explanation of the operation of the Nanowatt Voltage Detection circuit. The schematic of the circuit is presented in Fig A.5. The description of the signal propagation throughout the circuit during follows the stages described in the Analysis and Implementation Section 3.3 of Chapter 4.

The operation of the entire circuit will be explained on an operation cycle of the NVD. It is assumed that both VIN and OUT voltages are on 0V on the beginning. As the power source becomes available the buffer capacitor gets charged by the harvester. When the voltage level reaches the threshold voltage of Q2 the voltage monitoring stage is activated. The C_IN capacitor begins to charge through R8. The combination of C_IN and R8 provide a low pass filter functionality which will be explained later.

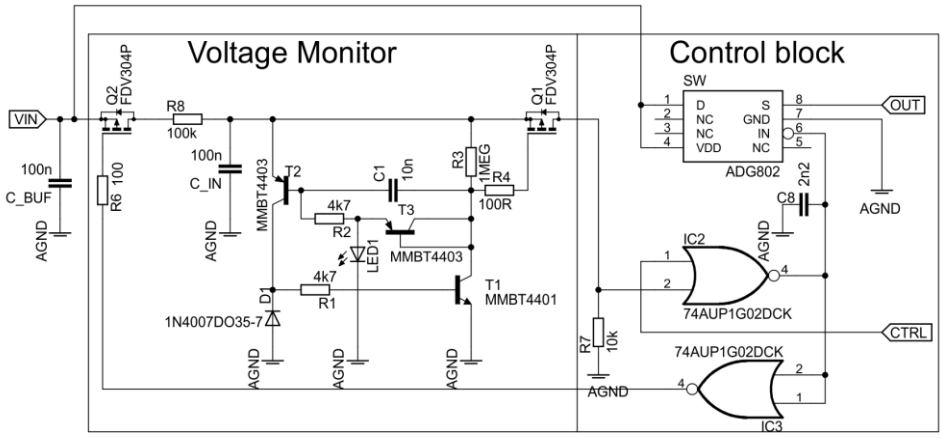


Fig A.5 Schematic of the Nanowatt Voltage Detector circuit

As the voltage continues to rise the LED1 gets forward biased through R3 and C1. When the LED1 begins to conduct it will prevent further rise of voltage on the gate of T2 while the voltage on the emitter will continue rising. Once the voltage difference between base and emitter voltage of T2 reaches 400mV the transistor T2 will begin conducting. This current will activate the T1 transistor that would in turn activate the Q1 by pulling its gate voltage to ground level.

When the Q1 conducts it provides a low impedance connection between the input of the IC2 XOR circuit and the C_IN capacitor. As the C_IN is on the same voltage level as the supply of the IC2 the output of the IC2 will be discharged hence activating the main switch, SW. This action connects the C_BUF with the load. At the same time second XOR, IC3, will change its output voltage hence disconnecting the voltage monitor stage from the input buffer capacitor. In this way the voltage monitoring stage is being bypassed removing any additional power consumption from that stage.

In order SW to remain active it is necessary to keep the CTRL line on a high voltage level, thus keeping the output of IC2 on a low voltage level. After activation of the SW there is a short period of time that is required for CTLR line to reach the supply voltage level. This time is defined by the time circuitry controlling the CTLR requires to power up. One of the main factors that will define the time before CTLR line becomes active is the total load capacitance attached to the OUT line of the circuit. High capacitive loads would require longer time to reach the voltage of the input buffer capacitor.

The rise time of CTRL line is in close connection with the capacitor C_IN. When the voltage monitoring stage gets disconnected from the input buffer capacitor through Q2, as mentioned earlier, C_IN has to provide sufficient energy for the voltage monitoring stage to maintain the voltage on IC2 input long enough for CTLR line to stabilize. By sizing the C_IN and R4 the delay time can be altered to fit the application. Once the CTRL voltage reaches the supply voltage the IC2 will maintain the low voltage level on its output regardless of the voltage on the output of the voltage monitoring stage.

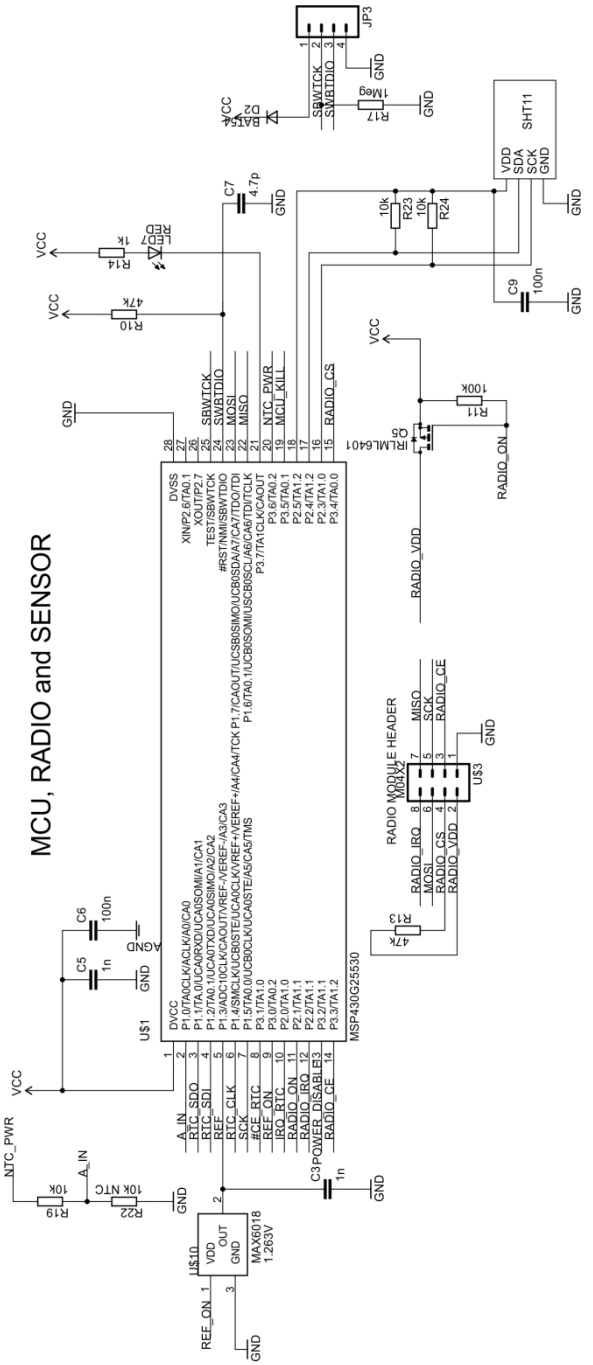
The circuit proposed doesn't have any means of automatically disconnecting the load from the input buffer capacitor when the voltage on buffer capacitor goes below the operating voltage of the load. This has been done deliberately allowing a variety of disabling mechanisms.

In order to detach the load from C_BUF an external circuit has to connect the CTLR voltage to ground potential, thus disabling the SW. At this same moment IC3 will connect the gate of the Q2 to ground potential allowing reconnection of the voltage monitoring stage to the supply. It is important to note that at this moment the C_IN is empty as it was discharged through R4. At this moment there is a voltage difference between C_IN and input buffer capacitor. This difference in voltages required use of R8. With C_IN, R8 composes a low pass filter that will prevent Q1 from activating due to fast rise of source voltage.

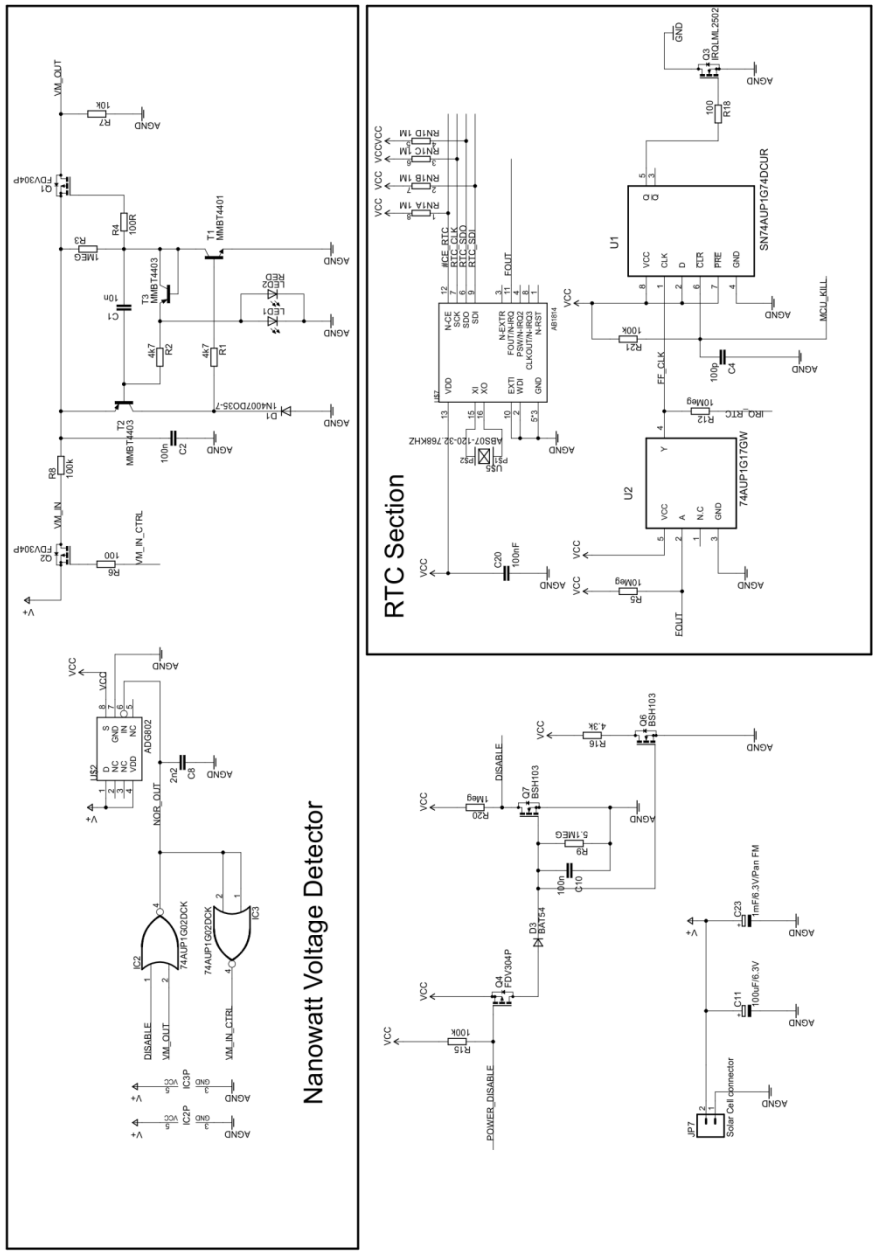
Appendix B

Ultra-Low Power Wireless Sensor Node Schematic

The full schematic of the circuit used in the first case study is presented here. The schematic includes all parts of the ultra-low power wireless sensor node.



Schematic B.1 The MCU; the Radio and the sensors (the SHT11 and the Thermistor)



Schematic B.2 Nanowatt Voltage Detector; RTC and power control part of the ADC energy management; interface circuit between MCU and NVD; solar cell connector and storage capacitors

Appendix C

Detailed Description of Phase 2 Circuit Operation

This appendix will provide an in depth description of the operation of the circuit used in Phase 2 of the second case study presented in Chapter 5.

This circuit was aimed at detecting the stepping direction of a person on a floor tile, using the piezoelectric cymbals placed inside the tile, as both the generator and as a sensing element. The operation of the circuit can be explained by examining the voltage levels of the cymbal output, the primary buffer and the secondary buffer as shown in Fig C.1.

The circuit operation can be divided into three separate stages:

- Stepping on stage
- Waiting stage
- Stepping off stage

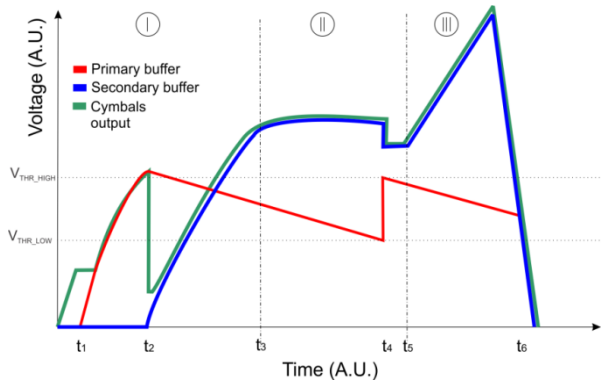
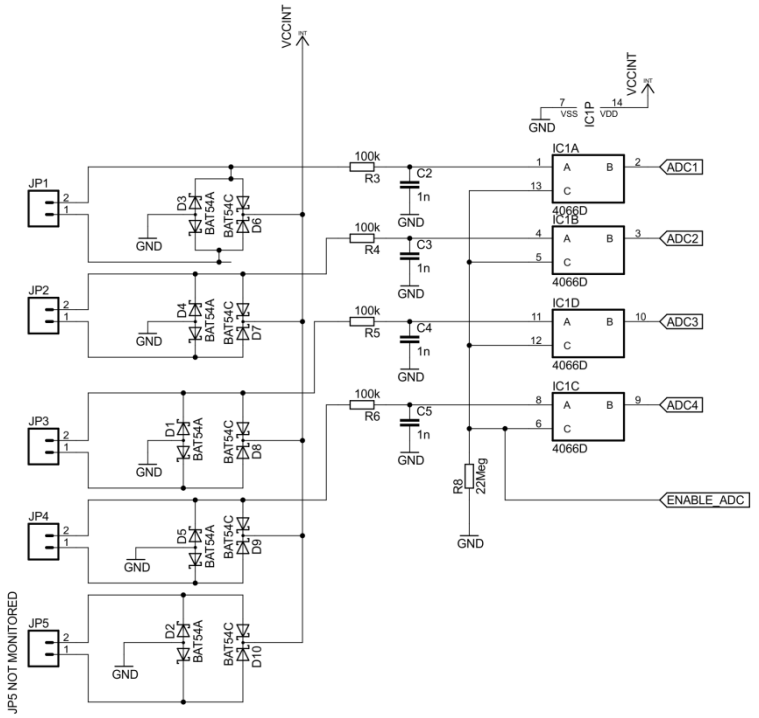
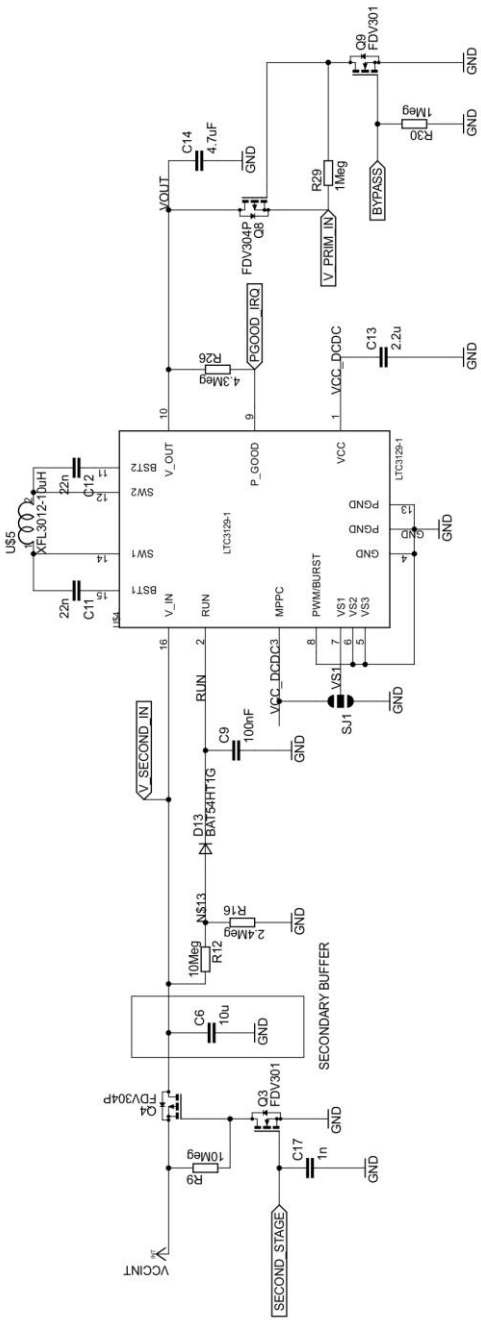


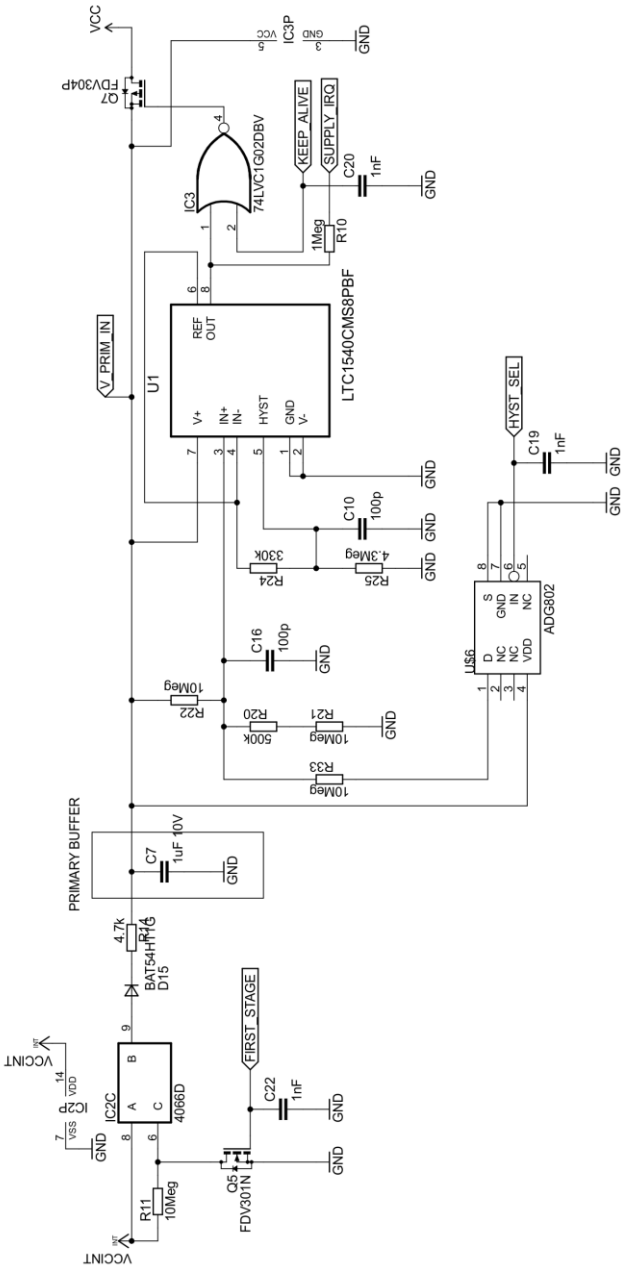
Fig C.1. The three stages of the EH tile circuit operation depicted through the voltages on the primary buffer capacitor, secondary buffer capacitor and cymbal output. The three operation stages are marked with numbers: I – stepping on stage, II – waiting stage and III- stepping off stage



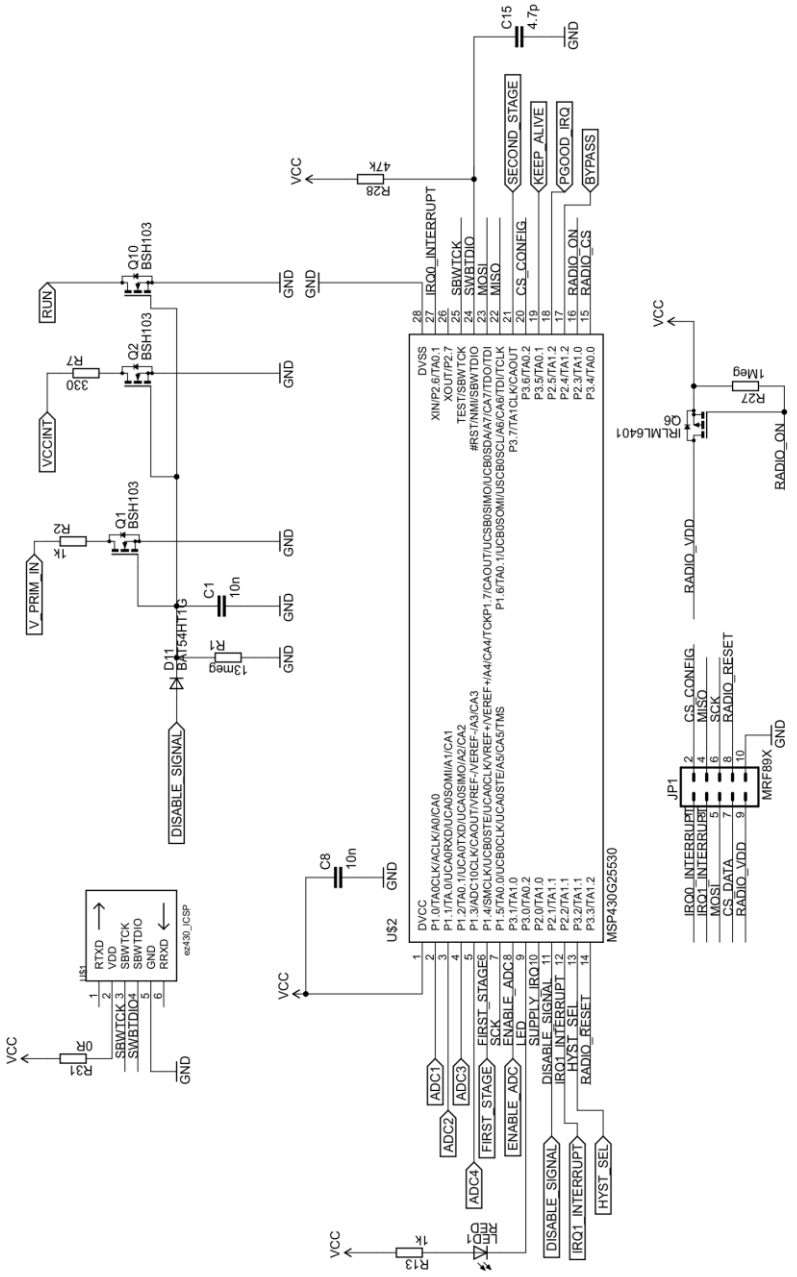
Schematic A.1. The cymbal connectors with the ADC control stage



Schematic A.2. The secondary buffer capacitor, the Stage 2 control and the DC/DC converter section



Schematic A.3 - the voltage monitoring and buffer storage



Schematic A.4 The microcontroller, radio and circuitry for discharging the primary and the secondary buffer capacitor

Each stage will be addressed in detail in the following subsections. The block diagram of the circuit is shown in Fig. 5.20

First Stage – Stepping on the EH Tile

The critical aspect of the circuit operation is determining the stepping direction. The cymbals inside the EH tile are connected in a way their outputs have the same phase when EH tile is stepped on. The signal from the cymbals, which is on higher voltage level during stepping on, is connected to a sampling capacitor through a resistor. There is one capacitor per cymbal. These capacitors are used for sampling the voltage output of the cymbals before it gets rectified. The 100kΩ resistor is placed between the cymbal and the sampling capacitor to a prevent large current flow when the voltage on the cymbal is higher than the supply voltage of the bilateral gate CD4066, marked IC1 on schematic 1. Furthermore, it reduces the current flow when the voltage on the input of IC1 falls below 0V during the stepping off from the tile, as cymbals are then generating the voltage in the negative part of the cycle.

This resistor also acts as a protection element while the MCU is performing the AD conversion. In cases where the output voltage of the cymbal would be higher than the MCU's power supply, at the time of sampling, these resistors prevent excessive current flow from the cymbal into MCU.

When a person begins to step onto the tile, marked as point t_0 in Fig C.1, as soon as the heel contacts with the tile, the nearest two cymbals to the place where the initial contact is made, will start to generate the voltage output. At this point there are no conducting paths from cymbals to the rest of the circuit as bilateral gates IC1 and IC2 are unpowered. The voltage output on the cymbals rises fast until it reaches 2V where the IC1 and the IC2 start operating. This is occurring at point t_1.

The IC1 gates are disabled using a resistor between the control input and the ground potential. On the other hand, the IC2 is activated as a 10MΩ resistor is connected between the supply and the control gate of the IC2. This will, in turn, allow the charging of the primary buffer capacitor. The voltage on the input pin of IC2 will remain constant until the primary buffer capacitor reaches 2V, at this point the voltage on the cymbals' output will continue to rise together with the voltage on the primary buffer capacitor.

The voltage control block has a complex function in the circuit. During the initial, stepping on stage, it is preventing the MCU from stating up until the voltage reaches V_{THR_HIGH} of 3.5V shown as t_2 in Fig C.1. At this point the voltage monitoring circuit realized using LTC1540 from Linear Technology [153], changes its output to high, this signal propagates through the XOR circuit activating the PMOS transistor. The activation of the PMOS transistor allows a current flow from the primary buffer capacitor to the MCU. It was necessary to accumulate the energy in the primary buffer capacitor before the

MCU could be activated, as two cymbals cannot supply enough power for the MCU to run.

As soon as the MCU starts up, it activates the KEEP_ALIVE line. This line is connected between the MCU and the second input to the XOR circuit. In this way the control of the switch that connects the supply line of the MCU to the primary buffer capacitor, is not any more under the sole control of the LTC1540. The reason why this fact is important will be discussed later.

Next step is performing the measurement of the voltage levels on the cymbals. By activating the IC1 the connection is achieved between the sampling capacitors and the analogue input pins of the MCU. Once the connection is established the MCU measures the voltage on the four sampling capacitors. It should be noted that the value of the voltage is not important, only if there is charge on the capacitor or not. This information will be later on used to determine which cymbals got activated when the step began.

Once the measurement has been completed, it is necessary to reroute the power coming out of the cymbals to the secondary buffer capacitor. This is done for two reasons. First the primary buffer capacitor has to be small in order to charge to the MCU operating voltage before the second pair of cymbals gets activated; hence the potential for storing energy is small, as explained in phase 1. Second, when other two cymbals get activated, the voltage on this capacitor would rise to levels which would damage the MCU and the radio, therefore, there was a need for inserting a voltage converter between the buffer capacitor and the MCU and radio.

Rerouting of power is done by disabling the first stage. This is done by applying the ground potential to the control input of the IC2 preventing the flow of charge between the cymbals and the primary buffer capacitor. Following is activation of the connection between the cymbals' output with the secondary buffer capacitor. At this instant the voltage on the cymbals will drop to the value near the threshold voltage of the transistor used as a switch between the cymbals and the secondary buffer capacitor. This can be seen in Fig C.1 at t_2.

There is a protection diode located between the input pin and the supply pin of the IC2. If the voltage on the output pin of the bilateral switch is above one diode voltage drop of the supply, current would flow from the output pin to the supply pin due to the protection diode placed inside the integrated circuit. The diode located between the output of the IC2 and the primary capacitor buffer prevents the charge from the primary buffer capacitor from flowing back into the IC2.

The secondary buffer continues charging as long as there is a change of pressure on the EH tile. The moment foot rests on the tile there is no more

change in pressure and the charging ceases. This point is marked at t_3 in Fig C.1. Now the system transfers into the waiting stage.

Second Stage – Waiting for Stepping off the EH Tile

In this stage the circuit is waiting for the person to step off the EH tile, thus generating the remaining energy required for the transmission. During this period is imperative to maintain the value of the measurements on the stepping direction stored in the MCU's RAM. This is done by using the remaining energy available in the primary buffer storage. Regardless of how low the power consumption could be, at some point the circuit will deplete the primary buffer capacitor leading to the loss of the measured data. In order to avoid this scenario, the voltage monitoring block is again used to monitor the voltage of the discharging primary buffer capacitor.

In order to detect the low voltage condition on the primary buffer capacitor a new threshold voltage is being set by disconnecting one of the resistors located in the voltage divider connected to the input pin of the LTC1540. By disabling the bilateral switch ADG802 the threshold voltage of the LTC1540 comparator becomes V_{THR_LOW}. The V_{THR_LOW} is set to 2.3V in this application. It should be noted that that the switch connecting the power supply line of the MCU is no longer dependent only on the output of the comparator, therefore, allowing use of the comparator output as the low voltage detector.

When the primary buffer capacitor gets depleted to the voltage level V_{THR_LOW}, at the moment t_4 in Fig C.1, the output of the LTC1540 changes, indicating that the low voltage state has been reached. At this point the MCU activates the first stage while keeping the second stage active, thus recharging the primary buffer capacitor from the secondary buffer capacitor.

As soon as the connection between the primary and secondary buffer is established, the threshold voltage of the LTC1540 is changed back to 3.5V by activating the ADG802 gate. The rise of the voltage on the primary buffer capacitor will be dependent on the difference between the primary and the secondary buffer. A resistor is placed between them in order to limit the inrush current that would flow once two capacitors with different voltages get connected together. This resistor is limiting the rise time of the voltage hence providing the control circuitry with sufficient time to react and disable the connection between the buffers before the primary buffer gets charged over 3.6V. When the primary buffer capacitor reaches once again the 3.5V the primary buffer is detached from the secondary buffer capacitor. Not he circuit continues to wait for stepping off to occur. The LTC1540 threshold is set back to 2.3V allowing the continuation of the primary buffer voltage monitoring in case another recharge becomes necessary.

Third stage – Stepping Off the EH Tile

As the person steppes off the tile the secondary buffer continues to charge as the motion of the person is generating power from the EH tile. The charging continues until the activation threshold of the DC/DC converter is reached. The DC/DC block is the same as the one used in the Phase 1 of the project, therefore, its method of operation will not be discussed in detail here.

There is a PMOS gate placed between the output of the DC/DC stage and the primary buffer capacitor. In contrast to Phase 1, where the output of the DC/DC converter was directly connected to the MCU and the radio, here it was necessary to separate the output of the DC/DC from the primary buffer capacitor. The direct connection would result in charging the output capacitance of the DC/DC converter during the stepping on stage. This is unacceptable as the minimum capacitance recommended for stable operation of the DC/DC converter was 4.7µF and charging a 4.7µF would not be possible using power generated by two cymbals before the window of opportunity for direction detection closes.

Once the DC/DC converter is active and stable the "power good" signal is sent to the MCU. At this point the MCU activates the connection between the primary buffer capacitor and the output of the DCDC converter. Following is the transmission of the packet over the radio.

When the packet is transmitted the blocks for discharging both primary and secondary capacitors are activated. The block's schematic is shown in the Schematic 4. It can be seen that there is a diode blocking the back flow of charge from the gate of the transistors to the supply. This is necessary to provide a sufficient period of time for the transistor to discharge the primary buffer and the secondary buffer. Furthermore, as there is still charge left on the gate, if there is any additional charge being generated by the cymbals, it will be connected to the ground through the transistors, thus preventing any additional charge build up before the next step.