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ABSTRACT

We have designed and for the first time experimentally verified a topology optimized mode (de)multiplexer, which demultiplexes the fundamental and the first order mode of a double mode photonic wire to two separate single mode waveguides (and multiplexes vice versa). The device has a footprint of ~4.4 μm x ~2.8 μm and was fabricated for different design resolutions and design threshold values to verify the robustness of the structure to fabrication tolerances. The multiplexing functionality was confirmed by recording mode profiles using an infrared camera and vertical grating couplers. All structures were experimentally found to maintain functionality throughout a 100 nm wavelength range limited by available laser sources and insertion losses were generally lower than 1.3 dB. The cross talk was around -12 dB and the extinction ratio was measured to be better than 8 dB.

Keywords: Topology optimization, space division multiplexing, mode division multiplexing, photonic integrated circuit

1. INTRODUCTION

Recently interest has been shown in optical components for mode conversion[1,2] and multiplexing[3-8] as space division multiplexing (SDM) is considered an efficient way to increase transmission capacity for optical transmission systems[9]. Photonic integrated circuits (PICs) are preferable for cost effective wide-scale deployment of the technology, which in turn will require a small footprint and low sensitivity to fabrication errors. Previous implementations of on-chip mode multiplexers have typically been based on asymmetric directional couplers[4], Y-junctions[6] and multimode interferometers[7]. Although these candidates are all very promising, they have footprints around 10-50 μm, that tend to scale substantially in size with the number of modes to be multiplexed as the schemes commonly rely on cascading the designs[3].

Topology optimization[10] (TO) is an inverse design tool, which has been experimentally proven to deliver robust designs for various nanophotonic components with controllable bandwidth and low loss[11,12]. The benefits of TO include ultra-small device footprints and the possibility of adding device functionalities without cascading multiple devices. In this paper, we present experimental results for low-loss, broadband (de)multiplexing of the transverse-electric fundamental even (TE_0) mode and the first higher-order odd (TE_1) mode in a silicon photonic wire component. The design has been obtained using TO and has been fabricated in silicon-on-insulator (SOI) material. Measurements of the mode profiles as well as the losses are performed and verifies the potential usage of TO for ultra-compact PIC SDM components.

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2. DESIGN GENERATION AND MODELLING

2.1 Topology optimization of the (de)multiplexer

The objective of the TO is to demultiplex the fundamental and the first order mode of a double mode photonic wire to two separate single mode waveguides. The initial and naïve design of the silicon demultiplexer is shown in Figure 1. In- and out-put ports (black) of the demultiplexer, comprised of a 2.5 μm x 2.5 μm silicon square region (red), are silicon photonic wires with widths of 694 nm and 432 nm, respectively. The widths are chosen so that the former supports both the TE_0 and the TE_1 mode while the latter supports only the TE_0 mode.
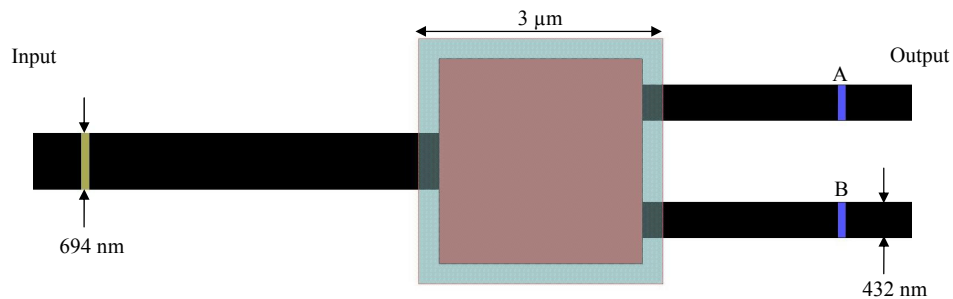

Figure 1: First iteration design for topology optimization of the silicon demultiplexer. The in- and out-put ports (black) in which the modes are excited (yellow bar) and recorded (purple bars A and B). The 3 μm x 3 μm design domain (blue) encloses the 2.5 μm x 2.5 μm demultiplexer region (red).

The TO is performed through repeated finite-difference time-domain (FDTD) calculations and sensitivity analysis using a software package developed in house[13,14]. For specific information on the TO method we refer to refs. [13] and [14]. The TE_0 and TE_1 modes are excited in the input waveguide (at yellow bar in Figure 1) and the distribution of silicon material in a 3 μm x 3 μm square design region (blue in Figure 1) is iteratively modified to obtain the targeted intensity distribution of the demultiplexed modes at position A and B in the two output arms. Here, the input TE_0 mode is targeted to be transmitted to the upper output port whereas the input TE_1 mode should be converted to a TE_0 mode and transmitted to the lower port. As previously demonstrated, 3D optimization leads to superior results compared to performing 2D TO when the designs are to be fabricated[1,13]. 2D TO is favored in initial steps to lower computation time and used to determine a minimal footprint of the design domain which maintain low loss and high extinction ratios. Subsequently, 3D optimization is applied to the 2D generated designs to obtain structures that will function optimally in practice.

2D and 3D TO were performed with spatial resolutions of 16 nm and 32 nm and using a relative permittivity of silicon ε_{Si} = 11.680 and perfectly matched absorbing layers as boundary conditions. In the case of the 3D optimization, the silicon photonic wire had a height of 340 nm, was surrounded by air above and placed on top of a silica layer with a relative permittivity of ε_{SiO2}=2.085. The design domain extended vertically through the silicon and the distribution of material was restricted to be uniform in the vertical direction to render fabrication feasibile using standard dry etching techniques. The light source used in all optimizations was a Gaussian pulse with a spectral width of ~280 nm (full-width half-maximum). The pulse was centered on ~1760 nm and ~1580 nm in 2D and 3D, respectively. The converged (de)multiplexing designs were collected after 200 TO iterations in 2D and 160 in 3D.
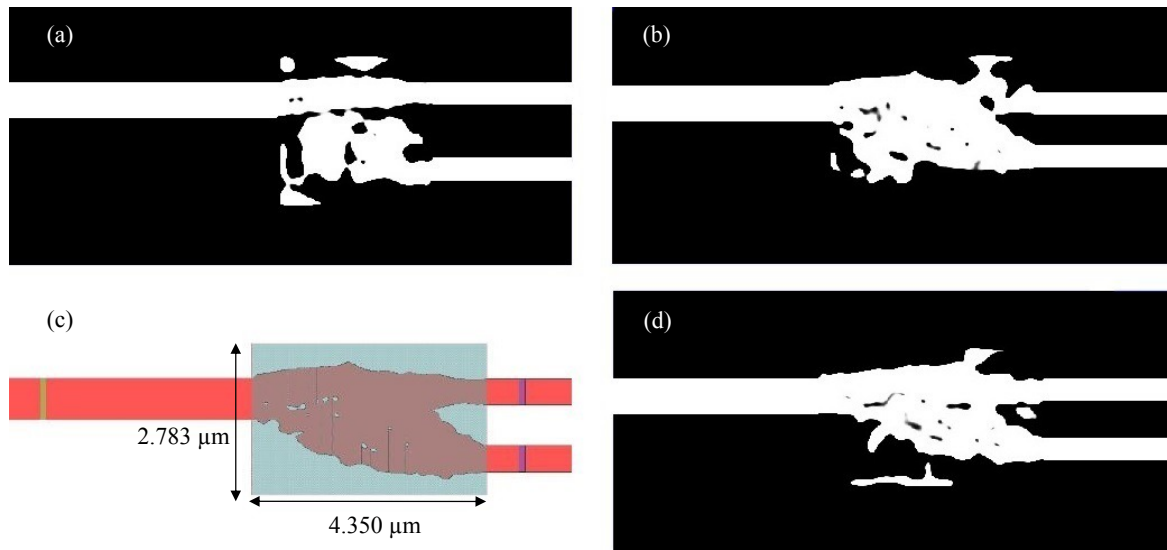
Figure 2: Black (air) and white (silicon) image of the 2D topology optimized structure leading to efficient transmission of the (a) TE_0 and (b) TE_1 mode. (c) Design starting point for the TO, based on the optimized structures shown in (a) and (b). (d) 2D TO applied to the combined design given in (c) resulting in efficient performance for both the TE_0 and the TE_1 mode. This design was used for performing 3D TO of the final design.

Throughout the 2D optimization procedure, alterations were made to the starting design shown in Figure 1 by changing the distance between the output arms as well as the relative position of the input arm and altering the size of the design domain. This procedure led to various designs performing better for either maintaining good transmission of the TE_0 mode or converting the TE_1 to the TE_0 mode. The two optimal designs obtained in this manner are shown in Figure 2(a) and 2(b), respectively, and the design shown in Figure 2(c) was constructed by manually overlapping these designs and removing side structures, which were found to have minor influence on the fields. The design in Figure 2(d) is the result of performing TO on that structure and was subjected to 3D optimization to obtain the final 3D design.

2.2 Design robustness

Several variations of the final design were made to investigate the design robustness during fabrication. Firstly, 3D TO was done both at 16 nm and 32 nm resolutions; these are shown in Figure 3(a) and 3(b), respectively. The lower resolution (32 nm) omitted smaller features, which would be less reproducible during fabrication. Secondly, optimized designs containing gray scale features were extracted from the raw data to the design file using different threshold values. Finally, all structures were fabricated twice with different lengths of nanowires before and after (de-)multiplexing to ensure that any unwanted Fabry-Perot effects were not concealed by the chip-design.
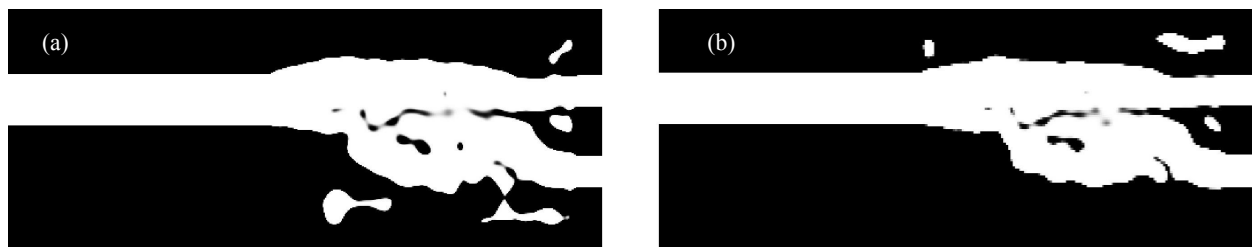

Figure 3: 3D TO of the design shown in Figure 2(d) with a spatial resolution of (a) 16 nm/pixel and (b) 32 nm/pixel.

2.3 Modelling of the optimized structure

Figure 4(a) and 4(b) shows the calculated spectra of TE_0 and TE_1 light propagating through the multiplexer, respectively. Spectra are included for three threshold values, and are in all cases normalized to the spectrum of TE_0 light passing through a straight photonic wire. T and B refers to output in the top or bottom arm respectively; only T is meant to carry

an output for an input TE_0, while only B is to carry signal for an input of a TE_1 mode. For the TE_0 mode, Figure 4(a), the change of threshold has little impact on the T channel, while the highest threshold value (blue) leads to an increase of loss for the TE_1 mode in Figure 4(b). Clearly, the lower threshold values perform best with insertion losses ~1 dB in the 1520 nm – 1620 nm wavelength range. For these, the crosstalk between the lower and upper arms are $\leq$ -14 dB. In Figure 4(c) and 4(d) the simulated H-field at 1578 nm is visualized in the two operational modes of the multiplexer clearly demonstrating the functionality. Figure 4(e) and 4(f) shows the calculated and normalized flux of a TE_0 mode multiplexed from the upper (Figure 4(e)) and lower (Figure 4(f)) arm to the double mode photonic wire and reveals a mode extinction ratio ~24 dB in the best case of Figure 4(f).
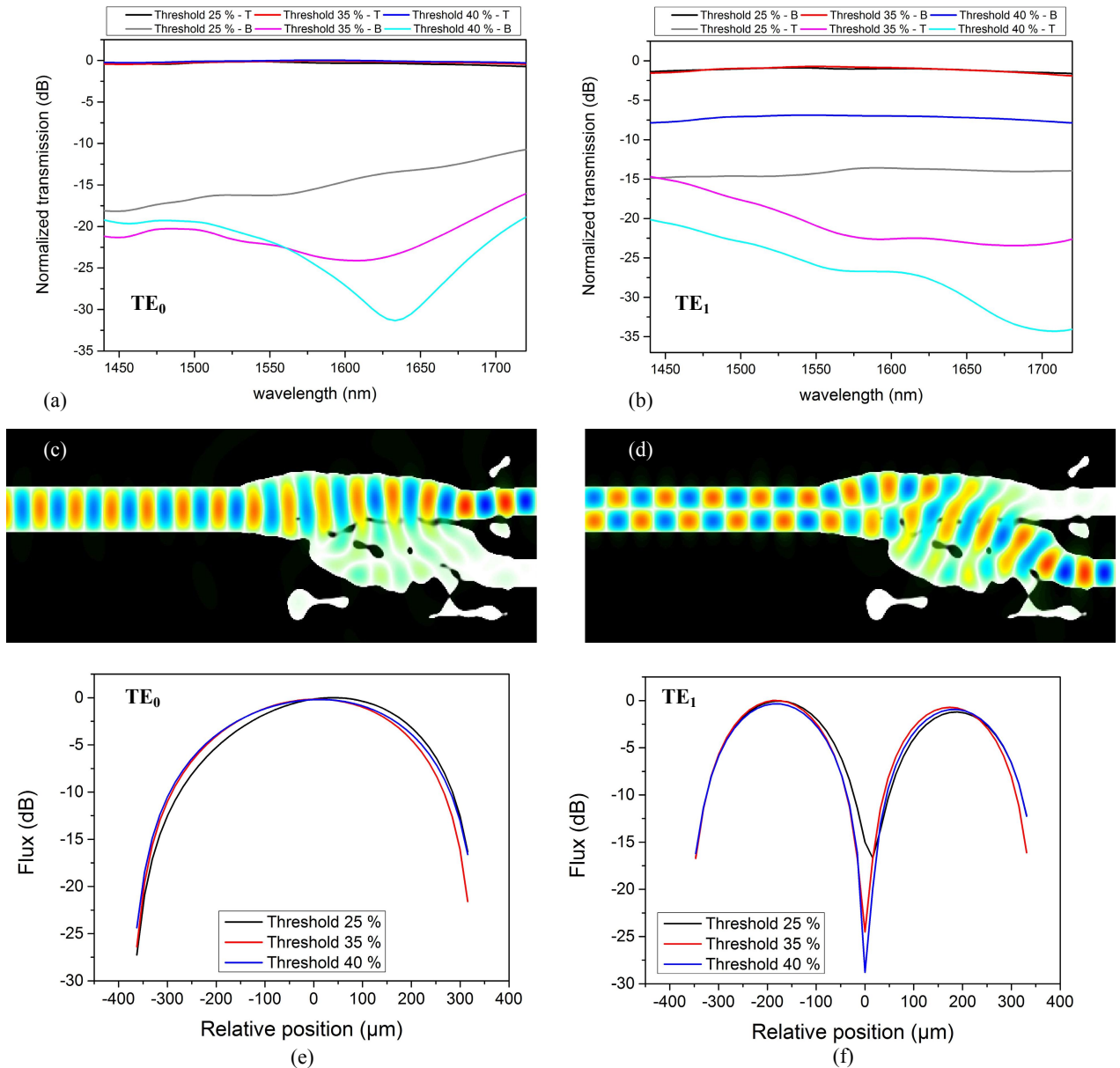

Figure 4: (a,b) 3D FDTD calculated transmission spectra for the demultiplexed (a) TE_0 mode and (b) TE_1 mode given for the three fabricated threshold values. All spectra are normalized to the TE_0 transmission spectrum of a straight waveguide. T and B refer to top and bottom output arms, respectively. (c,d) Mode profiles of the (c) TE_0 mode and the (d) TE_1 mode transmitted through the design with a 16 nm/pixel resolution and a threshold of 35 %. Profiles were recorded at 1578 nm. (e,f) Power fluxes of a TE_0 mode input from the (e) upper arm and (f) lower arm and transmitted to the double mode photonic wire.

3. FABRICATION

The demultiplexer structures were fabricated in a SOI material with an ~340 nm thin silicon layer placed on an ~2000 nm thick silica buffer layer. For the sake of characterization, two types of structures S1 and S2 were fabricated as sketched in Figure 5. Structure S1 refers to single structures allowing for input of the TE_0 mode to the lower or upper arm that will output either the TE_1 or the TE_0 mode, respectively, to a vertical grating coupler and allows recording of the mode profile. Structure S2 is a cascaded multiplexing (MUX) and de-multiplexing (deMUX) structure that will input and output a TE_0 mode which has undergone either a TE_0-TE_1-TE_0 path (BB) or a TE_0-TE_0-TE_0 path (TT). The structure S2 is realized by mirroring the S1 design. Thus, for low crosstalk, no transmission should occur from top input to bottom output (TB) or vice versa (BT). In S2 the separation between the multiplexers is ~8.5 μm.
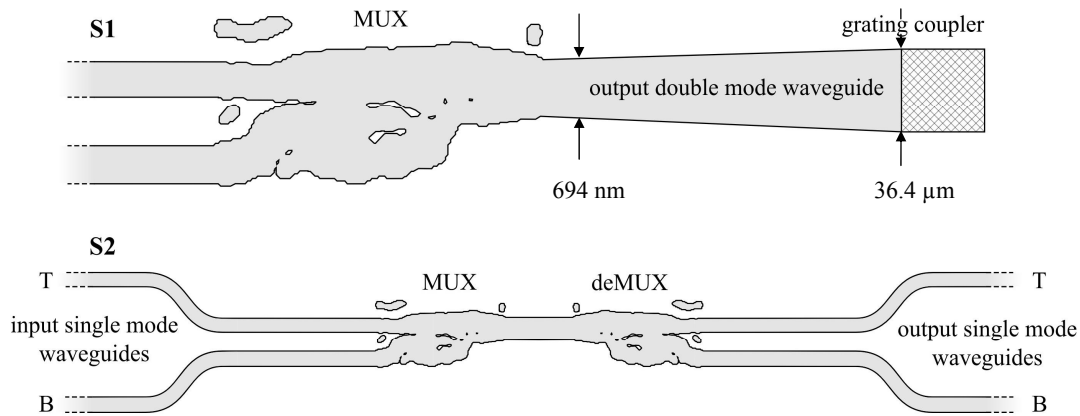

Figure 5: Sketches of the two types of fabricated structures (not to scale). (top) The S1 structure in which a multiplexed signal is sent to a vertical grating coupler over which an IR-camera is placed to record the mode profiles. (bottom) The S2 structure with MUX and deMUX functionality. The distance between the (de)multiplexers is ~8.5 μm. The notation of T and B indicates top and bottom input and output. The top input will face a TE_0-TE_0-TE_0 transmission path while the bottom line will undergo conversion from TE_0-TE_1-TE_0.

The topology optimized designs were defined in an ~110 nm thick layer of ZEP520A positive electron beam resist using a JEOL JBX-9500 electron-beam lithography system. The system was operated at 100 keV and the writing field of the machine was set to 0.5 mm x 0.5 mm. The electron beam has an estimated diameter of 12 nm and is scanned in steps of 4 nm. Proximity error correction is applied to account for backscattered electrons during the writing of the structure. Once developed and postbaked, the resist is used as a soft mask during etching. The etching system is an inductively coupled plasma reactive ions etching using SF_6 and C_4F_4. Finally, ~3 μm thick and wide SU-8 polymer waveguides were defined, also using electron-beam lithography, to overlap with inversely tapered silicon ridge in- and output waveguides. Figure 6 shows a scanning electron micrograph (SEM) image of a fabricated S2 structure.
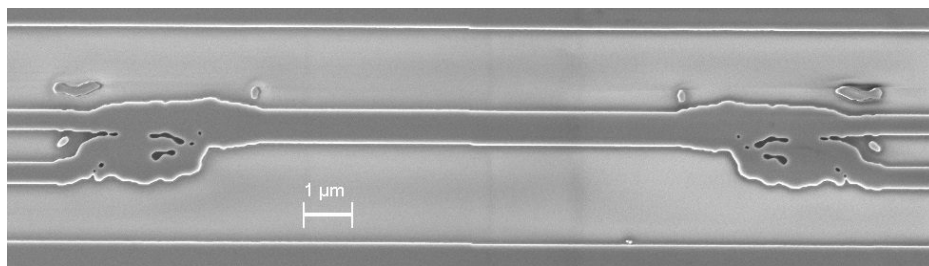

Figure 6: SEM image of a fabricated 3D topology optimized MUX and deMUX design.

4. CHARACTERIZATION

4.1 Confirmation of multiplexing

To experimentally verify functionality of the (de)multiplexer, structure S1 is used to record the resulting mode profiles of TE_0 modes transmitted from the upper and lower arms to the double mode photonic wire using an InGaAs infrared camera (IR-Cam – Xenics XEVA XC130). As shown in Figure 5(a), the output waveguide of S1 was gently tapered from 694 nm to 36.4 µm and ended in a vertical grating coupler above which an IR-camera is placed. Figure 7 shows the qualitative mode profiles recorded at various wavelengths for input of light through the upper and lower arms of the S1 multiplexer, respectively. Clearly, multiplexing occurs in a broad wavelength range from 1530 nm to 1610 nm.
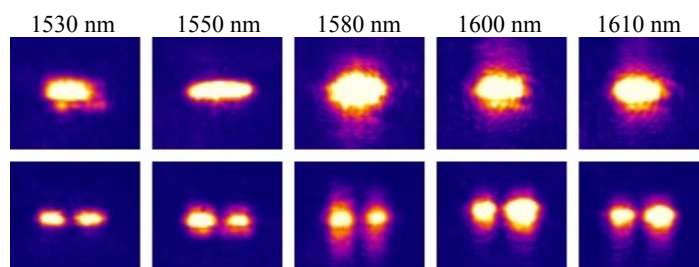

Figure 7: Mode profiles of the multiplexed signals recorded at various wavelengths using an IR camera. The upper/lower row represents the TE_0 mode input to the upper/lower arm of the S1 structure.

4.2 Experimental on-chip multiplexing and demultiplexing

Transmission spectra were only measured for the S2 structures as no efficient tapered few-mode fibers supporting the TE_1 mode were available to us and, thus, it was not possible to record spectra for the S1 structure. The transmission spectra were recorded in the wavelength region from 1520 nm to 1620 nm using an optical spectrum analyzer and normalization of the spectra is done using TE_0-carrying waveguides as references.
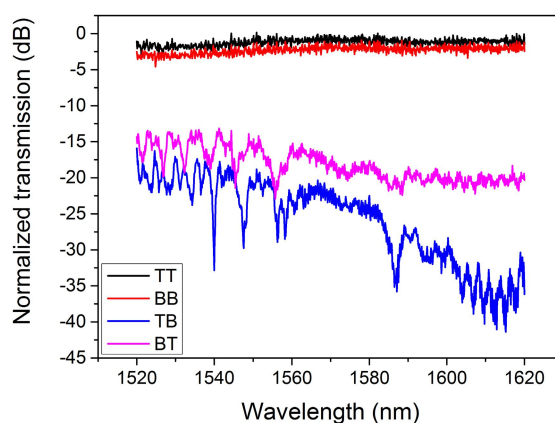

Figure 8: Normalized transmission spectra of the S2 structure optimized with a resolution of 16 nm and extracted with a threshold of 35 %. Spectra are normalized to the TE_0 mode of a single mode waveguide with the same length and bends at input and output.

Figure 8 shows the measured spectra of S2 (threshold value 35 %) for the four different channel combinations following the naming convention given in the sketch in Figure 5. As the structure S2 includes two (de)multiplexers and as the design is reversible and characterized in the linear regime, the loss of one (de)multiplexer can be estimated by halving the measured loss in Figure 8. Thus the insertion loss for the TT channel is < 1 dB and for the BB channel ~1.5 dB. Agreeing with intuition, the loss of the TE_0 mode following the BB path is slightly higher than for the channel which maintains the TE_0 mode throughout the structure. The broad band functionality is observed as predicted by the 3D FDTD calculations of Figure 4 and the cross-talk between the channels is < -12 dB.

Figure 9(a) and 9(b) shows the comparison of different threshold values for the 16 nm resolution S2 structures, for the TT and BB channels, respectively. It is observed that the 35 % value of the threshold leads to the better result for both the TE_0 and TE_1 channel, while straying from this will improve one at the cost of the other. In spite of these variations the overall functionality is maintained and the crosstalk is < -10 dB.
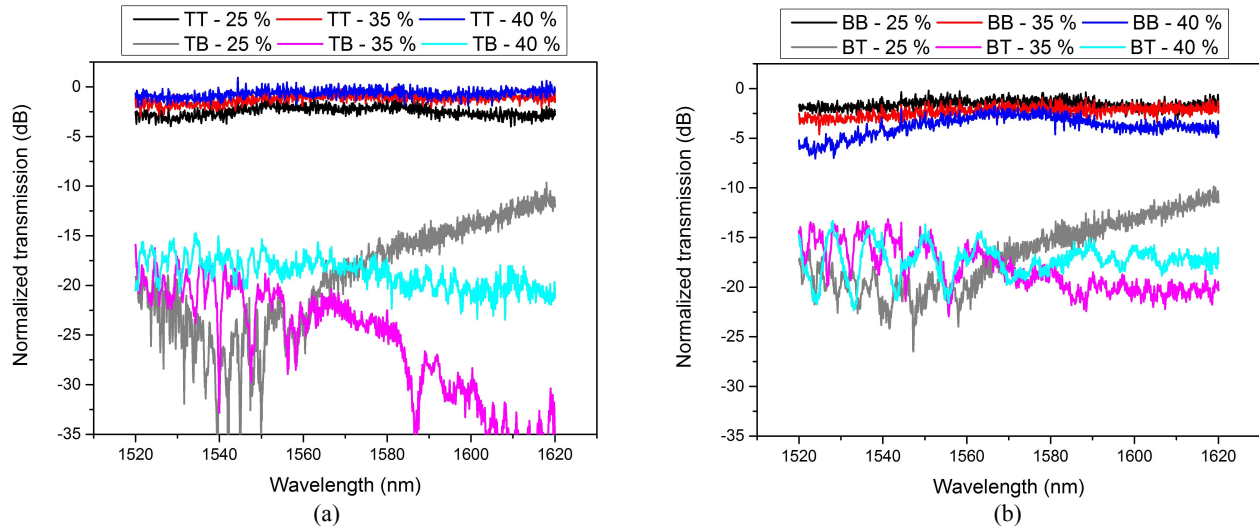

Figure 9: Spectra from the S2 structure optimized with a resolution of 16 nm for three different choices of structural threshold values. (a) Spectra of the TE_0-TE_0-TE_0 conversion and (b) of the TE_0-TE_1-TE_0 conversion. Data is normalized to the TE_0 mode of a single mode waveguide with the same length and bends at input and output.

Figure 10 shows the measured spectra of the S2 design with a threshold of 35 % at a 16 nm and 32 nm resolution, respectively. The losses are quite similar; however loss is decreased slightly for the lower resolution. This is explained by the larger design features, which are more reproducible during fabrication; however the functionality of the smaller features was the quenching of crosstalk as this tends to be less stable for the higher resolution design.
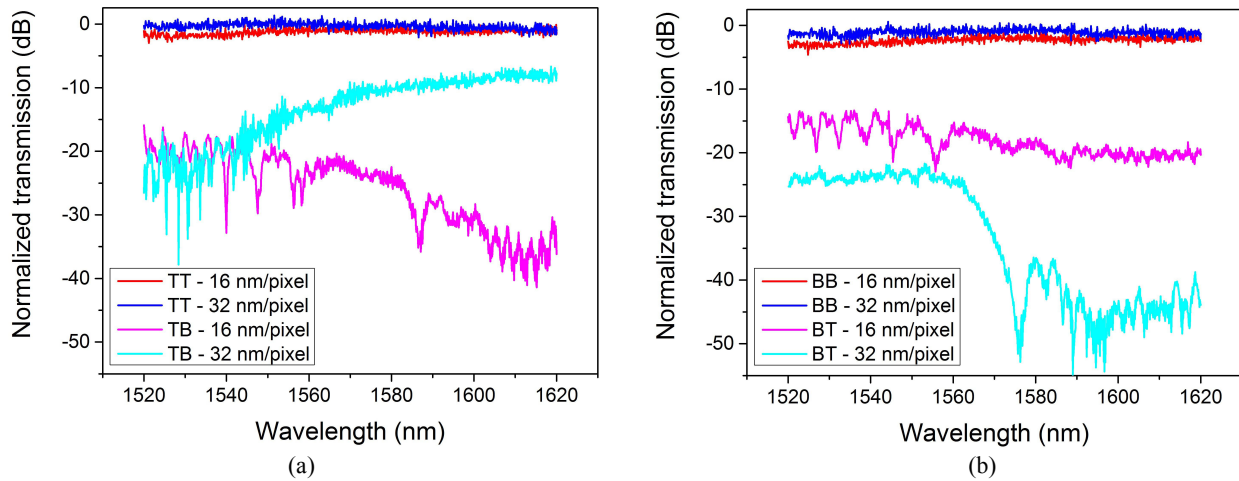

Figure 10: Measured spectra of the S2 structure with a threshold of 35 % and designs optimized with different resolutions. Measured spectra for light following (a) a TE_0-TE_0-TE_0 path and (b) a TE_0-TE_1-TE_0 path. Data is normalized to the TE_0 mode of a single mode waveguide with the same length and bends at input and output.

Figure 11 shows line scans across the mode profiles of the 16 nm and 32 nm structures with 35 % and 40 % thresholds, respectively. They were recorded at 1552 nm and 1582 nm, respectively. From these we can find an experimental TE_1/TE_0 extinction ratio of 8-10 dB. However, it is likely that the actual extinction ratios are higher as the measurements suffer from saturation of the signal on the IR-camera.
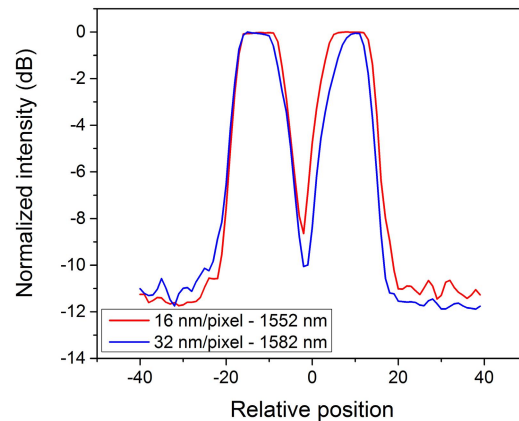
Figure 11 Line scans across the mode profiles of two S1 structures (red) at 16 nm resolution with a threshold value of 35 % recorded at 1552 nm and (blue) 32 nm resolution with a threshold value of 40 % recorded at 1582 nm. Unfortunately, the signal is saturated for the peak values, obscuring the actual extinction ratio.

5. CONCLUSION

We have demonstrated the usage of topology optimization for the design of a mode (de)multiplexer, with ultra-compact size of ~4.4 µm x ~2.8 µm, which demultiplexes two signal channels from a photonic wire supporting both the TE_0 and the TE_1 mode onto two separate single mode waveguides. Designs were made using 16 nm/pixel and 32 nm/pixel resolution and fabricated for three different threshold values to investigate the robustness of the designs. The designs were fabricated in silicon-on-insulator material and experimentally verified to perform multiplexing through measurements of the mode profiles. Insertion losses were < 1.4 dB for the ideal structures and remained < 3 dB for all design variations in the measured 100 nm region. The cross-talk of the device was around -12 dB and had an extinction ratio of at least 8 dB. In future, we believe that topology optimization can be applied to realize (de)multiplexing of more modes while maintaining ultra-compact device footprints.

REFERENCES

[1] Frandsen, L. H. Elesin, Y., Frellsen, L. F., Mitrovic, M., Ding, Y., Sigmund, O. and Yvind, K., "Topology Optimized Mode Conversion in a Photonic Crystal Waveguide Fabricated in Siliconon-Insulator Material." Optics Express 22(7), 8525–8532 (2014).

[2] Huang, Y., Xu, G., and Ho, S.-T., "An ultracompact optical mode order converter," IEEE Photonics Technology Letters, 18(21-24), 2281–2283 (2006).

[3] Luo, L.-W., Ophir, N., Chen, C. P., Gabrielli, L. H., Poitras, C. B., Bergmen, K., and Lipson, M., "WDM-compatible mode-division multiplexing on a silicon chip," Nature Communications, 5, 3069 (2014).

[4] Ding, Y., Xu, J., Da Ros, F., Huang, B., Ou, H., & Peucheret, C., "On-chip two-mode division multiplexing using tapered directional coupler-based mode multiplexer and demultiplexer," Optics Express, 21(8), 10376–10382 (2013).

[5] Dai, D., Wang, J., and Shi, Y., "Silicon mode (de)multiplexer enabling high capacity photonic networks-on-chip with a single-wavelength-carrier light." Optics Letters, 38(9), 1422–1424 (2013).

[6] Love, J. D., and Riesen, N., "Single-, Few-, and Multimode Y-Junctions," Journal of Lightwave Technology, 30(3), 304–309 (2012).

[7] Kawaguchi, Y., and Tsutsumi, K., "Mode multiplexing and demultiplexing devices using multimode interference couplers," Electronics Letters, 38(25), 1701–1702 (2002).

[8] Lu, J., and Vuckovic, J., "Nanophotonic computational design, "Optics Express, 21(11), 13351–13367 (2013).

[9] R. Kirchain and L. Kimerling, "A roadmap for nanophotonics," Computer Methods in Applied Mechanics and Engineering, 71, 197-224 (1988).

[10] M.P. Bendsøe and N. Kikuchi, "Generating optimal topologies in structural design using a homogenization method", Computer Methods in Applied Mechanics and Engineering, 71, 197-224 (1988)

[11] Borel, P. I.m Harpøth, A., Frandsen, L. H., Kristensen, M., Shi, P., Jensen, J.S. and Sigmund, O., "Topology optimization and fabrication of photonic crystal structures", Opt. Express 12, 1996-2001 (2004).

[12] Jensen, J. S., and Sigmund, O., "Topolgy optimization for nano-photonics," Laser & Photon. Rev., 5, 308-321 (2011)

[13] Elesin, Y., Lazarov, B. S., Jensen, J. S., and Sigmund, O., "Time domain topology optimization of 3D nanophotonic devices," Photonics and Nanostructures - Fundamentals and Applications, 12(1), 23–33, (2014).

[14] Elesin, Y., Lazarov, B. S., Jensen, J. S., and Sigmund, O., "Design of robust and efficient photonic switches using topology optimization," Photonics and nanostructures-Fundamentals and Applications, 10(1), 153–165 (2012).