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Towards Electrically Pumped Nanolasers for Terabit Communication

Ph.D. Thesis

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Submitted to the Department of Photonics Engineering at The Technical University of Denmark in partial fulfilment for the degree of Doctor of Philosophy

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Preface

This dissertation has been submitted to the Department of Photonics Engineering at the Technical University of Denmark (DTU) for the partial fulfillment of the degree of Doctor of Philosophy (Ph.D.). The work presented in this Thesis was carried out as a part of my Ph.D. project in the period from March 15$^{\text{th}}$, 2012 to September 14$^{\text{th}}$, 2015. The work took place at DTU Fotonik (Technical University of Denmark, Department of Photonics Engineering).

The Ph.D. project was financed by the Villum Kann Rasmussen center of excellence NATEC (NAnophotonics for TErabit Communication) and was supervised by:

- Kresten Yvind (main supervisor), Associate Professor, DTU Fotonik, Technical University of Denmark, Kgs. Lyngby, Denmark
- Il-Sug Chung (co-supervisor), Associate Professor, DTU Fotonik, Technical University of Denmark, Kgs. Lyngby, Denmark

Abstract

This thesis deals with modeling, design, fabrication and characterization of vertically electrically pumped photonic crystal light-emitting devices. For this purpose a new material platform of III-V semiconductors on silicon has been developed. The devices fabricated on this platform can be used as optical interconnects, where compatibility with Complementary Metal Oxide Semiconductor (CMOS) technology is required.

The first part of this work is dedicated to modeling and simulations of electrically pumped photonic crystal nanolasers with diverse material configurations and different concepts for electrical injection. The analysis of the models is conducted with focus on laser performances, energy efficiency, and thermal properties.

The second part of this thesis deals with design, fabrication and characterization of vertically electrically pumped photonic crystal light-emitting devices. The devices consist of a double heterostructure Photonic Crystal (PhC) membrane with line-defect waveguide for the optical configuration and a pillar under the membrane as a path for vertical electrical injection. The fabricated devices have been tested under electrical injection and photonic crystal light-emitting diodes (LEDs) have been demonstrated. Furthermore the characterization of the devices under optical injection resulted in lasing emission.

The main result of this work is the realization of vertically electrically pumped photonic crystal light-emitting devices on a new material platform. This result has been achieved through a long and complicated cleanroom fabrication process. The processing includes the development of a mutual SiO_2-benzocyclobutene (BCB) planarization with approximately the same dry etch rate for SiO_2 and BCB and double-side processing through adhesive BCB bonding to silicon. The use of chip-mark alignment had to be employed for the second electron-beam lithography of the PhC pattern, in order to compensate for the discovered random sample distortion after the

bonding step.

Resumé

Denne ph.d.-afhandling omhandler modellering, design, fabrikation og karakterisering af vertikalt elektrisk-injicerede lysemitterende komponenter baseret på fotoniske krystaller. Til dette formål er der blevet udviklet en ny materiale-platform baseret på III-V halvledere på silicium. Optiske komponenter fremstillet på denne nye platform kan blive brugt som optiske forbindelseselementer, der kan integreres med CMOS-teknologi.

Den første del af afhandlingen omhandler modellering og simulering af elektrisk-pumpede nanolasere baseret på fotoniske krystaller med forskellige materialekonfigurationer og koncepter for elektrisk injektion. Analysen af disse modeller er udført med fokus på opførslen af laseren, energieffektivitet og termiske egenskaber.

Den anden del af afhandlingen omhandler design, fabrikation og karakterisering af vertikalt elektrisk-injicerede lysemitterende komponenter baseret på fotoniske krystaller. Enhederne består af dobbelt heterostruktur fotoniske krystal membraner med linjedefekt bølgeledere til at kontrollere de optiske egenskaber samt en søjle under krystal membranen til vertikal elektrisk injektion. De fabrikerede komponenter var under elektrisk injektion lysemitterende dioder (LEDs) og derfor ikke lasere. Karakterisering af enhederne ved brug af optisk injektion gav laseremission fra de fabrikerede enheder.

Hovedresultatet fra dette arbejde er fabrikation og realisering af vertikalt elektrisk-injicerede lysemitterende komponenter baseret på fotoniske krystaller fremstillet på en ny materialeplatform. Dette resultat er opnået ved udvikling af en kompleks renrums-fabrikationsproces. Processen bygger på udviklingen af en kombineret SiO_2-benzocyclobutene (BCB) planarisering. Planariseringen er opnået ved brug af cirka den samme hastighed for tøræstning for SiO_2 og BCB og dobbelt-sidet forarbejdning med BCB-hæftning til silicium. Orientering ved hjælp af chip-markering var essentielt før den anden eksponering med elektronstråle litografi for at

frembringe det fotoniske krystal-mønster i korrekt position. Dette var nødvendigt for at kompensere for den tilfældige orientering af enhederne efter bindingstrinnet.

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Thanks to all my friends, colleagues and Ph.D. fellows that I bothered during my project: thanks to Claudia, Corinna, Francesco, Marco T., Marco M., Solené, Sidsel, Anders for the never-ending chats during coffee

breaks, danish classes, and knowledge sharing.

Last but not least I would like to thank my whole family and in particular my mother and my father who always believed in my capabilities and supported me during this adventure in Denmark.

In the end I would like to thank Theis for the thesis proof reading and for the support and the patience that have been essential in the life besides work.

List of publications

The following publications have been authored or co-authored during the course of the Ph.D. project:

I A. Lupi, I.-S. Chung, and K. Yvind, "Electrical injection schemes for nanolasers," *Proceedings of SPIE, Novel In-Plane Semiconductor Lasers XII*, **8640**(86400Y), (2013).

II A. Lupi, I.-S. Chung, and K. Yvind, "Electrical Injection Schemes for Nanolasers," *IEEE Photonics Technology Letters*, **26**(4), 330–333 (2014).

III W. Xue, L. Ottaviano, Y. Chen, E. Semenova, Y. Yu, A. Lupi, J. Mork, and K. Yvind , "Thermal analysis of line-defect photonic crystal lasers," *Optics Express*, **23**(14), 18277–18287 (2015).

Contents

Chapter 1

Introduction

1.1 Optical interconnects

Global mobile data traffic grew 69% in 2014, the number of mobile-connected devices has exceeded the world's population in 2014 and by the end of 2019 there will be nearly 1.5 mobile devices per person [1]. The recent increase of data traffic and overloaded communication networks are posing significant challenges on volume of data, high speed, and bandwidth in optical communication systems. Optical fibers have replaced copper cables in the last century because of their wider bandwidth and higher speed. The contemporary optical technologies are pushing the employment of optical interconnects for a much shorter distance i.e. rack-to-rack, chip-to-chip and intra-chip communication to reduce the power consumption. For these purposes not only speed plays an important role, but also energy efficiency and heat dissipation are target requirements.

Power consumption can mainly be attributed to electrical interconnects showing that on-chip electrical interconnects use more than half of the total power consumption [2]. Electrical interconnects cannot physically keep up with more complex signal processing, since the size scaling does not help the link capacity. Space limits and signal attenuation are the main issues as presented in [3, 4]. With the same perspective Miller [5] also predicts that the energy budget for sending a bit signal is required to be 10 fJ/bit for on-chip communication in the near future. Due to the electrical wiring limitation, optical links offer further advantages over the electrical ones, since the former can bare higher capacity and lower power consumption due to the low operating energy.
The necessity of an alternative path to electrical wiring has become more

and more compelling due to the scaling of Complementary Metal Oxide Semiconductor (CMOS) technology very large-scale integration that David Moore predicted in 1965 [6].
A promising solution is to replace electrical interconnects with optical ones, as optical interconnects may solve interconnect density and scaling limitations and lower power consumption compared to electrical interconnects [7]. Unfortunately optical interconnects for chip integration have to be competitive with their electrical counterparts concerning energy requirements, power consumption, and density. The future key technology will likely allow the integration of optics on CMOS chip for signal processing with increased transmission speed and reduced power consumption.

The aim of this thesis is to bridge the gap between optics and electronics, fabricating a platform where electrically pumped lasers can coexist with silicon for the future generation of CMOS optical interconnects.

1.2 Nanolasers and photodetectors

Miniaturization of optical components is essential for intra-chip optical interconnects. Scientists are therefore investigating micro- and nano-laser sources that can be integrated on-chip.
To implement an optical link, a crucial component is an electrically-driven and compact light source with low energy consumption. For this reason we will examine different designs of nanolasers in Chapter 2, discussing advantages and disadvantages of different configurations and correlating devices, performances, and energy requirements. However an optical link also needs efficient detectors and that is why we discuss the latest results on the topic later in this section.

Although the "nano" prefix in the word nanolaser describes a laser with small physical sizes, it has to be intended from an optical point of view as a device with a cavity mode volume of $0.1\,\mu m^3$ or less. The mode volume is a measure of how tightly the mode is localized into a cavity and for example Photonic Crystal (PhC) nanocavities are good candidates for very small mode volumes, since the PhC geometry allows small changes that lead to ultra-low mode volumes [8].

In this work we fabricate and characterize ultra-small devices, however the manufacture of the smallest-ever-fabricated laser is beyond the scope of this project. We want to focus on nanolasers that are small from an integration point of view, but still big enough to provide the required output power for the detection site. For intra-chip optical interconnects nanolasers

are light sources that have to send data across the chip, but light sources themselves are not enough for signal processing: photodetectors and modulators are important as well [5]. Germanium photodetectors can for instance guarantee a fully compatible integration with CMOS technology, as it was proposed by Huang et al. in [9] or with a more sophisticated approach of monolithical integration of Ge photodetectors by Ahn et al. in [10]. More recently Balram et al. investigated Ge-based photodetectors with a planar nanometallic resonant cavity: the metal-dielectric cavity enhances Ge absorption improving the device performance for telecommunication applications [11, 12].
In other words, photodetectors and lasers have to follow a parallel development in order to be employed in real optical wiring and that is why improvements in both light sources and receivers are needed.

1.3 Photonic Crystals

What are photonic crystals? PhC are defined as low loss dielectric materials with periodic regions of high and low refractive index, with periodicity on the order of the wavelength of light [13]. This periodicity induces a very high reflectivity in a spectral range for which light cannot propagate in the crystal, similar to the energy gap formed in a semiconductor crystal. In PhCs the spatial variation of the crystal influences and hence changes the dispersion relation, which is the link between the photon energy and the wave vector. Changing the structural parameters of the crystal results in the modification of the propagating modes and therefore the dispersion properties can be engineered for different applications. PhCs have the capability of integrating many different devices such as amplifiers [14], all-optical memories [15], lasers, and switches [16] on the same platform. A reference for a detailed description of the theory of PhCs can be found in textbook "Molding the Flow of Light" [13].

1.3.1 Why photonic crystals

Confining and emitting light, where the physical dimensions can be compared to the diffraction limit of light, is quite a complicated task. A feasible approach for the nano downscaling is using PhCs. Even though photonic crystals are not the only way to solve this task, we believe it is the most efficient for several reasons:

1) Notomi et al. in [17] discuss how PhC can realize strong light confinement through the photonic band gap (Photonic Band Gap (PBG)). PhC can effectively increase light-matter interaction leading to small devices because of small cavities and high Q design that is essential for dense photonic integration. Furthermore a stronger light-matter interaction can be used to improve performances of nanophotonic devices such as lasers, switches, and memories.

2) In 2005 it was shown that the PhC platform can also be used to "slow-down" light [18]. A more recent demonstration of manipulating light on PhC membranes [19] reports that slow-light enhances the effective gain of the material enabling ultra-compact optical amplifiers for integration on photonic chips. Due to the PhC design and including slow-light properties, Krauss in [20] investigates the benefits of the slowdown factor for linear and non-linear effects, since Hughes at al. in [21] previously demonstrated that losses scale as the square of the slowdown factor; this result makes PhCs even more appealing if losses can be reduced.

3) Plasmonic is the most well-known way to downscale components: metallic cavities of a few hundred nm size can easily be fabricated. However no matter the small dimensions, good thermal performances and room temperature Continuous Wave (CW) operation of such devices are still far from what the actual requirements for optical interconnects are [5]. Furthermore the intrinsic use of metal introduces higher losses, thus plasmonic becomes a less suitable technique than PhCs. Ding et al. in [22] discuss some fabrication challenges for nanometallic cavities: due to the ultra-small cavities even microscopic processing imperfections can significantly degrade already small cavity Q-factors and increase thresholds beyond the optical gain achievable in semiconductors. An enriched version of metallic nanocavities is given in [23], where the Bowtie design has been used. Even with this new proposed design for plasmonic nanolasers, lasing was not

observed at room temperature.

4) PhCs can be employed to fabricate small cavities with both a high quality factor and a small modal volume. With these conditions the Purcell enhancement of spontaneous emission can become large enough to affect the dynamics of a device as demonstrated in [24, 25]. In particular the Purcell enhancement is shown to contribute to a very fast modulation speed [26]. Moreover Ek et al. investigated how an enhancement of the amplified spontaneous emission can be observed close to the bandedge, where light is slowed down due to photonic crystal dispersion [14]. The observations are explained by the enhancement of net gain by light slowdown [14]. However scientists are still debating on whether the enhanced spontaneous emission of small cavities that can be funneled into the lasing mode can decrease the coherence of the lasing output modifying the overall performances.

5) PhCs can be used to control the spontaneous emission from emitters embedded in the crystal [24]. It is possible to inhibit emission as well as increase it by placing an emitter in a cavity [27]. The emission is increased due to the Purcell enhancement, which is caused by the overlap between the emitter and the optical density of states of the cavity structure.

6) For on-chip optical interconnect integration electrical injection is a strict requirement. PhCs and in particular PhC membranes are compact structures with a design that allow an easy accessibility for metal contacts without major modification in the device processing. A more detailed overview on electrical injection is given in Chapter 2.

1.3.2 History of photonic crystals

The concept of PhCs first appeared in 1979, when Ohtaka [28] described the photon band structure as an analogy to the electronic bandgap, however he did not postulate the existence of a PBG. The demonstration of a new paradigm where the band structure concept of solid-state physics is applied to electromagnetism creating a photonic bandgap is published in 1987 with the contribution of both Yablonovitch [29] and John [30].

PhCs belong to Nature: the eye of the peacock feather [31] and the wing-scales of the Morpho butterfly originate from a periodic biological nanostructuring of the feather or wing [32]. Despite the absence of color pigments, both the Morpho butterfly and the peacock exhibit striking colours.

These effects occur because lightwaves in a structural periodic material experience a periodic perturbation due to the nano-structuring that make them behave in a different way than in a homogeneous material. This situation is analogous to electrons in crystalline solids. In crystalline solids electrons are scattered by the periodic potential of the atoms: electrons with specific energies are allowed to propagate in specific directions, while others are prohibited to propagate in certain energy regions referred to as bandgaps. Similar to electronic bands in condensed matter physics, the analogy between electrons in a crystalline solid and photons in a periodic material suggests the evidence of photonic bandgaps, where the propagation of certain light frequencies is forbidden. The design of PhCs is quite flexible, since it can be be scaled in order to match the bandgap region in the desired wavelength range. Indeed the first experimental demonstration of PBG was in the microwaves [33], where light can be confined in the millimeter range, while for a later PhC demonstration in the infrared regime [34], micrometer structures and therefore much higher fabrication resolution are required. For infrared applications the demand on fabrication technology increases, since the photonic crystal periodicity has to the be on the order of the wavelength of the confined light.

1.3.3 Photonic crystal types

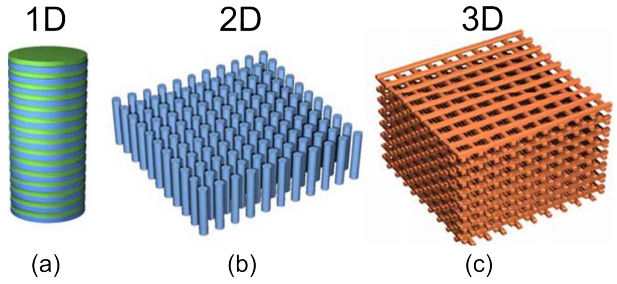


Figure 1.1: Schematic illustration of (a) 1D, (b) 2D, and (c) 3D photonic crystal, adopted from [35].

A complete PBG implies an omnidirectional bandgap, which is independent on the propagation of the lightwave. A remarkable difference among PhCs relies on how many dimensions light can be confined, as shown in Figure 1.1 for structures that can confine light in one, two or three dimensions.

3D PhCs are quite challenging to fabricate [13]. For 3D light confinement (3D bandgap) a good 2D compromise is PhC slabs [36], later discussed

in section 1.3.4. In the case of PhC membranes light is confined by a combination of total internal reflection (TIR) in the direction perpendicular to the crystal and the Bragg reflection from the PhC pattern in the in-plane direction. Furthermore PhC devices fabricated with semiconductors offer:

- A strongly modulated crystal can be created by etching air-holes into a high refractive index semiconductor material (n > 3), and a refractive index ratio of at least 2 is achieved, which is a requirement to obtain 2D or 3D PBGs [37, 38].
- Direct bandgap semiconductors can be manipulated to emit light at a wavelength within the photonic bandgap of the PhC design.

1.3.4 Photonic crystal membranes

As mentioned in section 1.3.3, the 3D PhC approach is quite difficult to fabricate and that is why the 2D PhC slabs are used in this work, with the consequence that the bandgap is only defined in two dimensions, covering a limited range of directions for a certain polarization. Despite the "incomplete" bandgap, an appropriate design of the 2D bandgap can work in a very similar way to a complete PBG. The geometry of the crystal is chosen as an hexagonal array of holes, defined in a slab of semiconductor material. The hexagonal lattice is chosen because it can result in the largest 2D PBG in TE-polarization (the electric polarization parallel to the 2D plane) [39]. In a standard (bulk) PhC structure the repetition of a specific pattern is the unit cell for obtaining light confinement, however when a defect is included in the crystal pattern, it is possible to create cavities that can confine light in a very small volume on the order of a cubic wavelength [40], resulting in a strong light-matter interaction in the cavity. If a full row of defects is introduced, a waveguide (WG) can be fabricated (missing row of holes). By tailoring the dispersion of the waveguide it is possible to slow light down, create components such as delay lines and optical buffers and increase light-matter interaction in the WG [41]. PhCs are a versatile platform where cavities and WGs can be coupled for the realization of optical circuits [13].

Defects, such as a missing row of holes or single holes that have a bigger or smaller dimension compared to the crystal, may allow localized modes to exist, with frequencies within the PBG, as shown in Figure 1.2. The details about dielectric and air band definition on the low and high frequency side of the bandgap will be discussed in Chapter 2 for the designed PhC pattern. Figure 1.2 exemplifies that when a single defect (missing hole) is

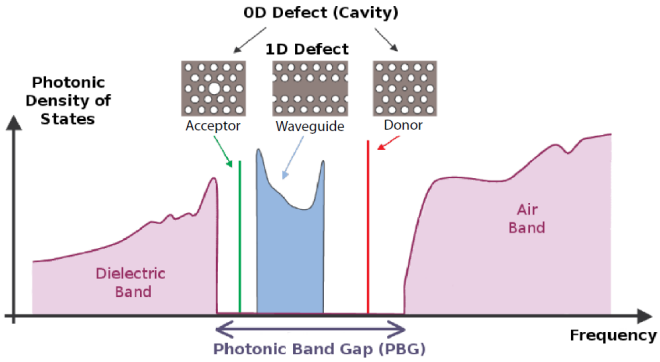


Figure 1.2: Schematic representation of the photonic density of states (DOS) for a PhC. Defects such as waveguides or cavities create modes within the PBG which are very well confined in the crystal [14].

created, the pattern works as a cavity where the localized mode is trapped, because it has a frequency inside the bandgap. The defect mode decays exponentially away from the defect and it is localized in two dimensions, while it extends in the propagation direction. When a row of holes is missing, a line defect mode is trapped inside a WG, since its frequency is in the forbidden energy gap. In this fashion light cannot leak out into the surrounding material. However, in the out-of-plane dimension the guiding mechanism is still given by TIR. When light in a high index material sees an interface of a low index material, it may be transmitted or reflected depending on the incident angle. If the angle is greater than the critical angle, all light is reflected back into the waveguide, according to Snell's law of refraction. For optimal vertical confinement the 2D PhC is implemented in a membrane surrounded by air. This option enables low transmission loss through sharp bends, which is a desired feature for guiding light in a dense network of devices.

1.4 State of the art of PhC lasers

This section is dedicated to an excursus about the PhC platform evolution from optical pumping to the recent electrical pumping for the future application as optical interconnects. Since the fist III-V semiconductor PhC demonstration in 1994 [42], the 2D photonic crystal slabs have been employed for device realization and characterization. The first approach for laser characterization was optical pumping, while a few years later electrical

pumping was introduced. As the possible device application concerns the telecommunication field, lasers should operate around the wavelength of 1.55 µm, where the minimum transmission loss of common optical fibers is reached. In the particular case of only on-chip level applications, the operative wavelength could be chosen in a larger infrared range with a minimum value of 1.15 µm, where silicon is transparent.

For the monolithic integration of light sources on chip diverse characteristics are required. These high-performance light sources must have a compact footprint, provide reasonable power levels under electrical CW operation at room temperature (RT), and preferably emit in the in-plane wafer direction to better facilitate coupling to waveguides.

1.4.1 Optical injection

After the establishment of PhCs as an excellent and versatile tool, devices built on cavities and waveguides have been designed and studied. The characterization begins in pulsed regime and at low temperatures. Due to the conformation of 2D photonic crystal slabs, material gain, and material choices, thermal issues cannot be neglected, so that diverse strategies are applied in order to get CW and RT measurements. The first demonstration of PhC lasers with InGaAsP Quantum Wells (QWs) was reported in 1999, where measurements have been carried out in pulsed regime and at the temperature of 143 K [43]. In order to benchmark CW and RT operations several platforms can be considered.

One possibility is to use the bonding technique, in order to address the heat generation issue. Fusion bonding between InP and GaAs with aluminum oxide has been reported to be successful to achieve RT operation in [44] and even the CW regime in [45]. Both RT and CW operations have been achieved with the method of wafer bonding on silicon with either SiO_2 [46] or the adhesive benzocyclobutene (BCB) bonding [47]. Improved thermal properties have also been shown through sapphire bonding [48, 49], where heat conductive claddings have been introduced. Even though the strategy of bonding helps the reduction of heat, the input power thresholds are still on the order of mW, which are high power levels compared with other optimized and non-bonded 2D PhC membrane devices. Low threshold lasers in pulsed regime have been reported in [50, 51]. In [50] the characterization of both single cavity perturbations and rows of defects define new laser designs. In [51] a comparison between PhC with free-standing membrane and SiO_2 epoxy-bonded is carried out. For the free-standing devices the best vertical confinement is observed, while improved thermal properties at

the expenses of vertical confinement are observed for the bonded devices. Optical pulsed pumping and RT have also been achieved with a modified version of a 2D PhC slab with a "post" underneath the cavity [52]. This new structure paved the way to the first low-threshold electrically pumped PhC nanolaser [53].

The optimization of the PhC design is also a winning strategy for CW and RT operations, as shown in [54], where the smallest power threshold on the µW order has been measured.

The last technique to improve thermal issues for optically pumped devices is the choice and the extension of the active material. Quantum Dot (QD) lasers possess small active volumes on the order of the dot size. As a result of the small active volume, RT, CW and a low-threshold power of 2.5 µW have been reported for InAs QD PhC lasers [55]. A developed version of QD PhC lasers on Si substrate with low input threshold has been reported in [56], as first demonstration of III-V devices wafer bonded to silicon with low power consumption.
The incorporation of a buried heterostructure (BH) in a PhC laser is another successful way to reduce the active volume and improve thermal dissipation, carrier confinement and optical pumping efficiency. The first BH PhC laser with the ultra-low input power threshold of 1.5 µW has been demonstrated at RT and CW operation [57]. With the development of an advanced PhC pattern ultra-compact BH PhC nanocavity lasers, with integrated in-plane input and output waveguides on the PhC design, have been reported [58]. The devices exhibit a low input power threshold of 6.8 µW, with a high direct modulation of 20 Gbit/s, resulting in the smallest energy cost per bit of 8.76 fJ/bit until then reported.

1.4.2 Electrical injection

Electrical injection for nanolasers is a challenging task. One of the main issues that has to be solved is how to integrate electronics and optics on the same platform, since diverse requirements are needed. When electrical injection is added to optical devices it is usually at the expenses of optical properties and vice versa, so that a good compromise has to be sought.

There are two possible strategies for electrical injection: vertical electrical injection [53] and lateral electrical injection [59]. The difference consists in the diverse path the current has to follow and therefore in the placement of doped layers and metals contacts. In the case of vertical current injection (VCI) the doped layers are on opposite sides of the PhC membrane (top and bottom), while in the case of lateral current injection (LCI) the

doped regions are embedded in the photonic crystal membrane through ion-implantation and thermal diffusion on opposite sides of the cavity (right and left). To achieve VCI, the doped regions are fabricated during the epitaxial growth of the wafer, whereas for LCI the doped regions have to be defined with ion implantation and carrier diffusion.

The first demonstrations of vertically electrically pumped PhC lasers at RT and in pulsed regime consists of surface-emitting lasers with the introduction of a 2D PhC design and fusion bonding technique [60, 61]. The diverse combination of a PhC design and plasmonic properties led to the demonstration of surface-emitting quantum cascade microcavity lasers in pulsed regime and at RT [62]. These devices [60–62] still exhibit large mode volumes and high threshold currents that do not permit CW operation. Thus a new approach for the photonic crystal design and thermal properties has to be investigated.

In 2004 Park et al. [53] reported the experimental demonstration of an electrically driven, single-mode, low threshold current (260 µA) photonic bandgap laser in pulsed regime and at room temperature. In this new design a vertical electrical injection scheme is shown for the first time: apart from a PhC slab, a central post under the point-defect cavity is fabricated in order to electrically pump the device. This novel scheme was already reported successful with optical pumping [63], where by PhC and membrane thickness engineering the monopole mode was confined. The introduction of a post under the center of the cavity - for small sizes - should not compromise the laser quality factor, since the mode has its intensity minimum in the center. Despite the novelty of VCI achieved by a current post, optical properties of the laser can be degraded if an accurate PhC design is not carried out [53, 64]. In this configuration thermal properties should be improved compared to a pure PhC membrane device, since the post can also act as heat sink [65].

The lateral current injection (LCI) scheme was proposed by Choquette et al. in [59] in order to excite 2D PhC membrane light emitters. This new strategy has been successfully applied by Ellis et al. in [66], where electrically pumped PhC QD lasers with ultra-low current threshold in CW regime have been demonstrated. Despite the small threshold current of a few hundreds of nA, the lasing condition could only be implemented at cryogenic temperatures. The gain and thermal configurations at RT were indeed fatal for the same type of devices presented in [67], where no lasing was achieved at RT.

Only with a confined active region with a BH design laterally injected PhC

lasers at RT and in CW regime have been reported [68]. Despite this remarkable result, the relatively high current threshold of 390 µA was a synonym of leakage current through the InGaAs sacrificial layer. One way of solving leakage issues has been the introduction of InAlAs as sacrificial layer [69, 70], which allowed 4.8 µA and 7.8 µA current thresholds respectively. Besides the employment of a new material for the sacrificial layer, the improved device performances have been obtained because of the current-blocking trenches design within the PhC cavity, which additionally decreased the power consumption [69].
On-chip CMOS light sources integration requires a silicon compatible platform. The great potential of lateral electrical injection of low threshold III-V PhC lasers with BH design wafer bonded to Si has been recently demonstrated [71]. In this work BH PhC lasers exhibit the low current threshold of 31 µA in CW and RT operation.

Despite all the successful electrically injected lasing devices listed above, a lot of papers have been published on electrical injection of PhC light-emitting devices, where the lasing condition could not be achieved. Several groups tried to develop electrically pumped PhC lasers [67, 72–75] but they could only observe enhanced properties of PhC emitters.

Low threshold PhC lasers with either VCI or LCI have been presented. The controversial matter on which of the two injection strategies can be the most compatible with CMOS technology for on- and off-chip optical interconnects with ultra-low power consumption is still an open issue. The requirements on optical, electrical and thermal properties that have to be simultaneously met, increase the challenges for device realization leading to big room for improvements for the fabrication of the best performing nanolasers.

1.5 Aim of the project

In this project modeling, fabrication and characterization of electrically pumped PhC lasers with a vertical injection scheme have been pursued.

The optical design is characterized by the implementation of a double hetero-photonic crystal with a line-defect waveguide design. This choice has been made according to the fabrication possibilities available at the beginning of the project, which could not rely on BH expertise. The strategy of using a BH would be more effective than uniform active material (QWs), because of better carrier confinement in the laser cavity. The BH design can be implemented as an optimized version of these devices, when the BH

regrowth capability is achieved. In order to achieve current injection the strategy of a vertical injection scheme has been followed. The electrical design consists of a pillar under the PhC membrane, which is a structure that can efficiently inject carriers (holes) into the laser cavity. Although the possibility of a lateral injection scheme with uniform active material could have been considered, the conducted simulations proved the inefficiency of this design.

The sample and the view of the fabricated devices are depicted in Figure 1.3. In Figure 1.3(a) the size of the final piece of sample is given, approximately equal to a 1/4 of a 2" wafer. In Figure 1.3(b) a microscope top-view represents a typical double heterostructure PhC device with vertical electrical injection scheme. The current path achieved through a post under the PhC membrane can be observed in Figure 1.3(c), where a scanning electron microscope (SEM) image of a device is presented. The devices are fabricated through a double-side processing, where on the first side the pillar is fabricated and after adhesive bonding to silicon the second side of the PhC pattern is fabricated. For the PhC scheme the evaluation of two e-beam resists (hydrogen silsesquioxane (HSQ) and ZEP) have been considered.

Even though the main goal of the project is to fabricate electrically pumped nanolasers, due to diverse fabrication issues only electrically pumped PhC light-emitting devices have been obtained.

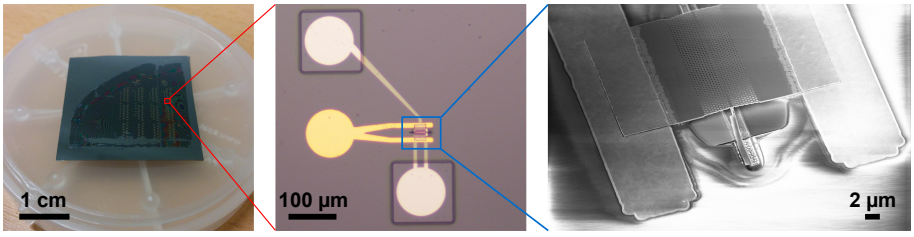


Figure 1.3: (a) Sample top-view after fabrication processing. (b) Microscope top-view of a single device. (c) SEM tilted-view of a device with focus on the membranized PhC and the injection pillar structure.

1.6 Thesis outline

In Chapter 2 the modeling and electrical and thermal simulations of electrically injected devices is conducted and considerations about the results

are given. Chapter 3 describes the development of the fabrication process of double heterostructure photonic crystal lasers with a pillar structure for vertical current injection analyzed throughout the project. In Chapter 4 the electrical and optical characterization of the devices is presented. In Chapter 5 the design and characterization of PhC nanobeam devices is given. Chapter 6 concludes the work and gives an outlook for future investigations and improvements on the established platform for the next generation of optical components compatible with CMOS technology.

In addition in Appendix A all the parameters used for the simulations are given. Appendix B comprises a detailed description of each fabrication step used for the processing.

Chapter 2

Design: Optical and Electrical Modeling

In this chapter the optical and electrical modeling of the devices and current injection concepts are described. The choices of the optical design are made through an analysis of the Photonic Crystal (PhC) pattern. Afterwards analyses, considerations and discussions about electrical injection and thermal properties of the models are given.

2.1 Aim of the design

We have chosen to investigate, design and fabricate a vertically injected laser. For the optical part we employed a hetero-photonic crystal cavity achieved by a W0.98 waveguide and a change in the lattice constant of the cavity that is elongated compared to the one of the mirrors. For the electrical injection we relied on a post under the PhC membrane, which we believe is a good structure to inject carriers into the cavity and to remove generated heat from the device. The design, presented in Figure 2.1 with a schematic in (a) and a SEM image in (b), is relatively complicated, since it has to meet conflicting requirements concerning optical and electrical properties. The buried heterostructure (BH), the best way for optical confinement with a double heterostructure PhC configuration [69], is not pursued for an initial lack of fabrication expertise, but it should be implemented as an optimized version of these devices. Furthermore a BH allows passive and active components integration and passive PhCs, since the active material is localized. Instead of vertical injection, lateral current injection could have been used. However, as our simulations show, a lateral injection scheme with uniform

active material is not an efficient design, whereas if the BH can be fabricated in a lateral injection scheme, it is a very promising configuration.

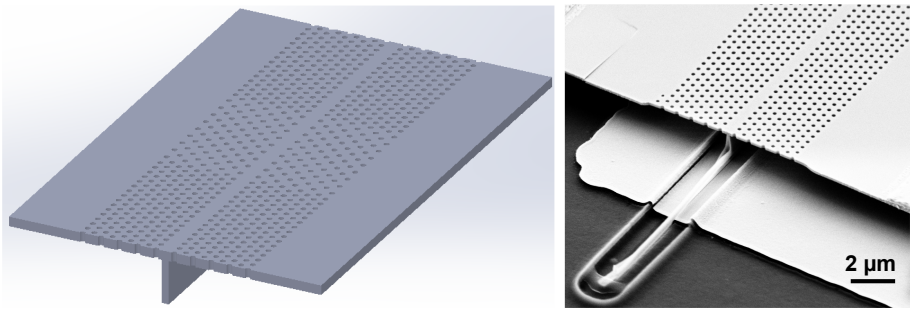


Figure 2.1: (a) Schematic and (b) SEM views of the double heterostructure photonic crystal device with pillar for electrical injection.

2.2 Optical design

2.2.1 Double heterostructure photonic crystal approach

The carrier confinement is one of the first requirements for a low threshold laser. This issue has been solved by NTT with the BH design [68–70]: for a BH the active low bandgap material is confined into a determined region, so that carriers can easily be localized. Together with the active material in a BH design, the PhC pattern enriches the devices creating a double heterostructure photonic crystal device. In the case of BH the photonic crystal double heterostructure is achieved through the material refractive index difference between the laser cavity (confinement of active material) and the mirrors (passive material). This approach has proved itself to be successful, but it is demanding and it requires a lot of expertise and optimization steps. Due to an initial lack of BH expertise, it was decided to implement the carrier confinement with a different technique exploiting the PhC design.

For our devices in the in-plane direction there is no change in the material refractive index, unlike the BH design, since the layers are uniformly grown with metal-organic vapor-phase epitaxy (MOVPE) (InP membrane with either InAs QDs or InGaAsP QWs). An engineered PhC design is therefore required to achieve the heterostructure cavity, which becomes a double hetero-photonic crystal cavity. In this case the diverse manipulation of the

PhC pattern in the cavity and in the mirrors gives the overall index change for the double heterostructure design. Thus a double heterostructure photonic crystal design can be achieved both through a BH (active and passive material refractive index change) and with PhC manipulation (overall index modulation). These two techniques can generate PhC modulated mode-gap cavities (principle depicted in Figure 2.2d), where strong light confinement can be achieved [17]. Song et al. first introduced the idea of heterogeneous interfaces in PhC patterns, simply changing the lattice constant between one PhC region and the following one [76]. A further demonstration of waveguides with hetero-photonic crystal interfaces has been investigated in [77], where a frequency-gap for modes that can be guided in one PhC region and not in the following one has been observed. One year later the same group reported the fabrication of double heterostructure PhC cavities with a record-level quality factor of 6×10^5 [78] in the case of a 2D PhC slab with line-defect waveguide. This high-Q nanocavity record could only be achieved with the double heterostructure PhC design. A previous demonstration of high-Q cavity with the hole tuning/shifting approach [79], gave an experimental Q-factor of 4.5×10^4, which is not sufficient for the ultimate high-Q cavity.

A schematic representation of the principles and design of a double hetero-photonic crystal structure is shown in Figure 2.2, adopted from Nature Materials [78]. In Figure 2.2a the basic 2D PhC triangular lattice structure with a line-defect waveguide formed by a missing row of holes is shown. In Figure 2.2b the calculated band structure is represented. Due to the photonic bandgap, along the waveguide only specific modes are allowed. If the geometry (lattice constant) is changed and therefore the guiding mode at the bandedge is lowered (red arrow in Figure 2.2b), the propagation is inhibited, while if the mode is raised (blue arrow in Figure 2.2b) propagation is allowed through the waveguide. Figure 2.2c shows the double hetero-photonic crystal structure. In our design the two regions I located at the sides of region II are the laser mirrors, which have the standard geometry as in Figure 2.2a. Region II is the laser cavity, whose lattice constant is elongated in the waveguide direction and it is the same as region I in the orthogonal direction due to lattice matching conditions (rectangular face-centred lattice structure). Figure 2.2d represents the band diagram in the waveguide direction of a mode-gap cavity: due to the lattice constant difference, photons with a specific energy can exist only in the cavity, where both regions I act like laser mirrors.

Inspired by double hetero-photonic crystal cavities design, we decided

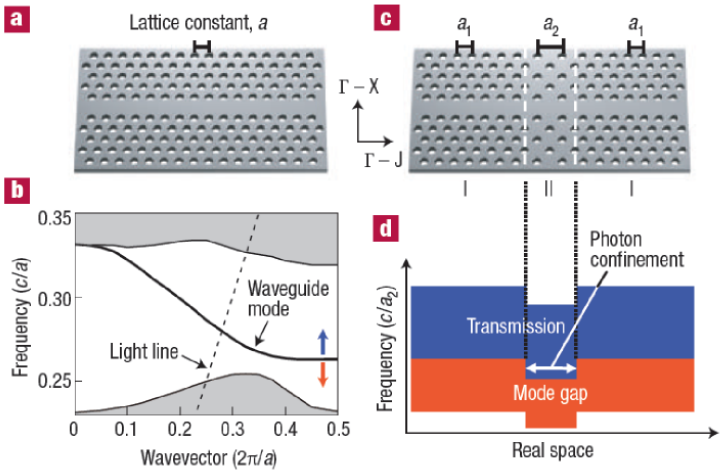


Figure 2.2: Figure adopted from Nature Materials [78]. Schematic of a 2D photonic crystal structure and photonic double-heterostructure. a) A PhC slab with triangular lattice and waveguide made by a missing row of holes. b) The band-structure representation of a). The blue arrow indicates the transmission region where the propagation of photons is allowed through the waveguide and the red arrow indicates the mode-gap region in which propagation is inhibited. c) Photonic double-heterostructure constructed by combining two photonic crystals structures (I and II). The photonic crystal region I has a triangular-lattice structure with a lattice constant of a1 and the photonic crystal II has a deformed triangular-lattice a2 (>a1) in the waveguide direction. In the orthogonal direction the same lattice constant a1 is applied to maintain lattice-matching conditions. d) Schematic of the band diagram along the waveguide direction. Photons of a specific energy can exist only in the waveguide of photonic crystal II, thus region I functions as mirrors.

to employ this type of design with 2D PhC slab with line-defect waveguide formed by a row of missing holes in the $\Gamma - J$ direction. The heterogeneous interface between the cavity and the mirrors can be designed mainly using two techniques: changing the hole size while keeping constant the pitch or conversely changing the pitch while keeping constant the hole size between neighbouring PhC regions. Due to any possible fabrication imperfections we imagined that the change in the PhC lattice constant is easier to control than the change in the hole size, since the PhC holes have to be written with e-beam lithography and processed through etching. A similar approach has previously been reported in [80]. The choice of a double heterostructure photonic crystal design with PhC pattern modulation allows a continuous

pillar under the membrane for electrical injection. In principle, if the pillar was fabricated only under the cavity, no PhC pattern manipulation would be required for the index modulation. Unfortunately, when this type of design was theoretically modeled, we discovered that the pillar degrades the laser performance due to mode-mismatch between cavity and mirrors. Thus the pillar continuity under the entire PhC pattern is necessary to guarantee the mode matching condition.

The choice of the geometrical parameters and a schematic of our double heterostructure PhC cavity can be found in the following section 2.2.2.

2.2.2 Photonic crystal design

The optical design, presented in Figure 2.3, requires two criteria that have to be simultaneously met: a hetero-photonic crystal structure depicted in Figure 2.3(a) with a high-Q cavity and a current injection path that we designed as a post under the PhC membrane for the vertical electrical injection as presented in Figure 2.3(b). For the simulation and optimization of the PhC design, specific boundary conditions due to the 2D symmetry can be made. The initial dispersion diagram of a PhC slab device with pillar under the membrane has been calculated through the electromagnetic eigenmode solver MPB in the frequency domain.[1] Even though the electrical injection design will be discussed in more details in section 2.3, some considerations have to be taken into account for the optical design, in order to have a good and possibly high-Q cavity. It has been mentioned earlier that the optical design consists of a modified version of a basic PhC slab with a line-defect waveguide and therefore the current post needs to be placed under the waveguide. Its width needs to be less than the waveguide width. The width constrains of the pillar are considered imprimis for an optical confinement issue: if the pillar is too wide there is risk that the optical mode is not confined in the PhC slab, but can leak into the current post. From a theoretical point of view for an optimal PhC membrane cavity the size of the pillar should be close to zero. Although this is not realistic and no current injection would happen because of carrier depletion, the pillar width has to be small enough for the optical mode not to leak into the pillar and it has to be wide enough for the carriers to start the electrical injection.

For the optical design a lot of parameters such as slab thickness, lattice constants and hole radius size have been calculated through a FEM mod-

[1] The optical MPB (MIT Photonic Bands) calculations have been made by Postdoc Yaohui Chen, DTU Fotonik.

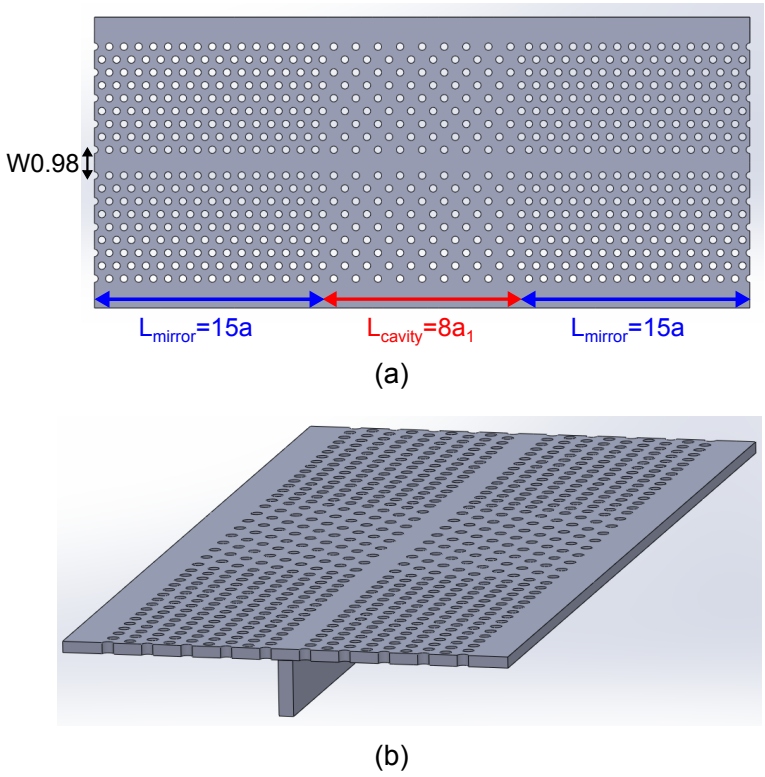


Figure 2.3: (a) Schematic top-view of the double hetero-photonic crystal design. In the laser cavity the lattice constant (a_1) is elongated compared to the mirrors (a). The cavity length is $8a_1$, while the mirrors are 15a long. (b) Scheme of the whole device with PhC membrane and a post for electrical injection under the line-defect waveguide.

eler with solutions in the frequency domain.[2] The pillar width constrain was fixed in a small range between 100 nm and 250 nm according to similar designs with vertical electrical carrier injection proposed in [81, 82]. The height of the pillar is also important for the mode confinement. If the pillar height is too low, it is more likely that the optical mode can leak into the pillar, giving high optical losses. A too high pillar could be difficult to fabricate and it could give troubles with current injection. Inspired by the first ever demonstrated electrically pumped PhC laser by Park et al. [53]

[2]The FEM (Finite Element Method) code has been implemented in COMSOL Multiphysics modeling software. The code and the calculations have been carried out by Postdoc Yaohui Chen, DTU Fotonik.

and driven by thermal considerations the InP pillar height has been fixed to 1 µm in our design.

For the PhC design two different patterns have been included and fabricated: a double hetero-photonic crystal cavity with electrical injection structure under the line-defect waveguide and a double hetero-photonic crystal cavity with both vertical injection and in-plane outcoupling waveguide, depicted in Figure 2.4(b) and (c) respectively. In the first type of design the light emission can be inspected as scattered light from the top of the device, which has previously been observed in [66]. For the second type of design an output waveguide is included in the PhC membrane, that is equivalent to the design presented in [58]. In the following the parameters of the PhC double heterostructure design are listed and briefly discussed:

- For the hetero-photonic crystal cavity a stretched lattice constant is chosen for the laser cavity and it is related to the mirror/vertical lattice constant by a defect of ~0.04% stretch in the waveguide direction.
- The waveguide line is W0.98, which is 2%, smaller than the traditional line-defect W1. This choice was based on both by the idea of output waveguide implementation and by the presence of a heterostructure. In the laser cavity one would want to operate at the bandedge, where slow-light regime can be achieved, while for the mirrors and the output waveguide a different regime is needed. W0.98 gives a slightly bigger separation between even and odd modes of the PhC, giving more chances to operate in a single-mode regime, which is preferred in order to reduce the complexity of the whole device [83]. A schematic representation is given in Figure 2.4(b).
- The output waveguide is W1.1 with the missing holes at row #5 in the mirror with the following rows to be shifted to $0.1 \times \sqrt{3}\times$ the mirror lattice constant. A schematic is represented in Figure 2.4(c).
- Since the desired laser resonance is around 1550 nm, a range of PhC holes was calibrated with a radius of 110 nm, 115 nm, and 120 nm, in order to cover the defined frequency range.

The final parameters for the optical design are listed in Table 2.1. The evolution of the optical design is represented in Figure 2.4: an intrinsic double heterostructure PhC cavity in Figure 2.4(a), a double heterostructure PhC cavity with pillar for vertical electrical injection in Figure 2.4(b), and a double heterostructure PhC cavity with in-plane outcoupling waveguide and

with pillar for vertical electrical injection in Figure 2.4(c). Schematics (b) and (c) of Figure 2.4 are the ones that have been used for the device fabrication. The estimated cavity Q factors for the PhC designs in Figure 2.4 are 7.3×10^5, 1.4×10^5 and 2.0×10^4 for the intrinsic double heterostructure PhC cavity, the double heterostructure PhC cavity with pillar for vertical electrical injections and for the double heterostructure PhC cavity with the post for the vertical injection and output waveguide respectively.[3]

Table 2.1: Parameters for the photonic crystal design.

Parameter	Value [nm]
Slab thickness	220 nm
Lattice constant mirrors	438 nm
Lattice constant cavity	456 nm
Hole radius	110 nm, 115 nm, 120 nm

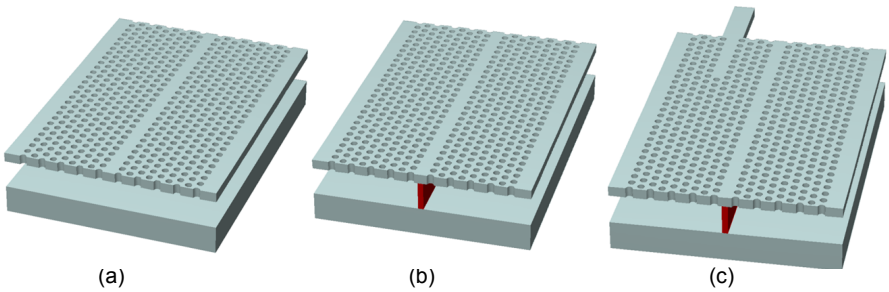


Figure 2.4: Schematics of double heterostructure PhC cavities. (a) Intrinsic double heterostructure PhC cavity. (b) Double heterostructure PhC cavity with vertical injection scheme. (c) Double heterostructure PhC cavity and in-plane outcoupling waveguide with vertical injection scheme. (b) and (c) represent the fabricated devices with PhC membrane design and a post for vertical current injection highlighted in red under the line-defect waveguide.

[3]FEM calculations made by Postdoc Yaohui Chen, DTU Fotonik.

2.3 Electrical modeling of existing PhC laser types

2.3.1 Geometry and parameters for the simulations

In this section three different electrical pumping schemes employed in the recently demonstrated PhC lasers are numerically investigated: a vertical p-i-n junction through a post structure [53], a lateral p-i-n junction with a homostructure [66], and a lateral p-i-n junction with a buried heterostructure [68]. Compared to the original lasers, the models have been simplified in order to allow qualitative comparisons among the concepts of different electrical injection schemes with different material and design configurations. For the evaluation of optical and electrical properties of the nanolasers, Lastip [84], a commercial 2-dimensional laser diode simulator that self-consistently solves optical, electrical, and thermal equations has been used. In the model the third dimension is assumed invariant and the $k \cdot p$ method and the drift-diffusion model are implemented to describe optical gain and carrier transport respectively [85]. All these results have been published in [86]. In Figure 2.5 the three investigated laser structures are presented: a lateral p-i-n junction with a BH active material shown in (a), hereafter designated as LBH; a lateral p-i-n junction with a uniform active material shown in (b), hereafter designated as LU; and a vertical p-i-n junction with a post for hole injection shown in (c), hereafter designated as VCP. In both the LBH and LU structures, the 0.9 µm-wide middle part is undoped, while the left and the right sides of this middle part are p-doped and n-doped respectively. In the undoped middle region designated as active region, stimulated recombination of electrons and holes is expected to occur. Both p- and n-metal contacts of 1 µm width lie on the top of the device. Current is laterally injected from the p-doped part on the left into the active region in the middle. Subsequently, it flows to the n-doped part on the right. The LBH and LU structures differ only in the extension of the active material, i.e., QW layers. In the LU structure, the QW layers extend in the entire lateral direction of the membrane, whereas the LBH structure has the QW layers confined only within the BH. This difference explains our denotation for LU as homojunction, since the active material extends to the full width of the device, while LBH is a heterojunction, since the active material is localized in the middle of the device. These structures share the same doping concentration in the right and left parts of the devices [87], as shown in Figure 2.5.

For the lateral electrical injection schemes, implantation defects and sur-

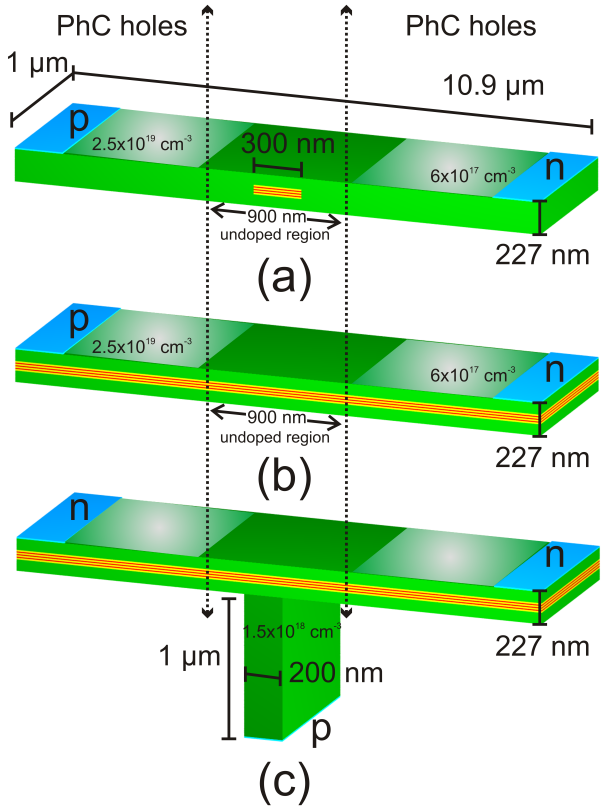


Figure 2.5: 3D geometries of the three modeled nanolasers: (a) LBH, (b) LU, and (c) VCP. The color legend is: green for InP, red for QWs, yellow for barriers, and light-blue for the metal contacts. On the devices p and n indicate the type and localization of the contacts. In (a) and (b) the entire doping concentration is reported.

face recombination are expected within the doped regions with PhC holes, since the doping process needs ion implantation or thermal diffusion. Their main effect is to obtain a faster quasi-equilibrium in these regions, but they have not been included in the modeling. Although their presence could increase the leakage current, the overall trend in the devices would be the same. This simplification has been considered in order to get a general overview about recently demonstrated injection schemes for nanolasers. In the VCP, the QW region is laterally undoped, since the doping is performed during epitaxial growth. Instead, the layer above the QW layers is n-doped, and only the post underneath the membrane is p-doped, which is a mod-

ification compared to the device in [53], where a layer in the quaternary membrane below the QWs is p-doped. The two 0.5 µm-wide n-metal contacts lie on top of the laser structure and the p-metal contact lies on the bottom, under the post structure. The current is vertically injected through the post into the QWs. Thereafter, it diffuses in the lateral direction as well as flowing vertically towards the n-doped top layer. The extension of the active region will be determined by the extent of the lateral diffusion of current.

In order to allow a fair comparison, minor modifications from the original structures in [53, 66, 68] are made, which are listed below.

- For all three models the same active material composition of InGaAsP QWs Q(1.65) and barriers Q(1.30) on InP substrate has been chosen.
- The LU model (based on [66]) has a uniform active region of QWs instead of QDs, since we needed all the devices to have nominally common characteristics and therefore the same type of active material, i.e. QWs, in order to analyze the differences in the electrical injection. Despite the simplification we made for the models, for real devices QDs would give better performances in structures like the LU, since QDs are less sensitive to surface recombination.
- In the VCP we design the post to be 200 nm wide based on previous studies [82]. The contact-pillar width has been established as a compromise between achieving an optical mode with low propagation loss (thin pillar) and low electrical losses (wide pillar), as reported in [82].
- For the VCP the p- and n-doped layers are all assumed to be InP, instead of Q(1.24), as in [53]. This hypothesis has been validated, since comparing the model with InP membrane (later discussed and fabricated) [86] and the previous version with quaternary membrane [87], we got better performances with InP devices due to the better thermal performances.

Concerning the doping of the VCP, the p-doping in the post is $1.5 \times 10^{18}\,\mathrm{cm}^{-3}$ and $2.7 \times 10^{19}\,\mathrm{cm}^{-3}$ n-doping lies in the top 60 nm InP membrane. More details about the settings for the simulations can be found in Appendix A. The VCP also has an intrinsic symmetric plane across the post structure, a property that has been exploited during the computation. The width of the structure is chosen to allow for a typical photonic crystal. If control of spontaneous emission is not required, this

width can be reduced. This will result in a reduced electrical and thermal resistance [88]. To accommodate the PhC region in the simulator, its optical and electrical features are modeled as follows: for longitudinal laser amplification condition, a 1 µm-long cavity with facet reflectivity of 99.5% is assumed. The transverse mode profile of the fundamental mode has been determined by three dimensional finite element method (FEM) simulations and it is therefore modeled in the simulator by using the Dirichlet boundary conditions. In this fashion the optical mode is artificially defined. With the chosen reflectivity value the loaded Q factor is ~1000, as can be calculated from the equation 2.1.

$$Q = 2\pi\nu_0 \frac{1}{c\alpha_r} = \frac{2\pi}{\lambda_0} \frac{d}{(-lnR)} \tag{2.1}$$

where ν_0 is the resonant frequency, c speed of light in vacuum, α_r the loss coefficient, λ_0 the resonant wavelength considered 1550 nm, d the cavity length assumed 1 µm, and R the mirror reflectivity assumed 99.5%.

This Q factor is chosen for all the models, assuming that the losses are dominated by the output, since the calculated intrinsic Q factor was one or two order of magnitude higher, as reported in section 2.2.2. We also assume a lowered carrier mobility in the lateral regions where the air holes would be located (reduced by the fill factor 25%) and an increased injection of spontaneous emission (β factor equal to 0.01) into the lasing mode. The thermal properties of the devices are not included in these simulations, but they will be discussed in section 2.5. In order to understand the performances of the simulated devices, we report the analyses on the electrical properties in section 2.3.2, the energy performances in section 2.3.3 and the leakage current issues in section 2.3.4. Self-consistent laser-diode simulations revealed that the lateral injection scheme with a buried heterostructure achieves the best lasing characteristics at a low current, whereas the vertical injection scheme performs better at a higher current for the chosen geometries.

2.3.2 Electrical properties

In Figure 2.6, the voltage and output power curves as a function of current (V-L-I) for the three laser structures are presented. The LU has the lowest threshold voltage of 0.84 V and the lowest resistance of 15.4 kΩ, the VCP has 1.03 V and 18.7 kΩ, and the LBH holds the highest values of 1.2 V and 39 kΩ. The lower electrical resistances in LU and VCP are attributed to the higher mobility of InGaAsP QWs layers than that of InP. Figure 2.8 shows that in LU and VCP cases the lateral current flows considerably within

the InGaAsP QW layers, while it flows mainly within the InP layer in the LBH.
It is worth remarking that although the resistances of the devices are very large, the operating voltage is comparable to conventional laser diodes, due to very low injection current. However, as the devices should ideally be driven directly from CMOS logic, the operating voltage may still be an issue. The details of the driving are an important topic for future research in laser sources for optical interconnects.

The threshold currents of each device can be found from Figure 2.6. The LU has the highest threshold current of 8.5 µA, the VCP 6.8 µA, and the LBH 0.6 µA. The employment of a BH as active material in the LBH leads to a threshold current more than 10 times smaller than in the other examined structures. This result manifests that a BH structure is a very efficient construction for confining carriers in the active material of nanolasers.

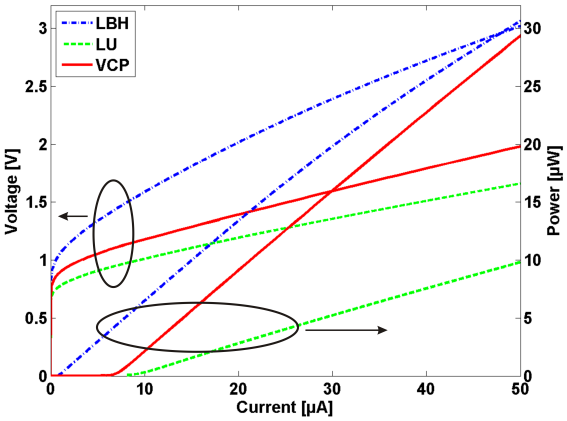


Figure 2.6: Voltage and output power as a function of injection current for LBH (blue dash-dot line), LU (green dash line), and VCP (red solid line).

2.3.3 Laser efficiency

Besides the traditional way of analyzing the efficiency of a laser, we introduced a different quantification of the laser efficiency for on-chip optical interconnects. For this reason, a new metric, i.e., number of output photons per bit as a function of energy/bit has been introduced, as shown in Figure 2.7. Indeed an adequate number of output photons in a bit is another important requirement as well as small energy/bit. This will be dis-

cussed further in section 2.3.5. At a specific energy/bit, a nanolaser should generate a sufficient number of photon/bit for efficient light detection. Otherwise, the nanolaser is not desirable for on-chip optical interconnects. In order to have a yardstick for further analyses, we can determine a theoretical limit for 1 fJ/bit and 100% wall-plug efficiency (WPE) of a 1550 nm laser to be 7800 photons/bit.

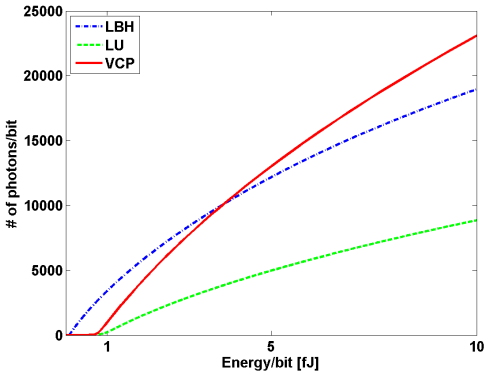


Figure 2.7: Number of output photons per "1" bit as a function of input energy per "1" bit for LBH (blue dash-dot line), LU (green dash line), and VCP (red solid line). A bit period of 100 ps is assumed.

From Figure 2.7, the LBH is the most efficient device at low energy/bit whereas the VCP becomes the most efficient above ~4 fJ/bit. At 1 fJ/bit, the LBH generates over 3300 photons/bit. This corresponds to 41% WPE. At the same energy/bit, the LU and the VCP generate 200 photons/bit and 800 photons/bit, respectively. The high efficiency of the LBH at low energy/bit can be attributed to its very low threshold current. The higher the energy is, the more efficient the VCP becomes. The lower resistance of the VCP than that of LBH with the chosen geometries gives rise to higher WPE at high energy/bit, overcoming the handicap of one order of magnitude higher threshold current than the LBH. The reason why the LU has the lowest WPE despite of its smallest resistance is discussed in section 2.3.4 in relation to leakage current.

Which set of energy/bit and photon/bit in Figure 2.7 is the most desirable is still an open question for at least two reasons: on one hand the future performance of photodetectors and transmission losses are uncertain, which may put a constraint on required photons/bit. On the other hand, the CMOS compatible laser driver possesses voltage and current, which de-

termines the energy/bit. These values should be coherent with the energy demands of the nanolasers for proper technology integration.

2.3.4 Leakage current

In order to explain the efficiency trend in Figure 2.7 and in particular why the LU has the poorest performance, considerations concerning the leakage current need to be taken.

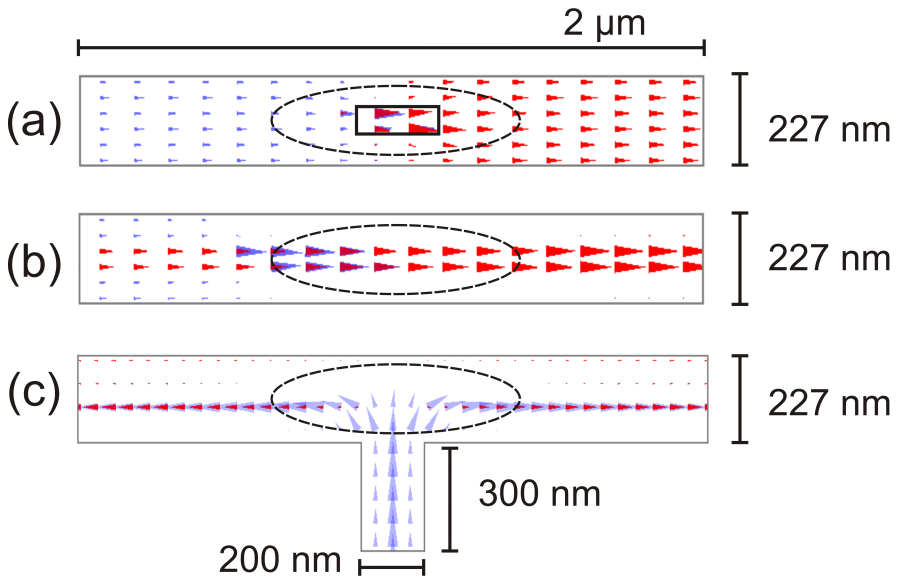


Figure 2.8: Vector plots of electrons (red cones) and holes (blue cones) currents at 5 µA injection current to evaluate contributions for recombination and leakage. (a) LBH, (b) LU, and (c) VCP structures. In each sketch the 30%-intensity contour of the optical mode has been drawn as a circle. In (a) the BH is designated by a rectangle. Only the central part of each structure is shown to visualize the important transition region and only qualitative information can be drawn from this plot.

In Figure 2.8 the vector plots of the separated contributions of hole current (blue cones) and electron current (red cones) are illustrated for the three laser structures with the same scaling factors. Recombination is represented by the transition from hole to electron current (blue to red). Leakage current is the minority carrier current, i.e. hole current in n-doped regions and electron current in p-doped regions. The electron leakage currents are quantified by integrating electron current at an interface between

the p-doped part and the undoped active region. The hole leakage current is quantified at an interface between the n-doped region and the active region.

In the vector plots in Figure 2.8, it is apparent that the current injection scheme reflects the type of leakage: in both lateral injection schemes (LBH in Figure 2.8(a) and LU in Figure 2.8(b)), the current leakage is dominated by electrons, whereas for the vertical injection scheme (VCP in Figure 2.8(c)), hole leakage current is the major contribution.

For the LBH, the leakage issue is negligible, since the heterojunction effectively keeps carriers in the BH active region (confinement of electron and hole currents). Additionally, the bottom and top InP layers are thin enough that carriers are efficiently funneled into the BH. Thus, the optical mode designated by 30% contour line in Figure 2.8(a) overlaps optimally with the BH active region with high carrier densities. This property explains the low threshold current of the LBH structure. The relatively high resistance is attributed to the lower mobility of p-doped InP, as stated earlier for the VCP structure.

In the LU case shown in Figure 2.8(b), the amount of leakage current is three orders of magnitude higher than in the LBH. This fact is attributed to the laterally-extended active material design of LU, which essentially forms a p-n homojunction in the QW layers. The homojunction makes inversion and carrier confinement in the central undoped active region less efficient, which results in a large leakage current. Consequently, a large part of electron-hole recombination takes place in the left p-doped part due to lower mobility of holes than that of electrons. Since this unwanted recombination region does not overlap with the optical mode (c.f., 30% contour in Figure 2.8), it does not contribute effectively to the lasing mode. The high leakage current explains the higher threshold current and lower efficiency of the LU structure. In real LU-type device samples, some extent of intermixing of the QW layers in the doped regions will occur due to the dopant implantation and subsequent activation annealing. This QW intermixing may reduce leakage current and undesirable recombination outside the active region.

For the VCP, as seen in Figure 2.8(c), a hole leakage current component escapes the central region of the mode (c.f., 30% contour). However, this amount is considerably smaller than in the LU and besides the VCP still exhibits a better efficiency than the LU, as shown in Figure 2.7. This can be explained by a better overall injection efficiency of the carriers into the VCP cavity, as holes are supplied by the p-doped pillar and they mostly re-

combine with electrons near the central post and do not diffuse too far from there. The InP post of the VCP promotes a better carrier confinement and a higher rate of electron-hole recombination near the central post, where the optical mode is excited.

2.3.5 On-chip energy consumption

What is the requirement of energy per bit in a photonic network on a chip? Miller [5] gave a prediction of maximum energy consumption for on-chip interconnect of 10 fJ/bit. This number has since then been used as a guideline in order to reach competitive optical interconnects. The fact of still relying on electrical interconnects is due to immature and yet uncompetitive photonic components to be used for interconnects. Several articles [5, 7] report that more than half of the total power is consumed by electrical wiring; and that is why new solutions are needed in order to solve environmental challenges [89] and the increased demand for data communication [1]. The largest amount of energy is dissipated by interconnects among the core operations (logic switching, memory, interconnect), since most of it is associated with charging and discharging the capacitance of signal lines [3]. However, even though the scaling of transistors has been persisting until today, the miniaturization for capacitances does not follow the same trend and therefore electrical interconnects are the future bottleneck for on/off chip communication. The energy prediction in [7] states a consumption of hundreds of fJ/bit for optical devices in the next five years, which is still a higher target compared to the desired condition of 10 fJ/bit.

An optical interconnect system is constituted by a transmitter driver circuit, an optical emitter (possibly a laser), and a detection site (photodetector and receiver). Therefore, when taking the total 10 fJ/bit of energy budget, we have to consider that this is the target for the whole optical wiring and it has to be divided into the different blocks. The focus of this thesis is nanolasers, i.e. the emitter in an optical interconnect and therefore the energy consumption that can be taken into account is of units of fJ or hundreds of aJ. We have chosen to focus on nanolasers and not on nano light-emitting diodes (LEDs), due to concerns about a too small output power because of the small modal volume needed for nano-LEDs to allow high-speed modulation [25]. The active material volume, being smaller than the modal volume, limits the output power.

2.3.6 Photon conversion

In this section we examine the energy consumption calculated as number (#) of photons, which is the physical quantity that travels along the optical interconnect.

Following the discussion in [86] and from Notomi at al. [16], optical processing is limited by the energy of a single photon, which is ~0.13 aJ at $\lambda = 1550$ nm. Classical communication does suffer from noise, due to the approximation of light as a Poissonian source: in this case a reasonable number of photons is required in order for the communication to take place. Taking this hypothesis into account and in the quantum limit, i.e. assuming a detection limit of one photon, for a bit error rate (BER) of 10^{-9} at least 21 photons are required for the transmission of "1" bit, corresponding to ~2.7 aJ. On the other hand for a BER of 10^{-12} 27 photons are required, corresponding to ~3.5 aJ (value equal to a power of 17.5 nW at a frequency of 10 Gbit/s). These are the ultimate limits in a classical approach. Thus, even in this theoretical case the very small output power from a recently demonstrated high-speed nano-LED, which was less than 1 nW, corresponding to an energy of a fraction of a photon [67], cannot guarantee high-speed error-free light detection required in on-chip optical interconnects. PhC nanocavities are good examples of low energy consumption devices. A nanolaser was recently reported by Takeda et al. [69], with a very low operating energy of 4.4 fJ/bit at a frequency of 10 GHz, which is at present one of the best emitters.

On the receiver side, current detectors are far from the quantum limit, but theoretical considerations of receiverless designs point towards energies about three times the quantum limit, if parasitic capacitances can be made negligible [90]. The results of the low-energy plasmonic photodetector model reported in [90] estimate an energy per bit between 10 aJ and 100 aJ with a parasitic capacitance in the range from 20 aF to 100 aF. For the full use of these low-energy plasmonic photodetectors, the input capacitance of the front-end amplifiers has to be drastically lowered, since the best performing front-end amplifier still has a high input capacitance of 30 fF [91]. Although further technology development and optimization of the laser sources and receivers are needed to reach the predicted energy requirements, any other transmission and routing losses will do nothing but significantly increase the requirements to the sources.

2.4 BH calculations

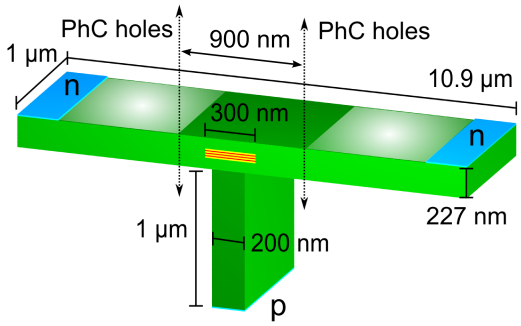


Figure 2.9: 3D geometry of VCP-BH model. The color legend is: green for InP, red for QWs, yellow for barriers, and light-blue for the metal contacts. On the devices p and n indicate the type and localization of the contacts.

In the analysis conducted in section 2.3, the strength of the BH and the potential of the vertical electrical injection have been highlighted. Thus we believe that the combination of a BH in a vertical injection design is expected to decrease the threshold current and further increase the performances of the nanolaser. In this section we discuss the model made with VCI and a BH, hereafter designated by VCP-BH.

In Figure 2.9 the geometry of this new model is presented. In the design the width of the BH is chosen to be 300 nm like the previous LBH model. In this section we want to investigate the correlation between pillar width and BH width and therefore two cases are analyzed, given that the pillar width is fixed to 200 nm. The first case belongs to width of the BH larger than the pillar, i.e. 300 nm, 400 nm, and 500 nm. In the second case the BH width is the same or thinner than the pillar, i.e. 200 nm and 100 nm. The doping concentrations are the same as VCP: the p-doping in the post is $1.5 \times 10^{18}\,\mathrm{cm}^{-3}$ and n-doping of $2.7 \times 10^{19}\,\mathrm{cm}^{-3}$ lies in the top 60 nm InP membrane. The other simulation parameters such as cavity length, mode confinement and the mirror reflectivity are the same as for the above discussed designs of section 2.3.

Figure 2.10 shows the curves of current as function of voltage and power as function of current for the three VCP-BH models. Figure 2.10 clearly displays that the different BH widths larger than the pillar show very similar L-I-V characteristics. In particular the voltage threshold is ~1 V for all the three models (300 nm, 400 nm, and 500 nm BH width), as can be seen

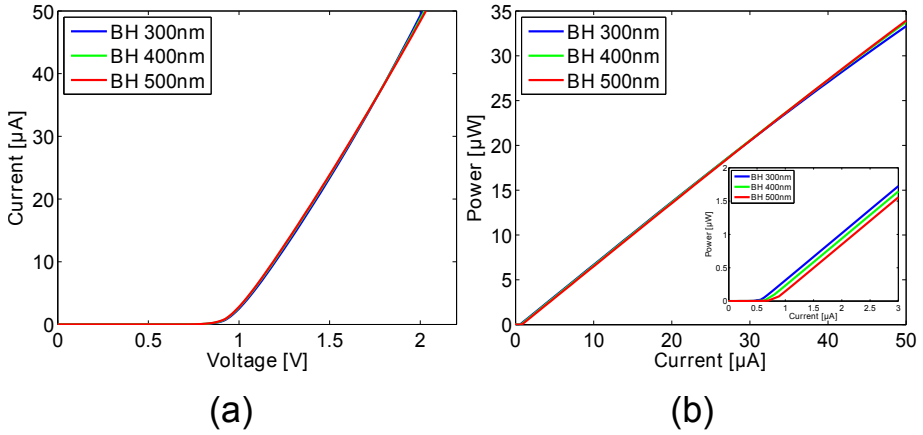


Figure 2.10: Current, voltage and power plot of VCP-BH. In (a) the I-V characteristic. In (b) the L-I characteristic, and as inset the L-I-V curve up to 3 µA to better distinguish the different thresholds for the diverse BH widths. The color legend gives the BH width: 300 nm blue, 400 nm green, and 500 nm red.

in Figure 2.10(a) and electrical resistances of 19.4 kΩ, 19.9 kΩ, and 20.4 kΩ respectively can be calculated. In Figure 2.10(b) the power performances are represented and, as for the voltage case, the three curves almost overlap with each other. From the inset in Figure 2.10(b) (magnification of the L-I-V curve in the current threshold region up to 3 µA) it can be seen that very small changes of current threshold occur. All the current thresholds

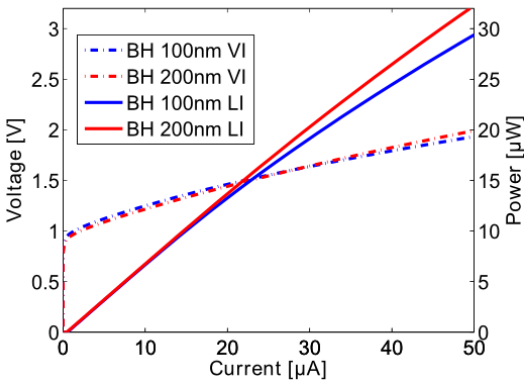


Figure 2.11: Current, voltage and power plot of VCP-BH for a BH width of 100 nm (blue) and 200 nm (red). The V-I curve is a dash-dot line, while the L-I curve is a continuous line.

are less than 1 µA and they increase with the BH width: the 300 nm BH has 0.56 µA, the 400 nm 0.67 µA, and the 500 nm 0.79 µA.

In Figure 2.11 the simulated L-I-V plot for the VCP-BH is represented, where the BH width is comparable to the pillar width. In the extreme case of the thinnest BH, the slightly higher voltage and current thresholds are at the expenses of a smaller electrical resistance, i.e. 1.13 V, 0.54 µA, and 14.9 kΩ, which can be seen as a sign of current leakage. This trend is reversed as soon as the BH width is at least as wide as the pillar: 1.06 V, 0.47 µA, and 18 kΩ.

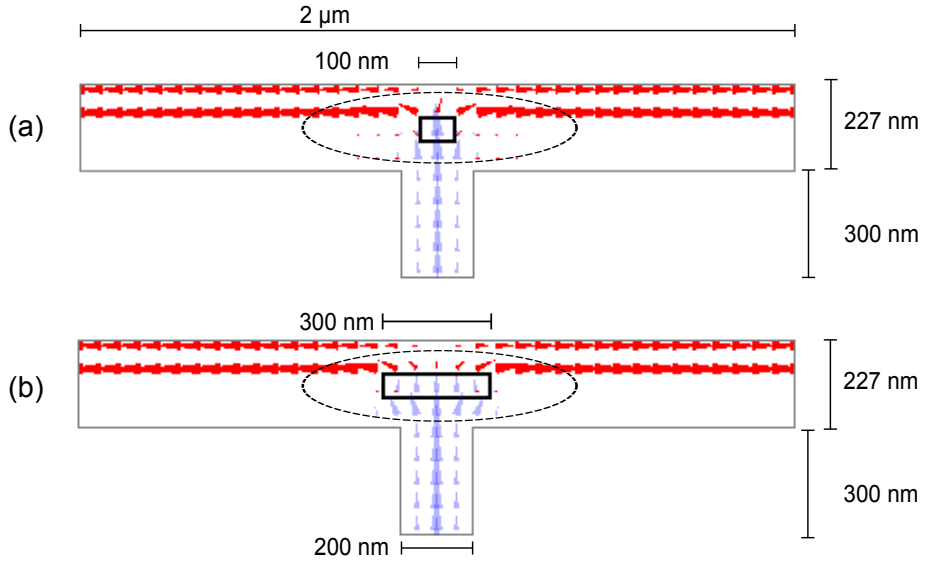


Figure 2.12: Vector plots of electrons (red cones) and holes (blue cones) currents at 5 µA injection current to evaluate contributions for recombination and leakage for VCP-BH structures with BH widths of 100 nm in (a) and 200 nm in (b). In each sketch the 30%-intensity contour of the optical mode has been drawn as a circle and the BH is designated by a rectangle with a black line. Only the central part of each structure is shown to visualize the important transition region. Only qualitative information can be drawn from this plot.

In the following all the power-voltage trends are further discussed referring to the leakage current plots in Figure 2.12 and the energy performances represented in Figure 2.13. For the sake of simplicity we decided to plot the two most representative models, which better explain the trend of BH thinner and wider than the pillar width, i.e. widths of 100 nm and 300 nm respectively.

Even though the vector plots in Figure 2.12 only give a qualitative

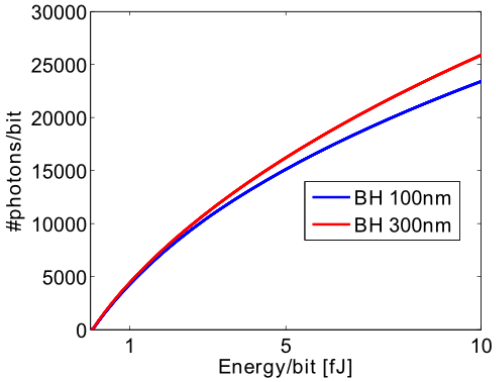


Figure 2.13: Number of output photons per "1" bit as a function of input energy per "1" bit for VCP-BH with 100 nm (blue) and 300 nm (red) BH widths. A bit period of 100 ps is assumed.

trend, and relying on the resistance and efficiency values, we can see that the VCP-BH model with a 100 nm BH suffers from more leakage issues than the 300 nm one. In this case carriers may prefer not to recombine in the tiny BH, but run through the device giving a lower electrical resistance and a lower WPE of about 10%, compared to the BH in 300 nm size. However Figure 2.12 shows a good recombination trend, since a gradual transition between hole current (blue cones) running through the post towards the BH and electron current (red cones) is displayed. Regarding the actual size of the active material, other circumstances also have to be addressed. In fact simply taking into account the fabrication process, larger margins for regrowth can be desirable. Concerning the performances, the aim of the device has to be decided in advance. Less material gain (small number of QWs or small BH) lead to low threshold devices at the expenses of the speed. A compromise is usually made between how low the threshold can be and how fast the laser has to perform.

Recalling what was given as a new metric for performances in section 2.3.3 and comparing Figure 2.7 and Figure 2.13 an energy comparison among the simulated models can be made. Already at 1 fJ/bit in the VCP-BH case, about 1000 more photons are generated than for the LBH (i.e. VCP-BH model 300 nm: 4660 photons, VCP-BH model 100 nm: 4100 photons, and LBH: 3300 photons), which was the best performing device for low injection levels. This fact can be related to both the very low current threshold that VCP-BH can achieve, but also to the vertical injection

that gives a lower electrical resistance. For high injection levels the VCP model was shown to be better performing than LBH and the VCP-BH results in the best performing device. The difference in number of generated photons further increases for higher injection levels, where the VCP was performing better: at 5 fJ/bit energy LBH generates 12200 photons, VCP 12900 photons, and VCP-BH 300 nm model 16000 photons. A summary for the number of generated photons and energy consumption is given in Table 2.2 for the four models. Even though the VCP-BH shows very good performances, the distributed n-doping on the top membrane layer, like VCP, can suffer in real processes from high optical losses, fact that has to be considered during design development and fabrication. Furthermore the presence of the pillar for vertical injection that perturbs the 2D PhC slab lowers the Q factor of the device, compared to lateral injection schemes with a pure membrane design.

We believe that the VCP-BH with the mentioned geometry and properties is the best performing device for two reasons: first it guarantees the best optical confinement, since the optical mode entirely overlaps with the active region (same principle as LBH); second the central post gives a more powerful carrier injection path, so that electron-hole recombination can more easily occur in the middle of the device, where the active material is confined. Additionally it provides an extra thermal escape path as will be elaborated below in section 2.5.

Table 2.2: Number of output photons per "1" bit as a function of input energy, for the models LBH, LU, VCP, and VCP-BH with 300 nm width.

Model	Energy [fJ/bit]	# of photons
LBH	1	3300
	5	12200
LU	1	200
	5	4900
VCP	1	800
	5	12900
VCP-BH	1	4660
	5	16000

2.5 Thermal simulations

Heat generation is a parameter that cannot be neglected for a working device. Semiconductor lasers are quite sensitive to heating and their design has to be carefully carried out, since the device performances can be drastically influenced by heat. In the worst case, if the generated heat cannot be overcome, no-lasing is observed. There is no way of avoiding heat generation, but the solution consists in minimizing it and looking at how the heat can be efficiently removed. Not only the thermal conductivities of the materials are important, but also the geometry that can better facilitate the heat removal through the device. This section is dedicated to thermal simulations of the four presented models: LBH, LU, VCP, VCP-BH. The geometry and set-up parameters for the electrical and optical solver are the same as listed in section 2.3, 2.4 and further in Appendix A. In the following the parameters for the thermal solver are listed and discussed.

- The simulations are carried out with the boundary conditions temperatures of 300 K, 350 K, and 400 K, in order to understand different operative conditions of the devices. We want to emulate a plausible temperature rise due to heating of other components and circuitry, in the case the laser was integrated in a platform with other devices. These conditions are translated as set-up temperatures at the metal contacts.

- The model includes a self-heating part, where the heat-flow takes the joule, optical, recombination and radiative heating contributions into account.

- The thermal boundary conditions are defined in accordance with the diverse material thermal conductivities: InP $68\,\mathrm{Wm^{-1}K^{-1}}$, InGaAsP $5.2\,\mathrm{Wm^{-1}K^{-1}}$ [92], and the contacts are assumed to be Au with $318\,\mathrm{Wm^{-1}K^{-1}}$ [93].

- The thermal conductivity of the PhC region has been scaled with the filling factor (25%).

2.5.1 Heat components

In a semiconductor laser the first sign of heat generation can be observed as the saturation of the output power for high injection current levels, when

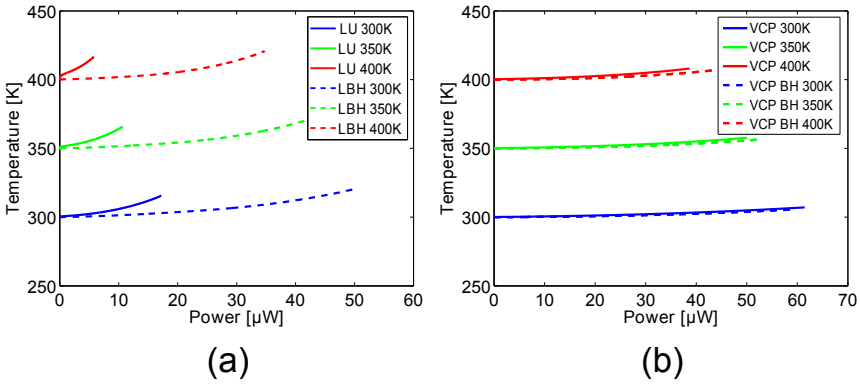


Figure 2.14: Temperature as a function of output power for LU (solid lines) and LBH (dash lines) in (a), and VCP (solid lines) and VCP-BH (dash lines) in (b) for the same injection current interval up to 100 µA. The initial temperature follow the same color legend: 300 K blue, 350 K green, and 400 K red.

the self-heating becomes a dominant heat component. However when investigating heat sources and heat flow in a device a lot of different mechanisms have to be considered. We want to derive a trend among our four models concerning thermal properties, looking at both the performances and at the different heat mechanisms. Figure 2.14 represents the temperature change as a function of output power for the four models. In Figure 2.14(a) we can see a remarkable difference in the output power between the LU and LBH devices of around a factor of three. The results for LBH show a slightly higher temperature increase due to the higher voltage. At the three starting temperatures (300 K, 350 K, 400 K) the output power decreases with temperature as expected. In Figure 2.14(b) we notice that VCP-BH is more stable at higher temperatures, since its output power increases more than VCP, as temperature increases.

The investigation of the total heat leads to four major contributions: Joule, recombination, radiative, and optical heat. Joule heating arises from the doped areas of the junction as an equivalent of an electrical resistance. Recombination heat accounts for the total energy converted in the p-i-n junction, part of this is the radiative heat, that takes into account the energy of the photons. Radiative heat is the heat that photons remove from the cavity when they escape from it. Optical heat is the heat created by photons that are re-absorbed for example by free carriers and can generate phonons. All these contributions are represented in Figure 2.15. The most interesting result obtained from Figure 2.15 is that for all the models

at low injection levels the different heat parts do compete with each other having similar values, while at high injection levels the Joule contribution is dominant and can be considered to be the total heat. Depending on the injection level, which gives diverse heat contributions, needed to operate the laser, a suitable thermal design is necessary to optimize the device performances. A good current operation point should satisfy a low heat generation and low power consumption, but a high output power.

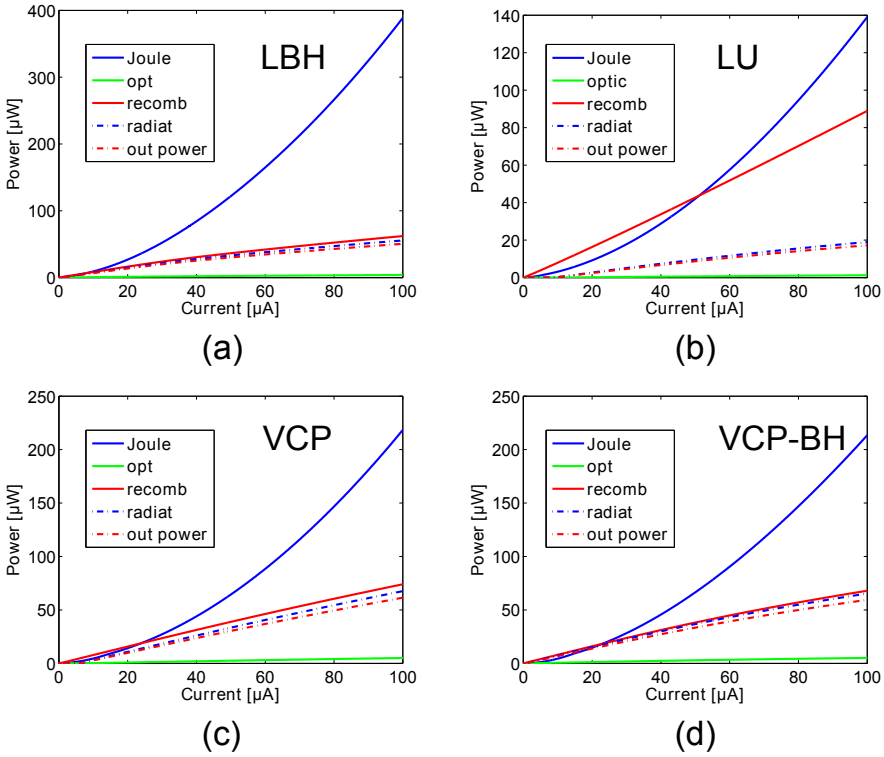


Figure 2.15: Heat components as a function of injection current for the designed models: (a) LBH (b) LU (c) VCP (d) VCP-BH. In the four graphs the diverse heat-parts follow the same legend: Joule heat solid blue line, optical heat solid green line, recombination heat solid red line, radiative heat dash-dot blue line, and output power dash-dot red line.

2.5.2 Dissipated power

The dissipated power (P_{diss}) can be written on the first order approximation as:

$$P_{diss} = P_{in} - P_{out} = V_{in} \times I_{in} - P_{out} \tag{2.2}$$

where P_{in} is the input power calculated from the product of driving current I_{in} and voltage V_{in} and P_{out} is the output power. Figure 2.16 shows P_{diss} as defined in equation 2.2, where temperature is plotted as a function of the dissipated power.

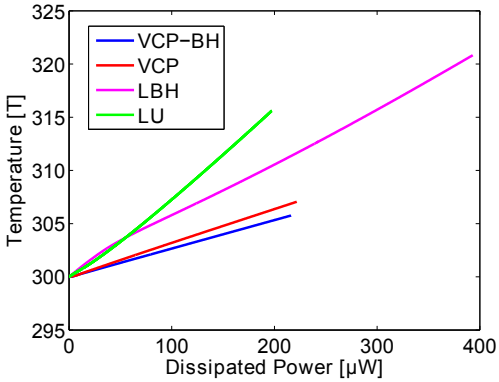


Figure 2.16: Temperature as a function of dissipated power for a starting temperature $T = 300\,\mathrm{K}$ for VCP-BH (blue), VCP (red), LBH (magenta), LU (green) for the same injection current interval up to 100 µA.

In Figure 2.16 we are interested in the slope of the represented curves that can be regarded as the device thermal resistance. The evaluation of the slope gives the following thermal resistances: LU 83 K/mW, LBH 46 K/mW, VCP 32 K/mW, and VCP-BH 27 K/mW. Avoiding been redundant, we only report the data concerning the simulation at 300 K, since similar trends were seen at higher temperatures, but with a general increase in the thermal resistance for all the devices. The thermal resistance trend confirms that LU model has the worst thermal performance, because a lot of power is dissipated across the structure (low output power compared to input power). This issue could also be due to the presence of extended active quaternary material, which has an intrinsic thermal conductivity approximately one order of magnitude smaller than InP. The VCP and VCP-BH have a lower thermal resistance than LBH, in other words a smaller dissipated power, which could be due to the injection scheme. The pillar can

also work as heat sink in the device, since it offers an extra path for heat flow, as discussed in [65]. In a pure membrane design like LU and LBH models, the heat can only escape through the membrane, while in a vertical electrical injection design the heat is removed faster, because it can escape from both the membrane and the post. The smaller thermal resistance of VCP-BH than VCP can be related to the extension of the active region: a BH involves a total thermal conductivity that is higher than extended QWs, due to the material properties.

2.6 Summary

In this chapter the analyses of the optical and electrical design are conducted. The optical simulations define the parameters of the PhC pattern according to the double hetero-photonic crystal approach with the extra pillar structure under the membrane for vertical electrical injection.

The results obtained by the electrical simulations of the four modeled devices show that on one hand the localization of the active material as BH decreases the laser thresholds and it gives a confined path for the electron-hole recombination in the cavity with negligible leakage current issues. On the other hand the pillar for the vertical electrical pumping is a powerful mean for effective carrier injection into the laser cavity and energy efficient because of its low power consumption. A good carrier confinement is promoted by the pillar, since it supplies holes and electron-hole recombination takes place in the laser cavity near the central post. In the vertical injection scheme leakage current issues are less evident, because holes are directly supplied from the pillar into the laser cavity and the high electron-holes recombination rate decreases the likelihood of carrier diffusion far from the cavity. According to our results the combination that best fits the aim of a low-threshold energy efficient laser consists of both the presence of a device with a BH in a vertical injection scheme.

The thermal simulations confirm that the vertical injection devices can dissipate the heat in a more efficient way than the laterally injected devices, since the pillar provides an extra path for the heat removal besides the membrane.

We believe that the VCP-BH model gives the best performances for a nanolaser device, however all the models can be further optimized according to geometry, design, and doping levels, in order to achieve specific scopes according to the technology expertise and advanced fabrication processes.

Chapter 3

Fabrication Process Development

The fabrication process developed within this Ph.D. project to achieve electrically pumped photonic crystal devices is described in this chapter. The fabrication has been entirely done at DTU Danchip cleanroom facility, besides a single step that was outsourced at NanoLab in Lund for the lack of the machine in the cleanroom facility at DTU. Before the detailed description of the more critical process steps, a schematic overview is given.

3.1 Process introduction

The fabrication of the nanolaser devices includes a relatively long and non-trivial design and cleanroom processing: a vertical injection scheme with a post structure under the Photonic Crystal (PhC) membrane, a hetero-photonic crystal cavity, and double-side processing through adhesive wafer bonding. After introducing the epitaxial layout, a schematic process overview for the device fabrication is outlined. A detailed description of each fabrication process step can be found in Appendix B.

3.2 Epitaxial layout

Table 3.1: Epitaxial layers of 2 PQ QWs wafer. The layers highlighted in bold describe the epitaxy of the final device.

Material	Thickness $[nm]$	Doping type & specie	Doping concentration $[cm^{-3}]$	Comment
InP	20			cap layer
InGaAs	5			protection mask layer
InP	50			ions protection
InGaAs	175	p (Zn)	1.0×10^{19}	contact layer
InGaAsP	100	p (Zn)	5.0×10^{18}	contact layer PQ(1.22)
InP	25	p (Zn)	$2.0 \times 10^{18}-$	post
		p (Zn)	5.0×10^{18}	graded doping
InP	575	p (Zn)	2.0×10^{18}	post
InP	125	p (Zn)	$1.5 \times 10^{18}-$	post
		p (Zn)	2.0×10^{18}	graded doping
InP	225	p (Zn)	7.0×10^{17}	post
InP	50			post - diffusion
InGaAsP	10			etch stop layer PQ(1.15)
InP	90			membrane
InGaAsP	4			QB
InGaAsP	4			QW PL(1550 nm)
InGaAsP	8			QB
InGaAsP	4			QW PL(1550 nm)
InGaAsP	4			QB
InP	40			membrane
InP	30	n (Si)	1.0×10^{18}	membrane
InP	26	n (Si)	1.0×10^{19}	membrane
InGaAs	250			etch stop layer
InP	200			buffer layer
InP wafer				substrate

All the processed wafers have been epitaxially grown in a metal-organic vapor-phase epitaxy (MOVPE) system on InP substrates at DTU Danchip cleanroom facility.[4] In Table 3.1 the epitaxial structure with two QWs is outlined. Besides the structure presented in Table 3.1, samples with 3 layers of InAs QDs, and single QW have also been processed. For the

[4]The growth has been performed by Elizaveta Semenova and Kresten Yvind, DTU Fotonik.

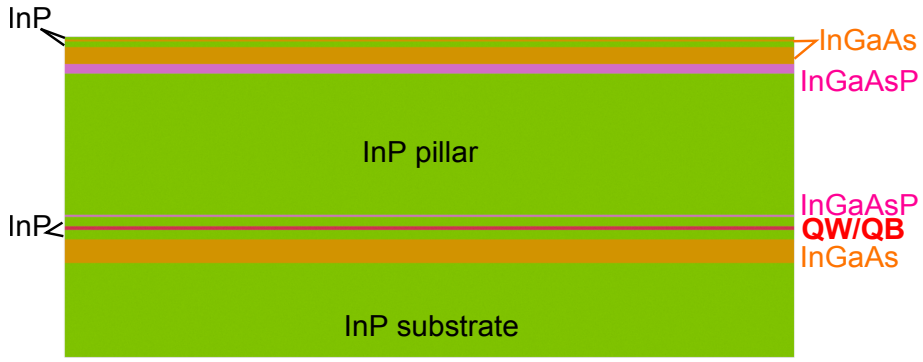


Figure 3.1: Schematic of the III-V layer epitaxy. All the layers are on scale apart from the bottom InP substrate. Color legend: InP green, InGaAs orange, InGaAsP magenta, active region with QW/QB red.

QWs growth the strain-compensation method has been used. Although a comparison among devices with different active materials would have been interesting, the best results have been obtained with the described epitaxy of two QWs. The sketch of the layer epitaxy is also presented in Figure 3.1 with the material color legend. The layers highlighted in bold in Table 3.1 belong to the final device and their band diagram configuration is sketched in Figure 3.2. All the other layers are sacrificial layers that are removed during the fabrication process.
The layer layout has been designed according to the following principles:

- The top 5 nm InGaAs and 50 nm InP layers - apart from the thin InP cap layer that is grown for protection purposes and is etched as first step of the processing - have an important role during the planarization of the sample and will be later discussed in section 3.6. These two layers are a novelty of this process, since they are not usually found for standard ridge laser fabrication.

- The p-doped side consists of InGaAs and InGaAsP highly doped contact layers and 1 µm gradually doped InP layer, which form the whole post for current injection. The doping levels were chosen according to the standard ridge laser processing developed in our group and scaled to the sizes needed for the devices presented in this thesis. The contact layers are highly doped in order to improve the junction to the metal.

- The membrane that hosts the PhC pattern includes the layers that

follow the post starting from the 10 nm InGaAsP etch stop layer and ending before the second 250 nm InGaAs etch stop layer. Most of the membrane is InP, that is undoped below the QWs and it is partially n-doped on the top of the active material. From characterization of unsuccessful devices, the InP n-doped layer, which was at first at the highest doping concentration that is possible to achieve during the MOVPE growth, was split into two thinner doped layers in order to reduce optical losses.

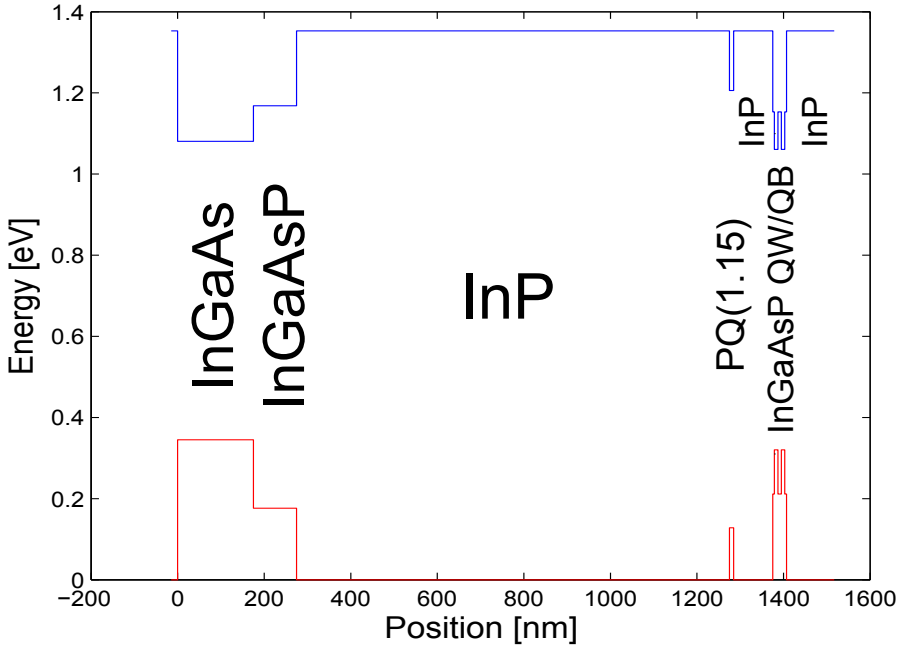


Figure 3.2: Sketch of the final device band diagram. The material evaluation is based on [94]. The red line represents the valence band and the blue line the conduction band. The x-axis reports the layer position in the epitaxy, on the left the position of the contact layers and on the right the position of the membrane.

3.3 General process description

From Figure 3.3 to Figure 3.12 a schematic overview of the process is illustrated and a brief description of the fabrication steps indicated with numbers is given. For the sake of understanding the layer representation in the schematics is on scale apart from the InP and Si substrate that are thinner. In Appendix B a detailed description of each fabrication step and the cleanroom recipes can be found. For the entire process any photolithographic steps are done with 365 nm UV lithography.
In Figure 3.3(0) the III-V wafer is depicted after the growth. After the InP cap layer removal with the wet etching solution $1\,HCl : 4\,H_3PO_4$, the wafer is spin covered with ~330 nm negative e-beam resist hydrogen silsesquioxane (HSQ) (Fox-15 from Dow Corning) for the pillar electron-beam lithography in Figure 3.3(1). In Figure 3.3(2) the pillar mask after resist development in the basic solution $3\,H_2O : 1$ AZ400K is shown.
In Figure 3.4 the pillar etching is illustrated. In Figure 3.4(3) the dry etching step in a reactive ion etching (RIE) tool using a cyclic $CH_4/H_2 - O_2$ chemistries is depicted. After the dry etching, the wet etching with $1\,HCl : 4\,H_3PO_4$ to reach the InGaAsP etch stop layer is presented in Figure 3.4(4).

Figure 3.5(5) shows the deposition of ~1.5 µm plasma enhanced chemical vapor deposition (PECVD) SiO_2 to entirely cover the pillar. The SiO_2 deposition follows the pillar profile. Afterwards ~3.8 µm thick polymer benzocyclobutene (BCB) is spun on the sample and cured in an oven for a planarization purpose. In Figure 3.5(6) the combined SiO_2-BCB dry etching with the RIE tool through CHF_3/O_2 gives a planarized sample, where all the BCB has been removed and the pillar contact layers and the top-thin protecting layers are revealed.
After a photolithography with negative resist (UV lithography 356 nm), the removal of the thin top 5nm-InGaAs and 50nm-InP, metal evaporation and lift-off to fabricate the p-contact are shown in Figure 3.6(7). In Figure 3.6(8) the III-V sample is flipped and bonded to silicon using as adhesive layer ~2 µm thick BCB. The bonding process is carried out in an EVG bonder, where BCB is cured for 1 hour at 250°C under a piston force of 750 N and with a chamber pressure of 1.6×10^{-3} mbar. After bonding, it is important to remove the BCB covering the sample edges before the substrate removal. This is done in a CF_4/O_2 plasma ashing step and it should prevent the formation of InP cliffs at the edge of the III-V sample during the following anisotropic wet etching. In Figure 3.6(9) the InP sub-

strate and the InGaAs sacrificial layer are selectively wet etched in HCl [95] and $H_2SO4 : H_2O_2$ [96] solutions, respectively, leaving a smooth InP membrane bonded to the Si carrier. At this stage the process schematic is divided into sections *(a)* and *(b)* to differentiate between the HSQ and ZEP (Zeon ZEP-520A) processing for the PhC pattern respectively.
In Figure 3.7(10a) the sample is spin coated with ~330 nm thick HSQ for the Photonic Crystal (PhC) electron-beam lithography. After the resist development in $3\,H_2O : 1$ AZ400K the PhC holes are made in HSQ that works well as hard mask as shown in Figure 3.7(11a). The pattern is therefore transferred to the semiconductor membrane in Figure 3.8(12a) through semiconductor dry etching (cyclic $CH_4/H_2 - O_2$ process in RIE). In Figure 3.8(13a) HSQ is removed with BHF and the sample is processed with a negative resist for the n-contact photolithography with following metal evaporation and lift-off. Figure 3.9 reports the membranized device in a perspective view (14a) and in cross-section (14a'). In this step the membrane is suspended in air, since the SiO_2 layer is wet etched through the PhC holes in a BHF solution with a wetting agent.
From Figure 3.10 to Figure 3.12 the processing with the positive e-beam resist ZEP is described. In Figure 3.10(10b) the deposition of the hard mask layers of ~20 nm plasma enhanced atomic layer deposition (PE-ALD) SiO_2, ~200 nm PECVD Si_3N_4 and ZEP spinning of ~500 nm are shown. Figure 3.10(11b) shows the sample after the PhC electron-beam lithography and resist development in ZED N50 , where the PhC pattern on ZEP is formed.
In Figure 3.11 the two PhC dry etching steps are represented. In Figure 3.11(12b) the pattern is transferred from ZEP to the hard mask layers in RIE with CHF_3/O_2 chemistry. After ZEP stripping in heated ultrasonic bath of microposit® remover 1165 the PhC holes scheme is transferred from the hard mask to the membrane through a semiconductor dry etching with a cyclic $CH_4/H_2 - O_2$ process in the RIE in Figure 3.11(13b).
The sample after photolithography for the n-metal (negative resist), metal evaporation and lift-off is shown in Figure 3.12(14b). In Figure 3.12(15b) the membranization step is depicted, where the PhC membrane is released through a BHF solution with wetting agent. This step is also necessary to remove the hard mask layers from the top of the PhC membrane.

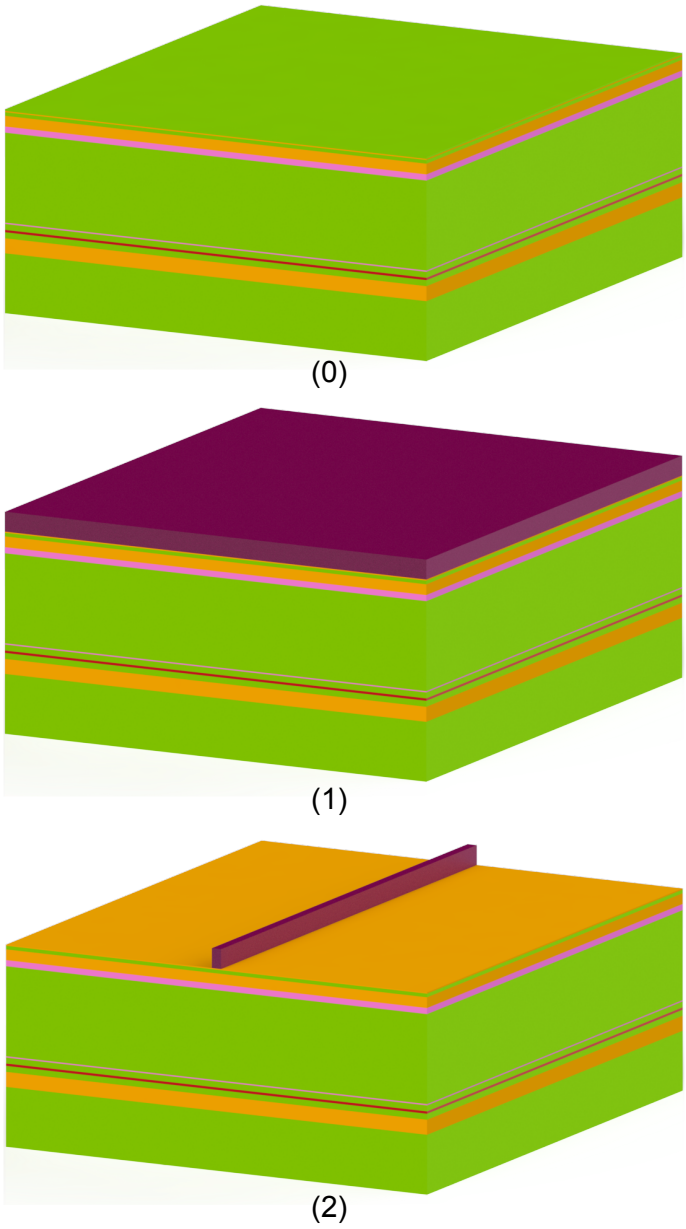


Figure 3.3: (0) III-V sample. (1) InP cap layer removal and HSQ (purple) spinning. (2) HSQ development. Color legend: green InP, orange InGaAs, magenta InGaAsP, red active region, and purple HSQ .

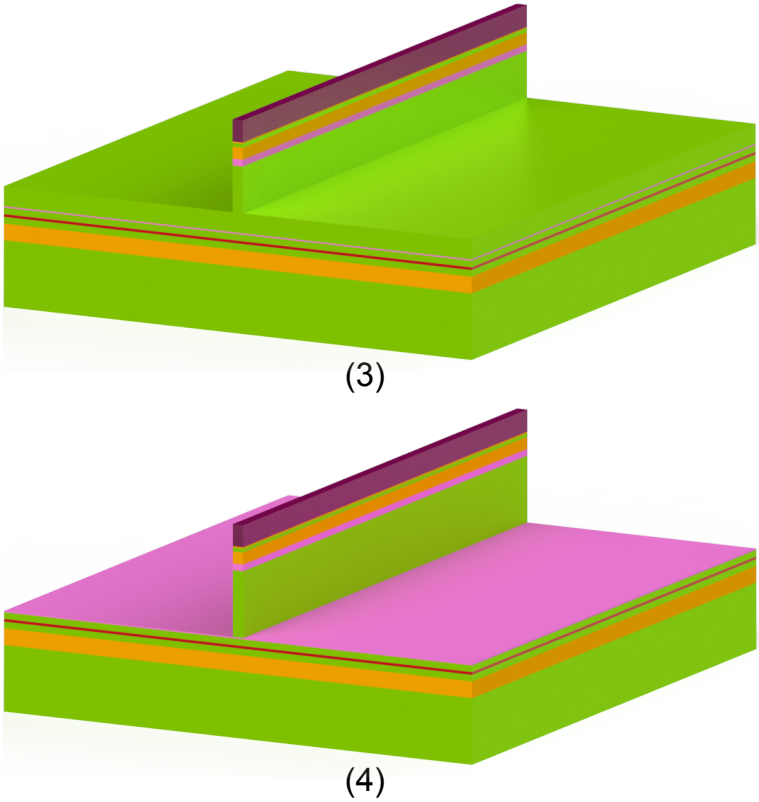


Figure 3.4: (3) Pillar dry etching in a RIE system. (4) Pillar wet etching until the InGaAsP etch stop layer.

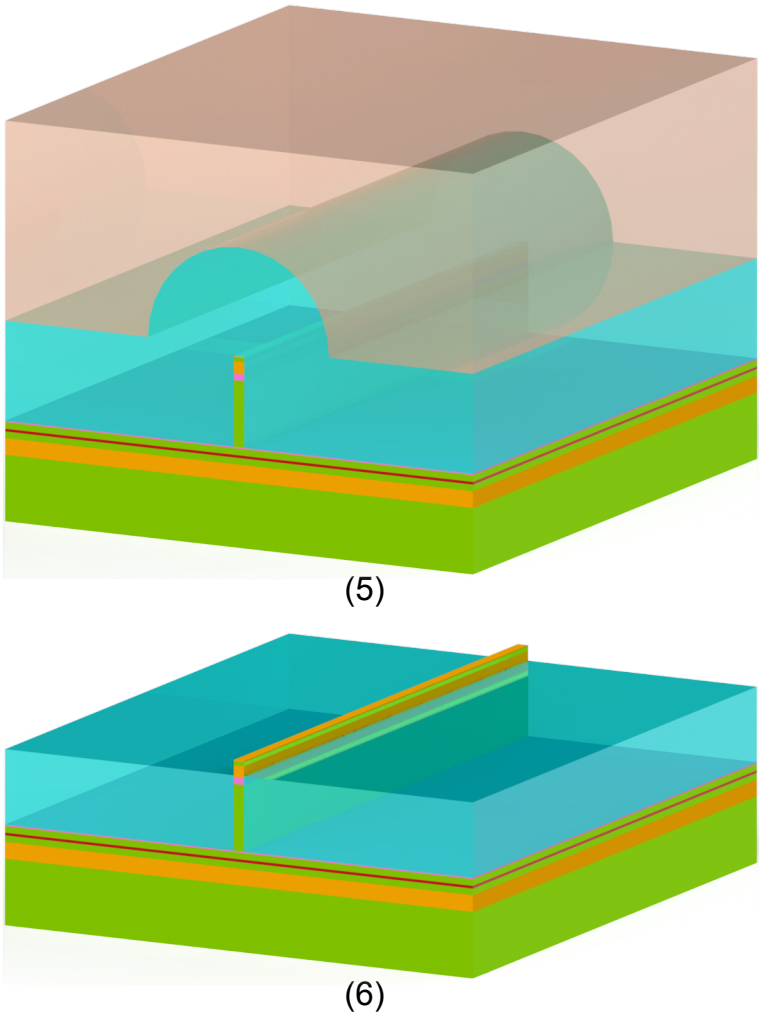


Figure 3.5: (5) SiO_2 (light blue) PECVD deposition and BCB (light red) spinning. (6) Mutual BCB and SiO_2 etchback in RIE.

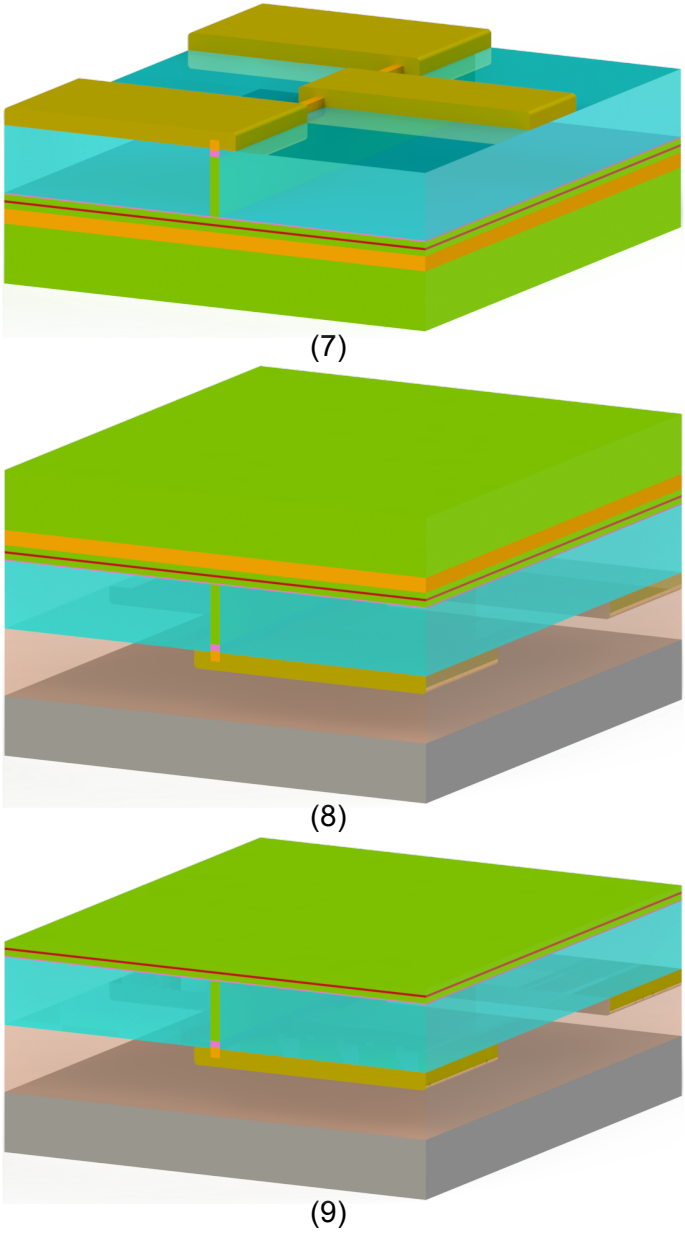


Figure 3.6: (7) Removal of 5nm-InGaAs and 50nm-InP protecting layers and p-metal (gold like color) lithography. (8) Wafer flip and adhesive BCB bonding to silicon substrate (grey). (9) InP substrate and InGaAs etch stop layer removal.

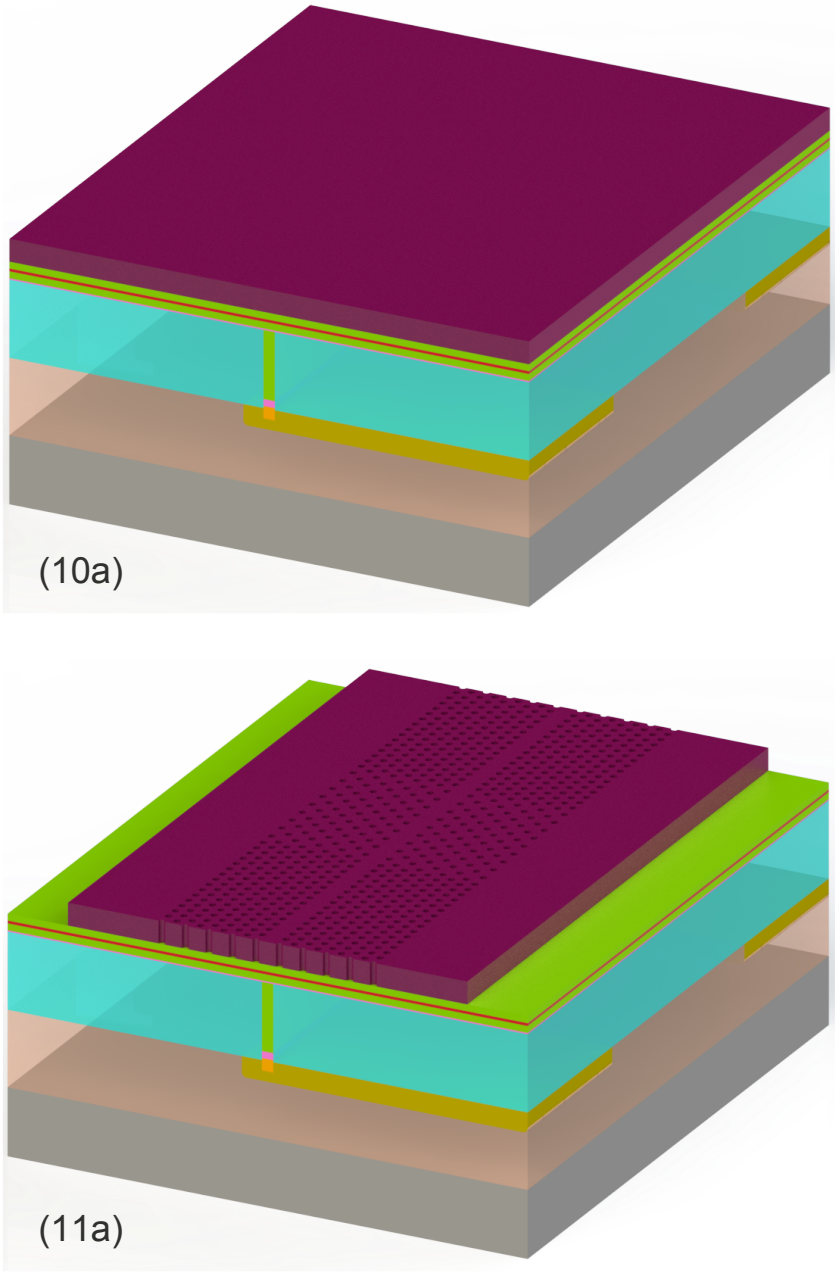


Figure 3.7: (10a) HSQ (purple) spinning for e-beam PhC lithography. (11a) HSQ development with the desired PhC pattern.

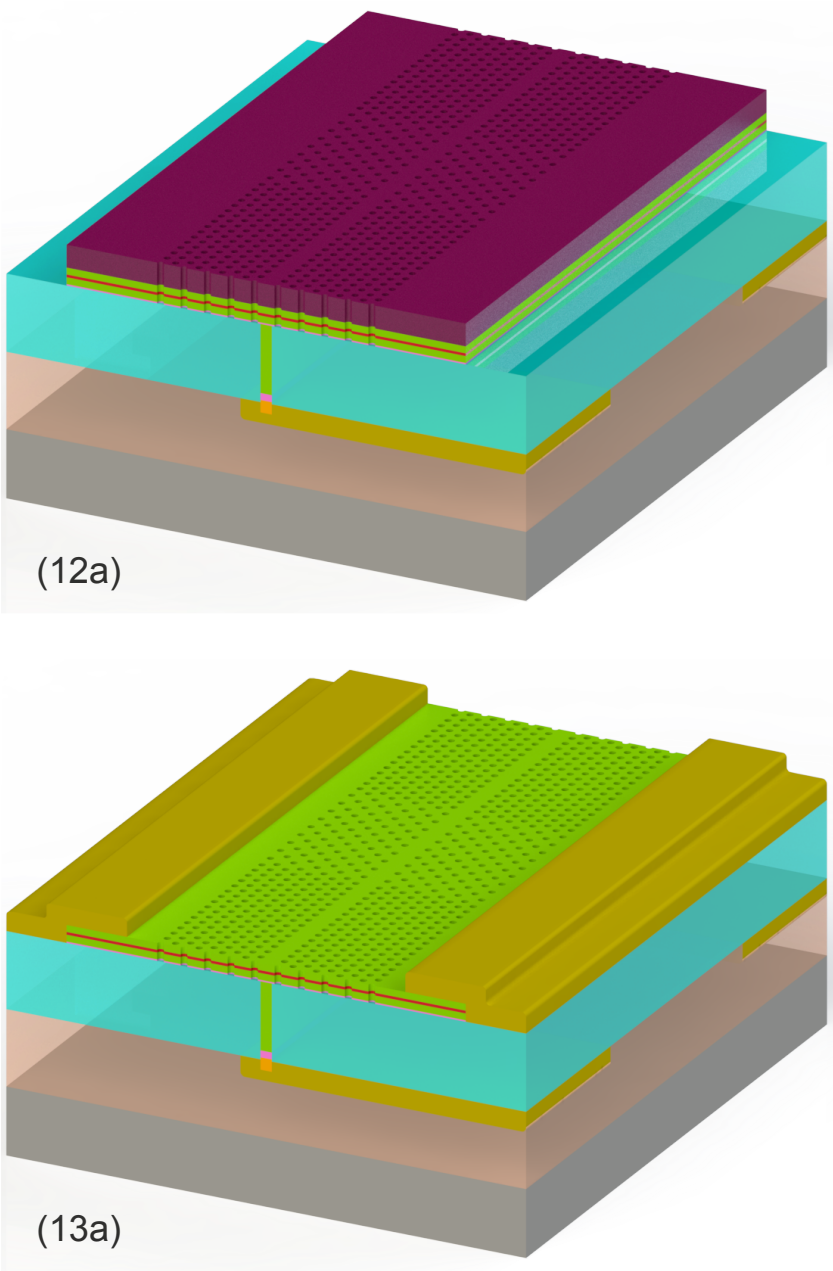


Figure 3.8: (12a) PhC dry etching from the HSQ mask to the membrane. (13a) HSQ removal and n-metal (gold like color) lithography .

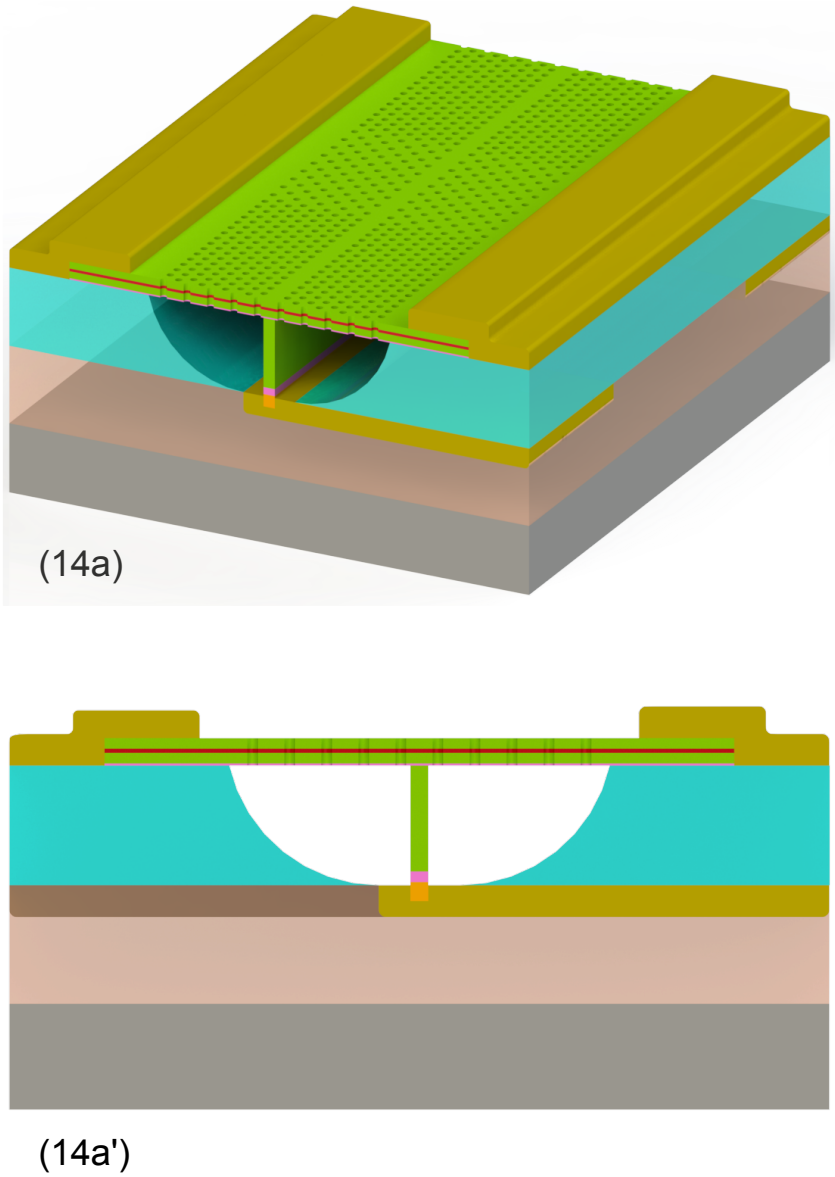
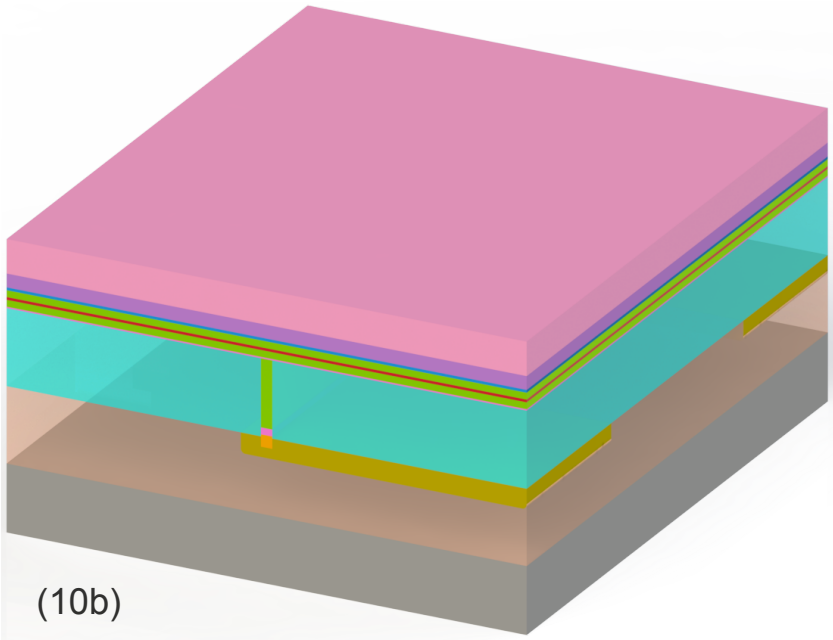


Figure 3.9: (14a) Device membranization in tilted-view and (14a') in cross-section view.



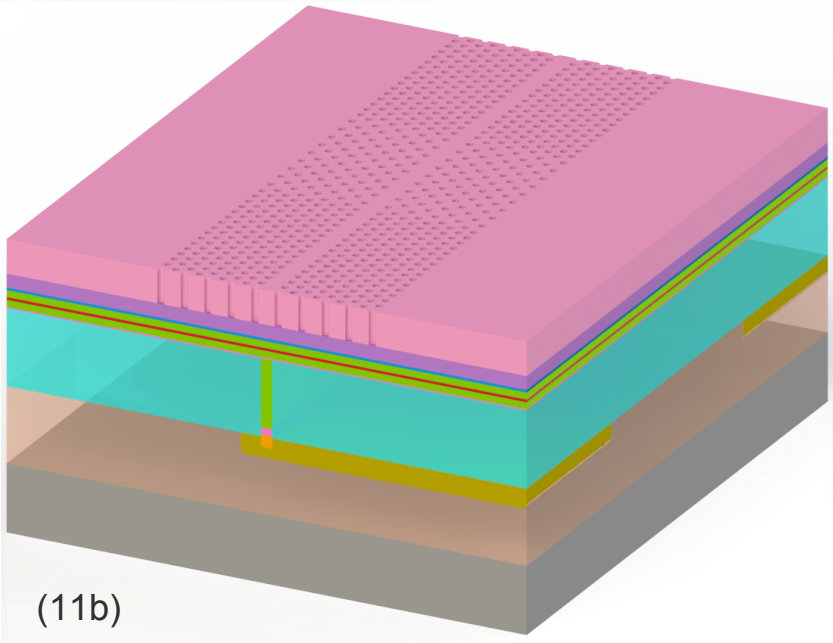


Figure 3.10: (10b) PE-ALD SiO_2 deposition (blue), Si_3N_4 PECVD deposition (violet) and ZEP spinning (pink). (11b) ZEP development after the PhC e-beam exposure with the desired PhC pattern.

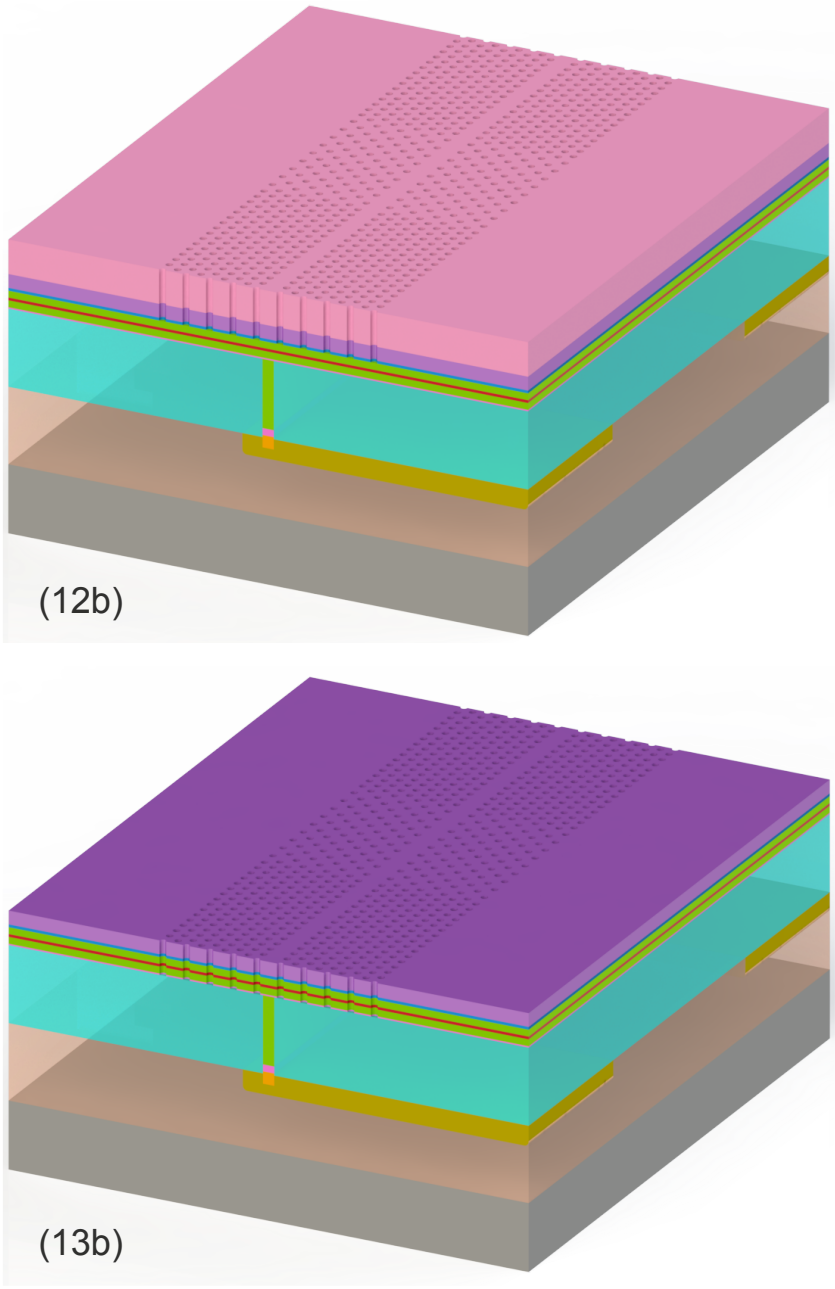


Figure 3.11: (12b) Dry etching from ZEP to the hard mask layers in RIE. (13b) ZEP removal and semiconductor dry etching in RIE.

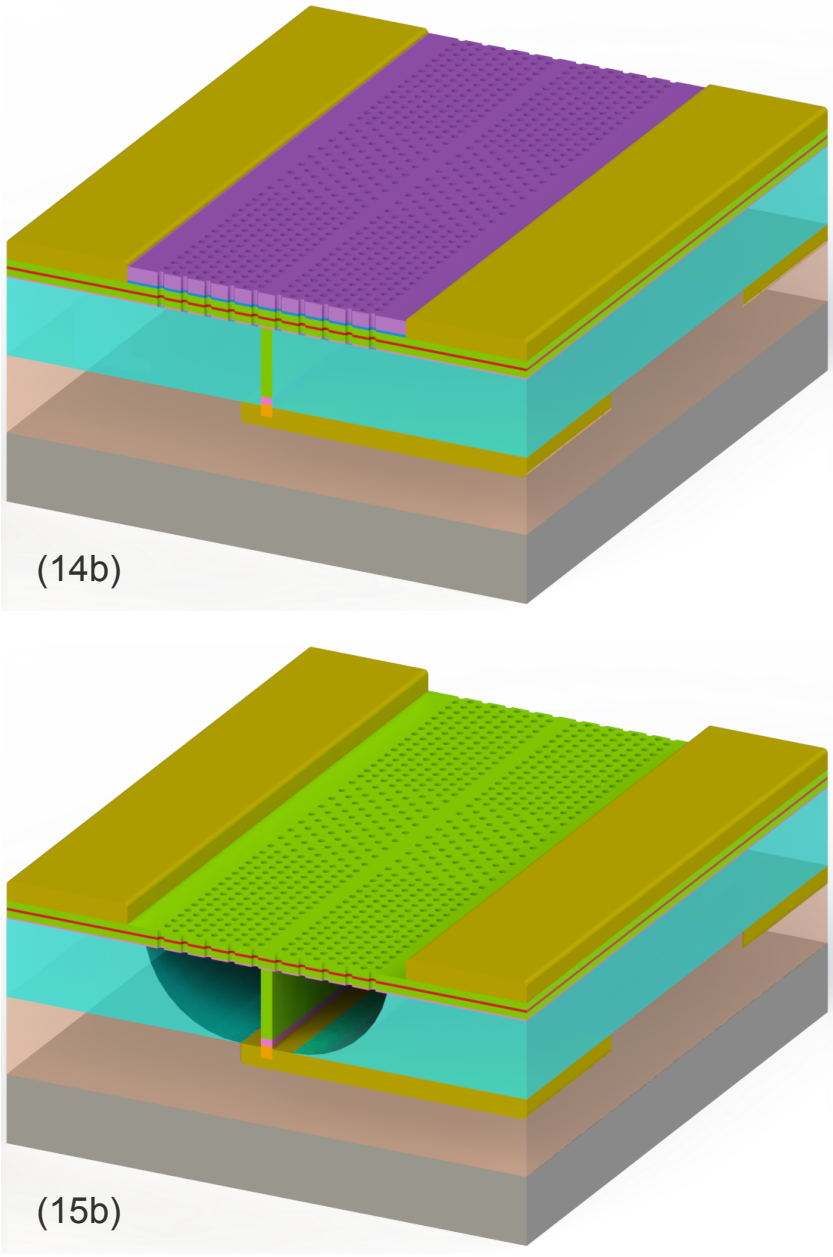


Figure 3.12: (14b) N-metal (gold like color) lithography. (15b) Device membranization.

3.4 Pillar e-beam lithography

The first step in the fabrication process is the definition of the pillar. Standard photolithography cannot be used due to the small pillar widths and therefore e-beam lithography is necessary. HSQ is the high-resolution negative-tone inorganic resist employed for electron-beam lithography for the pillar patterning. The resist is spin coated on the 2" InP wafer with spinning parameters chosen in order to reach a thickness of ~330 nm. The pattern is written using a JEOL JBX-9500FS electron beam writer at Danchip with an acceleration voltage of 100 kV. In the equipment the beam spot for the electron beam writing is generated by an emitter and a system of 4-stage magnetic lenses is needed to focus the beam on the sample. The pattern is written point by point with a writing field up to 1000 µm × 1000 µm. For the e-beam exposure a current of 6 nA and a dose of 3750 $\mu C/cm^2$ with proximity error correction (PEC) were found to be the best parameters after running a dose test. The PEC option was included in order to take into account the contributions given by the interaction of forward and backward scattered electrons with the resist and the substrate. In this case the dose is partially modulated on the single structures according to the dimensions and the distances respective to each other. For this e-beam exposure the main contribution of back-scattered electrons is given by the InP substrate. After the exposure the sample is developed in 3 H_2O : 1 AZ400K for 2.5 min.

HSQ is employed because of its high resolution down to 20 nm [97] and because of its radical change to glass-like layer after exposure due to the crosslinking process, however various issues about aging of the resist, contrast, sensitivity and development have been reported [98, 99] and had to be taken into account for repeatability reasons. For example even though the contrast of HSQ seems to be improved after several days from the exposure and its sensitivity reduced [97], due to the total length of the process and once proved that spinning, exposure and development steps gave the desired results, the same procedure has been followed for all the wafers. The sample was spin coated just before the e-beam exposure and it was developed straight after that. Another advantage of HSQ is its transformation in a SiO_x layer after the e-beam writing. This means that the crosslinked HSQ can be used as hard mask for the pattern transfer without having to introduce intermediate steps. Moreover when HSQ needs to be removed (adhesion issues, wrong e-beam exposure, removal of resist after pattern transfer), dipping the sample in BHF (or HF compounds) results in a fast

and easy procedure.

3.5 Dry and wet etching

3.5.1 Pillar etching

The total pillar height is more than 1 µm, which is a relatively deep layer to be etched. Different approaches have been investigated, but mainly two strategies can be applied: a quite long and deep dry etching in order to maintain reproducible and straight profiles and a short wet etching or a short dry etching and a long wet etching. We decided to end the total pillar etching with a wet step for two reasons: on one hand a too deep dry etching could compromise the quality of the active material, on the other hand the final wet etching gives smoother surfaces and homogeneity at the expenses of the crystallographic dependences. For the InP wet etching a thin InGaAsP etch-stop layer is employed. In the end we have decided to use a long dry etching for about 1 µm of total pillar height (including contact layers), in order to stop the dry step at a good distance from the membrane and avoid damages to the QWs. The pillar etching is concluded with a short InP wet step in $1\,HCl : 4\,H_3PO_4$. The importance of the top thin InGaAs and InP layers on the pillar side will be discussed in the planarization step in section 3.6. Although the pillar etching step has been optimized, the addition of the two top layers in the epitaxy increased the number of fabrication steps before the p-metal deposition.

3.5.1.1 Dry etching of InP

The RIE used for the fabrication process has a parallel plate system that creates a radio frequency (RF) field with a frequency of 13.56 MHz, which excites a plasma sheet in the center of the chamber. The bottom electrode is the lower part of the chamber, while the lid is the top electrode. Ions are accelerated perpendicular to the chamber surface and are bombarded onto the sample, which lies on a quartz plate on the bottom of the chamber. The ion bombardment during the etching depends on the chamber pressure and on the power from the RF-field as reported in [100]. To avoid the damage induced by the ion bombardment, the resist used as mask works as protection layer if it is not over-etched. The approach of metal organic reactive ion etching (MORIE) with CH_4/H_2 chemistry was employed during the etching. Although excellent anisotropy can be achieved with this chemistry, as shown since 1986 [101], a major issue consisting in the formation of

a resistant film according to the CH_4/H_2 ratio mixture appears. This film was at first reported to arise when the CH_4 concentration is 15% [101], and later demonstrated that the etching remains stable up to 25% concentration [102]. The complexity of this chemistry was further investigated until Carter et al. [103] reported that the film could be removed by O_2 plasma, therefore resulting in an organic polymer. If the polymer is not carefully removed during the semiconductor etching, it can destructively cause a distorted pattern transfer and in the worst case the stop of the semiconductor etching [102, 104]. For this reason the MORIE etch needs to be cyclic, where each cycle has a the first part consisting of a mixture of CH_4/H_2 that etches InP, and more slowly InGaAs and InGaAsP compounds, and a second step of O_2 plasma cleaning, that is needed to remove the generated polymer.

3.5.2 Wet etching: crystallographic planes dependence

Hydrochloric acid based etchants are used for preferential InP etching [105]. To complete the wet etching of the pillar the mixture $1\,HCl : 4\,H_3PO_4$ has been employed, while gently stirring the sample as successfully reported in [105, 106], when an etch stop layer is present in the epitaxy. The investigation of the ridge profiles conducted by Brenner in [106] with a similar acid mixture reports that during the wet etching different crystallographic planes are revealed with regard to the ridge orientation to the major flat, plane $< 011 >$. Therefore an accurate ridge orientation perpendicular to the major flat of the wafer is necessary for a reproducible profile, when wet etching is employed.
Moreover Brenner [106] found out that the relation between the sidewall angle α is proportional to the tilt angle ϑ to $< 011 >$ plane (direction perpendicular to the major flat of the wafer) with the following expression:

$$\alpha = 87.8° - 1.4 \times \vartheta \tag{3.1}$$

Even with a different hydrochloric and phosphoric acid mix, equation 3.1 was tested and proved to be valid in our case. The main difference is that in case of [106] the concentration of HCl compared to H_3PO_4 is higher compared to our choice of mixture, therefore the etch rate speed decreases from ~0.9 µm/min [106] to ~0.5 µm/min. Even though for standard ridge processing the ridge sidewalls have to be precisely controlled for optical mode confinement, in our process the pillar profile interferes with optical properties on a second-order level. In order for the PhC membrane to confine the optical mode, the pillar has to be thin, ~200 nm as shown

in [81, 82]. Therefore the orientation of the pillar has to be controlled in order to achieve the desired width, if wet etching is involved.

The angle α in equation 3.1 indicates that even if the pillar is exactly perpendicular to the major flat ($\vartheta = 0$), the sidewall profile will not be perpendicular to the substrate, but 2.2° tilted. For this reason a rigorous analysis was conducted in order to predict how the pillar profile looks like after the wet etching. At first the pillar mask needs to be placed as perpendicular as possible to the major flat, unfortunately the accuracy of this step relies on the manual placement of the wafer in the e-beam cassette for the exposure and to the effective wafer substrate properties. An example of pillar profile is shown in Figure 3.13. These pillars consist of the top InGaAs and InGaAsP contact layers and 1 µm InP, which is almost the same epitaxy as the one employed in the fabrication. Figure 3.13(a) and (b) show the typical pillar cross section: in Figure 3.13(a) the pillar has a bottom width of ~60 nm, while in Figure 3.13(b) ~200 nm. In particular in Figure 3.13(b) the angle dependencies of crystal planes and etching steps are drawn. The top drawn angle shows the contact layers and dry etch dependence and it is estimated of 83°. The bottom drawn angle gives the relationship between the wet etching and InP. This angle depends on the anisotropy of the selected wet etching solution with InP crystallographic planes and it is estimated of ~85°. Figure 3.13(c) shows a pillar that collapsed after the wet etching because of its thin width. This fact proves that there is a minimum pillar width for which pillars are kept vertical. The knowledge of the experimental angles during the etching processes was used for the a-posteriori calculation of the mask pillar width with the further introduction of the top InP protection layer and InGaAs mask layer as described in Table 3.1 and section 3.6. In the end the mask pillar widths are designed of 225 nm and 280 nm, which should result in the target widths of 170 nm and 210 nm respectively. Even keeping the process steps as reproducible and as repeatable as possible, small fabrication modifications can always occur and therefore a further way of monitoring the size of the pillars is employed. In the mask design we include test pillar structures with widths varying from 20 nm to 320 nm with a 20 nm step. According to how many pillars survive the wet etching, a rough on-time estimation of the pillar width can be derived for each wafer processing.

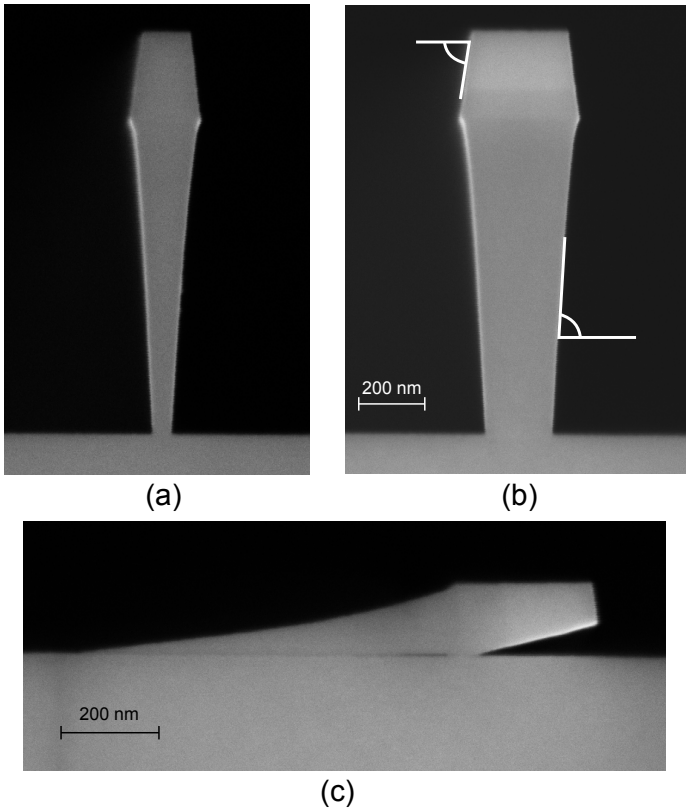


Figure 3.13: SEM images of pillar cross-sections after a long dry etching and a short wet etching. The same scale applies to (a) and (b). The epitaxy of the pillar from the top is the same as the fabricated samples with InGaAs and InGaAsP contact layers and 1 µm InP. (a) The thinnest pillar width of ~60 nm in the bottom. (b) A ~200 nm wide pillar with the indication of crystallographic dependences and angles of the etching steps. (c) The "sleeping" pillar: a too thin pillar collapsed without surviving the wet etching.

3.6 SiO_2 and BCB planarization

In section 1.3.4 the importance of a PhC slab surrounded by air was highlighted because light is confined by total internal reflection (TIR) in the out-of-plane direction. For TIR to be the most effective, the highest refractive index difference between the semiconductor membrane and the surrounding material has to be employed. One of the most common choices is therefore to confine PhC slabs in air. Due to cleanroom processing, the wafer epitaxy is usually carefully chosen with a semiconductor layer underneath the slab

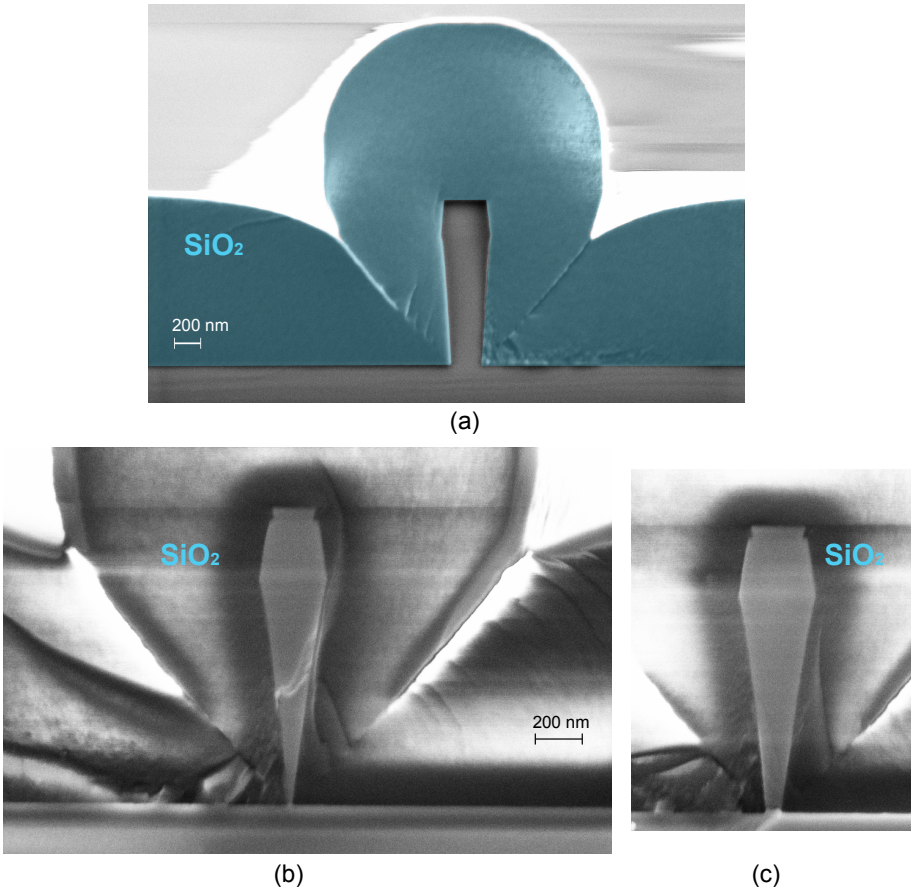


Figure 3.14: SiO_2 deposition after pillar definition. SiO_2 shows a "hot-air balloon" profile that follows the defined pillar with light blue color in (a). In (b) and (c) the thinnest pillars of bottom widths of ~30 nm and in (c)~70 nm covered by glass. The same scale applies to (b) and (c).

that can be removed (sacrificial layer), so that the PhC slab is suspended in air [14, 69]. Another approach is the one presented in [53], where HCl is used both for the pillar definition and the PhC membranization. Due to a different material choice for the membrane, we solved the membranization step with the use of a glass layer.

After the pillar definition, a thick SiO_2 layer is deposited in a PECVD system. This layer has to entirely cover the pillar and therefore its thickness is chosen of ~1.5 µm. In this fashion the membranization step (at the end of the whole fabrication process) can easily be realized by dipping the sample

in hydrofluoric acid to etch the glass layer away. When depositing SiO_2, one has to bear in mind that the glass follows the profile of what is already present on the sample, therefore it is not surprising that Figure 3.14(a) shows a "hot-air balloon" profile coloured in light blue, which follows the pillar walls. In Figure 3.14(b) and (c) other cross-section views of the pillar after glass deposition are depicted. Here the diverse etch profiles of the fabricated devices can be seen with the different angle dependencies (thin InGaAs and InP, contact layers, InP). The bottom pillar widths are among the thinnest inspected throughout the fabrication: in Figure 3.14(b) the thinnest pillar is ~30 nm and in Figure 3.14(c) ~70 nm.

A planar surface is required for the following metal contact step, and thus a way to planarize the sample and remove the glass from the top of the pillars was needed. A good option for planarization steps is benzocyclobutene (BCB), a well-known polymer in the microelectronic technology. BCB has the property of embedding all the structures already fabricated on the wafer, if a thick enough layer is spun on the sample and according to the heights of the features already present. In this way we span a thick layer of BCB after the SiO_2 deposition and after the polymer curing the sample becomes relatively planar. The major issue that was investigated at this point was a successful planarization of the sample that included the dry etching of both SiO_2 and BCB at approximately the same rate. When this condition is achieved, the whole BCB layer and the SiO_2 on the top of the pillar are removed. However since during the planarization step the physical part of the dry etching can deteriorate the quality and the doping of the top pillar layers, a protecting layer was introduced in the epitaxy. A first attempt was done by adding a thin InP layer on top of contact layers not to make major changes in the epitaxy, but bad adhesion between InP and HSQ resulted in the collapse of the structures during the wet etching for the pillar definition. We observed that the SiO_x hard mask fell and the InP pillars were partially etched reducing their height. Due to adhesion and masking issues the thin InP and InGaAs layers have been added on the top of the contact layers, as shown in the epitaxy in Table 3.1.

Figure 3.15 shows the results of the experiment conducted for the combined glass and BCB dry etching. RIE with a combination of CHF_3/O_2 was employed for the planarization etching, since it is known that this mixture of gases can etch both materials. For these tests the etch rates of BCB and SiO_2 have been evaluated as a function of the oxygen flow as shown is Figure 3.15. At first the pure etching of glass was evaluated (blue line), then pure BCB (green line), and in the end the etch rate of a SiO_2 piece placed

on a 4" wafer spun with BCB. In order to reduce the process sensitivity to "loading" effects, a 4" Si wafer covered with BCB has been used as carrier wafer in the RIE chamber both when only BCB and BCB plus SiO_2 have been etched. This trick renders the etching repeatable and reproducible without being dependant on the size of the sample. From Figure 3.15 it can be seen that the etch rate increases for both SiO_2 and BCB as the oxygen flow increases, with a similar value of about ~52 nm/min (blue and green lines) for an O_2 flow rate of 5 sccm. Unfortunately when a SiO_2 piece on the BCB carrier was monitored, a similar etch rate for the two materials was found at 4 sccmO_2 (magenta line). This value was chosen for the planarization recipe.[5] Although this step may seem relatively easy, it is quite delicate and small changes in the materials or machines (PECVD, RIE) could lead to slightly different etch rates than the results presented in Figure 3.15. Thus a constant monitoring with the laser interferometer (integrated in the RIE) was needed during the etching. In case the BCB etch rate is too fast compared to the glass etch rate, when the SiO_2 on top of the pillars is reached, the sample has to be further processed decreasing the oxygen flow to 3 sccmO_2 in the recipe.

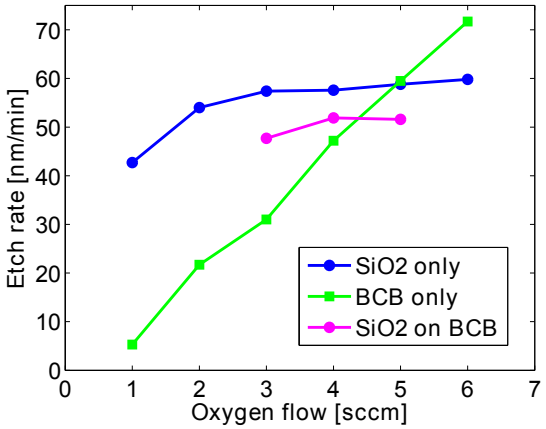


Figure 3.15: SiO_2 and BCB dry etching curves for the sample planarization in the RIE system. The blue line reports the SiO_2 etching only, the green line BCB etching only, the magenta line the combined etching of SiO_2 on 4" carrier spun with BCB. The combined etching of SiO_2 and BCB (magenta) was monitored for the most plausible oxygen flow candidates, i.e. 3, 4, 5 sccmO_2

[5] The parameters of the recipe can be found in Appendix B.

3.7 P-metal contact design

Due to symmetry issues, the pillar extends for the whole length of the PhC membrane and therefore an efficient way to electrically pump only the laser cavity is required. Although a standard method for separating contacts is to make additional openings through a photolithography step, adding extra complexity to the fabrication was not desired. The approach we developed consists in having two separated p-contact pads on the pillar side, as shown in Figure 3.16. In this fashion the contact lying in the middle of the PhC cavity is used to locally inject the current in the cavity. In order to avoid the current injection into the mirrors, a separated contact is made, which can work independently. Applying a separate voltage ($> 0.8\,\mathrm{V}$) on the mirrors-pad makes the PhC mirrors optically transparent with respect to the cavity.

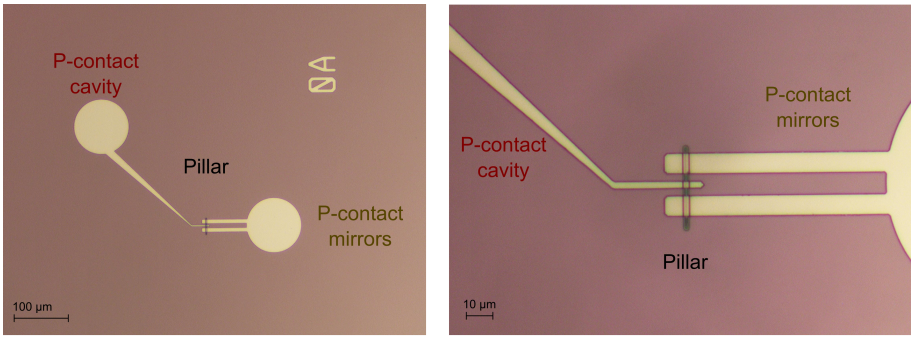


Figure 3.16: Microscope top-view of the devices after p-metal lift-off. (a) and (b) show the double p-contact design with different scales. In each image the pillar, the p-contact for the cavity and the p-contact for the mirrors are indicated.

3.8 Double-side processing

The whole fabrication process relies on the possibility of double-side processing, which is possible if a stable and good bonding technique can be used. After the pillar definition, the combined SiO_2-BCB planarization and p-metal deposition, the p-side of the device is completed. At this stage the wafer is flipped and bonded to a Si wafer in order to process the n-side of the components. The PhC pattern is written with e-beam lithography and due to the waveguide design and the pillar widths, the alignment between

the pillar and membrane layer is quite critical with a tolerance of ~100 nm in the worst case, depending on the pillar width and the hole radius.

3.8.1 Misalignment

One of the main challenges of the fabrication process has been the alignment between the pillar and the photonic crystals. Both patterns are written by e-beam lithography because of the small feature sizes and because of the high alignment accuracy of ~10 nm. The standard procedure is to do the alignment using "global marks", which consists of having two relatively big marks (because they have to be found by optical microscope at first) with L or cross shapes that can be used as reference for the machine, as stated in the e-beam manual [107]. Furthermore drift correction with a mark on the sample was chosen instead of the standard method with the drift mark on the e-beam cassette. If the assumption of a rigid system composed by the e-beam cassette and the sample was true, taking the drift mask on the sample or on the cassette would not make any difference. However when the e-beam cassette enters the chamber, the temperature has to stabilize and an expansion of the cassette due to the material of the cassette occurs according to the temperature drift. The temperature stabilizes over time, although small temperature drifts can also be detected during the exposure. In order to avoid being dependant on the cassette thermal stabilization for the drift compensation, the drift mark is taken directly on the sample. The accuracy of the mark position is measured of less than 15 nm, when repetitive scans of the same mark are performed.
Unfortunately the employment of drift correction on the sample and global mark alignment gave rise to contradictory results regarding alignment, as shown is Figure 3.17, and therefore an investigation of the causes was needed. Figure 3.17(a) and (b) show results of very good alignment between the PhCs and the pillar, in Figure 3.17(c) the pillar is at the edge of the WG with acceptable partial alignment. Figure 3.17(d), (e) and (f) show top and tilted-views of a bad misalignment ~750 nm. In Figure 3.17(e) and (f) the pillar can be recognized and seen even through the PhC holes. A few tests on the different e-beam resists (HSQ and ZEP) and exposure conditions led to the conclusion that the e-beam lithography was not the problematic step. The only other reasonable cause must have come from the adhesive BCB bonding, as it was proved with further tests.

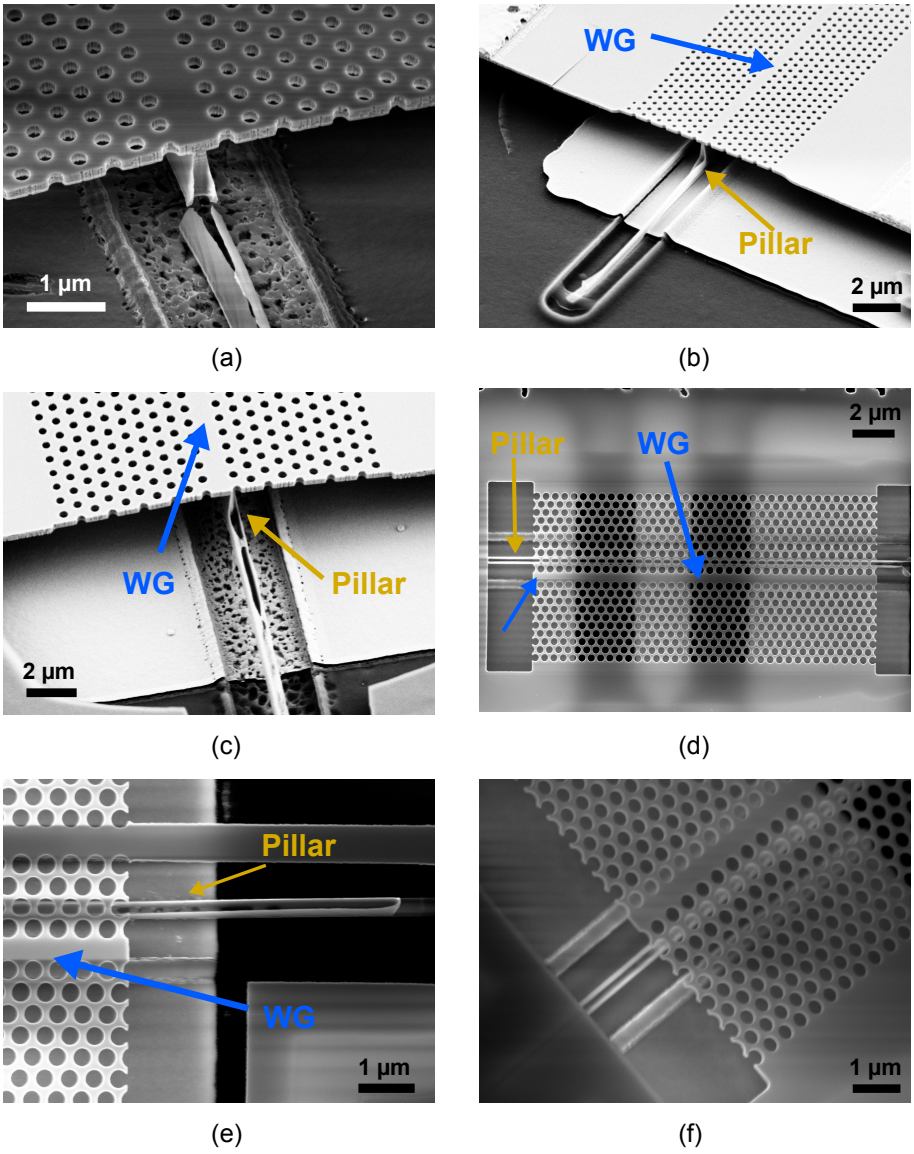


Figure 3.17: SEM images of finished devices with focus on alignment. In (a) and (b) pillar and PhCs are aligned, in (c) the pillar is partially aligned. (d), (e) and (f) show that the pillar is ~750 nm misaligned to the WG. (a), (b), (c) and (f) are tilted-views of the devices. (d) and (e) are top-views.

3.8.2 Adhesive BCB bonding

Due to the particular design of the devices and the double-side processing, the III-V wafer had to be bonded to another substrate and a good candidate is silicon, considering the final aim of hybrid integration. The bonding step can be realized with different techniques such as direct or adhesive bonding. In [108] a deep investigation of bonding requirements and analyses concerning stress, thermal properties and bonding strength is conducted in the comparison of direct and adhesive bonding for the realization of photonic devices.

The p-side of the devices is processed on a full 2" wafer, and before the bonding step, the wafer is cleaved into four quarters. Each quarter is bonded through BCB to a 2" silicon wafer in the EVG bonder. The option of bonding a 1/4 of a 2" processed III-V wafer to a full 2" Si wafer is relatively different compared to the standard full wafer [109] or dies [110] bonding, also because the III-V materials are usually processed after the bonding step. We chose this option, since we imagined that the following fabrication processing with a 2" wafer size would have been easier for example in the spin-coating steps. Due to double-side processing direct bonding was not further considered, because of the already processed III-V sample. The surface of the processed wafer cannot comply with the cleanness and smoothness required for direct bonding, since bonds are formed at an atomic level scale [108]. Adhesive BCB bonding is a powerful technique with a few advantages over the direct bonding, for example the high bonding strength at a low temperature (250°C) and less sensitivity to the wafer topography [111]. BCB is a thermosetting polymer that is in a gel-like state after spinning and soft baking, and it can therefore easily embed the topography of the wafers that have to be in contact [111]. During the bonding/curing stage, BCB becomes solid and bonds the two substrates together.

3.8.3 Bonding: pattern transformation

Bonding of different materials such as InP and Si, where the former has a thermal expansion coefficient almost double than the latter ($4.7 \times 10^{-6}/K$ and $2.6 \times 10^{-6}/K$ [93]), can be a delicate and problematic issue. The first assumption when bonding diverse materials consists of a uniform expansion or shrinking of the already processed pattern. For similar samples processed with BCB bonding our colleagues measured an expansion after

bonding of ~0.04%. If the expansion or the shrinkage are uniform on the sample, the e-beam machine can compensate enlarging or shrinking the mask, when alignment to a previous topography is carried out. Therefore we thought that even including a bonding step, the PhC pattern should have been aligned to the pillar layer with the standard "global mark" approach during the e-beam exposure. Unfortunately Figure 3.17 gives evidence of unrepeatable alignments with the standard global mark alignment method. For this reason we monitored how an already present pattern was modified after the bonding step. The tested wafer had a similar processing as our PhC devices and we investigated how the pattern (coordinates of features) written before the bonding step was modified after bonding. The results are reported in Figure 3.18 and discussed below. The unpredictable alignment with global marks of Figure 3.17 forced us to use a more accurate and somehow complicated alignment technique that requires extra alignment marks called "chip marks" [107]. In this case the alignment is carried out using both global marks and chip marks, which can have the same shape as the global marks. As suggested in the e-beam manual [107] we verified that the best chip mark alignment is obtained using four chip marks per chip, since pattern shifts and rotations can locally be corrected with this method. One could argue that the best alignment should be reached when the global marks are far from each other, as the accuracy is higher, than using chip marks, since a chip is by definition smaller than the sample size. This concept holds true if the change in the processed sample is uniform and therefore predictable, otherwise the local chip mark correction is more precise, because it can compensate for a non-uniform sample distortion. In Figure 3.18 we present the result of the test conducted on a bonded 2" sample that was processed in a similar way as the nanolasers: e-beam for the pillar, dry and wet etching for pillar definition, SiO_2-BCB planarization and adhesive BCB bonding to Si. For this experiment the equivalent of the pillar layer has been written by e-beam, the sample was processed and bonded, and after the InP substrate and InGaAs sacrificial layer removal, the positions of chips marks have been checked on the sample. Figure 3.18 represents a map of the designed and the measured coordinates of the chip marks that had been written before bonding and detected after bonding. The vectors represent the direction and magnitude of the marks displacements after bonding from the original designed positions. For this purpose the e-beam machine has been employed as "metrological SEM", since the mark coordinates are calculated by the electron beam scan of each chip mark on the sample. The accuracy of these measurements is the same as

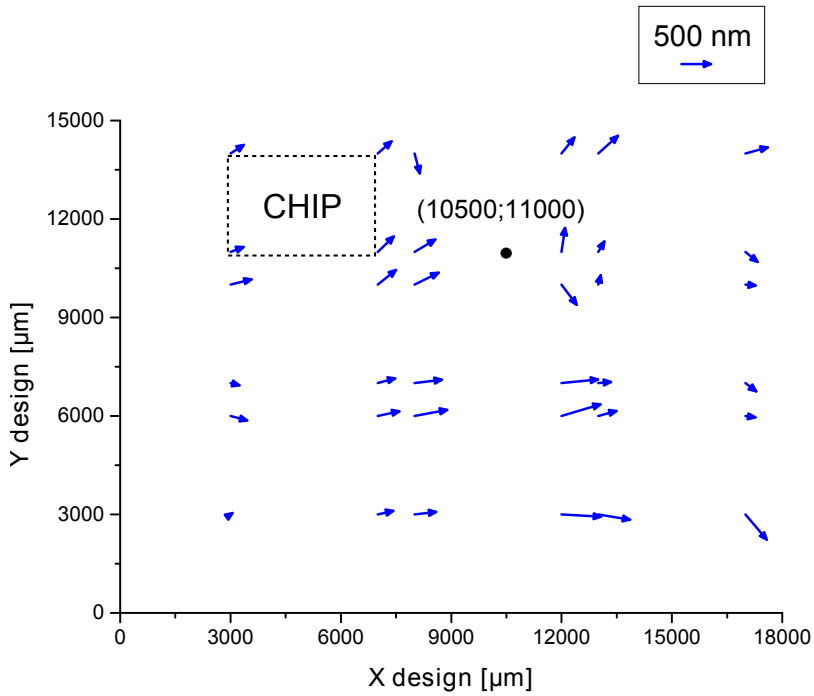


Figure 3.18: Vector graph representing the chip marks displacements after bonding from the original designed position. The sample is divided into chips with four chip marks each. An example of chip is indicated with a dash line rectangle. Each arrow gives the shift from the design coordinates of chip marks to the detected coordinates from the e-beam scan (e-beam as metrological SEM). The axes indicate real coordinates of one quarter of a full two 2" InP and Si wafers bonded through BCB. The vectors indicate the magnitude and the direction of the transformed coordinates.

the drift module, which is less than 15 nm. If a uniform change in the topography is expected, all the vectors should comply with the same type of transformation. On the contrary Figure 3.18 gives evidence of a distorted pattern, visible for example around the coordinates (10500;11000), where vectors close to each other have different directions and magnitudes. For this reason the chip mark alignment is a powerful mean, because it can compensate for random distortion of the sample topography that cannot be taken into account with standard global mark detection.

The proved random distortion of the pattern due to the bonding step is a relevant issue that should be modified and optimized in order to have a reproducible behaviour and a higher device yield. This unfortunate bond-

ing issue was discovered far in the processing and further changes in the bonding step could not be applied. The causes of the non-uniform bonding can be diverse: particles in the BCB, formation of bubbles or voids during the bonding step, and the difference of the thermal properties of the materials is not compensated in the cooling step after bonding. Furthermore when the piston applies the force in the bonder, if the sample is slightly off-centred or the piston itself damaged, a non-uniform force is applied on the sample, which can result in areas with different stresses and therefore different coordinate transformations. Since the origin of the bonding distortion may be quite difficult to be investigated, a diverse processing such as direct bonding, bonding with thinner BCB or with a different material is suggested for further improvements of this fabrication process.

We want to highlight that the chip mark alignment greatly improves the yield of good devices, because with the local alignment to chip marks there is more likelihood that a bigger number of chips and therefore a bigger number of devices is aligned. Conversely the alignment with global marks would results in aligned devices only close to the global marks and with the same coordinate transformation.

3.8.4 Bonding and substrate removal

The p-side of the devices is fabricated, when the main substrate is InP. After wafer-flip and adhesive bonding of the III-V sample to a Si wafer, the main carrying substrate becomes Si, since InP is removed by wet etching with pure HCl until the InGaAs etch stop layer is reached. After bonding the remains of BCB that cover the sample are removed by a plasma asher through CF_4/O_2 chemistry. This step is done to prevent the formation of InP cliffs at the edges of the III-V wafer during the following wet etching steps. Although this step is extremely useful to avoid cliffs at the edges, other types of cliffs appeared on the III-V epitaxy during the wet etching, as discussed below. The InP substrate and the InGaAs sacrificial layer are selectively wet etched in HCl [95] and $H_2SO4 : H_2O_2$ [96] solutions respectively. At this point the InP membrane is accessible and the n-side of the devices can be fabricated.

The mentioned random distortion of the pillar pattern after bonding is not the only cause of low device yield. Bonding is an art and any particles or mismatches of planes when the piston applies the force (750 N) during bonding can generate cracks that can propagate towards the InP substrate surface or remain buried into the substrate. Unfortunately the cracks are revealed after the InP substrate etching and have to be manually

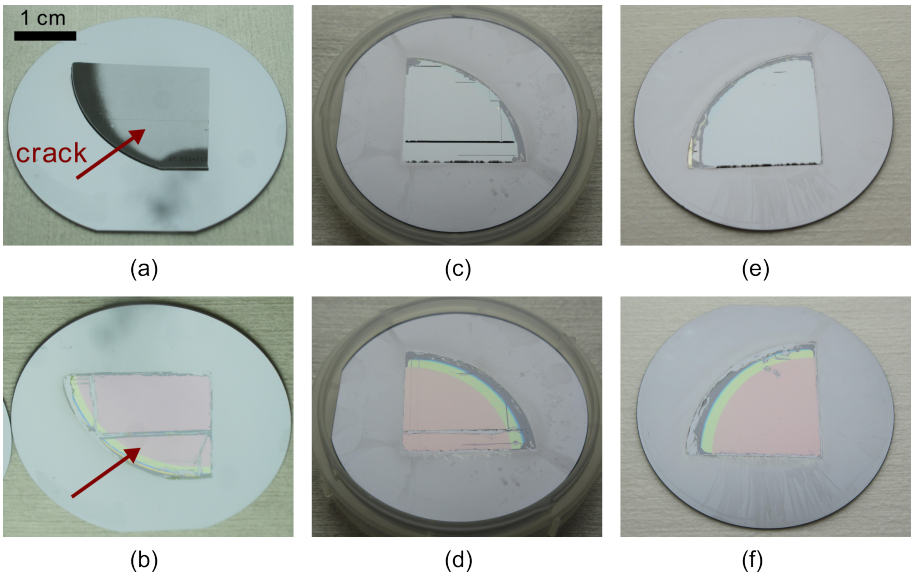


Figure 3.19: Images of three different 1/4 of III-V samples bonded to 2" silicon wafers. The same wafer is shown in (a) and (b), (c) and (d), (e) and (f) at different steps after bonding. The sample in (a) already shows a crack after bonding, which leaves a big material gap after wet etching and chiselling in (b). (c) reports the sample configuration after InP substrate removal with a visible cliff in the middle and on the side of the III-V quarter, which leave a material gap after the InGaAs etching shown in (d). The best bonded sample is shown in (e), where only a cliff at the edge of the III-V quarter appears after InP etching. In (f) the III-V quarter looks almost intact after chiselling and InGaAs etching. The scale provided in (a) is valid for all the images.

removed with a chisel, in order to reach good precision in the following photolithographies. The origin of the cracks is not known, but the statistics of their appearance on bonded samples is high, about 95%. The main problem for the cracks is that BCB before curing can penetrate into the gaps of InP and therefore it can mask, after it solidifies, some InP planes during the InP wet etching. The cliffs emerging after the substrate removal can be tens of microns high and after the wet etching steps many devices can be compromised, since cliffs can appear on top of the components. As mentioned above these remaining cliffs have to be manually removed with a chisel. This step increases the chances of damaging the wafer and in particular devices or marks for the e-beam alignment. No matter how delicate and how cautious the chiselling can be, if some chip marks of a chip are dam-

aged, close by chip marks have to be used instead. However, if even chip marks that are close to each other do not withstand the same distortion (random), as reported in Figure 3.18, the alignment for that chip can partially or totally fail. Figure 3.19 reports the images of a few bonded samples after bonding and after layers removal by wet etching. In Figure 3.19(a) the InP crack is already evident after bonding. In Figure 3.19(b) a big material gap along the crack has formed after InP removal, chiselling, and InGaAs removal. Figure 3.19(c) and (d) report the presence of a cliff in the middle and at an edge of the sample after etching, leaving material gaps. In Figure 3.19(e) and (f) one of the most successful bonding of 1/4 of III-V wafer to 2" silicon wafer is shown : in (e) only one cliff at the edge of the III-V sample appears after substrate etching, chiselling and InGaAs removal. In Figure 3.19(f) most of the III-V quarter looks intact, with a promising device yield.

Several attempts such as changing the one-step wet etching of InP with hydrochloric acid to two steps etching with the first one in a mixture of acetic acid and hydrogen peroxide ($CH_3COOH : H_2O_2$)[112], which is not selective to InGaAs, followed by HCl (selective to InGaAs), did not improve the result. The option of mechanical lapping has also been considered, since it was reported successful by other groups, e.g. [113]. The samples after mechanical lapping and InP substrate removal are presented in Figure 3.20. The results provided by this procedure are even worse than for pure wet etching, as shown in 3.20(a) and (b). It is apparent from 3.20(a) that mechanical lapping is a too harsh technique for our wafers, since cracks on InP have been generated all over the sample.

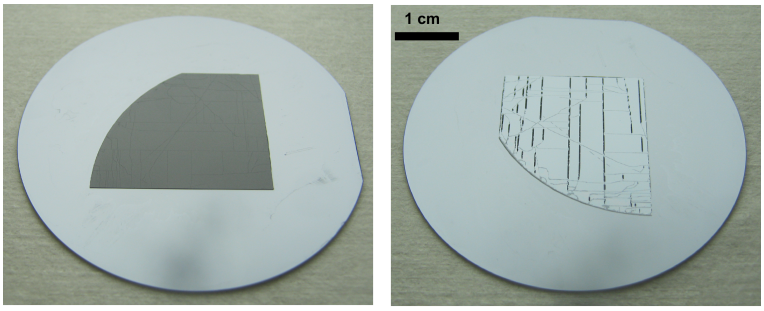


Figure 3.20: Image of a sample after lapping (a) and after InP substrate removal (b). Cracks and cliffs are already evident after lapping. The scale provided in (b) is valid for both images.

3.9 PhC pattern

The PhC pattern is written by e-beam lithography with two different high resolution resists: either the negative-tone HSQ (Fox-15) or the positive-tone ZEP (ZEP 520A). The two approaches have been investigated, since high quality of holes and robust fabrication steps are required. Although the employed resists should be among the best for writing patters such as PhCs, the difference in the resist-tone and the following dry etching step give different quality of the etched PhC holes. Furthermore the fabrication steps following the e-beam lithography have to be modified according to the areas written with the e-beam, which depend on the resist-tone.

3.9.1 Fabrication of PhC holes with HSQ

3.9.1.1 PhC pattern

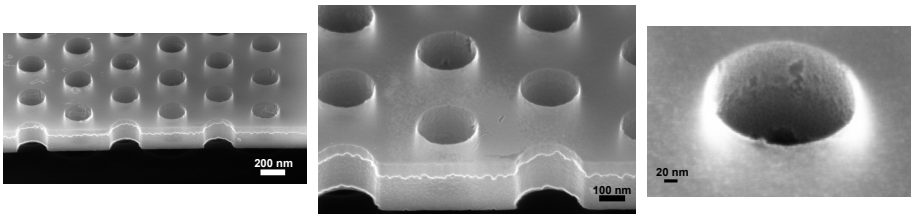


Figure 3.21: SEM inspection of PhC holes processed with HSQ after dry etching and membranization. In (a) and (b) the PhC membrane at different magnifications. In (c) a single PhC hole with the highest resolution possible for the sample is reported.

In order to get good optical properties with PhCs, the holes have to be very well defined, smooth, and with vertical sidewalls. PhC holes obtained with HSQ are shown in Figure 3.21 with different scales, which are quite good in terms of smoothness and definition. After e-beam exposure and resist development the crosslinked HSQ, which has become a glass-like layer, forms the photonic crystal hard mask for the semiconductor etching. As for the pillar case, HSQ is used as hard mask for the pattern transfer to the semiconductor membrane in a dry etching step. The dry etching, like in the pillar case, c.f. section 3.5.1, is performed in the RIE system with a cyclic process of the CH_4/H_2 chemistry and oxygen cleaning.

Since HSQ is a negative-tone resist the complementary image of the hole pattern is written in the e-beam and a bigger area surrounding the scheme

is also included, in order to allow metal contact on the membrane. PhC holes need a high resolution, achieved with a low current of 6 nA, while 60 nA is used for the bigger areas surrounding the holes pattern. For both patterns the same base dose of 5000 $\mu C/cm^2$ and PEC have been applied.

The good quality and resolution of the holes pattern that can be achieved with HSQ [97], is also at the expenses of the following fabrication steps in our process. When etching small (PhC holes) and big features (devices membrane pads) in the RIE, several effects have to be considered. The main issue of lag effect has already been reported and analyzed for example by Keil and Anderson [114] and it was proposed to be a mechanism caused by ion shadowing, neutral shadowing, and differential charging. The RIE lag is also largely dependent on the etching chemistry used and the processes taking place in the etching chamber. Earlier work performed on the same RIE machine at Danchip for the etching of trenches and pillars likely identified ion shadowing as a limiting factor in the etch rate for high aspect ratio features [115]. Ion shadowing can be due to the fact that all ions do not strike the surface of the sample in a perpendicular way, and from geometric considerations, the smaller the features and the thicker the mask, the slower the etch rate becomes, since more ions are blocked [116]. Besides lag effects for PhC holes investigated in [117], the semiconductor load in the RIE chamber during the CH_4/H_2 dry etching should be considered. Due to the design of the devices (negative-tone resist), after a few cycles of dry etching, most of the InP membrane is removed, giving separation among the devices. In this fashion the InP load drastically changes in the chamber. However a continuation of the process is needed to obtain straight PhC holes, due to the slower etch rate of small features. To keep the InP load constant, an InP carrier can be introduced during the dry etching of the processed sample. However testing different RIE recipes and dry etching durations, the best performance was achieved with the optimized recipe for CH_4/H_2 in a 12.5% ratio and without including any InP carriers for the whole etch duration, as shown in Figure 3.21.

3.9.1.2 N-metal and membranization

For the n-metal lithography the HSQ hard mask has to be removed and for this step a short dip in BHF is easy to perform. However, since all the devices have been isolated during the PhC dry etching because of most of the InP membrane removal, a direct dip of the sample in BHF would also etch the surrounding SiO_2 layer, creating a higher step height than the semiconductor membrane, which should be compensated by a thicker metal

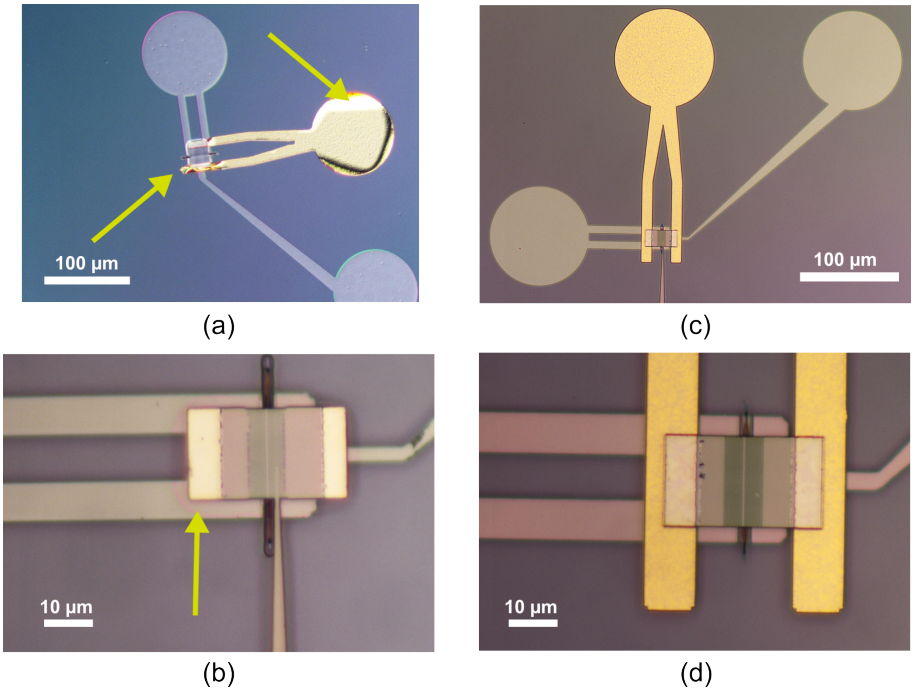


Figure 3.22: Microscope images of n-metal pattern for devices processed with HSQ for PhC holes. (a) Device with big metal pad (arrow to the right) that is not entirely connected to the metal on the top of the semiconductor membrane (arrow to the left). (b) Device with n-metal only on the top of the semiconductor membrane (arrow). In (c) and (d) the n-metal adheres to both glass and semiconductor layers.

deposition. We therefore decided to add an extra step in order to selectively remove the HSQ glass-like layer from the top of the devices. A kind of planarization step with AZ resist (photoresist by Microchemicals) was used to only reveal the top of the devices. A short ashing recipe (dry etching of AZ with oxygen) in the RIE was performed for this purpose. It is a delicate step, because accurate and continuous dektak height measurements of the resist have to be performed, in order to precisely control when the device membrane is revealed. In this way the hard mask can be selectively wet etched and no step height increase between the semiconductor membrane and SiO_2 is created.

The n-metal deposition is performed with a negative photolithography with AZ2020 resist, metal evaporation and lift-off process, analogously to the p-contact. The problem we encountered for this step was evident at

the later stage of electrical characterization of the devices. Unfortunately no current could be driven for most of the devices from the big n-metal pad to the n-doped InP membrane, as depicted in Figure 3.22(a) and (b) with arrows where metal disconnection can be observed. This metal disconnection was further proved by measuring the current when one needle probe was touching the big metal pad lying on SiO_2 and the other one was touching the metal on top of the device. The electrical characterization was difficult to carry out, since the devices are very fragile after the SiO_2 membranization, as they mostly stand on the thin pillar and because of the small dimensions of n-doped InP areas with metal compared to the needle sizes. This issue arose the likelihood that the metal discontinuity could be due to bad adhesion of metal on glass and to a high step height between the semiconductor membrane and surrounding glass layer (metal thickness ~290 nm vs membrane thickness ~220 nm). Examples of successful metal adhesion to both SiO_2 and InP membrane are shown in Figure 3.22(c) and (d).

3.9.2 Fabrication of PhC holes with ZEP

For the PhC fabrication another high resolution positive-tone e-beam resist ZEP520A was also tested. Previous work on PhC devices reported a major problem of ZEP foaming if the pattern after the e-beam lithography is directly transferred to III-V semiconductors [117]. For this reason an intermediate layer has to be deposited, which can work as hard mask during the semiconductor dry etching. PECVD Si_3N_4 has been reported as a good material for this purpose, since it can withstand the semiconductor RIE step [14, 117]. In this fashion prior to the e-beam lithography, a layer of ~200 nm of Si_3N_4 is deposited.

ZEP is a positive-tone resist and therefore the PhC holes are written during the e-beam exposure. Compared to the HSQ pattern discussed in section 3.9.1, the separation of the devices does not occur during the RIE dry etching. This is due to the tone of the resist: in the case of positive-tone resist only the photonic crystal pattern is written, since it is the part that is going to be removed after the resist development; in the case of negative-tone resist a design complementary to the PhCs and the InP membrane pads have to be written, since only the crosslinked HSQ will remain after development. Thus when making PhCs with ZEP the removal of most of the InP membrane for the devices separation had to be added during the photolithography after the bonding step, where the global alignment marks are revealed. After e-beam exposure the pattern is transferred to the

Si_3N_4 layer during the RIE dry etching with the CHF_3/O_2 chemistry. The e-beam resist is stripped and then the PhC pattern can be finally transferred to the semiconductor membrane with the same recipe as for HSQ. However a shorter dry etching is necessary, since the semiconductor load is fairly constant as the etching mainly occurs into the PhC holes. In Figure 3.23 the PhC holes are displayed. Comparing Figure 3.21 and Figure 3.23 it is evident that the introduction of a hard mask for the ZEP processing worsen the quality of the holes that can be achieved with HSQ.

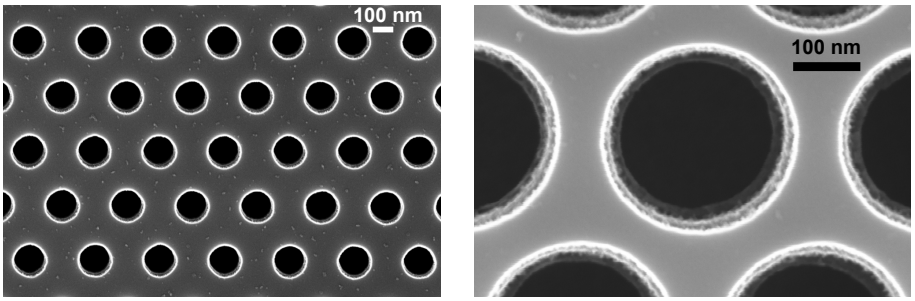


Figure 3.23: SEM inspection of PhC holes processed with ZEP after dry etching and membranization. In (a) and (b) the PhC membrane is shown at different magnifications.

3.9.2.1 ZEP holes correction

Controlling the size of the PhC holes is important for the optical properties of the devices. Ideally the holes should have the same size as specified in the design file for the e-beam writer. However all the following fabrication steps such as resist development, PEC, hard mask and semiconductor etching can enlarge the hole size. The hole widening phenomenon was analyzed and successfully controlled in previous work [14, 117] and a similar approach has been adopted in this project.

The reproducibility of the process is chased keeping the development, the hard mask etching and the semiconductor etching time constant, while optimising the dose for the e-beam exposure. The latest dose test is reported in Figure 3.24(a). Considering previous experience [117], the trends of Figure 3.24(a), and the quality of the PhCs, a dose of 240 $\mu C/cm^2$ was used. This dose gives a cumulative hole widening of ~60 nm in diameter in the target range of 220 nm-240 nm in hole diameter. The result of a too

long semiconductor dry etching is shown in Figure 3.24(b), where the hole widening is evident.

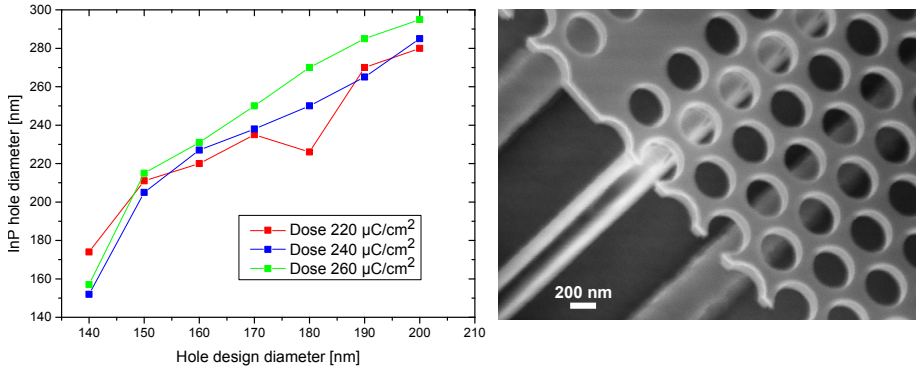


Figure 3.24: (a) Dose test results for the final PhC holes size after the dry etching step as a function of the designed hole size. The dose color legend is 220 µC/cm^2 red, 240 µC/cm^2 blue, and 260 µC/cm^2 green. (b) Tilted-view of a PhC membrane with hole widening due to a too long semiconductor dry etching.

3.9.2.2 Electrical injection issue

With ZEP processing the devices are less fragile than in the HSQ case, since the InP membrane extends in larger areas, so that the devices are both standing on the thin pillar and on wide membrane side-pads. This fact derives from the tone of the e-beam resist. After the PhC pattern transfer the sample follows the same steps of n-metal lithography and membranization as described in section 3.9.1.

When characterizing the first sample processed with ZEP, the current injection seemed not to be possible at low voltages. The cause behind this issue had to be investigated and the physics behind it understood in order to fabricate good devices. Several considerations about doping issues have been made since a dependence of the current to external light sources has been observed. At first the p-side has been examined in terms of the depletion of the pillar and device passivation. The conducted passivation tests with ammonium sulphide ($(NH_4)_2S$) did not give any further hints, excluding the hyphotesis of InP persistent photoconductivity [118–120]. Thereafter the n-doped side was analyzed. The hypothesis of PhC depletion reported in [121] was ruled out, since devices with similar PhC hole patterns processed with HSQ lithography did not show behaviours of

too high resistance or high input voltage.

The possibility of "dopant passivation" was therefore considered, as other likely cause presented in [122]. Problems with n-doping levels may have occurred, since a high electrical resistance was measured. The InP n-doping consists of two thin n-doped layers on the top of the PhC membrane, as listed in Table 3.1. The choice of having two n-doped layers is made in order to reduce optical losses. On one hand a good contact is formed when the metal is in contact with a highly doped semiconductor. On the other hand optical losses originate from the overlap integral between the field and the doped layers. When the field amplitude increases and the doping level decreases, losses decrease, which is a favourable situation than a constant doped top layer. Although this considerations are beneficial for losses, if the thin highly n-doped top layer is damaged, it can loose its doping concentration and not allow current flow. The high electrical resistance and the high driving voltage could have therefore been a result of a too low doping level. The cause of dopant passivation has been investigated with several tests performed with the Si_3N_4 PECVD deposition, as we recognized this step the most plausible for surface (doping) damages, as proposed in [123]. Photoluminescence was employed as diagnostic method for the doped semiconductor surface quality. Low doped InP samples have been analyzed after the Si_3N_4 deposition with or without a spin-on glass-like layer protecting the semiconductor. The decrease in the photoluminescence (PL) intensity proved that the recipe used in the PECVD for the Si_3N_4 deposition damages the sample surface, and therefore decreases the doping level. This doping issue was unfortunately never addressed in earlier work performed at Danchip [14, 117], since only optical characterization was performed and no doping needed. An optimization of the nitride recipe could solve the doping-level problem, however the possibility to use a plasma enhanced atomic layer deposition (PE-ALD) system was evaluated to prevent surface damages.[6] A thin SiO_2 layer of about 20 nm was deposited with a PE-ALD system in order to avoid the dopant/surface damage during the Si_3N_4 PECVD deposition. This additional step solved the dopant passivation issue and improved the electrical characterization of the devices.

As an optimized version of this fabrication process a different Si_3N_4 PECVD recipe should be investigated. In this new recipe the specific condition of avoiding ion bombardment for the first ~20 nm of deposition is essential to preserve the doping concentration.

[6] This fabrication step has been performed at Lund NanoLab facility, Lund, Sweden.

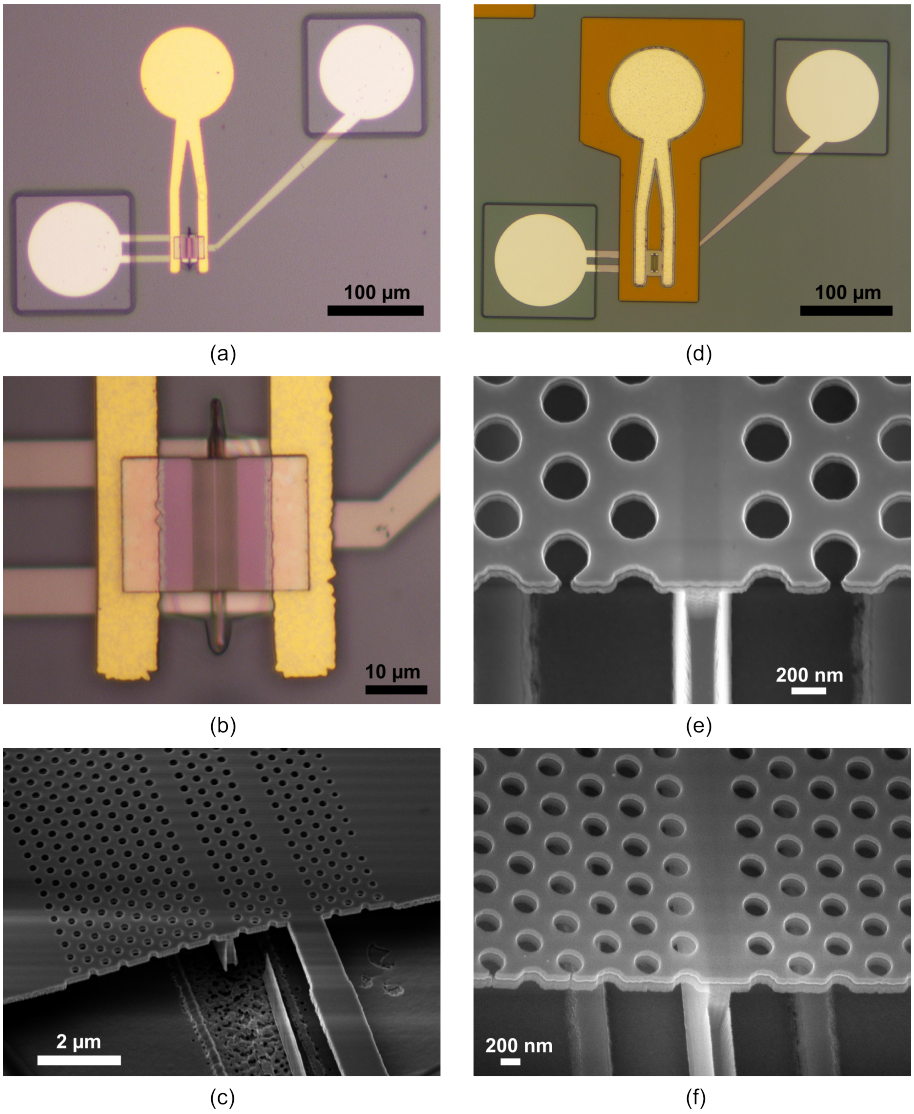


Figure 3.25: Microscope (a), (b), (d) and SEM (c), (d), (e) images of final devices after the membranization step. (c) and (e) are tilted-views, while (d) is a device top-view with focus on the PhC membrane with pillar underneath. In (a) and (c) the p-contact pads are revealed (squares surrounding the pads) through the membranization lithography. In (a), (b) and (c) the devices are processed with HSQ, while in (d), (e) and (f) the devices are processed with ZEP for the PhC pattern.

3.10 Final device

The final step in the fabrication process consists in the membranization of the PhC membrane. In this step the SiO_2 layer underneath the PhC membrane has to be wet etched and the acid solution called SiOetch is used for this purpose. The wet etching solution is composed by a BHF mixture and a wetting agent, so that the membranization of the devices is facilitated through the PhC holes. The final devices are reported in Figure 3.25 both in the case of PhCs processed with HSQ in (a), (b), (c), and ZEP in (d), (e), (f). The membranization lithography is also necessary to access the p-contact pads embedded in the system, as can be observed in Figure 3.25(a) and (d).

3.11 Summary

In this chapter the entire fabrication process has been presented and described. A more detailed discussion about the most challenging steps has been given. The pillar profile has been investigated according to the dry and and wet etching steps. A successful way of mutual SiO_2-BCB planarization with approximately the same etch rate condition of dry etching has been found. The double-side processing has been examined with focus on the adhesive BCB bonding, due to the random results of misalignment between the pillar layer and the PhC pattern. The experimental tests conducted on adhesive bonding revealed the randomness of sample distortion after the bonding step. To improve the PhC alignment the use of chip-mark alignment has been employed during the e-beam writing. However if InP cliffs appear after substrate removal, damages on chip marks and devices can be expected. Therefore if some chip marks for a specific chip are not available, nearby chip marks have to be used. As a matter of fact if the new chip marks do not withstand the same distortion of the original chip due to the bonding step, the alignment for that chip can partially or totally fail. In the end the analysis of the e-beam lithography for the PhC holes with HSQ and ZEP resists has been conducted. HSQ revealed its superiority concerning the quality of the PhC holes at the expenses of the following fabrication steps. The ZEP lithography showed advantages in guaranteeing an overall robust fabrication processing, although a hard mask layer (Si_3N_4) has to be deposited with PECVD before e-beam resist spinning. A further step of thin glass deposition with PE-ALD had to be introduced before the Si_3N_4 deposition in order to avoid surface and doping damages from the

PECVD to the top n-doped InP layer of the membrane to secure electrical injection.

Chapter 4

Device Characterization

In this chapter the characterization of the fabricated Photonic Crystal (PhC) devices is described. In order to achieve electrically injected devices, the electrical characterization has been carried out. The optical characterization of the devices under electrical injection only resulted in light-emitting diodes. The devices have also been optically pumped and lasing was achieved at room temperature (RT) and in pulsed regime.

4.1 Photoluminescence emission

The first characterization of the devices consists in a qualitative evaluation of the photoluminescence (PL) spectra of the active material. This is an important step in order to match the emission wavelength of the active material to the Photonic Crystal (PhC) design. In Figure 4.1 an example of RT PL spectral map of the peak wavelength is shown on the right side. The PL emission cannot be done after wafer growth, since the emission would come from the contact layers. Furthermore the PL spectra can be acquired only after bonding, when the InP substrate and the InGaAs etch stop layer are removed. Any PL characterizations before the InGaAs etch stop layer removal would show the InGaAs emission and not the QWs, since the etch stop layer is thicker than the active layers, as reported in Table 3.1. This is why the spectral map of Figure 4.1 is confined to a III-V quarter. The PL spectral map shown in Figure 4.1 on the right does not look uniform with the given color scale bar and this is due to the fact that the sample has already been extensively processed. On the left part of Figure 4.1 single spectra of the peak wavelength in diverse sample locations are reported. Although the center emission wavelength of the QWs should have been at

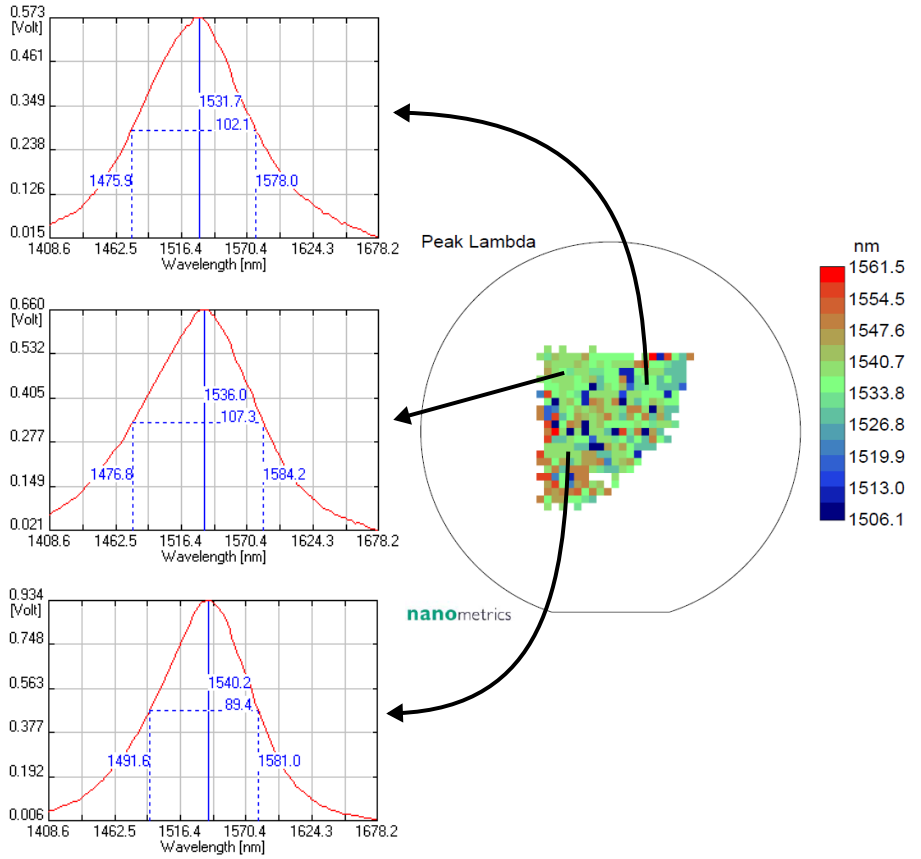


Figure 4.1: On the right RT PL peak wavelength spectral map of a sample with two PQ QWs. On the left single RT PL spectra at different locations of the III-V quarter. The spectra are obtained with a 532 nm laser source.

1550 nm, the small variation (1531 nm-1540 nm) is still acceptable for the designed PhC pattern.

4.2 Light emission of photonic crystal devices

A few examples of the devices light-emission from a top-view inspection are presented in Figure 4.2. The infrared light emission of the fabricated devices is a great achievement, although no lasing has been observed. To better understand the device position on the stage and observe the position of the emitted light, we illuminated the devices with an IR 940 nm GaAlAs/GaAs

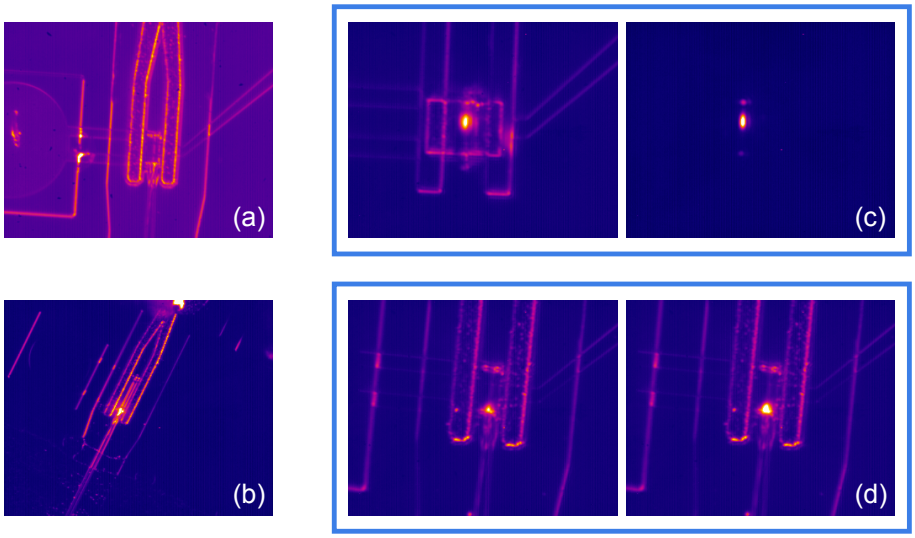


Figure 4.2: Top-view of the devices under electrical injection and infra-red light illumination with IR 940 nm GaAlAs/GaAs LED. (a) IR illumination of a PhC device with output WG. (b) Illumination of a PhC device with output WG under current injection. The optical characterization of this device is shown in Figure 4.7 (a). In (c) on the left a device for top inspection (no output WG) is shown under IR illumination and current injection. On the right the device emission is shown without illumination. The applied voltage is 3.5 V. (d) Device with output WG under IR illumination and electrical pumping for two increasing pumping levels 16 V on the left and 18 V on the right. All the images are taken with an IR camera, which is cooled at the temperature of 242 K.

LED. A device under illumination is reported in Figure 4.2(a). In Figure 4.2(b) we present a device with an output WG design when it is under illumination at the electrical injection level of 13 V (high voltage issue of the 2nd generation of devices). Due to the WG design, the light-spot is concentrated at the end of the PhC output WG. From the comparison between Figure 4.2(c) and (d), we can observe that the different light spots follow the optical design (with and without PhC output WG). In Figure 4.2(c) a device for top inspection when the IR LED is turned on (left) and off (right) at 3.5 V is presented. The main light spot can be observed in the middle of the PhC cavity with some scattered light at the edges of the mirrors. In Figure 4.2(d) a device with output WG is depicted at two increasing pumping levels and with IR illumination. In this case the major light spot can be recognized at the edge of the PhC output waveguide.
Although the fabricated PhC devices are designed for in-plane emission, the

utilized optical setup can collect the spectra of the scattered light from a vertical direction that is perpendicular to the device in-plane PhC laser emission. From this top inspection not only the emission from the photonic crystals can be observed (from a critical angle), but all the spontaneous emission of the device is collected. We relied on this type of measurement, since lasing emission has been demonstrated for optically pumped PhC lasers in a similar way [47]. For the in-plane detection an optimization of the output waveguide and cleaving techniques have to be implemented.

4.3 Device generation and measurement setup descriptions

During the fabrication diverse samples have been processed, but only a few devices could be characterized. The aim of this chapter would have been the discussion of the results and the investigation of different trends among diverse cavity lengths, active materials and designs, but a few complications during the fabrication did not allow us to conduct such an analysis. For this reason only the most significant characterization results are shown in this chapter. The discussion of the results is divided into four categories:

- The **1st generation** comprehends the sample processed with HSQ for the PhCs. In this case only the electrical characterization is shown.
- **The 2nd generation** includes the first sample processed with ZEP for the PhCs. In this fabrication process the PE-ALD deposition step was not included. In this case the electrical characterization shows a strange behaviour of high electrical resistance and light dependence, which has already been mentioned in Chapter 3. Representative optical results are given.
- **The 3rd generation** includes the sample processed with ZEP for the PhCs including PE-ALD deposition. In this case the problem of high resistance found in the 2nd generation has been solved and representative optical measurements are given. Both optical and electrical results can be considered mainly for a qualitative analysis, since this sample got damages at the end of the fabrication process in the annealing step, probably due to a too high temperature achieved in the chamber compared to the setting. The layer of BCB used for bonding could not stand the high temperature and created air bubbles that destroyed most of the devices.

- **The 4th generation** of devices was fabricated in the same way as the 3rd generation (PhCs with ZEP and including the PE-ALD deposition), taking precautions during the annealing step. Even though the fabrication process was successful, only a few devices could be electrically pumped. The electro-optical characterization is shown, although lasing was not observed.

All the devices are named with a letter and a number that describe their position on the sample and specific design parameters. Furthermore in the following graphs each device name is followed by "op" or "wg" according to the type of PhC design. The "wg" ending stands for the optical design with output waveguide, whereas "op" devices are without. For all the devices the cavity pitch is 456 nm long.

The setup for the electrical characterization is presented in Figure 4.3. The sample is mounted on a copper stage with Peltier element to control the temperature through the temperature controller. The high current Source Meter Unit (SMU) Keithley 238 is remotely controlled with a LabView program for the voltage-current sweep via PC through GPIB interface. The setup for the optical characterization under electrical injection is presented in Figure 4.4. The sample is electrically injected with the high current SMU Keithley 238. The light emission from the sample is observed through an infrared camera and the emission from the PhC devices is vertically collected using a microscope objective with a numerical aperture of 0.65. The signal is collected through a multi-mode fiber and thereafter sent to a grating mirror and analyzed with a highly sensitive spectrometer with a cooled array of low-noise InGaAs photodetectors.

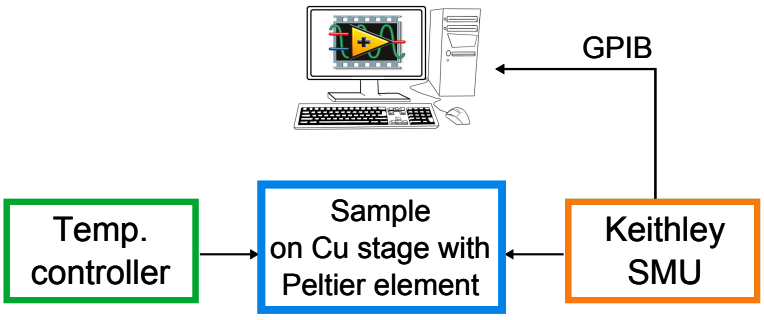


Figure 4.3: Schematic of the experimental setup used for electrical characterization of PhC light-emitting devices. The temperature controller was set at 20°C.

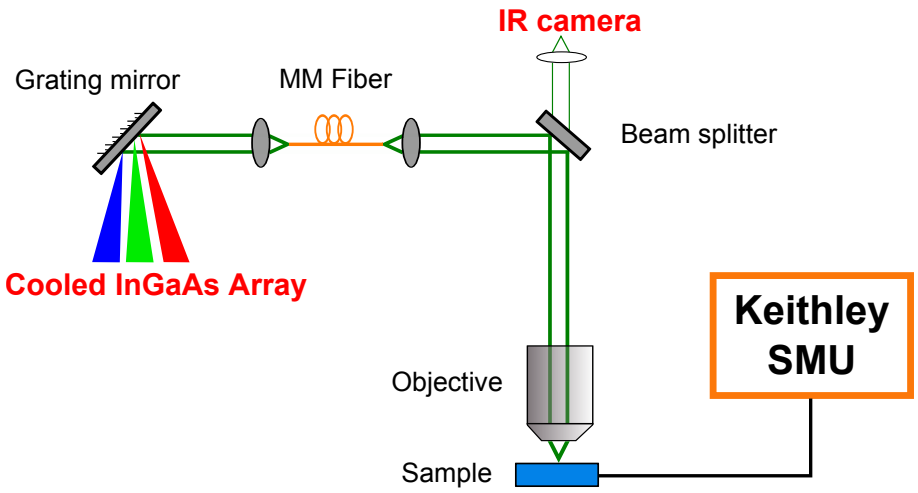


Figure 4.4: Schematic of the experimental setup used for optical characterization of PhC light-emitting devices under current injection. The cooled InGaAs array spectrometer operates at −100°C.

4.4 Electrical and optical characterization

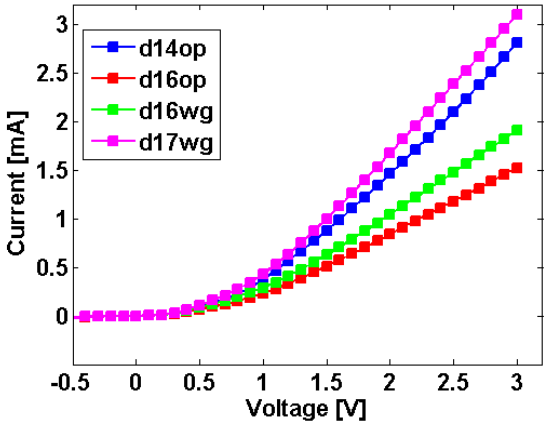


Figure 4.5: Current as a function of voltage for the first generation of devices. All the devices have the same cavity length of 99 pitch. Devices d14op and d17wg have a hole size of 110 nm in radius, while devices d16op and d16wg have a 115 nm radius. The pillar width at the bottom of the membrane is ~170 nm for d14op and ~220 nm for the other three devices.

For the 1st generation of devices the electrical characterization is reported in Figure 4.5. The four devices have the same cavity length of 99 pitch. Devices d14op and d17wg have a hole radius of 110 nm and devices d16op and d16wg of 115 nm. The electrical resistance is derived from the slope of the voltage-current curves above threshold and all the values are ~1 kΩ. Devices d16op and d16wg show a slightly higher electrical resistance of 1.5 kΩ and 1.2 kΩ respectively that could be due to the bigger photonic crystal hole size and to the thinner pillar widths. Devices d14op and d17wg show a 800 Ω and 700 Ω resistance. All the four characterized devices have a voltage threshold ~0.8 V, which is the expected value for these light-emitting devices.

For the 2nd generation the electrical characterization is quite problematic as shown in Figure 4.6(a). These curves are quite different compared to the first generation, due to the higher voltage that has to be applied and because of the sensitivity of the devices to illumination. After a device is illuminated with the microscope light and light from an infrared LED (940 nm GaAlAs/GaAs), a decent electrical characterization under illumination and after illumination could be carried out. The illumination works as a turn-on feature, which gives an intermittent performance. In Figure 4.6(a) the

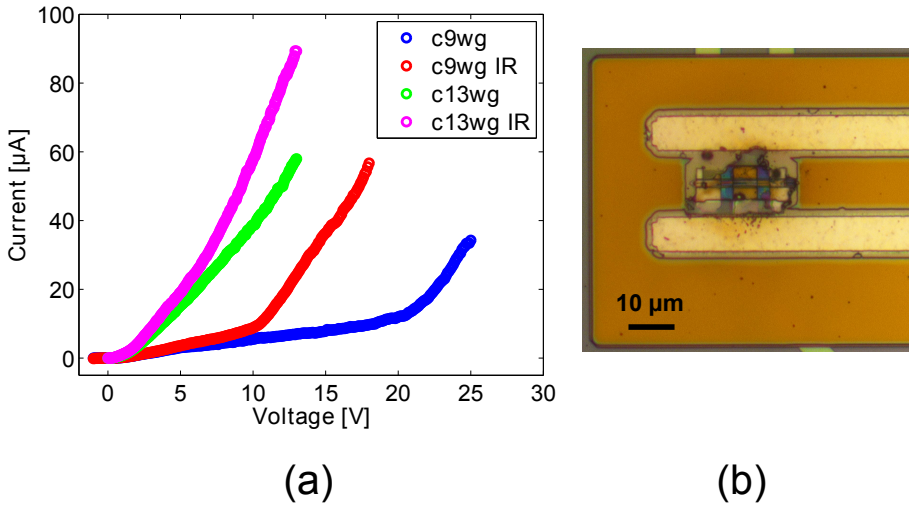


Figure 4.6: (a) Current as a function of voltage for the second generation of devices. Device c9wg has 19 pitch cavity length, 120 nm hole radius, and ~170 nm pillar top width. Device c13wg has 99 pitch cavity length, 115 nm hole radius, and ~220 nm pillar top width. In the legend the IR ending stands for the measurement under IR illumination. (b) Microscope top-view of a device burnt on the cavity.

voltage-current characteristics of two representative devices are shown. The two curves per each device are taken under IR illumination and after having illuminated the sample. The electrical resistances that can be interpolated from the graph are on the order of hundreds of kΩ, which is a too high value for such small devices. For example the calculated electrical resistance for device c13wg is ~100 kΩ under IR illumination and ~200 kΩ without. The resistance values have been derived from the slopes of the curves from Figure 4.6(a). The high voltage issue has become a big problem, when a few devices have been burnt on the PhC membrane because of the generated

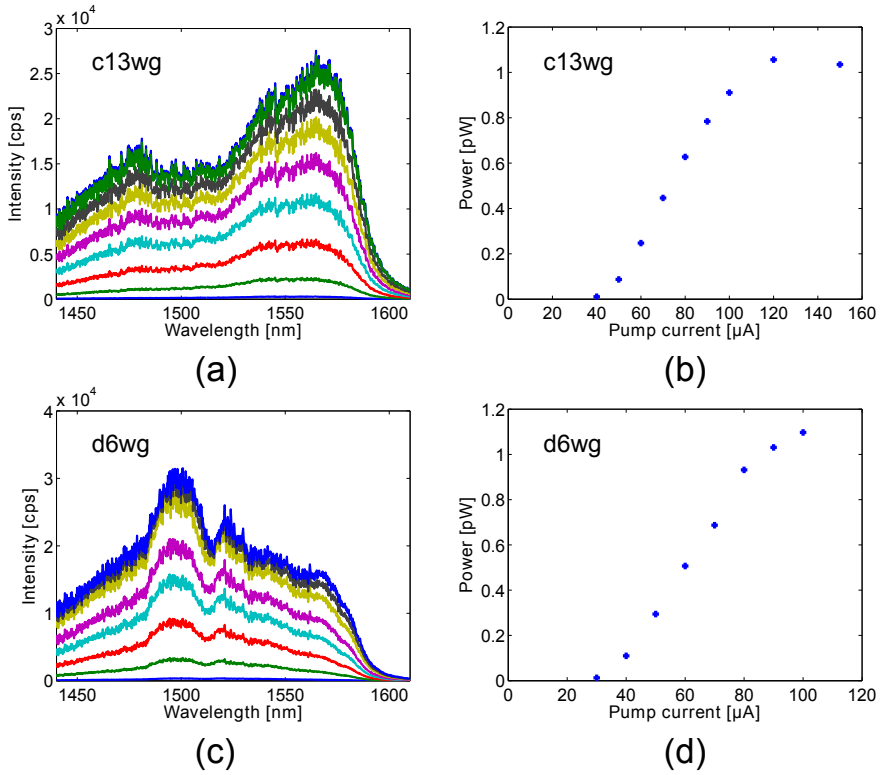


Figure 4.7: Optical characterization of devices of the 2nd generation. In (a) and (b) the optical spectra (linear scale) and the measured output power as a function of input current for device c13wg. The input current range is from 40 µA to 150 µA. Device c13wg has 99 pitch cavity length, 115 nm hole radius, and ~220 nm pillar top width. In (c) and (d) the optical spectra (linear scale) and the measured output power as a function of input current for device d6wg. The input current range is from 30 µA to 100 µA. Device d6wg has 49 pitch cavity length, 120 nm hole radius, and ~220 nm pillar top width.

heat, as shown from the microscope top-view in Figure 4.6(b). The devices that could survive high voltages have also been optically characterized as reported in Figure 4.7 with the experimental setup shown in Figure 4.4. No lasing emission has been detected, as reported in Figure 4.7(a) and (c). In Figure 4.7(b) and (d) the curves of the output power as a function of the input current are shown. For this evaluation the integration of each optical spectrum in the wavelength range 1430 nm-1615 nm is considered. The reason for the strange physical behaviour of these devices has been derived through a difficult analysis already discussed in Chapter 3, which resulted in a small change in the fabrication process. After several tests that included the device passivation with ammonium sulphide and investigation of InP persistent photoconductivity due to the light-dependent curves [118–120], the hypothesis of dopant passivation has been tested. PL measurements have been performed on low-doped InP with and without a protecting layer before Si_3N_4 PECVD deposition. For the obtained PL spectra we observed that if no protecting layer was applied before the Si_3N_4 deposition, the intensity of the PL emission dropped. Thus we proved that the recipe used for the PECVD deposition (low RF frequency) creates damages on the surface of the sample, as similarly discussed in [123]. Unfortunately the surface damage is directly translated into doping passivation of the n-side of the membrane, since for our devices a very thin layer of highly n-doped InP lies on the top of the PhC membrane. The explanation of effective low doping due to surface damage fits quite well with the high electrical resistances. Even though the PL method for surface diagnostic is only qualitative, we believe that adding a protecting layer in the fabrication process solved the electrical characterization issue as shown below for the 3rd and the 4th generation of devices.

For the 3rd generation of devices the electrical and optical characterizations are shown in Figure 4.8. The measurements in Figure 4.8(a) and (b) are correlated, in the sense that while acquiring the optical spectra, the voltage was recorded and that is why the experimental curves do not start from zero. From Figure 4.8 the high voltage issue of the 2nd generation seems to be solved. The components have 99 pitch cavity length (corresponding to 45.144 µm). Devices d12wg, d14op and d15wg show a voltage threshold between 1 V and 2 V, while device c11wg needs a higher voltage. From the measurements we observe that the devices are not not sensitive to illumination for being turned on, as for the 2nd generation of devices. The electrical resistances that can be derived from the voltage-current curves are ~9 kΩ, ~12 kΩ and ~26 kΩ for d12wg, d14op and d15wg respectively.

The trend among the mentioned devices can be due to the pillar widths. Device d12wg and d14op have a similar resistance value, sharing a wider pillar width, compared to d15wg, which has a bigger resistance and a thinner pillar. Although only qualitative results are described, we believe that the high voltage issue has been solved. The optical emission of device d15wg is shown in linear and logarithmic scale in Figure 4.8(c) and (d). Even for this batch of devices no PhC emission could be observed. We believe

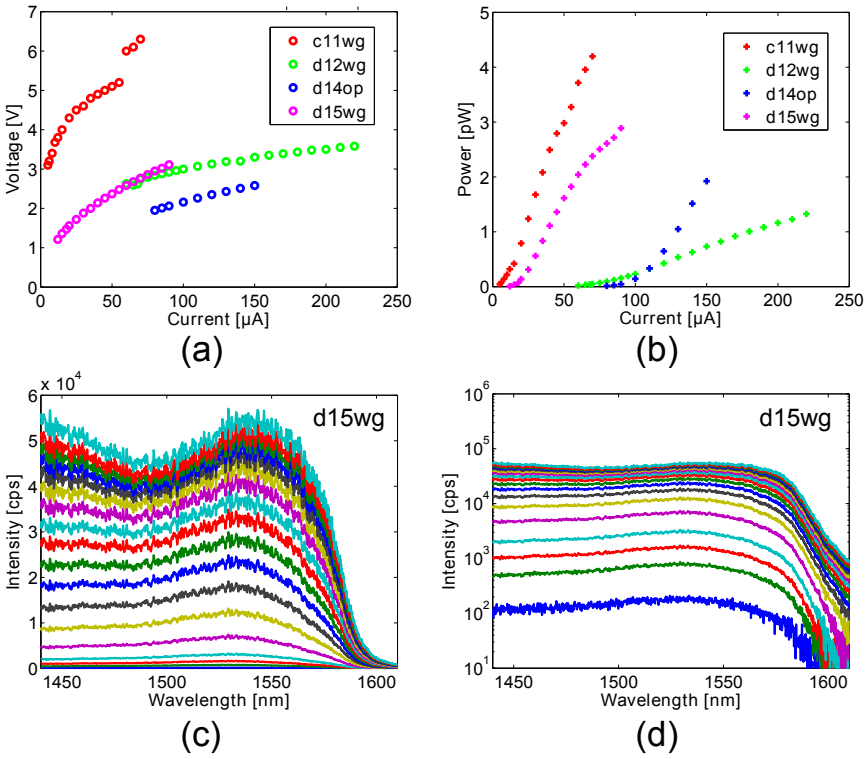


Figure 4.8: Characterization of devices of the 3rd generation. In (a) and (b) the measured values of voltage as a function of current and output power as a function of current for devices c11wg (red circles), d12wg (green circles), d14op (blue circles), and d15wg (magenta circles) for different sets of input current range. Device c11wg has 19 pitch cavity length, 110 nm hole radius, and ~170 nm pillar top width. The other devices have a 99 pitch cavity length. d14op has 110 nm hole radius and ~220 nm pillar top width. Device d12wg has ~220 nm pillar top width, while d15wg ~170 nm, and they both have a hole radius of 120 nm. In (c) and (d) the optical spectra in linear and logarithmic scale for device d15wg. The input current range is 12 µA-90 µA.

that the optical characterization of these devices did not succeed because of the final unlucky fabrication step, where most of the devices have been damaged from the air bubbles created by the BCB layer for the bonding step, as BCB could not stand the too high and wrong temperature in the annealing step.

The characterization of two devices of the 4th generation is shown in Figure 4.9. In this case the device yield for electrical injection has been very low and therefore the most two significant devices are described. The spectra of devices c14wg and c16wg are shown in Figure 4.9(a) and (b) in linear scale. These two devices have a long cavity of 99 pitch (45.144 µm). From the spectra we can observe that there is a resonant peak at ~1550 nm for c14wg and ~1530 nm for c16wg. Device c14wg has a wider pillar and a smaller PhC hole size, whereas device d16wg has a thinner pillar and a wider PhC hole size. The different resonant wavelengths can be explained with the combined action of both the different pillar top width and diverse PhC hole sizes, since a wider pillar should result in a red-shift in wavelength and a wider PhC hole in a blue-shift.
In Figure 4.9(c) a top-view image of device c14wg under electrical injection on the right and IR illumination on the left are presented. As expected the scattered light that can be seen from the top of the device comes from the transition regions between the PhC cavity and the mirrors. In Figure 4.9(d) the L-I-V curves for c14wg (red circles) and c16wg (blue crosses) are represented. From the voltage curve an electrical resistance of ~7 kΩ can be derived for both devices. The voltage threshold is higher for d14wg than c16wg. The electrical resistance value of the 4th generation is similar to the 3rd generation, confirming that the PE-ALD deposition solved the voltage issue described for the 2nd generation of devices. From the L-I curve in Figure 4.9(d) and the spectra in Figure 4.9(a) and (b), lasing action cannot be observed, since the whole optical spectrum increases with higher current levels and no gain clamping is seen. Although the devices are not lasing, the small peak that can be see from the optical spectra could be a sign of the PhC waveguide operating in slow-light regime, where spontaneous emission is enhanced.
We still believe that if the yield for this sample were higher, shorter devices could have been electrically pumped and could have been lasing. The issue of the current injection can be related to cleanroom processing, where a compromising step could have been the SiO_2-BCB planarization: if SiO_2 is not removed from the top of the pillars, it acts as insulator.

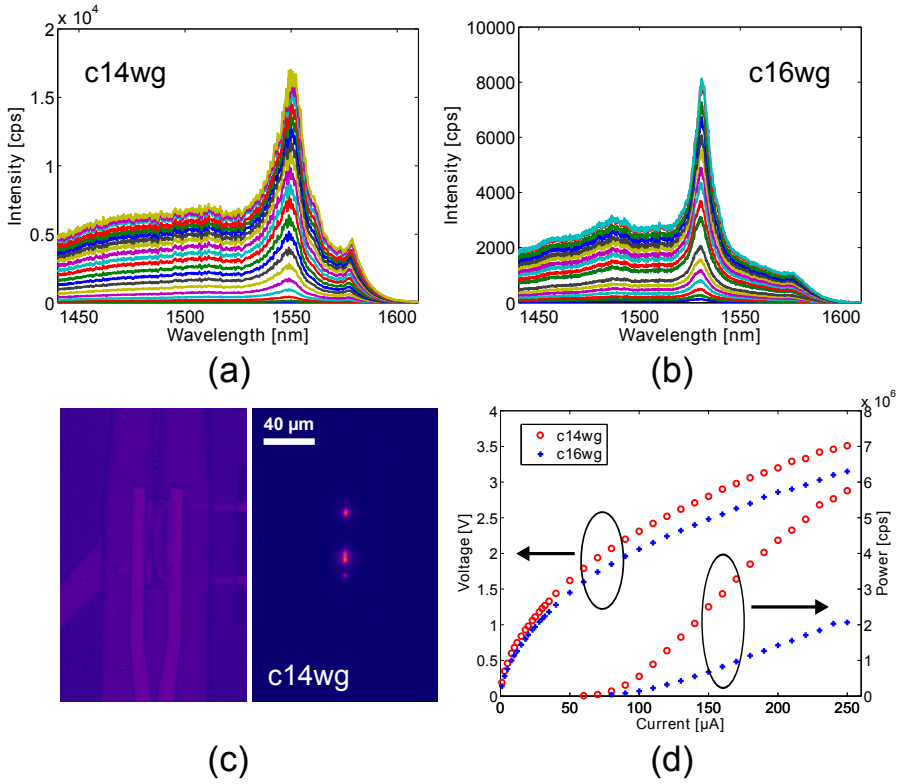


Figure 4.9: Characterization of devices of the 4$^{\text{th}}$ generation. In (a) and (b) optical spectra in linear scale of devices c14wg and d16wg that have 110 nm and 115 nm hole size in radius, and a pillar top width of ~220 nm and ~170 nm respectively. The input current range is 60 µA-250 µA. (c) Light top-emission under electrical injection on the right and IR illumination (940 nm GaAlAs/GaAs LED) on the left of device c14wg. (d) Measured values of voltage as a function of current and output power as a function of current for c14wg (red circles) and c16wg (blue crosses). The current sweep for the L-I curve is the same as the optical spectra, while for the V-I curve the range is 0 −250 µA.

4.5 Optically pumped lasers with vertical electrical injection design

4.5.1 Optical setup and lasing emission

The setup for the optical characterization under optical injection is presented in Figure 4.10. It is the same setup that has been employed for the optical characterization under electrical injection in Figure 4.4, besides the

optical pumping scheme. As shown in Figure 4.10 a pulsed pump diode at a wavelength of 980 nm is used to excite the PhC lasers. The pump pulse width is fixed at 500 ns and the duty cycle (t/T) of the pulse train is 5%. After passing through a tunable optical attenuator, the pump beam is focused on the sample through a microscope objective with a numerical aperture of 0.65. The spatial profile of the pump beam is monitored using an IR camera. The emission from the PhC sample is collected vertically using the same objective. After being isolated from the reflected pump beam by a longpass filter, the signal is sent to a grating mirror and analyzed using a highly sensitive spectrometer with a cooled array of low-noise InGaAs photodetectors.

The images of a device under IR illumination (left) and how the light emission from the top (right) look like are presented in Figure 4.11. The two represented devices have a different laser cavity length (Figure 4.11(a) 9 pitch cavity and Figure 4.11(b) 49 pitch cavity), but they show similar light emission with a major light spot in the middle of the PhC cavity and further scattered light at the edges of the mirrors. The observed laser emission is similar to 2D PhC membrane lasers without a vertical electrical injection path. The optical pumping characterization has been successful only for the components with a PhC design for top-emission inspection (without output WG), therefore the suffix "op" will be omitted in the name of the devices.

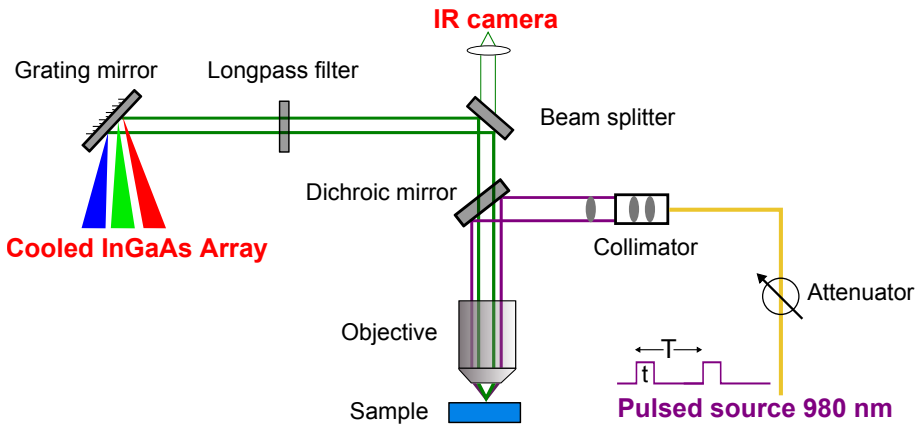


Figure 4.10: Schematic of the experimental setup used for optical characterization of PhC laser devices under optical injection. The cooled InGaAs array spectrometer operates at −100°C.

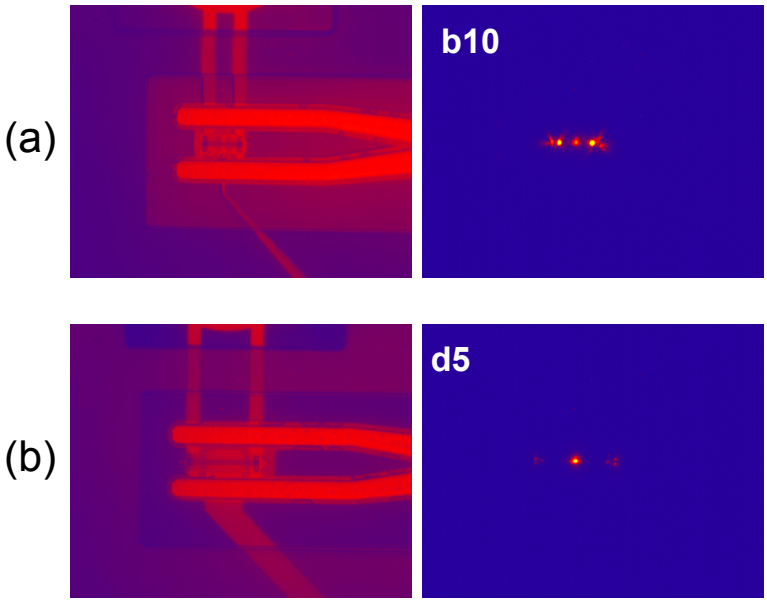


Figure 4.11: (a) 9 pitch cavity length laser (device b10). (b) 49 pitch cavity length laser (device d5). On the left side the IR image of the device, on the right side the laser emission under optical pumping of 10 mW and 9 mW peak power respectively.

4.5.2 Results and discussion

The optical measurements are presented in Figures 4.12 and 4.13 for devices with different cavity lengths and hole sizes.[6] Concerning the post for electrical injection, only devices with the thin top pillar width < 200 nm show lasing behaviours. The devices presented in this section have an optical design for out-of-plane emission (without output WG).
In Figure 4.12 all the devices have the same cavity length of 9 pitch and the hole size determines the lasing wavelength following a red-shift in wavelength for smaller hole sizes: in Figure 4.12(a) lasing is observed at ~1514 nm with 120 nm radius, in Figure 4.12(b) at ~1534 nm, with 115 nm radius and in Figure 4.12(c) at ~1544 nm with 110 nm radius. The input power thresholds are ~3.5 mW, ~3 mW and ~4 mW for Figure 4.12(a), (b), and (c) respectively. The power threshold are quite similar probably due to the same cavity length.
A similar red-shift behaviour of the lasing wavelength can also be observed

[6]The optical measurements have been acquired by Postdoc Weiqi Xue.

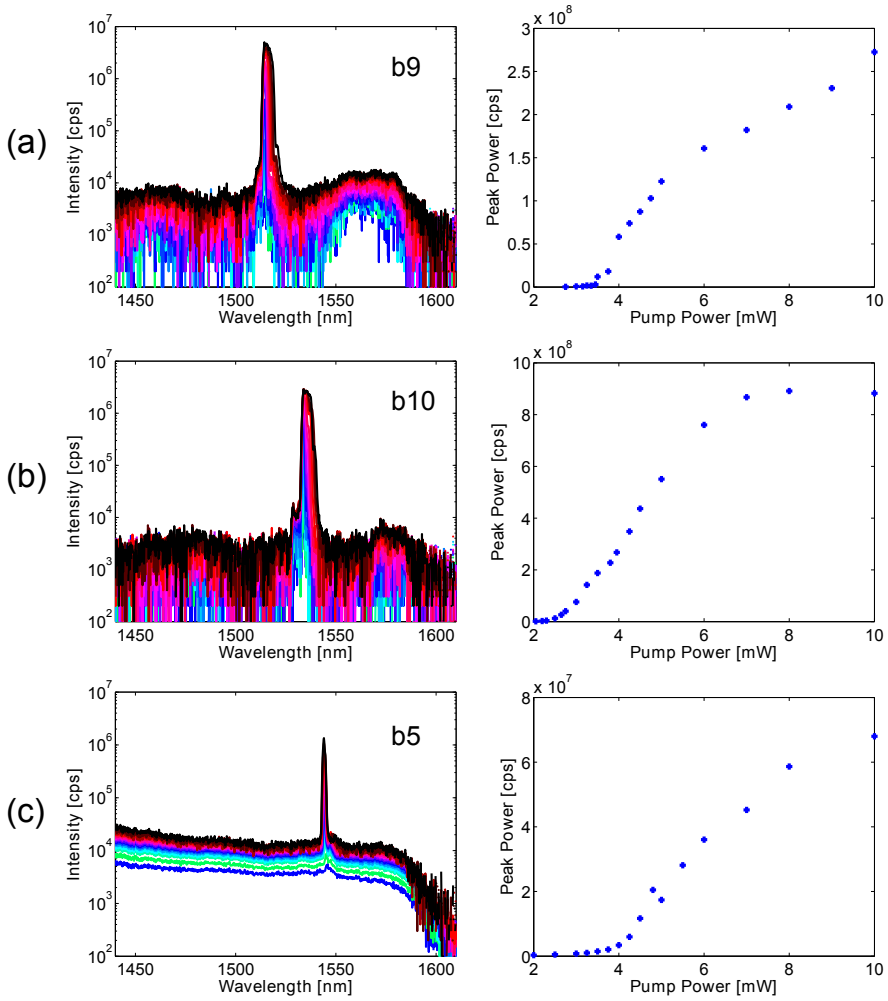


Figure 4.12: Lasing devices under optical pumping. On the left side optical spectra and on the right side output power as a function of input power. All the devices have 9 pitch cavity length. (a) Device b9 120 nm hole radius. (b) Device b10 115 nm hole radius. (c) Device b5 110 nm hole radius.

in Figure 4.13. Even though the devices in Figure 4.13(a) and (b) have a smaller cavity length of 49 pitch than the laser in (c) of 99 pitch, the bigger the hole radius, the smaller the lasing wavelength becomes. The laser emissions are at ~1531 nm with 115 nm radius, ~1547 nm with 110 nm radius and ~1509 nm with 120 nm radius for (a), (b) and (c) respectively. From the right part of Figure 4.13 the power thresholds can be derived.

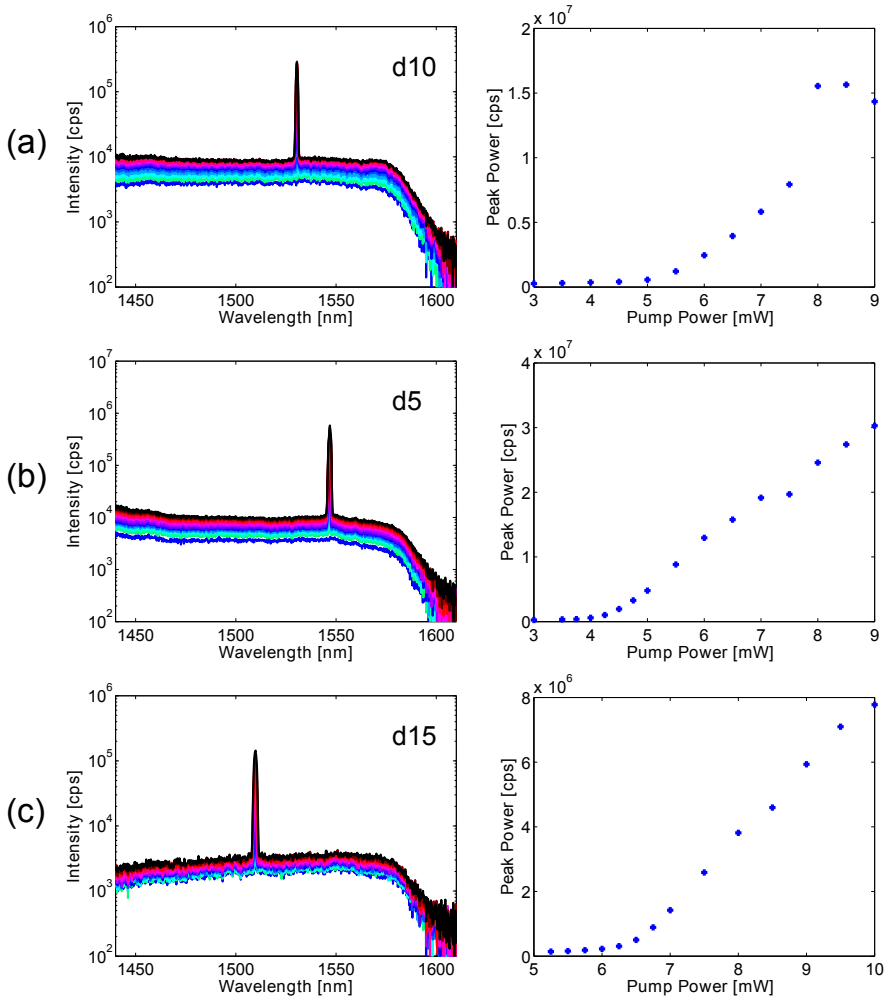


Figure 4.13: Lasing devices under optical pumping with long cavities. On the left side optical spectra and on the right side output power as a function of input power. Device d10 in (a) and d5 in (b) have 49 pitch cavity length. Device d15 in (c) has 99 pitch cavity length. (a) Device d10 115 nm hole radius. (b) Device d5 110 nm hole radius. (c) Device d15 120 nm hole radius.

The devices in Figure 4.13(a) and (b) have the same cavity length and their power threshold are ~5.5 mW and ~4.3 mW respectively. For the long 99 pitch device in Figure 4.13(c) a higher power threshold of ~6.5 mW is derived.

4.6 Summary

The fabricated devices have been successfully electrically and optically characterized. Although lasing through current injection at room temperature has not been observed, PhC light-emitting diodes have been demonstrated. The issue of high input voltage that was needed for the 2nd generation of devices processed with ZEP lithography was solved with a thin SiO_2 deposition with PE-ALD system previous the Si_3N_4 PECVD deposition as described in Chapter 3. This step was needed in order to prevent surface damage during the PECVD deposition (low RF frequency).
The new design of double heterostructure PhC nanolasers with a post for current injection under the membrane have been optically pumped. The optical characterization shows typical trends of PhC lasers according to cavity length and holes sizes. As the PhC hole radius increases, the lasing wavelength follows a blue-shift. Devices with different cavity lengths have been optically pumped showing a higher threshold power for longer devices. The optical emission has not been significantly altered by the presence of the vertical electrical injection path, provided that the pillar top width is smaller than 200 nm.
So far it has been demonstrated that the new design of double heterostructure PhC devices can lase on the developed platform of III-V semiconductors on Si under optical injection. However these results are promising for the electrical injection of the future generation of lasing devices.

Chapter 5

Nanobeam Light-Emitting devices

In this Chapter Photonic Crystal (PhC) nanobeam devices are described and characterized.

5.1 Nanobeam devices

Nanobeams are 1D PhCs which consists of a single row of holes. To create a cavity the main approaches consist of hole removal and holes tuning for high quality factor lasers. Hybrid nanobeam lasers have been reported for silicon photonics applications. However although the integration of III-V semiconductor on Si is demonstrated, these hybrid solutions are not yet mature for electrical injection [124].
We decided to include nanobeam devices during the fabrication of electrically pumped PhC lasers, since nanobeams with a vertical electrical injection scheme have been recently electrically pumped [125]. Inspired by these results that include nanobeam cavities and a pillar structure under the membrane for electrically injection, we adopted a similar technique for our samples. The possibility of including other designs and devices on our wafers relies on the fact that a good platform for optics and electronics integration on silicon has been established. Even though lasing of electrically injected nanobeams has been reported [125], we could not achieve this goal. A deeper optimization of the PhC design on our platform is required in order to obtain nanobeam lasers.

The fabrication process is the same as described in Chapter 3, apart from the final membranization step, which is not performed on nanobeams.

The PhC pattern is therefore embedded between air on the top and SiO_2 on the bottom of the InP membrane.

5.2 Nanobeam design

Two types of nanobeam cavities have been designed, similarly to [125]. They are presented in Figure 5.1. In the sketches of Figure 5.1 on the top a tilted-view and on the bottom a top-view with the design parameters are given, with further reference in Table 5.1. The first design is a "L3" type with 3 missing holes for the cavity and 18 holes in total is represented in Figure 5.1(a). The pillar for the vertical electrical injection stands under the L3 cavity and it is designed in the perpendicular direction compared to the nanobeam cavity. This laser is expected to have a low Q factor of ~500. For the second nanobeam presented in Figure 5.1(b) a "L0" cavity is chosen. In this case no holes are missing, but the cavity is defined by the size tuning of the 6 central holes. This type of nanobeam has a pillar that is located along the nanobeam membrane. This design is not expected to show lasing action, since the PhC pattern is perturbed by the pillar and no effective optical design calibration has been conducted. All the design parameters for the fabrication are listed in Table 5.1. For this type of component, the pillar size varies in width from 170 nm to 1 µm.

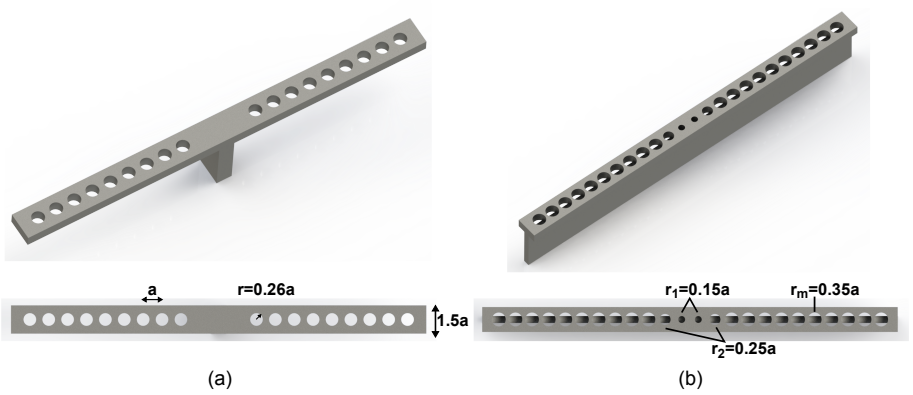


Figure 5.1: Sketch of L3 nanobeam device in (a) and L0 nanobeam device in (b). On the top a perspective view and on the bottom a top-view with the design parameters. The letter "a" stands for the pitch.

Table 5.1: Design parameters for the nanobeam devices.

Cavity type	L0	L3
Lattice constant(a) [nm]	480	480
Beam width	1.5a	1.5a
Total numbers of holes	24	18
Hole radius cavity	0.15a & 0.25a	/
Hole radius mirrors	0.35a	0.26a

5.3 Nanobeams characterization

5.3.1 Nanobeams with L0 cavity

The L0 cavity nanobeams have been inserted in the processing to test a new type of nanobeam design with a pillar for electrical injection. The optical design has not properly been calibrated for this platform and therefore it is not surprising that the optical spectra of a representative device presented in Figure 5.2(a) are very broad. In Figure 5.2(b) the output power and the voltage as a function of input current are depicted.

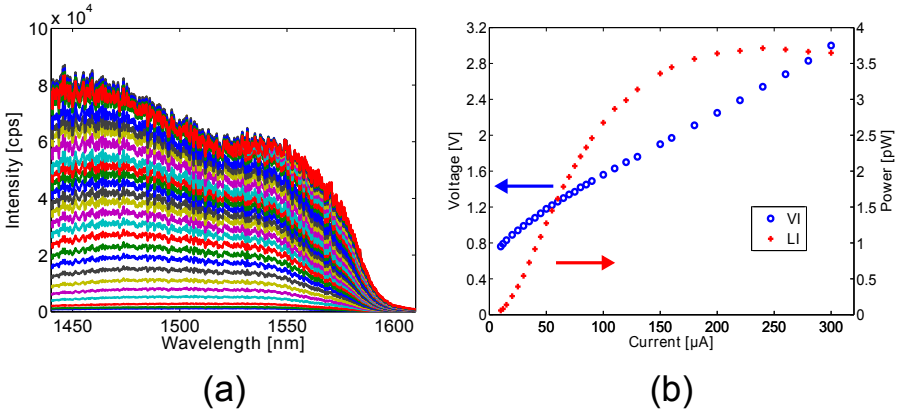


Figure 5.2: Characterization of a L0 nanobeam with a pillar width of 280 nm under current injection (3rd generation). (a) Optical spectra in linear scale. (b) Combined voltage-current-power VI (blue point) and LI (red cross) curves.

5.3.2 Nanobeams with L3 cavity

For the L3 cavity nanobeams no variation of the optical design has been introduced, but only a variation of different pillar widths. In Figure 5.3

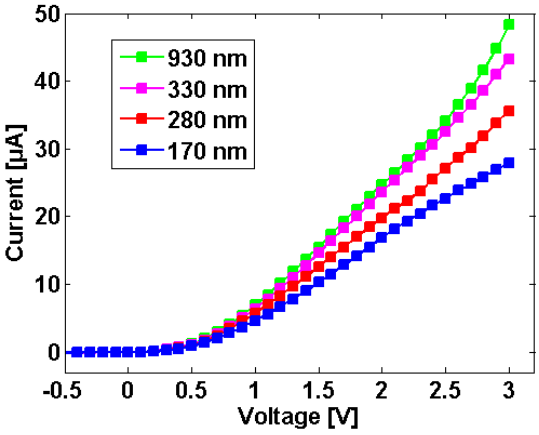


Figure 5.3: Current as a function of voltage for the 1st generation of L3 nanobeams. The legend gives the dimension of the top pillar width.

the voltage as a function of current is plotted for the first generation of nanobeams (PhCs processed with HSQ). The legend indicates the pillar top widths. The electrical resistance trend is evident: as the pillar width increases, the electrical resistance decreases. The resistance values calculated from the slope of the curves are in the tens of kΩ range. The wider 930 nm pillar has a resistance of ~55 kΩ and the thinnest 170 nm pillar has a resistance of ~80 kΩ. All the devices show a voltage threshold of ~0.7 V. The resistance trend described for the 1st generation of devices is still valid for the other generations with slightly different values depending on the fabrication process.

A nanobeam device belonging to the 3rd generation of devices is presented in Figure 5.4(a). Compared to the sketch of Figure 5.1 the pillar extends for a few µm at the sides of 1D PhC and this is due to the fact that we cannot precisely control the wet etch on this crystallographic direction (< 211 >). In Figure 5.4(b) a L3 nanobeam with output waveguide design is shown. This WG design has been added in a similar way as with the nanolaser design, although no investigation of the coupling parameters has been carried out. In Figure 5.4(b) on the bottom of the light emission from a nanobeam device (later characterized in Figure 5.5) is depicted. In Figure 5.4(b) on the top the same device is illuminated by the IR LED. The light spot is quite bright and centred in the middle of the cavity. The optical characterization of some nanobeam devices resulted in an optical spectrum that can resemble a PhC cavity, although no lasing has been observed. This

behaviour is presented in Figure 5.5(a) with a peak appearing at ~1549 nm. In Figure 5.5(b) the combined curves of voltage as a function of current (VI blue) and power as a function of current (LI red) are presented. From the VI curve an electrical resistance of ~26 kΩ can be estimated.

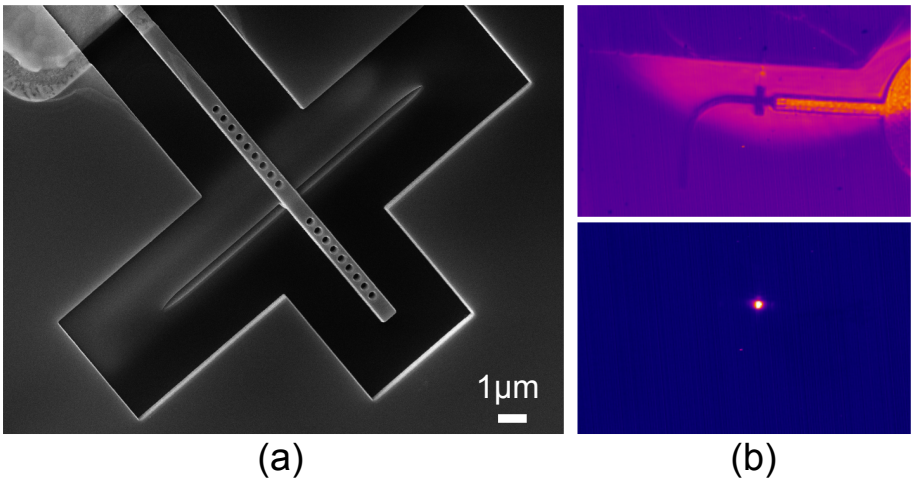


Figure 5.4: (a) SEM image of a L3 nanobeam in tilted view of the 3rd generation of devices. (b) On the top a L3 nanobeam with output WG illuminated by IR LED, on the bottom the device emission at 40 µAinputcurrent. This device is characterized in Figure 5.5.

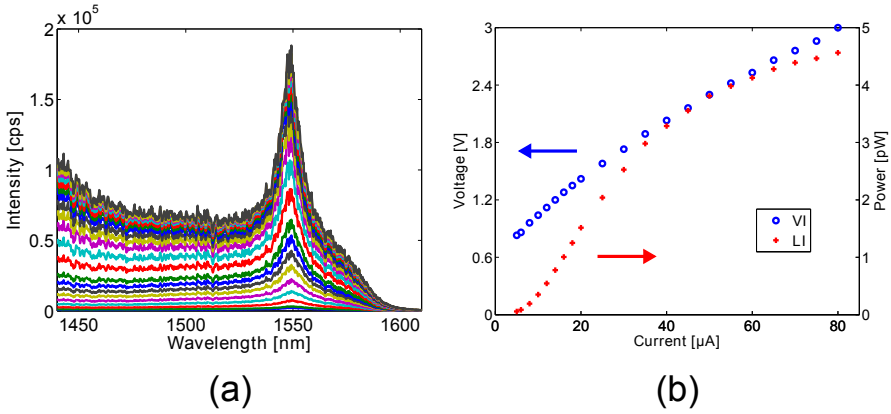


Figure 5.5: Characterization of a L3 nanobeam with a pillar width of 170 nm under current injection and output waveguide design (3rd generation). (a) Optical spectra in linear scale. (b) Combined voltage-current-power VI (blue circles) and LI (red crosses) curves.

5.4 Summary

The design and characterization of 1D photonic crystal nanobeam devices has been carried out. L0 cavity nanobeams only show a light-emitting behaviour, and therefore a more accurate optical design should be implemented, taking into account the presence and the direction of the pillar for electrical injection. The L3 cavity nanobeams do not show lasing emission, although a PhC cavity behaviour was observed under electrical injection. With this result we believe that with further optimization of the optical and electrical parameters for L3 nanobeams, lasing under current injection can be achieved.

Chapter 6

Conclusions and Outlook

6.1 Conclusion

The main result of the thesis has been the establishment of a new III-V platform on silicon with double-side processing for the fabrication of vertically electrically pumped double heterostructure Photonic Crystal (PhC) light-emitting diodes.

The results from the conducted theoretical modeling of devices with different current injection schemes (vertical of lateral) and active material extension (extended QWs or buried heterostructure (BH)) show that the localization of the active material as BH decreases the laser threshold and gives a confined path for the electron-hole recombination in the cavity with negligible leakage current issues. However the pillar for the vertical electrical pumping is also a powerful mean for efficient carrier injection into the laser cavity, since it directly supplies holes into the cavity, where electron-hole recombination takes place. According to the results the combination that best fits the aim of a low-threshold energy efficient laser consists of a device with a BH in a vertical injection scheme configuration. The thermal simulations also confirm a similar trend among the modeled devices and prove that devices with a vertical injection scheme can dissipate heat in a more efficient way than the laterally injected ones, as the pillar provides an extra path for the heat removal, besides the membrane.

For the optical design of the PhC devices a double heterostructure photonic crystal cavity approach with a line-defect waveguide and an elongated lattice constant for the laser cavity compared to the mirrors has been pursued.

The establishment of a new platform of III-V semiconductors bonded to

silicon has been challenging and difficult to achieve. A complicated clean-room process for PhC devices with a vertical electrical injection path has been developed with the optimization of the most critical steps. The pillar profile for current injection has been investigated according to the dry and and wet etching steps. A successful way of mutual SiO_2-BCB planarization with approximately the same etch rate has been found. The double-side processing has been examined with focus on the adhesive BCB bonding. The misalignment between the pillar and the photonic crystal pattern has been solved with the employment of chip-mark alignment for the second electron beam exposure, in order to compensate for the random sample distortion after the bonding step.

The fabricated devices have been successfully electrically and optically characterized. Although lasing through current injection at room temperature has not been observed, spectra from light emission have been reported. The issue of high input voltage that was needed for the 2^{nd} generation of devices processed with ZEP lithography for the PhC pattern was solved with a thin SiO_2 deposition with a plasma enhanced atomic layer deposition (PE-ALD) system previous the Si_3N_4 plasma enhanced chemical vapor deposition (PECVD), in order to prevent surface damage during this step.
The double heterostructure PhC nanolasers with a post for current injection under the membrane have been optically pumped. The optical characterization showed typical trends of PhC lasers according to cavity length and hole sizes, with lasing peaks close to 1550 nm, as it was designed. Furthermore the optical emission from the photonic crystals has not been significantly altered by the presence of the vertical electrical injection path, provided that the pillar top width is smaller than 200 nm.

In the end the introduction and fabrication of other devices together with the designed double heterostructure PhC lasers such as nanobeam light-emitting devices demonstrate the possibility of diverse electro-optical device integration on the new established platform.

6.2 Outlook

For the realization of the future generation of electrically pumped photonic crystal nanolasers several options can be pursued.
For a better optical characterization of the PhC devices the chip should be cleaved in order to get the in-plane emission from the devices and not only the top one. Therefore an accurate cleaving technique for example through

laser cutting should be investigated. Due to the BCB bonding of the III-V wafer to silicon and the small size of the devices, the standard approach of scribing and manual cleaving of the sample has not been implemented. If cleaving is successful a further optimization of the output waveguide design for light-coupling into an optical fiber has to be considered.
For a more advanced fabrication process the realization of a BH design is expected to improve the laser performance and help for the reduction of thermal issues and for improvement of carrier confinement, even though this approach must rely on perfect regrowth and perfect e-beam alignment techniques. The BH design is currently under development at DTU Fotonik with the butt-joint regrowth strategy.
In this new platform for III-V semiconductors on silicon the fabrication of photonic integrated circuits is the future for electronics and optics integration as the evolution of Integrated Circuit (IC) with CMOS technology.

6.2.1 Silicon processing

Another perspective for integration consists in the opportunity of utilizing the Si substrate as active part of the devices. The developed fabrication process relies on the double-side processing through adhesive bonding. In this case the Si wafer acts as a passive component. However if the pillar side can be processed on the Si wafer, better electrical (mobility comparison) and thermal properties (thermal conductivity of Si $130\,\mathrm{Wm^{-1}K^{-1}}$ is almost twice of InP $68\,\mathrm{Wm^{-1}K^{-1}}$ [93]) can be achieved. Unfortunately one of the biggest challenge is direct bonding, not only because of its intrinsic grade of difficulty (grade of roughness, amount of particles), but also because this step has to guarantee electrical injection from one to the other bonded side: from Si to the InP membrane. Another advantage of the vertical electrical injection structure is the possibility of exploiting the pillar as an output waveguide path, if a specific hybrid optical design with a silicon pillar and III-V photonic crystals can be implemented.

Appendix A

Parameters for the simulations

In this appendix all the parameters used for the simulations with Lastip [84] software are listed. The software version is CROSSLIGHT LASTIP 2012.

A.1 Parameters for the electrical simulation

The parameters that are common to all the models are listed below:

- device cavity length 1 µm;
- mirror reflectivity 99.5%;
- background loss 500 1/m;
- beta factor 0.01.

The materials used for the computation are InP and quaternary InGaAsP compounds for the active regions of Q(1.65) for QWs and Q(1.30) for barriers. All the material macros are on InP substrate. In the macros of the materials in the PhC region the mobility has been reduced of 25%, as fill fraction reduction.

In the following tables the material settings for the four models are listed: LBH in Table A.1, LU in Table A.2, VCP and VCP-BH in Table A.3. LU and LBH include an upper and lower air layer that is necessary for the simulation set-up. In the tables the layer lengths are not included and more size settings are depicted in Figure A.1.

Table A.1: Parameters for LBH model.

Material	Thickness	p-doping	n-doping	Comment
air	300 nm			
InP	80 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	
PQ(1.65)	7 nm			3× QWs
PQ(1.65)	11.5 nm			4× barriers
InP	80 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	
air	300 nm			

Table A.2: Parameters for LU model.

Material	Thickness	p-doping	n-doping	Comment
air	300 nm			
InP	80 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	
PQ(1.65)	7 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	3× QWs
PQ(1.65)	11.5 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	4× barriers
InP	80 nm	$2.5 \times 10^{19}\,\mathrm{cm}^{-3}$	$6.0 \times 10^{17}\,\mathrm{cm}^{-3}$	
air	300 nm			

Table A.3: Parameters for VCP and VCP-BH model.

Material	Thickness	p-doping	n-doping	Comment
InP	60 nm		$2.7 \times 10^{19}\,\mathrm{cm}^{-3}$	
InP	20 µm			
PQ(1.65)	7 nm			3× QWs
PQ(1.65)	11.5 nm			4× barriers
InP	80 nm			
InP	1 µm	$1.5 \times 10^{18}\,\mathrm{cm}^{-3}$		pillar

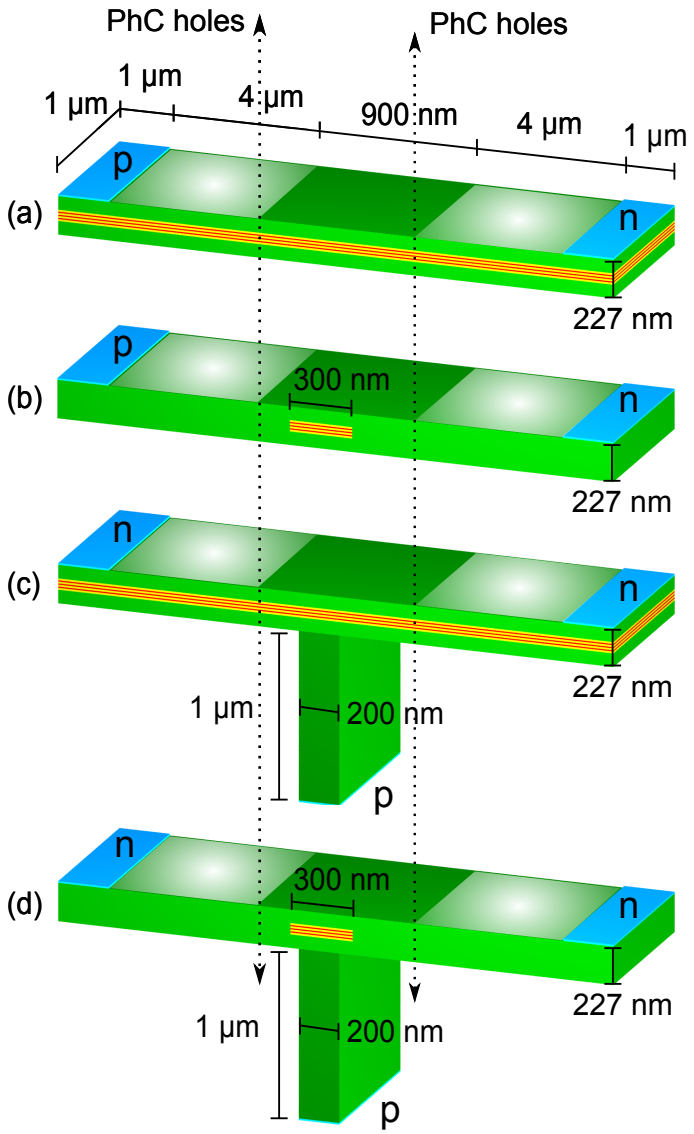


Figure A.1: Models for electrical and thermal simulations. (a) LU, (b) LBH, (c) VCP, and (d) VCP-BH. The color legend is: green for InP, red for QWs, yellow for barriers, and light-blue for the metal contacts. On the devices p and n indicate the type and localization of the contacts.

As shown in Figure A.1 the total device width is 10.9 µm, with the contacts regions of 1 µm and a middle region of the membrane of 900 nm that is undoped for the laterally injected components. In the PhC regions

the mobility of the materials is reduced of 25%. For the VCP and VCP-BH models the region that extends from the pillar to the sides of the device under the membrane is defined as an air layer (air macro).
The optical mode is defined with Dirichlet conditions as a box with its center in the middle of the membrane, whose width is 1.5 µm for all the models. The mode-box height extends in the air layers for the LU and LBH. For the vertical injection schemes VCP and VCP-BH the mode-box height is the same as the membrane, but the center of the field is lowered of 100 nm into the pillar with respect to the center of the membrane.

A.2 Parameters for the thermal simulation

For the thermal simulations the material configurations are the same as listed in section A.1 with the following settings for the thermal model:

- The temperatures for the thermal simulations are 300 K, 350 K, 400 K with the use of the self-heating model and the including heat-flow option.
- The initial temperatures of 300 K, 350 K, 400 K are set on the metal contacts in order to reproduce the behaviour of the devices in different environmental conditions.
- The values of the thermal conductivities of the considered materials are: InP 68 $Wm^{-1}K^{-1}$, InGaAsP 5.2 $Wm^{-1}K^{-1}$ [92], and the contacts are assumed to be Au with 318 $Wm^{-1}K^{-1}$ [93].
- The thermal conductivity of the PhC region has been scaled with the filling factor (25%).

Appendix B

Process flow

This appendix contains all the steps for the fabrication of vertically electrically pumped Photonic Crystal (PhC) light-emitting devices presented in this work. All the process steps apart from one (PE-ALD deposition at NanoLab Lund, Sweden) have been performed at Danchip cleanroom using the facilities available during the time of this Ph.D. project. All the recipes should be tested and adjusted in case of transfer to another machines.

B.1 Device fabrication

In the following pages all the fabrication steps are listed in the case of the epitaxy presented in Table 3.1 with two PQ QWs. If a different active material composition is used, the wet etch step of the membrane has to be modified accordingly.
The fabrication steps are divided into three sections. In the first part the fabrication of the p-side is presented until the bonding step. In the second and third parts the steps for the n-side are listed according to the PhC lithography with HSQ (second part) or ZEP (third part).
For the pillar e-beam lithography the orientation of the pillars has to be perpendicular to the major flat, as mentioned in Chapter 3.

1. Wafer preparation

Cleaning	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min; N2 blow dry
InP cap layer removal	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 μm/min

2. E-beam exposure

HSQ (Fox-15) coating ~330nm thickness	Pre-bake 220°C – 5 min HSQ spinning 7000 rpm, 4000 rpm/s – 60 s Bake 120°C – 2 min Post-bake 220°C – 2 min
E-beam exposure	Current 6 nA, Dose 3750 μC/cm^2 PEC (proximity error correction) with PSF (point spread function)
HSQ development	3 H2O : 1 AZ400K – 2.5 min; DI-water – 1 min; N2 blow dry

3. Pillar dry etch

RIE etch for ~1μm (protecting layers, contact layers and InP pillar)	RIE cyclic process CH4/H2 8.4/42 sccm, 80 mTorr, 60 W, 2.5 min - O2 50 sccm, 150 mTorr, 20 W, 1 min to remove polymer. Etch rate (InP) ~ 20 nm/min, etch rate (InGaAs) ~ 9 nm/min

4. Pillar wet etch

InP wet etch	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry

5. HSQ removal

HSQ mask wet etch	BHF – 1.5 min; DI-water – 1 min; N2 blow dry Etch rate ~400 nm/min

6. SiO2 deposition

Deposition of ~1.5 µm SiO2	PECVD SiH4/N2O 17/800 sccm, 400 mTorr, 380 W, 300°C Deposition rate ~180nm/min

7. BCB coating for planarization

BCB coating ~3.8 µm	Bake 200°C – 5 min AP3000 spinning program with 2 steps 500 rpm, 1000 rpm/s – 5 s 2000 rpm, 1500 rpm/s – 60 s Bake 160°C – 1 min BCB (Cyclotene 3022-46) spinning 2000 rpm, 4000 rpm/s – 60 s Post-bake 90°C – 6 min
BCB on 4" carrier ~5.5 µm	BCB (Cyclotene 3022-46) spinning 1000 rpm, 4000 rpm/s – 60 s Post-bake 90°C – 6 min
BCB curing	Curing in oven at 250°C for ~3 hours

8. SiO2 and BCB planarization

RIE SiO2-BCB etchback. The III-V wafer is on the top of the 4" silicon wafer with spun BCB	RIE CHF3/O2 16/4 sccm, 100 mTorr, 90 W Combined etch rate of both SiO2 and BCB ~50nm/min Laser interferometer monitor and dektak measurements until ~200nm of pillar is revelaed

9. P-metal UV lithography

Photoresist coating (negative resist) ~2.2 µm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min AZ2020 spinning 1800 rpm, 4000 rpm/s – 60 s Soft-bake 120°C – 1 min

UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 11 s
	Post-exposure-bake 120°C – 1 min
AZ2020 development	AZ726MIF – 1.5 min; DI-water – 2 min;
	N2 blow dry
Descum	O2 plasma asher, 0.2 mbar, 40 W, 30 s
RIE bombardment of protecting layers	RIE CH4/H2 8.4/42 sccm, 80 mTorr, 60 W – 1 min
Wet etch of protecting layers	1 HCl : 4 H3PO – 30 s; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 μm/min

10. P-metal contact

Metal evaporation	Ti/Pt/Au/Ti 30/50/250/20 nm
Lift-off	Acetone – 15 min in ultrasonic bath with low ultrasound activity; ethanol – 1min;
	DI-water – 2 min; N2 blow dry

11. III-V wafer cleave into 4 quarters

Resist coating ~1.5 μm	AZ5214 spinning 4000 rpm, 4000 rpm/s – 60 s
	Hard-bake 130°C – 2 min
Cleave	Wafer scribing and manual cleave into 4 quarters
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min;
	N2 blow dry
	O2 plasma asher, 0.2 mbar, 100 W, 10 min

12. Adhesive bonding of a quarter of III-V to 2" silicon wafer

III-V sample	Bake 160°C – 5 min
	AP3000 spinning program with 2 steps
	500 rpm, 1000 rpm/s – 5 s
	2000 rpm, 1500 rpm/s – 60 s

	Bake 160°C – 1 min
Si wafer	Bake 160°C – 5 min
	AP3000 spinning program with 2 steps
	500 rpm, 1000 rpm/s – 5 s
	2000 rpm, 1500 rpm/s – 60 s
	Bake 160°C – 1 min
BCB coating ~2.4 µm	BCB (Cyclotene 3022-46) spinning
	5000 rpm, 4000 rpm/s – 60 s
	Post-bake 90°C – 6 min
	The III-V sample is flipped and placed on the top center of the 2" silicon wafer
EVG bonder	Curing at 250°C for 1 hour with a piston force of 750 N, chamber pressure $1.6x10^{-3}$mbar
BCB residual removal	Plasma asher CF4/O2 50/350 sccm, 600 W, 1 mbar

13. InP substrate removal

Wet etch InP substrate removal (~350µm)	HCl etch with magnetic stirring. Etch for about 40 min. InP etch rate ~9 µm/min; DI-water – 2 min; N2 blow dry

14. InGaAs etch stop layer removal

Wet etch (InGaAs)	1 H2SO4 (10%) : 8 H2O2 (30%) : 80 H2O – 30 s; DI-water – 1 min; N2 blow dry. Etch rate ~ 0.5 µm/min

15. PL-mapping

PL-mapper	Laser sources 532 nm and 405 nm

From this step the processing is divided into 2 sections **a)** for the HSQ processing and **b)** ZEP processing of the photonic crystal pattern.

HSQ Process

16a. Reveal p-side UV lithography

Photoresist coating (positive resist) ~1.5 μm	Dehydration-bake 180°C – 5 min AZ5214 spinning 4000 rpm, 4000 rpm/s – 60 s Soft-bake 90°C – 90 s
UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 12 s
AZ5214 development	5 H2O : 1 AZ351B – 1 min; DI-water – 1 min; N2 blow dry Hard-bake 130°C – 2 min

Wet etch of membrane

InP wet etch	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 μm/min
PQ wet etch	1 H2SO4 (10%) : 8 H2O2 (30%) : 80 H2O – 1 min; DI-water – 1 min; N2 blow dry. Etch rate <0.5 μm/min
InP wet etch	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 μm/min
PQ wet etch	1 H2SO4 (10%) : 8 H2O2 (30%) : 80 H2O – 1 min; DI-water – 1 min; N2 blow dry. Etch rate <0.5 μm/min
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min; N2 blow dry O2 plasma asher, 0.2 mbar, 100 W, 10 min

17a. E-beam lithography for Photonic crystals

HSQ (Fox-15) coating ~330nm thickness	Pre-bake 220°C – 5 min HSQ spinning HSQ spinning 7000 rpm, 4000 rpm/s – 60 s Bake 120°C – 2 min Post-bake 220°C – 2 min
E-beam exposure	Current 60 nA and 6 nA, Dose 5000 μC/cm^2 2 exposures

	Global and Chip mark alignment, PEC (proximity error correction) with PSF (point spread function)
HSQ development	3 H2O : 1 AZ400K – 2.5 min; DI-water – 1 min; N2 blow dry

18a. Photonic crystal dry etch

RIE photonic crystal etch	RIE cyclic process CH4/H2 4.2/33.6 sccm, 80 mTorr, 60 W, 2.5 min - cyclic O2 45sccm, 150 mTorr, 20 W, 1 min to remove polymer Total etch time 50 min to achieve straight PhC sidewalls

19a. HSQ hard mask removal

Photoresist coating (positive resist) ~1.5 µm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min
	AZ5214 spinning 4000 rpm, 4000 rpm/s – 60 s
	Soft-bake 90°C – 90 s
	Hard-bake 130°C – 2 min
RIE etch	RIE O2 45 sccm, 100 mTorr, 50 W, ~5 min
	Etch rate AZ5214 ~230nm/min
Wet etch	BHF – 30 s; DI-water – 1 min; N2 blow dry
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min; N2 blow dry
	O2 plasma asher, 0.2 mbar, 100 W, 10 min

20a. N-metal UV lithography

Photoresist coating (negative resist) ~2.2 µm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min
	AZ2020 spinning 1800 rpm, 4000 rpm/s – 60 s
	Soft-bake 120°C – 1 min

UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 11 s
	Post-exposure-bake 120°C – 1 min
AZ2020 development	AZ726MIF – 1.5 min; DI-water – 2 min;
	N2 blow dry
Descum	O2 plasma asher, 0.2 mbar, 40 W, 30 s

21a. N-metal contact

Metal evaporation	Pd/Au 40/250 nm
Lift-off	Acetone – 15 min in ultrasonic bath with low ultrasound activity; ethanol – 1min;
	DI-water – 2 min; N2 blow dry
Annealing	RTA (rapid thermal annealing) 420°C – 5 s

22a. Membranization

Photoresist coating (positive resist) ~4.8 μm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min
	AZ4562 spinning 7000 rpm, 4000 rpm/s – 60 s
	Air – 5 min; Bake 100°C – 50 s
UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 18 s
AZ4562 development	4 H2O : 1 AZ351B – 1 min; DI-water – 2 min;
	N2 blow dry
	Hard-bake 130°C – 2 min
Descum	O2 plasma asher, 0.2 mbar, 40 W, 30 s
Wet etch	SiOetch – 8 min; DI-water – 1 min; N2 blow dry
	Etch rate SiO2 ~220 nm/min
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min;
	N2 blow dry
	O2 plasma asher, 0.2 mbar, 100 W, 10 min

ZEP Process

16b. Hard mask deposition

SiO2 PE-ALD deposition (Lund)	Fiji PE-ALD, 250°C, Bisdiethylaminosilane Oxygen Plasma Deposition of ~20 nm
Si3N4 deposition ~200 nm	PECVD SiH4/NH3/N2 30/20/1000 sccm, 500 mTorr, 80 W, 300°C. Deposition rate ~65nm/min

17b. Reveal p-side UV lithography

Photoresist coating (positive resist) ~1.5 µm	Dehydration-bake 180°C – 5 min AZ5214 spinning 4000 rpm, 4000 rpm/s – 60 s Soft-bake 90°C – 90 s
UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 12 s
AZ5214 development	5 H2O : 1 AZ351B – 1 min; DI-water – 1 min; N2 blow dry Hard-bake 130°C –2 min

Wet etch of membrane and hard mask layers

Si3N4 and SiO2 wet etch	BHF – 2.5 min; DI-water – 1 min; N2 blow dry
InP wet etch	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 µm/min
PQ wet etch	1 H2SO4 (10%) : 8 H2O2 (30%) : 80 H2O – 1 min; DI-water – 1 min; N2 blow dry. Etch rate <0.5 µm/min
InP wet etch	1 HCl : 4 H3PO – 1 min; DI-water – 1 min; N2 blow dry. Etch rate (InP) ~ 0.5 µm/min
PQ wet etch	1 H2SO4 (10%) : 8 H2O2 (30%) : 80 H2O – 1 min; DI-water – 1 min; N2 blow dry. Etch rate <0.5 µm/min
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min; N2 blow dry

	O2 plasma asher, 0.2 mbar, 100 W, 10 min

18b. E-beam lithography for Photonic crystals

ZEP (Zeon ZEP520A) coating ~500nm thickenss	Dehydration-bake 180°C – 5 min
	ZEP spinning program with 2 steps
	500 rpm, 200 rpm/s – 5 s;
	2600 rpm, 1500 rpm/s – 60 s
	Bake 160°C – 5 min
E-beam exposure	Current 0.8 nA, Dose 240 μC/cm^2
	Global and Chip mark alignment
ZEP development	ZED N50 – 2 min; isopropanol – 30 s; N2 blow dry

19b. Photonic crystal pattern transfer to hard mask

RIE dry etch	RIE CFH3/O2 16/2 sccm, 10 mTorr, 20 W
	Total etch time 16 min
ZEP strip	microposit® remover 1165 at 70°C in ultrasonic bath
	with low ultrasound activity – 2 hours;
	acetone – 5 min; isopropanol – 1 min; N2 blow dry

20b. Photonic crystal dry etch

RIE photonic crystal etch	RIE cyclic process CH4/H2 4.2/33.6 sccm, 80 mTorr, 60 W, 2.5 min - cyclic O2 45sccm, 150 mTorr, 20 W, 1 min to remove polymer. Total etch time 35 min to achieve straight PhC sidewalls. In the RIE chamber an InP wafer is introduced to have a constant load.

21b. N-metal UV lithography

Photoresist coating (negative resist) ~2.2 µm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min
	AZ2020 spinning 1800 rpm, 4000 rpm/s – 60 s
	Soft-bake 120°C – 1 min
UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 11 s
	Post-exposure-bake 120°C – 1 min
AZ2020 development	AZ726MIF – 1.5 min; DI-water – 2 min;
	N2 blow dry
Descum	O2 plasma asher, 0.2 mbar, 40 W, 30 s
Si3N4 and SiO2 wet etch	BHF – 2.5 min; DI-water – 1 min; N2 blow dry. Step needed to have the metal openings on the membrane

22b. N-metal contact

Metal evaporation	Pd/Au 40/250 nm
Lift-off	Acetone – 15 min in ultrasonic bath with low ultrasound activity; ethanol – 1min;
	DI-water – 2 min; N2 blow dry
Annealing	RTA (rapid thermal annealing) 420°C – 5 s

23b. Membranization

Photoresist coating (positive resist) ~4.8 µm	Dehydration-bake 180°C – 5 min; HMDS – 15 min; air 5 min
	AZ4562 spinning 7000 rpm, 4000 rpm/s – 60 s
	Air – 5 min; Bake 100°C – 50 s
UV exposure (365 nm)	Vacuum mode, 5mW/cm^2 – 18 s
AZ4562 development	4 H2O : 1 AZ351B – 1 min; DI-water – 2 min;
	N2 blow dry

	Hard-bake 130°C – 2 min
Descum	O2 plasma asher, 0.2 mbar, 40 W, 30 s
Wet etch	SiOetch – 8 min; DI-water – 1 min; N2 blow dry
	Etch rate SiO2 ~220 nm/min
Resist removal	Acetone – 5 min; ethanol – 1 min; DI-water – 1 min;
	N2 blow dry
	O2 plasma asher, 0.2 mbar, 100 W, 10 min

Acronyms

CMOS	Complementary Metal Oxide Semiconductor
PhC	Photonic Crystal
PBG	Photonic Band Gap
CW	Continuous Wave
WG	waveguide
TIR	total internal reflection
QW	Quantum Well
RT	room temperature
QD	Quantum Dot
BH	buried heterostructure
LCI	lateral current injection
VCI	vertical current injection
SEM	scanning electron microscope
MOVPE	metal-organic vapor-phase epitaxy
FEM	finite element method
WPE	wall-plug efficiency
BER	bit error rate
LED	light-emitting diode

PEC	proximity error correction
RIE	reactive ion etching
RF	radio frequency
MORIE	metal organic reactive ion etching
SEM	scanning electron microscope
HSQ	hydrogen silsesquioxane
PECVD	plasma enhanced chemical vapor deposition
BCB	benzocyclobutene
PL	photoluminescence
PE-ALD	plasma enhanced atomic layer deposition
IC	Integrated Circuit
SMU	Source Meter Unit

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