DTU Library

Burst mode control

Kovacevic, Milovan; Madsen, Mickey Pierre

Publication date:
2015

Document Version
Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

Citation (APA):
Kovacevic, M., & Madsen, M. P. (2015). Burst mode control. (Patent No. *WO2015128398*).

(54) Title: BURST MODE CONTROL

Fig. 1

(57) Abstract: The present invention relates to a new method of power converter regulation, in particular regulation of very high frequency (VHF) power converters operating at frequencies in the MHz range, wherein accurate output regulation utilises inherent delays in the regulation loop, whereby, contrary to hysteresis on/off control, the new method does not require immediate responses to comparisons of a sense voltage to two reference voltages; rather, according to the new method, only one reference voltage is used, and delays in the feedback loop are allowed to cause some variation of an output of the power converter.

WO 2015/128398 A1

BURST MODE CONTROL
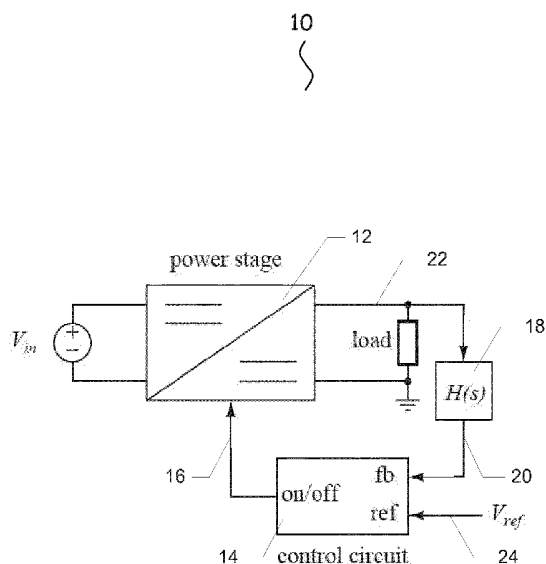
The present invention relates to a new method of power converter regulation, in particular regulation of very high frequency (VHF) power converters operating at frequencies in the MHz range.

5   BACKGROUND OF THE INVENTION

Reducing the physical size of electronic equipment in power applications is desired in order to add more features into existing products, integrate power converters in places normally unfit for such equipment, and reduce system cost. Increasing the operating frequency of the converter is a direct way of reducing the size of energy storage elements such as bulky
10   capacitors and inductors, which usually dominate the overall converter volume. Due to reduction in energy storage requirements the transient response is dramatically increased. LED lighting applications and point-of-load (PoL) converters particularly benefit from very high frequency (VHF) converters due to size, price, and weight reduction, and faster transient response.

15   Conventionally, burst mode control is used to control the output voltage or current of resonant power converters. Burst mode control allows the converter designer to optimize resonant power converters for operation in one operating point. The output voltage or current is controlled by turning the resonant power converters on or off as necessary to maintain constant output voltage or current. A disadvantage of burst mode control is that
20   the EMI performance is the same or worse compared to hard switched converters at the same modulation frequency. Typically, the modulation frequency ranges from 20 kHz to 1 Mhz.

Typically, prior art burst mode control is either hysteresis based, or pulse width modulation (PWM) based with constant switching frequency.

25   With hysteresis and PWM control, fast responses – ideally zero time delays - of the components of the regulation loop are required so that low cost components cannot be used.

The converter start-up circuit must also provide very little delay. As a consequence, passive start-up circuits (which have lower cost) are usually not an option.

30   Hysteresis based control results in tight output regulation, but requires a high cost, high performance comparator with very small propagation delays.

A conventional hysteretic burst mode control method of controlling a power converter, comprises the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a first reference voltage, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to an absolute value of a second reference voltage that is larger than the absolute value of the first reference voltage.

Typically, the difference between the first and second reference voltages is a predetermined fixed value.

SUMMARY OF THE INVENTION

The present invention provides a modulation method for obtaining accurate output regulation of a power converter while exploiting inherent delays in the feedback loop. Contrary to hysteresis on/off control, i.e. hysteretic burst mode control, the new method does not require immediate responses to comparisons of a sense voltage to two reference voltages. Rather, according to the new method, only one reference voltage is used, and delays in the feedback loop are allowed to cause some variation of an output of the power converter. The variation can be predicted and accounted for during the converter design process.

Thus, a new method of controlling a power converter is provided, comprising the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

In the following, the new method is termed phase-shift burst mode control due to the phase shift caused by the first and second time periods. According to the new method, hysteresis is provided in the time domain.

A power converter operating in accordance with the new method is also provided.

Thus, a new power converter is provided, comprising a control circuit coupled to compare a sense voltage with a reference voltage, and having a control output that is coupled to control turn-on and turn-off of the power converter in such a way that

the power converter is turned-on when the absolute value of the sense voltage is less than or equal to the absolute value of the reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

the power converter is turned-off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

The first time period may include a third time period of a predetermined duration that has to elapse from the point in time when the absolute value of the sense voltage drops below the absolute value of the reference voltage until the power converter is turned-on.

The second time period may include a fourth time period of a predetermined duration that has to elapse from the point in time when the absolute value of the sense voltage raises above the absolute value of the reference voltage until the power converter is turned-off.

The predetermined durations of the third and fourth time periods may be different.

Throughout the following disclosure, the process of alternatingly turning a power converter on and off, is termed "modulation" of the power converter, and the time between two consecutive turn-on events is termed a "modulation period", and the rate of turn-on is termed the "modulation frequency".

The sense voltage may correspond to an output voltage of the power converter; or an output current of the power converter; or another desired characteristic of the power converter.

An output current of the power converter is a current consumed by a load connected to an output of the power converter.

The control circuit may perform turn-off of the power converter by turning at least one switch of the power converter off, e.g. by short-circuiting the gate of a Field-Effect-Transistor (FET) to its source; or, the base of a bipolar transistor to its emitter, and turn-on of the power converter by allowing the at least one switch of the power converter to turn-on again, e.g. by opening the short-circuit.

The control circuit may also perform turn-on and turn-off of a resonant power converter by changing the impedance or the loop-gain of the resonant part of the power circuit, whereby the resonant power converter is turned-off by changing the impedance or loop-gain to a first value at which the resonant part of the power circuit does not oscillate, and whereby the resonant power converter is turned-on by changing the impedance or loop-gain to a second value at which the resonant part of the power circuit oscillates.

The control circuit may comprise one or more delays configured to provide at least part of one or more of the respective first and second time periods. Propagation delays in circuit components, such as propagation delays in a comparator, filtering elements, the power circuit, etc., may advantageously be incorporated into the appropriate time period.

The control circuit may comprise a comparator coupled to compare the sense voltage with the reference voltage, and an output of the comparator may constitute the control output that is coupled to control turn-on and turn-off of the power converter, and thus, the delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), constitute part of the respective first and second time periods.

The delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), may provide at least part of the third and fourth time periods.

The output voltage of the power converter may be coupled to signal conditioning circuit, such as a low-pass filter, etc., configured to output the sense voltage.

The power converter may be of any known type of power converters, and in particular any type of VHF power converters, such as square wave power converters, quasi-square wave power converters, resonant transition power converters, resonant power converters, etc.

The power converter may have a plurality of power circuits operating in series and/or in parallel and/or interleaved, e.g. with inputs in series and/or parallel and/or with outputs in series and/or parallel. All or some of the plurality of power circuits may be controlled with a single control circuit.

A resonant power converter may be of any known type of resonant power converters, such as converters comprising: a class E inverter and a class E rectifier, a class DE inverter and a class DE rectifier, a class DE inverter and a class E rectifier, etc.; or, class EF2 (or class Φ) converters, resonant Single-Ended Primary-Inductor Converters (SEPIC), etc.

The power converter may be driven by an oscillator, or the converter may be self-oscillating. Further, the power converter may be interleaved.

Basing control of the output of the power converter on a single reference voltage and time periods during which the power converter does not change state from a turned-on state to a turned-off state, or vice-versa, leads to lowered performance requirements for control circuit components as compared to components of conventional control circuits, e.g. utilizing PWM-control or hysteresis control. E.g., low cost components and passive start-up circuits may be used in the new control circuit.

Furthermore, it is possible to include low-pass filtering, or other signal conditioning, of the output voltage for provision of the sense voltage, thus improving signal integrity.

Increasing at least one of the first and second time periods provided by the control circuit lowers modulation frequency of the control output signal controlling the on/off states of the

power converter. This in turn increases variation of the output voltage; however, output voltage variations may be lowered by provision of a suitable output filter at the output of the power converter.

Due to the time periods provided by the control circuit, the response time of the control circuit is longer than the response time of hysteresis control. Still, desired regulation is achieved within one modulation cycle.

Conventional control circuits, such as PWM-control or hysteresis control, rely on high-end components and on minimizing time delays in the control circuit, leading to higher cost and lower component availability than for the corresponding components of the new control circuit.

For example, a comparator used in the new control circuit may be 9-10 times slower than a comparator used in a conventional control circuit, e.g. 4.5 ns vs 40 ns.

As further explained below, at least one of, or both of, the first and second time periods may be equal to, or substantially equal to, one fourth the modulation period, e.g. at 50 % duty cycle, for example at least one of, or both of, the third and fourth time periods may be equal to, or substantially equal to, one fourth the modulation period, e.g. at 50 % duty cycle.

The sense voltage may be a function of the output voltage supplied to a load connected to an output of the power converter; or, the sense voltage may be a function of the output current supplied to a load connected to an output of the power converter; or, the sense voltage may be a function of power, i.e. output voltage times output current, supplied to a load connected to an output of the power converter; etc.

An output capacitor connected to an output of the power converter stabilizes the output voltage supplied by the power converter. The output capacitor is charged during turn-on of the power converter and discharged during turn-off of the power converter. During turn-on, the capacitor is charged with the current supplied by the power stage of the power converter minus the current supplied to the load connected to the output of the power converter. During turn-off, the capacitor is discharged with the load current. Thus, the slope of the voltage ripple ΔV_{out} developed across the output capacitor as a result of the charging and discharging of the output capacitor depends on the output current. If the output current is low, the slope of the voltage ripple is steep during turn-on of the power converter and low during turn-off of the power converter, and vice versa if the output current is high. This together with the first and second time periods causes the output voltage ripple to vary with varying output current and also causes the mean value of the output voltage V_{out} to vary with varying output current. Correspondingly, the ripple of the output current I_{out} and

output power P_{out}, and the mean value of output power P_{out} may also vary with varying output current.

This variation may be compensated in various ways in order to lower the amount of variation and making the desired output value more constant and independent of the output current at least within a predetermined output current range.

For example, the control circuit may be configured to compensate a dependence of the sense voltage, and thereby a dependence of the output voltage; or, the output current; or the output power; etc., on the output current, for example by varying the reference voltage in dependence on the output current in such a way that the dependence of the sense voltage on the output current is compensated. For example, an increase in output voltage may be compensated by lowering the reference voltage so that the power converter is turned-on at a lower voltage thereby lowering the resulting output voltage. The change in reference voltage takes place over a plurality of modulation periods. When the load is constant, the reference voltage does not change unless an adjustment of the output, such as the output voltage or current, is performed.

Additionally; or, alternatively, the control circuit may be configured to vary at least one of the first and second time periods in dependence of the output current, whereby the dependence of the sense voltage on the output current is compensated. For example, an increase in output voltage may be compensated by lowering the second time period so that the power converter is turned-on during a shorter time period thereby lowering the resulting output voltage. When the load is constant, the first and second time periods do not change.

BRIEF DESCRIPTION OF THE DRAWINGS

Below, the new method and the new power converter are explained in more detail with reference to the drawings in which various resonant examples of the new power converter are shown. In the drawings:

Fig. 1   shows a schematic diagram of a resonant power converter with the new control circuit,

Fig. 2   shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 3   shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 4   shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 5   shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 6   shows exemplary signal conditioning circuits,

Fig. 7   shows exemplary switch drivers,

Fig. 8   shows a schematic circuit diagram of an exemplary new resonant power converter
          with a stop circuit,

Fig. 9   shows a switch driver with oscillator turn-off,

Fig. 10   shows a power circuit diagram of a VHF interleaved self-oscillating resonant SEPIC
          converter,

Fig. 11   is a plot of simulated waveforms of the power circuit shown in Fig. 10,

Fig. 12   shows a schematic circuit diagram of a model of a new resonant power converter
          used for calculation of component values,

Fig. 13   shows a circuit diagram of a control circuit used to control the power circuit shown
          in Fig. 10,

Fig. 14   is a plot of characteristic waveforms of the model shown in Fig. 12,

Fig. 15   is a plot of experimental waveforms of the control circuit shown in Fig. 13,

Fig. 16   is a plot of experimental waveforms of the power circuit shown in Fig. 10,

Fig. 17   (a) shows a plot of converter efficiency as a function of output power and (b) shows
          a plot of output voltage offset as a function of the load,

Fig. 18   is a flowchart of the new method,

Fig. 19   shows (a) a schematic circuit diagram of a model of the new resonant power
          converter together with (b) a conventional hysteretic control circuit and (c) a
          phase-shift burst mode control circuit,

Fig. 20   shows a plot of simulated waveforms of the model converter current and voltages
          controlled by the hysteretic control circuit,

Fig. 21   shows a plot of simulated waveforms of the model converter current and voltages
          controlled by the phase-shift burst mode control circuit, and

Fig. 22   shows schematic circuit diagrams of control circuits with varying sense voltage.

DETAILED DESCRIPTION OF EMBODIMENTS

The accompanying drawings are schematic and simplified for clarity, and they merely show
details which are essential to the understanding of the new resonant power converter, while
other details have been left out. The new resonant power converter according to the
appended claims may be embodied in different forms not shown in the accompanying
drawings and should not be construed as limited to the examples set forth herein.

Like reference numerals refer to like elements throughout. Like elements may, thus, not be described in detail with respect to the description of each figure.

Fig. 1 shows a schematic block diagram of a resonant power converter 10 controlled in accordance with the new method. The illustrated resonant power converter 10 comprises a
5   VHF power circuit 12, a control circuit 14 with a control output 16, and a signal conditioning circuit 18 providing a sense voltage 20 based on and corresponding to the output voltage 22.

The control circuit 14 is coupled to compare the sense voltage 20 with a reference voltage 24.

10   Alternatively, the sense voltage 20 may be provided by a current sensor, such as a resistor, a hall element, etc., coupled so that the sense voltage corresponds to an output current of the resonant power converter 10.

The control circuit 14 has a control output 16 that is coupled to control turn-on and turn-off of the VHF power circuit 12 of the resonant power converter.

15   In the illustrated examples, the output voltage and the sense voltage have positive values, so that the absolute value of the sense voltage or the output voltage is equal to the value itself.

The VHF power circuit 12 of the resonant power converter 10 is turned-on when the sense voltage 20 is less than or equal to the reference voltage 24 and a first time period has
20   elapsed since a previous turn-off of the VHF power circuit 12. The VHF power circuit 12 of the resonant power converter 10 is turned-off when the sense voltage 20 is larger than or equal to the reference voltage 24 and a second time period has elapsed since a previous turn-on of the VHF power circuit 12.

The VHF power circuit 12 may be of any known resonant power converter topology with a
25   frequency of operation in the MHz range, such as at or above 20 MHz, such as at or above 30 MHz, such as in the 30 MHz – 300 MHz range, such as converters comprising: a class E inverter and a class E rectifier, a class DE inverter and a class DE rectifier, a class DE inverter and a class E rectifier, etc.; or, class EF2 (or class Φ) converters, resonant SEPIC converters, etc.

30   The resonant power converter may be driven by an oscillator, or the converter may be self-oscillating. Further, the resonant power converter may be interleaved.

Inherent signal propagation delays of the components of the control circuit 14 forms parts of the first and second time periods, and the inherent signal propagation delays may form the entire first and second time periods. Additionally, one or more delay circuits may

provide part of the first time period and/or part of the second time period, namely part of the third time period and/or part of the fourth time period.

The control circuit 14 may comprise a comparator that is coupled to compare the sense voltage 20 with the reference voltage 24, and having a comparator output that is the

5   control output 16.

The delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), constitute part of the respective first and second time periods, namely part of the third time period and/or part of the fourth time period.

The signal conditioning circuit 18 may be a low-pass filter configured to output the sense

10   voltage.

The control output 16 may be coupled to control turn-off of at least one power switch (not shown) of the resonant power converter 10 thereby turning the resonant power converter off.

This is illustrated in the class E inverter based resonant power converters shown in Figs. 2

15   and 3. The only difference between the resonant power converter of Fig. 2 and the resonant power converter of Fig. 3 is that inductor L_3 of Fig. 2 has been substituted by rectifier D_1 in Fig. 3.

Alternatively, or additionally, the control output 16 may be coupled to control other parts of the resonant power converter circuit than the power switches, e.g. by enabling and

20   disabling energy transfer from the input to the output of the resonant power converter 10, e.g. by turning the resonant power converter on and off by changing the impedance or the loop-gain of the resonant part of the power circuit, whereby the resonant power converter is turned-off by changing the impedance to a first value at which the power circuit does not oscillate, and whereby the resonant power converter is turned-on by changing the

25   impedance to a second value at which the power circuit oscillates.

This is illustrated in Figs. 4 and 5 showing a class E inverter based resonant power converter similar to the class E inverter based resonant power converters shown in Fig. 3 except for the fact that the control output 16 turns S_2 on and off.

In Fig. 4, the resonant part of the resonant power converter 10 does not oscillate when

30   switch S_2 is turned-on, and the resonant part of the resonant power converter 10 oscillates and operates like the resonant power converter 10 of Fig. 3 when switch S_2 is turned-off.

In Fig. 5, the functions of rectifier D2 and switch S2 of Fig. 4 are combined in switch S2 functioning as a synchronous rectifier in Fig. 5 when the second self-oscillating gate driver is enabled so that the resonant power converter is turned on.

Fig. 6 shows circuit diagrams of two examples of low-pass filters that may constitute the signal conditioner 18.

The signal conditioners shown in Figs. 6 (a) and (b) may be substituted with any suitable signal conditioner chosen from other signal conditioner designs available to the person skilled in the art.

Examples of self-oscillating gate drivers are shown in Fig. 7.

In Fig. 7(a), a low enable signal keeps the gate of the power switch at zero voltage, whereby oscillation of the power circuit is inhibited, while a high enable signal allows propagation of the VHF oscillator signal driving the gate of the power switch causing the power circuit to oscillate.

In Fig. 7(b), a low enable signal switches switch transistor S_{aux} off and keeps the gate of the power switch at a constant voltage, whereby oscillation of the power circuit is inhibited, while a high enable signal allows propagation of the VHF oscillator signal driving the switch transistor S_{aux} on and off thereby driving the power switch on and off causing the power circuit to oscillate.

The gate drivers shown in Figs. 7 (a) and (b) may be substituted with any suitable gate driver chosen from other gate driver designs available to the person skilled in the art.

Fig. 8 shows a schematic circuit diagram of an exemplary new resonant power converter with a stop circuit,

Fig. 9 shows a switch driver with oscillator turn-off,

Fig. 10 is a circuit diagram of a power circuit 12 of an interleaved self-oscillating resonant SEPIC converter, wherein two power circuits 12a, 12b drive each other via capacitive coupling C_{X1} and C_{X2} between the switches S_1 and S_2 and operate in interleaved mode.

The power circuits are substantially identical, i.e.:

$$L_{I1} = L_{I2} = L_I$$

$$C_{I1} = C_{I2} = C_I$$

$$C_{X1} = C_{X2} = C_X$$

$$C_{S1} = C_{S2} = C_S$$

The values of the most important parasitic components of the semiconductor devices, namely diode junction capacitors and parasitic capacitors of the semiconductor switches, are included in determination of operating frequency of the resonant power converter. The

oscillation frequency f_S is determined mainly by the inductance L_I and the total capacitance seen from the drain when the rectifiers are shorted, $C_{DS,tot}$

$$f_s = \frac{1}{2\pi\sqrt{L_I C_{DS,tot}}}$$

where

$$C_{DS,tot} = C_I + C_{OSS} + C_S + C_X||C_{ISS}$$

$$C_{OSS} = C_{DS} + C_{DG}$$

$$C_{ISS} = C_{GS} + C_{DG}$$

Oscillations start once the gate voltages of the MOSFET switches S_1 and S_2 become slightly higher than the MOSFET threshold voltage. Simulated waveforms of the resonant power circuit of Fig. 10 are shown in Fig. 11. Ideally, respective waveforms of the two interleaved power converters are identical and shifted 180° with relation to each other.

If VHF ripple is neglected, the converter output can be modeled as a current source with the current value of I_0. When an on/off modulation is applied on the converter, the current supplied by the converter i_{conv} to C_{out} and the load may be approximately modeled as a current square wave:

$$i_{conv} = \begin{cases} I_0, & \text{when the converter is ON} \\ 0, & \text{when the converter is OFF} \end{cases}$$

Output current I_{out} is equal to average value of i_{conv} over one modulation cycle. The resulting current going into C_{out} is $i_{conv} - I_{out}$, which has no DC component in steady state. If parasitics of C_{out} are negligible, the resulting V_{out} voltage waveform is a triangular wave. Assuming that turn-on and turn-off delays are independent of the output voltage rate of change, the output voltage ripple is

$$\Delta V_{out} = \frac{I_{out}}{C_{out}} t_{D,on} + \frac{I_0 - I_{out}}{C_{out}} t_{D,off}$$

where $t_{D,on}$ is the fourth time period and $t_{D,off}$ is the third time period, i.e. $t_{D,on}$ and $t_{D,off}$ are the control loop turn-on and turn-off delays, respectively, from the sense voltage crossing the reference voltage and to turn-on or turn-off, respectively, of the power converter. If the control circuit's delays are constant, the equation shows that V_{out} is a linear function of I_{out}, and the longer delay defines $V_{out,max}$. In the special case of $t_{D,on}$ and $t_{D,off}$ being equal, V_{out} is independent of I_{out}. At any given load, the offset of V_{out}: $\Delta V_{out,off}$, and f_M are determined from the values of C_{out} and the delays $t_{D,on}$ and $t_{D,off}$ by:

$$\Delta V_{out,off} = \frac{\Delta V_{out}}{2} \frac{t_{D,on} - t_{D,off}}{t_{D,off} + t_{D,on}}$$

and

$$f_M = \frac{I_0}{C_{out} \, \Delta V_{out}} \frac{I_{out}}{I_0} \left(1 - \frac{I_{out}}{I_0}\right)$$

Modulation frequency is highest at 50% duty cycle, i.e. the power converter is turned on half the time:

$$f_{M,max} = \frac{1}{2 \left(t_{D,on} + t_{D,off}\right)}$$

I_0 is not known from values of circuit components. An approximate value of I_0 can be determined from Spice simulations. Once I_0 is obtained, the output filter and the feedback circuit need to be designed to provide a desired modulation frequency f_M at a specified load.

Fig. 12 shows a block diagram of such a low frequency model of a resonant power. The VHF power circuit 12 is modelled as an on-off controllable DC current source.

The conditioning circuit 18 at the input of the control circuit 14, see Fig. 13, has a simple transfer function:

$$H(s) = \frac{A_{FB}}{1 + s\tau_{FB}}$$

Where

$$A_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$\tau_{FB} = \frac{R_{FB1}R_{FB2}}{R_{FB1} + R_{FB2}} C_{FB}$$

The comparator 26 of the control circuit 14 model is ideal; the propagation delay of the real comparator is added into the delay block. The delay block is represented by two different time delays, since the shutdown of the power circuit is significantly faster than the start-up sequence. This is because shutdown is performed by the auxiliary switches S_{aux1} and S_{aux2}, while during start-up C_{ISS} is passively charged from the bias voltage V_B through the biasing resistors.

Fig. 13 shows the control circuit 14. The sense voltage 20 is low-pass filtered in $H(s)$, a voltage divider/low pass filter 18 formed by R_{FB1}, R_{FB2}, and C_{FB}, and input to the comparator 26. The comparator output 16 turns the switches S_{aux1} and S_{aux2} on and off in response to

the voltage difference at the comparator inputs. When S_{aux1} and S_{aux2} are on, v_{GS1} and v_{GS2} are zero and the power circuit oscillations are inhibited. Once S_{aux1} and S_{aux2} are off, C_{ISS1} and C_{ISS2} are charged through R_{B1} and R_{B2}, whereby v_{GS1} and v_{GS2} start to increase from 0 to V_B. After the first time period, when v_{GS1} and v_{GS2} exceed the power MOSFET threshold

5   voltage V_{th}, switches S_1 and S_2 enter saturation and initiate oscillations in the power circuit. $H(s)$ has two primary purposes: to filter high frequency noise and adjust the feedback voltage level. It also contributes to propagation delay in the feedback loop.

In Fig. 14, characteristic voltage and current levels from a numerical example of the model are shown, where

10   • C_{out} = 3.3 μF

       • I_0 = 1.04 A, I_{out} = 0.52 A

       • R_{FB2} = 2 kΩ, R_{FB1} = 8.2 kΩ

       • C_{FB} = 220 pF

       • $t_{d,on}$ = 700 ns + 170 ns = 870 ns

15   • $t_{d,off}$ = 170 ns

The parameters are chosen to approximate the experimental setup described below. $v_{gate}(t)$ represents the gate voltages of S_1 and S_2 with removed VHF component. $V_{out}(t)$ passes through the single pole transfer function $H(s)$ and results in a distorted triangular waveform $v_{FB}(t)$. Average value of $v_{FB}(t)$ is slightly lower than the reference V_{ref} voltage, which is due

20   to $t_{d,on} > t_{d,off}$. This is also the cause of the duty cycle of the comparator output $v_{cmp}(t)$ to be lower than 50%. Since the referent output voltage is 10 V, a small offset can be observed in $V_{out}(t)$. This offset is dependent on the duty cycle of the power circuit, the time difference $t_{d,on} - t_{d,off}$, and C_{out}. $t_{d,on}$ depends on the voltage difference between V_B and V_{th}. Obtained modulation frequency is very close to 300 kHz.

25   In order to verify the analysis explained above, a 10.5 W prototype converter with regulation of the output voltage was produced and the measurements for the prototype converter is disclosed below.

Plots of drain, gate, and rectifier voltages in the power circuit are shown in Fig. 15. The drain and rectifier voltages were measured with capacitance of 2.2 pF in series with an

30   oscilloscope probe, in order to reduce influence of the probe to the power circuit. This introduces attenuation of A = 0.19 in the measurement and removes the DC component of the measured voltages. Component values of the power circuit are listed in Table I. Switching frequency of the power circuit is f_S =49 MHz. Open loop output voltage and output voltage and current are V_{out} = 10.2 V and I_0 = 1.04 A, respectively.

14

When the duty cycle of 50% is obtained, I_{out} =0.5 I_0 = 0.52 A. Plots of the waveforms of the relevant voltages in the converter for this case are shown in Fig 9. Modulation frequency f_M is at its maximum value of 300 KHz at 50% duty cycle, and drops as the duty cycle moves away from 50%. In addition, under these conditions output voltage ripple $\Delta V_{out,pp}$ is at its
5   maximum as well.

The comparator used in the circuit is AD8468 from Analog Devices. The component datasheet specifies 40 ns propagation delay. For comparison, a high speed TLV3501 comparator has a 4.5 ns propagation delay, which is a reduction by a factor of 9. This is by no means a limit since there are other significant contributors as well (conditioning and
10   power circuit on-off circuit). This delay may be increased even further at a cost of a lower modulation frequency f_M and higher output voltage ripple for a given C_{out}.

Figs. 15 and 16 illustrate relationships between the signals in time domain, v_{cmp+}, v_{cmp-}, v_{GS}, v_{DS}, and v_{out} (upper waveforms) with respect to the comparator output (lower waveforms). High output voltage ripple is caused by a small output filtering capacitance (C_{out} = 3.3 µF).

15   Efficiency of the converter is shown in Fig. 17(a) as a function of output power. Since f_M is allowed to drop significantly under light load conditions, efficiency is maintained high over wide load range (η>75%above 20% load) with peak efficiency above 81%.

Since the control is based on phase shift, a small DC error is introduced in the value of v_{out}, which varies with the load. If the output voltage ripple is assumed triangular (which is
20   reasonable since i_{conv} is a current square wave), the peak values of v_{out} are determined as:

$$V_{out+} = V_{out,ref} + \frac{I_0 - I_{out}}{C_{out}} \Delta t_+$$

$$V_{out-} = V_{out,ref} + \frac{-I_{out}}{C_{out}} \Delta t_-$$

So that the offset of V_{out} is determined by

$$V_{out,offset} = V_{out,ref} - \frac{\Delta V_{out+} + \Delta V_{out-}}{C_{out}} \Delta t_-$$

$V_{out,ref}$ is a target value for the output voltage set by V_{ref} and $R_{FB1} - R_{FB2}$ voltage divider. Δt_+ and Δt_- are the time delays from a point when v_{out} crosses $v_{out,ref}$ to a point where v_{out} reaches its maximum and minimum value, respectively. Depending on the variables in these
25   equations, $v_{out,offset}$ may be either positive or negative, and decreases with I_{out}. Measured dependence of Δv_{out} is shown in the lower plot of Fig. 17. Both the offset and the output ripple are reduced with increase in C_{out}, while the switching frequency will be reduced.

A comparison between the model disclosed above and experimental results show close, but not perfect matching. The reasons for this are subjects of further investigation; it is

15

assumed that imperfections in the active components and tolerances of the passive components are the main contributors. Still, the model gives significant insight into the system operation, and can be used as a good estimate during the converter design.

Compared to hysteresis based burst mode control, the new method of controlling the
5   resonant power converter allows use of a significantly slower and less expensive components in the control circuit, which is of importance for cost sensitive applications such as LED lighting and PoL converters. The illustrated power circuits and control circuits were implemented using only low cost commercially available components, with peak efficiency above 81% and high efficiency over wide load range.

10   Fig. 18 is a flowchart 100 of the new method of controlling a resonant power converter. The method starts with method step 110 wherein the resonant power converter is turned on.

When the resonant power converter is turned on, the output voltage and/or output current increases. A sense voltage is provided in the resonant power converter that corresponds to the output voltage or output current, and a reference voltage is provided in the resonant
15   power converter that corresponds to a desired resulting output voltage or output current of the resonant power converter.

According to method step 120, the output voltage and/or output current continue to increase until the corresponding sense voltage V_{sense} is equal to or larger than the reference voltage V_{ref}, and

20   according to method step 130, the output voltage and/or output current continue to increase until also a second time period t_2 has elapsed since a previous turn-on of the resonant power converter.

Thus, when the sense voltage V_{sense} is equal to or larger than the reference voltage V_{ref}, and a second time period t_2 has elapsed since a previous turn-on of the resonant power
25   converter, the resonant power converter is turned-off in method step 140.

When the resonant power converter is turned on, the output voltage and/or output current decreases.

According to method step 150, the output voltage and/or output current continue to decrease until the corresponding sense voltage V_{sense} is equal to or less than the reference
30   voltage V_{ref}, and

according to method step 160, the output voltage and/or output current continue to decrease until also a first time period t_1 has elapsed since a previous turn-off of the resonant power converter.

Thus, when the sense voltage V_{sense} is equal to or less than the reference voltage V_{ref}, and a first time period t_1 has elapsed since a previous turn-off of the resonant power converter, the resonant power converter is turned-off in method step 110.

In the following, properties of the phase-shift burst mode control method for very high
5   frequency (VHF) DC-DC converters are compared with a conventional control method with hysteresis based on comparison of a sense voltage with two threshold values. Again, an on-off controllable current source is used to model the low-frequency behaviour of VHF converters. Large output capacitance is used for output voltage filtering. The model is shown in Fig. 19(a).

10   Fig. 19(b) shows the model of Fig. 19(a) controlled with a conventional hysteretic control circuit and Fig. 19(c) shows the model of Fig. 19(a) controlled with a phase-shift burst mode control circuit.

For both circuits, the VHF power converter is operating (turned-on) when V_{ctrl} is high, e.g. 2 Volt, delivering an average current of $I_0 = 2$ A. The VHF power converter is turned-off when
15   V_{ctrl} is low, e.g. 0 Volt. In the present example, capacitor C_{out} and load R_{load} are set to 10 μF and 10 Ω, respectively. Reference voltage V_{ref} equals 1 V, high impedance signal conditioning network $H(s)$ has ratio of $V_{sense}/V_{out} = 1 : N$, e.g. 1 : 10, independent of frequency. The circuit configurations and component values are selected so that the target output V_{out} is equal to 10 V and at nominal load, the VHF power converter operates at a 50
20   % duty cycle. It is assumed that gate drivers do not introduce any delay in any of the circuits of Figs. 19 (a) – (c) so that $V_{ctrl} = V_{cmp}$.

In the control circuit with hysteresis shown in Fig. 19(b), instantaneous response of the comparator is assumed so that the comparator does not add a delay in the control loop. In the present example, the hysteresis window is $V_H = 20$ mV. The comparator turns the
25   converter on when $V_{sense} < V_{ref}$ and turns it off otherwise. Simulated waveforms of the converter voltages of the converter with hysteresis control are shown in Fig. 20.

Modulation frequency f_M, i.e. the frequency at which the converter turns on and off, is given by:

$$f_M = \frac{I_0/2}{2\,\Delta V_{out}\,C_{out}} = \frac{I_0/2}{2\,N\,V_H\,C_{out}}$$

30   This equation is derived under the assumption that propagation delay t_D of the comparator, the gate driver, and the power stage of the converter is zero, and the equation is a good approximation when $t_D \ll 1/f_M$. Expensive components, e.g. comparators, gate drivers, etc., have to be used in VHF designs to realize small propagation delays in the feedback loop.

Time difference ΔT from $V_{sense} = V_{ref}$ until $V_{sense} = V_{ref} + V_H$ in Fig. 20 equals $1/(4\ f_M)$. If $V_H \rightarrow 0$ and $t_D \rightarrow 1/(4\ f_M)$, the waveforms shown in Fig. 20 turn into the waveforms shown in Fig. 21 showing simulated waveforms of the converter voltages of the converter with phase shift burst mode control. The waveforms in Figs. 20 and 21 are aligned so that V_{sense}

5   voltages cross the respective V_{ref} voltages at the same time, e.g. 2 μs, 4 μs, 6 μs, etc. The output voltage ripples are identical in Figs. 20 and 21, however the signal propagation delay through the feedback loop is $1/(4\ f_M)$, see the time difference between converter currents $I_{conv,H/PS}$, comparator output voltages $V_{cmp,H/PS}$, etc.

With the component values mentioned above, the modulation frequency is 250 kHz.

10 In Fig. 21, the power converter is turned-on at 3 μs, 7 μs, 11 μs, and 15 μs, and the power converter is turned-off at 1 μs, 5 μs, 9 μs, and 13 μs, and the first time period is equal to the second time period that is equal to 2 μs and the fourth time period, i.e. the turn-on delay $t_{D,on}$, is equal to the third time period, i.e. the turn-off delay $t_{D,off}$, that is equal to 1 μs.

15 The converter with phase shift burst mode control provides the same output voltage ripple (i.e. $\Delta V_{out,H} = \Delta V_{out,PS}$) as the converter with conventional hysteresis control, while using one or more components in the feedback loop with significantly larger respective delays. The resulting delay may be distributed arbitrarily between the power stage, the comparator, and the gate driver(s). This is very important for VHF converters, since numerous start-up

20 and shutdown techniques (self-oscillating gate drivers and converters) with small, but finite delays may be utilized in a VHF converter with phase shift burst mode control.

Turn-on and turn-off delay ($t_{D,on}$ and $t_{D,off}$) do not need to be equal, either. Any one of the components in the feedback loop in any combination may contribute to the values of the turn-on and turn-off delays, with the restraint that:

$$t_{D,on} + t_{D,off} = \frac{1}{2\ f_M}$$

25

Output voltage of a converter with hysteresis control resides within the range from $H(s)^{-1}(V_{ref,H} - V_H)$ to $H(s)^{-1}(V_{ref,H} + V_H)$, resulting in a voltage ripple of $\Delta V_{out,H}$.

This is different of a converter with phase shift burst mode control as illustrate in Fig, 19 (c) in which the output voltage V_o is load dependent. The output voltage V_o decreases with

30 increased load. If output voltage ripple at $I_{out} = 1A$ is $\Delta V_{out,PS}$ and under assumptions of constant delay in the comparator (and otherwise ideal components), average value of $V_{out,PS}$ ranges from $\Delta V_{out,PS}/2$ at $I_{out} = 0$ to $-\Delta V_{out,PS}$ at $I_{out} = I_0$ linearly with I_{out}.

18

The variation of the output voltage V_o as a function of output current may be decreased in various ways. One way is to allow the reference voltage to change as a function of the output voltage V_o to compensate for the change in the output voltage V_o.

Fig. 22(a) shows a control circuit in which the sense voltage 20 is compared to a reference voltage 28 that is adjusted as a function of the mean output voltage V_o. $H_1(s)$ is an ordinary low-pass filter. In the illustrated circuit $V_{ref1} = V_{ref} - (V_{ref,mean} - V_{ref})$, where $V_{ref,mean}$ is the output of the low-pass filter $H_1(s)$. Thus, $V_{ref1} = V_{ref}$ when $V_{ref,mean} = V_{ref}$ and V_{ref1} decreases when the mean output voltage V_o increases and vice versa whereby the variation of the mean output voltage V_o as a function of output current is counteracted.

Fig. 22(b) shows another control circuit in which the sense voltage 20 is compared to a reference voltage 28 that is adjusted as a function of the mean of the comparator output voltage $V_{cmp,PS}$ 16. The operation of the illustrated control circuit is based on the fact that the average value of $V_{cmp,PS}$ varies linearly with the output current I_{out}.

Reference voltage V_{ref1} is formed by superposition of $V_{ref,PS}$ and low-pass filtered $V_{cmp,PS}$. The resistor and capacitor values in the compensation network need to be chosen to provide sufficient attenuation of the ac component of $V_{cmp,PS}$.

In the illustrated control circuit, when the converter operates at 50% modulation, the average of $V_{cmp,PS}$ equals V_{ref}. If the output current I_{out} is reduced, the average value of $V_{cmp,PS}$ is reduced, thus decreasing reference voltage V_{ref1} 28 thereby counteracting the increase of the output voltage V_o that would otherwise result for the reduced output current I_{out}. If the output current I_{out} is increased, the average value of $V_{cmp,PS}$ is increased, thus increasing reference voltage V_{ref1} 28 thereby counteracting the decrease of the output voltage V_o that would otherwise result from the increased output current I_{out}. V_{ref1} is calculated with the following formulae:

$$V_{ref1} = V_{ref,PS} \frac{R_1 \| (R_2 + R_3)}{R_1}$$
$$+ V_{cmp,PS,high} \frac{I_{out}}{I_0} \frac{R_1 \| (R_2 + R_3)}{R_1}$$

.

CLAIMS

1. A power converter comprising a control circuit coupled to compare a sense voltage with a reference voltage, and having a control output that is coupled to control turn-on and turn-off of the power converter in such a way that

5
the power converter is turned-on when an absolute value of the sense voltage is less than or equal to an absolute value of the reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

the power converter is turned-off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a

10
second time period has elapsed since a previous turn-on of the power converter.

2. A power converter according to claim 1, wherein the control circuit comprises a comparator that is coupled to compare the sense voltage with the reference voltage, and having a comparator output that is the control output.

15   3. A power converter according to claim 1 or 2, wherein the power converter is configured for operation at a frequency above 1 MHz.

4. A power converter according to any of the previous claims, comprising a delay circuit configured for providing at least part of at least one of the respective time periods.

5. A power converter according to any of the previous claims, wherein an output voltage

20
of the power converter is coupled to a signal conditioning circuit configured to output the sense voltage.

6. A power converter according to any of the previous claims, wherein the control output is coupled to control turn-off of at least one power switch of the power converter.

7. A power converter according to any of claims 1 - 6, wherein the control output is

25
coupled to control disconnection of energy transfer from the input to the output of the power converter.

8. A power converter according to any of claims 1 - 6, wherein the control output is coupled to control connection of energy transfer from the input to the output of the power converter.

30   9. A power converter according to any of the previous claims, wherein the power converter is a SEPIC converter.

10. A power converter according to claim 9, wherein the SEPIC converter is a self-oscillating SEPIC converter.

11. A power converter according to claim 9 or 10, wherein the power converter is an interleaved SEPIC converter.

12. A power converter according to any of the previous claims, wherein the control circuit is configured to compensate a dependence of the sense voltage on an output current.

13. A power converter according to claim 12, wherein the control circuit is configured to vary the reference voltage in dependence on the output current, whereby the dependence of the sense voltage on the output current is compensated.

14. A power converter according to claim 12, wherein the control circuit is configured to vary at least one of the first and second time periods in dependence of the output current, whereby the dependence of the sense voltage on the output current is compensated.

15. A method of controlling a power converter, comprising the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

10
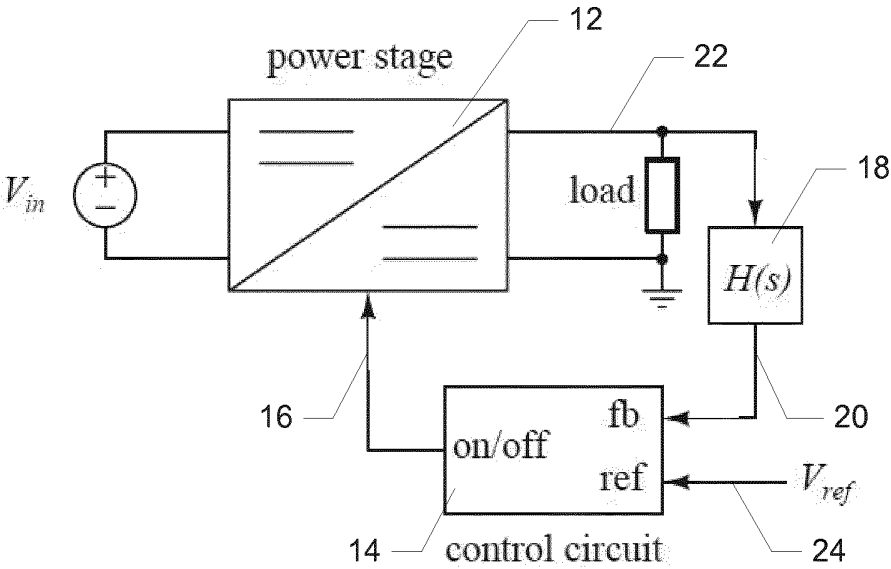
Fig. 1

2/22
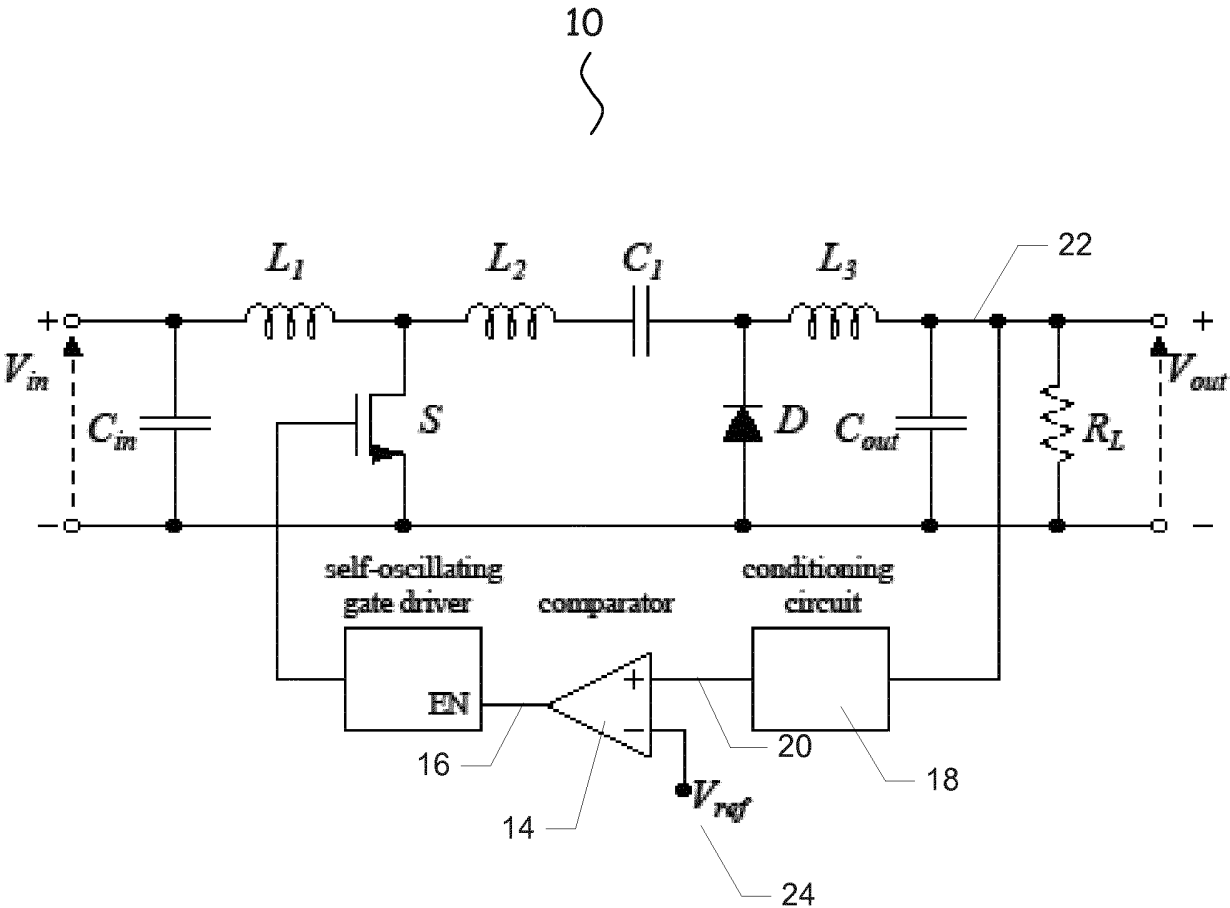
Fig. 2

3/22
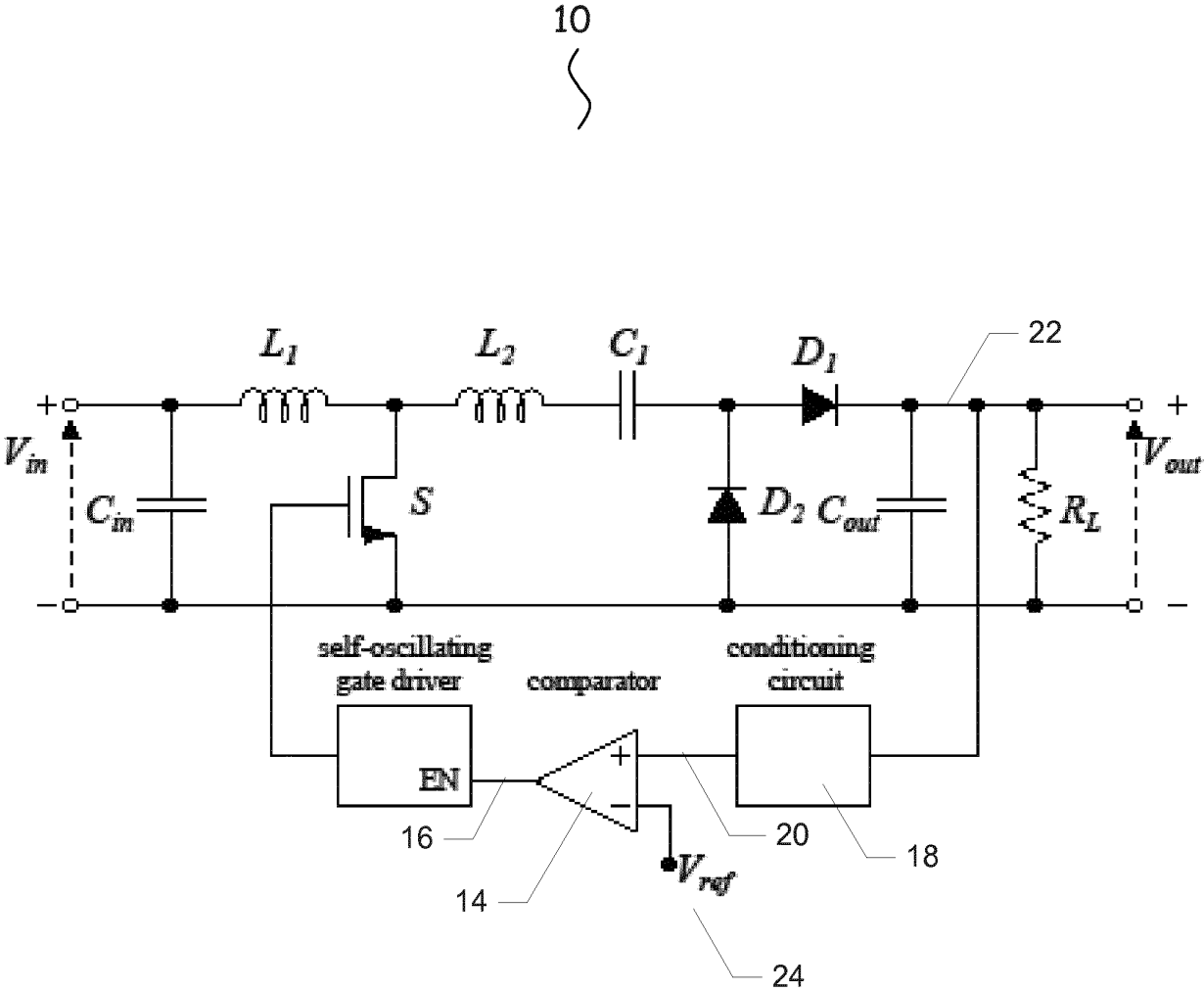
Fig. 3

4/22
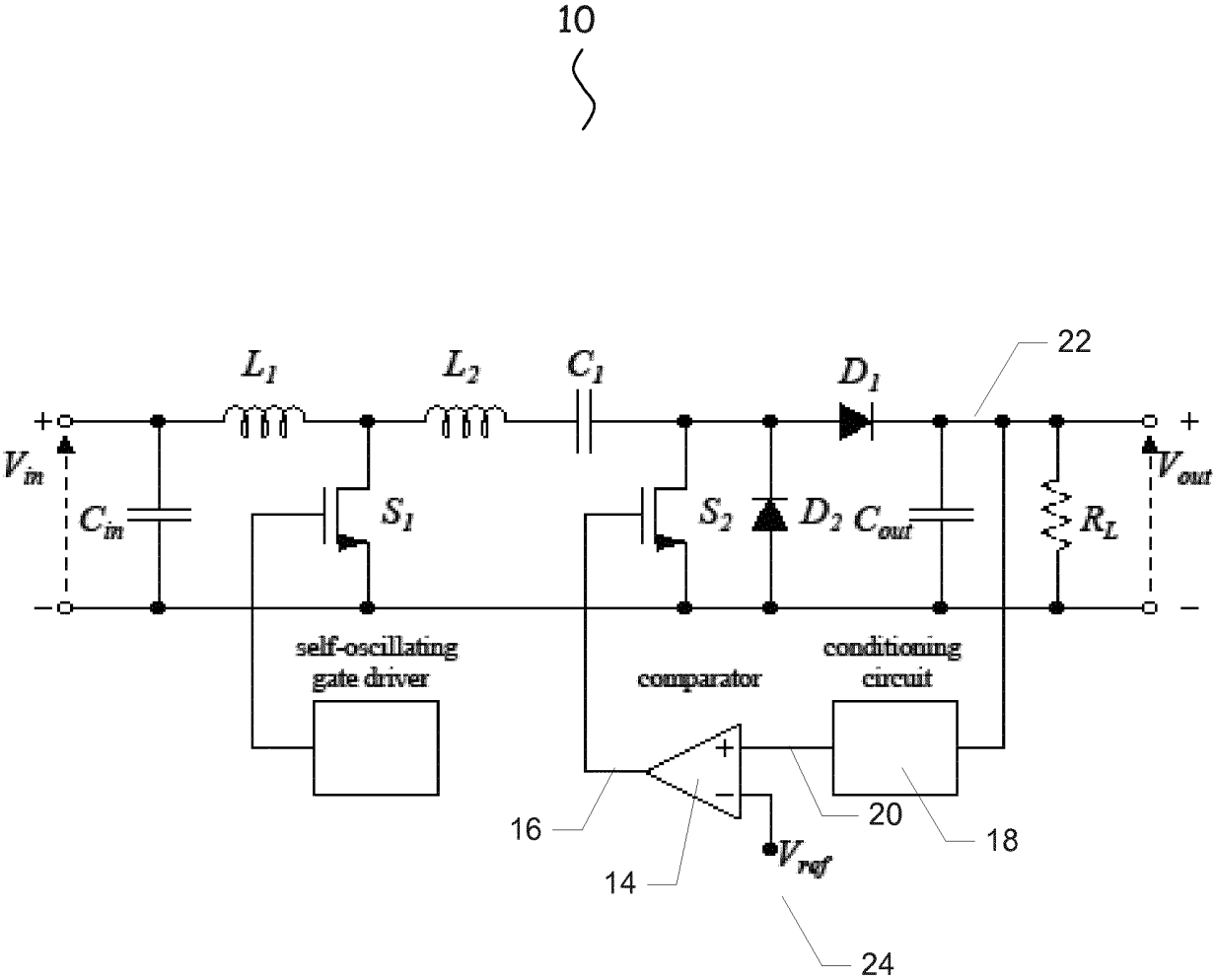
Fig. 4

5/22
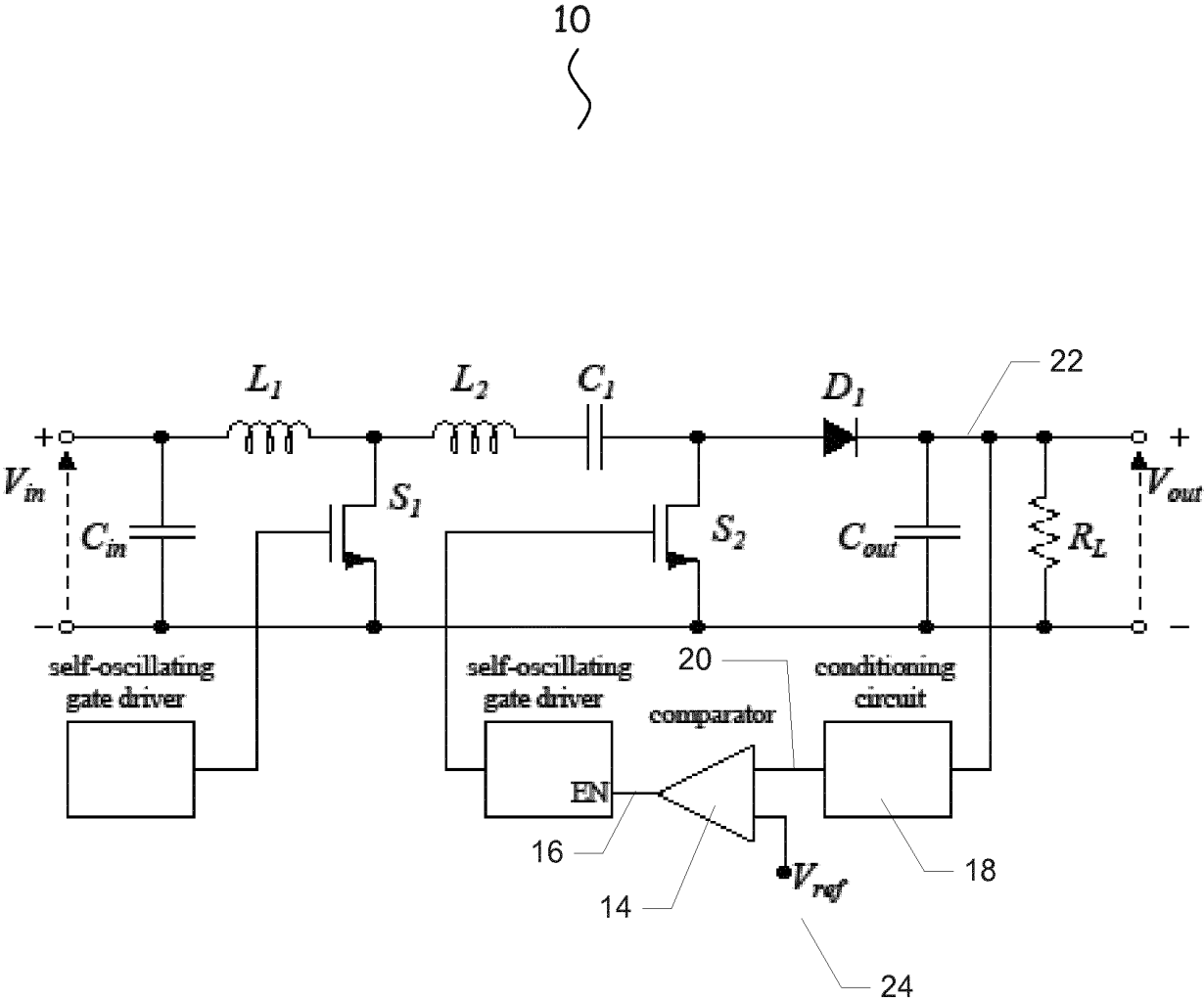
Fig. 5

6/22
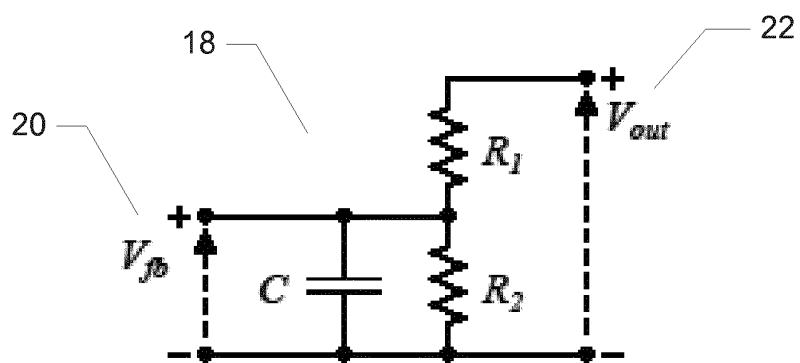
(a)
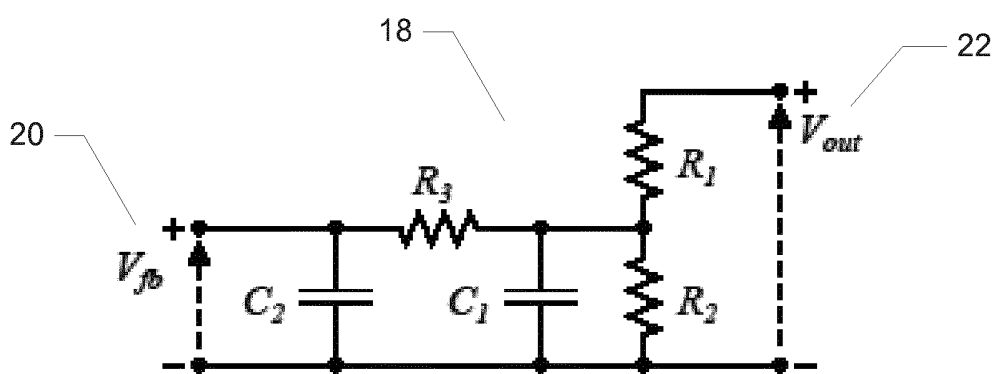
(b)

Fig. 6

7/22
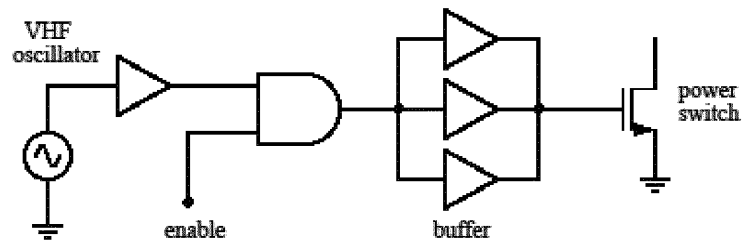
(a)
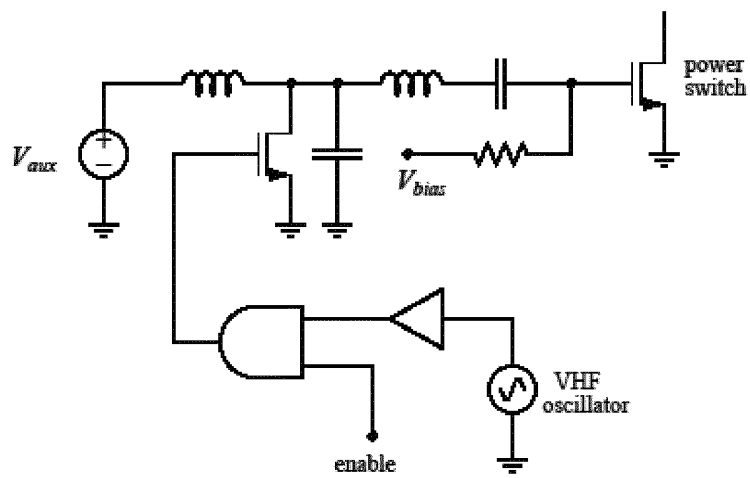
(b)

Fig. 7

8/22
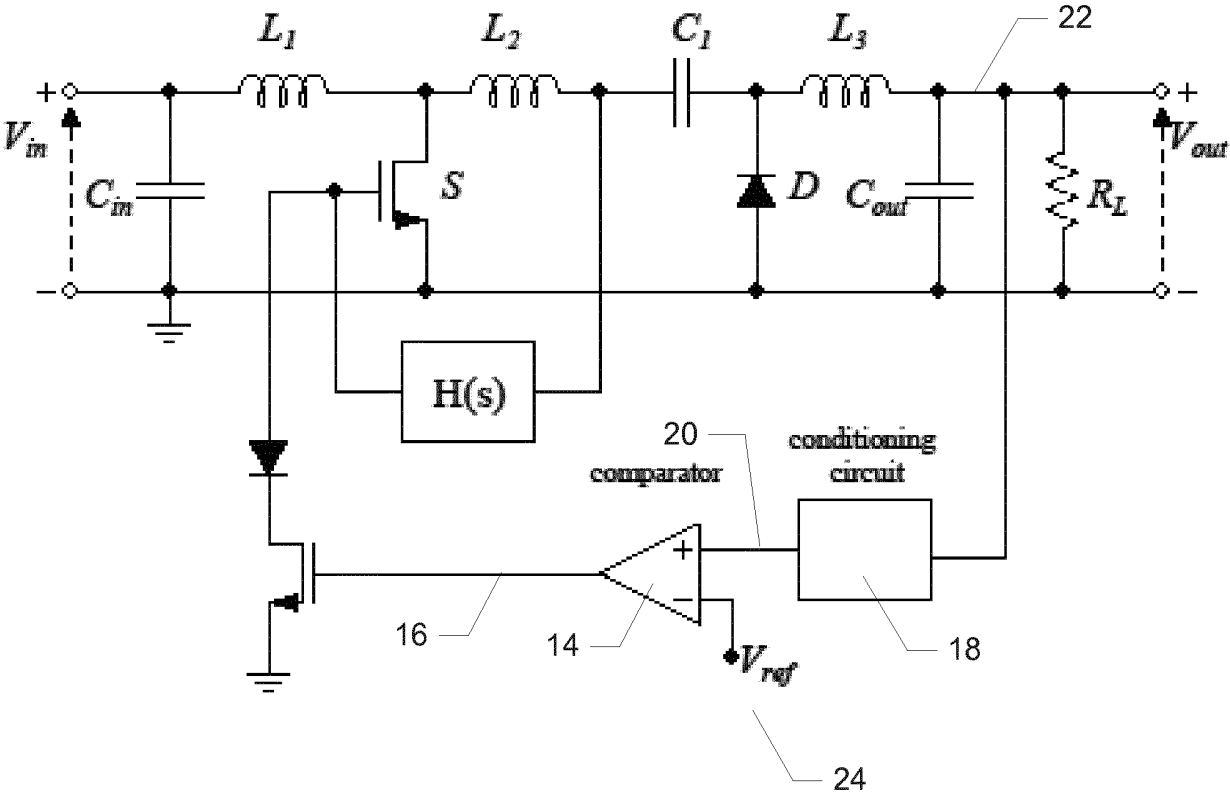
Fig. 8

9/22
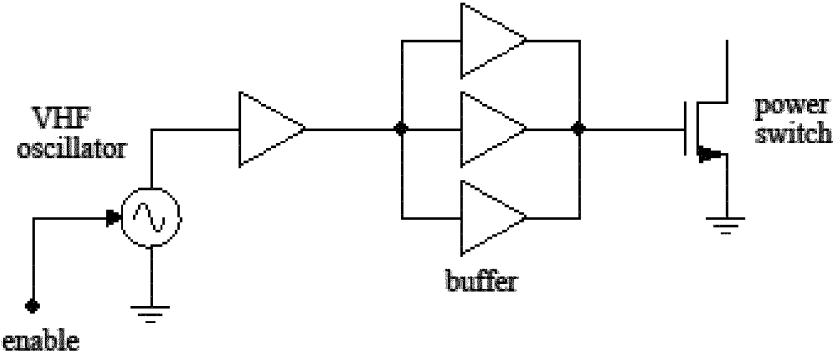
Fig. 9

10/22
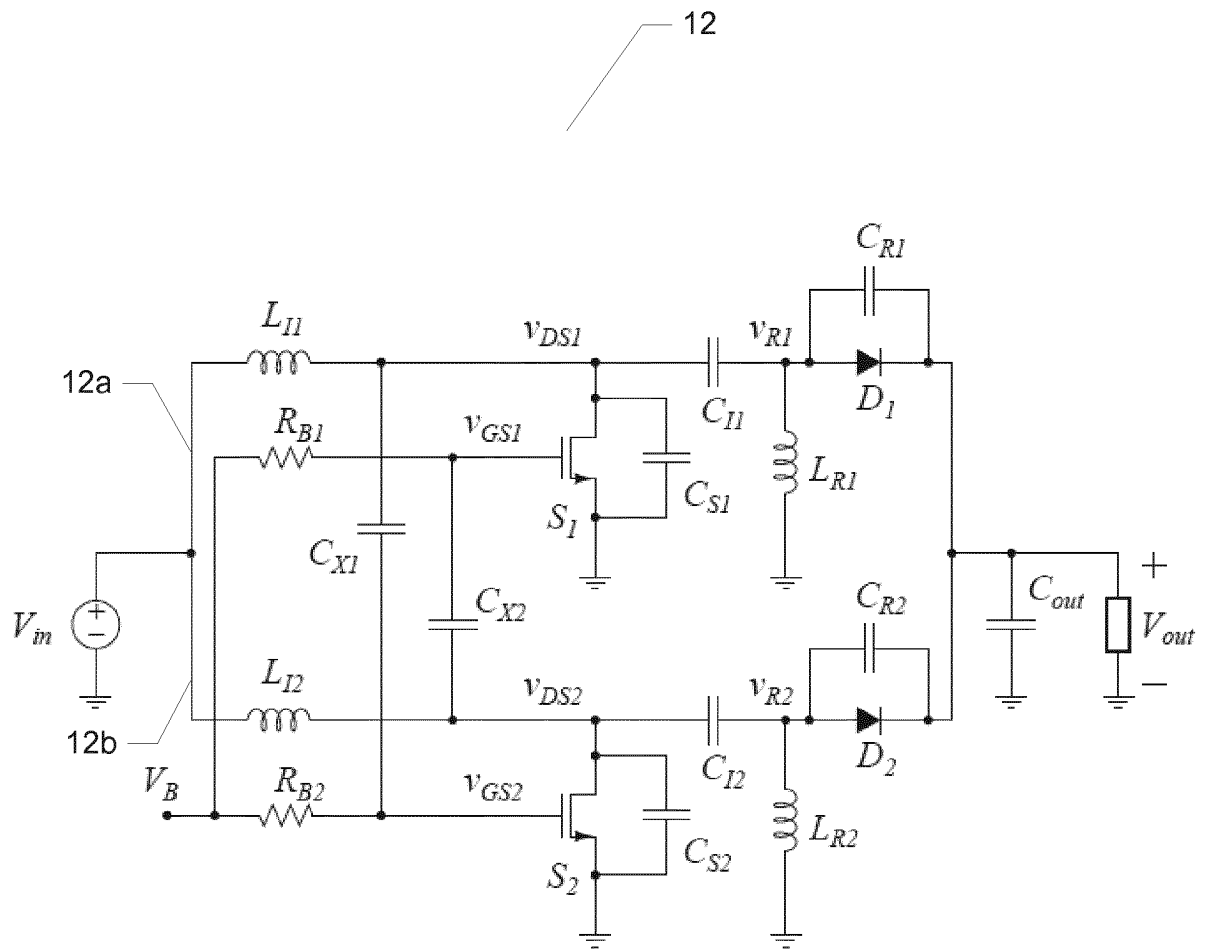
Fig. 10

11/22
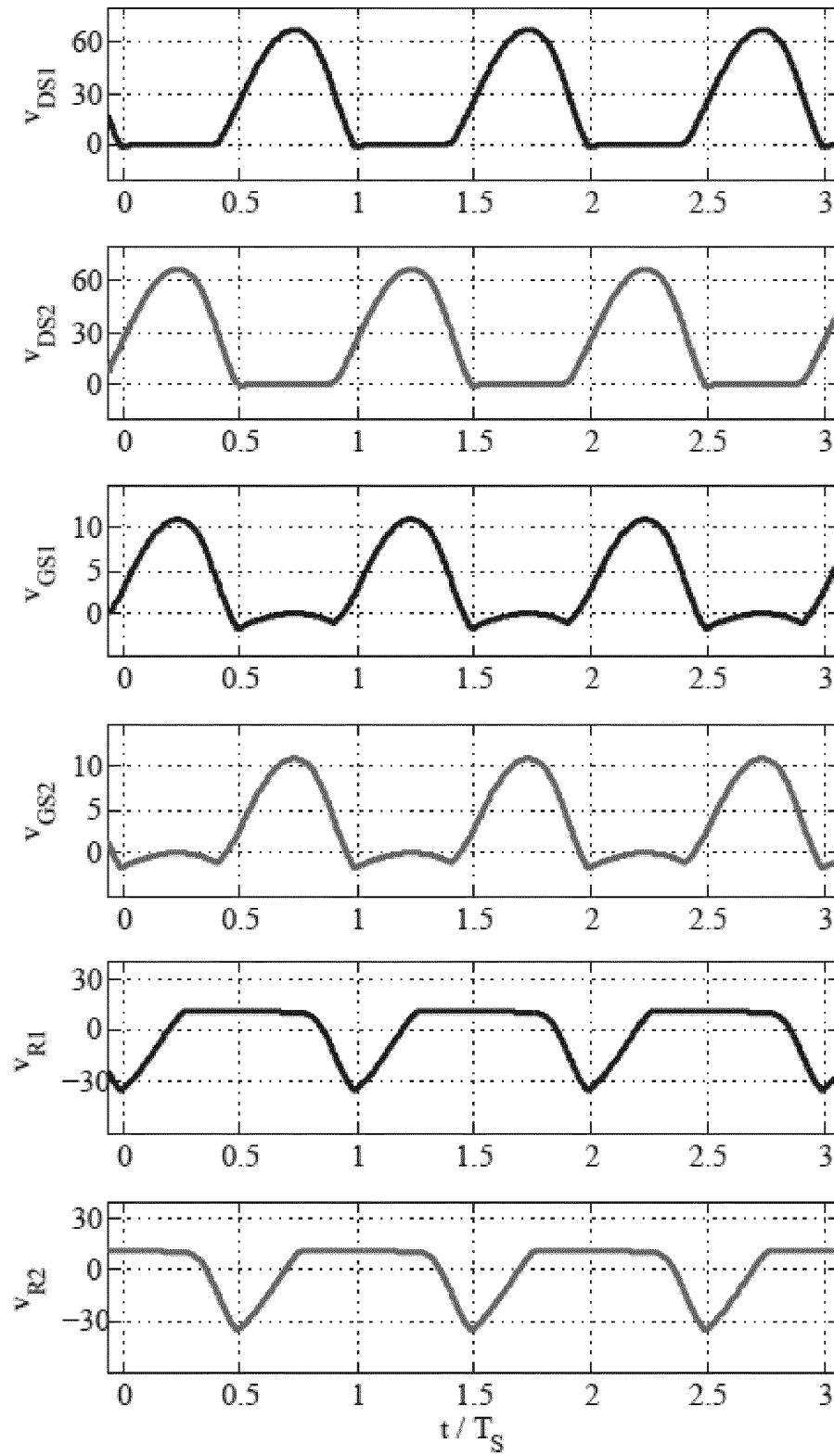
Fig. 11

12/22
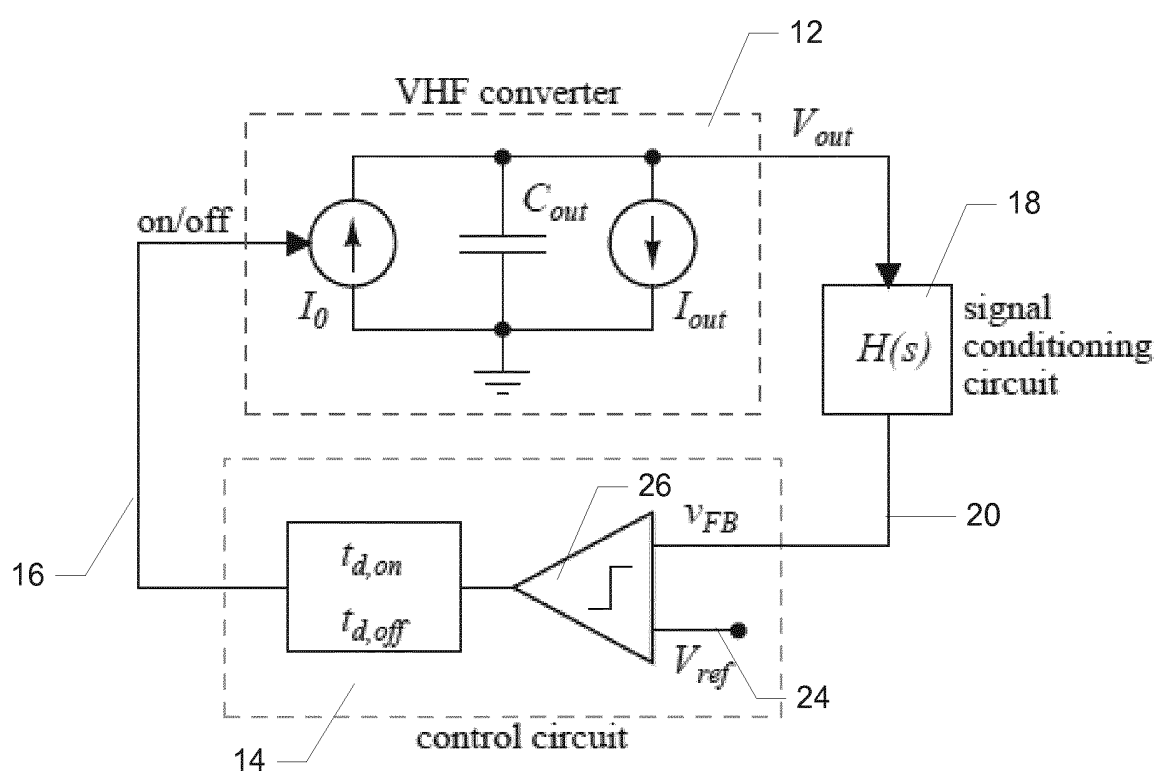
Fig. 12

13/22

Fig. 13

14/22

Fig. 14

15/22

(a) $v_{cmp+}(t)$: 50 mV/div, 1 μs/div

(b) $v_{cmp-}(t)$: 50 mV/div, 1 μs/div

(c) $v_{out}(t)$: 100 mV/div, 1 μs/div

Fig. 15
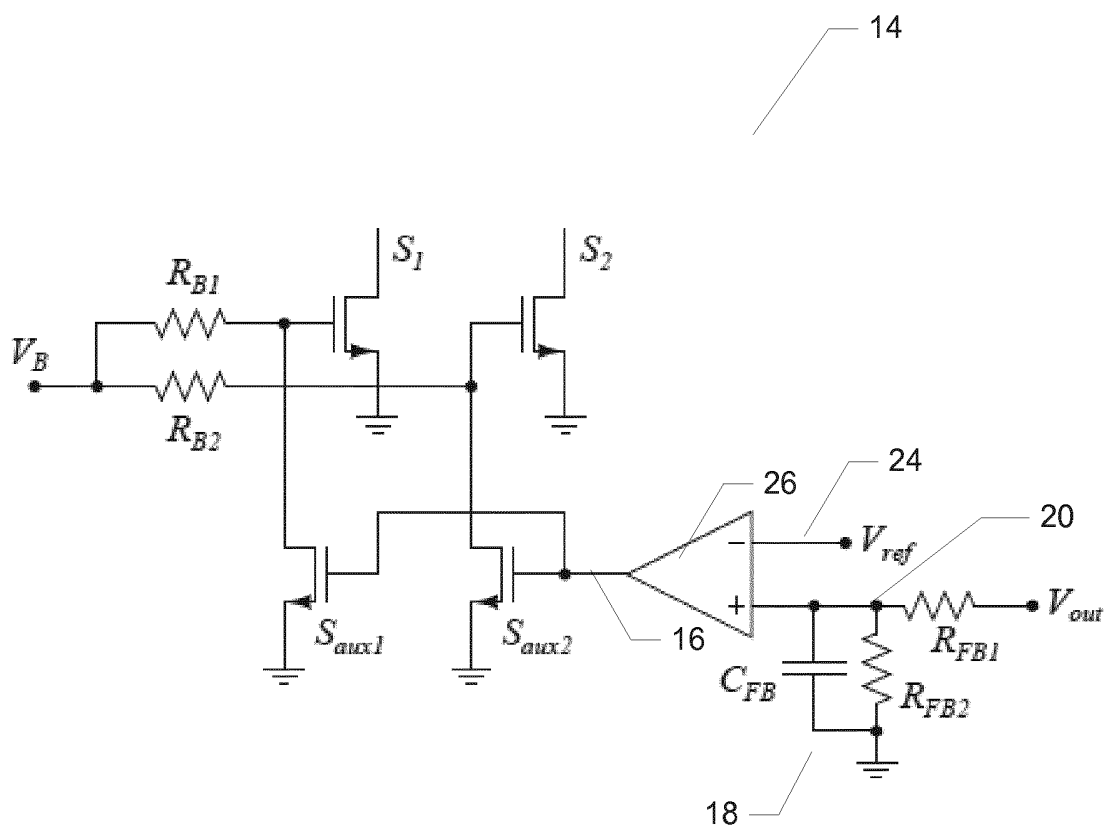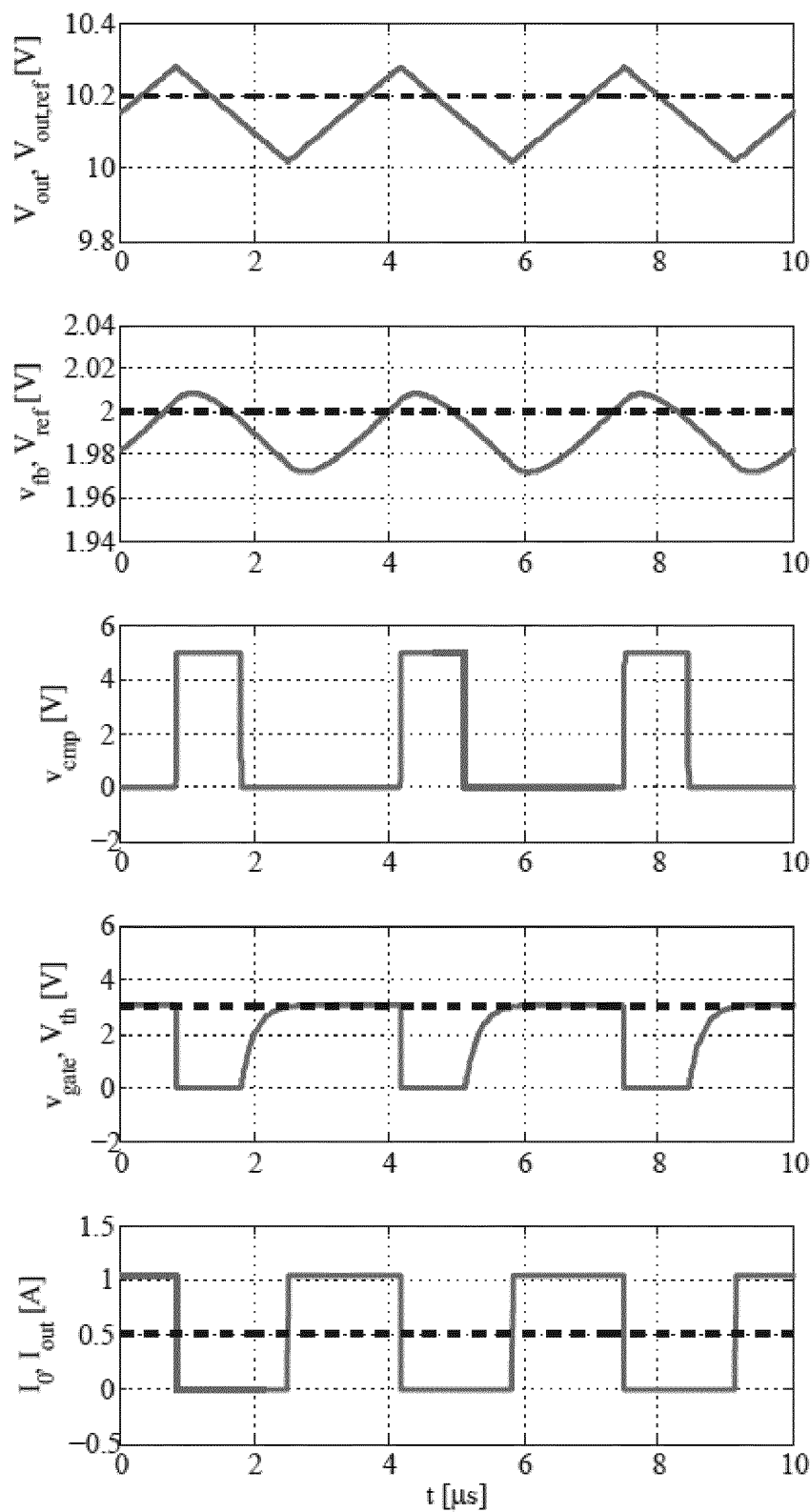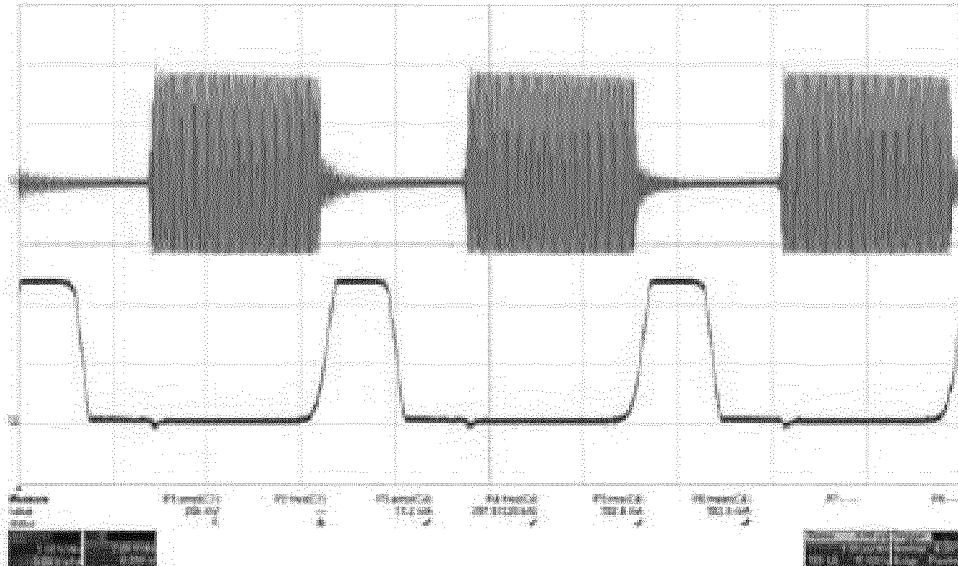
(a) $A \, v_{DS,AC}(t)$ (scaled, no DC): 5 V/div, 1 μs/div
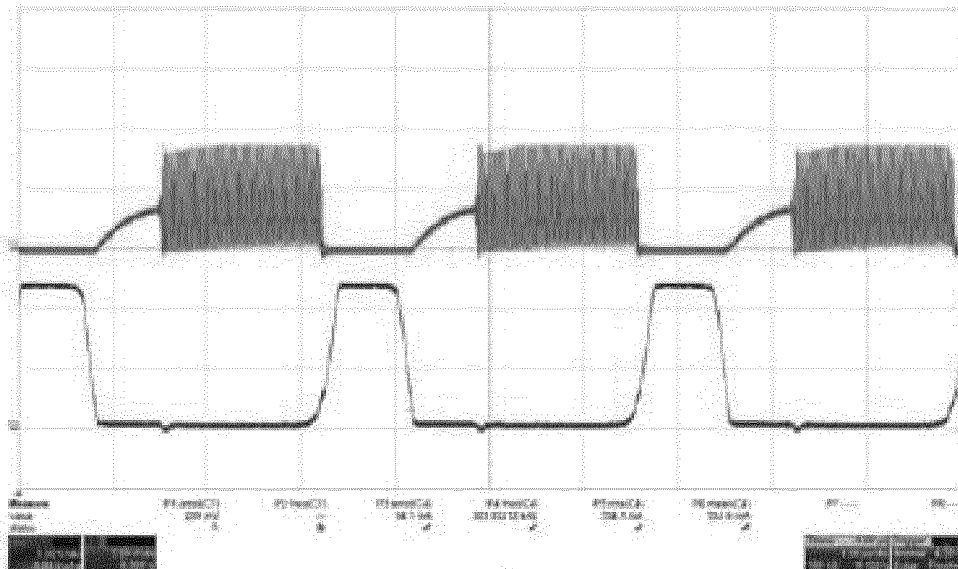
(b) $v_{GS}(t)$: 5 V/div, 1 μs/div
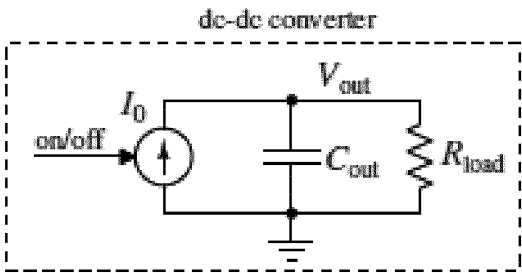
Fig. 16

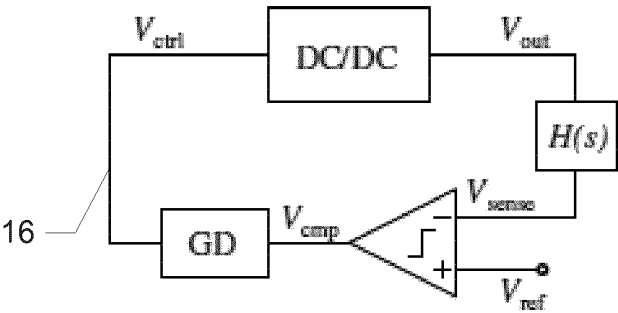# 17/22
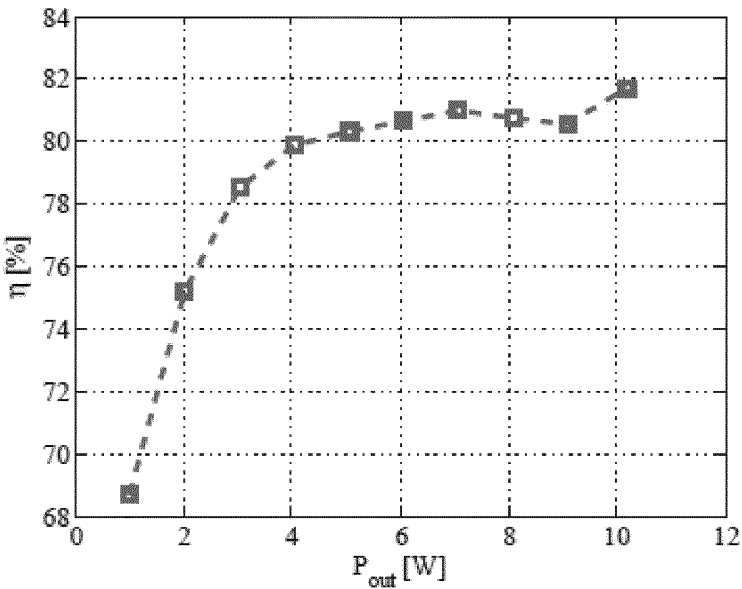
(a)
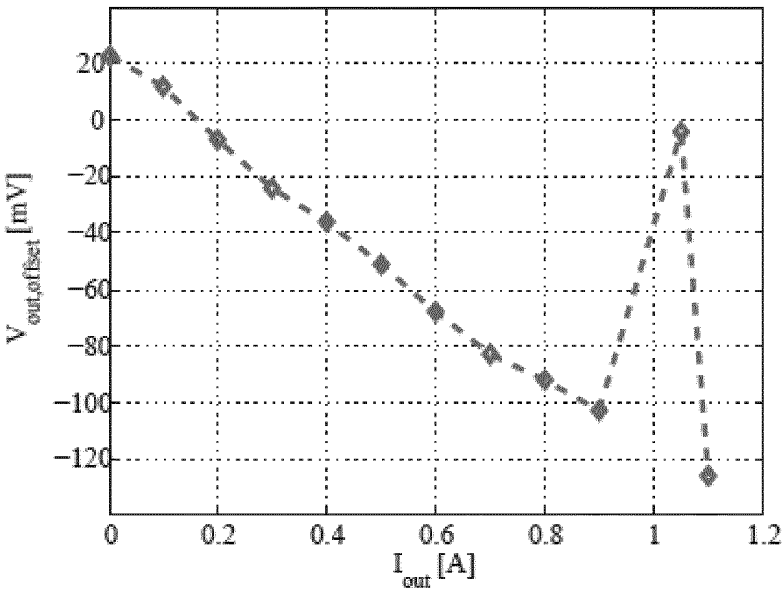
(b)

Fig. 17

18/22
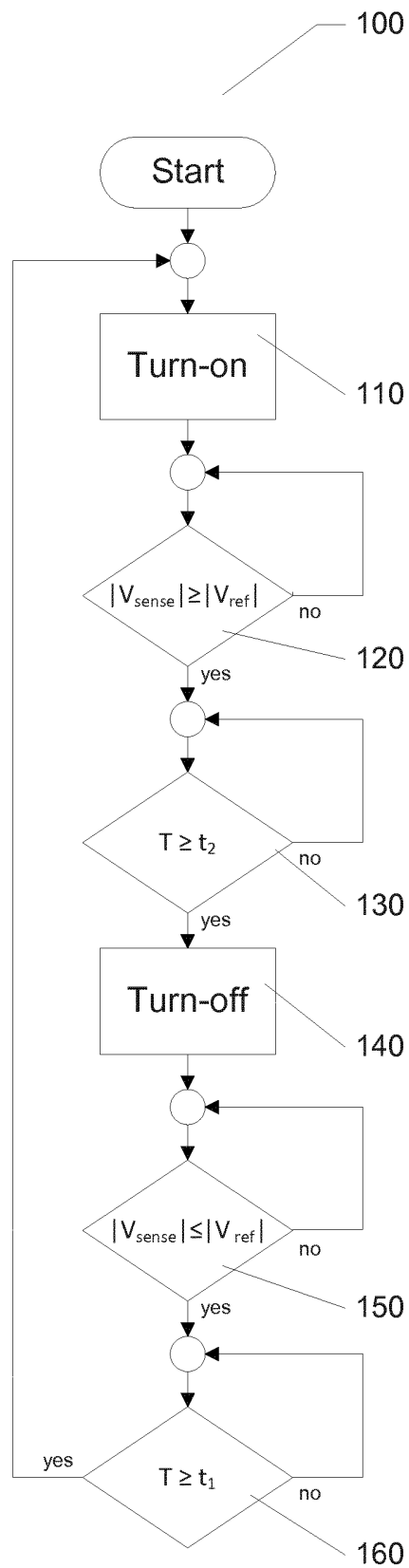
Fig. 18

19/22

(a)
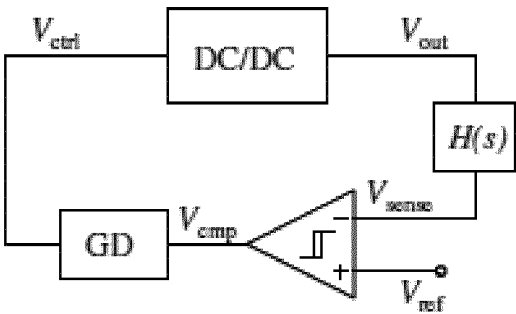
(b)

(c)

Fig. 19

20/22
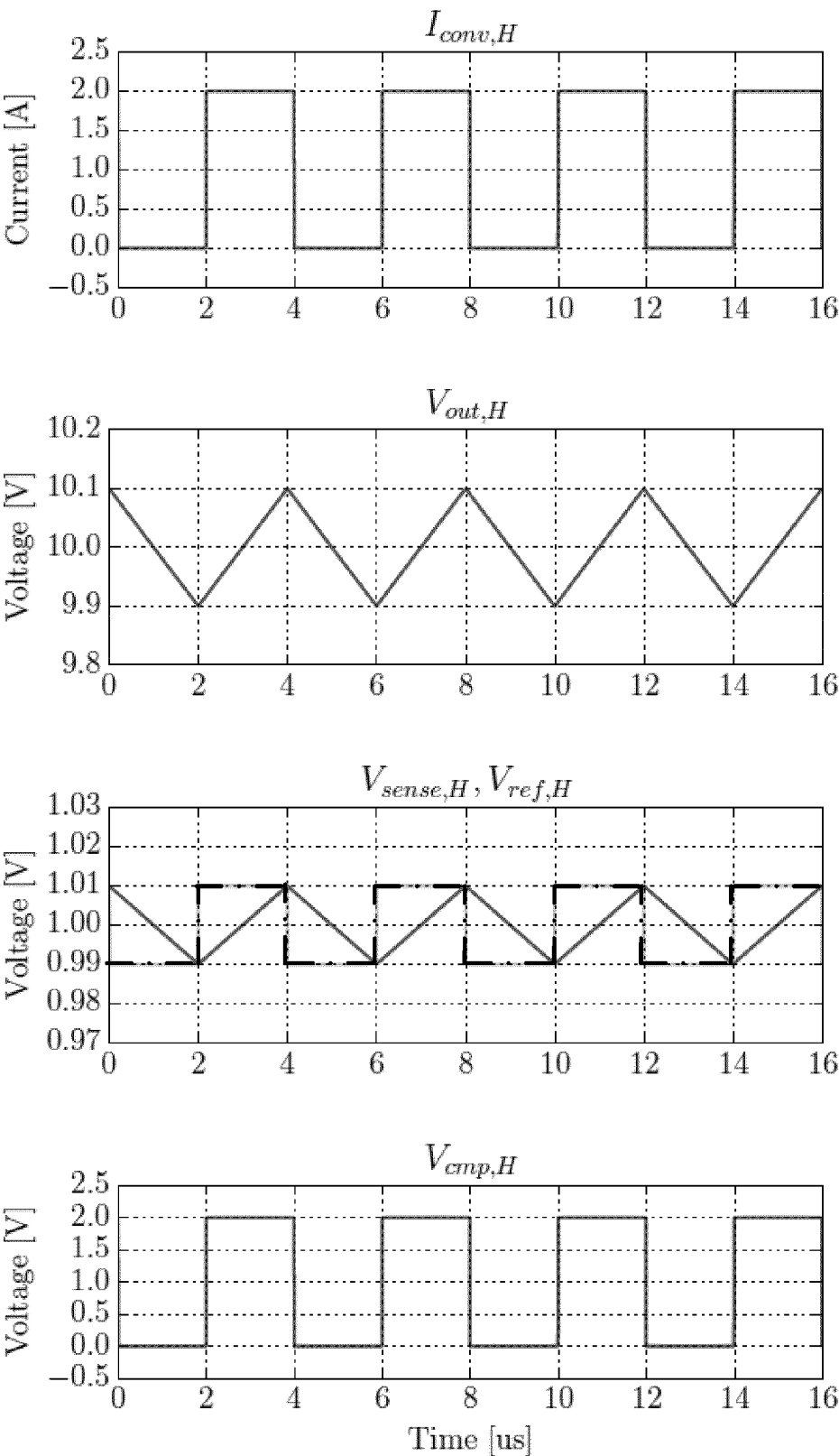
Fig. 20
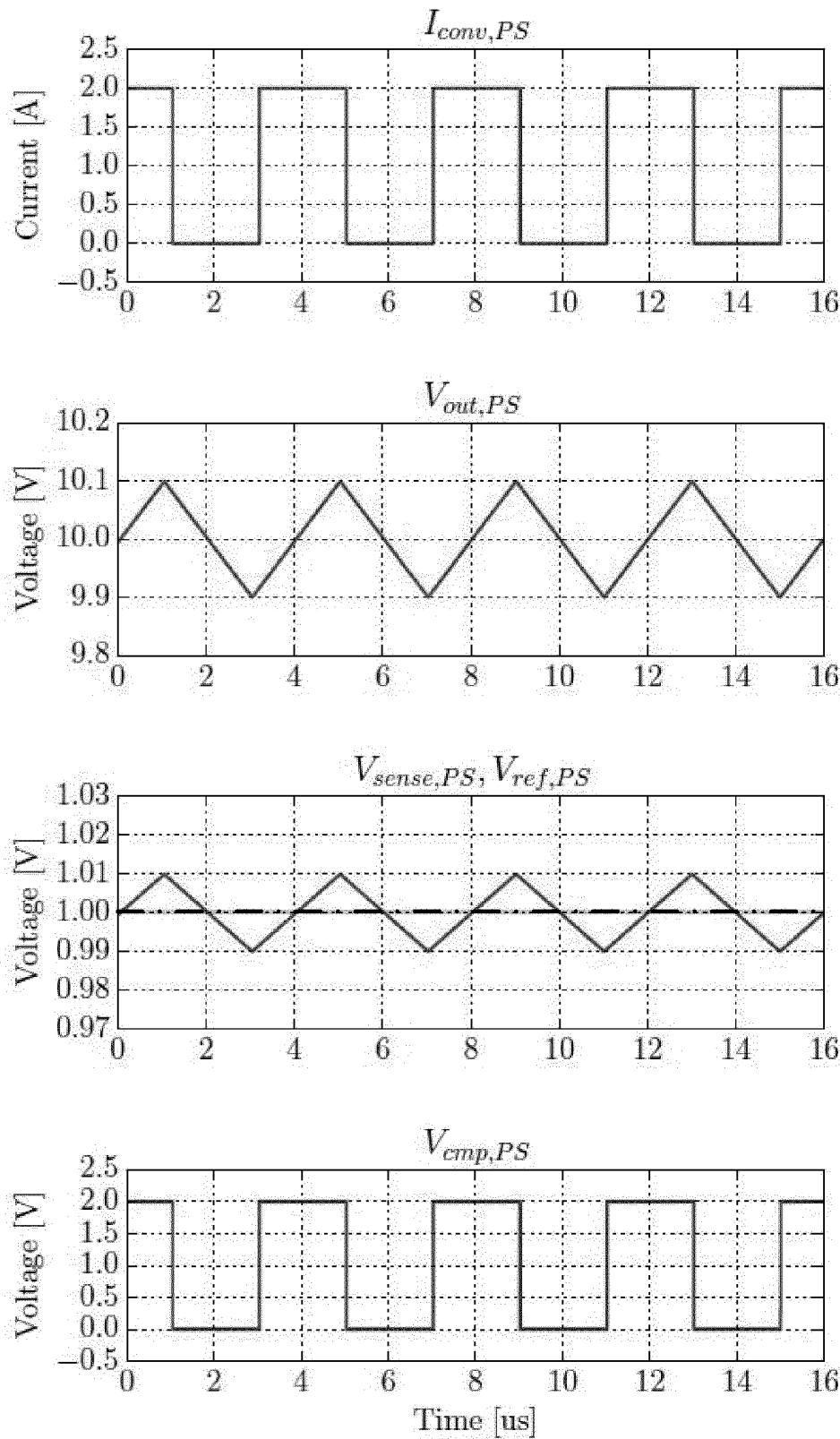
Fig. 21

22/22
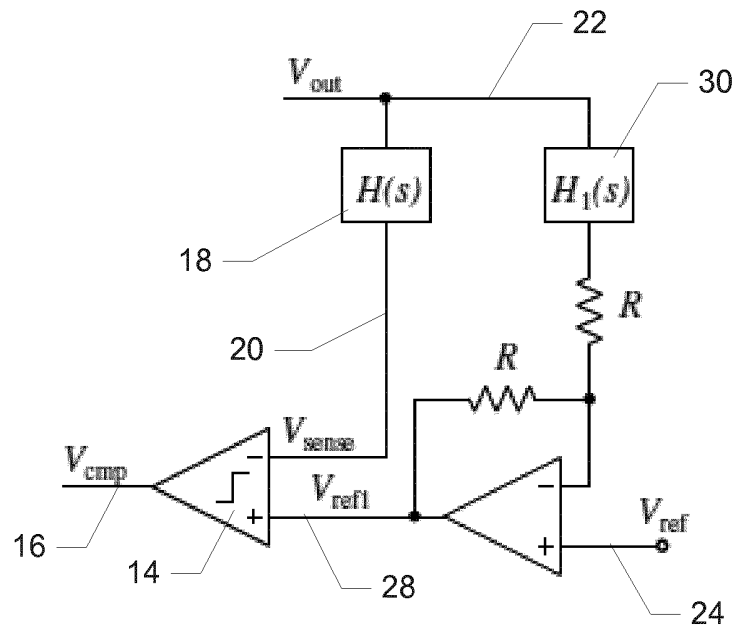
(a)
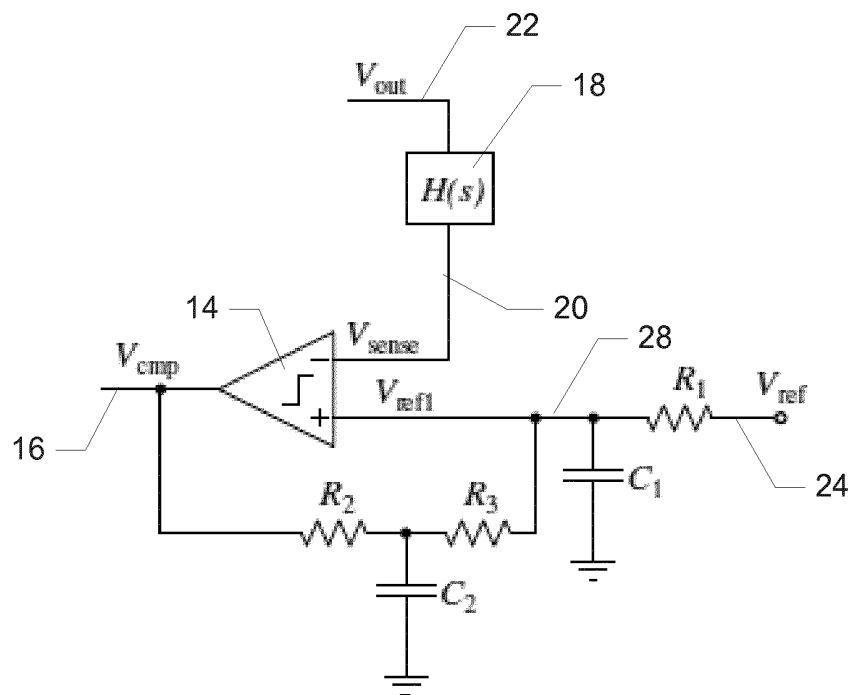
(b)

Fig. 22

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/155   H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/003094 A1 (SOERENSEN ALEX [DK]) 2 January 2014 (2014-01-02)	1-11,15
Y	paragraphs [0189] - [0191]; figures 1-6 -----	12-14
Y	US 2010/213911 A1 (OKI HIDETA [JP]) 26 August 2010 (2010-08-26) paragraphs [0004], [0007], [0008], [0025], [0034]; figure 7 -----	12
Y	US 2011/031948 A1 (CHIEN MIN CHU [TW] ET AL CHIEN MIN-CHU [TW] ET AL) 10 February 2011 (2011-02-10) paragraphs [0077], [0082] - [0087], [0106], [0149] - [0168]; figures 17,20 -----	12-14

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 May 2015	02/06/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gusia, Sorin

Form PCT/ISA/210 (second sheet) (April 2005)

Patent document cited in search report			Publication date	Patent family member(s)			Publication date
US 2014003094	A1		02-01-2014	EP	2678927	A2	01-01-2014
				US	2014003094	A1	02-01-2014
				WO	2012113396	A2	30-08-2012
US 2010213911	A1		26-08-2010	JP	2010200450	A	09-09-2010
				US	2010213911	A1	26-08-2010
US 2011031948	A1		10-02-2011	TW	201106597	A	16-02-2011
				US	2011031948	A1	10-02-2011
				US	2013147456	A1	13-06-2013
				US	2014084891	A1	27-03-2014