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A 3D Hybrid Integration Methodology for Terabit Transceivers

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Abstract—This paper presents a three-dimensional (3D) hybrid integration methodology for terabit transceivers. The simulation methodology for multi-conductor structures are explained. The effect of ground vias on the RF circuitry and the preferred interposer substrate material for large bandwidth 3D hybrid integration are described. An equivalent circuit model of the via-throughs connecting the RF circuitry to the modulator is proposed and its lumped element parameters are extracted. Wire bonding transitions between the driving and RF circuitry were designed and simulated. An optimized 3D interposer design demonstrated a simulated -3 dB transmission bandwidth up to 95 GHz with associated return loss better than 10 dB. A thermal analysis of a subassembly for the packaged transmitter module is performed. A maximum temperature of 74 °C is predicted when copper-tungsten is used as the material of the sub-mount and heat sink layer.

I. INTRODUCTION

With the ever increasing demand worldwide for high-speed communication, the optical Ethernet has been considered to be an ideal candidate for the next-generation high-speed data transmission system [1]. As internet has become an essential part of people's life, large amounts of data, such as high-definition videos, images, voices, and files, have to be transmitted and received by the transmission systems every day. On one hand, these blooming data traffic and multimedia services dramatically increase the workload for the transmission system and degrade the performances of the currently used edge switches and data-center gateways. On the other hand, it promotes the development of high-speed optical Ethernet. Besides, the modulation scheme of dual-polarization quadrature phase-shift keying (DP-QPSK) cannot meet the increasing demand of massive transmission. The next migration from 100 Gbit/s to 400 Gbit/s and further on to 1 Tbit/s optical line card products based on higher-order quadrature amplitude modulation (QAM) should take place in the near future [2].

PANTHER, the abbreviation of “Passive and electro-optic (EO) polymer photonics and indium phosphide (InP) electronics iNtegration for multi-flow Terabit transceivers at edge software-defined networking (SDN) switchEs and data-center gateways”, is an European project that aims to combine electro-optic with passive polymers and develop a novel photonic integration platform with unprecedented potential for high-speed modulation and optical functionality on-chip. By using three-dimensional (3D) hybrid integration techniques, PANTHER will integrate these components into compact

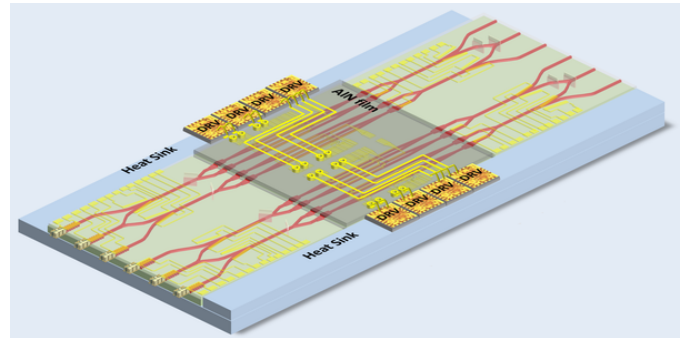


Fig. 1. The 3D hybrid integration scheme of photonic and electronic components (from [3]).

system-in-package transceivers with 64 Gbaud operation rate. By using dual-polarization (DP) 64-QAM, the overall capacity of the transceivers can go up to 1.536 Tbit/s [3].

Fig. 1 shows the envisioned scheme for the PANTHER transmitter based on the 3D hybrid integration of photonic and electronic components. Since the operation rate of the transceiver is 64 Gbaud, the optical and electronic devices should work well at least up to 64 GHz. At such a high operation frequency, the circuitry and transitions need to be designed and optimized carefully due to dielectric loss, impedance mismatch, parasitic effects, higher-order modes, resonances, and radiations.

In this work, contributed to PANTHER, differential high-speed electrical lines on thin ceramic films are designed and analyzed by using appropriate electromagnetic (EM) simulation methodology. The via-throughs are modelled and optimized for the 3D integration scheme to support a bandwidth up to 64 GHz. The wire bonding transitions between the driving and RF circuitry are simulated and optimized for minimal inductive discontinuities. RF circuitry based on a quartz interposer is designed. The main challenges with respect to the RF circuitry are achieving sufficient bandwidth with good phase balance when signals are transmitted differentially and suppression of the resonances of the interconnections. Besides, the power handling capability of the transmitter modules can be hard to estimate and is investigated by thermal simulations.

In Section II, the fundamental properties, modeling methodology, and effects of ground vias of the RF circuitry are described. Besides, the modeling methodology and optimization of the via-throughs, the proposed structure of wire bonding

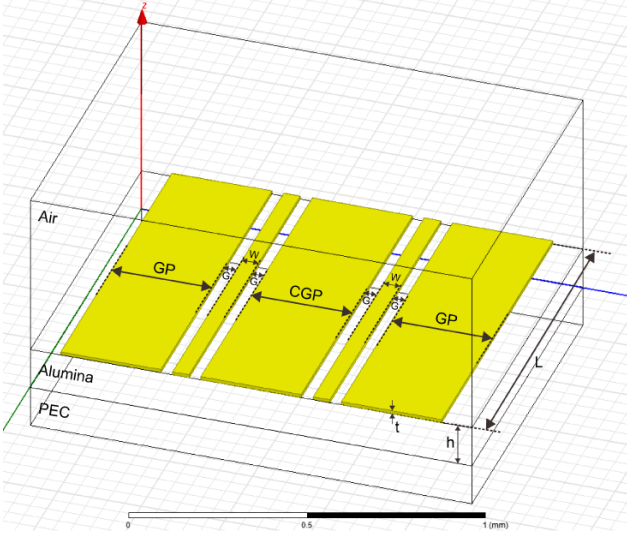


Fig. 2. Coupled coplanar waveguide structure.

transitions and its electromagnetic simulation are presented. Finally, In Section III, the designed full circuitry of the terabit transmitter is characterized by electromagnetic and thermal simulations.

II. RF CIRCUITRY, VIA-THROUGHS, AND WIRE BONDING TRANSITIONS

A. RF Circuitry on Interposer

In high-speed signaling it is often necessary to transmit the information in a differential manner for improved immunity towards noise. The RF circuitry on the interposer should therefore be able to support differential signals as both the output of the driving circuitry and input of the modulator are designed assuming differential signals. Coplanar waveguide (CPW) was first demonstrated by C. P. Wen in 1969 [4]. Two ground traces are located on both side of the signal trace forming a ground-signal-ground (GSG) structure. For a GSGSG structure shown in Fig. 2, it is called coupled coplanar waveguide (CCPW) [5]. The dielectric constant (ϵ_r) of the substrate is usually different from air (ϵ_0) which means that the wave propagates in an inhomogeneous material. A quasi-TEM mode is supported by CPW structure instead of a true TEM mode. According to [6], CPWs are easy to fabricate and it is easy to mount active and passive devices on its surface. It also provides lower radiation loss compared to conventional microstrip lines. Besides, the characteristic impedance of CPW is mainly determined by the ratio of $W/(W + 2G)$, in which W and G represent the width of the signal trace and the width of the gap between the signal trace and the ground trace. This special characteristic makes CPW easy to be tapered in and out without affecting the characteristic impedance. As a result, CPW is widely used in microwave integrated circuits (MICs) as well as monolithic microwave integrated circuits (MMICs).

It is well-known that available commercial electromagnetic simulators can have difficulties with such multi-conductor structures and reasonable simulation results are not always straightforward to obtain. High Frequency Structural Simulator (HFSS), the industry standard for 3D full-wave electromagnetic field simulations, is used in this work. In order to find

TABLE I. CCPW DIMENSIONS AND SUBSTRATE PARAMETERS.

CCPW dimensions (μm)					
W	G	GP	CGP	t	L
50	35	300	300	10	1000
Alumina substrate parameters					
ϵ_r	$\tan\delta$		h		
9.4	0.006		127 μm		

a reliable simulation method, an example, shown in Fig. 2, is tested with several different simulation setups. The metalization is gold and the substrate is alumina for simulations. The heat sink layer will be made of copper-tungsten (CuW) but it is modelled as perfect electric conductor (PEC) for simulations. The dimensions and substrate parameters used in HFSS are given in Table I. The CCPW example is designed to have characteristic impedance of approximately 50 Ω based on alumina substrate.

The preferred simulation setup in HFSS, shown in Fig. 3, is based on the solution type of driven terminal and it uses vertical PEC ground bridges together with lumped ports as an excitation scheme. In this setup the PEC bridges are perpendicular to the conductor traces and touch the ground traces. The PEC bridges could also be horizontal with slightly difference on the simulation results. The lumped ports are assigned to the surface which connects the signal traces to the PEC bridges. The PEC bridges are selected to be references while the two signal traces are selected to be terminals. The ground planes are short-circuited together by the connected PEC bridges. This simulation setup resembles well the real excitation assuming wire bonding transitions to the driving InP electronics. It is also the preferred method for correlating simulation results with probed measurements [7]. The PEC ground bridge adds a small parasitic inductance to the port excitation while the lumped port across the gap introduces a small parasitic capacitance. For highest accuracy these parasitic elements should be carefully calibrated out using the technique described in [8]. For the CCPW example, the effect of the small-valued parasitic elements remains negligible in the simulated frequency range up to 100 GHz. The red lines in Fig. 5 show the simulation results using the excitation with PEC ground bridges and lumped ports. The return loss remains better than 20 dB while the insertion loss is less than 1 dB in the whole frequency range up to 100 GHz. Notches are located at 28 GHz, 47 GHz, 60 GHz, and 83 GHz where the ground traces resonate despite the connection by the PEC ground bridge at the two ends of the CCPW structure. This shows the importance of distributing ground vias along the ground traces of the CCPW structure.

In order to suppress the resonances of the ground traces, vias are added which connect the ground traces to the bottom conductor layer. Fig. 4 shows the CCPW structure with ground vias. When designing the ground vias, the dimensions and the positions of the vias are usually limited by the requirements from the manufacturer. The diameter of the ground vias is 100 μm and they are located as close to the edges of the ground traces as possible. The blue lines in Fig. 5 show the simulation results of the CCPW example with ground vias. A big improvement is achieved in comparison with the CCPW example without ground vias. The resonances of the ground traces are successfully suppressed. The return loss is better than 20 dB and the insertion loss is less than 0.4 dB up to 100 GHz.

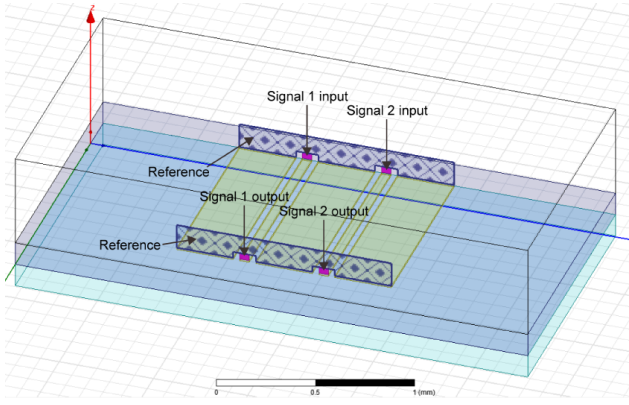


Fig. 3. Vertical PEC ground bridges with lumped ports in HFSS.

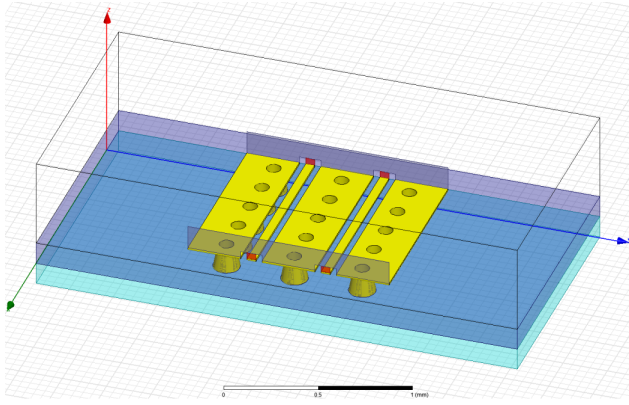


Fig. 4. CCPW structure with ground vias.

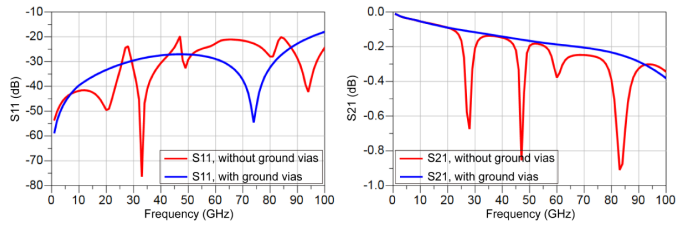


Fig. 5. Simulation results of CCPW with (blue solid lines) and without (red solid lines) ground vias.

B. Modeling and Optimization of Via-throughs

Via-throughs are used for the transition from the RF circuitry on the interposer to the input pads of the modulator on the EO polyboard. The via-throughs should be optimized for a bandwidth larger than 64 GHz. For a seamless transition between the RF interposer and the modulator this roughly translates into a requirement of a return loss better than 10 dB up to 64 GHz. As is shown in Fig. 6, the dimensions of the input pads of the modulator on the EO polyboard are fixed. The width of the signal pad is 150 μm with a 55 μm gap at each side while the width of the ground pads is 300 μm . Besides, the design and optimization of the via-throughs should fulfil the requirements from the manufacturer. Here the effect of the substrate material on the bandwidth of the via-throughs is investigated. The following substrate materials of the RF interposer are simulated: Alumina (*Alumina_96pct*), Aluminum Nitride (*Al_N*), Beryllium oxide (*Be_O*), Rogers

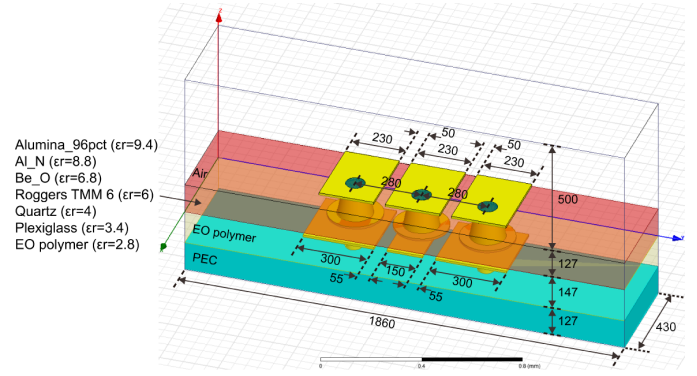


Fig. 6. Simulation structure of GSG via-throughs with various substrate materials for the RF interposer.

TABLE II. SUBSTRATE MATERIAL PARAMETERS.

Material	ϵ_r	$\tan\delta$	Conductivity (<i>siemens/m</i>)
<i>Alumina_96pct</i>	9.4	0.006	0
<i>Al_N</i>	8.8	0	0
<i>Be_O</i>	6.8	0	0
<i>Rogers TMM 6</i>	6	0	0
<i>Quartz</i>	4	0	0
<i>Plexiglass</i>	3.4	0.001	0
<i>EO polymer</i>	2.8	0.0004	0
<i>Silver epoxy</i>	1	0	5e4

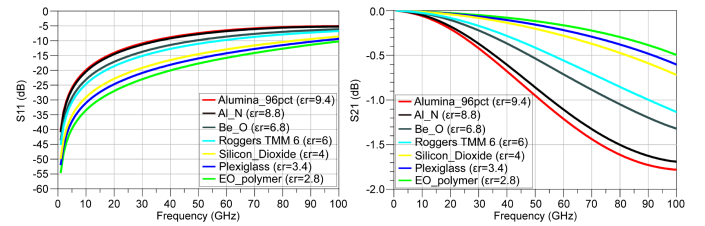


Fig. 7. Simulation results of via-through with various substrate materials for the RF interposer.

TMM 6, Silicon dioxide (*Quartz*), and Plexiglass. For comparison, a substrate material similar to EO polymer is also simulated. The electromagnetic material parameters of these substrate materials together with silver epoxy filling of the via-throughs are given in Table II.

The GSG via-throughs investigated in HFSS is shown in Fig.6. Each via-through consists of a conical shape with top and bottom radius of 50 μm and 75 μm , respectively, and filled with conductive silver epoxy. Besides, an annular ring of diameter 230 μm is placed at the bottom of the via-through structure due to the design rules from the manufacturer. The height of the substrate of the RF interposer is assumed to be 127 μm (5 mil). Fig.7 shows the simulation results for the via-throughs with different substrate materials of the RF interposer. In general, the materials with lower dielectric constant (ϵ_r) lead to better performances with larger bandwidth. Especially, the return loss remains better than 10 dB all the way up to 80 GHz for a quartz (SiO_2) substrate with an associated insertion loss of 0.5 dB. The improved performance using materials with lower dielectric constant is mainly due to the lower capacitive loading of the pad structures of the interposer and the modulator.

To elaborate further on this point, an equivalent circuit model, shown in Fig. 8, is identified for the studied via-

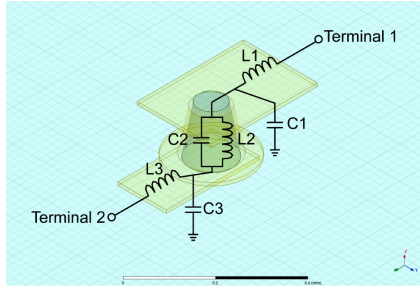


Fig. 8. Equivalent circuit model for via-through transition.

TABLE III. EXTRACTED EQUIVALENT CIRCUIT PARAMETERS FOR ALUMINA AND QUARTZ SUBSTRATES.

Alumina					
$L1$	$L2$	$L3$	$C1$	$C2$	$C3$
27.5 pH	55.5 pH	42.9 pH	40.4 fF	2.4 fF	73.1 fF
Quartz					
$L1$	$L2$	$L3$	$C1$	$C2$	$C3$
27.5 pH	55.5 pH	42.9 pH	28.6 fF	2.4 fF	45.7 fF

through transition. Table III gives the extracted equivalent circuit elements for the via-through transition based on alumina and quartz substrates. It can be seen that the capacitances loading the RF circuitry on the interposer and the pads of the modulator are significantly reduced with the quartz substrate. As expected the inductance of the via-through transition is not influenced by the choice of interposer substrate material.

C. Wire Bonding Transitions

Fig. 9 shows the wire bonding transitions between the driving and RF circuitry on the interposer. As the driving and RF circuitry locate on the same horizontal plane, there is no height difference between the two sides of the wire bonding transitions. The height and length of the wire bonding are $50\ \mu\text{m}$ and $200\ \mu\text{m}$, respectively. The diameter of the wire bonding is $20\ \mu\text{m}$ and the material is gold. In order to reduce the inductive discontinuity, three wire bonding transitions are used to connect each pad of the driving circuitry to the corresponding trace on the interposer. The gap between the InP and quartz substrates is $50\ \mu\text{m}$. The wire bonding transitions are simulated up to 150 GHz. As is shown in Fig. 10, the return loss remains better than 10 dB up to 100 GHz with an associated insertion loss of 0.8 dB. Based on this analysis it is believed that the wire bonding transitions between the driving and RF circuitry will not be a significant limiting factor in order to meet the bandwidth requirement.

III. METHODOLOGY FOR 3D HYBRID INTEGRATION

A. Design and EM Simulation of the Full Circuitry

In Section II, the properties of the RF circuitry, via-throughs, and wire bonding transitions are explained. Based on these investigations and the dimensions of the modulator, the full circuitry is designed as shown in Fig. 11. As it can be seen, the modulator supports four signal channels and each channel has two signal traces which can be used for a differential signal pair or two single-ended signals. Each signal channel has two input signal pads and three ground pads which together form a GSGSG structure. The dimensions

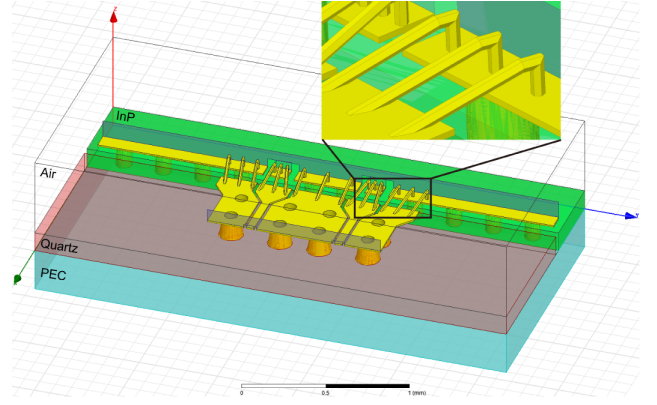


Fig. 9. Wire bonding transitions between the driving and RF circuitry.

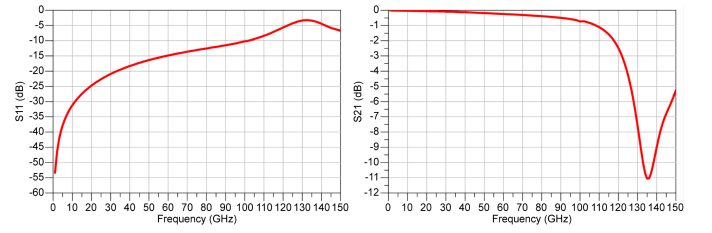


Fig. 10. Simulation results of wire bonding transitions.

of the input pads of the modulator and the via-throughs are demonstrated in Fig. 6. For a better performance at high frequency, the annular ring at the bottom is removed and the corners of the pads are rounded. The wire bonding transitions between the driving and RF circuitry are the same as is shown in Fig. 9. The RF circuitry on the interposer is based on the CCPW structure with ground vias distributing along the ground traces. According to the requirements, ground vias are not allowed in the area of EO polyboard. The CCPW lines are designed to have characteristic impedance of $50\ \Omega$ based on quartz substrate. At each end of the CCPW lines, the signal traces are tapered out to meet the dimensions of the via-throughs and wire bonding transitions. Based on the modulator, the RF circuitry is designed to support different signal channels and the challenge is to keep the signals in phase when they are transmitted through different traces. As a result, the signal traces are carefully designed to have the same physical path length which guarantees their phase balance. Due to the symmetrical structure of the modulator, signal traces S1, S2, S3, S4 are the same as signal traces S5, S6, S7, S8, respectively.

The EM simulation of the full circuitry is based on vertical lumped ports with PEC ground bridges. Driven terminal with network analysis is selected to be the solution type. The mesh and simulation frequencies are both 100 GHz. Fig. 12 shows the simulation results for all signal traces. The return loss is better than 10 dB for all signal traces up to 85 GHz. The insertion loss for signal traces S1, S2, S5, S6 is less than 2.5 dB up to 100 GHz while it is less than 3 dB up to 95 GHz for the rest signal traces. According to previous analysis, the high level return loss of the full circuitry is caused by the via-throughs. The notches on the signal traces S3, S4, S7, S8 are related to lacking of ground vias.

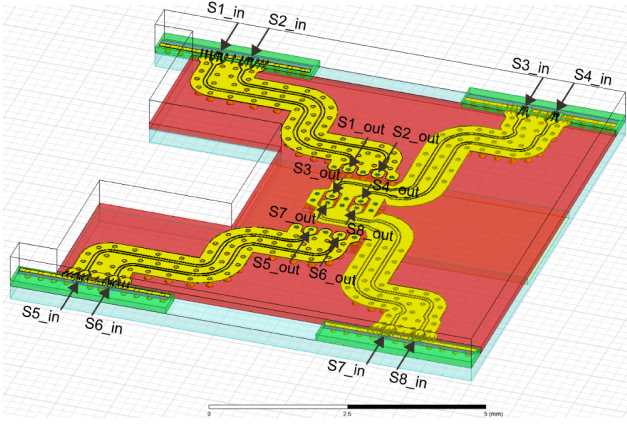


Fig. 11. Designed full circuitry of the transmitter.

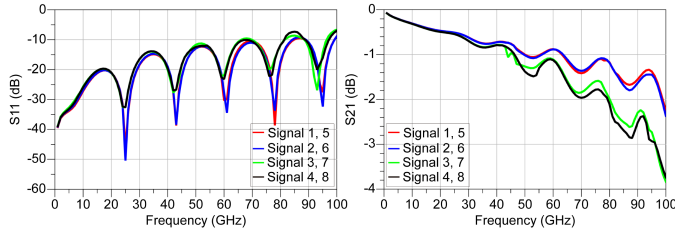


Fig. 12. Simulation results of the full circuitry.

B. Thermal Simulation of the Subassembly

A simplified subassembly of the packaged transmitter module is shown in Fig. 13. The proposed structure, containing the full circuitry, sub-mount, and heat sink layer, is imported into ANSYS Mechanical for steady-state thermal analysis. The full circuitry consists of four InP double-heterojunction bipolar transistor (DHBT) based drivers and each generates 3 W of heat which is specified as a volume power density of $3.4722e9 \text{ W/m}^3$. In the thermal simulation only the heat generated from the drivers are considered. The environment of the subassembly is natural air and the heat transfer coefficient is set to be $10 \text{ W/(m}^2 \cdot ^\circ\text{C)}$. The simulated steady-state temperature profile is shown in Fig. 13. The highest temperature of the packaged transmitter module is 74°C when the material of the sub-mount and heat sink layer is CuW. This should be acceptable with respect to the performance of the driving electronics.

IV. CONCLUSION

A 3D hybrid integration methodology for terabit transceivers has been presented. The fundamental properties and modeling methodology of the CCPW structure on the interposer were described. The placement of ground vias along the ground traces of the CCPW structure proved the necessity to guarantee resonance-free behaviour of the RF circuitry up to 100 GHz. The bandwidth of the via-through was shown to be limited if alumina was used as the interposer substrate material. Changing the substrate material to quartz was shown to increase the bandwidth of the via-through to well over 100 GHz. An equivalent circuit model of the via-through was proposed and the extracted lumped element parameters were shown. Besides, It was shown that the transitions from the drivers to RF circuitry can be performed with multiple wire

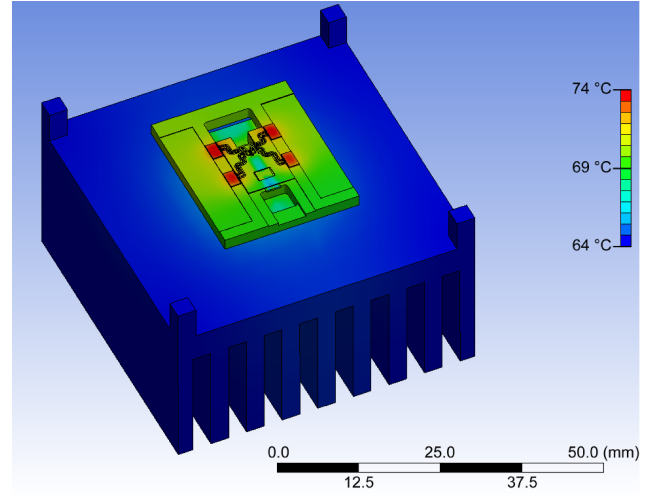


Fig. 13. Simulated temperature profile in subassembly.

bonding connections without significant bandwidth penalty up to 100 GHz. The full circuitry of the interposer has been designed. It was shown that the transmission bandwidth of the optimized circuitry could reach 95 GHz. This should be sufficient to support the targeted 64 Gbaud operation rate. The thermal analysis of the subassembly for the packaged transmitter module has been performed in ANSYS Mechanical. A maximum temperature of 74°C was predicted when CuW was used as the material of the sub-mount and heat sink layer.

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