Advances in PV Inverters

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Abstract

Renewable energies have experienced a significant growth and importance in the last two decades, of which energy from photovoltaic plants are a major contributor. Since solar cells have low efficiencies themselves, however, the necessity of high efficiency power converters at low cost and preferably low complexity leads to new research demands. This is especially true in the field of low cost residential PV inverters where efficiencies are used as major selling arguments. Traditional converter topologies equipped with conventional Silicon based semiconductors to date reach their limitations and new approaches are necessary. Therefore, research areas typically focus on both new topologies and utilizing more advanced semiconductor devices.

To this end, semiconductor devices made of Silicon Carbide have been gaining increasing interest in the last two decades after the successful commercialization of high voltage power diodes. By now, the performance potential of switching devices made of Silicon Carbide is commonly accepted, though they have not found commonplace usage within commercial converter systems for several reasons, among others reliability, availability/cost and gate driver complexity. Therefore, more complex Silicon based converters can be used instead to achieve lower semiconductor losses.

While there is no absolute solution in which direction to go to achieve the aforementioned design goals, this dissertation will thoroughly investigate two potential approaches and discuss their trade-offs.

The contributions are:

- Comprehensive loss analysis and identification of major loss contributors within T-Type converter topology operating in inverter and rectifier context.
- Evaluation of the use and loss benefits of Silicon Carbide switching devices in the T-Type structure.
- Thorough investigation of the Hybrid-Neutral-Point-Clamped (Hybrid-NPC) topology as an alternative for the Silicon Carbide based T-Type converter.
- Alternative methodology of semiconductor loss model validation by experimental means.

As to the advanced three-level T-Type converter topology, its unusual operation

mode is thoroughly described identifying its limitations for high efficiency operation. With these results, the first approach utilizes low loss switching devices and their influence on the semiconductor loss behavior is analyzed. The results show that, for near unity power factor operation, a replacement of only two switching devices per phase leg can greatly reduce the semiconductor losses.

The Hybrid-NPC converter can be seen as an attractive and cost competitive alternative to the Silicon Carbide based converter, also allowing to overcome the major drawbacks with the conventional Silicon IGBT based T-Type structure.

Both alternatives are based on a semiconductor/topological level and thus this is where the loss reduction occurs. The difficulty in experimentally evaluating only the semiconductor losses within a converter operating context is addressed in this work by presenting an alternative measurement approach. Using known heat loads, and a careful calibration procedure on the device heat sink, analytically obtained semiconductor loss models based on datasheet information and in-circuit switching transitions measurements can be experimentally verified and thus a fair performance comparison between two approaches is enabled.

Resumé

Vedvarende energi har oplevet en markant vækst og betydning i de sidste to årtier, hvoraf energi fra solcelleanlæg er en stor bidragyder. Idet solcellerne har lav effektivitet og efterspørgslen af højeffektive konverter med lave omkostninger og fortrinsvis lav kompleksitet er stigende, medfører dette nye forskningskrav. Dette er især tilfældet inden for billige solcellekonvertere til boliger, hvor effektiviteten anvendes som et større salgsargument. Traditionelle konverter-topologier har til dato nået deres begrænsninger og nye løsninger er nødvendige. Derfor har forskningsområderne typisk fokus på både nye topologier og anvendelse af mere avancerede halvledere.

Til dette formål har halvlederkomponenter lavet af siliciumkarbid (SiC) vundet stigende interesse i de sidste to årtier efter den vellykkede kommercialisering af SiC-højspændingsdioder. På nuværende tidspunkt, er halvledere fremstillet af SiC almindeligt accepteret, selv om SiC halvledere af flere grunde ikke er almindelige i kommercielle konverter systemer. Dette begrundes i deres upålidelighed, tilgængelighed / omkostninger og gate driver kompleksitet. Derfor kan mere komplekse konvertere være et attraktivt alternative til opnå et mindre tab.

Der er ingen absolut løsning for i hvilken retning man skal gå for at opnå de førnævnte designmål. Denne afhandling indeholder en grundig undersøgelse af to potentielle muligheder og diskutere deres fordele og ulemper. De forskningsmæssige bidrag er:

- Omfattende tabsanalyse og identifikation af de store tabsbidrag indenfor T-Type inverter og ensretter-drift konteksten
- Evaluering af brugen af og tabsfordelene ved SiC-halvledere i T-Type konverter
- Grundig undersøgelse af Hybrid-Neutral-Point-Clamped (NPC) som et alternativ til SiC-baserede T-Type konverter
- Præsentation af en alternativ metode til at måle halvlederes tab

T-Type konverterens usædvanlige driftstilstand vil blive beskrevet, hvormed begrænsningerne for høj effektivitet er identificeret. Disse resultater bruges til at undersøge anvendelse af halvledere lavet af SiC og deres tab i T-Type konverteren.

Resultaterne viser, at når effektfaktoren er tæt på én, er det kun nødvendigt at udskifte to halvledere til SiC. Hybrid-NPC konverteren kan ses som et attraktiv og effektivt konkurrencedygtigt alternativ til SiC T-Type konverteren. Hybrid-NPC konverteren gør det også muligt at overvinde de store ulemper med den konventionelle silicium (Si) IGBT-baserede T-Type konverter. Begge alternativer er baseret på et halvleder / topologisk grundlag, og det er her at tabet reduceres. Vanskeligheden i at måle tab i halvlederne i de forskellige T-Typer konvertere bliver diskuteret og et alternativt måleprincip er præsenteret. Ved brug af kendte varmebelastninger og en præcis kalibreringsprocedure på halvlederens køleplade, bliver det muligt at validere halvledernes tabsmodeller med målinger. Dermed er en fair sammenligning imellem de to løsninger mulig.

Preface

This PhD project *Advances in PV Inverters* is part of the Intelligent Efficient Power Electronics (IEPE) research program, in which Danish universities and companies collaborate to achieve more sophisticated power electronic systems. It gave me the chance to explore and extend my knowledge within power electronics in photovoltaic inverters and to participate in interesting and challenging dialogues with experts in this field.

My deepest gratitude is to my supervisors Michael A. E. Andersen and Zhe Zhang at the Department of Electrical Engineering, Technical University of Denmark, who gave me the opportunity to conduct the PhD project at the Electronics Group of DTU. I further appreciate their support and their consistent encouragement that helped me finish this project.

I am very thankful to be part of this excellent work environment and I would like to gratefully and sincerely thank all my friends and colleagues in the Electronics Group at DTU. I would like to give my special appreciation to Pere, Juan and Maria, Gabriel and Kristian for the enjoyable time in the department as well as during conferences. Last but not least, I would like to thank our group secretary Henriette, our former engineer assistant Bertil and our current engineer assistant Hans-Christian.

I am thankful to Professor Grahame Holmes and Associate Professor Brendan McGrath for accepting me as a visiting student at their Power and Energy Research Group at RMIT University in Melbourne, Australia, and deep gratitude goes to Dr. Carlos Teixeira for the very supportive help during the laboratory work.

Finally, I would like to thank my family and friends for their support and encouragement, and their love, which helped me go through this kind of work.

Contents

Acronyms

AC Alternating Current

ANPC Active Neutral-Point-Clamped

BSNPC Bipolar-Switched-Neutral-Point-Clamped

CM Common Mode

DC Direct Current

DPT Double Pulse Test

DPWM Discontinuous Pulse Width Modulation

EMC Electromagnetic Compability

EMI Electromagnetic Interference

EV Electric Vehicle

FC Flying Capacitor

FEM Finite Element Method

FIT Feed-in Tariff

GaN Gallium Nitride

IGBT Insulated-Gate-Bipolar-Transistor

NPC Neutral-Point-Clamped

PD Phase Disposition

PV Photovoltaic

RMS Root Mean Square

Si Silicon

SiC Silicon Carbide

SPWM Sine Pulse Width Modulation

SVM Space Vector Modulation

VSC Voltage Source Converter

VSD Variable Speed Drive

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Chapter 1

Introduction

1.1 Scope

This thesis presents the results achieved throughout the PhD project entitled *Advances in PV Inverters* which has been carried out by the author from November 2012 until October 2015. The research outcome has been presented or submitted in form of peer reviewed conference and journal papers. These papers build the basic structure of this thesis and are therefore included in the appendix. This dissertation gives more elaborated insights on the already published information, and thereby presents a more coherent and complete analysis of the research topics in this work. Furthermore, this thesis including its appendix contains a large amount of advanced knowledge on the analysis, design and performance evaluation associated with advanced multilevel inverters and their semiconductor loss profiles.

1.2 Motivation

The integration of renewable energy generation in our society has undergone a tremendous development in the last two decades and is still ongoing. In 2012, a contribution of 19 % from renewable energies was estimated [1]. Looking at the growth rate, energy coming from Photovoltaic (PV) experiences a significant importance within renewable energies with a record year in 2013 [1]. With 39 GW added in 2013, PV energy reached a total global capacity of 139 GW. The growth of installed PV generation is demonstrated in Fig. 1.1 [1].
The installation of PV in the residential sector has several advantages over other renewable energy resources such as smaller size compared to wind farms, and consequently cost. The high Feed-in Tariff (FIT) in some countries (Germany for instance) further strengthened the attractiveness of PV. Related to the high amount of PV installations (as well as other distributed renewable energy sources), an ongoing development from conventional standalone systems towards systems including energy storage units [2] which can be used for self consumption or grid support becomes more and more attractive. Nevertheless, all solutions have in common

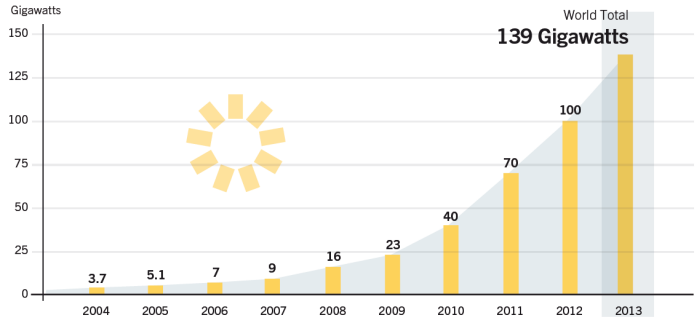


Figure 1.1: Global PV capacity

to have major demand for proper and high efficient grid-connection because solar cells are reported to have low efficiencies themselves (typically in the range of up to 20 % [3]). Therefore, loss reduction and thus high efficiencies of the power converters become major design goals for low cost PV systems. To this end, commercial power converters for residential PV systems can show high efficiencies in the range of 98 % [4]. Since efficiency is a major selling argument (keeping in mind that the customer receives money for feeding energy to the grid), a competition of very high efficiencies is still ongoing.

Using next generation semiconductor devices made of Silicon Carbide (SiC), efficiencies for PV inverters of over 99 % are reported [4]. Such advanced switching devices, however, are still in an ongoing development stage and thus cost expensive, so that they have not found commonplace usage within commercial systems. The majority of publications on the utilization of SiC shows the benefits of reduced losses, but are rarely covering the topic cost, which are a major design constraint as well. This PhD project will therefore investigate possible alternatives to achieve high efficiency power converters and discusses them against the converter design constraints complexity and cost.

1.3 Project objectives

Based on the aforementioned demand for high efficient power converters, the aim of this project is to identify current limitations within high efficiency power conversion in PV inverters, and to thoroughly investigate possibilities to overcome these. This thesis focuses on the investigation on a semiconductor and a topological level as this is where a major loss contribution within electrical power conversion is typically found. The benefits of achieving high efficiency in two possible ways will be discussed against their design trade-offs such as increased complexity and cost. This thesis will not intend to follow an optimization routine that results in the highest possible efficiency as this topic is well established and typically includes an overall converter design covering input filters, topologies, semiconductors, output filters, modulation strategies and control, and cannot be covered in a single PhD project alone.

The main objectives in this project are therefore:

- to accurately identify major loss contributors and limitations for high efficiencies in a commonly used PV inverter topology for given operating points,
- to investigate the utilization of new semiconductor power devices within PV inverter operation context,
- to investigate the approach of a more complex but promising topology as an alternative to SiC based converters.

This thesis, however, does not cover:

- EMC filtering
- AC filtering
- Magnetic design
- Control and modulation related issues

1.4 Structure

Fig. 1.2 demonstrates the outline of this dissertation and how each publication relates to the key parts of the project. More elaborated, Chap. 2 gives an overview of current practices within PV systems based on previous work that has been carried out on both a topological point of view and on a semiconductor level. From this point, a tendency is drawn to which this dissertation can give an update and hence contribute.

A thorough elaboration on the state-of-the-art work on a topological level is given in Chap. 3, in which the advantages and drawbacks of two commonly used topologies are compared against each other. The conclusion from this chapter will lead to the starting point of Chap. 4 which represents the main work carried out in this PhD, i.e. thoroughly demonstrating design considerations on how efficiency improvements can be achieved and to accurately validate the proposed approaches through measurements. This chapter ends with a discussion on both solutions including the cost factor. The consequences of loss reduction will be introduced in Chap. 5 in terms of possible design alternatives, which directly leads to the conclusions and recommendations for future work, presented in Chap. 7.

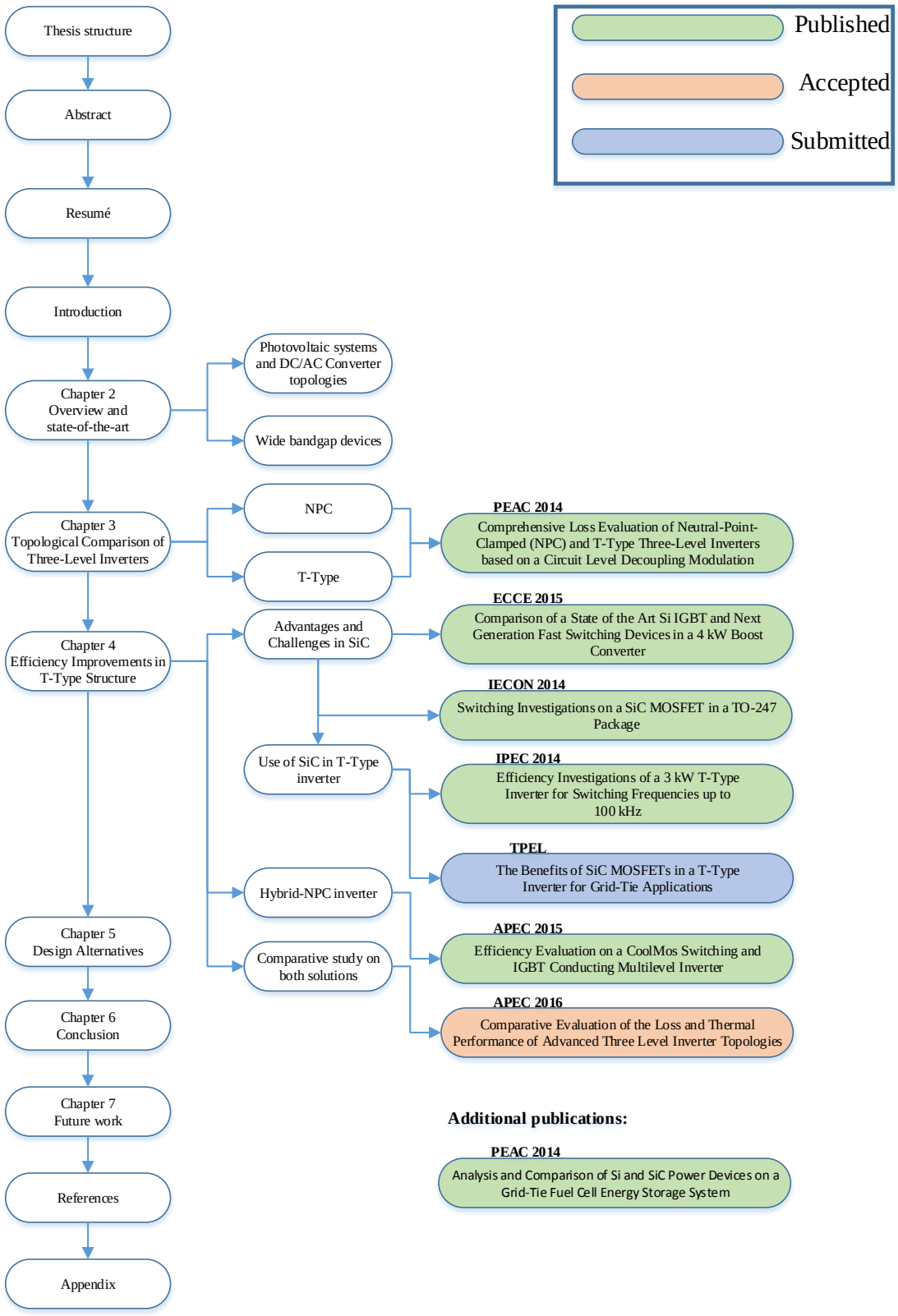


Figure 1.2: Thesis outline

Chapter 2

Overview and state-of-the-art

2.1 Photovoltaic systems and DC/AC converter topologies

Based on the increased interest in PV systems explained in Sec. 1.2, strong research is conducted in several fields within PV, starting from increasing efficiencies in PV modules towards the full integration of complete systems. The integration of a PV system depends on its power rating, as demonstrated in Fig. 2.1 [5].

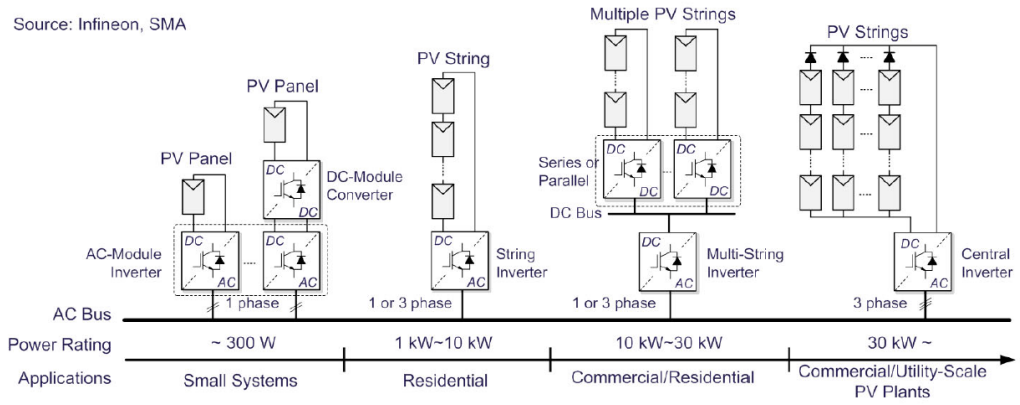


Figure 2.1: PV systems for different power levels

All configurations in Fig. 2.1 have in common to convert the electrical Direct Current (DC) power from the PV modules into Alternating Current (AC) power to comply with the grid specifications, e.g. 230 V/400 V, 50 Hz in most European countries. That conversion stage has been under intensive research within the last decades and can be grouped into two parts, i.e. transformer based and transformer-less systems [6]. Where transformer based systems have the particular advantage in their safety structures due to the galvanic isolation between the grid and the PV side, transformer-less systems can achieve higher efficiencies and higher power

densities at lower cost due to the absence of the transformer. However, a boost stage placed between the PV panels and the DC/AC converter is then necessary to ensure a DC link voltage large enough to achieve the required grid specifications. A block diagram of a typical transformer-less PV system is shown in Fig. 2.2.

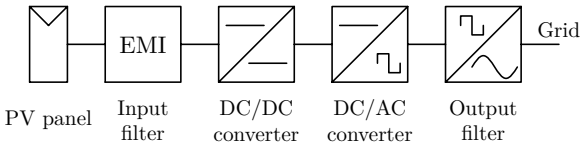


Figure 2.2: Block diagram of a transformer-less PV system

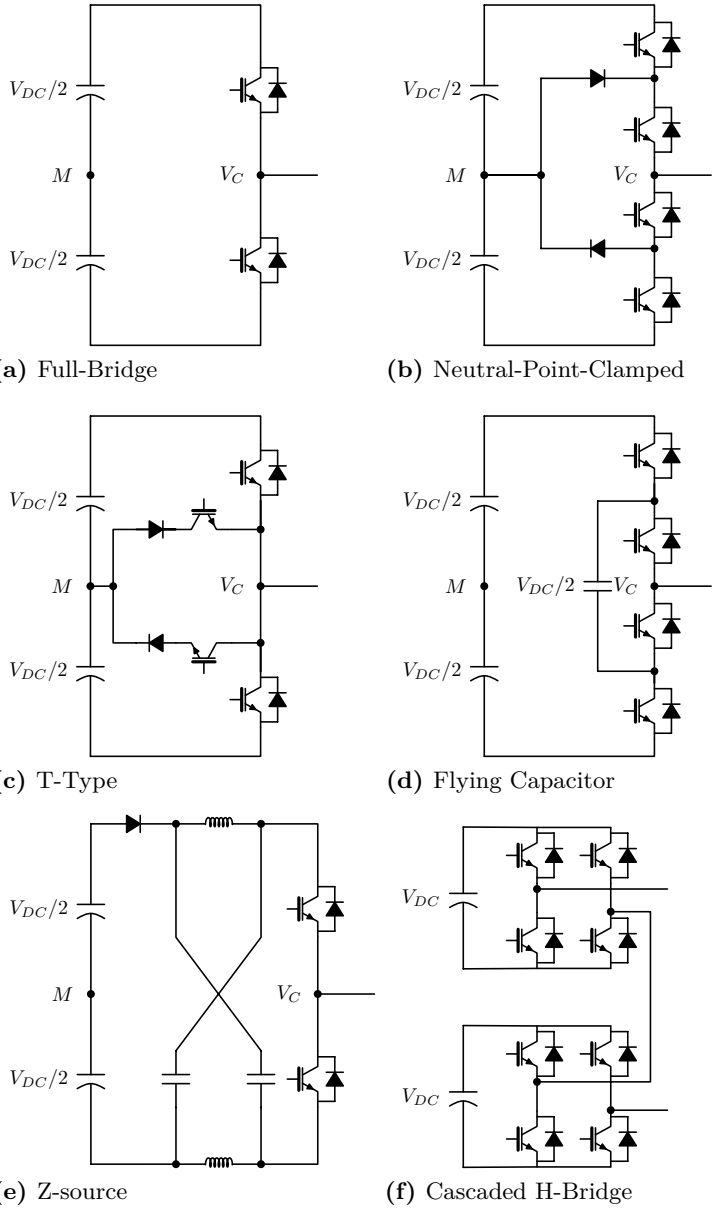
In recent years, safety regulations for grid-connected residential systems have been lowered such that a clear tendency is observed favoring transformer-less systems and thus accepting the additional DC/DC converter stage [7]. To this end, various studies have compared topologies against each other to further improve the integration of PV. Despite the various topological alternatives available to obtain the desired AC output, this work lists the most commonly used configurations within the prospect of PV application found in the literature.

The most mature configuration is the three-phase Full-Bridge topology. It is a two-level alternative meaning that the switched converter output terminals can achieve two defined voltage potentials. In contrast to the two-level inverter, multilevel inverter topologies can achieve staircase voltages on their output terminals. This kind of topology has been introduced in [8] in 1975 and has gained increasing interest ever since [9, 10], of which the minimum voltage levels are categorized as three-level topologies [9], which can then go up to n-level inverters. With an infinite number of levels, i.e. $n \to \infty$, the voltage at the output terminals will be a pure sinusoid and no filtering will be necessary [9,11], clearly at the expense of an infinite number of semiconductor devices.

Therefore, extensive research has been carried out in the past comparing two- and multilevel topologies against each other and it is found out that the choice of topology strongly depends on the given application. For PV systems, the following topologies have found major interest in the literature, of which one phase leg for each topology is shown in Fig. 2.3:

- The three-phase Full-Bridge structure [12], Fig. 2.3a
- The Neutral-Point-Clamped (NPC) structure [13, 14], Fig. 2.3b
- The T-Type structure [15] (known as Bipolar-Switched-Neutral-Point-Clamped (BSNPC) [16] or Conergy [17]), Fig. 2.3c
- The Flying Capacitor (FC) [18, 19], Fig. 2.3d
- The Z-source converter [20], Fig. 2.3e
- The cascaded H-Bridge [8], Fig. 2.3f

The last configuration in this list needs an individual DC source for each H-Bridge and is therefore only an interesting choice for medium and large scale PV systems [21, 22] rather than residential low cost PV systems. Hence it is not further



(a) Full-Bridge **(b)** Neutral-Point-Clamped

(c) T-Type **(d)** Flying Capacitor

(e) Z-source **(f)** Cascaded H-Bridge

Figure 2.3: One phase leg of each suitable topology. In (a) the Full-Bridge inverter, in (b) the NPC inverter, in (c) the T-Type inverter, in (d) the Flying Capacitor inverter, in (e) the Z-source inverter and in (f) the cascaded H-Bridge

included in this overview. A major advantage of multilevel inverters is that the semiconductor devices are commutating with only part of the DC link voltage. For instance, in a three-level inverter, each switching device switches only half the DC link voltage whereas in a conventional two-level inverter, each switching device switches the full DC link voltage. This directly leads to reduced switching losses for the three-level inverter at any given switching frequency. Nevertheless, total semiconductor losses in a two-level inverter can still be lower compared to a three-level inverter if the switching frequency is low enough. Hence, the operating condition becomes a crucial aspect when comparing topologies.

For instance, in [23], the two-level and the three-level NPC converter have been

compared against each other in terms of semiconductor losses, filter aspects, reliability and cost. It is found out that the staircase voltage at the NPC converter output terminals and hence the reduced harmonic content directly lead to a smaller AC filter size for a given operating condition. The size reduction in the AC filter and the lower heat sink requirements for a three-level inverter (due to the reduced switching losses) can lead to an equally expensive or an even cheaper PV inverter despite the fact that the semiconductor count is higher.

A similar comparison has been carried out in [24], in which a two-level inverter has been evaluated against the three-level NPC and the three-level T-Type inverters. The T-Type structure is a derivation of the NPC achieving the same output performance at reduced semiconductor count [10, 17]. Instead of cost as a comparison parameter, [24] uses the area chip size as a cost indicator. With similar results as in [23], three-level inverters can outperform the two-level inverter at increased switching frequencies, not only in losses but also in price. For residential PV systems, the switching frequency is usually set between 16 kHz and 48 kHz [4] with around 20 kHz as a good compromise between switching losses and filter size.

In [12], two-level and three-level inverter constellations have been evaluated based on their leakage currents, which is a major concern in transformer-less PV systems, and have found out that the Common Mode (CM) voltage is larger for the Full-Bridge structure compared to the NPC. This consequently results in larger leakage currents.

Within the three-level converter topologies, as pointed out in [24], the three-level T-Type structure achieves lower semiconductor losses compared to its NPC alternative at low to medium switching frequencies (approx. 20 kHz). That is because the NPC converter has relatively large conduction losses as always two semiconductor devices conduct the load current [25] (an elaboration on that is given in Chap. 3). This leads to an uneven loss distribution and consequently to an uneven thermal stress among the semiconductor devices [26]. While this can be overcome in an Active Neutral-Point-Clamped (ANPC) [27], in which the clamping diodes are replaced by switching elements, such solution clearly adds complexity to the circuitry and control. Above a certain switching frequency, the T-Type inverter shows higher total semiconductor losses compared to the NPC due to the relatively large switching losses in the outer DC bus connecting switches (S_1 and S_4 in Fig. 3.3a).

The topological comparison has been extended in [20, 28, 29] evaluating transformer-less inverter topologies including the Z-source structure from Fig. 2.3e, which has the particular benefit of having a boost stage without any additional switching elements. However, this solution has been commonly found to achieve lower efficiencies than the NPC including a separate boost state. The Flying Capacitor from Fig. 2.3d requires a more complex startup routine, extra capacitors and a proper voltage balancing scheme [23, 30, 31] and is therefore not commonly used for low-cost PV systems.

2.2 Wide bandgap devices

Apart from the topological investigation to achieve high efficiency power conversion, power losses in a converter can be reduced using low loss semiconductor devices. To this end, research interest not only tends to improve currently available Insulated-Gate-Bipolar-Transistors (IGBTs) made of Silicon (Si) to optimize their trade-offs between the saturation voltage and switching energies [32,33], but also to introduce wide-bandgap semiconductor devices. Especially devices made of SiC and Gallium Nitride (GaN) have been in the focus of high efficient power converters in grid-connected applications. Such devices were first commercially available with the introduction of SiC diodes in 2001. Their particular benefit is the absence of the reverse recovery current which not only lowers the switching losses in the diode itself, but also greatly reduces the turn-on switching losses of the commutating switching device [34–36]. The important properties of wide-bandgap material are listed in Table 2.1 [37].

Table 2.1: Properties of wide-bandgap materials

Properties	Si	GaN	4H-SiC
Bandgap, Eg (eV at 300 K)	1.12	3.4	3.2
Critical electric field Ec (V/cm)	$2.5 \cdot 10^5$	$3 \cdot 10^6$	$2.2 \cdot 10^6$
Thermal conductivity, λ (W/cmK at 300 K)	1.5	1.3	$3 - 4$
Electron mobility, μ_n (cm^2/Vs)	1350	1000	950
Dielectric constant, ε	11.9	9.5	10

The higher bandgap Eg is a very beneficial property since that directly relates to the on-resistance of the device, which is commonly used as a figure of merit within the comparison against Si. The specific on-resistance of a MOSFET can be calculated as [37]

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon \mu_n E_c^3} \quad , \tag{2.1}$$

where V_B is the breakdown voltage, ε the dielectric constant, μ_n the electron mobility and E_c the critical field strength. Eq. (2.1) illustrates the non-linear relationship between specific on-resistance and electric breakdown field which immediately demonstrates the superior performance of semiconductors made of wide-bandgap material. A comparison of Si, SiC and GaN is shown in Fig. 2.4 [38].

Thus, the use of SiC devices can be very attractive in order to keep conduction losses low. Not only are the new kind of devices attractive because of their possible lower conduction losses, also their high switching speeds are beneficial to reduce low switching losses. A common way to compare one device over another is by using simple Double Pulse Test (DPT) measurements, from which it is concluded that SiC switching devices offer performance benefits in terms of switching speed and hence switching losses can be greatly reduced compared to a state of the art Si IGBT [3, 39]. Such comparisons are extended to compare SiC switching devices in

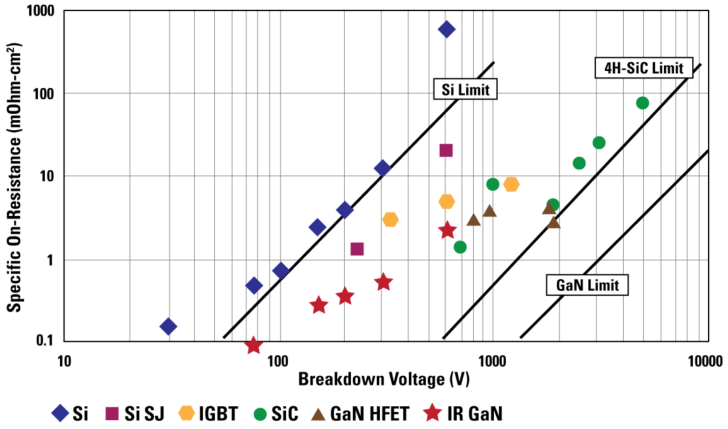


Figure 2.4: Specific on-state resistance comparison of Si, SiC and GaN

various applications. For instance, [40] demonstrates the potentials and challenges of SiC MOSFETs against Si IGBTs in a Variable Speed Drive (VSD), such as same overall converter losses at 50 kHz switching frequency for the SiC based system compared to the Si based system operating at 15 kHz. In [41], the utilization of SiC JFETs in Electric Vehicle (EV) is investigated and the energy consumption savings due to the higher efficiency are predicted.

The potential of SiC performance improvements within PV inverter context is explored in [3], in which the utilization of a SiC JFET in a two-level inverter is investigated and compared against a more complex three-level NPC inverter using conventional Si IGBTs, and has concluded that similar overall converter efficiencies can be achieved with the use of SiC. The analysis of the utilization of SiC in three-level inverters for PV systems is furthermore in some detail presented in [4, 42], in which efficiency curves of a commercially available PV inverter are shown.

The utilization of 650 V SiC MOSFETs and 1200 V SiC MOSFETs in a T-Type structure for PV inverters is demonstrated in [43], in which the feasibility of the intrinsic body-diode of such switching devices is investigated and concluded to be reliable. However, no detailed loss breakdown is shown to what extend the utilization of SiC switching devices in either the bi-directional or the vertical path of the T-Type structure can result in loss performance improvements.

While the majority of applications investigate the benefits of SiC such as reduced losses and high switching frequency operation, fewer publications are available that address the higher prices, which, to date, might be a strong argument for not utilizing such devices in commercial products. In the early introduction of SiC switching devices, [44] discussed the potential cost savings of PV inverters due to the reduction of inductive components (AC filter) for increased switching frequencies and cost reduction of the heat sink due to the higher operating temperature capabilities of SiC material paired with an increased annual benefit because of the loss reduction in the semiconductor devices. However, such gain is not compared against the increased initial cost due to the expensive SiC switching devices themselves. In [45], a time span of 15 years is predicted for a 2.5 kW DC/DC converter until the cost even point is reached with the SiC based system. A more recent approach in evaluating the cost benefits of SiC in power converters is presented in [46], in

which a 25 kHz Si boost converter is theoretically compared against a 100 kHz SiC based boost converter showing cost reductions due to the downsize of the inductor at increased switching frequencies, although no detailed analysis on the inductor itself is given (in particular if the same core material is used for 25 kHz and 100 kHz) and the comparison is based on an assumption that the SiC MOSFET is capable of operating reliable at high ambient temperatures, which then assumes a greatly reduced heat sink requirement. Another cost analysis is given in [47] predicting a relatively short payback time of around 2 years for the SiC based system. This is, however, under the assumption that a 5 kW converter operates 24 h a day at full load, which is obviously not applicable in the case of PV inverters.

2.3 Summary

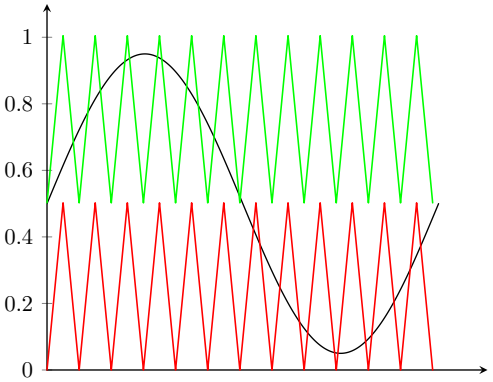
Based on the literature review given in this section, three-level topologies have found place in grid-connected applications due to their lower loss profile and the smaller AC filter size because of the lower harmonic content at the converter output terminals. The NPC inverter still seems to be an attractive choice for low cost PV systems even though it has been introduced over 30 years ago. That is mainly due to the high level of maturity and thus availability within semiconductor modules. However, it comes with the particular drawback that current must always flow through two semiconductor devices, which causes large conduction losses resulting in an uneven thermal stress among the semiconductor devices. At typical switching frequencies for residential PV systems, i.e. in the range of 20 kHz, the T-Type structure can achieve lower total semiconductor losses due to the reduced conduction losses. However, as the switching frequency increases, the T-Type structure will significantly increase the semiconductor losses and thus lower the efficiency compared to the NPC alternative.

To date, various publications on SiC can be found, including static and dynamic performance comparisons both standalone and demonstrating efficiency improvements in actual applications, while almost none of them address the cost factor. Instead, it seems that the higher price for SiC is simply accepted arguing that cost will automatically go down with mass production in the future. This leads to the generalized conclusion that SiC can greatly reduce losses compared to Si, although detailed loss breakdown analyses verified experimentally are often left out such that some applications may or may not inherently benefit from such new materials. Also, even several years after the introduction of SiC switching devices, no mass production is achieved yet and the factor cost may still be a design constraint when it comes to SiC based converter design.

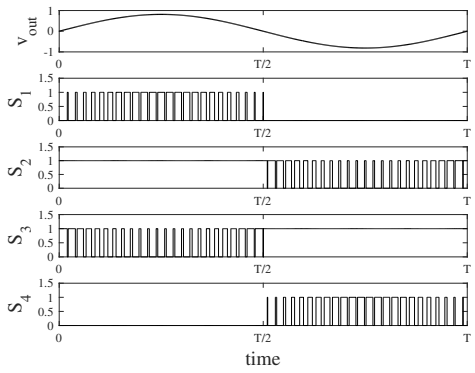
Chapter 3

Topological Comparison of Three-Level Converters

This chapter gives a more detailed comparison between two commonly used three-level inverter alternatives, namely the NPC and the T-Type inverter. Both topologies have in common to have a direct connection to the midpoint of the DC link and hence enable a three-level switched output voltage. One phase leg of each topology is depicted in Fig. 2.3b for the NPC and Fig. 2.3c for the T-Type alternative. Their main difference is the placement of the outer switches ($S_{1,4}$ in Fig. 3.3) which gives advantages on one side and disadvantages on the other. Before the analysis of both topologies is carried out, a brief introduction to the modulation principle is given. With several possible modulation strategies available for three-level inverters such as Space Vector Modulation (SVM) or Sine Pulse Width Modulation (SPWM), Phase Disposition (PD) PWM is applied which is found to be the optimum modulation strategy for these topologies [48, 49]. The basic principle for PD PWM is illustrated in Fig. 3.1a and can be applied to either the NPC or T-Type topology. The switching states from Fig. 3.1b are detailed in Table 3.1.



(a) Carrier based representation of PD PWM



(b) Principle of PD PWM with low carrier to fundamental ratio

Figure 3.1: Phase Disposition (PD) PWM as the chosen modulation principle

Table 3.1: Switching states for NPC and T-Type converters

Output voltage	S_1	S_2	S_3	S_4
$V_{DC}/2$	1	1	0	0
0	0	1	1	0
$-V_{DC}/2$	0	0	1	1

The modulation strategy will be explained on both the T-Type and the NPC structures and unity power factor is assumed for simplicity reasons, i.e. $cos\,(\varphi) = 1$. For clarification, the phase displacement φ describes to what degree the output voltage $v_{out}(t)$ and output current $i_{out}(t)$ are out of phase, illustrated in Fig. 3.2, and thus defines the amount of active and reactive power exchange according to

$$P_{out} = V_{out} I_{out} cos\,(\varphi) \qquad , \tag{3.1}$$

where V_{out} and I_{out} are the Root Mean Square (RMS) values of $v_{out}(t)$ and $i_{out}(t)$. Pure active power exchange is defined if voltage and current are in phase, i.e. $\varphi = 0°$, and the power factor $cos(\varphi)$ thus becomes $cos(0°) = 1$. Pure reactive power exchange occurs at $\varphi = 90°$ with a power factor of $cos(90°) = 0$.

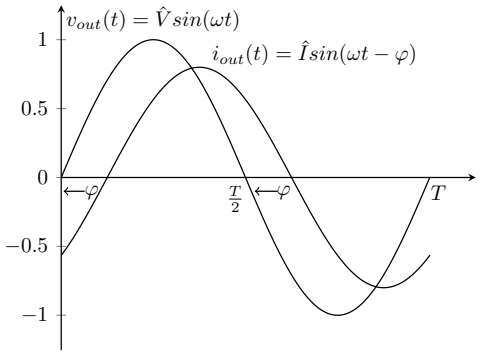
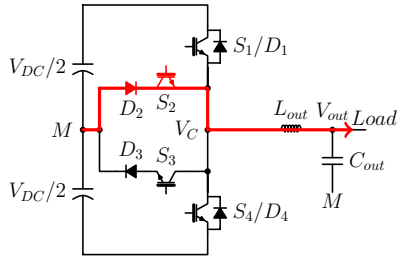


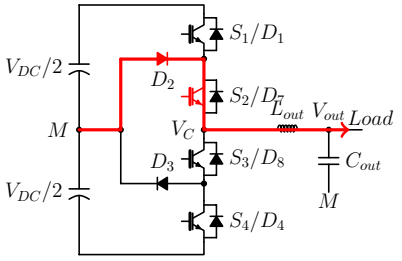
Figure 3.2: Output voltage and output current

The commutation states for both topologies are illustrated in Fig. 3.3. As an initial state, the load current is positive (representing the time interval from $t = [0..T/2]$ in Fig. 3.1b) and the converter output voltage V_c is zero, also called as zero output voltage. The current for both topologies flows through diode D_2 and S_2 towards the load. To achieve a positive output voltage, switch S_1 turns on and current commutates from D_2 to S_1 causing switching losses in S_1. Note that this statement is true for both the T-Type and the NPC converters.

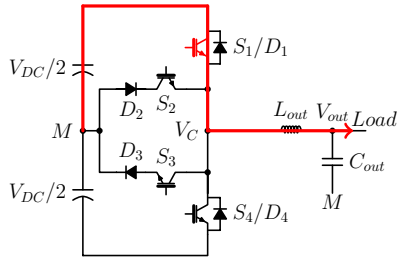
For a positive output voltage, current will flow through S_1 only in the T-Type constellation (Fig. 3.3c) whilst flowing through both S_1 and S_2 in the NPC alternative (Fig. 3.3d). When the load current is negative (during $t = [T/2..T]$) and the converter output voltage is zero, current flows from the load to the midpoint of the DC link through S_3 and D_3. To achieve a negative output voltage, switch S_4 turns on as depicted in Fig. 3.3g and Fig. 3.3h. The current paths for the T-Type and the NPC alternatives follow the same principle as for a positive output voltage, now only through S_4 in the T-Type structure against S_3 and S_4 in the NPC constellation. This clearly shows that current will always flow through two semiconductor



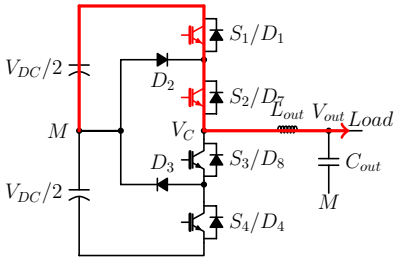
(a) Zero output voltage and positive output current. S_1 turned off, S_2 turned on



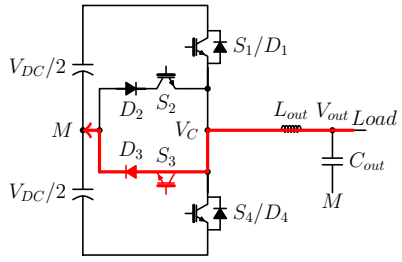
(b) Zero output voltage and positive output current. S_1 turned off, S_2 turned on



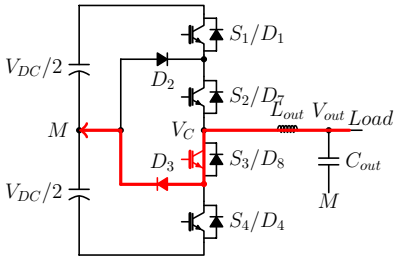
(c) Positive output voltage and positive output current. S_1 turned on



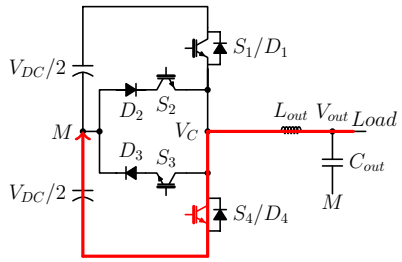
(d) Positive output voltage and positive output current. S_1 turned on



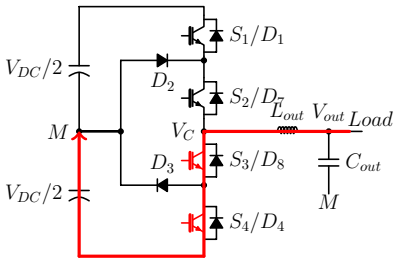
(e) Zero output voltage and negative output current. S_4 turned off, S_3 turned on



(f) Zero output voltage and negative output current. S_4 turned off, S_3 turned on



(g) Negative output voltage and negative output current. S_4 turned on



(h) Negative output voltage and negative output current. S_4 turned on

Figure 3.3: Switching states for T-Type inverter (left-hand side) and NPC inverter (right-hand side) operating at unity power factor

devices for the commonly used NPC in each switch constellation whereas current will only flow through two semiconductor devices when the T-Type topology is in its zero output voltage. This fundamental difference can achieve a reduction in conduction losses for the T-Type alternative.

3.1 NPC converter

The NPC topology is depicted in Fig. 2.3b and comprises of a DC link bus with split bulk capacitors, four switching devices and six diodes. The particular benefit of the NPC topology is that it can be realized with semiconductor devices that need to block half the DC link voltage only. This means that for the NPC topology, semiconductor devices can be chosen with a breakdown voltage half of the semiconductor devices that are utilized in a two-level topology, which can hence greatly reduce the switching losses for the NPC structure [23]. Its drawback, however, is that current will always flow through two semiconductor devices with associated conduction losses.

3.2 T-Type converter

The T-Type inverter is a derivation of the NPC inverter that aims to reduce its relatively large conduction losses. This is done by rearranging the outer switches $S_{1,4}$ as shown in Fig. 3.3. The result is that switches $S_{2,3}$ only conduct current at a zero output voltage on the converter output terminal. The conduction intervals for $S_{1,4}$ remain the same. This rearrangement of the outer switching devices can also reduce the semiconductor device count, now four switching devices and four diodes per phase leg only, which is two diodes less compared to the NPC alternative. The rearrangement, however, has the particular disadvantage that the outer switches in the T-Type alternative ($S_{1,4}$) now need to be able to block the full DC link voltage, despite the fact that the commutating voltage is only at half the DC link. This unusual operation mode of the T-Type structure indicates that the DC bus connecting devices need to be chosen to have breakdown voltages at the full DC link voltage, which then leads to increased switching losses compared to the NPC converter.

3.3 Efficiency comparison

As pointed out in [23], semiconductor devices with higher breakdown voltages suffer from larger conduction and switching losses compared to devices rated at lower breakdown voltages. It is then investigated in [24,50], that the switching frequency becomes a critical parameter when comparing the NPC and T-Type structures and have found that the T-Type alternative has superior loss performance particularly at lower operating frequencies. As the switching frequency increases, however, switching losses in the DC bus connecting switches in the T-Type structure become dominant, hence decreasing the overall converter efficiency. While switching losses can generally be reduced using loss optimized PWM strategies such as Discontinuous Pulse Width Modulation (DPWM) [15, 50, 51], a trade-off is usually made against other criteria (e.g. increased harmonic content for DPWM [11, 52]). Another alternative is to replace the Si diodes in the inner bi-directional path with SiC diodes to reduce reverse recovery losses [53]. An All-SiC T-Type inverter is demonstrated in [43].

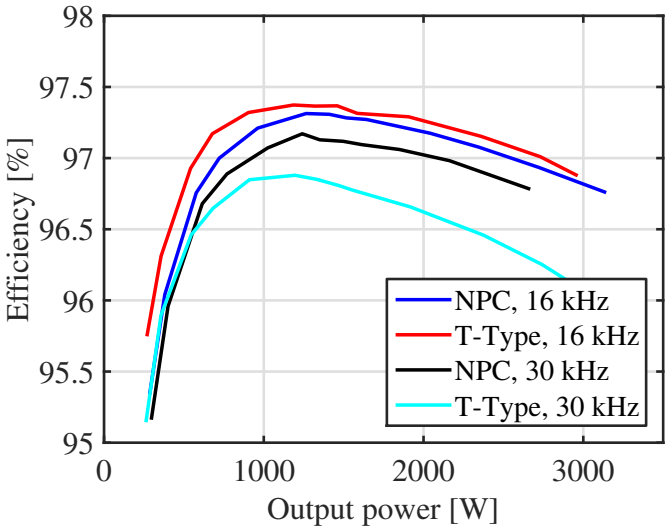


Figure 3.4: Measured efficiencies of NPC and T-Type for different switching frequencies and output power

The aforementioned analysis on the switching frequency influence on the converter losses is verified experimentally. Efficiency measurements are conducted with an N4L PPA5500 power analyzer based on the specifications from Table 4.4. Results for both topologies using conventional PD PWM and Si IGBT devices paired with SiC diodes are given for two different switching frequencies, i.e. 16 kHz and 30 kHz. The results are shown in Fig. 3.4 illustrating a large efficiency drop for the T-Type alternative as the switching frequency is increased. In particular, Fig. 3.4 shows that efficiencies for the T-Type inverter are highest as the switching frequency is set low. This is especially true for light load conditions where the T-Type converter can achieve lower conduction losses because only one device conducts current at positive or negative output voltage state. However, as the switching frequency increases, a major drop in efficiency for the T-Type converter is observed while the drop in efficiency for the NPC is less severe. Clearly, these curves can look different depending on the chosen semiconductor devices, modulation strategies and operating conditions such as DC link voltage, modulation index etc. However, Fig. 3.4 verifies the general statement in alignment to [24] that the efficiency in the T-Type structure is more dependent on the switching frequency than the NPC alternative, which, in turn, leads to the conclusion that the T-Type structure to date is not a suitable topology for high efficiency high switching frequency operation.

3.4 Summary

This chapter dealt with a direct comparison of two commonly used three-level inverter structures, i.e. the NPC and the T-Type topology. Using conventional PD PWM, the T-Type inverter can achieve high efficiencies at low switching frequencies. That is because its conduction losses are lower compared to the NPC due to the reduced current stress in the inner switching devices $S_{2,3}$. However, as the switching frequency increases, the switching losses in the outer switching devices

$S_{1,4}$ become large because they need to be able to block the whole DC link voltage even though the commutation voltage is only $V_{DC}/2$. This significantly reduces the overall efficiency in the T-Type inverter compared to the NPC structure because the latter alternative can be realized with semiconductor devices that need to block only half the DC link voltage.

Chapter 4

Efficiency Improvements in the T-Type Structure

Based on the previous chapter, the T-Type topology has its advantages in the low conduction losses but suffers from large switching losses due to the utilization of 1200 V switching devices in its outer path compared to the NPC alternative despite the fact that only half the DC link voltage applies during a switching commutation. This chapter represents the major part of this PhD project, i.e. to accurately quantify the inverter losses for a given application/specification and to investigate possible methods to overcome the fundamental issue linked to the T-Type structure. Two approaches are investigated in detail and compared to each other. The first approach is investigated in Sec. 4.1 and directly utilizes low loss switching devices made of SiC whereas the second approach, presented in Sec. 4.2, strategically adds lower breakdown voltage rated semiconductor devices in addition to the conventional T-Type inverter, resulting in a more complex topology. This approach is referred to *Hybrid-NPC* in further reading.

4.1 Using SiC switching devices

Semiconductor devices made of SiC are of great interest in power electronics applications because of their superior performance compared to regular Si based devices. An introduction to these semiconductor devices was given in Sec. 2.2 showing the potentials within the field of power electronics. This chapter compares two promising SiC switching devices against each other and a high-speed Si based IGBT. Based on the outcome of this analysis, the most promising candidate is utilized in the three-level T-Type inverter to investigate possible loss reduction on a topological level.

4.1.1 Advantages and Challenges with SiC Switching Devices

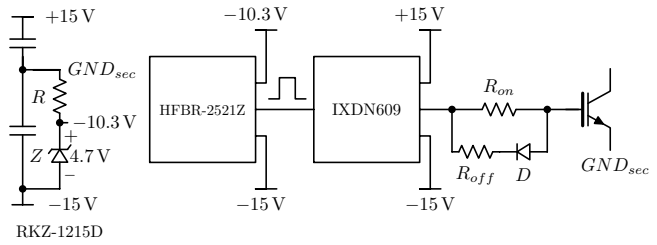
Despite their introduction and implementation in various prototypes, SiC switching devices have not found commonplace usage in commercial products. First of all, the commercial availability of SiC switching devices through distribution channels is mainly dominated by SiC MOSFETS [54] as these devices are closest to well known Si devices [37, 55]. Furthermore, there is no direct replacement meaning that for each SiC device implemented, modifications on their gate driver circuits must be done while the device itself often comes in the same package (TO-220 or TO-247 when discrete device are considered).

Another major aspect postponing the replacement of Si devices comes with the term reliability. SiC switching devices have their own characteristics, each with particular advantages and drawbacks. For instance, the SiC MOSFET is claimed to have reliability issues in its gate-oxide [55, 56]. Not only is the gate threshold voltage highly instable as the temperature in the gate-oxide increases, the gate can also degrade after a short-circuit operation [57–59]. While these issues are related to long-term reliability, which the SiC JFET does not have because of its missing gate-oxide, its depletion mode (normally-on) characteristic is the main drawback. Normally-on means that it is fully turned on when the gate-source voltage is 0 V and a negative voltage is required to turn the device off. This immediate reliability issue is important in Voltage Source Converters (VSCs) comprising of large DC link capacitor banks (for instance in each topology in Fig. 2.3). While this issue can be addressed with an in series placed low voltage Si MOSFET, known as a cascode configuration [60, 61], it increases the complexity of the converter system because an additional semiconductor device is necessary for each SiC JFET. Where only one gate driver is necessary for the conventional cascode [60, 61], only the low voltage MOSFET is directly controlled and no direct control of the JFET is possible. The other approach is the *Direct driven cascode* [62], which achieves direct control for both the JFET and the MOSFET, but comes at the expense of a clearly more sophisticated requirement to the gate driver. A detailed explanation of the Direct driven approach can be found in [62]. Since the Direct driven approach allows controllability of the JFET and the low voltage MOSFET only acts for normally-off behavior, the analysis and comparison are done on the JFET only since no switching losses in the cascode MOSFET are expected. The semiconductors used for this comparison are listed in Table 4.1.

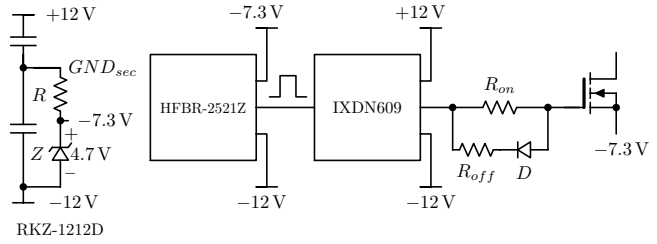
Table 4.1: Semiconductors used

Device	Name	I_C or I_D at 25 °C [A]	V_{GE} or V_{GS} [V]	C_{oss} [pF]
Si IGBT	IKW15N120H3	30	±20	75
SiC MOSFET	C2M0080120D	36	$-10/+25$	80
SiC JFET	IJW120R070T1	35	$-19.5/+2$	102

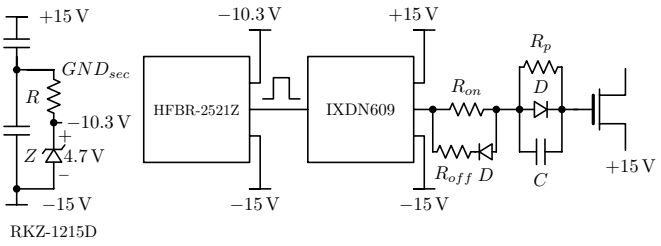
The basis in this comparison is chosen to be a similar current rating at 25 °C. Table 4.1 also details the particular gate-source or gate-emitter requirements given as absolute maximum ratings. Although the gate driver circuits for the use of SiC switching devices are well discovered by now, a direct comparison on the design alterations compared to a conventional gate driver for Si IGBTs are only partially



(a) Si IGBT



(b) SiC MOSFET



(c) SiC JFET

Figure 4.1: Schematic of the gate driver circuits

covered in literature, e.g. in [63]. The JFET driver circuit is taken from [64] which has found good acceptance for the use of normally-on JFETs. All three possible gate driver constellations are shown in Fig. 4.1.

The IGBT gate driver circuit with its most basic components uses the commercially available DC/DC converter *RKZ-1215D* to provide not only galvanic isolation (usually necessary in multilevel converters) but also the required voltage levels for the IGBT gate. The *HFBR-2521Z* receives the control signal from the evaluation board *C2000 Piccolo Launchpad*, and *IXDN609* is the gate driver IC. The voltage supply for the receiver is obtained using a simple zener diode.

The SiC MOSFET requires different gate voltages. This work uses the approach to obtain such voltage levels with a minimum adjustment with respect to the IGBT driver. First of all, the commercially available DC/DC converter RKZ-1215D is replaced with the *RKZ-1212D* providing ±12 V. The source of the SiC MOSFET is connected to the anode of the zener diode, i.e. −7.3 V. The driving voltage for turn on is then according to Kirchoff's voltage law (KVL)

$$V_{GS,on} = +12\,\mathrm{V} - (-7.3\,\mathrm{V}) = 19.3\,\mathrm{V} \tag{4.1}$$

and the turn off voltage, respectively

$$V_{GS,off} = -12\,\mathrm{V} - (-7.3\,\mathrm{V}) = -4.7\,\mathrm{V} \quad . \tag{4.2}$$

With respect to the IGBT gate driver, only two minor modifications are thus necessary:

1. Replace the DC/DC converter RKZ-1215D with the DC/DC converter RKZ-1212D which provides galvanic isolation and two output voltages $\pm 12\,\mathrm{V}$.
2. Reference the source of the SiC MOSFET to the voltage of the zener diode, i.e. $-7.3\,\mathrm{V}$.

The gate driver circuit for the SiC JFET is most different from the Si IGBT driver circuit. The reason for that lies in the internal structure of a normally-on SiC JFET, which is thoroughly described in [56, 62, 64]. It is turned on with $0\,\mathrm{V}$ and a negative voltage needs to be applied to turn the device off. This pinch-off voltage is given to be around $-16\,\mathrm{V}$ and a thus a voltage of around $-20\,\mathrm{V}$ is recommended to fully turn the device off. At around $-23\,\mathrm{V}$, the gate-source junction enters reverse breakdown causing a large current flowing through the gate. The gate driver shown in Fig. 4.1c is designed to allow reverse breakdown because the current is limited by the high ohmic resistor R_p [64]. The modifications for the JFET gate driver with respect to the IGBT gate driver are as follows:

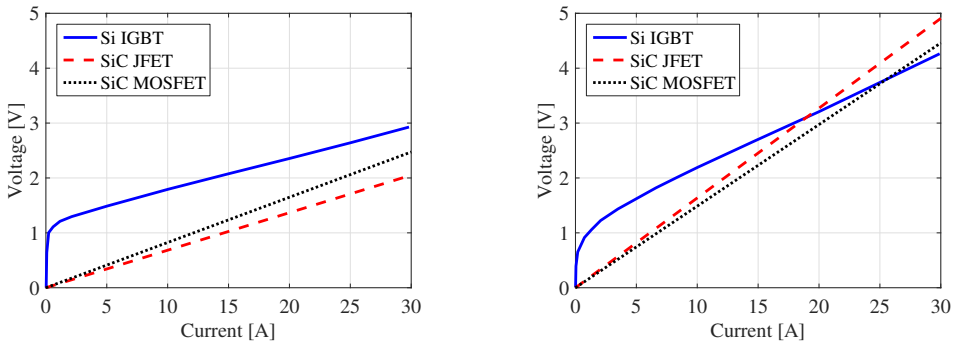
1. Place an RCD network between the gate resistance and the gate of the JFET.
2. Reference the source of the JFET to the positive supply voltage of the DC/DC converter output, i.e. $+15\,\mathrm{V}$.

Based on the gate driver circuit, neither the JFET standalone nor the MOSFET seem to show significant differences compared to the IGBT, although the JFET needs three more components (RCD network) and the statement holds only true if no low voltage cascode MOSFET is used. In case of a direct driven cascode configuration, two separate gate drivers and a proper undervoltage lockdown capability are necessary, which makes the SiC MOSFET then advantageous over the SiC JFET.

The second comparison basis uses the devices losses, based on datasheet information, switching transition measurements and converter loss measurements using a N4L PPA5500 power analyzer.

4.1.2 Conduction losses

Forward voltages of all three devices for two different junction temperatures T_j, i.e. $T_j = 25\,^\circ\mathrm{C}$ and $T_j = 175\,^\circ\mathrm{C}$, are shown in Fig. 4.2. The SiC devices have a lower voltage drop over the entire current range at a low junction temperature of $25\,^\circ\mathrm{C}$ and superior forward voltage behavior up to around $20\,\mathrm{A}$ at a junction temperature of $175\,^\circ\mathrm{C}$. This indicates that the SiC devices will have lower conduction losses compared to the Si IGBT over various operating points. Within the prospect of the SiC switching devices, both devices have a resistive output behavior and the SiC JFET has a lower on-state resistance than the SiC MOSFET alternative at $25\,^\circ\mathrm{C}$ junction temperature. At maximum junction temperature of $175\,^\circ\mathrm{C}$, the SiC JFET has a higher forward voltage compared to the SiC MOSFET. It is therefore of interest to show the on-state resistance as a function of junction temperature, shown



(a) Forward voltage drop of a Si IGBT and two SiC switching devices at a junction temperature of 25 °C

(b) Forward voltage drop of a Si IGBT and two SiC switching devices at a junction temperature of 175 °C

Figure 4.2: Forward voltages at different current levels and junction temperatures

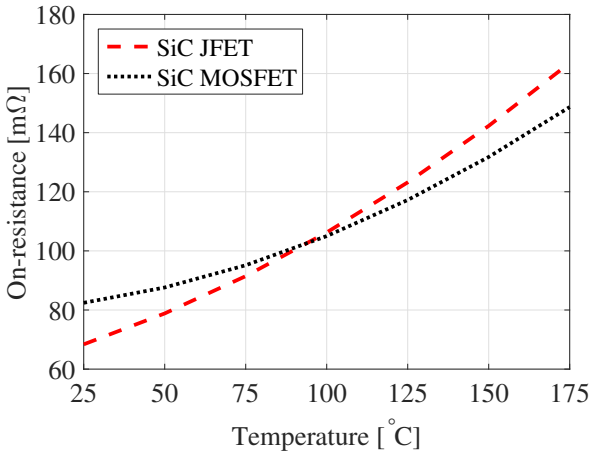
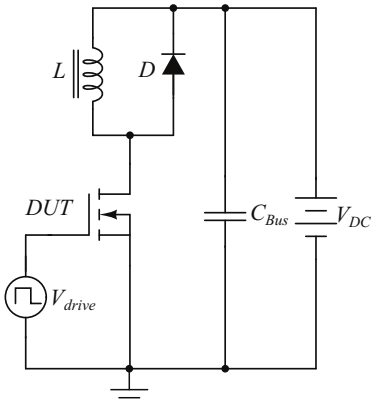


Figure 4.3: On-state resistances versus junction temperature

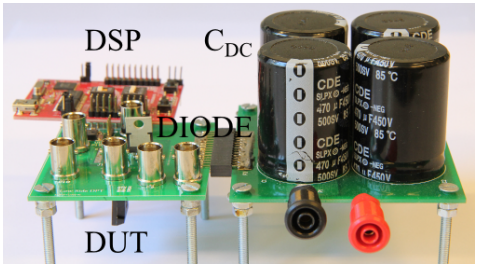
in Fig. 4.3. From a conduction loss point of view, the SiC JFET is beneficial at a junction temperature of up to 100 °C. Above that temperature, the SiC MOSFET shows superior conduction loss behavior.

4.1.3 Switching losses

Switching losses are another major loss contributor in a power electronics converter, caused during a commutation event where voltage across and current through the device are overlapping with significant large values for a short amount of time. A common way of measuring this overlap of current and voltage is done via a DPT circuit, which has been designed in a Master's thesis throughout this PhD project [65]. The schematic and the laboratory prototype are shown in Fig. 4.4. Measuring voltage and current over a wide range of operating points, and integrating the product of these two values, gives the energy dissipation during each particular switching transition. This is exemplary shown in Fig. 4.5 for the SiC MOSFET, and a turn on commutation of 800 V and 10 A. Note that a complete comparison including the other devices is presented in App. H. This principle is then used to

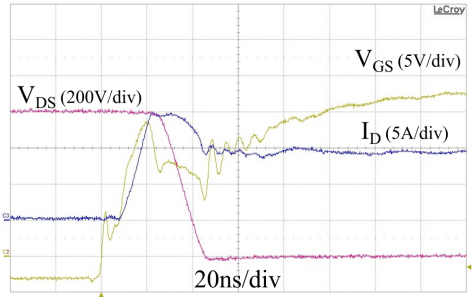


(a) Schematic of DPT circuit

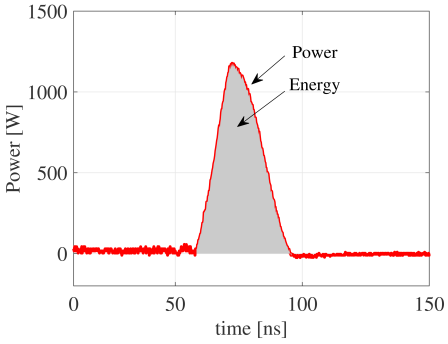


(b) Laboratory prototype of DPT circuit

Figure 4.4: Double pulse test circuit for switching energy measurements

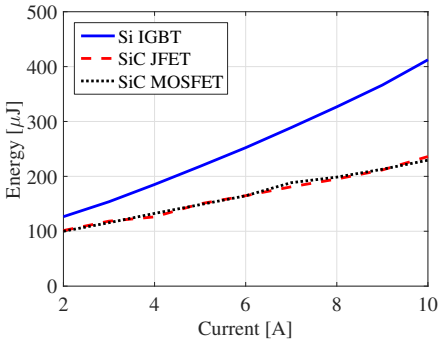


(a) Turn on transition for the SiC MOSFET

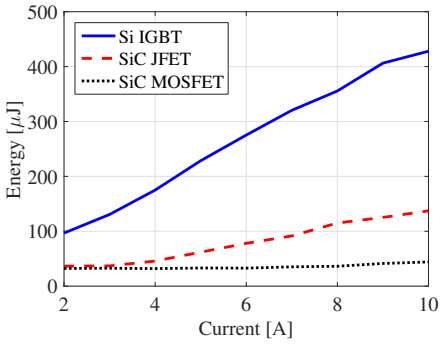


(b) Switching losses during switching commutation

Figure 4.5: SiC MOSFET turn on commutation in (a) and associated losses in (b)



(a) Turn on energies



(b) Turn off energies

Figure 4.6: Measured switching energies for different current levels and a junction temperature of 25 °C

obtain the switching energies plotted in Fig. 4.6. It is commonly known that SiC switching devices have significantly lower switching energies compared to their Si IGBT alternatives. It is therefore only worthy of comment that the SiC JFET and SiC MOSFET have very similar turn on energies throughout the current range. However, the SiC MOSFET shows turn off energies almost constant throughout

the measured current range, which are much lower than the turn off energies of the SiC JFET, that are increasing with the switched current.

4.1.4 Loss breakdown analysis

Based on the previous analysis on the static and dynamic characteristics of the semiconductor devices, loss models can be developed and used for a loss breakdown analysis. The performance analysis is carried out on a simple boost converter. This topology has been chosen not only due to its low complexity (only one switching element, one diode and one boost inductor are necessary as depicted in Fig. 4.7), but also because it is generally necessary in a transformer-less PV inverter system to obtain a constant DC link voltage and the boost converter then acts as a pre-regulator [35, 66].

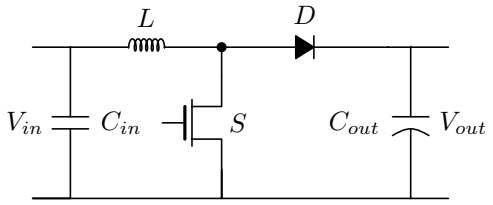


Figure 4.7: Schematic of a conventional boost converter

The voltage at the output of the PV panels is the input voltage of the boost converter V_{in}, and it is assumed to be between 400 V and 500 V under nominal operation. The boost converter provides a constant output voltage V_{out} of 700 V as the lower limit of the DC link for the inverter stage of the PV system. A typical switching frequency using standard Si IGBTs is in the range of 20 kHz to be above the audible range. This gives the following duty cycles d according to

$$d = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{400\,\mathrm{V}}{700\,\mathrm{V}} = 0.43 \tag{4.3}$$

and

$$d = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{500\,\mathrm{V}}{700\,\mathrm{V}} = 0.29 \quad . \tag{4.4}$$

The inductor current ripple can be calculated according to [67]

$$L = \frac{V_{in} d}{2 \Delta I f_{sw}} \quad . \tag{4.5}$$

Following the approach to keep the inductor current ripple to be within 20 % of the inductor DC current, the inductance is then calculated to be 2.3 mH. A 3 mH inductor is taken from a commercial PV inverter system (Danfoss 6 kV A TLX). The conduction losses of the Si IGBT are obtained using its piece-wise linear model, which uses the zero on-state voltage V_0 and the dynamic on-resistance r_{on}, i.e.

$$P_{con,IGBT} = V_0 I_{AV} + r_{on} I_{rms}^2 \quad , \tag{4.6}$$

where I_{AV} is the average current through the device and I_{rms} is the RMS current. The conduction losses for the SiC diode are based on its threshold voltage V_T and

Table 4.2: Specifications for boost converter

Symbol	Meaning	Value
V_{in}	Input voltage	400 V to 500 V
V_{out}	Output voltage	700 V
$f_{sw,1}$	Switching frequency	20 kHz
L_1	Boost inductor for $f_{sw,1}$	3 mH
$f_{sw,2}$	Switching frequency	100 kHz
L_2	Boost inductor for $f_{fsw,2}$	1 mH

its dynamic on-resistance r_{on}, i.e.

$$P_{con,Diode} = V_T I_{AV} + r_{on} I_{rms}^2 \quad . \tag{4.7}$$

The SiC JFET and the SiC MOSFET show a resistive output behavior, hence only the on-resistance $R_{DS(on)}$ is necessary. Therefore, conduction losses for both FET devices are obtained using Ohm's law.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2 \tag{4.8}$$

The switching energies for all three switching devices show a linear relationship to the commutated current, which can be described as

$$E_{on,IGBT,FET} = a_{on} I_{L,DC} + b_{on} \tag{4.9}$$

$$E_{off,IGBT,FET} = a_{off} I_{L,DC} + b_{off} \tag{4.10}$$

where $a_{on,off}$ and $b_{on,off}$ are the curve fitting constants obtained from Fig. 4.6. The averaged switching losses are then obtained by linearly scaling the energies at the measured voltage V_{Base} to the actual commutation voltage, which is V_{out} in a boost converter.

$$P_{sw} = f_{sw} \frac{V_{out}}{V_{Base}} \left(E_{on,IGBT,FET} + E_{off,IGBT,FET} \right) \tag{4.11}$$

Once the equations are established and the average and RMS currents are obtained either analytically or via simulations (the reader is referred to Chap. C which provides the necessary equations to obtain the average and RMS currents), the losses in the semiconductor devices can be calculated for any given operating point, with an associated loss breakdown. This has been done for the specifications from Table 4.2, an output power of 2.5 kW and a switching frequency of 20 kHz, where the results are shown in Fig. 4.8.

Within the boost converter operation, the SiC MOSFET has lower switching losses but higher conduction losses compared to the SiC JFET such that overall device losses will be very close to each other. Both SiC switching devices, however, will greatly reduce the losses compared to the chosen Si IGBT.

Efficiency measurements via an N4L PPA5500 power analyzer on a laboratory boost converter are carried out to verify the loss modeling approach. Overall converter efficiencies including their measurement bounds for $V_{in} = 400$ V and $V_{in} = 500$ V are shown in Fig. 4.9a and Fig. 4.10a, respectively. The semiconductor loss modeling approach from Eq. (4.6)-Eq. (4.11) quantifies the losses associated with

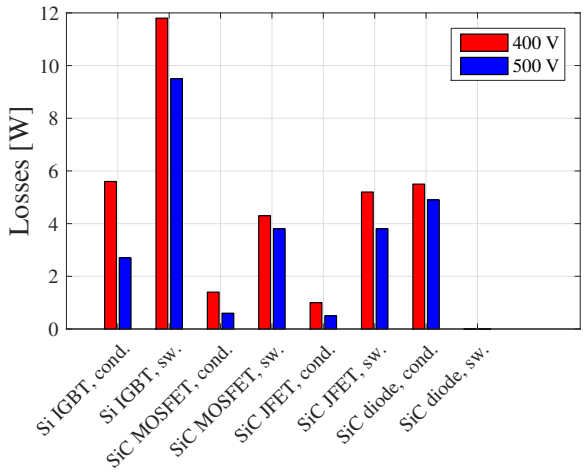
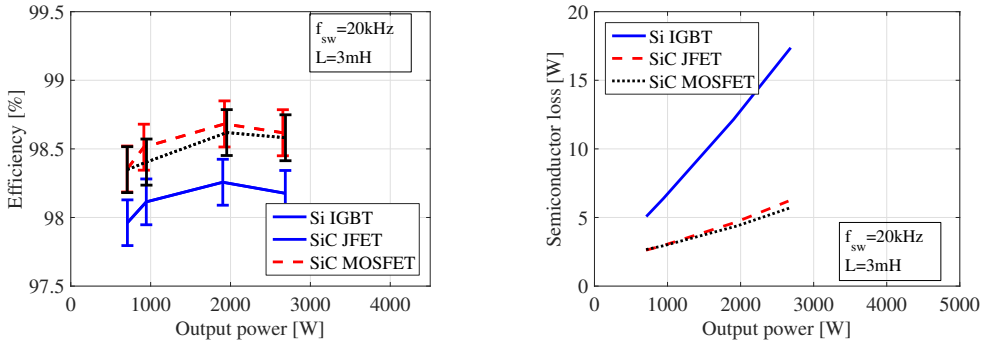
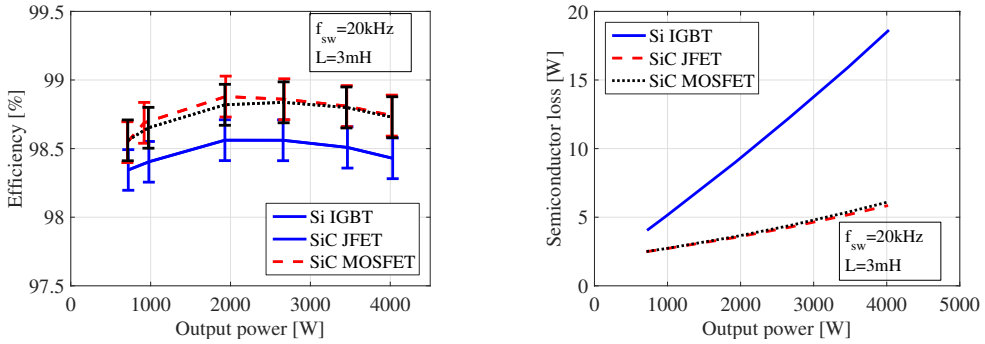


Figure 4.8: Semiconductor loss breakdown analysis in the boost converter operating at 20 kHz switching frequency and an output power of 2.5 kW



(a) Efficiencies for $V_{in} = 400\,\mathrm{V}$ **(b)** Semiconductor losses for $V_{in} = 400\,\mathrm{V}$

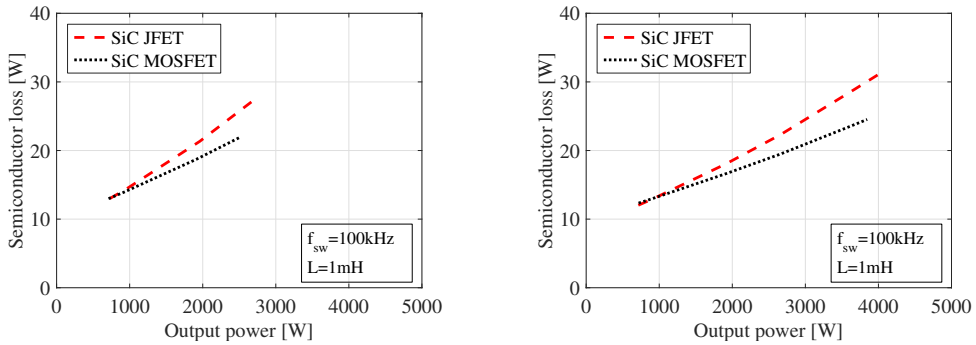
Figure 4.9: Measured efficiencies and calculated semiconductor losses for 400 V input voltage and 700 V output voltage



(a) Efficiencies for $V_{in} = 500\,\mathrm{V}$ **(b)** Semiconductor losses for $V_{in} = 500\,\mathrm{V}$

Figure 4.10: Measured efficiencies and calculated semiconductor losses for 500 V input voltage and 700 V output voltage

the particular switching device, shown in Fig. 4.9b and Fig. 4.10b, confirming a very similar loss performance in the entire power range. Following the same loss modeling approach, the semiconductor losses for any switching frequency can be predicted,



(a) Semiconductor losses for $V_{in} = 400\,\mathrm{V}$ **(b)** Semiconductor losses for $V_{in} = 500\,\mathrm{V}$

Figure 4.11: Semiconductor losses for different output power levels, input voltages and a switching frequency of 100 kHz

Table 4.3: Semiconductor comparison

	Si IGBT	SiC MOSFET	SiC JFET
Commercially availability	++	+	-
Gate driver simplicity	++	+	standalone: + conv. cascode: ++ direct dr. cascode: -
Maturity level	++	-	+
Hard switched high frequency operation	-	++	+

such as for 100 kHz operation, where associated semiconductor losses are presented in Fig. 4.11. The full analysis on the comparison between Si and SiC switching devices including inductor size reduction at increased switching frequencies can be found in App. H and it is only mentioned here that both SiC devices can be attractive alternatives for the Si IGBT when it comes to loss reduction. There is no absolute answer to which SiC device to use and it is therefore a question to the immediate needs for the design objectives, for which Table 4.3 can be used to summarize the aforementioned comparison.

4.1.4.1 Summary

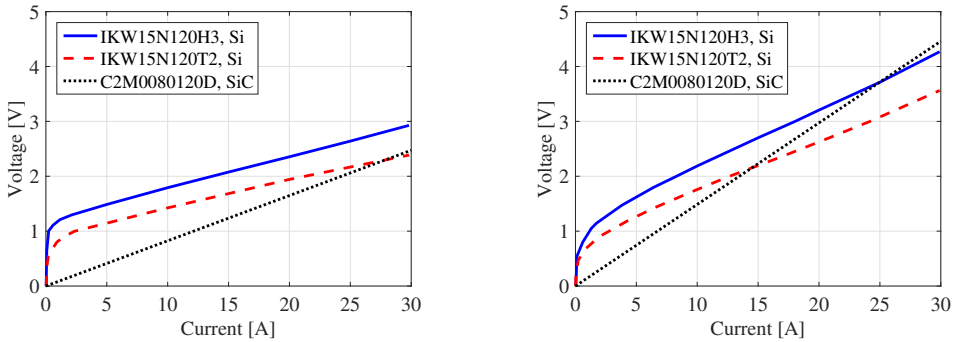
This section dealt with the investigation of two promising SiC switching devices as alternatives to a conventional Si IGBT. Both SiC switching devices have their particular advantages and drawbacks. The main argument against the SiC MOSFET to date is still its immaturity state for long-term reliability operation within converter context. The main argument against the SiC JFET is its normally-on characteristic. Although it can be overcome with a cascode configuration, it then increases complexity and hence major design changes are necessary compared to a Si IGBT based design. If high efficiencies are the main design objective for a hard switched converter operating at high switching frequencies, the SiC MOSFET can be an interesting choice due to its lower turn off energies compared to the SiC JFET.

4.1.5 Use of SiC in T-Type Inverter

The aim of this section is to investigate if and to what extend the utilization of SiC switching devices gives benefits within the T-Type converter operating context. Based on the previous subsection, the utilization of the SiC JFET in a VSC is only recommended in a cascode configuration, which then results in major design changes in the T-Type structure compared to the Si IGBT [4]. Since long-term reliability is not a design constraint of this PhD project, the SiC MOSFET is the device retained for further analysis, also due to its good commercial availability through distribution channels. The majority of commercial available SiC switching devices to date cover the range of voltages $\geq 1200\,\mathrm{V}$, which is why most of the references are comparing Si and SiC switching devices in such voltage range. Nevertheless, the manufacturer ROHM offers a 650 V SiC MOSFET which may be an alternative in the bi-directional path of the T-Type structure and it will therefore be included in the analysis.

Semiconductor device selection

A loss analysis on a semiconductor basis needs justification for the semiconductors used. This work uses semiconductor devices that seem appropriate for the given application rather than the most recent device available, that is optimized for a given parameter, because there is generally a trade-off between the on-state voltage and the turn off energies of an IGBT [32, 33]. An elaboration on that is given in the comparison of using Infineon's 2nd generation IGBT *IKW15N120T2* and Infineon's 3rd generation IGBT *IKW15N120H3*, where the latter device is optimized for low switching energies and hence increased switching frequency operation. The forward voltages of both devices are compared against the selected 1200 V SiC MOSFET *C2M0080120D* for different currents and temperatures, and the results of this comparison are presented in Fig. 4.12.



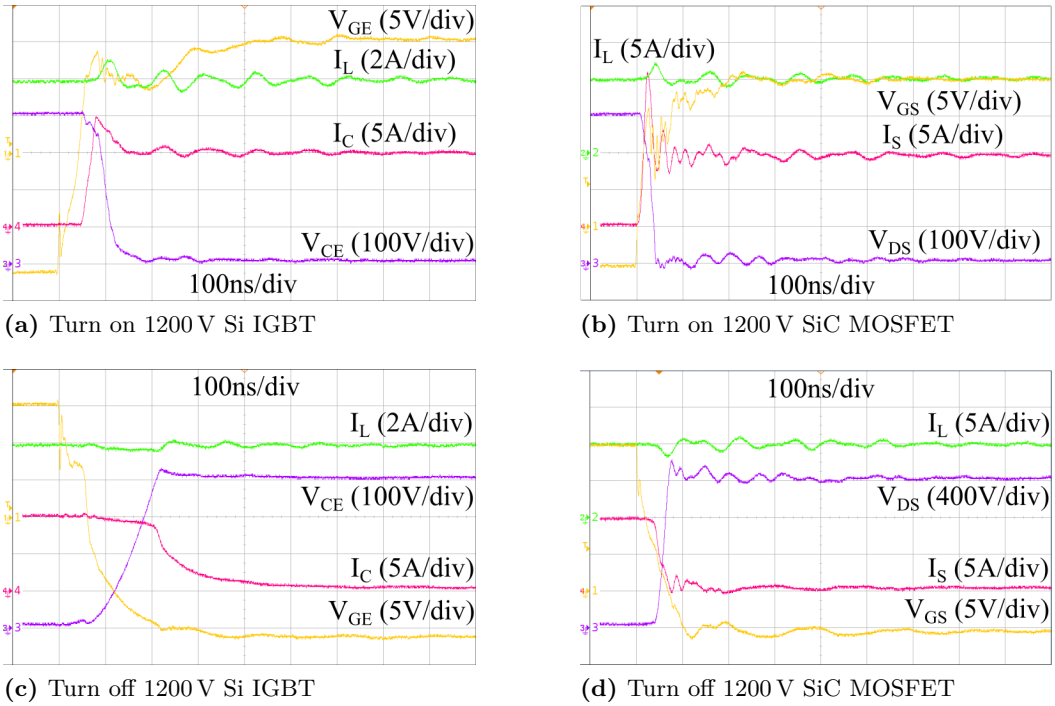
(a) Forward voltages at 25 °C junction temperature

(b) Forward voltages at 175 °C junction temperature

Figure 4.12: Forward voltage comparison of two 1200 V Si IGBTs and a 1200 V SiC MOSFET at different current levels and junction temperatures

An elaboration of Fig. 4.12 shows that the 3rd generation IGBT from Infineon has larger forward voltages over the entire current range and both extremes of junction temperatures, and hence larger conduction losses are expected for this

device. While it may be true that its switching energies are lower compared to the 2nd generation IGBT, one must keep in mind that residential PV inverters to date are operating at rather low switching frequencies in the range of up to 20 kHz, and that the outer devices of the T-Type converter commutate current at less than half their rated voltage. Therefore, Infineon's 2nd generation IGBT is considered an appropriate device and is thus retained for further analysis. Although a comparison of switching energies for different devices have been given in Sec. 4.1.3, in-circuit switching transition measurements on the prototype from Fig. 4.21 are shown in Fig. 4.13 since the commutation voltage is at a much lower level (recall that for the T-Type inverter, the commutation voltage is only $V_{DC}/2$).



(a) Turn on 1200 V Si IGBT

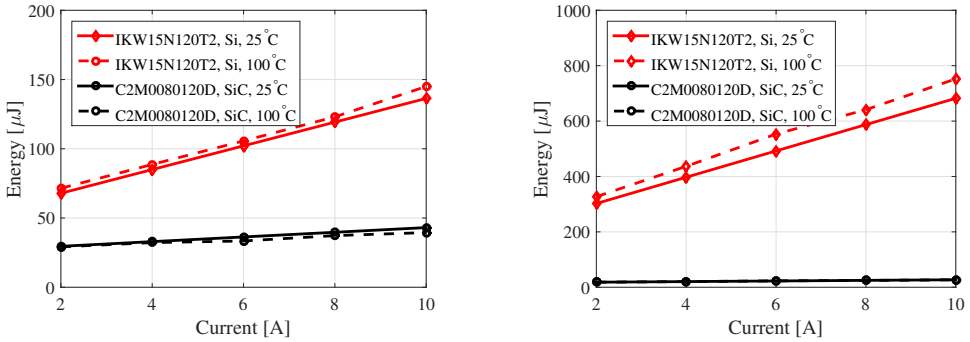
(b) Turn on 1200 V SiC MOSFET

(c) Turn off 1200 V Si IGBT

(d) Turn off 1200 V SiC MOSFET

Figure 4.13: Turn on and turn off transitions in the T-Type inverter context

From the in-circuit transition measurements presented in Fig. 4.13, the slow turn off commutation of the Si IGBT due to its tail current can be seen in Fig. 4.13c. In contrast, the SiC MOSFET turns off much quicker as a consequence of being a majority carrier device. This also reflects the large turn off energies in the Si IGBT compared to the very low turn off energies to the SiC MOSFET, which have been obtained using the same principles presented in Fig. 4.5b and the results for the T-Type application are shown in Fig. 4.14. It is worthy of comment that the turn on switching energy of the SiC MOSFET at increased temperatures is slightly reduced. While this may seem unusual and one would typically expect an increase in switching energies with junction temperature, the phenomenon of reduced switching energies at increased junction temperatures for the SiC MOSFET has been observed in previous literature [68–70], and can be explained by the decreased threshold voltage at increased temperatures as well as the increased transconductance. What can be seen from Fig. 4.14 is that even though the commutation voltage is way below the rated voltage of the 1200 V switching devices in the T-Type converter,



(a) Turn on energies within T-Type inverter context

(b) Turn off energies within T-Type inverter context

Figure 4.14: Measured switching energies of utilized 1200 V devices at a commutation voltage of 400 V

large switching energies are still present in the Si IGBT and a major benefit of using SiC MOSFETs can be seen in this context.

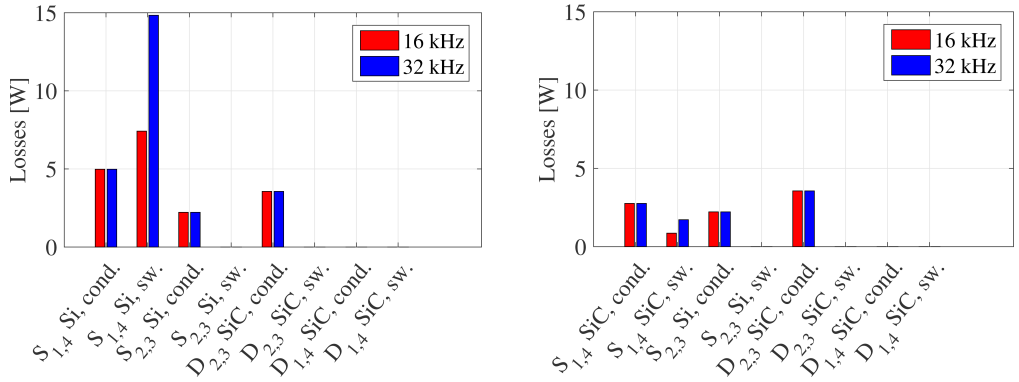
Loss breakdown analysis

Now that the characterization of the switching devices has been carried out, the same semiconductor loss modeling approach from Sec. 4.1.4 can be applied to the T-Type inverter operating context with the specifications from Table 4.4.

Table 4.4: Specifications inverter

Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 µF
M	Modulation index	0.85

The corresponding semiconductor loss breakdown graphs are shown in Fig. 4.15. Investigating the conventional operation mode of the Si IGBT based inverter in Fig. 4.15a, i.e. pure active power operation, the losses in the DC bus connecting switches $S_{1,4}$ are representing the dominating loss contributor. This immediately shows that within the inverter operating context, a major semiconductor loss reduction can be found in optimizing switches $S_{1,4}$, as presented in Fig. 4.15b, in which the 1200 V SiC MOSFET replaces the 1200 V Si IGBT. In particular, switching losses of around 7.4 W in the Si IGBTs can be reduced down to only 0.9 W when upgrading to SiC MOSFETs. This gives a switching loss reduction of more than 85 % and a conduction loss reduction of almost 50 %. An elaboration on the loss reduction including different power factors is given in a later section of this chapter after discussing the Hybrid-NPC alternative.



(a) Si IGBT based inverter at $P_{out} = 1500\,\text{W}$ and $cos\,(\varphi) = 1$

(b) SiC MOSFET based inverter at $P_{out} = 1500\,\text{W}$ and $cos\,(\varphi) = 1$

Figure 4.15: Loss breakdown analysis comparison for Si IGBT and SiC MOSFET based inverter

4.2 Using 600 V Si Switching Devices / Hybrid-NPC

Due to the drawbacks of SiC switching devices to date, one might want to retain a completely Si based converter design. As pointed out in Fig. 4.15a, the losses associated in the T-Type inverter within PV operating context are mainly located in $S_{1,4}$ and that switching losses are sensitively affected by the switching frequency. Thus, the question arises whether there is an alternative way of reducing such switching losses other than placing SiC switching devices which have not fully entered mass production yet. Recalling Chap. 3, the NPC inverter is beneficial in terms of switching losses because each semiconductor device can be rated at half the DC link voltage, which then consequently reduces the switching losses. A combination of the NPC and the T-Type converter has been introduced in [51], called Hybrid-NPC (Fig. 4.16), and has been found to be effective in minimizing the losses associated with the T-Type inverter.

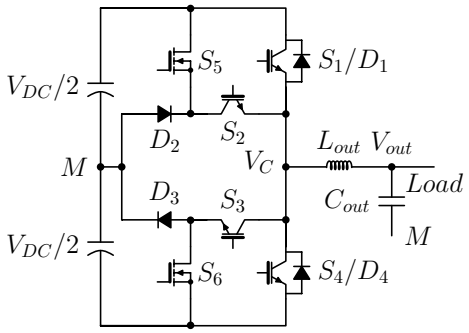
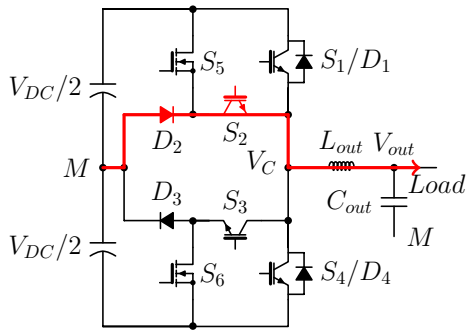


Figure 4.16: Hybrid-NPC topology

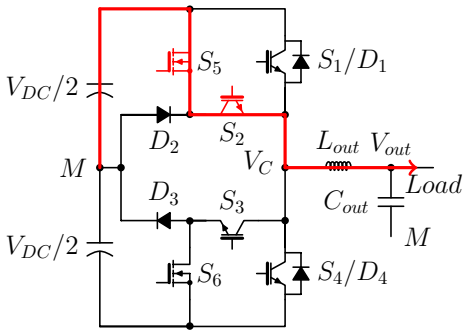
In particular, its effectiveness comes with the additional placement of low switching loss 600 V devices ($S_{5,6}$) aiding the commutation events, and the purpose of the conventional 1200 V Si IGBTs ($S_{1,4}$) is then to create an additional current path to reduce conduction losses. Thus it can be an attractive alternative to the SiC based T-Type structure in terms of reliability, cost and efficiency. To date, however, only few references can be found on this topological approach [51, 71, 72] and no detailed

loss and thermal performance comparison to the conventional T-Type alternative using SiC switching devices is known to the authors. This work furthermore uses 600 V Si CoolMos devices to aid the commutation events due to their low switching energies, depicted as $S_{5,6}$ in Fig. 4.16.

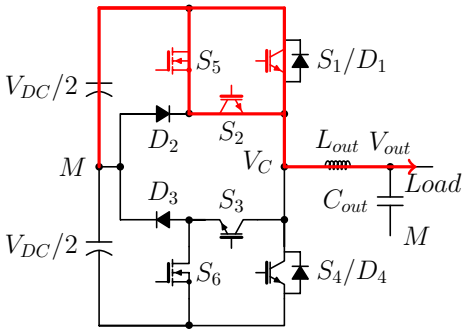
The idea adopted in this work is that the CoolMos devices ($S_{5,6}$) turn on before the Si IGBTs ($S_{1,4}$). This is shown in the transition from Fig. 4.17a to Fig. 4.17b for a positive output voltage. After the commutation procedure is done and the conducting period starts (Fig. 4.17b), relatively large conduction losses would be expected because current flows through two semiconductor devices S_5 and S_2 (note that this is equivalent to the NPC operation principle). Thus, $S_{1,4}$ is turned on creating a current divider, depicted in Fig. 4.17c. When the switching period is over, $S_{1,4}$ turns off first with ideally zero switching losses, because the voltage across S_4 is now reduced to the total voltage drop of S_5 and S_2 instead of the commutation voltage $V_{DC}/2$. After a short period, the CoolMos devices will then turn off with the commutation voltage $V_{DC}/2$. The carrier-based implementation of this principle is shown in Fig. 4.17d.



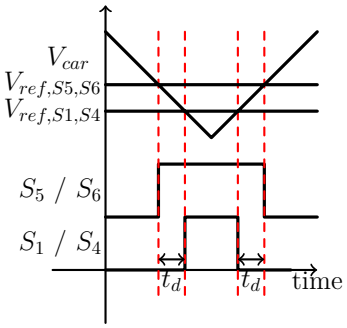
(a) Zero output voltage and positive output current



(b) Positive output voltage and positive output current



(c) Positive output voltage and positive output current



(d) Modulation principle for Hybrid-NPC inverter

Figure 4.17: Switching transition from zero to positive output voltage in Hybrid-NPC inverter

From Fig. 4.13a and Fig. 4.13c, one can see that the turn on and turn off times for the Si IGBT are different and thus the time delay between the CoolMos and the IGBT can affect the converter efficiency. This has been investigated in [72] (Sec. G) and it is found out that a time delay of 2 µs can achieve lowest losses for the system in this thesis. The reason for that is, that if the time delay is chosen too small, the tail current from the IGBT will contribute to the switching losses. If the time delay

is chosen too large, the tail current influence will be less, but conduction losses in the CoolMos device will then have a significant contribution to the overall losses; hence there is a trade-off between CoolMos conduction losses and IGBT switching losses.

Another important aspect for a proper semiconductor loss modeling is to verify the current sharing between the CoolMos and the 1200 V IGBT. A current measurement of the load current and the current through S_4 is shown in Fig. 4.18, detailing that the Hybrid-NPC can be quite effective in reducing the current path through S_3 and S_6 over the whole current range. It is crucial to keep in mind that the current

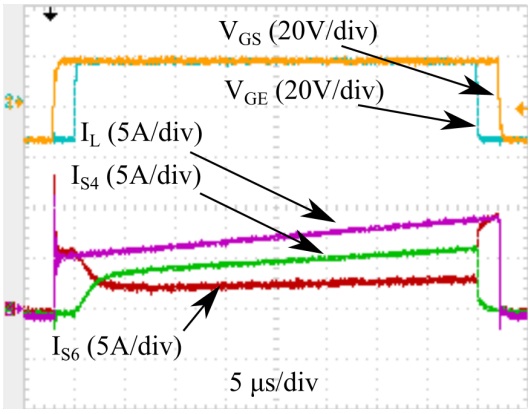
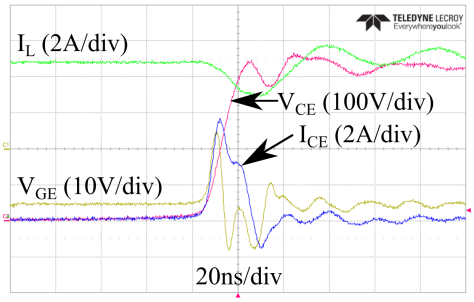
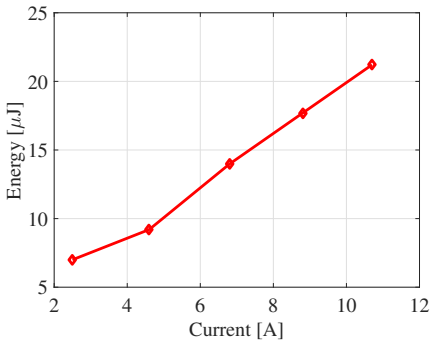


Figure 4.18: Inductor current and current through S_6 when both S_6 and S_4 are turned on

has been measured with a current probe instead of a current measuring resistor or flat shunt resistor [73] because any additional resistance would alter the impedance path and thus the current divider. From Fig. 4.18, one can see that the load current is split up to approx. 2/3 into the path of S_4 and 1/3 into the path of S_3 and S_6. Another aspect is to verify whether and to what extend switching losses occur in $S_{1,4}$. The current has therefore been measured for different current levels whilst being turned off. For a current of 9 A, the influence of the dv/dt of the CoolMos device on S_4 is shown in Fig. 4.19a. Assuming that the product of voltage and current, and hence power, is dissipated within the Si IGBT ($S_{1,4}$),



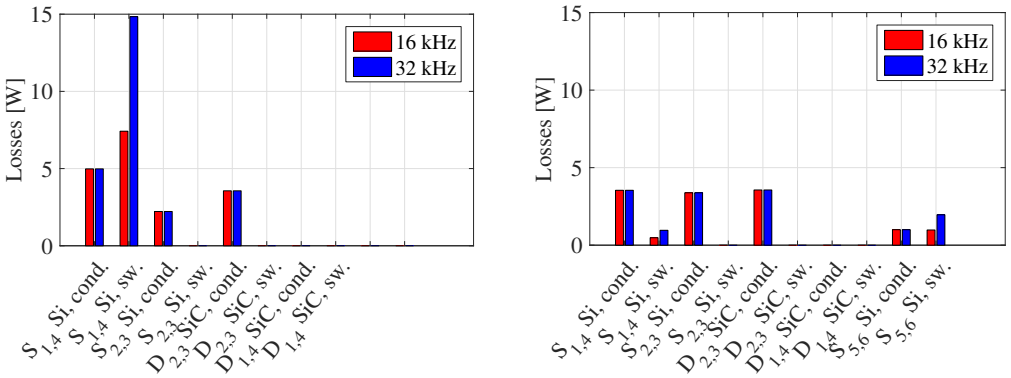
(a) Current through S_4 while being turned off



(b) Switching energies of S_4 whilst turned off

Figure 4.19: Induced current in S_4 in (a) and its associated switching energies in (b)

the next step is to get a quantification of such. This has been done for current levels up to 10 A and is shown in Fig. 4.19b. While this additional loss due to the output capacitance is usually only severe with converters operating at high frequency [74], it is included in this analysis for the sake of completeness from a loss modeling point of view. Including the current sharing and the switching energies into the loss models, the corresponding loss breakdown analysis for the Hybrid-NPC topology can be established, compared to the conventional T-Type structure from Fig. 4.15a. The results are shown in Fig. 4.20, demonstrating that also the Hybrid-NPC topology can be quite effective in minimizing the switching losses associated with the conventional T-Type structure.



(a) Si IGBT based T-Type inverter at $P_{out} = 1500\,\mathrm{W}$ and $cos\,(\varphi) = 1$

(b) Hybrid-NPC inverter at $P_{out} = 1500\,\mathrm{W}$ and $cos\,(\varphi) = 1$

Figure 4.20: Semiconductor loss breakdown analysis of conventional T-Type inverter in (a) and Hybrid-NPC inverter in (b)

It is worthy of comment, though, that although the conduction losses in $S_{1,4}$ are reduced in the Hybrid-NPC converter, conduction losses in $S_{2,3}$ are increased. The reason for that is that $S_{2,3}$ now operate in the usual way in the NPC topology, which is known to have its drawback in increased conduction losses in the inner switching devices.

4.3 Experimental results - Loss Model Validation by Thermal Measurements

The last two sections dealt with a topological investigation of whether and to what extend semiconductor losses in the conventional T-Type structure can be reduced. Loss models have been developed and consolidated into a loss breakdown analysis. This section now presents the results of the experimental approach to validate the semiconductor loss models. While the most common approach in evaluating losses from a topological point of view seems to use electrical input and electrical output power measurements using an oscilloscope or a power analyzer, it can be challenging to get accurate results with this approach because of the difficulty of measuring the high speed pulse width modulated voltages and currents of the converter with adequate precision [75–77]. Although this particular challenge can be addressed with inserting proper filtering, the consequence is that losses of the

DC link capacitors (and thus their in parallel connected balancing resistors) and the output AC filter are included so that overall converter losses are obtained. Another alternative is to conduct calorimetric loss measurements, although this approach is not only cost expensive and time consuming but also includes loss contributions from gate driver circuits, balancing resistors and the AC filter. Hence neither strategy readily provides access only to the semiconductor losses within the converter operation context.

This work therefore uses an alternative measurement approach by means of calibrated heat sinks using known heat loads. The idea behind that approach is based on the fact that semiconductor losses lead to increased heat sink temperatures, and therefore thermal measurements on the particular heat sink can be conducted to translate the thermal energy back to semiconductor losses. While the whole calibration procedure is described in App. A, only the results of the measurements are shown in this section which are compared against the predicted losses from the semiconductor loss modeling approach.

Several prototypes have been developed throughout this PhD project, including both gate driver and power stage design. As for the gate driver design, several approaches to obtain galvanic isolation have been investigated, and the most reliable constellation for the laboratory prototype has been found to use optic fiber technology. For the power stage design of the T-Type inverter, different topological possibilities have been investigated to connect the semiconductor devices in the bidirectional path (such as common emitter/common source connection presented in Fig. 4.25). Using discrete devices, best results in terms of minimized commutation loops were found to use the constellation from Fig. 4.25a. The Hybrid-NPC converter was the final prototype in this project by simply adding two discrete CoolMos devices into the circuit, thereby using the Hybrid-NPC topology to operate both in conventional T-Type or Hybrid-NPC mode, and for the SiC based version, only two switching devices with their associated gate drivers must be replaced. Furthermore, for simplicity, the whole converter in its final stage has been mounted on a common heat sink, as shown in Fig. 4.21.

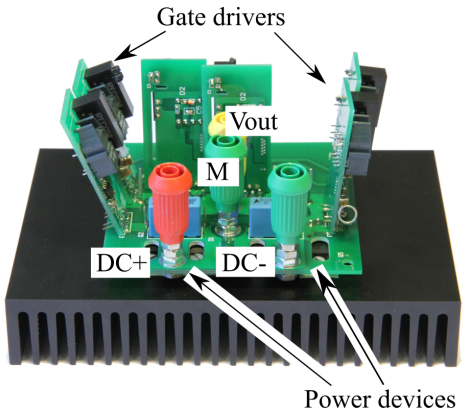
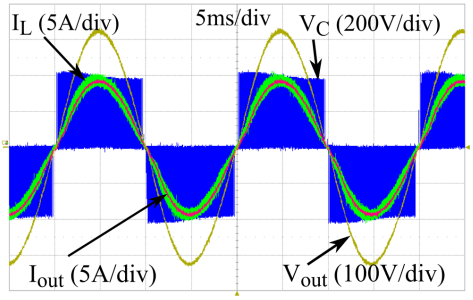
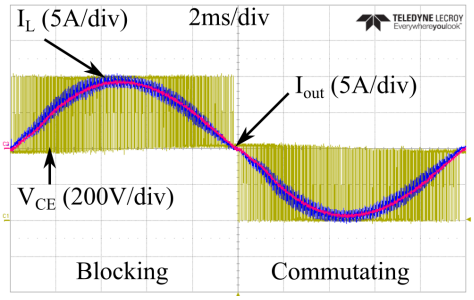


Figure 4.21: Photograph of the final laboratory protytpe

The converter test setup uses a DC power supply at the input and a resistive load at the output, whose value can be changed to achieve different output power levels. Experimental waveforms of the converter operating at the specifications from



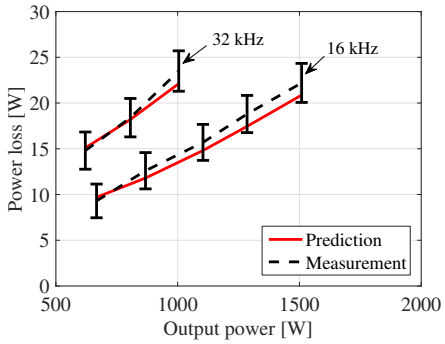
(a) Converter output waveforms



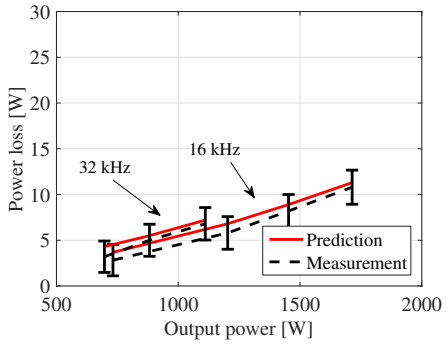
(b) Collector-emitter voltage of S_4 along a fundamental cycle during inverter operation

Figure 4.22: Experimental waveforms of the converter operating at full load

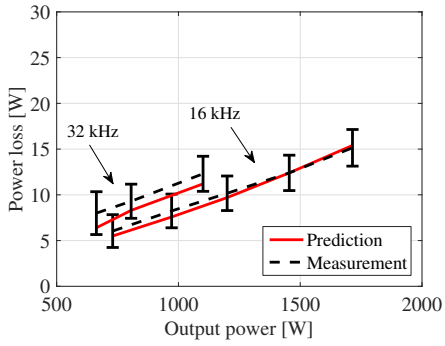
Table 4.4 at full load are shown in Fig. 4.22. The heat sink temperatures have been measured during converter operation and then calculated backwards to achieve the semiconductor losses for various operating conditions such as output power (by varying the load resistance) and switching frequency. The results including their measurement bounds for the conventional Si IGBT based T-Type converter, the SiC MOSFET based T-Type converter as well as the Hybrid-NPC converter are shown in Fig. 4.23.



(a) Semiconductor losses for Si T-Type inverter



(b) Semiconductor losses for SiC T-Type inverter



(c) Semiconductor losses for Hybrid-NPC inverter

Figure 4.23: Predicted and measured semiconductor losses for different converter alternatives

The conventional T-Type inverter not only has highest semiconductor losses, the switching frequency becomes a major design constraint. This verifies the statement that the 1200 V Si IGBTs are the weak point within high efficient inverter operation context. Both alternatives, the SiC MOSFET based T-Type structure and the Hybrid-NPC can greatly reduce semiconductor losses especially at increased switching frequency operation, although the SiC alternative is less susceptible to the switching frequency compared to the Hybrid-NPC.

4.4 Comparative Study on these two Alternatives

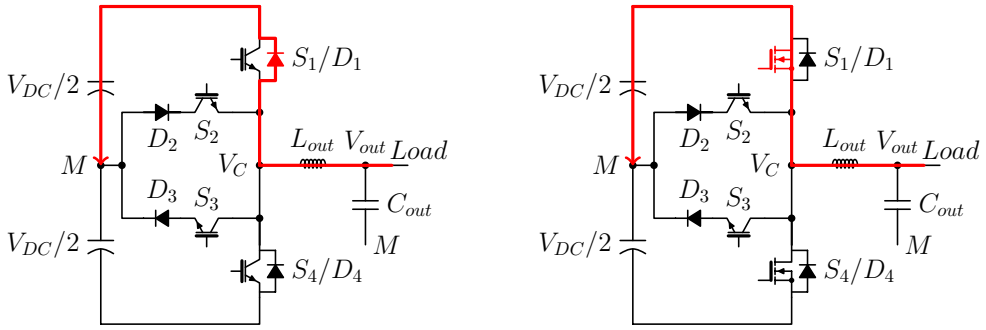
The loss modeling approach has been experimentally verified over numerous operating conditions to be within the measurement bounds of the test equipment, and thus the semiconductor loss models can be used with confidence for further analysis. Although PV inverters in standalone operation are supposed to operate at unity power factor to date [78], this traditional regulation may change in the future due to the issues related to the increasing installation of distributed PV systems [79, 80]. Some countries (Germany as an example) already require reactive power control for grid-connected converters [81], and reactive power control may become an even more important factor in the future with the increasing installation of energy storage systems, which can then be used to support the grid [2]. To date, commercial PV inverters with energy storage systems typically have bi-directional power flow only in the DC/DC conversion part, but not in the DC/AC conversion [2]. Nevertheless, bi-directional power flow in the DC/AC converter will be included in this work as bi-directional power flow in the DC/AC converter may bring another degree of freedom to support the utility grid [82]. The semiconductor loss comparison of the two topological alternatives is based on the loss models derived in this work, and will include both inversion and rectification for different power factors in addition to switching frequency. Note that the analysis uses the converter specifications from Table 4.4 in terms of DC link and AC output voltage.

4.4.1 Loss comparison

Before presenting the results on the topological alternatives, several assumptions and explanations are necessary for further understanding. It is assumed that current can flow through the SiC MOSFET channel in either direction whilst turned on. This is in contrast to the Si IGBT converter which will have to have an anti-parallel diode. This is visualized in Fig. 4.24 for a positive output voltage and a negative current. The loss modeling approach for the SiC MOSFET based converter therefore uses the voltage-current characteristic for a discrete SiC diode $D_{1,4}$ for the Si IGBT based converter and the channel resistance of the SiC MOSFET for the SiC MOSFET based inverter. Any conduction losses during the dead-times are neglected in this analysis. In the previous section, the utilization of 1200 V SiC MOSFETs as direct replacements for 1200 V Si IGBTs have been successfully demonstrated. It is therefore of interest to what extend the utilization of the 650 V SiC switching devices in the bi-directional path can offer benefits in terms of semiconductor loss reduction. A comparison of this particular SiC device against the equivalently rated Si IGBT in terms of forward voltages and switching energies

is given in App. B and only the conclusions are presented here:

- The forward voltage crossover point between the 650 V SiC MOSFET and the 600 V Si IGBT occurs at a lower current level compared to the semiconductor devices in the 1200 V range, thus less conduction loss reduction is expected.
- Turn on switching energies of the 650 V SiC MOSFET are slightly higher compared to the turn on energies of the 600 V Si IGBT.
- Turn off switching energies of the 650 V SiC MOSFET are greatly lower compared to the turn off energies of the 600 V Si IGBT due to the absence of the tail current.

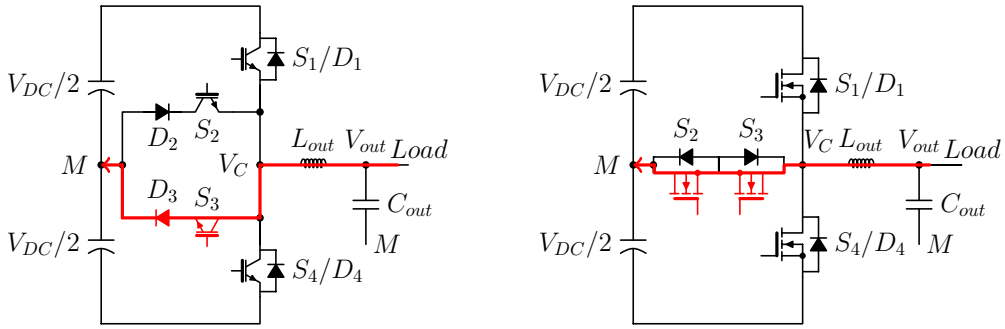


(a) Non-unity power factor operation using Si IGBTs and an anti-parallel freewheeling diode (Configuration 1)

(b) Non-unity power factor operation using SiC MOSFETs bypassing the internal body-diode (Configuration 2)

Figure 4.24: Current flow for non-unity power factors

For further understanding, the bi-directional path in the T-Type structure can be reconfigured, known as common-emitter for IGBTs [15, 51] or common-source for MOSFETs [43], where the latter reference shows the successful utilization of the 650 V SiC MOSFETs in the T-Type structure, but no detailed loss breakdown analysis of such is presented.



(a) Current flow in conventional T-Type structure for zero output voltage (Configuration 1)

(b) Current flow in T-Type inverter with common-source configuration (Configuration 3)

Figure 4.25: Switching states for T-Type inverter operating at unity power factor

Although it is found in App. B that the 650 V SiC have similar forward voltages compared to their Si IGBT alternatives in the current range of interest, conduction losses in the bi-directional path can still be reduced because of the relative

large forward voltages of the SiC diodes $D_{2,3}$ placed in series to the Si IGBTs $S_{2,3}$ (Fig. 4.25a). The semiconductor utilization for both configurations is presented in Table 4.5 and the calculated semiconductor losses are presented in Fig. 4.26.

Table 4.5: Semiconductor utilization for configurations 1, 2 and 3 according to Fig. 4.24 and Fig. 4.25

	Config. 1	Config. 2	Config. 3
$S_{1,4}$	IKW15N120T2	C2M0080120D	C2M0080120D
$S_{2,3}$	IKP15N60T	IKP15N60T	SCT2120AF
$D_{2,3}$	C3D10060A	C3D10060A	
$D_{1,4}$	C4D15120A	C4D02120A	C4D02120A

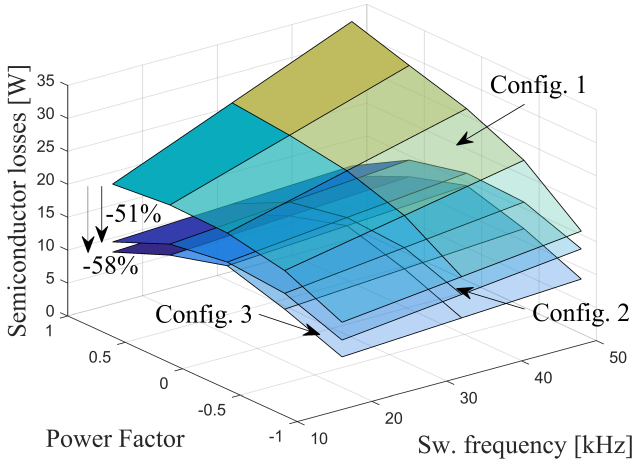


Figure 4.26: Si based T-Type in configuration 1 compared to 1200 V SiC MOSFET T-Type in configuration 2 and a full SiC based T-Type inverter in configuration 3

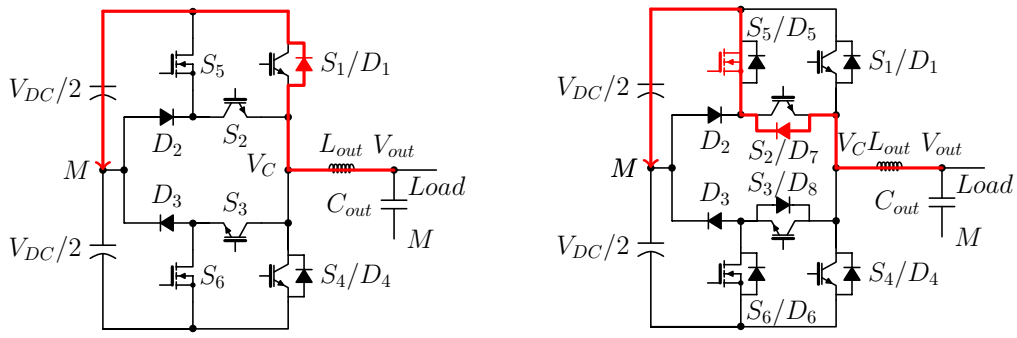
The utilization of 650 V SiC MOSFETs in the T-Type structure can achieve a loss reduction in the entire operating range, although the benefit is small compared to what can be gained with the utilization of 1200 V SiC MOSFETs for the DC bus connecting switches. An elaboration of Fig. 4.26 details the benefits. At high power factor, no commutation losses in the bi-directional path occur and thus the only loss reduction one can gain is from the smaller conduction losses due to the absence of the clamping diodes $S_{2,3}$. At low power factors, further loss reduction can be achieved because not only conduction losses in the bi-directional path are reduced, but also the commutation events are shifted to the bi-directional path, and the 650 V SiC MOSFET can show lower total switching losses due to the absence of the tail current. It is worthy of comment, though, that the frequency dependency on the switching losses is much flatter compared to the devices in the 1200 V range. This leads to the conclusion that the Si IGBTs in the 600 V range can already perform well in terms of switching losses. Hence, from a loss point of view, the bi-directional path within T-Type converter context can achieve low semiconductor losses and the utilization of the 650 V SiC MOSFET can not show a further significant loss reduction. The losses and loss reductions for the

Table 4.6: Semiconductor utilization for configurations 1, 4 and 5

	Config. 1	Config. 4	Config. 5
$S_{1,4}$	IKW15N120T2	IKW15N120T2	IKW15N120T2
$S_{2,3}$	IKP15N60T	IKP15N60T	IKP15N60T
$D_{2,3}$	C3D10060A	C3D10060A	C3D10060A
$D_{1,4}$	C4D15120A	C4D15120A	
$S_{5,6}$		SPP20N60S5	SPP20N60S5
$D_{7,8}$			C3D10060A

three configurations from Fig. 4.26 for the two extreme power factor cases with the operating specifications from Table 4.4 are listed in Table 4.7. Considering the high cost for SiC, the utilization of the 650 V SiC switching devices may result in an unreasonable cost-performance trade-off and thus, only configuration 2 is retained for further comparison against the Hybrid-NPC.

Regarding the Hybrid-NPC alternative, the question arises which path the current will take when operating at non-unity power factor. As for the constellation shown in Fig. 4.16, current would flow through the anti-parallel diodes $D_{1,4}$ since no anti-parallel diodes are present for $S_{2,3}$ and thus no current will flow through $S_{5,6}$, depicted in Fig. 4.27a. However, this would require two additional diodes $D_{1,4}$ being rated at the full DC link voltage as well as the full current, which may result in a cost expensive solution. Instead, anti-parallel diodes ($D_{7,8}$) could therefore be used to bypass $S_{2,3}$ and current would flow through the channels of the CoolMos devices whilst turned on. The utilization of anti-parallel diodes $D_{7,8}$ for $S_{2,3}$ could be done with diodes rated at half the DC link voltage only, which could result in a cost attractive solution. The principle for both alternatives are shown in Fig. 4.27.



(a) Non-unity power factor operation using D_1 (Configuration 4)

(b) Non-unity power factor operation using D_7 and S_5 (Configuration 5)

Figure 4.27: Possible current flows for non-unity power factors in the Hybrid-NPC structure

Thus, there are two configurations under investigation for the Hybrid-NPC, for which the semiconductor device utilization is listed in Table 4.6. Before the comparison between the Hybrid-NPC and the SiC based T-Type inverters are given, it is investigated which of the two constellations in Fig. 4.27 will result in lower losses. For the sake of simplicity, diodes $D_{7,8}$ are chosen to be the same devices as $D_{2,3}$

and the results of the investigation are presented in Fig. 4.28, showing a dramatic loss reduction for configuration 4 at low power factors. The result identifies that

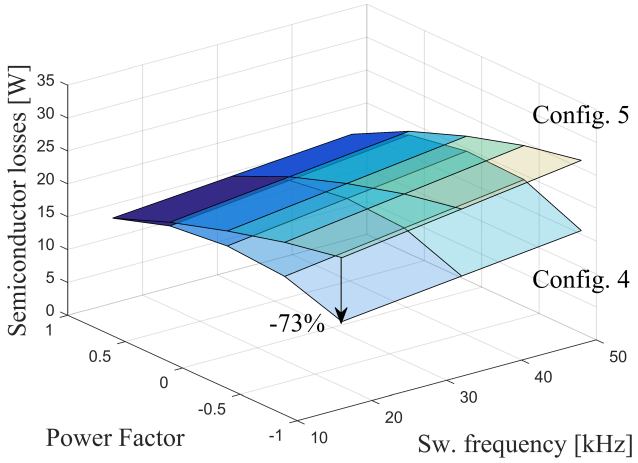


Figure 4.28: Loss comparison of configuration 4 and configuration 5 using two different current paths from Fig. 4.27

a loss reduction from 0 % at unity power factor of up to 73 % at $cos\,(\varphi) = -1$ is possible when choosing configuration 4. The reason for that is that the forward voltage of the 600 V diode ($S_{7,8}$) together with the on-state voltage of the CoolMos device ($S_{5,6}$) lead to conduction losses larger than the conduction losses occurring in $D_{1,4}$ alone when choosing configuration 4. Due to its superior semiconductor loss profile, configuration 4 for the Hybrid-NPC is retained for further comparison against the SiC based alternative (configuration 2).

Having identified in which constellation either topology is most suitable, the comparison results between the SiC based T-Type structure and the Hybrid-NPC structure against the conventional T-Type can finally be presented in Fig. 4.29.

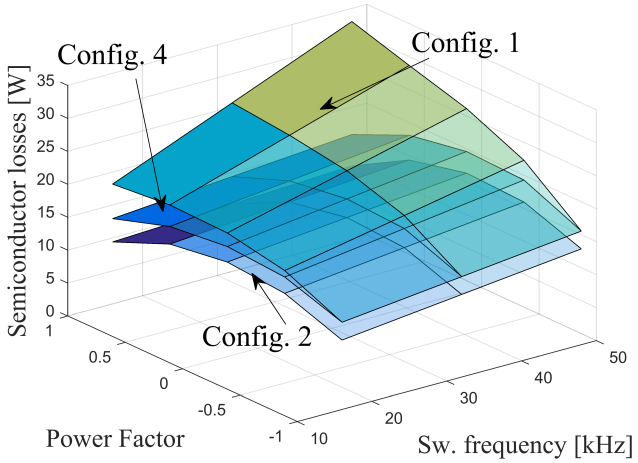


Figure 4.29: Loss comparison of the Si and SiC based T-Type converters and the Hybrid-NPC converter

Several conclusion can be drawn:

- As for the conventional T-Type alternative, semiconductor losses are greatly dependent on the switching frequency at large power factors. This has been pointed out in this work to be because of the large switching losses in the outer switches $S_{1,4}$. Such switching frequency dependency lowers as the power factor decreases. The reason for that is that at low power factors, the switching losses will shift from the outer switches $S_{1,4}$ to the inner bi-directional switches $S_{2,3}$ which have a competitive switching loss characteristic because of their lower breakdown voltages. As a consequence, the design of the T-Type converter operating mainly at low power factors or even as a pure rectifier can be conducted using higher operating frequencies compared to the operating mode of pure inversion.

- Since the Hybrid-NPC converter uses additional CoolMos devices to aid the commutation events in the 1200 V Si IGBTs, this is the operation point where the major loss reduction occurs. It happens at maximum power factor and a significant reduction of semiconductor losses can be seen. Such reduction is even more apparent as the switching frequency increases, as expected. However, the loss reduction due to the utilization of the CoolMos devices becomes less obvious as the power factor decreases. Recalling Fig. 4.28, it is pointed out that the loss profile is superior for the case of the free-wheeling diodes $D_{1,4}$. Since this scenario is exactly the same as for the conventional Si IGBT based T-Type constellation, the Hybrid-NPC loss profile converges to the loss profile of the T-Type structure. This can be seen in Fig. 4.29, when the power factor reaches $cos\,(\varphi) = -1$. Thus the Hybrid-NPC can show the greatest loss reduction at maximum power factor.

- As for the comparison to the SiC based alternative, the major loss reduction is again achieved at unity power factor. For the same reason as pointed out before, the loss reduction occurs in $S_{1,4}$ only. As the power factor decreases, however, losses can still be decreased because of the lower conduction losses in the SiC MOSFET compared to the free-wheeling diode $D_{1,4}$ in case of the Si IGBT T-Type structure. In other words, although the switching losses are completely moved from $S_{1,4}$ to $S_{2,3}$ at $cos\,(\varphi) = -1$, conduction losses can still be reduced with the utilization of SiC MOSFETs. This shows a clear distinction to the Hybrid-NPC converter, whose loss profile converges towards the conventional T-Type structure using Si IGBTs.

A summary for the loss comparison of each configuration against the conventional T-Type structure is given in Table 4.7, showing that the Hybrid-NPC constellation mostly benefits at unity power factor whereas the SiC based alternative (both configuration 2 and configuration 3) gives benefits in both operation modes. If the whole power factor range is to be covered, then configuration 4 can outperform configuration 5 in terms of losses. If the converter operates at unity power factor only, either configuration 4 or configuration 5 can be chosen based on other criteria, e.g. cost or semiconductor count.

Table 4.7: Loss comparison and loss reduction for different configurations. $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$

	$cos\,(\varphi) = 1$		$cos\,(\varphi) = -1$	
	Losses [W]	Loss reduction [%]	Losses [W]	Loss reduction [%]
Configuration 1	22.2	0	13.2	0
Configuration 2	10.8	-51	10.5	-20
Configuration 3	9.2	-58	8	-39.4
Configuration 4	12.9	-42	13.2	0
Configuration 5	12.9	-42	22.9	+73

4.4.2 Cost comparison

So far, only semiconductor losses have been taken into account and compared against each other. Another driving force in the converter design may be the price, though, which is therefore included in this work, because the benefits of both converter alternatives so far seem to come at higher expenses. The SiC based alternative may have a higher semiconductor cost due to the utilization of SiC switching devices, which to date, are more expensive than a Si switching device of an equivalent rating [83, 84]. The Hybrid-NPC converter uses additional switching devices and has thus a higher device count. While other references use the chip area size as a comparison basis [85,86], this work starts with a device price comparison through distribution channels. The reason for that is simply because devices can be bought discrete or as modules and the customer typically has no influence on the chip size. Furthermore, custom made devices are assumed to result in larger cost and seem only reasonable in high production rate, i.e. mass production. Each configuration from the loss comparison is listed in Table 4.8. Also, the cost comparison for each configuration including rectification capability is used, i.e. $cos\,(\varphi) = [-1...1]$. What can be seen in Table 4.8, is, that the conventional Si IGBT based converter in configuration 1 results in a cost expensive solution if also rectification capability

Table 4.8: Price configuration for the entire power factor range $cos\,(\varphi) = [-1..1]$

	Config. 1	Config. 2	Config. 3	Config. 4	Config. 5
$S_{1,4}$	IKW15N120T2 2x3.90 $	C2M0080120D 2x16.03 $	C2M0080120D 2x16.03 $	IKW15N120T2 2x3.90 $	IKW15N120T2 2x3.90 $
$S_{2,3}$	IKP15N60T 2x1.6 $	IKP15N60T 2x1.6 $	SCT2120AF 2x9.07 $	IKP15N60T 2x1.6 $	IKP15N60T 2x1.6 $
$D_{2,3}$	C3D10060A 2x4.02 $	C3D10060A 2x4.02 $		C3D10060A 2x4.02 $	C3D10060A 2x4.02 $
$D_{1,4}$	C4D15120A 2x16.88 $	C4D02120A 2x2.26 $	C4D02120A 2x2.26 $	C4D15120A 2x16.88 $	
$S_{5,6}$				SPP20N60S5 2x5.28 $	SPP20N60S5 2x5.28 $
$D_{5,6}$					C3D02060A 2x0.96 $
$D_{7,8}$					C3D10060A 2x4.02 $
Total	52.80 $	47.82 $	54.72 $	63.36 $	39.56 $

is required. The reason for that lies in the high price of the anti-parallel diodes $D_{1,4}$ which must be rated at a similar current level than the switching devices $S_{1,4}$. Also, the use of SiC for such diodes is considered due to the absence of the reverse recovery and thus reduced switching losses in $S_{2,3}$. In such scenario, the utilization of 1200 V SiC MOSFETs, and thus configuration 2, can end up in a potential cost attractive solution, because they can be used for both operation modes and lower current rated anti-parallel diodes may be chosen to only conduct current during the dead-time intervals. Configuration 3 uses additionally 650 V SiC MOSFETs in the bi-directional path. With the current price of these devices, configuration 3 yields a slightly more expensive solution compared to configuration 1 with only minor semiconductor loss reduction compared to configuration 2. As for the Hybrid-NPC inverter, a large discrepancy in price can be observed depending on which configuration, and thus, current path is chosen.

Configuration 4 is the more efficient solution as the power factor decreases, but clearly at a higher cost. The reason for that is, as for configuration 1, that expensive SiC diodes are used for $D_{1,4}$. Configuration 5, on the other hand, uses two additional 600 V SiC diodes $D_{7,8}$ and the CoolMos' channel, and can hence be designed without costly 1200 V SiC diodes rated at the full current, which then reduces the cost significantly. Therefore, to give a fairer cost comparison, expenses are compared to each other when the converter is operating at unity power factor only, as conventional standalone PV inverters do to date. For unity power factor, the cost analysis is given in Table 4.9.

Table 4.9: Price configuration for unity power factor only, $cos\,(\varphi) \approx 1$

	Config. 1	Config. 2	Config. 3	Config. 4	Config. 5
$S_{1,4}$	IKW15N120T2 2x3.90 $	C2M0080120D 2x16.03 $	C2M0080120D 2x16.03 $	IKW15N120T2 2x3.90 $	IKW15N120T2 2x3.90 $
$S_{2,3}$	IKP15N60T 2x1.6 $	IKP15N60T 2x1.6 $	SCT2120AF 2x9.07 $	IKP15N60T 2x1.6 $	IKP15N60T 2x1.6 $
$D_{2,3}$	C3D10060A 2x4.02 $	C3D10060A 2x4.02 $		C3D10060A 2x4.02 $	C3D10060A 2x4.02 $
$D_{1,4}$	C4D02120A 2x2.26 $	C4D02120A 2x2.26 $	C4D02120A 2x2.26 $	C4D02120A 2x2.26 $	
$S_{5,6}$				SPP20N60S5 2x5.28 $	SPP20N60S5 2x5.28 $
$D_{5,6}$					C3D02060A 2x0.96 $
$D_{7,8}$					C3D02060A 2x0.96 $
Total	23.56 $	47.82 $	54.72 $	34.12 $	33.44 $

Considering only the operation close to unity power factor gives a cost benefit for the conventional T-Type structure (configuration 1) because the free-wheeling diodes associated with $S_{1,4}$ can also be rated at a lower current now. For the following analysis, the SiC diode C4D02120A will be used for $D_{1,4}$ in all configurations except configuration 5, which will use two 600 V rated low current SiC diodes C3D02060A in anti-parallel to $S_{2,3}$ as well as $S_{5,6}$. What can be seen in Table 4.9 is, that the SiC based alternative in configuration 2 will not be a cost competitive solution anymore because the unipolar characteristics of the SiC MOSFETs do not fully

apply anymore, thus at high power factors, the comparison will be moved back to a single switching device comparison of Si IGBT versus SiC MOSFET again. It is also worthy of comment that configuration 4 became a cost competitive solution compared to configuration 5 because of the utilization of low cost 1200 V SiC diodes for $D_{1,4}$. Thus, the distinction between configuration 4 and configuration 5 can be moved to other criteria, for instance the converter design complexity, which is especially true when discrete components are used, because configuration 5 clearly uses a higher count of semiconductor devices.

4.4.3 Price discussion on SiC based converter

Since the price comparisons in Table 4.8 and Table 4.9 are based on the prices through distribution channel, and having in mind that manufacturers for SiC switching devices have not fully started mass production yet, the large price difference may vanish in the (near) future with mass production [87] and goals of selling prices of 0.1 \$/A for 1200 V SiC MOSFETs by the year 2019 have been reported [88]. Furthermore, a dramatic price fall has been experienced when it comes to SiC MOSFETs and a forecast estimates that SiC cost will reduce from a current factor of 10 down to a factor of 1.2 of the cost of Si in the next ten years [89]. Another argument for the use of SiC switching devices is that due to the properties of SiC material, a smaller chip size can be used compared to the Si IGBT device. Instead of using the same rated current at 25 °C as a common basis (as it has been done until now), this section uses the same junction temperature in $S_{1,4}$ as a comparison basis, and investigates how much the chip size for the SiC switching device can be reduced. This approach is based on [86]. This work, however, assumes that the switching energies will not change with the chip size. While in theory, a smaller chip size would result in smaller internal capacitances and thus enhance the switching speeds, this work assumes the same package parasitics and that the already very small switching energies (especially for the turn off commutations) are mainly limited by the parasitic inductances. In other words, any increase in dv/dt or di/dt will be counteracted by the package parasitics resulting in large and unwanted oscillations. This work therefore only considers a change in conduction losses according to

$$P_{con} = \frac{R_{on,nom} A_{SiC,nom}}{A_{SiC}} I_{rms}^2 \quad , \tag{4.12}$$

where $R_{on,nom}$ is the on-resistance from the SiC MOSFET used in this work (Fig. 4.3), $A_{SiC,nom}$ is the corresponding chip size of the device and A_{SiC} is the theoretically reduced chip size. The chip size of the 1200 V SiC MOSFET C2M0080120D can be found on the manufacturer's website to be

$$A_{SiC,nom} = 0.310\,\text{cm} \cdot 0.336\,\text{cm} \quad . \tag{4.13}$$

The thermal resistances for several Cree SiC MOSFETs with different current ratings are taken from their datasheets to relate the thermal resistance to the chip size, shown in Fig. 4.30. Using the loss modeling approach, the average junction temperature of the Si IGBT reaches 88 °C at 1.5 kW and 16 kHz operation. The junction temperatures for the different chip sizes in the SiC MOSFET used in $S_{1,4}$ are presented in Fig. 4.31a detailing that the size can be approx. halved until the SiC and Si alternative for $S_{1,4}$ have the same junction temperatures.

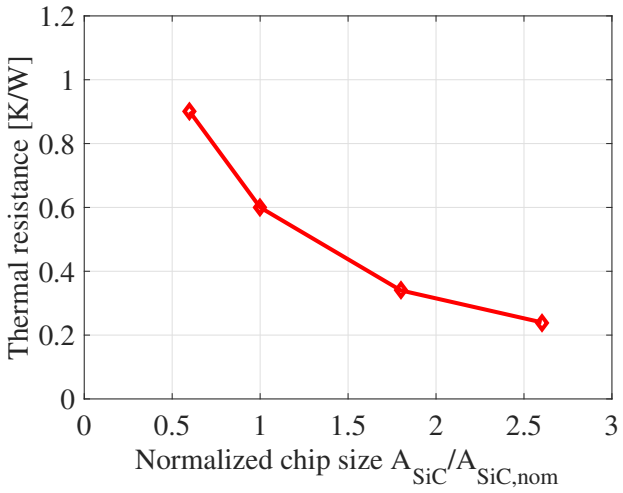
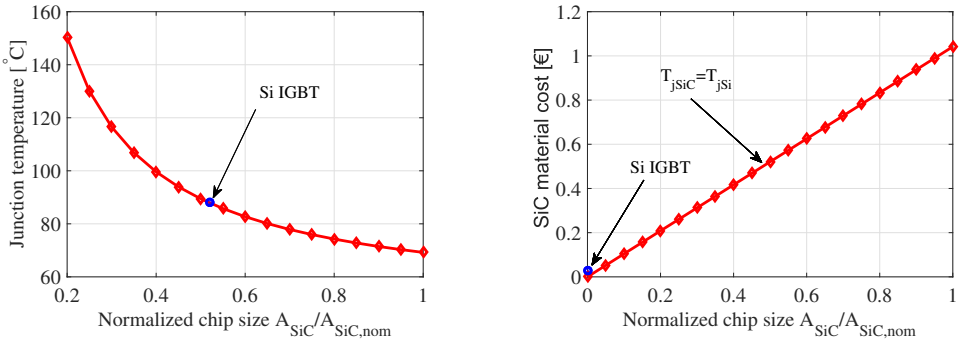


Figure 4.30: Thermal resistance against different chip sizes



(a) Junction temperature of SiC MOSFET against reduced chip size

(b) Material cost of SiC MOSFET against reduced chip size

Figure 4.31: Junction temperature against chip size in (a) and material cost against chip size in (b)

With a material cost of 10 €/cm^2 for SiC against 0.1 €/cm^2 for Si [84], the price can be halved as well. Although the chip size can be reduced by around 50 %, the cost for the SiC material is still beyond the material cost for the Si IGBT. This analysis reveals that some of the superior properties of SiC, such as low conduction and switching losses, compared to the Si IGBT can not inherently overcome the high price for SiC material to date. In other words, even if manufacturing cost would be equal for both kind of switching devices, the SiC MOSFET would still be more expensive device in the T-Type inverter with the specifications presented in this work. If and how the price for SiC material will change in the (near) future and how the price change will influence the converter design cost is beyond the scope of this work.

4.5 Summary

Due to the unusual operation principle of the T-Type structure, its outer switches must be rated at the full DC link voltage whilst its inner bi-directional switches can be rated at half the DC link voltage. This yields a loss performance that is strongly dependent on the operation mode. At conventional PV inverters, which are only feeding energy to the grid, the outer switches show a high loss profile that is easily affected by the chosen switching frequency. A direct replacement of such devices with equivalently rated SiC MOSFETs can greatly reduce the high losses and also significantly reduce the switching frequency influence on the switching losses. This solution, however, results in a very cost expensive alternative because of the high price for SiC switching devices to date. Even if the chip size of the SiC switch is reduced to achieve the same junction temperatures, the material cost for such device would still be higher. Using the Hybrid-NPC converter as an alternative approach striving towards a more complex topology, the losses associated with the T-Type structure can also be greatly reduced. Although the loss reduction with the modulation principle presented in this work is not as much as the SiC based alternative, it can be a cost attractive solution compared to the SiC converter.

If the operation capabilities of the inverter are extended to cover a wide range of power factors, the SiC MOSFET based alternative can become not only a loss benefit solution, but also at a comparable cost, because externally placed free-wheeling diodes rated at the full current are not necessary anymore with the usage of SiC MOSFET. This is in contrast to the Hybrid-NPC structure, whose loss benefits converges to zero as the power factor decreases; and it comes with the highest cost.

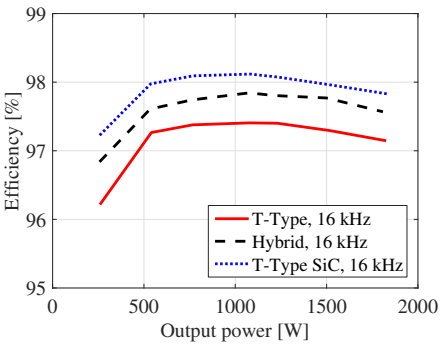
Chapter 5

Design Alternatives

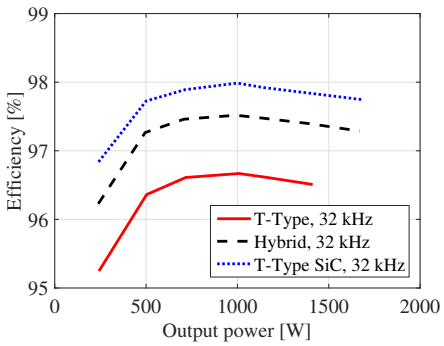
Based on the previous chapter, in which semiconductor loss reduction at the expense of increased semiconductor cost is evaluated, this chapter is intended to introduce different design objectives that could be applied with the utilization of SiC switching devices. For all cases, unity power factor is assumed as to date, this is where the converter mainly operates.

5.1 Efficiency Improvements and Reliability

The first aspect deals directly with the loss reduction which would yield in a higher efficiency. Although the aim of this dissertation is not to optimize the converter for highest possible efficiency, measurements on the overall converter have been conducted with a N4L PPA5500 power analyzer. Efficiency curves for all three prototypes are given in Fig. 5.1, confirming that the SiC based alternative can achieve highest efficiencies, followed by the Hybrid-NPC, and then the conventional Si based T-Type.



(a) Efficiency curves for 16 kHz switching frequency

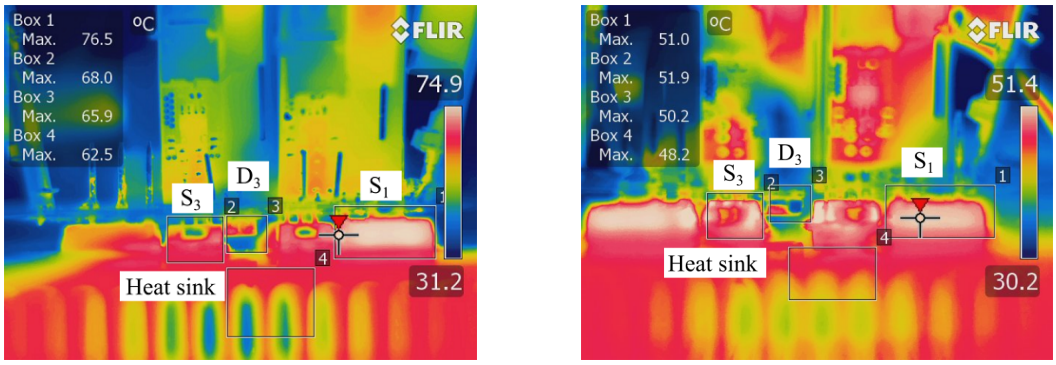


(b) Efficiency curves for 32 kHz switching frequency

Figure 5.1: Measured overall converter efficiencies for different switching frequencies

A higher efficiency may be beneficial considering the FIT, which is taken for Germany to be 0.13 €/kWh. Furthermore, an average solar irradiation of 4 h per day is assumed, i.e. 1460 h annually. As pointed out in Sec. 4, operating at 1.5 kW per phase, a loss reduction of 8.8 W per phase is achieved. Considering the higher price due to the semiconductors, i.e. 24.46 $ (approx. 22.28 €), the payback time would be more than 12 years.

However, the value in lower semiconductor losses could also be found in a more reliable operation in terms of less thermal stress among the devices. A direct comparison for the Si and SiC T-Type converter is given in Fig. 5.2.



(a) Case temperatures for the Si based converter

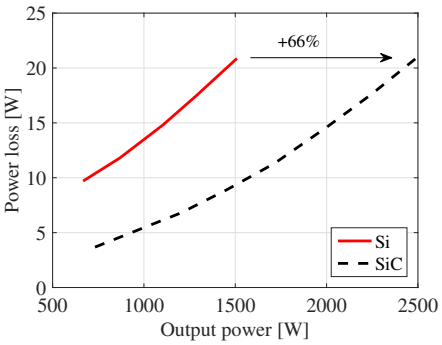
(b) Case temperatures for the SiC based converter

Figure 5.2: Case temperature measurements for the Si and SiC alternative

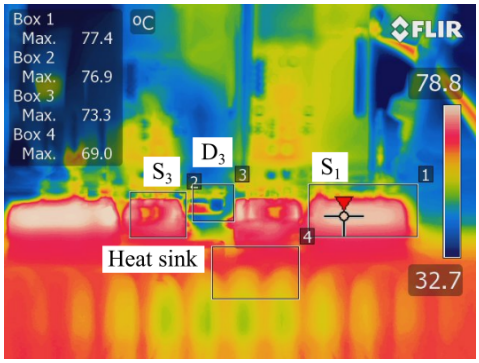
The Si based converter clearly operates at higher temperatures, especially for its outer switches $S_{1,4}$, which show a case temperature of 76.5 °C for the Si IGBT against 51 °C for the SiC MOSFET. It is interesting to note that due to the common heat sink and a close arrangement of the semiconductors to achieve short commutation loops, the adjacent devices in Fig. 5.2a automatically experience a higher thermal stress. Thus for the same cooling effort, reduced losses in $S_{1,4}$ can clearly reduce thermal stress of the other semiconductor devices.

5.2 Increased Output Power Rating

Taking advantage of the reduced losses in the SiC based converter, one might want to increase the output power rating until the same overall semiconductor losses are achieved. With the specifications in this dissertation in terms of modulation strategy and input voltage, potential output power increase of more than 60 % is possible. In particular, output power can be increased from 1.5 kW up to 2.5 kW while still achieving a thermal stress at the case of less than 80 °C for each semiconductor device.



(a) Possible increase in output power

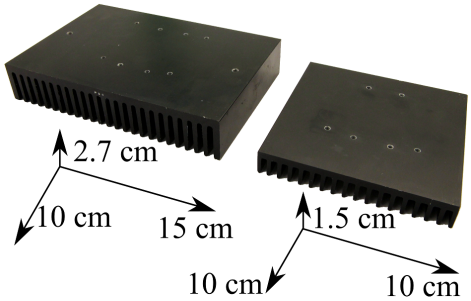


(b) Case temperatures for the SiC based converter operating at 2.5 kW output power for the same cooling effort

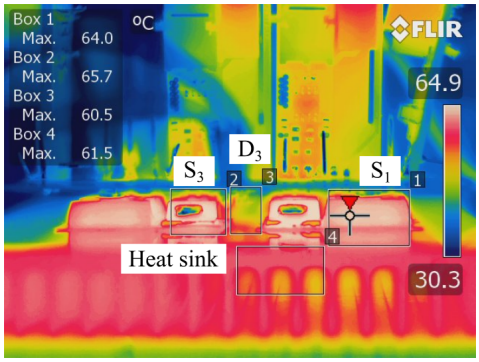
Figure 5.3: Possible increase in output power in (a) and resulting case temperature measurements in (b)

5.3 Heat Sink Size Reduction

If the design objective is to achieve a higher power density, this could be done by reducing the size of the heat sink. From the loss modeling approach presented in this work, the heat sink thermal resistance is increased from 1.25 K/W initially to 2 K/W to achieve a similar case temperature as for the Si IGBT based system. The volume size reduction as well as the resulting thermal pictures are shown in Fig. 5.4. Not only is the size reduced by more than 60 %, but also the cost for cooling; from initially 16.76 $ down to 11 $.



(a) Reduced heat sink size



(b) Case temperatures for the SiC based converter with the smaller heat sink

Figure 5.4: Reduced heat sink size in (a) and resulting case temperature measurements in (b)

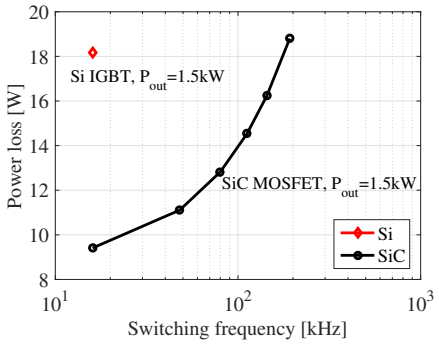
5.4 Filter Size Reduction

A major argument for the utilization of SiC MOSFETs is the capability to operate at higher switching frequencies. This section discusses the size reduction of the

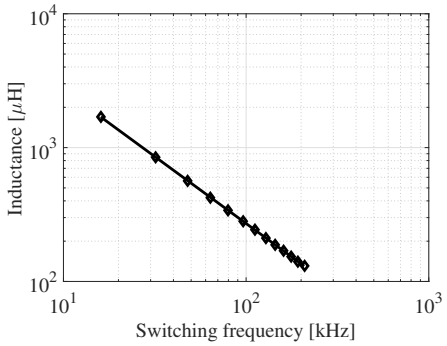
inverter side inductance of an LCL filter, for which design guidelines can be found in various references (e.g. in [90–92]). Following the commonly used design practice to limit the current ripple to 20 % of the maximum current, the relationship between inductance and switching frequency for PD PWM can be written as [93]

$$L = \frac{V_{DC}}{16 f_{sw} 0.2 \hat{I}} \quad . \tag{5.1}$$

The relationship between the inductance and the switching frequency is shown in Fig. 5.5b. While the switching losses in the SiC MOSFET are so much lower, the break even point for the same semiconductor losses than for the Si based system is at around 200 kHz, shown in Fig. 5.5a.



(a) Possible switching frequency increase with SiC based converter



(b) Reduced filter inductance for increased switching frequencies

Figure 5.5: Semiconductor losses versus switching frequency in (a) and resulting grid side inductance reduction in (b)

Due to the inverse proportional relationship between the inductance and switching frequency, one can see that the major reduction in inductance is achieved at rather low switching frequencies. Also, having in mind that the losses in the inductor are a strong contributor in the overall efficiencies, especially at high switching frequencies due to the core losses and AC winding resistance, the increase of switching frequency is investigated from 16 kHz to 48 kHz. The comparison follows the assumption that at these switching frequencies, the same core material (Kool Mu) can still be used. The same toroid material and geometry is used and the sample price remains the same, i.e. 25 $. Based on the design guidelines from the manufacturer, the copper length needed for the 16 kHz inductor would be 6.6 m against 3 m for the 48 kHz inductor. The price for copper is given to be approx. 1.65 $/m. This gives a cost reduction from 11.35 $ for the 16 kHz inductor down to 5.19 $ for the inductor designed for 48 kHz operation.

5.5 Summary

This section has briefly introduced several possible design alternatives with the SiC based T-Type alternative, as this is the most expensive configuration for unity power factor operation. A direct replacement without any additional redesign on

the converter results in higher efficiencies and thus lower thermal stress, as expected, but the increased cost for the semiconductors would require a large payback time. Therefore, additional benefits in higher efficiencies can be found, because of the lower thermal stress among the devices. This particular benefit can be used to significantly increase the output power of the converter without a reconsideration for the choice of the inner bi-directional semiconductor devices. The lower losses can also be used to reduce the cooling effort on the converter - in this work up to 63 % in volume while achieving similar thermal stress among the semiconductor devices. Lastly, the superior switching performance of the SiC devices can be used to increase the switching frequency and thus to reduce the size of the filtering aspects. A 12 fold increase in the switching frequency is possible until the total semiconductor losses are equal to the Si based T-Type inverter at 1.5 kW and 16 kHz switching frequency. However, since the AC filter is typically another major contributor to the overall losses, a complete redesign and a thorough investigation on the design trade-offs for such are thus necessary.

Chapter 6

Conclusion

This project has investigated in depth the weak points associated with the three-level T-Type converter. While such topology can achieve lower conduction losses compared to the more commonly used NPC structure, and can thus be seen as an attractive alternative, its outer switches must be rated at least at the full DC link voltage and therefore experiences larger switching losses, which then constraints the switching frequency choice. The semiconductor devices in the bi-directional path, on the other hand, can be rated at half the DC link voltage and can therefore demonstrate reduced semiconductor loss performances.

The results in this dissertation show that the loss reduction in the T-Type converter can be achieved in several ways, for instance using SiC switching devices or using additional 600 V Si devices to aid the commutation events. Using semiconductor devices made of SiC, two promising alternatives could be chosen from, i.e. the normally-off SiC MOSFET and the normally-on SiC JFET. Both devices have their particular advantages and drawbacks, but the SiC MOSFET is considered the more efficient device at high switching frequency operation due to its lower turn off energies compared to the SiC JFET. Also, the SiC MOSFET can easily be utilized in a VSC due to its normally-off characteristic and the gate driver adjustments are only minor.

With the SiC MOSFET implemented, semiconductor loss reductions of more than 50 % at unity power factor and full load are experimentally verified. Such loss reduction benefit is paid with a higher semiconductor material cost for SiC, which to date is around 100 times higher compared to Si for the same chip size. However, if bi-directional power flow of the converter is considered a possible scenario, the SiC based inverter can not only achieve a loss reduction, but also at a lower price because the MOSFET can be used for both current directions which reduces the current rating of its free-wheeling diode and thus cost.

Due to the drawbacks with SiC switching devices to date, a more advanced topology could be used by strategically adding 600 V devices into the circuit that will aid the commutation events, resulting in a mixture of the conventional NPC and the T-Type alternatives. Such approach can reduce the losses by up to 42 % under

the same operating condition and it can be a cost attractive alternative to the utilization of expensive SiC switching devices. However, if the whole power factor range is considered, the benefits of the Hybrid-NPC topology vanish as the loss profile converges to the loss profile of the conventional T-Type converter. This is due to the fact that the commutation events are shifted from the outer switching devices towards the inner bi-directional devices and therefore, the additional 600 V CoolMos devices will not support the large loss outer switching devices anymore.

The results from this study highlight that:

- High efficiencies can be achieved with the T-Type converter compared to the NPC alternative if the switching frequency is kept at low values and that the switching frequency is a fundamental design constraint in the T-Type converter using conventional Si devices.
- For PV inverters operating at near unity power factor, only two devices per phase leg need to be upgraded with SiC devices in order to achieve a significant loss benefit.
- A great loss reduction can also be achieved with a more complex Si based Hybrid-NPC converter, which can be an attractive and potentially cost effective alternative.
- Direct access to semiconductor losses only within a converter operating context can be achieved with a non conventional, simple but effective thermal measurement approach.

Chapter 7

Future work

This work has developed analytical loss models and verified them within a converter operating context using an alternative measurement approach. By doing so, weak points of a particular converter topology in an operating context could be identified and alternative approaches accurately evaluated. However, this work did not cover parts of the rest of the converter such as AC filter design, modulation and control to fully evaluate both topological solutions.

With the knowledge obtained in this work, an optimization routine for the overall converter can be initiated. As pointed out in this work, both solutions to date increase the semiconductor cost and circuit complexity. The higher cost for both solutions greatly overcome the major drawbacks associated with the T-Type converter, and increased switching frequency operation without an excessive thermal stress are now possible. Future work may therefore include:

7.1 Optimization of Hybrid-NPC Converter

The Hybrid-NPC converter could be optimized in several ways, of which one is briefly discussed here. The first optimization approach is linked to the selection of the 600 CoolMos devices. As pointed out in Fig. 4.17c, a current divider is used to reduce the current stress through the devices by simply paralleling their impedances. In Fig. 4.18, the current sharing is found out to be 1/3 and 2/3 for the CoolMos and the 1200 V IGBT path, respectively. The question arises how the current sharing is affected if a CoolMos device with a different on-resistance is chosen. Therefore, on a DPT, a 100 mΩ resistance is placed in series with the CoolMos device, thus increasing the impedance in this particular current path. The measured load current and the current through the CoolMos device S_6 are shown in Fig. 7.1. The result reveals that the increased impedance of S_6 causes less current (now approx. 1/5 only) flowing through the device. Therefore, an investigation could be done if a CoolMos with a larger on-resistance could be beneficial in reducing losses in the Hybrid-NPC converter. This would most likely also result in a cheaper device since a smaller chip size can be used for the CoolMos FET.

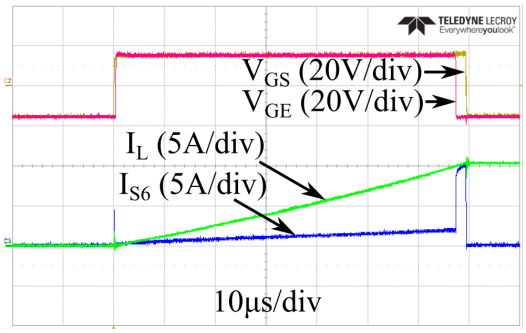


Figure 7.1: Inductor current and current through $S_6 + 100\,\mathrm{m\Omega}$ when both S_6 and S_4 are turned on

7.2 Inductor redesign

As pointed out in Chap. 5, the increase in switching frequency up to 48 kHz can greatly reduce the value of the converter side inductance and thus may lead to a cheaper inductor. However, the analysis did not include any loss modeling approach, as there are many different considerations to take into account when it comes to low loss design, such as core material cost, AC winding resistance and core loss predictions and typically the use of Finite Element Methods (FEMs) is required. Furthermore, an experimental verification of such inductor design with adequate accuracy is a challenging task. Therefore, an investigation into the optimized redesign of the converter side inductor for high efficiency at increased switching frequencies would be a reasonable next step since the AC filter is typically another major loss contributor to the converter losses.

7.3 EMC

For a commercial system, the Electromagnetic Compability (EMC) requirements are to be satisfied and thus proper EMC filtering may be necessary. Previous work has investigated the influence of the fast switching dv/dt and di/dt on the Electromagnetic Interference (EMI) and has highlighted the need for improved filtering with the use of SiC switching devices [40, 94]. Therefore, an investigation on the trade-offs between switching losses and EMI, and thus filtering aspects concerning volume and price will lead to a more complete evaluation on the use of SiC devices for high efficient, high power density converters.

7.4 High switching frequency operation

Due to the very low switching losses of the SiC MOSFETs, switching frequencies can be significantly increased (even beyond 48 kHz) until the same semiconductor losses are reached. This increase in switching frequency could be used to change the differential mode filter from a conventional LCL filter to a single L filter while still fulfilling the grid codes. Connecting the inverter to the grid with a single L filter could be advantageous because a conventional LCL filter typically requires an

additional resistive element to achieve proper damping at the resonance frequency, which then degrades the converter efficiency. This could be avoided with a single L filter, however, since the single inductor now needs to give the necessary attenuation of current harmonics, its inductance will be larger compared to the converter side inductance in a conventional LCL filter. While this is typically achieved with a larger number of turns, a large AC resistance in the windings would be expected as well as larger core losses. The feasibility of utilizing a single stage L filter from a loss and cost point of view could be an interesting investigation for the use of SiC based inverters.

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Appendix A

Calibration Procedure of Thermal Measurements

This chapter elaborates on the methodology of the measurement technique used in this work. Since electrical input and electrical output measurements may lead to large inaccuracies due to the difficulties in measuring high speed pulse-width signals, thermal measurements have been chosen. Since semiconductor devices are typically mounted on heat sinks in order to stay within their thermal limits, the heat sinks will consequently experience a temperature rise as well. This temperature rise is measured until a steady state condition is reached. To avoid influences from the closest surroundings such as gate drivers, the balancing resistors from the DC link capacitors or the AC filter, the heat sink is thermally decoupled from the converter using a wooden cutout board as depicted in Fig. A.1. The relative temperature difference between the input ambient temperature and the heat sink temperature is then readily obtained using

$$\Delta T = T_{HS} - T_{amb} \quad . \tag{A.1}$$

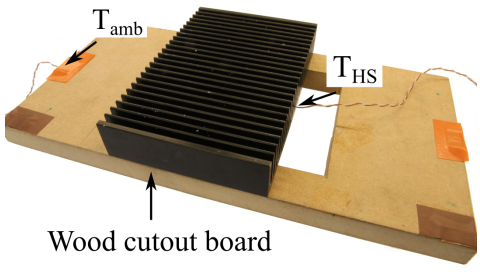
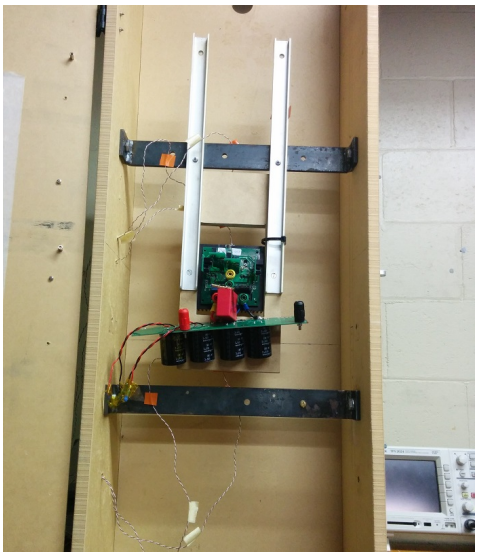


Figure A.1: Backside of the converter. Thermal measurements are performed directly on the heat sink T_{HS} and below the heat sink T_{amb}

To avoid further influences from the surroundings, the whole test system is put in an open ended closet (chimney) as shown in Fig. A.2a and Fig. A.2b. While the converter is operating according to the specifications in Table 4.4, thermal measurements are being conducted which can be used to identify the semiconductor losses



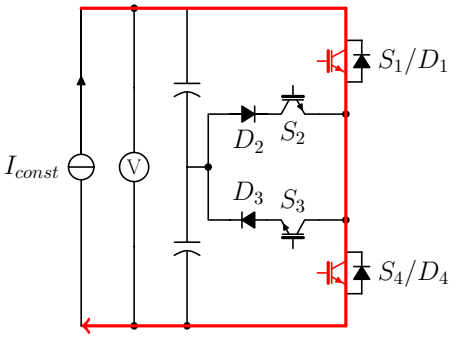
(a) Backside of the converter. Thermal measurements are performed directly on the heat sink T_{HS} and below the heat sink T_{amb}

(b) Open ended chimney during thermal measurements

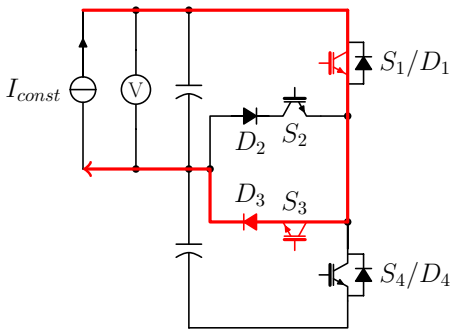
Figure A.2: Front view of converter in open ended chimney in (a) and thermal measurements performed inside in (b)

during this particular operating point. The key essence of this kind of measurements is to perform a thorough calibration using known heat loads. The calibration procedure uses the semiconductor devices themselves as heat sources, but they are operated differently during the calibration procedure. Instead of operating the converter in PWM mode according to Table 4.4, several switch pairs are hard turned on whilst others are completely turned off. The power supply at the input of the converter is set to current limitation mode, representing a constant current source. This is demonstrated in Fig. A.3 for different switch pairs. The current limitation function at the input of the converter results in a voltage caused by the voltage drop of the particular device pairs. These DC currents and voltages can easily be measured using an oscilloscope, and thus the input power is obtained. By measuring the relative temperature rise according to Eq. (A.1), the injected thermal energy into the heat sink can then be identified.

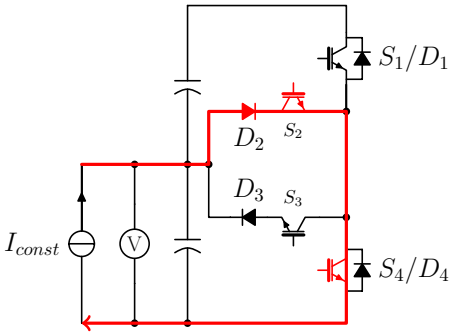
Note that care must be taken that the system operates in a thermal steady state condition, shown in Fig. A.3d. Also, the procedure must be repeated for different device pairs to achieve a thorough thermal profile of the heat sink. Then the steady state relative temperatures above ambient for each switch pair can be averaged. This procedure is repeated for several power levels (by simply increasing the current limitation) such that a relationship between relative temperature rise against power can be obtained. This is illustrated in Fig. A.4, showing a linear fit as one might expect for a constant heat sink thermal impedance. Now that the relation between temperature and semiconductor loss is established, the converter can be operated in its usual way, e.g. in Fig. 4.22 and the heat sink temperature rise, again, is measured in the same manner shown in Fig. A.1 and Fig. A.2. In thermal steady state, the obtained heat sink temperature rise can now be inserted in the relationship obtained in Fig. A.4 and hence only the semiconductor losses are readily available.



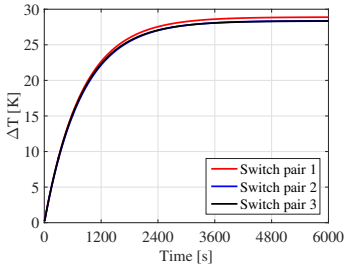
(a) Switch pair 1: S_1 and S_4 conducting



(b) Switch pair 2: S_1, S_3 and D_3 conducting



(c) Switch pair 3: D_2, S_2 and S_4 conducting



(d) Relative temperature rise ΔT versus time for different configurations

Figure A.3: Calibration procedure for heat sink

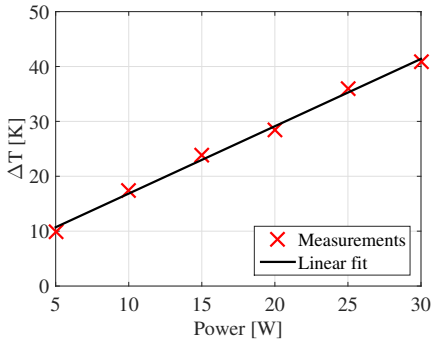


Figure A.4: Calibration fit

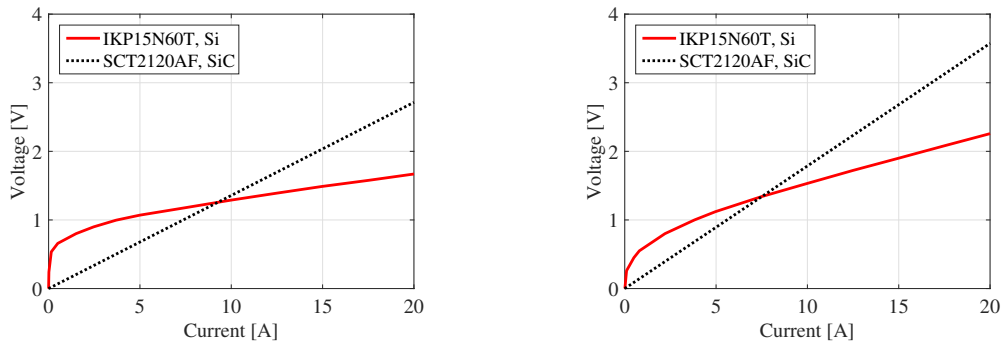
Appendix B

Comparison of 600 V devices

This chapter gives a comparison of Si and SiC switching devices in the 600 V range and the results of this comparative study are used in Chap. 4. Following the approach of using datasheet information for conduction loss calculations and in-circuit switching transition measurements for switching loss calculations, the chosen 600 V Si IGBT is compared against the 650 V SiC MOSFET.

Conduction losses

Forward voltages of the two switching devices used in the bi-directional path in the T-Type and Hybrid-NPC converters are shown in Fig. B.1, detailing that the superior conduction characteristics of the SiC MOSFET are less significant compared to the 600 V Si IGBT.



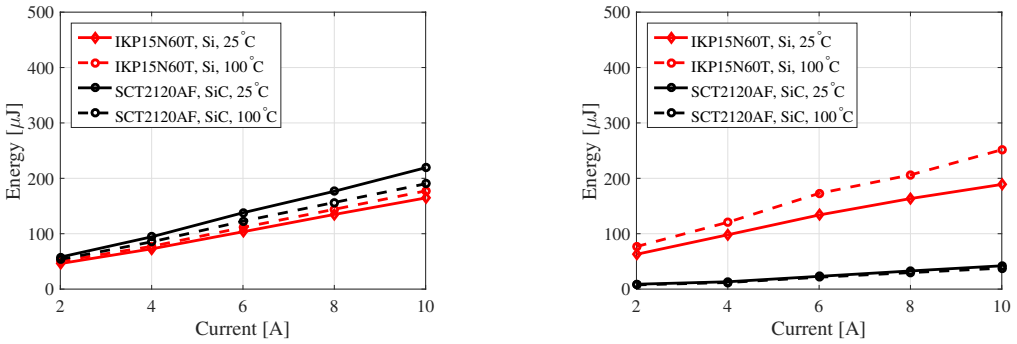
(a) Forward voltage drop at a junction temperature of 25 °C

(b) Forward voltage drop at a junction temperature of 175 °C

Figure B.1: Forward voltages for a 600 V Si IGBT and a 650 V SiC MOSFET at different current levels and junction temperatures

Switching losses

Using the DPT setup from [65], the switching energies for both devices can be obtained to predict switching losses when the converter operates at non-unity power factor. Fig. B.2 shows these measured energies for different current levels and junction temperatures.



(a) Turn on energies

(b) Turn off energies

Figure B.2: Switching energies of the utilized 600 V Si IGBT and 650 V SiC MOSFET for two different junction temperatures

It is interesting to note that the SiC MOSFET has slightly higher turn on energies compared to the Si IGBT. However, as the junction temperature increases, turn on energies of the SiC switching device reduces greatly whereas the turn on energies of the Si switching devices slightly increases. This can, once again, be explained by the decreased threshold voltage of the SiC device at increased temperatures as well as the increased transconductance [68–70]. The superior performance of the SiC alternative can be identified in the turn off energies, which are greatly reduced compared to the conventional Si device, which has typically larger turn off energies due to its tail current.

Appendix C

Equations for semiconductor average and RMS current calculations

The semiconductor loss models used throughout this project use datasheet information for conduction loss calculations, and in-circuit switching transition measurements to determine switching losses. Therefore, it is necessary to obtain the average and RMS currents, for which the equations are listed in this section of the thesis.

C.1 Average and RMS currents for boost converter

The calculations for the average and RMS currents in the boost converter can be found in [67]. In particular, the average current through the switch $I_{AV,S}$ is given to be

$$I_{AV,S} = dI_{L,DC} \quad , \tag{C.1}$$

where d represents the duty cycle and $I_{L,DC}$ is the inductor DC current. Similarly as for the switch, the current through the boost diode $I_{AV,D}$ can be determined as

$$I_{AV,D} = (1-d)\, I_{L,DC} \quad , \tag{C.2}$$

The RMS current through the switch $I_{RMS,S}$ is defined as

$$I_{RMS,S} = I_{L,DC}\sqrt{d}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I_{L,DC}}\right)} \quad , \tag{C.3}$$

where Δi is the peak ripple current (not the peak-peak ripple current) defined as

$$\Delta i = \frac{V_{in} d T_{sw}}{2L} \quad , \tag{C.4}$$

where V_{in} is the input voltage of the converter, T_{sw} the switching period and L the inductance. The RMS current through the diode $I_{RMS,D}$ is then

$$I_{RMS,D} = I_{L,DC}\sqrt{1-d}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I_{L,DC}}\right)} \quad , \tag{C.5}$$

C.2 Average and RMS currents for T-Type converter

Average and RMS calculations for the T-Type converter are thoroughly presented in [51] and [95]. The average current in $S_{1,4}$ can be determined according to

$$I_{AV,S1,4} = \frac{\hat{I}_{out}M\left[sin(\varphi)+(\pi-\varphi)cos(\varphi)\right]}{4\pi} \tag{C.6}$$

where $\hat{I}_{out}$ is the peak value of the load current, M is the modulation index and φ the phase displacement between voltage and current. For the inner bi-directional devices, average currents $I_{AV,S2,3,D2,3}$ are

$$I_{AV,S2,3,D2,3} = \frac{\hat{I}_{out}M\left[-2sin(\varphi)+(2\varphi-\pi)cos(\varphi)+\frac{4}{M}\right]}{4\pi} \quad . \tag{C.7}$$

The anti free-wheeling diodes $D_{1,4}$ have average currents according to

$$I_{AV,D1,4} = \frac{\hat{I}_{out}M\left[sin(\varphi)-\varphi cos(\varphi)\right]}{4\pi} \quad . \tag{C.8}$$

The RMS currents through $S_{1,4}$ are

$$I_{RMS,S1,4} = \hat{I}_{out}\sqrt{\frac{M\left[1+cos^2(\varphi)+2cos(\varphi)\right]}{6\pi}} \tag{C.9}$$

The RMS currents through the inner bi-directional path are

$$I_{RMS,S2,3,D2,3} = \hat{I}_{out}\sqrt{\frac{3\pi-8M+4Msin^2(\varphi)}{12\pi}} \quad . \tag{C.10}$$

Finally, RMS currents through $D_{1,4}$ can be calculated according to

$$I_{RMS,D1,4} = \hat{I}_{out}\sqrt{\frac{M\left[4sin^2(\frac{\varphi}{2})-sin^2(\varphi)\right]}{6\pi}} \quad . \tag{C.11}$$

C.3 Average and RMS currents for Hybrid-NPC converter

Now, since the Hybrid-NPC converter can be seen as a mixture between the conventional NPC and the T-Type structure, the equations for the average and RMS currents are slightly modified according to the operating principle. In particular, the inner bi-directional switches $S_{2,3}$ now conduct current when the converter output voltage is both in $\pm V_{DC}/2$ or 0. This means that the average and RMS currents

through $S_{2,3}$ comprise now of the average and RMS currents from the conventional T-Type structure plus an additional amount of current whenever the converter is in the positive or negative output stage. In particular, the average current for $S_{2,3}$ is given as

$$I_{AV,S2,3} = I_{AV,S2,3,TType} + I_{AV,S2,3,additional} \tag{C.12}$$

with $I_{AV,S2,3,TType}$ presented in Eq. (C.7) and $I_{AV,S2,3,additional}$ given by

$$I_{AV,S2,3,additional} = \frac{1}{2\pi}\int_{0+\varphi}^{\pi} \frac{1}{3}\hat{I}_{out} sin(\omega t - \varphi) mod1_{S2,3}(t) dt \quad , \tag{C.13}$$

where $mod1_{S2,3} = M sin(\omega t)$ is the modulation function for the switches $S_{2,3}$ for the when $S1, 4, 5, 6$ are clamping the converter output voltage to the positive or negative DC rails. Note that $\frac{1}{3}$ takes into account the current sharing for the devices used in this thesis. The MAPLE result of Eq. (C.13) becomes then

$$I_{AV,S2,3,additional} = \frac{\hat{I}_{out} M \left[2cos(\varphi)\pi + sin(\varphi - 2\pi) + sin(\varphi) - 2cos(\varphi)\varphi\right]}{24\pi} \quad . \tag{C.14}$$

The RMS current through $S_{2,3}$ can be calculated as

$$I_{RMS,S2,3} = \sqrt{I^2_{RMS,S2,3,TType} + I^2_{RMS,S2,3,additional}} \quad , \tag{C.15}$$

where $I_{RMS,S2,3,TType}$ is given in Eq. (C.10) and $I^2_{RMS,S2,3,additional}$ is given according to

$$I^2_{RMS,S2,3,additional} = \frac{1}{2\pi}\int_{0+\varphi}^{\pi} \left(\frac{1}{3}\hat{I}_{out} sin(\omega t - \varphi)\right)^2 mod1_{S2,3}(t) dt \quad , \tag{C.16}$$

The MAPLE result of Eq. (C.16) is given as

$$I^2_{RMS,S2,3,additional} = \frac{\hat{I}^2_{out} M \left[8cos(\varphi) + cos(3\pi - 2\varphi) - 3cos(\pi - 2\varphi) - 6cos(\pi)\right]}{6^3\pi} \quad . \tag{C.17}$$

As for the additional CoolMos devices $S_{5,6}$, the average current can be calculated as for the switches $S_{1,4}$ in the conventional T-Type structure, but with only a third of the load current with the device constellation in this work, such that the equation from Eq. (C.6) becomes

$$I_{AV,S5,6} = \frac{\hat{I}_{out} M \left[sin(\varphi) + (\pi - \varphi)cos(\varphi)\right]}{3 \cdot 4\pi} \quad , \tag{C.18}$$

which gives the same result as in Eq. (C.14). The RMS current can be calculated as for the switches $S_{1,4}$ in the conventional T-Type structure, but with only a third of the load current with the device constellation in this work, such that the equation from Eq. (C.9) becomes

$$I_{RMS,S5,6} = \hat{I}_{out}\sqrt{\frac{M\left[1 + cos^2(\varphi) + 2cos(\varphi)\right]}{9 \cdot 6\pi}} \quad . \tag{C.19}$$

Note that the in blue highlighted 9 accounts for the current sharing and the result in Eq. (C.19) is the same as using Eq. (C.17). Average and RMS currents for the bi-directional clamping diodes $D_{2,3}$ are equal as for the T-Type structure, i.e.

$$I_{AV,D2,3} = \frac{\hat{I}_{out} M \left[-2sin(\varphi) + (2\varphi - \pi)cos(\varphi) + \frac{4}{M}\right]}{4\pi} \quad , \tag{C.20}$$

and

$$I_{RMS,D2,3} = \hat{I}_{out}\sqrt{\frac{3\pi - 8M + 4Msin^2(\varphi)}{12\pi}} \quad . \tag{C.21}$$

The 1200 V DC bus clamping switches $S_{1,4}$ are derived as in Eq. (C.6), but with only $\frac{2}{3}$ of the load current, such that the average current can be calculated as

$$I_{AV,S1,4} = \frac{2\hat{I}_{out}M\left[sin(\varphi) + (\pi - \varphi)cos(\varphi)\right]}{3 \cdot 4\pi} \quad , \tag{C.22}$$

and the RMS is then

$$I_{RMS,S1,4} = \hat{I}_{out}\sqrt{\frac{4M\left[1 + cos^2(\varphi) + 2cos(\varphi)\right]}{9 \cdot 6\pi}} \quad . \tag{C.23}$$

Lastly, the average and RMS currents through the free-wheeling diodes $D_{1,4}$ are given to be

$$I_{AV,D1,4} = \frac{\hat{I}_{out}M\left[sin(\varphi) - \varphi cos(\varphi)\right]}{4\pi} \quad , \tag{C.24}$$

and

$$I_{RMS,D1,4} = \hat{I}_{out}\sqrt{\frac{M\left[4sin^2(\frac{\varphi}{2}) - sin^2(\varphi)\right]}{6\pi}} \quad . \tag{C.25}$$

Appendix D

Efficiency Investigations of a 3 kW T-Type Inverter for Switching Frequencies up to 100 kHz

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Efficiency Investigations of a 3 kW T-Type Inverter for Switching Frequencies up to 100 kHz

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***Abstract*—This paper deals with a 3 kW multilevel inverter used for PV applications. A comparison has been made based on simulations using IGBTs and SiC MOSFETs to see how much efficiency can be gained when SiC diodes are used. A prototype with the same IGBTs and SiC MOSFETs has been built but using regular soft-recovery Si diodes instead of SiC diodes. Efficiencies and switching transitions for different switching frequencies up to 100 kHz have been measured. Thermal investigations of both IGBTs and SiC MOSFETs have been conducted to analyze the feasibility of increased switching frequencies. When SiC MOSFETs are used in combination with Si diodes, switching frequencies could be doubled achieving the same efficiencies than the IGBT converter.**

Keywords*—*SiC MOSFET, IGBT, multilevel inverter, reverse recovery current

I. Introduction

Photovoltaic (PV) systems have become more and more attractive in recent years. Especially residential PV inverter systems gained much attraction. Due to the low efficiency of the PV panels themselves, much attention must be paid in the design of the PV inverter which leads to a strong demand for low cost and high efficiency power converters. Two-level inverters have the advantage of having a lower cost factor due to the smaller amount of components, being simple in structure and control but suffer from a strong switching frequency and power depending efficiency as well as a relatively large output filter [1]. Multilevel topologies such as the Neutral-Point-Clamped (NPC) inverter have, on the other hand, efficiencies which are less depending on the switching frequency and they give a good compromise between system complexity, cost and efficiency [2]-[3]. Among the three-level inverter topologies, the T-Type inverter (also called Conergy [4] or BSNPC [5]) shows a higher efficiency than the NPC counterpart for low to medium switching frequencies [3]. Furthermore, the efficiency of the T-Type inverter can be improved by using Silicon Carbide (SiC) switching devices in order to reduce switching losses by increased switching transitions and hence increase the overall efficiency. Previous work has shown that SiC switching devices such as normally-on/off SiC JFETs, SiC BJTs and SiC MOSFETs show superior switching performance in various applications over their silicon counterparts, [6]-[7]. An all SiC MOSFET T-Type inverter has been introduced in [8] achieving efficiencies over 98 %. A major aspect when using fast switching SiC devices is to equip the converter with SiC diodes instead of Si diodes in order to keep the switching losses low; otherwise the reverse recovery current caused by a high di/dt will increase the switching losses again and hence dampen the efficiency improvements. The feasibility of using SiC MOSFETs in the T-Type converter is investigated on a practical approach in this paper. Two 3 kW T-Type inverters equipped with 1200 V IGBTs and 1200 V SiC MOSFETs are compared for different power levels and switching frequencies. In Section II the topology including its modulation and current commutation is explained. Simulations of the topology have been carried out in Section III, in which expected efficiencies are obtained and a breakdown loss analysis is conducted. Practical results and efficiency measurements of a 3 kW prototype are introduced in section Section IV. Efficiency investigations for increased switching frequencies are investigated in Section V.

II. The T-Type inverter

The T-Type inverter is a derivation from the NPC inverter. One phase leg comprises of four switching devices and four diodes as shown in Fig. 1. The output voltage of the inverter has three states with reference to the midpoint M, i.e. $+0.5V_{DC}$, 0 and $-0.5V_{DC}$. It is a commonly used topology in three-phase PV inverters in the medium power range and rather low switching frequencies of up to 16 kHz. Switches S_1 and S_3 including their free-wheeling diodes D_3 and D_4 require a breakdown voltage of at least the full DC link voltage V_{DC} whereas switches S_3, S_4 and the diodes D_1 and D_2 require a breakdown voltage of at least half the DC link voltage. In PV inverter systems, the DC link voltage can usually increase up to 1000 V, so S_1, S_2, D_3 and D_4 are 1200 V and S_3, S_4, D_1 and D_2 are 600 V devices to have a margin for overvoltages. A sinusoidal output voltage can be obtained by having switches S_1 and S_2 operated at a chosen switching frequency whereas switches S_3 and S_4 operate at grid frequency as shown in Fig. 1. The T-Type topology benefits from having lower conduction losses than its NPC counterpart because only

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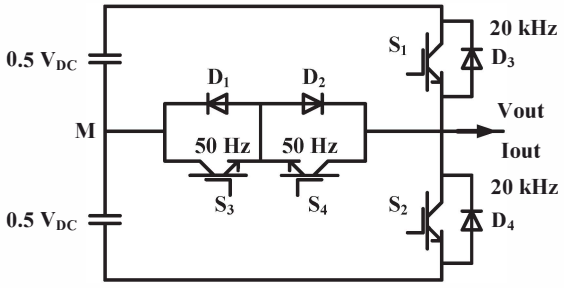
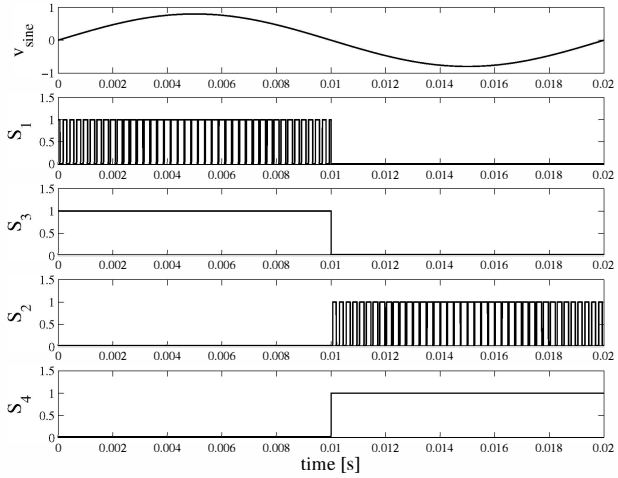


(a) Schematic of a single phase T-Type inverter with midpoint connection



(b) Output voltage creation of the T-Type inverter using sinusoidal PWM

Fig. 1. Schematic of a single phase T-Type inverter and sinusoidal PWM scheme

TABLE I. SPECIFICATIONS

Symbol	Meaning	Value
L	Output filter inductance	3 mH
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, RMS	230 V
P_{out}	Output power	250 W to 3000 W

one switch conducts current at the same time. The current commutations for a resistive load are shown in Fig. 2.

III. SIMULATION RESULTS WITH SIC DIODES

The simulations were done in PLECS and the semiconductor parameters were taken from their datasheets. The specifications for the inverter are shown in Table I. Switches S_1 and S_2 are chosen to be IGBTs due to their higher breakdown capabilities compared to Si MOSFETs. Their SiC counterpart will be a 1200 V SiC MOSFET C2M0080120D from Cree. Switches S_3 and S_4 are chosen to be IGBTs in both configurations due to their low switching frequency requirements. The diodes D_1 and D_2 are SiC diodes to show possible achievable efficiencies when no reverse recovery is taken into account. Table II shows the semiconductors used in the simulations. The Si converter comprises of 1200 V IGBTs and the SiC converter comprises of 1200 V SiC MOSFETs.

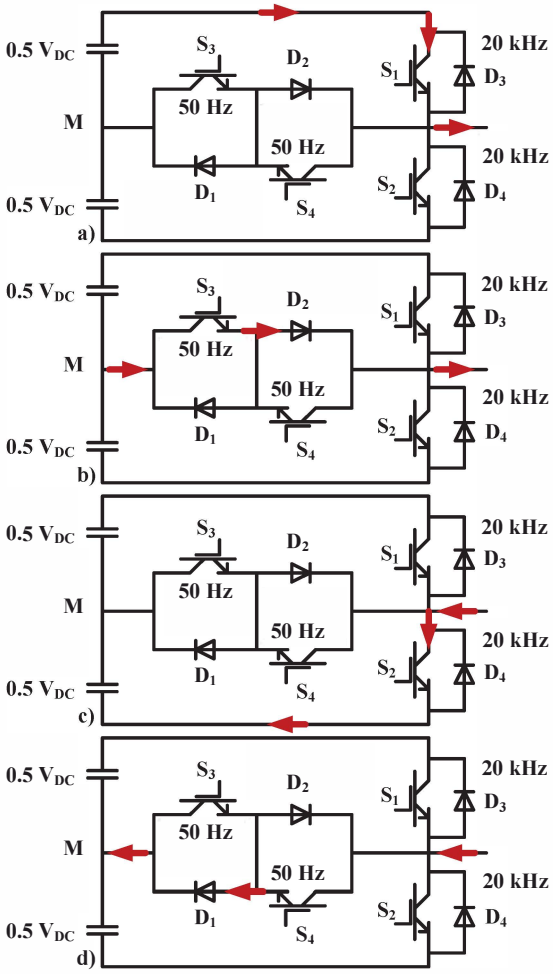
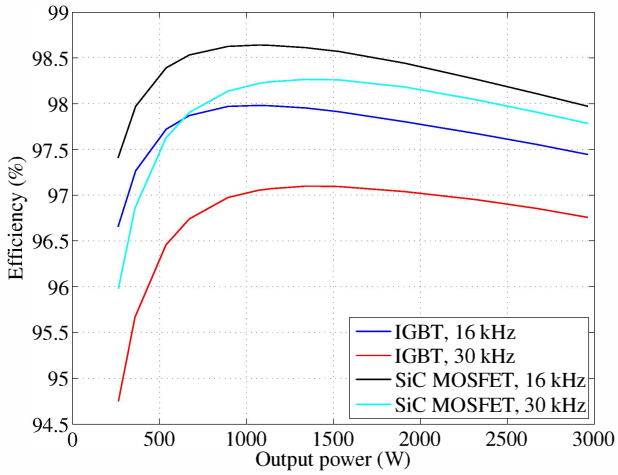


Fig. 2. Current paths in the T-Type inverter. a) Positive output voltage b) Zero output voltage c) Negative output voltage d) Zero output voltage

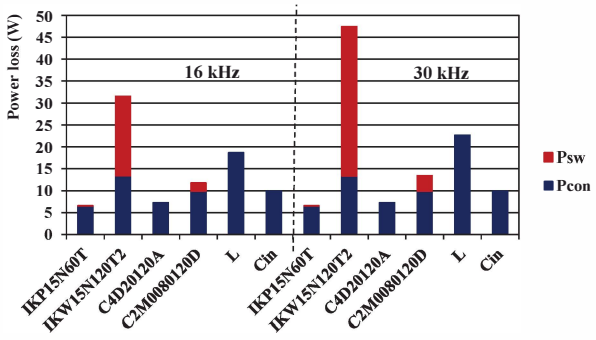
TABLE II. SEMICONDUCTORS

Version	D_1 and D_2	S_1 and S_2	S_3 and S_4
Si Converter	C4D20120A	IKW15N120T2	IKP15N60T
SiC Converter	C4D20120A	C2M0080120D	IKP15N60T

The simulation results of the T-Type inverter for 16 kHz and 30 kHz are shown in Fig. 3. At a switching frequency of 16 kHz, a maximum efficiency of 97.9 % is achieved when IGBTs are used and 98.6 % when SiC MOSFETs are used. A larger efficiency difference between the IGBT version and SiC MOSFET version can be obtained if the switching frequency is increased to 30 kHz. Then a maximum efficiency of 97 % with IGBTs and 98.2 % with SiC MOSFETs are achieved. Although the specifications do not exactly match with [8], the results are close to what has been presented in previous work so that the simulations can be considered a proper representation of what to expect. A breakdown loss analysis has been conducted to show the loss distribution of the converter system. Apart from the semiconductors, losses in the filter inductor as well as the DC link capacitors have been included. The results are shown in Fig. 3. It can be seen that due to the modulation applied, switching losses mainly occur in the 1200 V switches.



(a) Simulation results of T-Type inverter using 1200 V IGBTs with $R_g = 2.2\,\Omega$ and 1200 V SiC MOSFETs with $R_g = 5\,\Omega$



(b) Breakdown analysis of loss distribution in the T-Type inverter at a full power of 3 kW

Fig. 3. Simulation results of T-Type inverter using 1200 V IGBTs and 1200 V SiC MOSFETs

Hence the switching frequency is a limiting factor for the efficiency of the T-Type inverter. However, switching losses can be reduced by using SiC switching devices. The effect of the fast switching capabilities of SiC devices becomes more important when a higher power density is targeted because switching losses in regular IGBTs become dominant degrading overall efficiency. Based on the simulations, switching and conduction losses in the 1200 V IGBT are relatively balanced at a switching frequency of 16 kHz whereas switching losses of the SiC MOSFETs are still smaller than the conduction losses at a switching frequency of 30 kHz. Both the size of the filter inductor and the DC link capacitors were kept constant, though a redesign of these could have reduced losses at increased switching frequencies. However, a main requirement to the simulated efficiencies is that the diodes D_1 and D_2 do not show any reverse recovery current.

IV. Experimental Results

To see how the T-Type inverter performs with IGBTs and SiC MOSFETs, a prototype has been built which is shown in Fig. 4. For both the 1200 V IGBTs and SiC MOSFETs, a TO-247 package was used having the same pinning and hence the same printed circuit board

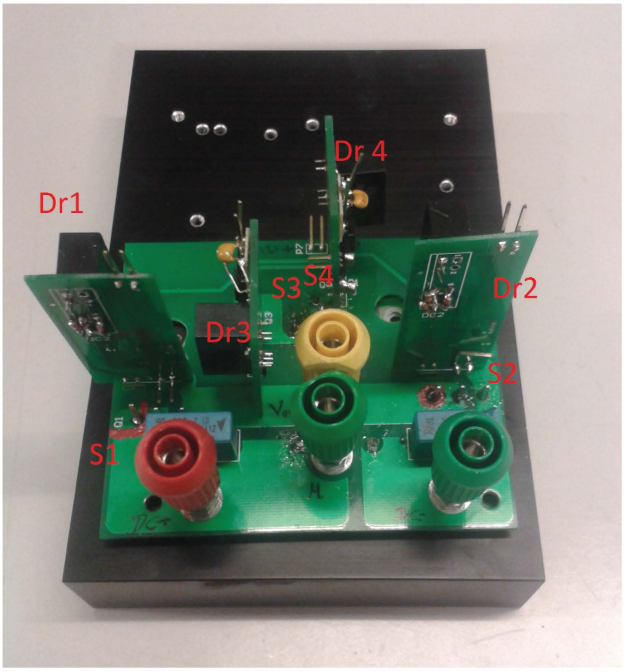


Fig. 4. Prototype of a 3 kW T-Type inverter. The dimensions of the printed circuit board are 8.5 cm by 7 cm

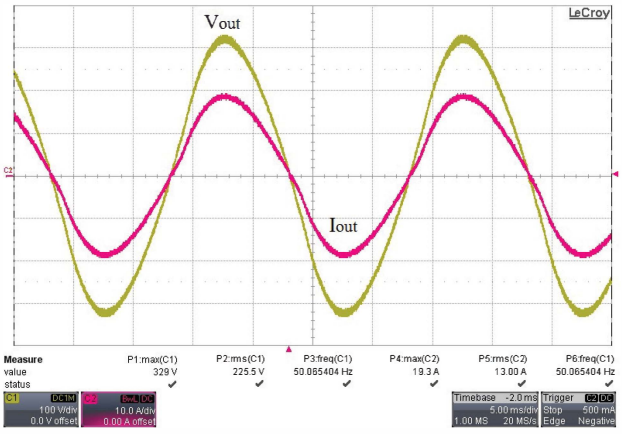


Fig. 5. Filtered output waveforms at an output power of 3 kW and a switching frequency of 16 kHz

(PCB) and layout could be used for a fair comparison. For layout optimization, S_3 and D_1 are packed in one TO-220 package and so are S_4 and D_2. Hence the whole converter could be built with four discrete devices. Only the gate drivers (Dr1 - Dr4) for the IGBTs and SiC MOSFETs were adjusted to stay within their absolute maximum ratings for the Gate-Source voltage. The IGBTs were switched on and off with a Gate-Source voltage of ± 15 V whereas the SiC MOSFETs were switched on with a Gate-Source voltage of 19 V and switched off with a Gate-Source voltage of -5 V. For further comparisons to the simulations, the prototype is equipped with soft-recovery Si diodes instead of SiC diodes. At full power, the filtered output voltage and current are shown in Fig. 5.

A N4L PPA5500 power analyzer was used for efficiency measurements. A first comparison is made with

an IGBT version having a gate resistance of 2.2 Ω and a SiC MOSFET version having a gate resistance of 5 Ω. The results are shown in Fig. 6.

It can be seen in Fig. 6 that the efficiency could be improved when a SiC MOSFET with a gate resistance of 5 Ω is implemented. However, efficiency improvements are larger as the switching frequency is increased. At 16 kHz, a maximum efficiency improvement of 0.3 % is achieved. Increasing switching frequency to 30 kHz leads to a maximum efficiency improvement of 0.8 %. It can furthermore be seen that the SiC MOSFET inverter has similar efficiencies at 30 kHz than the IGBT inverter at 16 kHz. The switching frequency for the SiC converter is therefore increased to 60 kHz and plotted in Fig. 6. It can be seen that the SiC converter at 60 kHz has similar efficiencies than the IGBT converter at 30 kHz which yields to the conclusion that the switching frequency can be doubled when SiC MOSFETs are implemented without degrading the efficiency. The case temperatures of the IGBTs and SiC MOSFETs were measured to get a comparison of the power dissipation in such devices. The operating conditions are at full power, i.e. 3 kW and 20 kHz for the IGBT and 30 kHz for the SiC MOSFET. The case temperatures were measured with an infrared camera and the results are shown in Fig. 7.

It is seen in Fig. 7 that even though the switching frequency is increased, the case temperature for the SiC MOSFET is around 10 °C lower. The thermal resistance of the 1200 V IGBT is given in the datasheet to be 0.63 K/W and the thermal resistance for the SiC MOSFET is given to be 0.60 K/W. Hence the junction temperature of the SiC MOSFET is around 10 °C lower as well. That the case temperature of the 600 V IGBT is higher than the case temperature of the SiC MOSFET can be explained by the fact that a regular TO-220 package for the IGBT was used. In that package, the IGBT comes along with a Si soft recovery free-wheeling diode. These free-wheeling diodes for the two 600 V IGBTs are used to be D_1 and D_2. As a consequence, the TO-220 package withstands the power dissipation for both the

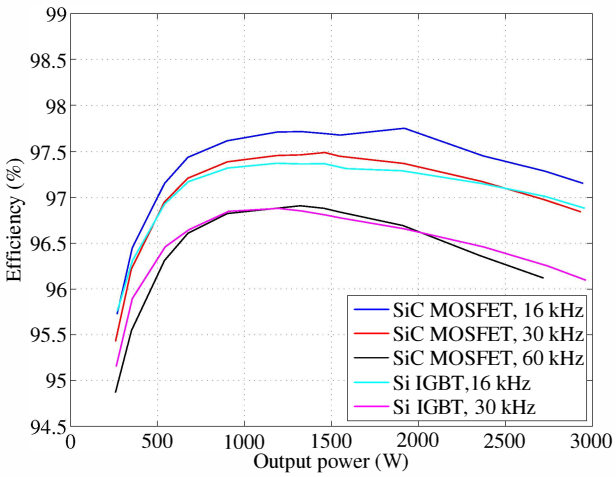
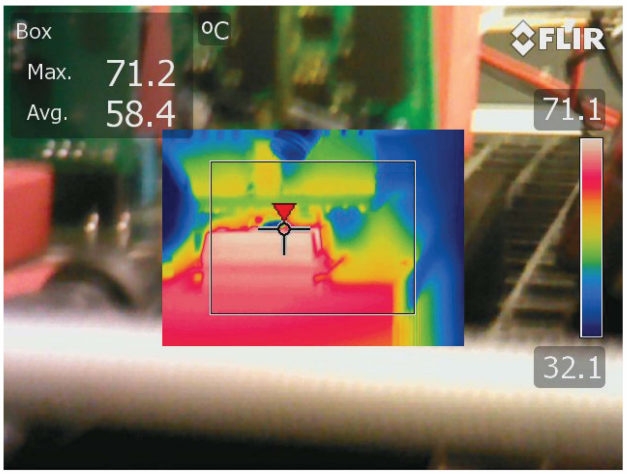
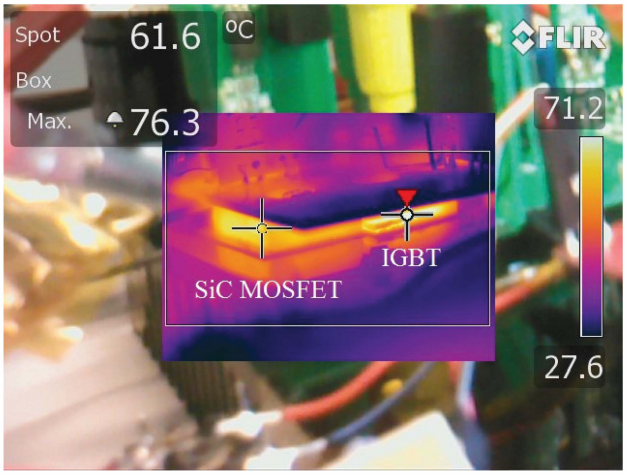


Fig. 6. Measured efficiencies of IGBT and SiC T-Type inverter at different switching frequencies



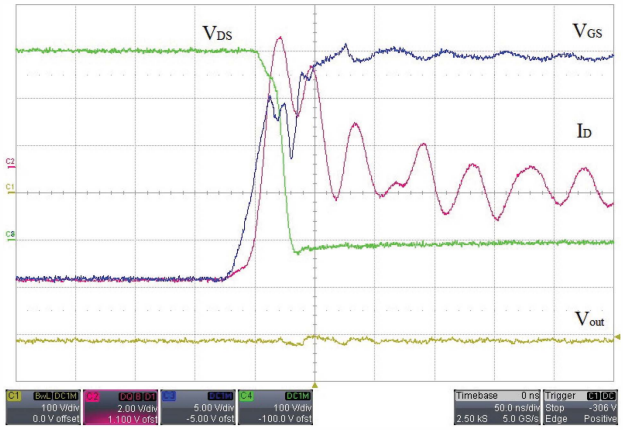
(a) Case temperature of IGBT at 20 kHz and 3 kW



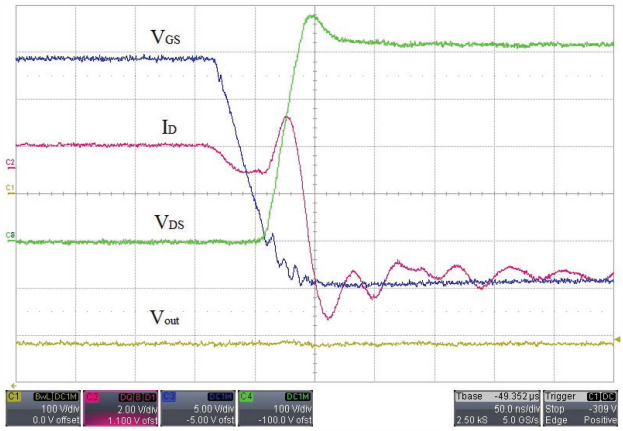
(b) Case temperatures of SiC MOSFET and 600 V IGBT+Diode at 30 kHz and 3 kW

Fig. 7. Temperature measurements of 1200 V switching devices

IGBT and the free-wheeling diode. A switching transition for both turn on and turn off of the SiC MOSFET has been captured. The gate resistance is kept to be 5 Ω, output power is 900 W and switching frequency is 16 kHz. The current was measured with a Rogowski coil having a 20 MHz bandwidth limitation. The Drain-Source voltage was measured with a high voltage probe with a 400 MHz bandwidth limitation and the Gate-Source voltage was measured with a voltage probe having a 500 MHz bandwidth limitation. Furthermore, the time delay of 24 ns of the Rogowski coil was compensated in the measurements and the attenuation for the current measurement was set such that 2 V/div equals to 2 A/div. The transitions are shown in Fig. 8. It can be seen in Fig. 8a that the SiC MOSFET switches 400 V within 30ns resulting in a dv/dt of more than 13 kV/µs. A maximum dv/dt was measured to be 25 kV/µs. The current rises 2 A within 4 ns resulting in a di/dt of 500 A/µs. The peak current is measured to be 10 A. During the turn off transition as shown in Fig. 8b, the maximum dv/dt is measured to be 20 kV/µs. The maximum di/dt is 400 A/µs. For comparison, the IGBT switched 400 V within 120 ns resulting in a dv/dt of 3 kV/µs.



(a) Turn on transition



(b) Turn off transition

Fig. 8. Turn on and turn off transition of SiC MOSFET

V. Efficiency Investigations for Increased Switching Frequencies

It is seen that the efficiencies could be improved when SiC MOSFETs are implemented and the switching frequency could be doubled achieving the same efficiencies when IGBTs are used. It is therefore of interest to furthermore increase the switching frequency and to see how it affects the efficiency. As a last operating point, the switching frequency is increased to 100 kHz. The efficiency curves for the SiC converter at different switching frequencies are shown in Fig. 9.

It can be seen that the overall efficiency dramatically drops as the switching frequency increases up to 100 kHz. Also, the maximum efficiency point is shifted down to a lower power operating point compared to lower switching frequencies. The measurements were limited to a maximum power of 1.6 kW as the case temperature of the TO-220 packages became too high and hence the risk of a thermal damage was increased. However, the case temperature of the SiC MOSFETs were still below 80 °C at an output power of 1.6 kW. So the limiting factor are the 600 V devices in the TO-220 package. A thermal picture of the TO-220 package at an operating point of 60 kHz and 2.7 kW was taken to verify the limiting factor at increased switching frequencies. The result is shown in Fig. 10.

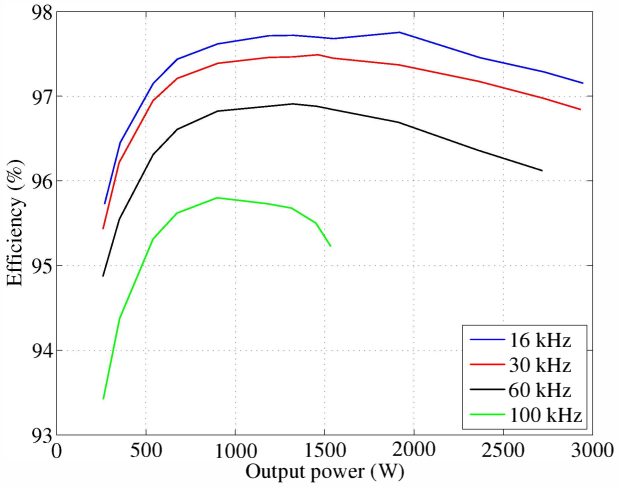


Fig. 9. Measured efficiencies of SiC T-Type inverter for switching frequencies up to 100 kHz

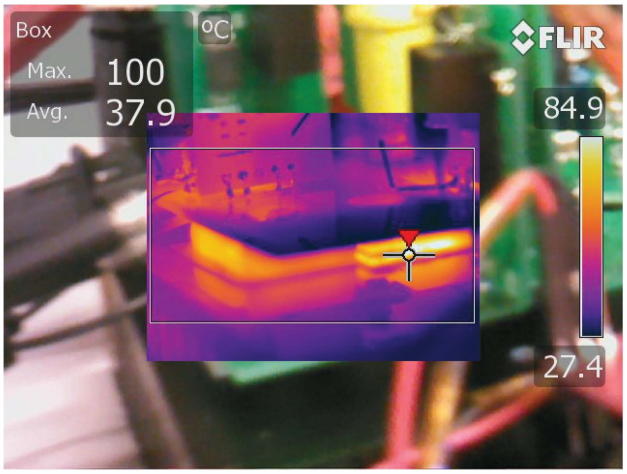


Fig. 10. Case temperature of 600 V devices in the TO-220 package at a switching frequency of 60 kHz and an output power of 2.7 kW

The case temperature of the TO-220 package is measured to be 100 °C and is much higher than the case temperature of the SiC MOSFET, as it can be seen in the scale on the right hand side of Fig. 10.

VI. Conclusions

In this paper the feasibility of SiC switching devices on a 3 kW T-Type inverter topology for PV applications has been investigated. Simulations with regular IGBTs and SiC MOSFETs have been carried out including a breakdown loss analysis to investigate the loss contribution on the overall efficiency. It is shown that efficiency improvements can be achieved when SiC MOSFETs are equipped in combination with SiC diodes. A prototype has been built using the same IGBTs and SiC MOSFETs but regular Si diodes instead of SiC diodes. Efficiency measurements have been done to see how much the reverse recovery current of the Si diodes will affect the overall efficiency. Using Si diodes instead of SiC diodes, efficiency improvements could be achieved but not as much as it could be in the simulations

with SiC diodes. However, switching frequency could be doubled achieving the similar efficiency curves when IGBTs are used. Switching frequencies were increased up to 100 kHz to see how much efficiency drop one might expect. The limiting factor at increased switching frequencies are the 600 V devices in a TO-220 package. Using external SiC diodes in combination with 600 V IGBTs could furthermore improve efficiencies and enable higher switching frequencies.

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Appendix E

Switching Investigations on a SiC MOSFET in a TO-247 Package

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Switching Investigations on a SiC MOSFET in a TO-247 Package

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***Abstract*—This paper deals with the switching behavior of a SiC MOSFET in a TO-247 package. Based on simulations, critical parasitic inductances in the circuit layout are analyzed and their effect on the switching losses highlighted. Especially the common source inductance, a critical parameter in a TO-247 package, has a major influence on the switching energy. Crucial design guidelines for an improved double pulse test circuit are introduced which are used for practical investigations on the switching behavior. Switching energies of a SiC MOSFET in a TO-247 package is measured depending on varying gate resistance and loop inductances. With total switching energy of 340.24 µJ, the SiC MOSFET has more than six times lower switching losses than a regular Si IGBT. Implementing the SiC switches in a 3 kW T-Type inverter topology, efficiency improvements of 0.8 % are achieved and maximum efficiency of 97.7 % is reached.**

***Keywords*—SiC MOSFET, IGBT, multilevel inverter, Switching Energy**

I. Introduction

Silicon Carbide (SiC) devices have become more and more attractive in recent years by introducing SiC diodes which reduce stress on the main switching device due to the absence of reverse recovery current compared to Si diodes. One more way to increase efficiency in power converters is to replace Si switches by SiC switches such as SiC MOSFETs, SiC JFETs or SiC IGBTs. Their faster switching transitions compared to their Si counterparts enable possibilities to operate power converters at a high power density. Previous research has been done to investigate and utilize such devices in power converters in various applications [1]–[5]. Having fast switching transitions, a low parasitic printed circuit board (PCB) becomes more important. The purpose of this paper is to investigate the effect of parasitic elements in the circuit layout. Based on simulations, the influence of the PCB parasitic inductances on the switching energies is pointed out. A commonly used switching cell and PCB layout considerations optimized for fast switching transitions are introduced in order to limit such parasitic elements. Finally, on an optimized double pulse test (DPT) circuit, measurements on a SiC MOSFET in a TO-247 package are conducted in which switching energies are investigated relative to the gate resistance, the common source inductance as well as the junction capacitance of the freewheeling diode. Furthermore, the switching energies are compared to a Si IGBT. In Section II critical parasitic elements in a PCB circuit are investigated followed by a design guideline for PCB layouts with fast switching devices. The gate driver in the experimental setup is introduced in Section III. In Section IV, measurements on Cree's C2M0080120D SiC MOSFET are done showing switching behavior under different scenarios, e.g. varying gate resistance and stray inductance. Efficiency comparison of Si IGBTs and SiC MOSFETs in a 3 kW T-Type inverter are done in Section V. The conclusion is given in Section VI.

II. Double Pulse Tester

As the devices speed increase due to the reduced die parasitic capacitances, the circuit and package parasitic become more crucial in achieving the devices real performance. In this work, a DPT has been used for dynamic characterization. The double pulse tester is basically an inductor with a freewheeling diode that is used to evaluate the device under test (DUT) switching performance under clamped inductive load operation. The schematic of this circuit and the operating principle are shown in Fig. 1. At the instant t_1 the DUT is turned on and the inductor is charged up to the desired current level. At t_2 the DUT is turned off and the inductor current freewheels in the diode. At t_3 the DUT is turned on again and the turn on energy loss is measured by integrating the power in the switching interval. Finally the turn off energy loss is measured at the t_4 instant. The pattern is repeated for different current levels with a very low frequency repetition interval. In this way no self-heating effects are present and the characterization can be performed under controlled junction temperature conditions. The implemented prototype needs to offer flexibility and a modular design is preferred where different gate drive circuits can be tested by using a fast connection. The design is based on the digital signal processor (DSP) evaluation board C2000 Piccolo Launchpad. The implemented prototype is designed to accommodate a TO-247 for the switch and a TO-220 package for the diode. In order to extract the maximum switching performance of the evaluated devices, the DPT PCB design needs to be optimized. A Spice based simulation is used to evaluate the PCB parasitics impact on the device switching performance. The simulation circuit is constructed using a 1200 V, 20 A SiC MOSFET model from Cree Semiconductor *CMF20120* in TO-247 package and a 1200 V, 20 A SiC diode model from Rohm Semiconductor in TO-220 package. The simulation is implemented adding some PCB parasitics on top of the parasitics included in the models. The DPT with the circuit parasitic components is shown in Fig. 2. The simulation conditions are inductor current $I_L = 20\,\text{A}$, supply voltage $V_{DC} = 800\,\text{V}$ and gate drive voltage $V_{drive} = -5\,\text{V}$ to $20\,\text{V}$. Several simulations are performed varying the PCB parasitic

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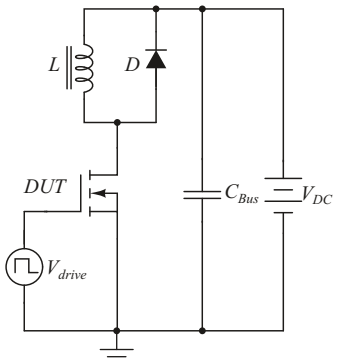
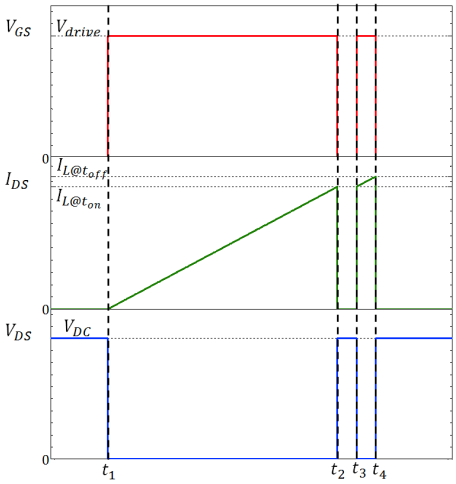


(a) Double pulse tester schematic



(b) Double pulse tester switching pattern

Fig. 1. Double pulse test circuit for evaluating switching performance of semiconductor power switches

inductances from 0 nH to 40 nH. The simulated turn on and turn off energy loss as well as the voltage overshoot at the DUT turn off event versus different parasitic inductances effects are shown in Fig. 3. According to the simulations, the gate drive inductance L_G does not have a remarkable effect on

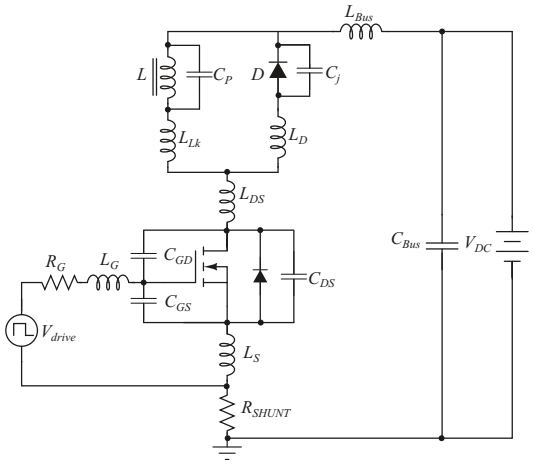
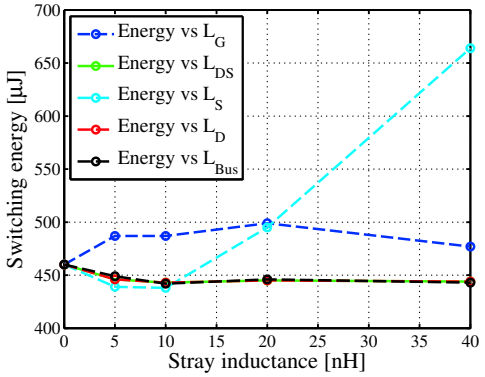
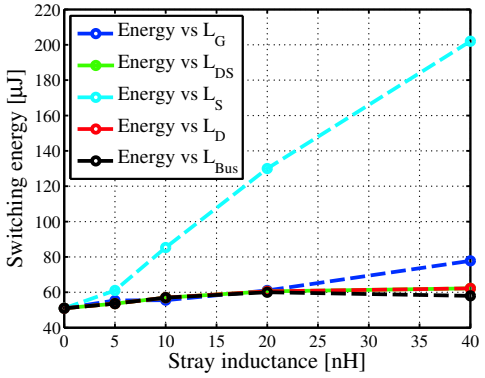


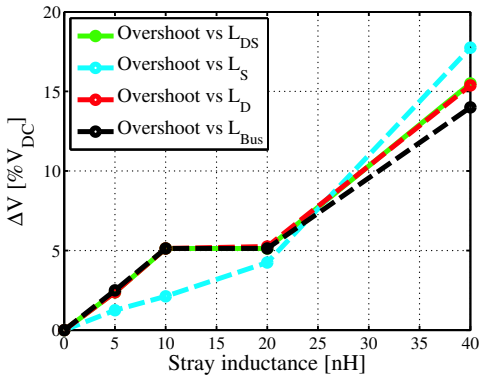
Fig. 2. Double pulse tester with parasitic components



(a) Simulated turn on energy loss vs. parasitic inductance



(b) Simulated turn off energy loss vs. parasitic inductance



(c) Simulated voltage overshoot vs. parasitic inductance

Fig. 3. Simulated switching energies and overshoot voltage on a non-ideal DPT

the device switching losses. During the turn on, the effect of this inductance will depend on the device threshold and the input gate charge. If these parameters are sufficiently large, the current through the driver loop parasitic inductance will build up before reaching the threshold voltage and the effect on the DUT switching energy will be minimal. The drain to source L_{DS} and diode L_D stray inductances do not increase the turn on loss and have a very small effect on the turn off energy loss that corresponds to the amount of stored energy on the stray fields when the DUT voltage reaches the supply voltage V_{DC}. In the same way, the supply loop stray inductance L_{Bus}

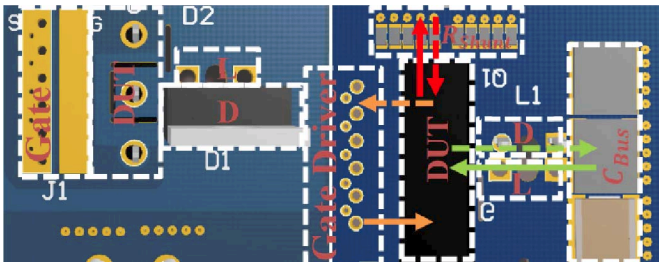


Fig. 4. DPT layout and current paths. Left (top view), right (bottom view)

will slightly reduce the turn on loss because it will create a voltage drop across the DUT, and will increase the turn off energy loss in a similar way to the loop inductances L_{DS} and L_D. However, the common source inductance L_S affects considerably the DUT switching energy both at turn on and at turn off. This parasitic element, shared between the power and driver loops produces a negative feedback Eq. (1) in the gate control signal when a high derivative is present in the current flowing through the switch.

$$V_{GS} = V_{drive} \pm L_S \frac{dI_{DS}}{dt} \tag{1}$$

The double pulse tester needs to be designed trying to minimize all the parasitic inductances, paying special attention to the common source inductance. The gate drive inductance needs to be minimized too because a low impedance gate drive circuit helps reducing parasitc gate activation due to current injection into the gate trough the C_{GD} capacitance at turn off. The implemented prototype uses a four layer PCB to increase the degrees of freedom in the design. The critical loop areas are minimized by implementing the current return paths (the arrows in Fig. 4 indicate the different current loops) in a contiguous layer. Capacitive coupling between drain to gate and gate to source is avoided and the capacitance of the switching node is minimized to avoid increasing the dissipated energy at turn on. Finally, the common source inductance effect due to the PCB is avoided by keeping the power loop current (green and red arrows) orthogonal to the driver loop current (orange arrows). The current measurement method selection is based on a study of state of the art techniques. Recent research work based on characterization of fast switching devices use coaxial current shunts [6]. These devices claim bandwidths up to 2 GHz and are very suitable for this work due to the fact that they only introduce 2 nH in the switching loop. In order to further reduce the inserted stray inductance in the loop, the current measurement proposed in [7] is implemented in this work. This current measurement technique has been previously used for characterizing high switching speed [8] devices and represents a non intrusive and low cost solution. The current measurement bandwidth is increased by decoupling the measurement from the inductive effect of the resistive structure. This is performed by using a pick up wire placed strategically in a low field intensity region. Moreover, the inductance of the structure is further reduced by mounting the resistors upside down in order to place the resistive element closer to the PCB to minimize the area of the current loop. The implemented current shunt structure is shown in Fig. 5.

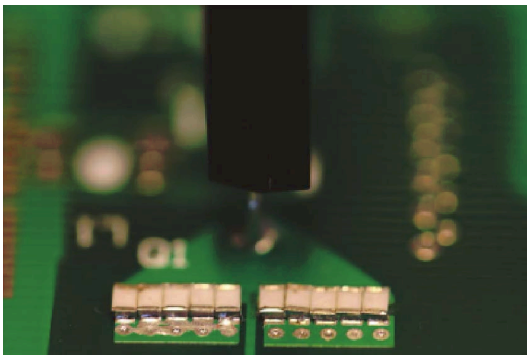


Fig. 5. Integrated flat current shunt

III. The Gate Driver

The gate driver used in this work comprises of a commercially available DC/DC converter, a digital isolator and a gate driver IC with a peak current capability of 9 A. The output of the DC/DC converter supplies ±15 V with a common ground on the secondary side. Two zener diodes are used to create the necessary voltage levels for the digital isolator as well as a reference voltage connected to the source terminal of the SiC MOSFET. An overview of the driver is shown in Fig. 6. With this constellation, the SiC MOSFET can be switched on with a positive voltage of 20.1 V and switched off with a negative voltage of −4.7 V.

IV. Practical Results

A. Low Side Measurements for Different Gate Resistances

Measurements on an optimized low side double pulse test circuit are conducted in order to investigate switching

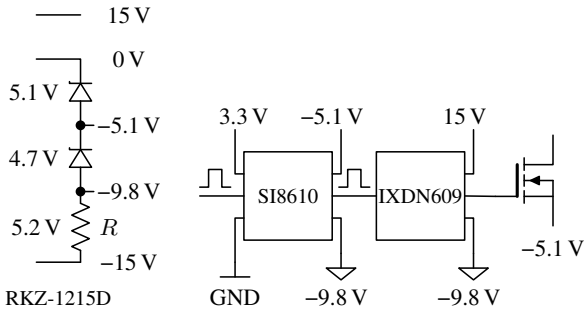


Fig. 6. Gate driver used for SiC MOSFETs

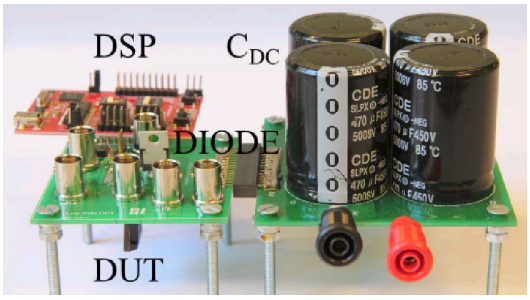
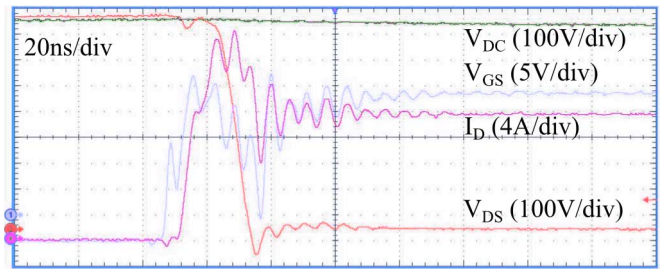
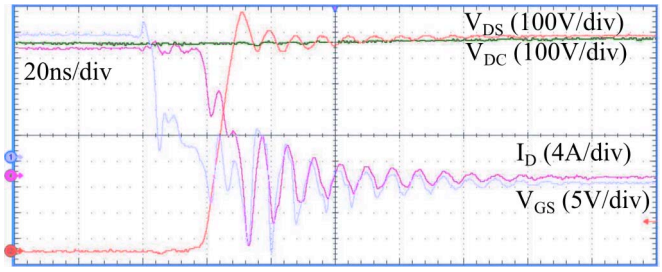


Fig. 7. Lab setup of the low side DPT



(a) Turn on transition



(b) Turn off transition

Fig. 8. Switching transition of a 1200 V SiC MOSFET in a double pulse test circuit. Gate resistance is 6 Ω

performance of SiC MOSFETs compared to varying gate resistors. The voltage probes in this work are Tektronix *P6139* (500 MHz) for the drain current and the gate to source voltage, and a Tektronix *P5100* (250 MHz) for the drain to source voltage. The DC link voltage is 800 V and the measured current range is from 5 A to 30 A. The setup can be seen in Fig. 7 and turn on and turn off transitions for a gate resistance of 6 Ω are shown in Fig. 8. Large oscillations in the gate to source voltage, the drain to source voltage as well as the drain current can be observed mainly due to the common source inductance of the TO-247 package. The resonance frequencies of the oscillations during turn on and turn off with SiC MOSFETs are 166.67 MHz and 125 MHz, respectively. The dv/dt for turn on and turn off are 84.6 V/ns and 85.88 V/ns. The di/dt is 8 A/ns and 1.33 A/ns for turn on and turn off, respectively. A common way to reduce and hence control the switching speeds is to increase the external gate resistance. The downside is an increase in switching energies due to the slower switching transitions. The switching energies for 0 Ω, 6 Ω and 12 Ω are

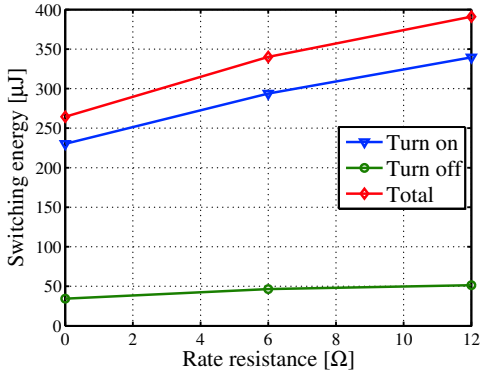
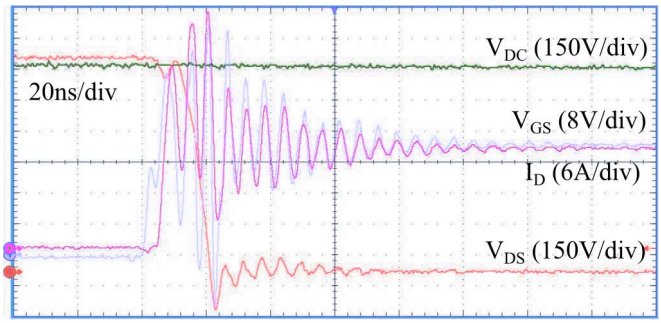
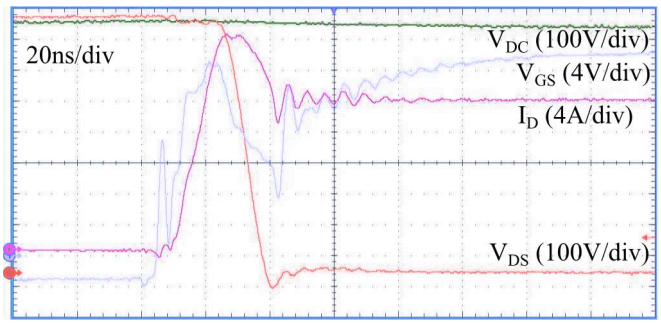


Fig. 9. Switching energies for different gate resistances



(a) Turn on transition for a gate resistance of 0 Ω



(b) Turn on transition for a gate resistance of 12 Ω

Fig. 10. Turn on transitions for different gate resistances

TABLE I. SEMICONDUCTOR COMPARISON

	$I_C/I_D[A]$	$Q_{Gate}[nC]$	$t_r[ns]$	$t_f[ns]$
IKW15N120T2	30	93	30	176
C2M0080120D	31.6	49.2	13.6	18.4

presented in Fig. 9. It can be seen that the turn on losses are mainly affected by an increased gate resistance whereas the turn off losses only slightly increase. A turn on switching comparison with 0 Ω and 12 Ω is shown in Fig. 10. Increasing the gate resistance reduces the peak gate current and hence the gate capacitance is charged slower such that the parasitics in the package as well as in the circuit become less critical. Especially the pointed out common source inductance shown in Eq. (1) has less influence.

B. Comparison to a Si IGBT

Commercially SiC switches come with a minimum breakdown voltage of 1200 V for different current ratings. Hence they are an alternative to replace 1200 V IGBTs in grid-tie applications, e.g. in photovoltaic systems, or motor drives. A comparison to a Si IGBT is conducted in order to see the reduction in switching energies. The chosen Si IGBT is Infineons IKW15N120T2, a second generation IGBT designed for frequency converters and uninterruptable power supplies. The main characteristics based on the semiconductor datasheets are listed in Table I. The same gate driver circuit as in Fig. 6 was used with the same voltage levels for turn on and turn off. Only the gate resistance was changed to 7 Ω in order to maintain the same peak gate current. The results can be seen in Fig. 11. Especially the turn off comparison shows the superior advantages of SiC MOSFETs over Si IGBTs due to the lack of the tail current. A total switching energy reduction of 84.2 % can be achieved at a switching current of 20 A.

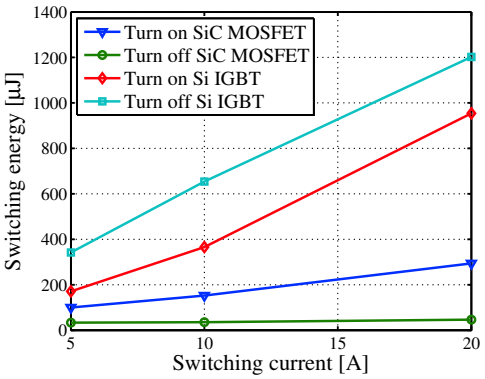
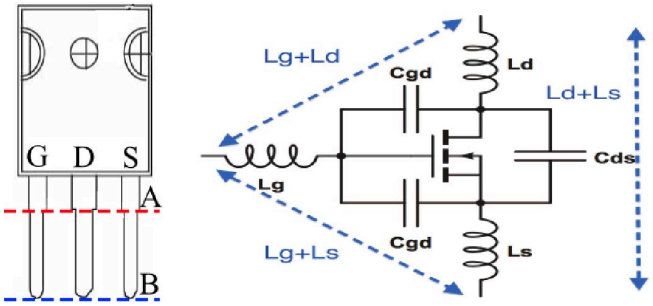


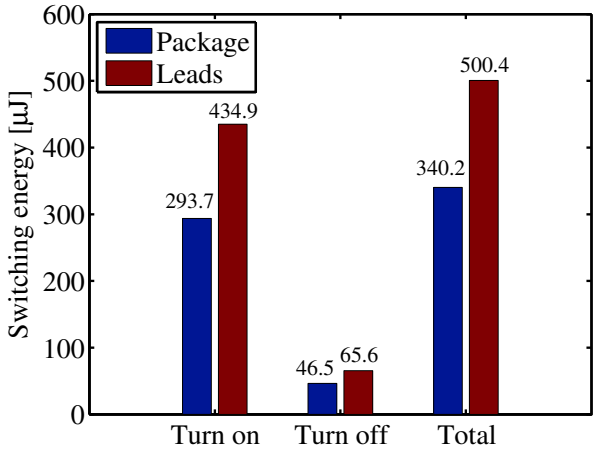
Fig. 11. Switching energy comparison between SiC MOSFET and Si IGBT

C. Effect of the lead inductance of the package

In the simulations, it is found out that the common-source inductance is a crucial aspect when it comes to switching energies. An increased inductance in the source path results in a larger switching energy loss. With an optimized PCB layout, the effect of the inductance of the leads of the TO-247 package is analyzed. A typical 1200 V switch in such package is shown in Fig. 12a and two kind of measurements were done. The first measurement represents the TO-247 SiC device being soldered to the DPT at the end of the leads (Point B, blue dotted line) from now on referred to as lifted leads. In the second measurement, the device is soldered to the DPT at the beginning of the leads (Point A, red dotted line). The comparison of these two scenarios with Cree's C2M0080120D SiC MOSFET is shown in Fig. 12b. It can be seen that having the TO-247 package soldered to the main PCB on Point A reduces the total switching energies by 32 %.



(a) Typical switch in a TO-247 package

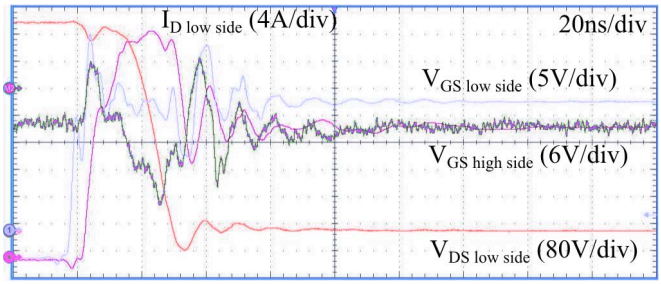


(b) Switching energies for different soldering points of the TO-247 package

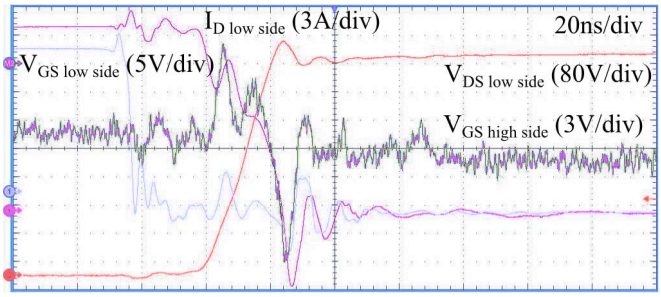
Fig. 12. Effect of the leads in a TO-247 package

D. Comparison of High Side Body Diode and Discrete SiC Diode

Until now, the DPT circuit comprised of a low side switch and a discrete SiC diode for free-wheeling the load current. A commonly encountered circuit configuration in power electronics is a phase leg comprising of a DC link voltage, a low side switch and a high side switch. Unlike Si IGBTs, SiC MOSFETs contain a parasitic body diode which can be used as a freewheeling diode. The effect of such body diode in the high side switch is investigated in this section and compared to a phase leg with an external SiC diode in parallel to the high side switch. Turn on and turn off transitions of the low side MOSFET as well as the gate to source voltage of the high side MOSFET are shown in Fig. 13. It can be seen that the gate to source voltage of the low side MOSFET is not dramatically affected by the switching transition. However, the gate to source voltage of the high side MOSFET is very much affected. By looking at the drain current through the low side MOSFET, it can be seen that no shoot through nor breakdown of the high side gate occurs. Comparing the switching energies of the low side MOSFET with a high side body diode and a discrete SiC diode, it can be seen that main efficiency improvements are achieved during the turn on process. At low current levels, the turn on energies using only the body diode presents the lowest losses because of the reduced parasitic capacitance. When an external SiC diode is used the increased



(a) Turn on transition



(b) Turn off transition

Fig. 13. Switching transition of a phase leg configuration

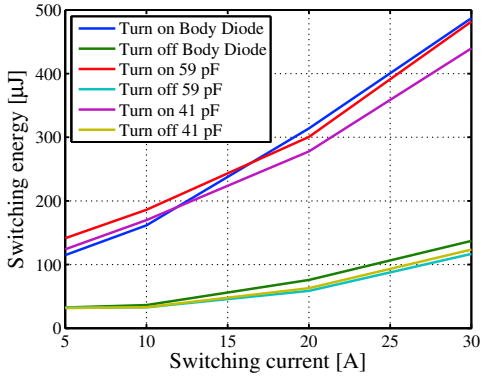


Fig. 14. Switching energies comparison for high side body diode and discrete SiC diodes

junction capacitance increases the losses at low current levels, however reduces the losses at high current levels because of the reduced reverse recovery effect in the body diode of the MOSFET. The turn off energies are less affected by the choice of discrete SiC diode or internal body diode as it can be seen in Fig. 14.

V. Efficiency Improvements Using SiC Switches

The effect of SiC switching devices is demonstrated on a 3 kW T-Type inverter whose schematic is shown in Fig. 15. It is a three level inverter topology that comprises of both 600 V and 1200 V semiconductor devices. More elaborated, switches S_3 and S_4 including their anti parallel diodes are 600 V devices because they have to withstand half the DC link voltage whereas S_1 and S_2 including their freewheeling diodes must be 1200 V devices because they have to block the whole DC link voltage. Furthermore, S_1 and S_2 are modulating the converter output voltage with a chosen switching frequency; typical values for residential photovoltaic applications are up to 20 kHz when Si IGBTs are used. The specifications are shown in Table II. A prototype of the T-Type inverter is designed according to the results and PCB guidelines in Section II in order to minimize the common-source inductance. Also, the switching devices are soldered to the PCB with a

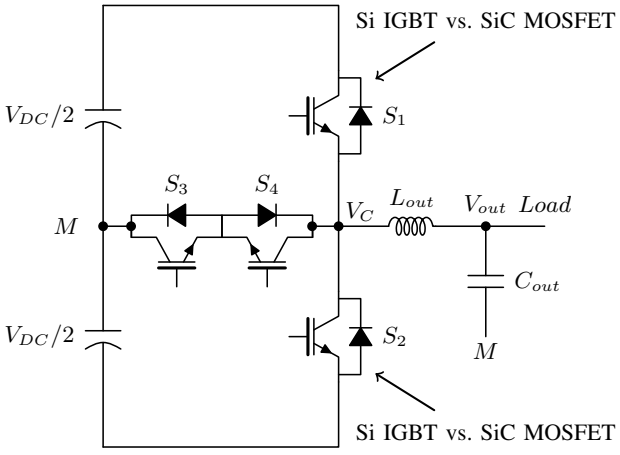
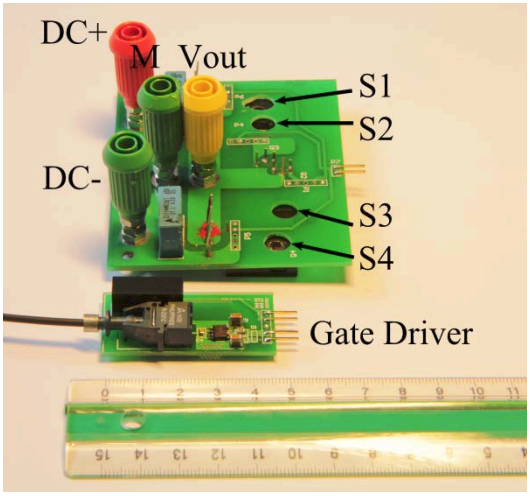


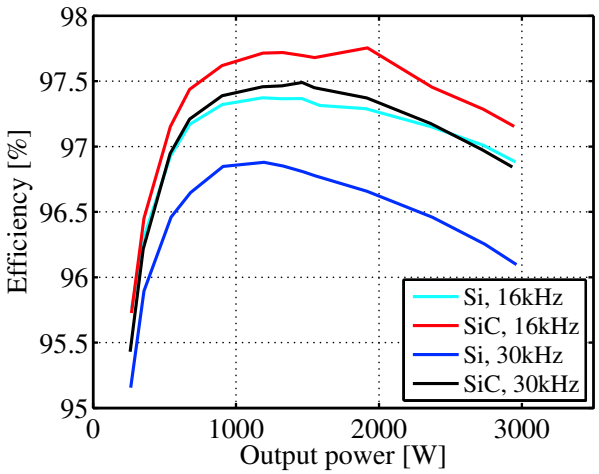
Fig. 15. T-Type inverter topology

TABLE II. Specifications

Symbol	Meaning	Value
L_{out}	Output filter inductance	3 mH
C_{out}	Output filter capacitance	4.4 µF
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, RMS	230 V
P_{out}	Output power	250 W to 3000 W



(a) 3 kW prototype of T-Type inverter



(b) Efficiency improvements with SiC MOSFETs

Fig. 16. Prototype in (a) and measured efficiencies in (b)

minimum lead lengths (Point A in Fig. 12). The prototype as well as the efficiency curves using a N4L PPA5500 power analyzer for both the Si IGBT (IKW15N120T2) and the SiC MOSFET (C2M0080120D) version are shown in Fig. 16. Maximum efficiency improvements of 0.3 % are achieved at a switching frequency of 16 kHz. However, the benefits of the SiC switches become more visible as the switching frequency is increased up to 30 kHz. Maximum efficiency improvements at that switching frequency is then up to 0.8 %. According to the measurement results, the SiC based T-Type inverter at 30 kHz achieves similar efficiencies than the Si IGBT based inverter at 16 kHz.

VI. Conclusion

In this paper, switching performance of a commercially available SiC MOSFET has been investigated on a low parasitic DPT. Simulations have shown that the common source inductance has a significant negative impact on the switching losses. PCB design recommendations have been pointed out how to minimize such parasitic. In an optimized DPT circuit, a SiC MOSFET in a TO-247 package was evaluated based on different gate resistances. Even though the DPT is optimized for a low common source inductance, large oscillations are present due to the package parasitics. With a gate resistance of $6\,\Omega$ and a trade off between switching energy and oscillations, the SiC MOSFET has switching energies of 84.2 % lower than a Si IGBT. It is furthermore pointed out that the reverse recovery effect of the body diode of the high side MOSFET has a strong influence on the switching energies at higher current levels. Furthermore, it is recommended to use an external SiC diode with a low junction capacitance instead of using the body diode of the SiC MOSFET. Having SiC MOSFETs equipped in a 3 kW T-Type inverter, efficiencies could be increased by 0.8 % compared to a Si IGBTs counterpart.

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Appendix F

Comprehensive Loss Evaluation of Neutral-Point-Clamped (NPC) and T-Type Three-Level Inverters based on a Circuit Level Decoupling Modulation

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2014 International Electronics and Application Conference and Exposition (PEAC), Nov 2014, pp. 82-87

Comprehensive Loss Evaluation of Neutral-Point-Clamped (NPC) and T-Type Three-Level Inverters based on a Circuit Level Decoupling Modulation

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Abstract— **In this paper, an efficiency comparison of neutral-point-clamped (NPC) inverters and bipolar switch NPC (T-Type) inverters is studied and the result shows that the T-Type inverter is more efficient at lower switching frequencies. Nevertheless, its efficiency suffers when the switching frequency increases due to high switching loss of the equipped high voltage power switches. In order to reduce switching loss and hereby enhance efficiency, a newly proposed circuit-level decoupling modulation (CLDM) scheme is applied for these two widely used three-phase three-level inverters, as well as their corresponding loss analyses are addressed. The switching loss reduction is evaluated comprehensively under variant modulation indices and load power factors. The analysis results reveal that the CLDM is an alternative discontinuous pulse-width modulation (DPWM) approach for inverters with high switching frequencies in order to achieve superior output voltage quality without lowering efficiency.**

Keywords—Three-level inverter; NPC; T-Type; switching loss; modulation; PWM

I. INTRODUCTION

Three-level inverters can offer several advantages over the more commonly used two-level counterparts; for instance, smaller output voltage steps, and smaller and less costly output filters. Neutral-Point-Clamped (NPC) and T-Type (Conergy or bipolar switch NPC) inverters, nowadays, are the two most widely used three-level inverter topologies in the industrial applications such as AC motor drives, photovoltaic (PV) systems and distributed power generation [1]-[4].

In order to choose the most suitable topology and hereby increase power efficiency, the loss evaluation of NPC and T-Type inverters, and the comparison between these two topologies have been investigated and reported in the literature [5]-[7] throughout the last decade. Since the NPC and T-Type inverters are mostly used for medium or high power applications, the minimization of the switching loss is such a relevant issue. For the purpose of reducing switching losses, the discontinuous pulse-width modulation (DPWM) strategies, including carrier-based and space vector based, were employed for efficiency improvement [8]-[10]. In [3], a DPWM modulation strategy based on circuit-level decoupling principle

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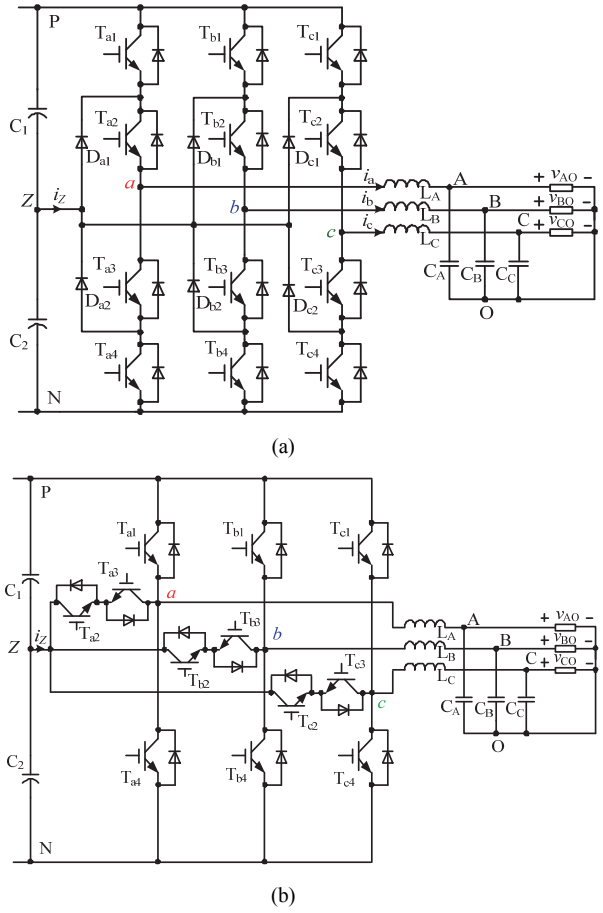

Fig. 1. Topology of three-level inverter. (a) NPC inverter, and (b) T-Type inverter.

was proposed for NPC inverters and later on applied to its four-leg counterparts [11]. By adopting the proposed circuit-level decoupling modulation (CLDM), the modulator and the closed-loop controllers can be simplified. Moreover, voltage balancing between the DC capacitors can be maintained without any additional control effort. Nevertheless, no detailed analysis of conduction and switching losses on semiconductors as well as the loss distribution, under variant load conditions, has been

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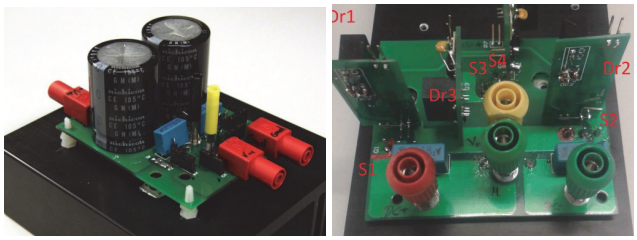

(a) (b)

Fig. 2. Prototype of single phase NPC and T-type inverters. (a) NPC inverter, and (b) T-Type inverter.

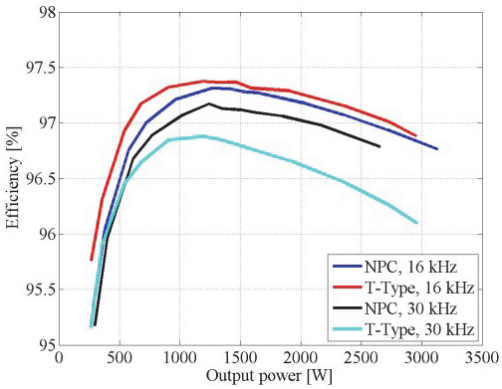

Fig. 3. Efficiency comparsion with different switching frequencies.

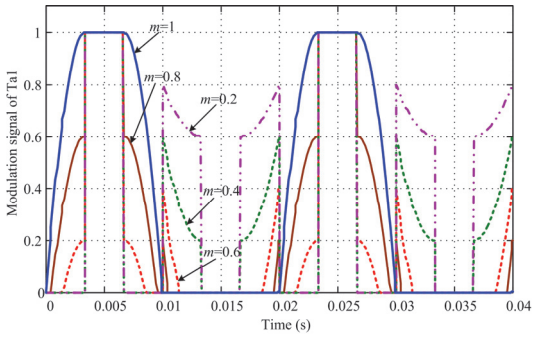

Fig. 4. Modulation reference signal of the switchT_{a1} with modulation indices.

presented. Therefore, this paper will deal with this issue. Furthermore, in this paper, the CLDM method is then employed for the T-Type inverter, thus the loss reduction compared to its NPC counterpart is analyzed in depth.

This paper is organized as: following the introduction, the NPC and T-type inverters are briefly discussed in Section II; circuit-level decoupling scheme and its application on NPC and T-Type inverters are presented in Section III; losses on semiconductors are studied in Section VI and finally a conclusion is given in Section V.

II. NPC AND T-TYPE INVERTERS

A. Topology

The topologies of NPC and T-Type inverters are depicted in Fig. 1. The output voltage of the inverters has three states with the reference to the midpoint Z, i.e. $+0.5V_{DC}$, 0 and $-0.5V_{DC}$. The three-phase NPC needs six diodes and four IGBTs/MOSFETs per phase-leg, and they require a breakdown voltage of the half DC link voltage V_{DC}. For the T-Type, which is a derivation from the NPC, the number of diodes required is only four per phase, and only one switch conducts current in each phase leg at the same time. Therefore, due to low conduction loss, it is more efficient for low switching frequencies; but in the T-Type inverter high voltage switches, i.e. T_{i1} and T_{i4} (i=a, b, c) including their free-wheeling diodes must be equipped in order to block the full DC bus voltage which results in larger switching losses.

B. Efficiency comparison

In order to compare efficiency of these two topologies and verify the aforementioned analysis result, the prototypes of a single-phase NPC and a T-Type inverter with the same specifications (V_{DC}=800 V, and 3 kW/230V/50Hz output) are constructed, as shown in Fig. 2. Thus, these two topologies can be compared in terms of efficiency with variant switching frequencies. A N4L PPA5500 power analyzer was used for the efficiency measurements. From the measured efficiency curves which are presented in Fig.3, it can be seen that the switching frequency strongly affects the efficiency. At the low switching frequency, i.e. 16 kHz, the T-Type inverter is more efficient, but at the high switching frequency, i.e. 30 kHz, due to the high switching loss, the efficiency of the T-Type inverter drops significantly compared to its NPC counterpart.

Based upon the experimental results, it is clear that in order to apply T-Type inverters to the high frequency applications in a more efficient way, reduction of switching loss is a more critical issue. Thus, adopting the CLDM scheme on T-Type inverters is introduced and a comprehensive loss analysis is studied in the ensuing sections.

III. CIRCUIT-LEVEL DECOUPLING MODULATION

The CLDM [3] is based upon the fact that, for a three-phase system, in a fundamental cycle there are six regions in which two phase voltages always have the same signs which are opposite to the third phase voltage. This fact leads to the idea of pulse-width modulating the switches in the phases with the same signs, and on the other hand keeping the switches in the other phase steady for either the entire or partial region. As an example, the modulation reference signal of the switch T_{a1} in the NPC or T-Type inverters in Fig.1 is shown in Fig. 4. It can be seen that (1) there are completely no switching actions in region II and V; (2) the line to line voltage is used as the modulation reference; (3) modulation signals are within the range [0, 1], so all the references can share one common carrier wave; i.e. the phase-shifted carrier is not needed. With this CLDM scheme, the switching losses can be reduced by not switching the phases which have the highest and lowest voltages. Moreover, it can keep the neutral point at half of the DC-bus voltage without any additional feedback or feed-forward regulation. In this paper, this modulation is utilized for NPC and T-Type inverters, respectively; therefore a comprehensive loss analysis and comparison can be carried out for load conditions with variant modulation indices and power factors (PFs).

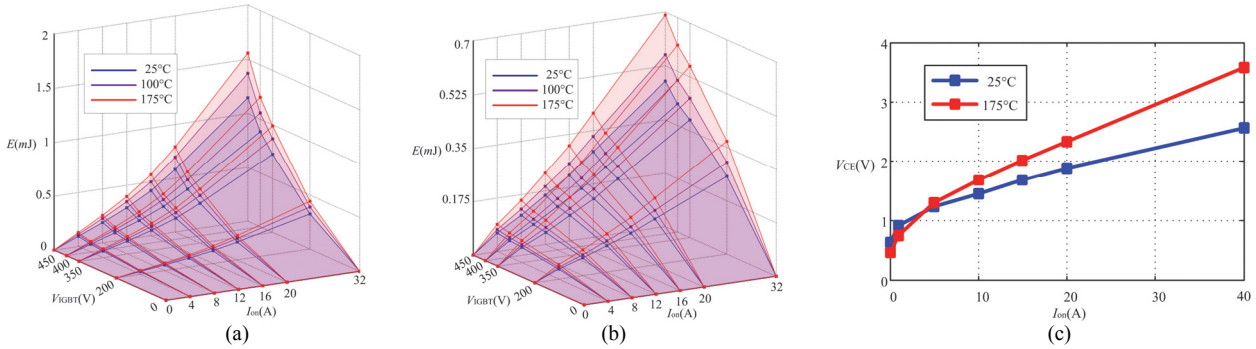

Fig. 5. Loss model of IGBT IGP20N60H3. (a) Turn-on loss, (b) turn-off loss and (c) conduction loss.

IV. Losses Analysis and Evaluation

The NPC and T-Type inverters use 600V 3rd generation Trench IGBTs and 1200V 2nd generation TrenchStop IGBTs from Infineon, respectively. SiC Schottky barrier diodes are anti-parallel to the 600V IGBTs, thus the losses due to reverse recovery are negligible. IGBTs conduction and switching losses are introduced in the model based on the datasheet values [12]. The IGBTs' switching losses are initially extracted from datasheets in which the losses can be scaled for variant temperatures, and switching current and voltage. Therefore, the switching loss can be calculated,

$$P_{sw,IGBT} = E_{on,IGBT}(i_{IGBT,turn-on}, v_{IGBT,turn-on}) \cdot f_{sw} + E_{off,IGBT}(i_{IGBT,turn-off}, v_{IGBT,turn-off}) \cdot f_{sw}. \quad (1)$$

IGBTs conduction losses ($P_{fwd,IGBT}$) are calculated based on the IGBTs forward characteristic; linearized to an on-state zero-current collector-emitter voltage (V_{CE0}) and an on-state resistance ($R_{on,IGBT}$) as expressed in (2).

$$P_{CON,IGBT} = V_{CE0} \cdot I_{avg,IGBT} + R_{on,IGBT} \cdot I^2_{sw,RMS} \quad (2)$$

where $I_{avg,IGBT}$ and $I_{sw,RMS}$ are the mean and RMS value of the conducting current through IGBTs.

The diodes conduction loss due to a threshold voltage (V_{T0}) and a dynamic resistance ($R_{on,D}$) is calculated by (3).

$$P_{fwd,D} = V_{T0} \cdot I_{avg,d} + R_{on,D} \cdot I^2_{D,RMS} \quad (3)$$

The specifications of the investigated NPC and T-Type inverter are given in Table I.

TABLE I. Specifications and Components

DC Link voltage V_{DC}	600 V
Input power P_{in}	15 kW
Rated three-phase output voltage, V_a, V_b and V_c	230 V/50 Hz
Output filters, L and C	1 mH/20 μF
600 V and 1200 V IGBTs	IGP20N60H3, IKW15N120T2
600 V clamping diodes	VS-HFA25TB60

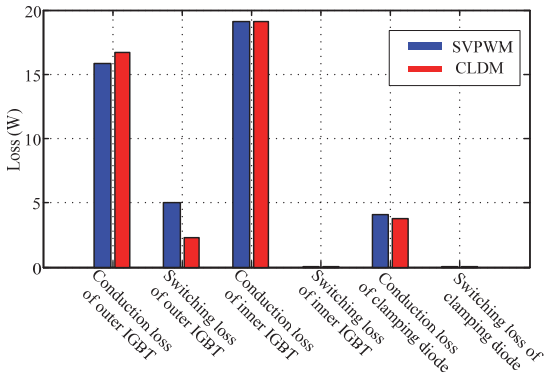

Fig. 6. Loss distribution of NPC with SVPWM and CLDM schemes.

A. Loss analysis of the NPC inverter

The power losses based upon the proposed CLDM and normal space vector pulse-width modulation (SVPWM or SVM) for various values of modulation index and load power factor are evaluated under the assumption of stiff voltage supply with the identical input and output filters, as specified in Table I. Due to symmetry, only the losses from the switches located in phase-leg *a* are analyzed. The reverse recovery effect from the anti-parallel diodes of the IGBTs and the clamping diodes is neglected for simplicity. All the tests were carried out with a switching frequency of 20 kHz and a modulating frequency of 50 Hz.

The loss models of the switching devices, including IGBTs and diodes, are created based on the parameters provided by the manufactures. As an example, the loss model for the 600V IGBT (IGP20N60H3) is illustrated in Fig. 5. With the modulation index of 0.9 and unity load PF, the loss distribution under the CLDM and SVPWM schemes is given in Fig. 6, respectively. It can be seen that the conduction losses of the outer and inner IGBTs (T_{a1} and T_{a2}) and clamping diode (D_1) are almost the same (within the error tolerance 5%); while the switching loss of the outer switch T_{a1} operating with the frequency of 20 kHz is obviously reduced about 50%. The switching loss of T_{a1} and the conduction losses of T_{a1}, T_{a2} and D_1 as a function of the modulation index are presented in Fig. 7, where the dashed lines are employed for depicting the results under SVPWM. Over different modulation indices, and

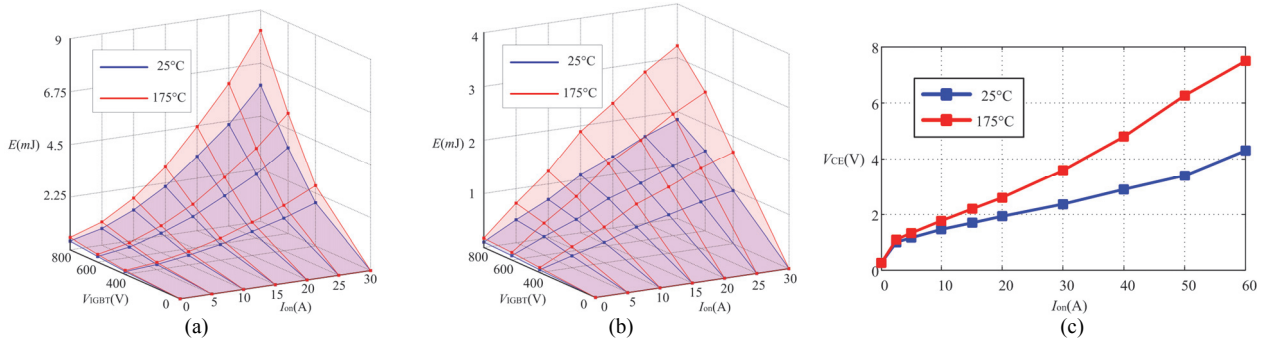

Fig. 9. Loss model of 1200V IGBT. (a) Turn-on loss, (b) turn-off loss and (c) conduction loss.

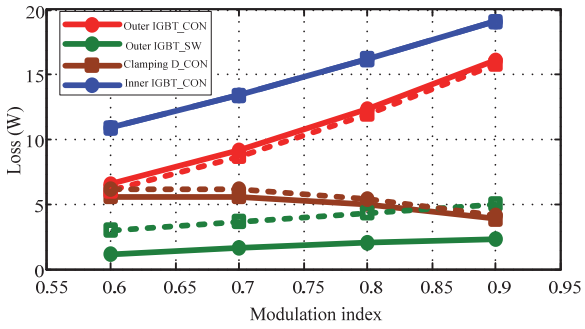

Fig. 7. Loss versus modulation index.

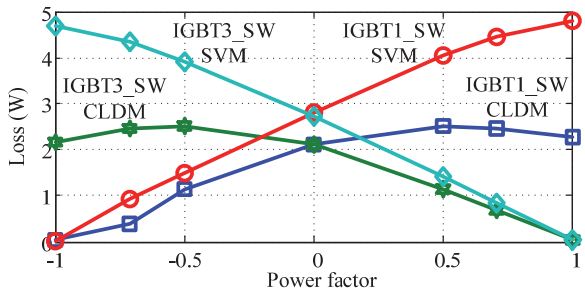

Fig. 8. Loss versus power factor with a modulation index of 0.8.

due to the no-switching branch with the highest or lowest instantaneous voltage value within an electric output angle of π/3, the outer IGBT's switching loss can be reduced when adopting the proposed CLDM scheme. Therefore, higher power efficiency is expected by using CLDM, especially when the switching frequency is increased. The conduction loss of the clamping diode D_1 decreases as the modulation index increases due to shorter conducting time when the modulation index is larger.

With the output of 210VAC/20A, in order to evaluate the switching losses of both the outer and the inner IGBTs versus different load power factors (-1~1), the resulting switching loss curves are depicted in Fig. 8. The power factor (PF) is defined as,

$$PF = \frac{P}{\sqrt{P^2 + Q^2}} \tag{4}$$

where P and Q represent active power and reactive power of the load, respectively.

Compared to the SVM or SVPWM, using the CLDM scheme on the NPC inverter can reduce switching loss of the outer or inter IGBT (IGBT1 or IGBT3) over the entire PF range, especially, when the PF is near to 1 or −1.

B. Loss analysis of the T-Type inverter

The proposed CLDM scheme is also applied to the T-Type inverter, where T_{x1} and T_{x3}, T_{x4} and T_{x2} (x=a, b and c), as shown in Fig. 1(b), have the complementary gate driving signals, respectively. 1200V IGBTs (IKW15N120T2) are employed for the switches, T_{x1} and T_{x4} (x=a, b and c). 600V IGBTs (IGP20N60H3) are used as the switches, T_{x2} and T_{x3} (x=a, b and c) and accordingly 600 V anti-paralleled clamping diodes are connected, in order to build the paths for conducting the currents in both positive and negative directions. Therefore, the loss models of the high voltage IGBT, in which the turn-on energy includes the anti-parallel diode's reverse recovery, are presented in Fig. 9. By comparing Fig. 5 and Fig. 9, the conduction loss of 1200V IGBT is comparable to that of its 600V counterpart, but the switching losses are approx. four times higher than the low voltage one, that leads to lower efficiency at high switching frequencies. This also can match the measured efficiencies shown in Fig. 3 well. Hence, under the same testing conditions listed in Table I, the loss distribution in phase leg a of the T-Type inverter is depicted in Fig. 9. It can be seen that, with the SVPWM scheme, the conduction loss of the outer IGBTs (1200V) is comparable or slightly higher than that of the 600V IGBTs in the NPC inverter. The conduction loss of the inner IGBTs and diodes (600V) is reduced, that is the advantage of T-Type inverters, but the switching loss of the outer IGBTs (1200V) is over twice as much higher than its NPC counterpart as shown in Fig.6. It indicates, on the other hand, that T-Type inverters' efficiency suffers at high switching frequencies.

Adopting the CLDM can keep the low conduction loss, and the switching loss can be reduced by approx. 50% as shown in Fig.10. Moreover, with the modulation index of 0.9, the switching losses of the outer IGBT and inner IGBT as a function of power factor at the diverse switching frequencies are depicted in Fig. 11. It shows that the high voltage switch has more switching loss over the entire power factor range, and that the switching loss distribution varies significantly as the power factor changes, which is relevant to the current conducting paths in the T-Type inverter.

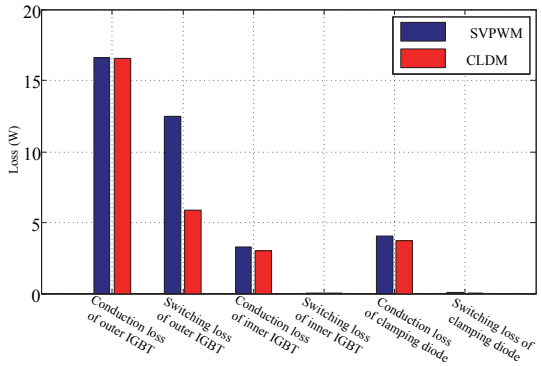

Fig. 10. Loss distribution of T-Type inverter.

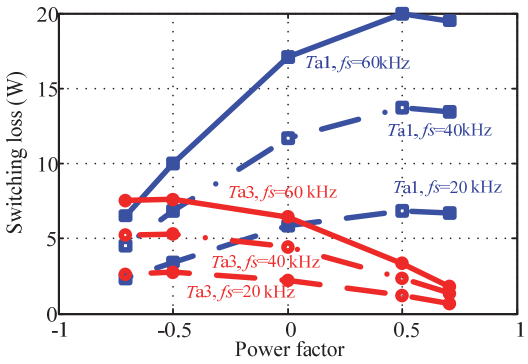

Fig. 11. Switching loss of outer IGBT (T_{a1}) and inner IGBT (T_{a3}) as a function of power factor with the CLDM.

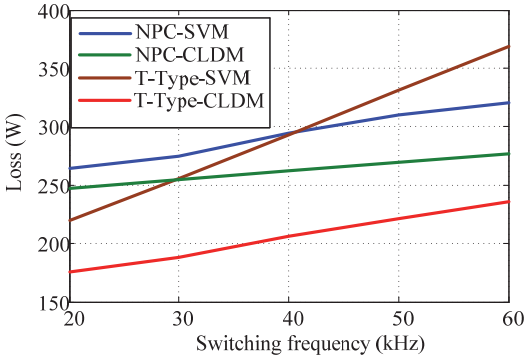

Fig. 12. Comparison of total losses with PF=1.

C. Comparison

The total semiconductor losses of a 15 kW inverter with NPC and T-Type configurations can be summarized in Fig. 12, where load PF=1 and modulation index is 0.9. With the SVM scheme, the T-Type inverter has a lower loss, which means higher efficiency, until the switching frequency up to around 40 kHz. After this frequency, the NPC inverter is more efficient. Using the CLDM scheme can reduce not only the total loss but also the loss growth rate over the entire frequency range. Moreover, with the CLDM, the total losses of the NPC and T-Type are compared comprehensively based on variant power factors and switching frequencies as presented in Fig.13. It shows clearly that the T-Type inverter

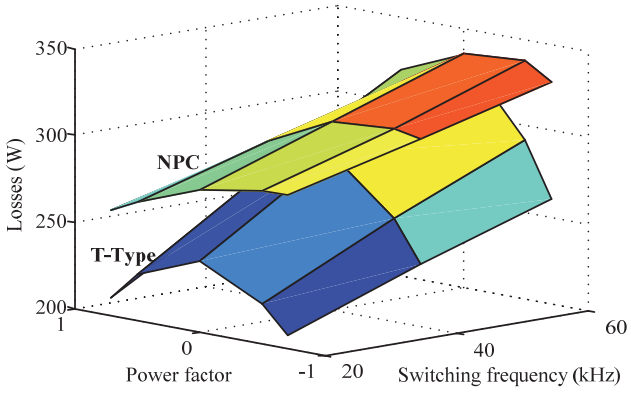

Fig. 12. Comparison of total losses with different set of power factors and switching frequencies.

with the CLDM scheme can achieve higher efficiency over its NPC counterpart in the entire load power factor range.

V. Conclusion

In this paper, a comprehensive analysis of the loss of the NPC and T-Type inverter with CLDM scheme compared to adopting SVPWM is presented. This CLDM approach allows for reducing the converters' switching losses and thus makes the converter suitable for high switching frequency applications. Moreover, this loss reduction can be achieved at different load conditions over the investigated switching frequency range. Finally, the total semiconductor loss of the NPC and T-Type are compared, revealing that the NPC is more suitable for high switching frequency applications, and that the T-Type has higher loss due to adopting 1200V IGBTs, but discontinuous modulation schemes such as CLDM can reduce the switching loss effectively, thus makes the T-Type inverter more efficient over its NPC counterpart even at high switching frequencies. Therefore, T-Type inverters are the more promising topology when the switching loss reduction is realized by adopting advanced modulation strategies or low switching loss semiconductors such as SiC or GaN devices.

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Appendix G

Efficiency Evaluation on a CoolMos Switching and IGBT Conducting Multilevel Inverter

Applied Power Electronics Conference and Exposition (APEC), March 2015, pp. 2251-2255

Efficiency Evaluation on a CoolMos Switching and IGBT Conducting Multilevel Inverter

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***Abstract*—This paper deals with a three-level inverter topology in the 3 kW range as an alternative to commonly used three-level topologies. The topology is attractive for having low switching losses due to the utilization of CoolMos switching devices while keeping conduction losses low due to the utilization of IGBTs. A proper time delay between the CoolMos and IGBT devices increases the efficiency by 0.2 %. Maximum efficiencies of 97.7 % are achieved and less than 0.2 % efficiency degradation is possible with doubled switching frequency. The case temperatures of the switching devices are below 60 °C at full power.**

***Index Terms*—CoolMOS, IGBT, multilevel inverter, NPC, T-Type**

I. Introduction

Power electronic converters are important in any electrical power conversion process and high efficiencies are a crucial aspect in the design procedure. In the low voltage applications such as residential grid-tie inverters and frequency converters for drives, a dc-ac inverter is necessary to obtain an ac power that complies with the load specifications. Several topologies are suitable for that and comparisons have shown that three-level inverters show lower total losses compared to their two-level counterparts especially at increased switching frequencies [1], [2]. Among the three-level topologies, the Neutral-Point-Clamped (NPC) and the T-Type (Conergy [3], BSNPC [4]) inverter are commonly used with their own advantages and disadvantages. The NPC can be equipped with semiconductor devices having breakdown voltages of half the DC link voltage only. Therefore switching losses are less affected by the switching frequency. However, an uneven thermal stress occurs among the devices [5], [6]. Due to its low conduction losses, the T-Type inverter shows higher efficiencies at low switching frequencies due to its rather acceptable switching losses. The strong switching frequency dependence, however, is a major drawback of the T-Type inverter due to the implementation of 1200 V Si IGBT switching devices as they have to withstand the whole DC link voltage. One way to reduce the switching losses is to implement next generation's fast switching devices such as Silicon Carbide (SiC) MOSFETs [7], [8] which have superior switching characteristics compared to their Silicon counterparts [9]. Another way towards increasing efficiencies is to combine the NPC and T-Type inverters. Adding two additional CoolMos switches in the T-Type inverter will be used to take over the switching transitions and the conventional 1200 V IGBTs are used afterwards to take over the conduction losses. The topology is referred to as the Hybrid-NPC converter [10], [11] and it is a recently introduced topology without a detailed analysis under which conditions one can benefit from it. The motivation for this work is therefore to investigate such topology in detail and to evaluate its performance in terms of efficiency with respect to chosen switching times between the CoolMos and the IGBT. The paper starts with a description of the inverter topology in Section II including its modulation and the necessary time delay considerations. After that, a loss breakdown analysis is introduced in Section III evaluating performance of the 600 V and 1200 V devices for various switching frequencies. In Section IV, a 3 kW prototype is shown and efficiency curves recorded. Possible efficiency improvements are also shown depending on the chosen time delay. A conclusion is given in Section V.

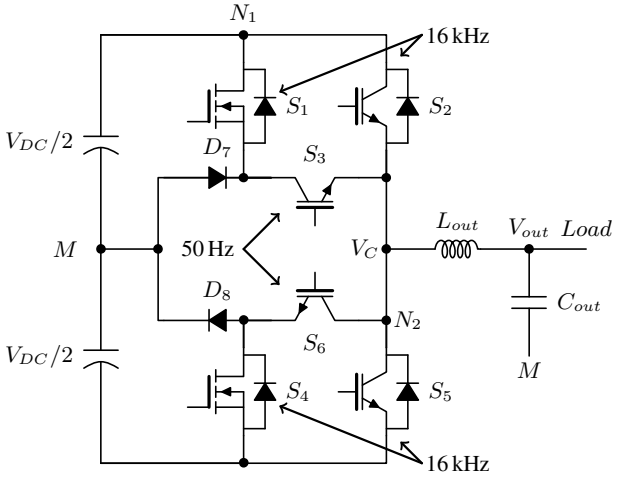


Fig. 1: Single phase schematic of the Hybrid-NPC topology

II. The hybrid-NPC topology

The Hybrid-NPC topology is a three-level inverter and comprises of six switching devices and two clamping diodes as shown in Fig. 1. The converter output voltage V_C can be

TABLE I: Semiconductors used

Semiconductors	Device	Voltage in [V]	Current at 25 °C in [A]
D_8 and D_7	C3D10060A	600 V	29.5 A
S_1 and S_4	SPP20N60S5	600 V	20 A
S_2 and S_5	IKW15N120T2	1200 V	30 A
S_3 and S_6	IKP15N60T	600 V	30 A

either $+V_{DC}/2$, 0 or $-V_{DC}/2$ with M as the reference point. The modulation of this topology is taken from [7] which is the same as for the NPC or T-Type. Only difference is that a necessary time delay t_d between switches S_1 and S_2 as well as S_4 and S_5 are added. The idea behind this topology is that switches S_1 and S_4 are chosen to be 600 V CoolMos devices in order to reduce switching losses. Once the switching transition is over, the voltage across S_2 and S_5 is reduced to the sum of the voltage drops of S_1 and S_3 as well as S_4 and S_6 as shown in (1) and (2).

$$V_{S_2} = V_{S_1} + V_{S_3} \tag{1}$$

$$V_{S_5} = V_{S_6} + V_{S_4} \tag{2}$$

Switches S_2 and S_5 then turn on with a very small voltage drop resulting in low switching losses. In that way, the large conduction losses of the 600 V CoolMos devices can be reduced by a current divider in the two nodes N_1 and N_2. The turn on principle for S_1 and S_2 is shown in Fig. 2. The turn on and turn off logics for S_1, S_2, S_4 and S_5 using sine pulse width modulation (SPWM) are shown in Fig. 3.

III. Simulation Results

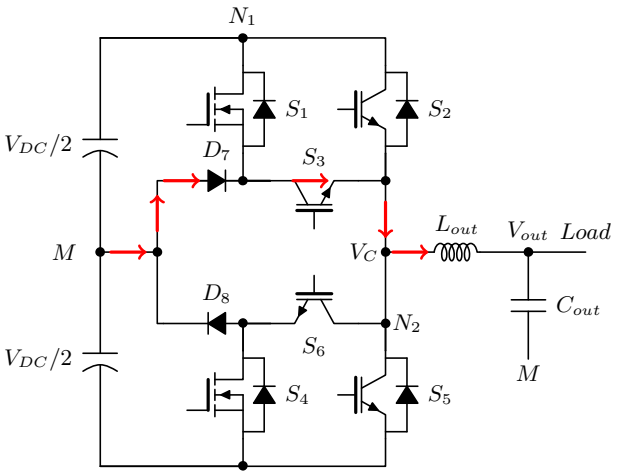
PLECS simulations are conducted in order to evaluate the inverter's efficiency based on the above considerations. A loss breakdown analysis is performed considering the semiconductors used in Table I and the specifications listed in Table II. The results are shown in Fig. 4. It can be seen in Fig. 4b that the switching losses in the converter are mainly occurring in the CoolMos devices because S_2 and S_5 have a very low voltage during the switching transition and S_3 and S_6 are operating at grid frequency; i.e. 50 Hz. Hence, the loss increase at increased switching frequencies depends on the switching losses in the CoolMos devices as well as the core and copper losses in the output filter inductor, though the latter is not part of this work since the focus is given to the topology itself.

IV. Experimental Results

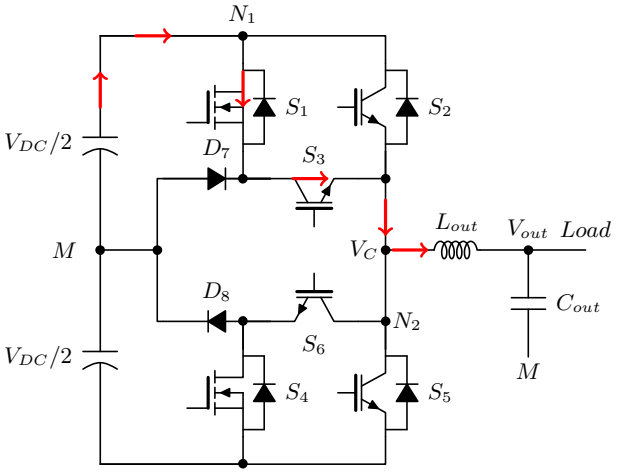
A 3 kW prototype has been built as shown in Fig. 5a. For the sake of simplicity, the gate drivers have been built

TABLE II: Specifications

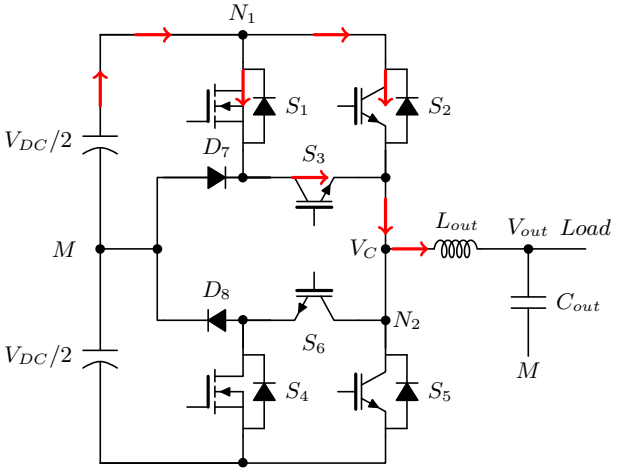
Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
P_{out}	Output power	250 W to 3000 W
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 µF



(a) Zero output voltage. S_1 turned off, S_2 turned off



(b) Positive output voltage. S_1 turned on, S_2 turned off



(c) Positive output voltage. S_1 turned on, S_2 turned on

Fig. 2: Converter output voltage change from 0 to $+V_{DC}/2$

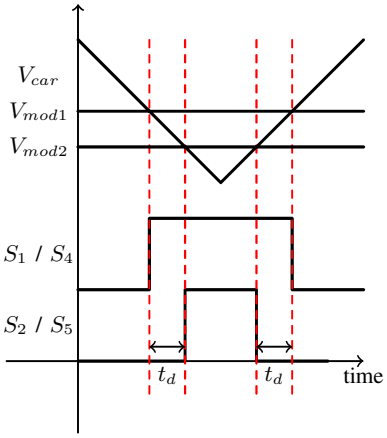
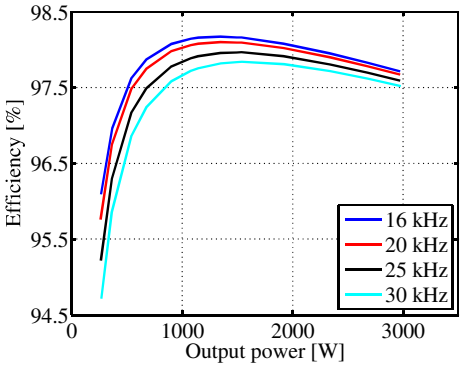
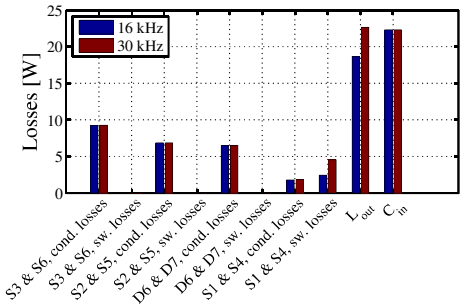


Fig. 3: SPWM implementation with necessary time delays t_d



(a) Simulated efficiencies



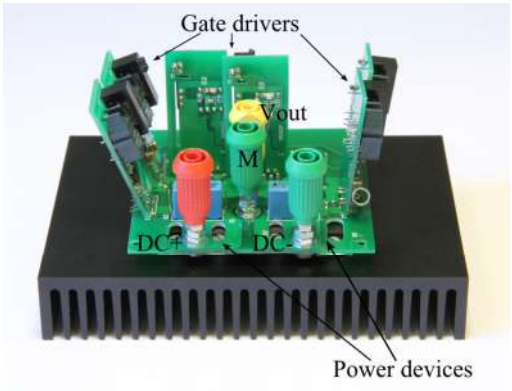
(b) Loss breakdown analysis

Fig. 4: Simulation results of hybrid inverter

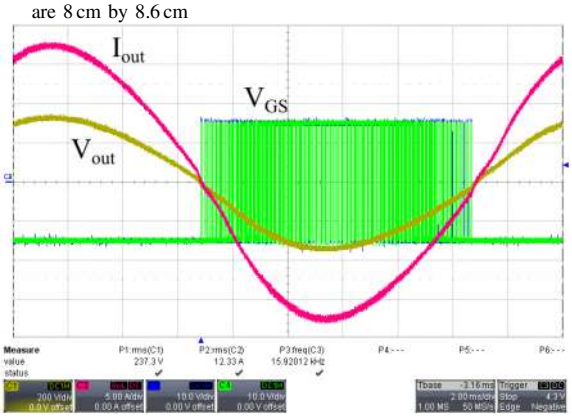
on a separate printed circuit board (PCB) and are mounted vertically to be easily interchangeable. All devices are discrete components, either TO-220 for the 600 V or TO-247 for the 1200 V devices. The filtered output current and voltage as well as the gate signals for S_4 and S_5 are shown in Fig. 5b.

A. *Importance of the chosen time delays*

Turn on and turn off switching transitions are captured to see the current commutation between the CoolMos and the



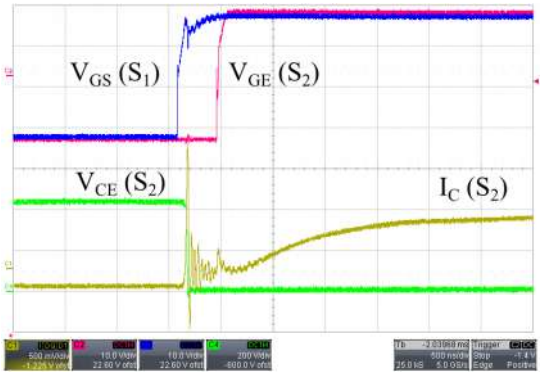
(a) Prototype of the Hybrid-NPC inverter. PCB measurements are 8 cm by 8.6 cm



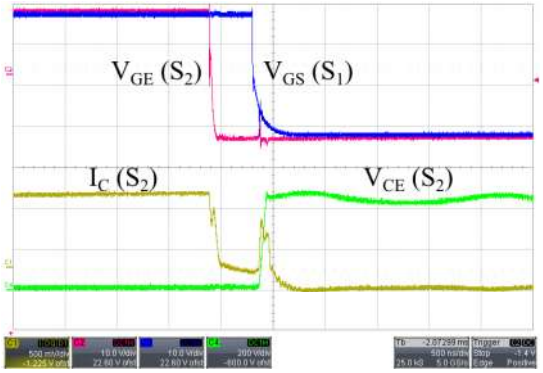
(b) Filtered output waveforms and gate signals at 3 kW and $f_{sw} = 16$ kHz

Fig. 5: Prototype of Hybrid-NPC inverter in (a) and measured output waveforms and gate signals in (b)

IGBT switching devices. The measurements were started with a time delay of 420 ns and are shown in Fig. 6. The collector current is measured with a Rogowski coil having a bandwidth of 20 MHz and a gain of 100 mV/A. The collector-emitter voltage is measured with a 400 MHz voltage probe and the gate voltages are measured with 500 MHz voltage probes. Figure 6a shows that the voltage across the 1200 V IGBT drops down to a minimum as soon as the CoolMos device is turned on. 420 ns later, the gate command of the IGBT gets high such that the current starts rising. However, it can be seen that the current rise time is rather slow which means that conduction losses still occur in the CoolMos device. By looking at Fig. 6b, it can be seen that the current commutation from the IGBT to the CoolMos device is rather slow, too. However, as soon as the CoolMos device switches, the current commutation progresses much quicker. The reason for that can be explained as follows. When the CoolMos device turns on, the current commutation occurs at a high voltage (in this prototype, the CoolMos device switches the current with 400 V). The voltage drops down to a minimum according to Eq. (2). When the IGBT turns on, the current commutates with a low voltage of a few volts only. Since the IGBT is a bipolar device with a

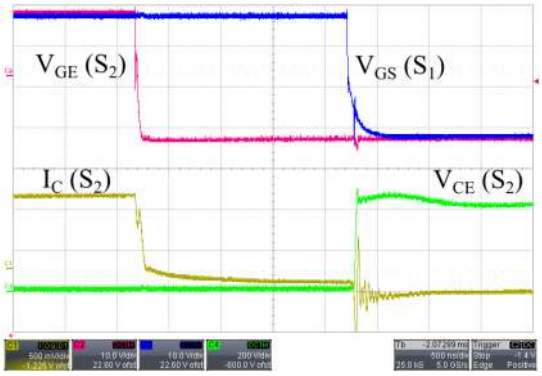


(a) Turn on switching transition

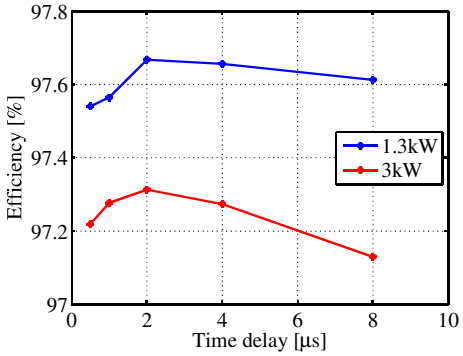


(b) Turn off switching transition

Fig. 6: Turn on and turn off switching transitions with a time delay of 420 ns



(a) Turn off switching transition for a time delay of 2 µs



(b) Efficiencies for different time delays

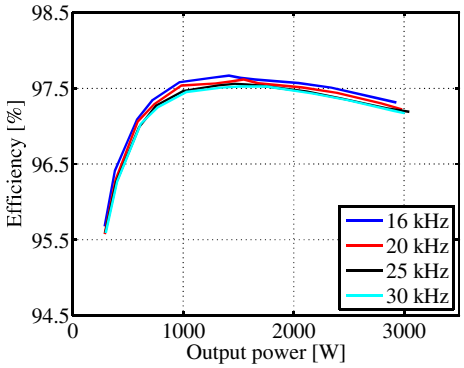
Fig. 7: Turn off switching transition for a larger time delay in (a) and efficiencies for different time delays in (b).

collector current that among others depends on the forward voltage drop of the IGBT (bipolar output characteristic), a rather high dynamic on-resistance might exist. Furthermore, the IGBT is a slower switching device compared to unipolar switches like MOSFETs. Another thing that contributes to the rather slow switching transition of the IGBT are parasitic inductances in the switching loop, both the inductances from the TO-220 and TO-247 packages as well as the inductances due to the PCB layout. In the turn off transition, The IGBT first turns off and the current commutates from the IGBT to the CoolMos device. In addition to the same arguments as before, the tail current contributes to a slow turn off transition. After the specified time delay, the CoolMos device also turns off before the IGBT has fully commutated the current. The consequence is that switching losses also occur in the 1200 V IGBT device. For comparison, the time delay is increased to 2 µs and the turn off transition is repeated, shown in Fig. 7a. Also, efficiencies are measured for different time delays using a N4L PPA5500 power analyzer with a basic accuracy of 0.01 %. For an output power of 1.3 kW and 3 kW and time delays $t_d = 0.42\,\mu s$ to 8 µs, the results are shown in Fig. 7b. It can be concluded that the efficiency clearly depends on the time delay for different output power levels. Choosing the time delay too small, large switching losses will occur in the 1200 V IGBT device. If the time delay is too large, increased conduction losses will occur in the CoolMos device. Highest efficiencies are achieved with a time delay of 2 µs.

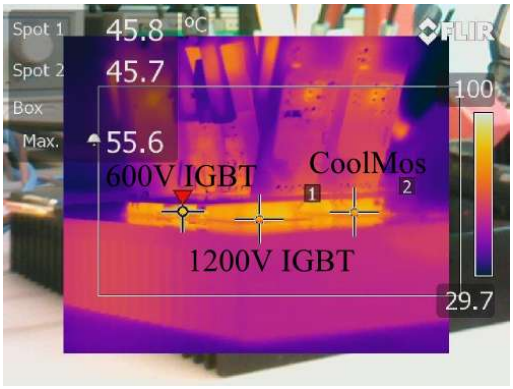
B. *Efficiency measurements*

Based on the previous analysis, the time delay is set to 2 µs and the efficiency curves for the whole power range and different switching frequencies are shown in Fig. 8a. Maximum efficiency is 97.7 % at 16 kHz and an efficiency degradation of 0.2 % occurs when the switching frequency is increased to 30 kHz. The measured results deviate from the simulated ones. The reason is that the simulations were done under ideal circumstances, i.e. all switches are switching instantly, parasitic inductances in the PCB are neglected. In order to evaluate the stresses on the semiconductor devices, case temperatures of S_1, S_2 and S_3 are measured using an infrared camera. For a switching frequency of 16 kHz, the results can be found in Fig. 8b. The CoolMos and 1200 V IGBT remain relatively cool with a temperature of 45.7 °C and 45.8 °C, respectively. The 600 V IGBT has the highest temperature with 55.6 °C. Increasing the switching frequency up to 30 kHz leads to only a small increase in the case temperatures of the devices as shown in Fig. 8c. Operating at 3 kW and 30 kHz, maximum case temperature is increased up to 58.3 °C. One can conclude that the Hybrid-NPC topology offers an even temperature distribution between the

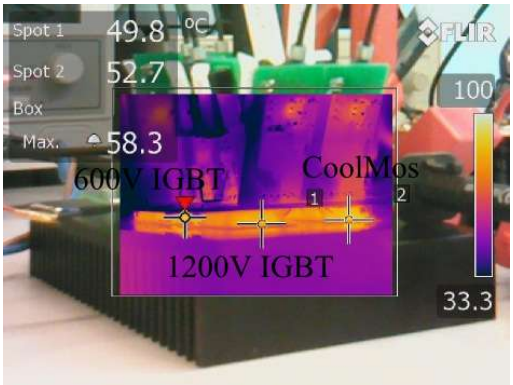
semiconductor devices which is one of the drawbacks of the standard NPC topology. Also, the efficiency is less affected by the switching frequency. Thus, the main drawback of the regular T-Type inverter topology is overcome. However, one must keep in mind that the hybrid mode is only valid for duty cycles greater than the total time delay per switching period.



(a) Measured efficicieny curves for switching frequencies up to 30 kHz and a time delay of 2 µs



(b) Measured temperatures of S_1, S_2 and S_3 at 3 kW and 16 kHz



(c) Measured temperatures of S_1, S_2 and S_3 at 3 kW and 30 kHz

Fig. 8: Measurements of efficiencies in (a) and temperatures for 16 kHz in (b) and temperatures for 30 kHz in (c)

In cases of duty cycles smaller than the specified time delay, the Hybrid-NPC inverter will operate in pure NPC mode, i.e. S_2 and S_5 will never be turned on.

V. Conclusion

In this paper, a hybrid topology is investigated to be an alternative for commonly used three-level inverters. The advantage of such topology is to keep the switching losses in the 600 V CoolMos devices while limiting the conduction losses mostly to the 1200 V IGBT devices. An even loss distribution between the semiconductors is therefore possible. However, the drawback of the topology is to be more complex as two more switching devices are needed and critical time delays between the CoolMos and IGBT devices are necessary in order to fully benefit from the complexity. Choosing too small time delays will result in additional switching losses also in the IGBTs; choosing the time delay too large, conduction losses in the CoolMos devices will increase and hence overall efficiency will be decreased again. With a time delay of 2 µs, maximum efficiencies of 97.7 % can be achieved in a 3 kW prototype. Maximum case temperature is 55.6 °C on the 600 V IGBT at 16 kHz and 58.3 °C at 30 kHz.

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Appendix H

Comparison of a State of the Art Si IGBT and Next Generation Fast Switching Devices in a 4 kW Boost Converter

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Comparison of a State of the Art Si IGBT and Next Generation Fast Switching Devices in a 4 kW Boost Converter

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***Abstract*—This paper gives a comprehensive comparison of two promising silicon carbide (SiC) switching devices, i.e. normally-off SiC MOSFET and a normally-on SiC JFET, as alternatives to a conventional state of the art Si IGBT. The comparison uses datasheet information to determine conduction losses, switching transition measurements for switching loss calculations and electrical power measurements in a boost converter. Using SiC switching devices, switching energies can be reduced by almost 70 % and the forward voltages of such devices are much lower compared to the IGBT which then reduce the conduction losses. This reduction in semiconductor losses can increase overall converter efficiencies up to 0.4 % at 20 kHz or enable high frequency operation up to 100 kHz which then reduces the size and weight of the inductor by more than 75 % while still achieving efficiencies over 98.3 %.**

***Index Terms*—Si IGBT, SiC MOSFET, SiC JFET, Efficiency, Boost converter**

I. Introduction

In residential photovoltaic (PV) systems, transformer-less topologies are favored due to the smaller size, weight, lower cost and higher efficiencies compared to their transformer-based alternatives [1]. However, a boost converter as a preregulator is then necessary in order to ensure a DC link voltage large enough to obtain the desired grid voltage. For three-phase PV systems, the DC link voltage is typically in the range of 700 V and can reach up to 1000 V. Thus, the semiconductor devices are typically chosen to have a breakdown voltage of 1200 V, which limits the choice mainly to Si IGBTs.

For power converters equipped with such semiconductor devices, however, the switching frequency usually becomes the limiting factor when it comes to high efficiency power conversion. Where a simple boost converter generally requires only one diode, one switching element and one inductor, the latter in this configuration usually becomes bulky, heavy and expensive due to the low switching frequency operation of the Si IGBT in order to maintain a reasonable small input current ripple. Interleaved boost converter (IBC) topologies can therefore be an attractive alternative due to the reduced input current ripple [2] which consequently improves the power quality and power-point tracking (MPPT) performance [3] with the trade-offs against other criteria such as additional components, increased complexity or unequal load sharing [4]. To furthermore improve the performance of the preregulator stage of the PV system, previous work has investigated the use of new semiconductor devices made of silicon carbide (SiC) material. With the commercialization of SiC diodes in 2001 [5], which have the particular benefit of having zero reverse recovery current, the positive impact of the new kind of semiconductor devices on switching loss reduction and reduced electromagnetic interference (EMI) has been reported for instance in [6], [7] and efficiency improvements of up to 0.8 % in a boost converter with SiC diodes were achieved in [3].

After the successful commercialization of SiC diodes, research interest has moved towards the utilization of SiC semiconductor switching devices in power converters as direct replacements for Si IGBTs and Si MOSFETs. Due to the higher electric field breakdown strength of SiC material, not only the on-resistance can be reduced compared to a Si MOSFET of an equivalent rating [8], but also the switching energies (in particular compared to IGBTs [9]). The benefits of SiC switching devices compared to Si based alternatives for various applications have been reported in previous work [10]–[15].

Among the various SiC switching alternatives to date, two main candidates can be pointed out and are hence intensively tested in this work: The normally-off SiC MOSFET and the normally-on SiC JFET. Although previous work clearly highlights the potentials of these two SiC switching devices, neither of them have fully become the new standard component in commercial products. Apart from the small availability through distribution channels, main issues are related to the (long-term) reliability, which is still ongoing research work [16]–[18].

The SiC MOSFET is claimed to have long-term reliability issues due to its thin oxide layer [19], [20], which is a major reason for not utilizing it in commercial products. In contrast, the depletion mode JFET does not have the reliability issue like the SiC MOSFET and shows a superior short circuit behavior [21], however its normally-on behavior is the main argument

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TABLE I
SEMICONDUCTORS USED

Device	I_C or I_D at 25 °C [A]	V_{GE} or V_{GS} [V]	C_{oss} [pF]
Si IGBT	30	± 20	75
SiC MOSFET	36	$-10/+25$	80
SiC JFET	35	$-19.5/+2$	102

for not using it as a direct replacement for Si devices. the normally-on characteristic is a crucial aspect when it comes to voltage source inverters (VSI) comprising of large DC link capacitors and additional protection may then be necessary [22]. Although the normally-on characteristic can be overcome with an in series placed low voltage Si MOSFET in cascode configuration (either conventional cascode [23] or direct driven cascode [24], [25]), this solution also adds complexity to the system. In a current source converter like the boost converter, however, the normally-on characteristic of the JFET is not a major drawback and a pure normally-on SiC could be an option in such application.

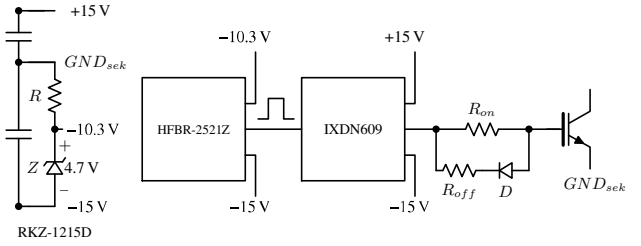
Although switching and conduction performance of these two SiC switching devices can be found in previous work, a direct performance comparison other than simple double pulse test measurements [26] is not known to the authors. This paper therefore gives a comprehensive comparison between these two promising SiC switching device technologies compared to a conventional Si IGBT of an equivalent rating. The comparison uses semiconductor loss models derived from datasheet parameters (conduction losses), measured switching transitions (switching losses) and efficiency measurements on a 4 kW boost converter under exactly the same operating conditions. Compared to a Si IGBT based converter as a reference, this work provides design guidelines when adopting the new kind of switching devices.

II. COMPARISON OF SI AND SIC SWITCHES

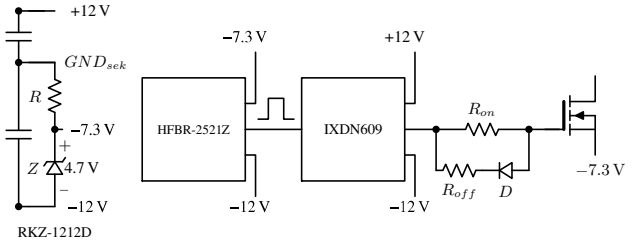
The devices used in this comparison are Infineon's third generation Si IGBT IKW15N120H3, Cree's SiC MOSFET C2M0080120D and Infineon's normally-on SiC JFET IJW120R070T1 with their main characteristics given in Table I. Since SiC switching devices are claimed to replace Si IGBTs in the future, their gate driver circuits are discussed in order to point out the differences and similarities because each switching device needs a specific gate driver circuit as different voltage levels on the gate are required.

A. Si IGBT gate driver

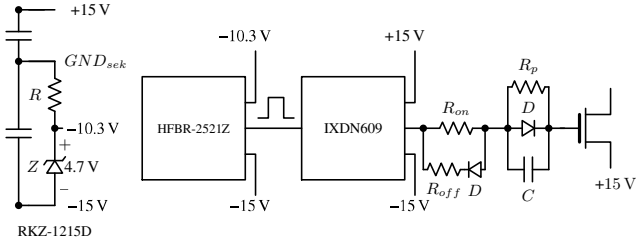
The gate driver circuit for the Si IGBT is used as a reference for comparison of the SiC MOSFET and SiC JFET; all gate driver constellations are shown in Fig. 1. Based on Table I, the IGBT can be switched on and off with $\pm 20\,\mathrm{V}$ as an absolute maximum rating. It is recommended in high speed high power applications to use negative voltages for turning off the IGBTs in order to increase the gap between the gate driver voltage and the threshold voltage of the semiconductor device. Else the risk for unwanted turn on may be increased either due



(a) Si IGBT



(b) SiC MOSFET



(c) SiC JFET

Fig. 1. Schematic of the gate driver circuits

to parasitic inductances in the switching loop or due to the effect of the Miller capacitance. For this reference design, only commercially available components are chosen to ease any reproduction. A 2 W DC/DC converter *RKZ-1215D* is used to provide galvanic isolation with $\pm 15\,\mathrm{V}$ output voltages which are used to turn the IGBT on and off, respectively. The signal transmission from the control board to the power stage is done with optic fiber, whose receiver *HFBR-2521Z* is driven with $4.7\,\mathrm{V}$ obtained by a simple zener diode. The PWM signal is amplified by the gate driver IC *IXDN609* supplied with $\pm 15\,\mathrm{V}$ yielding in a total voltage of 30 V. The collector of the IGBT is referenced to GND_{sek} which has been properly decoupled by two capacitors which are supposed to be placed as close as possible to the switching device in order to minimize any stray inductance in the gate driver loop.

B. SiC MOSFET gate driver

The absolut maximum ratings for the gate-source voltage of the SiC MOSFET are $-10\,\mathrm{V}$ for turn off and $+25\,\mathrm{V}$ for turn on. Hence the Si IGBT gate driver needs to be modified in order to fulfill these requirements. Taking into account some margin to stay safely within the absolute maximum ratings, the SiC MOSFET can be driven with approx. $-5\,\mathrm{V}$ and $+20\,\mathrm{V}$. Hence two things need to be modified:

1) Replace the DC/DC converter with the *RKZ-1212D* which provides galvanic isolation and two output voltages $\pm 12\,\mathrm{V}$
2) Reference the source of the SiC MOSFET to the voltage of the zener diode, i.e. $-7.3\,\mathrm{V}$

The driving voltage for turn on is then according to Kirchoff's voltage law (KVL)

$$V_{GSon} = +12\,\mathrm{V} - (-7.3\,\mathrm{V}) = 19.3\,\mathrm{V} \tag{1}$$

and the turn off voltage, respectively

$$V_{GSoff} = -12\,\mathrm{V} - (-7.3\,\mathrm{V}) = -4.7\,\mathrm{V} \tag{2}$$

Hence the SiC MOSFET can easily be adapted into a Si IGBT based converter with only minor modifications. Basically, only a change in the DC/DC converter and the reference voltage are necessary.

C. SiC JFET gate driver

The gate driver circuit for the SiC JFET requires more attention since the device differs internally from IGBTs or MOSFETs [27]. Since the JFET is a depletion mode device, it is turned on with a control voltage of $0\,\mathrm{V}$ and a negative voltage must be applied to turn the device off. The datasheet states this pinch-off voltage of the JFET to be around $-16\,\mathrm{V}$ which may vary from one device to another. Furthermore, at around $-23\,\mathrm{V}$, the gate-source junction enters reverse breakdown and hence a gate-source voltage of $-20\,\mathrm{V}$ is usually recommended in order to fully turn the device off. In [27], a driver circuit for a normally-on JFET is proposed to overcome this particular issue with the reverse breakdown, and it is therefore used in this work. Where the detailed explanation of the gate driver can be found in [27], it is only mentioned here that three additional electronic components are needed and the reference voltage, once again, must be shifted. The two modifications for the SiC JFET gate driver are therefore:

1) Place a RCD network between the gate resistance and the gate of the JFET
2) Reference the source of the JFET to the positive supply voltage of the DC/DC converter output, i.e. $+15\,\mathrm{V}$

D. Static characteristics

One of the properties of SiC based switching devices is to reduce the conduction losses. The voltage drop of a semiconductor device directly relates to the conduction losses which represent a significant contribution to the overall converter losses. The specific forward voltages for the devices used in this work are taken from datasheet information and are presented in Fig. 2. Once can see that over the whole current range of interest, the Si IGBT has the largest forward voltages. The reason for that is that the IGBT is a bipolar switching device which can be modeled as a series connection of a voltage source representing the zero on-state voltage V_0 and a dynamic resistance r_{on}. For a unipolar device such as the SiC MOSFET and the SiC JFET, there is no zero on-state voltage and only the channel resistance R_{on} is given. Hence, conduction losses of both SiC switching devices will be smaller at any given operating point in this work.

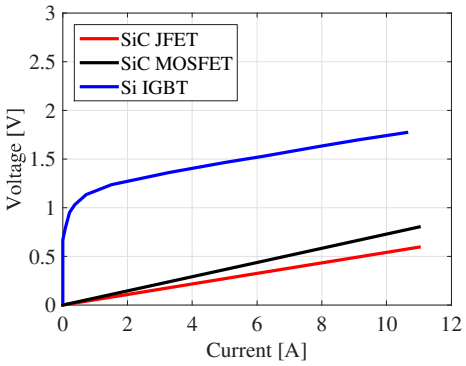


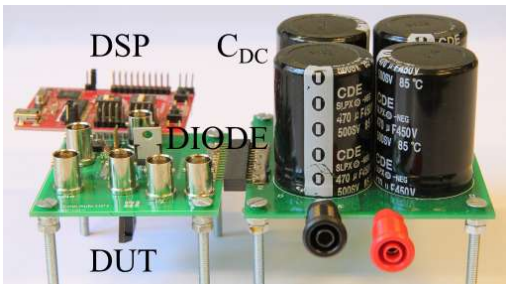
Fig. 2. Forward voltages of different switching devices at 25 °C junction temperature

E. Dynamic characteristics

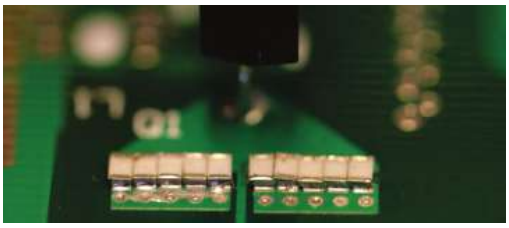
Another benefit when using SiC devices are the reduced switching losses in a given converter application. In an initial design approach, switching energies are mostly compared based on the information provided in the datasheet. However, this may lead to unfair comparisons if the test setup differ from one manufacturer to another (use of different free-wheeling diodes with different reverse recovery currents, different gate resistors, etc.). Therefore, this work compares the switching energies at exactly the same test conditions including the same inductor and the same free-wheeling diode. Furthermore, the gate resistors are adjusted to maintain a similar peak gate current for a fair comparison. The test setup is shown in Fig. 3a and the current measurement (flat current shunt) is shown in Fig. 3b which has been presented in [28].

The gate-source/gate-emitter voltages are measured with a LeCroy PP011 voltage probe having a bandwidth of 500 MHz, the drain-source/collector-emitter voltages are measured with a 400 MHz LeCroy PPE4kV voltage probe. The voltage drop across the shunt resistor is measured with a LeCroy PP011 voltage probe as well which is then translated back to the current according to Ohm's law. The turn on switching transitions of all three devices are shown in Fig. 4. One can clearly see the superior switching performance of the two SiC switching devices compared to the Si IGBT. All waveforms are captured such that the gate turn on occurs at the same time. The SiC MOSFET and the SiC JFET show similar switching speeds. Where the SiC MOSFET has a lower di/dt compared to the SiC JFET, its dv/dt is higher. Hence similar turn on switching energies are expected for the MOSFET and the JFET.

The turn off switching transitions are shown in Fig. 5 in order to complete the dynamic performance comparison. Also during the turn off events, both SiC switching devices show much faster transitions than the IGBT. However, within the comparison of SiC devices, the MOSFET turns off quicker than the SiC JFET alternative. Maximum dv/dt and di/dt values for each switching device are shown in Table II in order to quantify the switching transitions. Having the voltage and



(a) Double pulse test setup



(b) Current measurement

Fig. 3. Double pulse test setup and current measurement

current measured on the oscilloscope, switching energies can then be obtained by numerically integrating the instantaneous power (which is simply the product of the measured voltage and current). The results of this procedure for currents from 2 A to 10 A are shown in Fig. 6. It verifies that the Si IGBT has highest switching energies for both turn on and turn off, though the discrepancy is larger at the turn off energies. That is mainly due to the tail current associated to Si IGBTs. Especially at larger currents, the SiC devices outperform the Si IGBT. Comparing the SiC switching devices, the SiC MOSFET shows lower turn off switching energies compared to its SiC JFET competitor at increased currents.

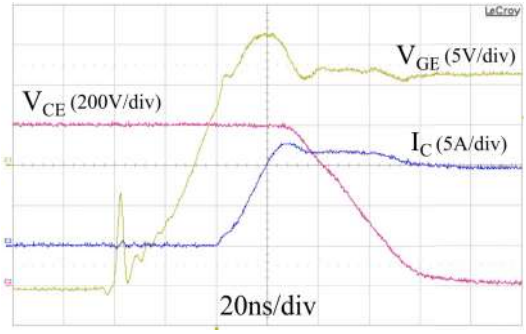
III. Boost Converter

Based on the previous analysis, the performance comparison between the SiC switching devices can be extended to a loss analysis for a given power converter; in this work it is a boost converter with specifications for a typical PV system whose block diagram is shown in Fig. 7a. The main components of the boost converter are the boost inductor L, the switching element S and a diode D as depicted in Fig. 7b. Assuming continuous conduction mode (CCM) with two different input voltages, 400 V and 500 V, and a fixed output voltage of 700 V, the duty cycle d can then be calculated according to

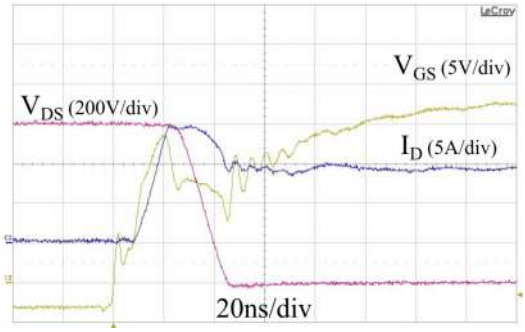
$$d = 1 - \frac{V_{in}}{V_{out}} \tag{3}$$

TABLE II
Switching evaluation

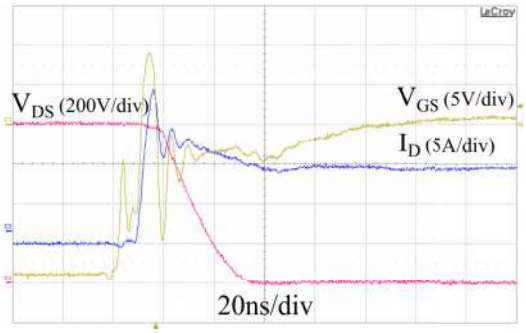
	Turn on			Turn off		
	IGBT	MOSFET	JFET	IGBT	MOSFET	JFET
dv/dt in kV/µs	16	40	23	8	27	18
di/dt in kA/µs	0.5	1.1	3.3	0.06	0.3	0.2



(a) Turn on IGBT, $R_g = 18\,\Omega$



(b) Turn on MOSFET, $R_g = 18\,\Omega$



(c) Turn on JFET, $R_g = 10\,\Omega$

Fig. 4. Turn on transitions. $V_{DC} = 800$ V, $I = 10$ A

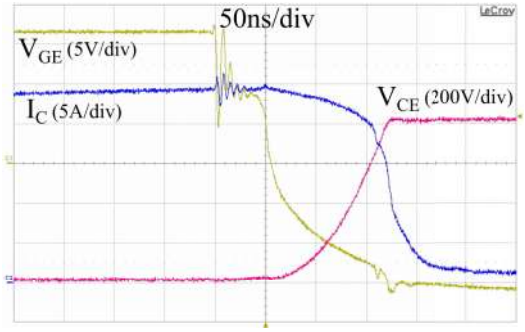
Maximum output power is set to 4 kW in this work to represent a residential PV system. The DC component of the current flowing through the boost inductor can then be calculated

$$I_{L\,DC} = \frac{V_{in} P_{out}}{(1-d)^2 V_{out}^2} \tag{4}$$

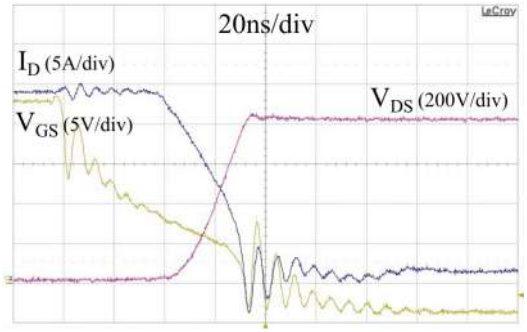
The current ripple is often a crucial factor when designing the boost converter as it creates harmonics and causes EMI. A typical design procedure is to limit the current ripple ΔI to be around 20 % of the DC current. With a switching frequency f_{sw} initially set to 20 kHz in order to avoid audible noise coming from the inductor, the size of the inductor is calculated to be 3 mH.

$$L = \frac{V_{in} d}{2 \Delta I f_{sw}} \tag{5}$$

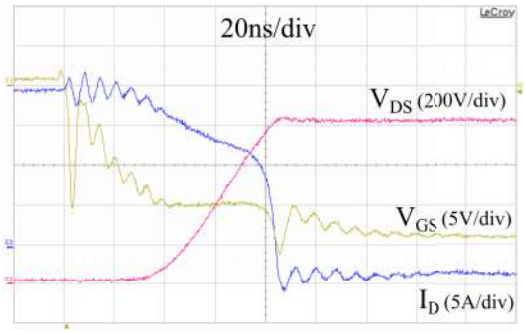
This yields in a current ripple of 22 %. The 3 mH boost inductor is taken from a commercial PV inverter and it



(a) Turn off IGBT, $R_g = 18\,\Omega$



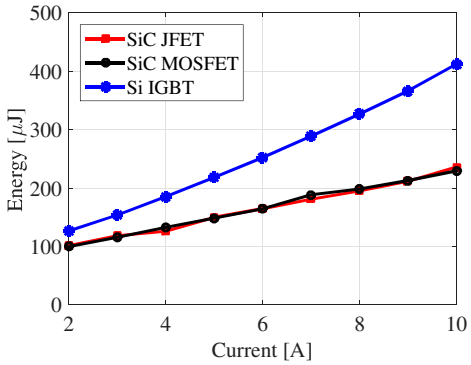
(b) Turn off MOSFET, $R_g = 18\,\Omega$



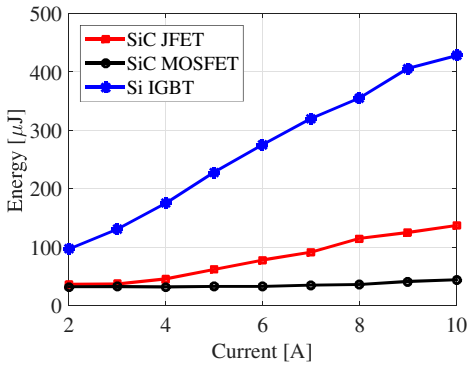
(c) Turn off JFET, $R_g = 10\,\Omega$

Fig. 5. Turn off transitions. $V_{DC} = 800\,\text{V}$, $I = 10\,\text{A}$

comprises of six KoolMu 77439-A7 cores stacked together with 60 turns. Taking advantage of the superior switching characteristics of the SiC switching devices, the switching frequency is increased to 100 kHz in this work which then reduces the size of the inductor for a given current ripple according to Eq. (5). The new inductor is set to 1 mH which will result in a current ripple percentage of 13 % only. This gives a current ripple decrease of more than 40 %. The new inductor is made of one MPP 55192-A2 core which in general may be more expensive than KoolMu, but it has a superior core loss performance which is very attractive at increased switching frequency operation. Also, due to the reduction in inductor size, only one core is necessary whereas the 3 mH core uses six KoolMu cores stacked together. Table III summarizes the most important specifications and Fig. 8 shows both inductors used in this work.

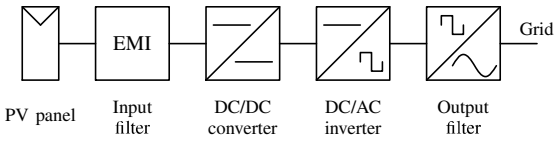


(a) Turn on energies

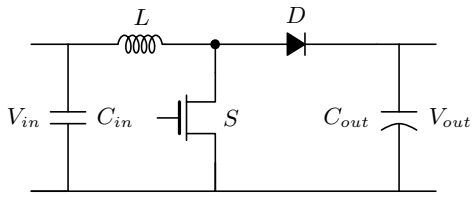


(b) Turn off energies

Fig. 6. Switching energy comparison of the three devices for different current levels. $V_{DC} = 800\,\text{V}$



(a) Block diagram of a PV inverter system



(b) Boost converter

Fig. 7. Block diagram of PV system in (a), schematic of a single phase boost converter in (b)

TABLE III
BOOST INDUCTOR PARAMETERS

	Inductor 1	Inductor 2
Inductance in [mH]	3	1
Cores	6xKoolMu 77439-A7	1xMPP 55192-A2
Turns	60	88
Volume in [cm^3]	345	72
Weight in [g]	1000	230

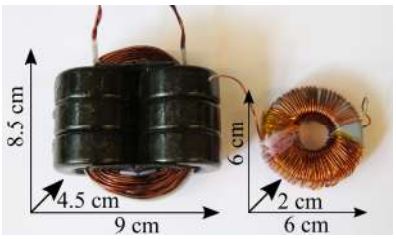


Fig. 8. Boost inductors used for different switching frequencies

A. Loss analysis

Since this work primarily compares the performances of the switching devices, the loss analysis focuses on the semiconductor losses only as this is where the loss reduction occurs. The conduction losses in the Si IGBT and the SiC diode can be expressed using piece-wise linear models, i.e.

$$P_{con\,Si,D_x} = V_f I_{AV} + r_{on} I_{rms}^2 \tag{6}$$

where V_f represents the zero on-state voltage, I_{AV} the average current through the switching device, r_{on} the dynamic on-state resistance and I_{rms} the root-mean-square (RMS) value of the current through the switch. The SiC MOSFET and SiC JFET are unipolar devices and hence only the on-resistance $R_{DS(on)}$ is used to calculate the conduction losses,

$$P_{con\,SiC} = R_{DS(on)} I_{rms}^2 \tag{7}$$

Referring to Fig. 6, the switching energies show a linear relationship to the current. Assuming the small ripple approximation, switching energies for a given base voltage ($V_{Base} = 800V$ in this work) can be described as

$$E_{on\,Si,SiC} = a_{on} I_{L\,DC} + b_{on} \tag{8}$$

$$E_{off\,Si,SiC} = a_{off} I_{L\,DC} + b_{off} \tag{9}$$

with a_{on},a_{off},b_{on} and b_{off} being the curve fitting constants. Switching losses can then be obtained by linear scaling the switching energies to the given switching voltage of the device (which is the output voltage in the case of a boost converter) and by multiplying the result with the chosen switching frequency f_{sw}

$$P_{sw} = f_{sw} \frac{V_{out}}{V_{Base}} \left(E_{on\,Si,SiC} + E_{off\,Si,SiC} \right) \tag{10}$$

Applying Eq. (6)-Eq. (10), the semiconductor losses can be calculated for any given operating point. As an example, for an output power of 2.5 kW and the two different input voltages (namely 400 V and 500 V), the results for the semiconductor loss breakdown analysis are shown in Fig. 9. The IGBT switching losses show a dominant contribution to the overall semiconductor losses. For instance, at an input voltage of 400 V, switching losses in the IGBT are 11.8 W whereas the switching losses of the SiC MOSFET are only 4.3 W which gives a switching loss reduction of more than 60 %. Not only switching loss reduction occurs by replacing the switching element to a SiC device. Also conduction losses

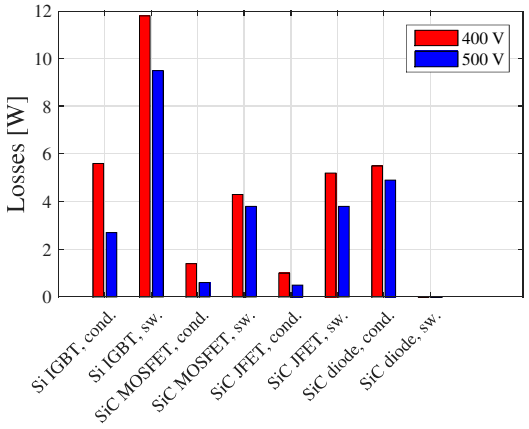


Fig. 9. Semiconductor loss breakdown analysis

can be drastically reduced. Taking an input voltage of 400 V as an example, conduction losses in the Si IGBT are 5.6 W and can be reduced down to 1.4 W with a SiC MOSFET. This gives a conduction loss reduction of 75 %. The diode contributes to the semiconductor losses with 5.5 W. A total semiconductor loss reduction of 11.7 W is achieved with the utilization of SiC MOSFETs for an input voltage of 400 V. Thus total semiconductor losses can be reduced by more than 50 %.

B. Experimental results

To verify the loss modeling approach from the previous section, a boost converter prototype is designed and shown in Fig. 10. Efficiencies for an output power up to 4 kW are recorded using a N4L PPA5500 power analyzer with a basic accuracy of 0.02 % and which can measure harmonics up to 2 MHz. The operating specifications are given in Table IV. Starting with a switching frequency of 20 kHz and 400 V input voltage, the results are shown in Fig. 11a and for an input voltage of 500 V, the results are presented in Fig. 11b. Both graphs show that both the Si and SiC based converters can achieve high efficiencies over 98 % throughout almost the entire operating range. Using SiC switching devices, maximum efficiency improvements of around 0.4 % can be achieved

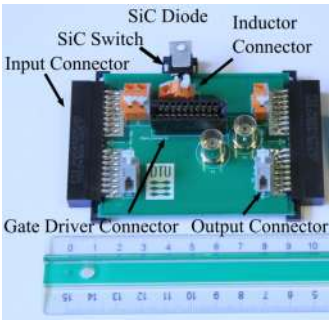


Fig. 10. Prototype of a 4 kW boost converter, heatsink not shown

TABLE IV
SPECIFICATIONS

Symbol	Meaning	Value
V_{in}	Input voltage	400 V to 500 V
V_{out}	Output voltage	700 V
f_{out}	Switching frequency	20 kHz, 100 kHz
L_{out}	Boost inductor	3 mH, 1 mH

which is a semiconductor loss reduction of more than 12 W. It is now possible to compare the predicted semiconductor loss reduction based on the modeling approach from the previous section with the measurements presented in this section. Fig. 12 shows that the predictions and measurements match well throughout the entire operating range. Furthermore, it states that the loss reduction with SiC based converters is greater at lower input voltages. The reason for that lies in the larger input current and duty cycle of the switch for a given output voltage and output power, which then stresses the switching element more because of the increased switched current (larger switching losses) combined with the larger conduction losses due to the larger RMS current through the switch.

Since the modeling approach from the previous section matches well with the measurements, the semiconductor loss models can be used with confidence for further analysis, presenting the semiconductor losses for the three switching devices in Fig. 13 in order to give a direct performance comparison. The increase in semiconductor losses against the output power is greatest for the IGBT whereas the MOSFET and the JFET show similar performance behavior. The reason for that is that the MOSFET has lower switching energies compared to the JFET, but its on-resistance is higher which,

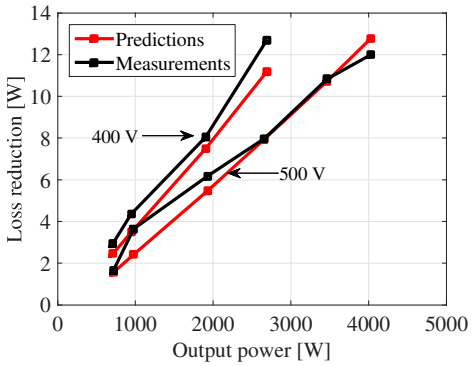
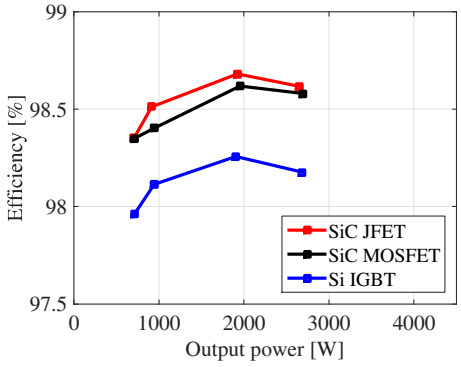
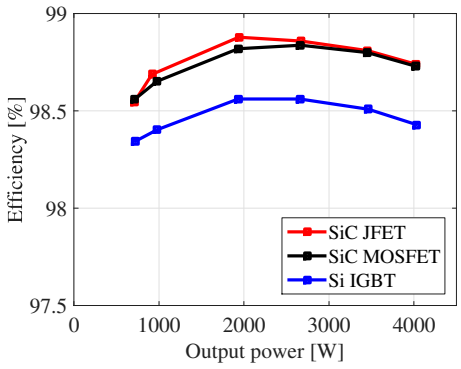


Fig. 12. Measured loss reduction versus predicted loss reduction. The comparison is based on the Si IGBT and the SiC JFET based converter

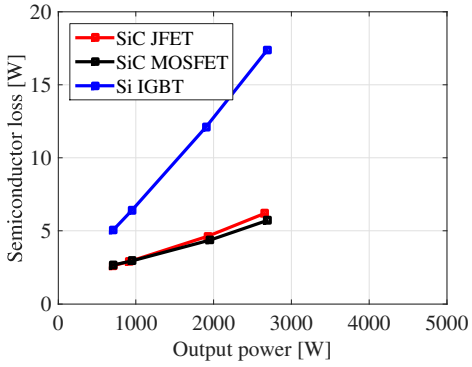


(a) Efficiencies for $V_{in} = 400$ V

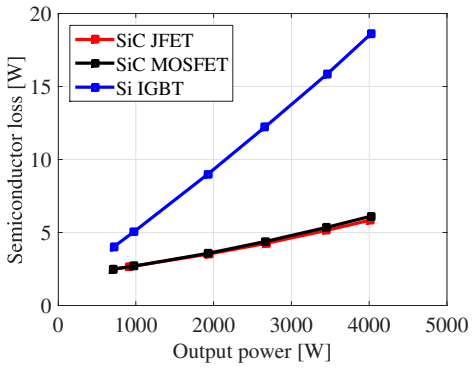


(b) Efficiencies for $V_{in} = 500$ V

Fig. 11. Efficiency measurements for a switching frequency of 20 kHz and an input voltage of 400 V in (a) and for an input voltage of 500 V in (b)

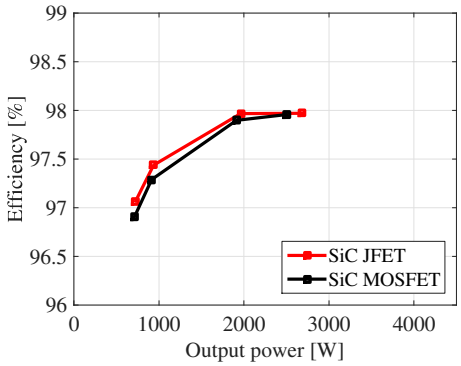


(a) Semiconductor loss for $V_{in} = 400$ V

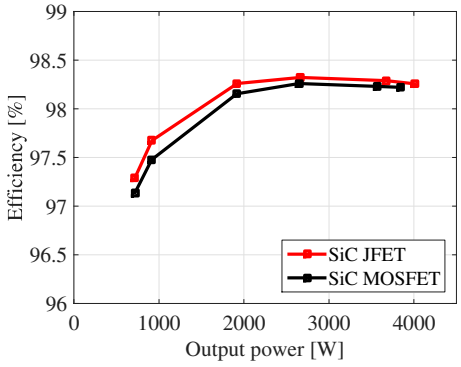


(b) Semiconductor loss for $V_{in} = 500$ V

Fig. 13. Semiconductor losses of the switching elements for different input voltages and output power

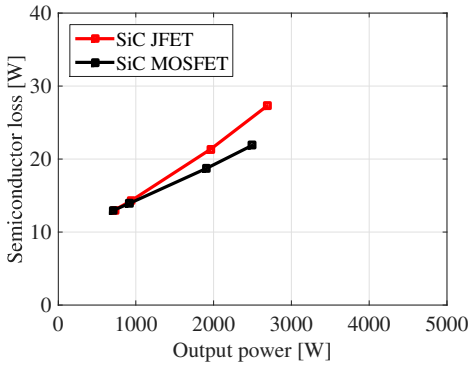


(a) Efficiencies for $V_{in} = 400\,\mathrm{V}$

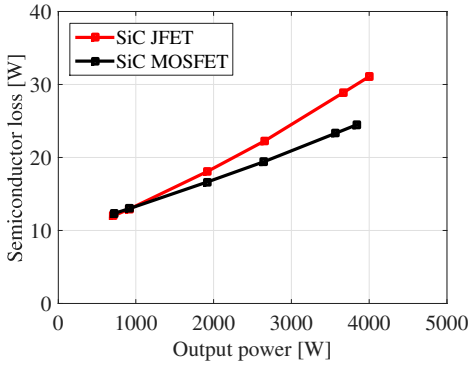


(b) Efficiencies for $V_{in} = 500\,\mathrm{V}$

Fig. 14. Efficiency measurements for a switching frequency of 100 kHz and an input voltage of 400 V in (a) and for an input voltage of 500 V in (b)



(a) Semiconductor loss for $V_{in} = 400\,\mathrm{V}$



(b) Semiconductor loss for $V_{in} = 500\,\mathrm{V}$

Fig. 15. Semiconductor losses of the switching elements for different input voltages and output power

in the end, results in very similar total semiconductor losses throughout the entire operating range.

Using SiC switching devices for increased switching frequency operation, in order to reduce the size of the passive components measurements are repeated for 100 kHz operation with the 1 mH inductor. The results are shown in Fig. 14. Also at higher switching frequencies, efficiencies are still close to each other and a peak value of up to 98.3 % is achieved. Only at low power operation, a significant drop in efficiency is present mainly because the switching losses and the core losses are major contributions in that operating range. It is worthy of comment that the SiC JFET seems to have higher efficiencies especially in the lower power range. Referring to Fig. 6, the SiC JFET has quite competitive turn off switching energies to the SiC MOSFET at low currents and the difference becomes only significant as the current increases. However, as the current increases at increased output power, the JFET can benefit from its lower on-resistance. Therefore, instead of looking at the overall efficiencies, semiconductor losses are used (based on the modeling approach from the previous section), shown in Fig. 15. One can see that the semiconductor losses of the SiC MOSFET become slightly lower compared to the JFET - especially at increased power levels. That is due to the superior turn off energies of the MOSFET which outperform the lower conduction losses of the JFET at this particular switching frequency. From a semiconductor loss point of view, the SiC MOSFET has total losses of almost 22 W at 400 V input voltage whereas the JFET has around 26 W. However, such loss reduction of 4 W operating at 2.6 kW output power has only a minor influence on the overall efficiency. The same statement can be extended to the operation with 500 V input voltage and up to 4 kW output power. Hence for the given specifications in this work, both the JFET and the MOSFET perform very similar in terms of semiconductor losses.

IV. Conclusion

In this paper, three state of the art switching devices have been compared to each other. The comparison uses analytical semiconductor loss models based on conduction losses derived from datasheet information, and switching losses obtained via switching transition measurements. The loss models and hence the predicted semiconductor loss reduction with the use of SiC switching devices are verified using electrical power measurements in a boost converter operating under various conditions up to 4 kW. Both SiC based converters achieve high efficiencies of up to 98.8 % at a switching frequency of 20 kHz, which is 0.4 % higher than its Si alternative. At that operating frequency, both SiC alternatives perform very similar. With SiC switching devices utilized, operating

frequency is increased up to 100 kHz which reduces the boost inductance from 3 mH down to 1 mH. This not only reduces the current ripple from 22 % down to 13 %, but also reduces the size and weight of the inductor by over 75 %. Even at 100 kHz operation, competitive efficiencies of up to 98.3 % can be achieved and both SiC alternatives show similar semiconductor losses. Therefore, within the specifications in this work, one SiC switching device can not be favored over the other based on a loss point of view.

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Appendix I

The Benefits of SiC MOSFETs in a T-Type Inverter for Grid-Tie Applications

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The Benefits of SiC MOSFETs in a T-Type Inverter for Grid-Tie Applications

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***Abstract*—It is well known that multilevel converters can offer significant benefits in terms of harmonic performance and reduced switching losses compared to their two-level counterparts. However, for lower voltage applications the Neutral-Point-Clamped (NPC) inverter suffers from relatively large semiconductor conduction losses because the output current always flows through two switching devices. In contrast, the T-Type multilevel inverter has less conduction losses because only a single outer loop switching device is required to connect the converter output to the upper and lower DC buses, albeit at the expense of increased switching losses since these outer switches must now block the full DC link voltage. Silicon Carbide (SiC) MOSFET devices potentially offer substantial advantage in this context with their lower switching losses, but the benefit of replacing all switching devices in a T-Type inverter with SiC MOSFETs is not so clear-cut. This paper now explores this issue by presenting a detailed comparison of the use of Si and SiC devices for a three-level T-Type inverter operating in grid-tie applications. The study uses datasheet values, switching loss measurements and calibrated heat sink thermal measurements to blueprecisely compare semiconductor losses for these two alternatives for a T-Type inverter operating at or near unity power factor. The results show that replacing only the DC bus connection switches with SiC devices significantly reduces the semiconductor losses, allowing either the converter power level or the switching frequency to be significantly increased for the same device losses. Hence the use of SiC MOSFETS for T-Type inverters can be seen to be an attractive and potentially cost effective alternative, since only two switching devices per phase leg need to be upgraded.**

***Keywords*—Photovoltaic, Semiconductor losses, Si IGBT, SiC MOSFET, T-Type Inverter**

I. Introduction

RENEWABLE energy generation has been gaining increasing interest in the last two decades. Among the renewable energy alternatives, photovoltaic (PV) generation is one of the most significant with a total global capacity of 139 GW in 2013 [1]. In the residential sector, single- and three phase PV systems are widely used and are typically grouped into systems with and without galvanic isolation. The latter approach has the particular benefits of higher efficiency, higher power density and lower cost due to the absence of the transformer [2], which are important design criteria for low cost PV systems. Recent studies [2]–[4] have compared in detail two- and three-level inverter topologies based on semiconductor losses and filter considerations, and have identified that in particular for higher switching frequencies, three-level inverter topologies can have lower semiconductor losses than their two-level counterparts because each switching event needs only commutate half the DC link voltage at each transition [3], [4]. Furthermore, since the AC output of a three-level inverter has a lower harmonic content because of its improved harmonic cancellation [5], significant size reductions of the AC filter components are possible [3].

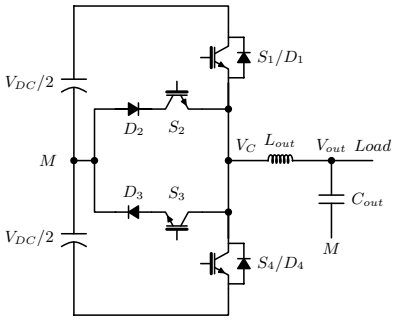
Of the various three-level inverter topologies available, the most mature configuration is the Neutral-Point-Clamped (NPC) inverter [6], which has been intensively researched since its introduction in 1981. The particular benefit of this converter is that it can be realized with semiconductor devices that need to block only half the DC link voltage. However, while this reduces switching losses [4], the topology suffers from higher conduction losses and an uneven device loss distribution because current must always flow through two semiconductor devices [7], [8]. A more recent alternative is the T-Type inverter [9], [10], which achieves the same converter harmonic output performance but only requires a single switch to connect its output to the upper and lower DC buses. However, the topology must consequently use semiconductors with higher voltage ratings for its outer switches since they now have to block the full DC link voltage, which means that its semiconductor switching losses are generally higher compared to a NPC converter at the same switching frequency [4]. Thus the choice of switching frequency becomes a crucial parameter in selecting between a NPC and T-Type inverter for any particular application [4]. Essentially, T-Type inverters have lower semiconductor losses at lower switching frequencies because of their reduced conduction losses, while NPC inverters become more advantageous at higher switching frequencies where switching losses become more significant.

Recent work has explored in some detail various ways to minimize T-Type three level inverter losses. For example the loss benefit of optimized discontinuous modulation (DPWM) [9] can be traded off against its increased AC output harmonic content [5]. Another alternative is to replace the Si diodes in the inner bi-directional path with SiC diodes to reduce reverse recovery losses [11]. However further work has identified that the primary limiting factor for efficient high switching frequency operation at unity power factor (as is generally required for residential PV inverter systems [12]) is still the switching losses in the DC bus connection switches [11]. [13] compares an optimally designed hard switched

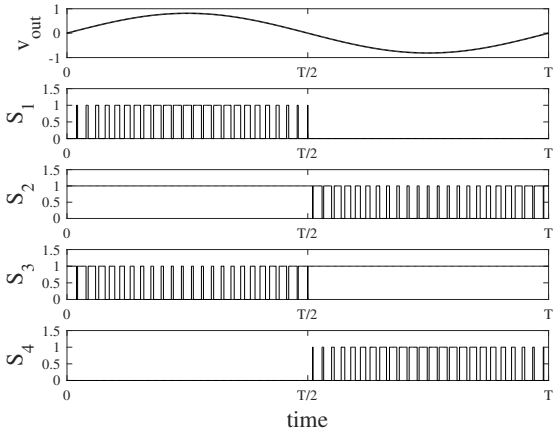
SiC based T-Type inverter against an optimally designed Zero-Voltage-Switching (ZVS) T-Type inverter, and concludes that the latter can only slightly increase the system efficiency at the cost of considerably more complexity. Essentially, the focus of most approaches to date has been to attempt to work around the basic T-Type inverter switching frequency limitation, which is that the outer DC bus connection switches have higher switching losses compared to a NPC inverter because they must have higher voltage rating to block the full DC link voltage. This paper now presents investigation results for the more direct approach of simply replacing the T-Type inverter outer switch 1200 V Si IGBTs (higher switching loss) with 1200 V SiC MOSFETs (lower switching loss). Of course the loss reduction advantages in principle of SiC devices compared to Si devices are already well established [14]–[22], but their benefit in the context of a T-Type inverter is not so clear-cut. This is because while the outer switches of a T-Type inverter must be rated to block the full DC link voltage, they only commutate at half the DC link voltage when actively switching. Thus their switching losses are substantially reduced compared to their normal rated operating conditions and hence analysis is required to determine the level of benefit to be gained by moving to SiC devices in this context. The methodology used in the investigation is to precisely identify the switching and conduction losses of both types of switching devices when the inverter is operating under the same conditions, using detailed semiconductor loss models based on datasheets and experimentally measured switching losses. Using these models, the potential increase in switching frequency or power rating that can be achieved using SiC MOSFETs as the outer switching devices can be determined as the overall inverter semiconductor losses are kept at the same value.

II. T-Type Inverter Description and Device Selection

Figure 1a shows the basic structure of one phase leg of a three-level T-Type inverter, comprising a HV DC link with split bulk capacitors, four switching devices, four diodes and an AC filter to obtain the target AC output voltage. The converter switches are operated as the complementary pairs S_1/S_3 and S_2/S_4 in accordance with Table I, to achieve the required switched output voltages of $+V_{DC}/2$, 0 and $-V_{DC}/2$ that produce a three level AC output voltage. Note that the switching states shown in Table I achieve the same switched output voltages as a NPC inverter (i.e. switch S_1 is closed to achieve a positive output voltage, S_2 or S_3 needs to be closed for a zero output voltage, and switch S_4 is closed for a negative output voltage) even though the detail switch usage is different for the two converter topologies. Figure 1b shows the switch commands created when the converter is controlled using the optimum phase disposition (PD) PWM strategy [23], [24], where the characteristic discontinuous operation of the two switch pairs can be clearly seen. Fig. 2a-Fig. 2c present a more detailed illustration of the switching transition between the zero output state and the positive output state for unity power factor operation during the fundamental positive half



(a) Single phase schematic of the T-Type inverter



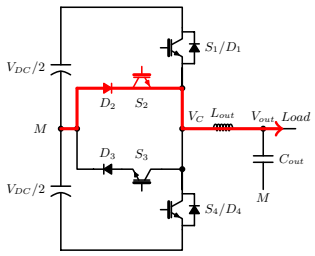
(b) PD PWM for three level inverter with a fundamental frequency of 50 Hz

Fig. 1: Schematic of T-Type inverter topology in (a) and its modulation principle in (b)

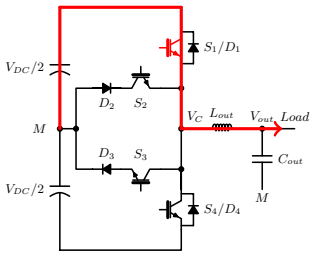
TABLE I: Switching states for T-Type inverter

Output voltage	S_1	S_2	S_3	S_4
$V_{DC}/2$	1	1	0	0
0	0	1	1	0
$-V_{DC}/2$	0	0	1	1

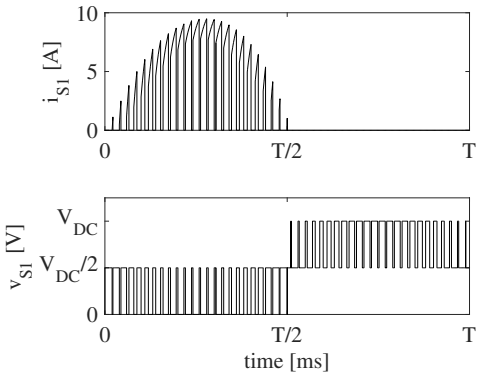
cycle. During the zero output state, the positive output current flows from the midpoint M through diode D_2 and switch S_2 to the load as shown in Fig. 2a, and the voltages blocked by switches S_1 and S_4 are both $V_{DC}/2$. Switch S_1 then turns on to create the positive output state, commutating the output current from D_2/S_2 to S_1 against an off-state voltage of $V_{DC}/2$ with associated switching losses, as shown in Fig. 2b. Outer switch S_4 now blocks a voltage of V_{DC}, depicted in Fig. 2f. This cycle repeats throughout the fundamental positive half cycle as shown in the left hand side of Fig. 2c. By symmetry, a similar switching process occurs during the fundamental negative half cycle as shown in Fig. 2d-Fig. 2f, with a switching commutation between D_3/S_3 and S_4 against an off-state voltage of $V_{DC}/2$, and with switch S_1 alternately blocking a voltage of $V_{DC}/2$ and V_{DC} as the output voltage changes from zero to negative, as shown in Fig. 2c. Thus



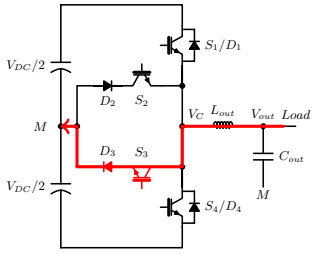
(a) Zero output voltage and positive output current



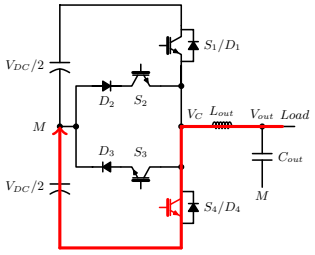
(b) Positive output voltage and positive output current



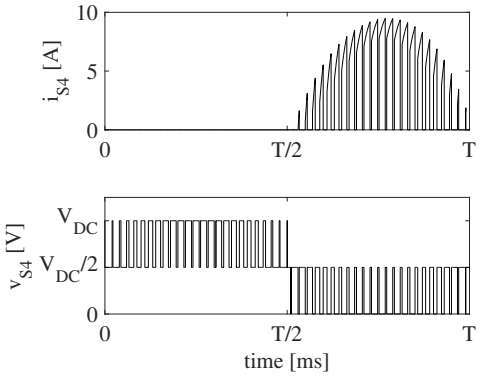
(c) Voltage across and current through S_1 along one fundamental cycle



(d) Zero output voltage and negative output current



(e) Negative output voltage and negative output current



(f) Voltage across and current through S_4 along one fundamental cycle

Fig. 2: Switching states for T-Type inverter operating at unity power factor

outer switches S_1 and S_4 must have a voltage blocking rating in excess of V_{DC}, even though their commutation switching voltage is only $V_{DC}/2$. This complicates their overall loss calculation since their on-state voltages will be typically higher than a lower voltage rated device [3], but their switching losses need to be determined at only half their rated voltage because of the operating sequence described above. In contrast, the inner switches S_2 and S_3 see only a reduced voltage blocking rating of $V_{DC}/2$ with corresponding lower forward conduction losses [3]. Also, since these switches do not have to commutate current when operating at unity power factor, they will have negligible switching losses irrespective of the type of switching device used. Furthermore, even with a near unity load power factor, their switching losses will still be quite small since they are commutating only low magnitude currents close to the fundamental current zero crossing transition.

Since for a typical residential PV system the DC link voltage can reach up to 1000 V, 1200 V rated devices are required for the outer switches S_1 and S_4 for a T-Type inverter operating in this application, while 600 V semiconductor devices are adequate for the inner parallel-connected devices $D_{2,3}$ and $S_{2,3}$. Hence this is the rating of the switching devices used in this investigation, as shown in Table II. The choice between using a 2nd or 3rd generation IGBT for the study was made on the following basis. Comparing their datasheet parameters, Infineon's 2nd generation IGBT devices are better optimized for lower switching frequencies, having 35 % lower conduction losses and 20 % higher switching losses than the Infineon 3rd generation IGBTs [25], [26]. Hence, since a T-Type inverter typically switches at a relatively low switching frequency, and the outer devices also only need to commutate current at less than half their rated voltage, a 2nd generation IGBT with ratings comparable to the chosen SiC MOSFET was selected as the more appropriate alternative for the comparison against the SiC MOSFET presented in this paper. The current rating for all devices was chosen to suit a 230 V 1.5 kW rated system (approx. 10 A peak current) with a 20 % overload capacity and a conservative 30 % to 40 % de-rating factor for long life reliability. Also SiC devices were used for all diodes to minimize the influence of reverse recovery charge on the switching device loss evaluation.

III. Loss Evaluation of Si and SiC Switching Devices

Evaluation of the semiconductor loss profiles for Si IGBTs and SiC MOSFETs requires quantification of the conduction and switching characteristics for both switch families in the context of the T-Type inverter application. For conduction losses it is sufficient to use manufacturer's datasheets which provide detailed performance data for the IGBT saturation voltages, the MOSFET $R_{DS(on)}$, and the forward voltage of the anti-parallel diodes [4]. However it is more difficult to determine the switching loss behavior of these devices from datasheets, particularly when they are operated well outside the test conditions that are used to obtain the datasheet results. Typically, switching energies need to be determined for particular operating conditions such as gate resistances, gate drive voltage, junction temperature and different types of free-wheeling diodes [4]. Hence to obtain a fair comparison for the switching loss behavior between IGBT and SiC devices, their switching energies were experimentally measured using the prototype T-Type inverter developed for this study.

A. Conduction Losses of the S_1 and S_4 devices

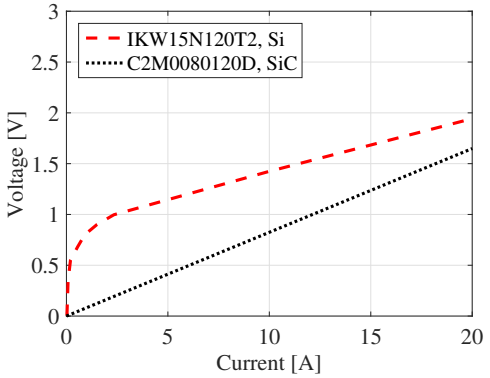
Conduction losses are determined by the voltage drop across the device and the current that is flowing through the device whilst turned on. These losses represent a major contribution to the overall semiconductor loss profile. The specified forward voltages of the selected IKW15N120T2 Si IGBT, and the C2M0080120D SiC MOSFET at different current levels as shown in Fig. 3 can be used to determine these conduction losses. Note that the SiC MOSFET has a significantly smaller voltage drop than the IGBT over most of the inverter's operating current range, which leads to smaller conduction losses. This is because the SiC MOSFET is an unidirectional device with a resistive output characteristic. Thus a smaller current flowing through the device will cause a smaller voltage drop according to Ohm's law. In contrast an IGBT is a bidirectional device with a bipolar output characteristic. This results in a larger voltage forward drop, especially for low currents.

B. Switching Characteristics

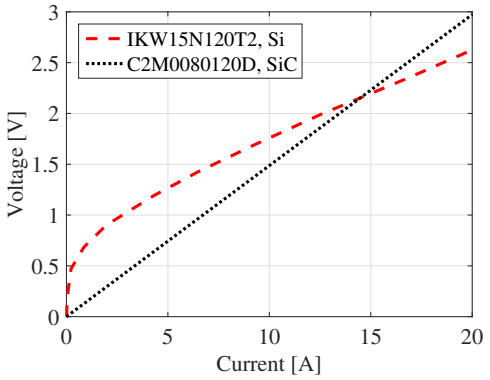
In order to adequately assess the switching characteristics and hence the switching energies of the devices, their switching transitions were measured directly using the laboratory prototype shown in Fig. 4a, with the switching voltages measured using oscilloscope probes places as shown in Fig. 4b.

TABLE II: Semiconductors used

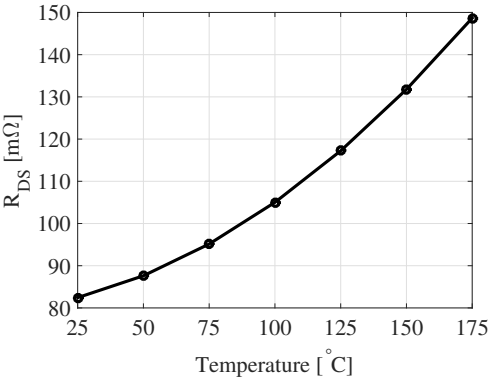
Semiconductors	Device	Voltage [V]	Current at 25 °C [A]	Price [USD]	Package
$S_{1,4Si}$	IKW15N120T2	1200 V	30 A	3.9	TO-247
$S_{1,4SiC}$	C2M0080120D	1200 V	36 A	16.03	TO-247
$D_{2,3SiC}$	C3D10060A	600 V	29.5 A	4.02	TO-220
$S_{2,3Si}$	IKP15N60T	600 V	30 A	1.6	TO-220
$D_{1,4SiC}$	C4D15120A	1200 V	41 A	16.88	TO-220



(a) Forward voltages of Si IGBT and SiC MOSFET at 25 °C junction temperature



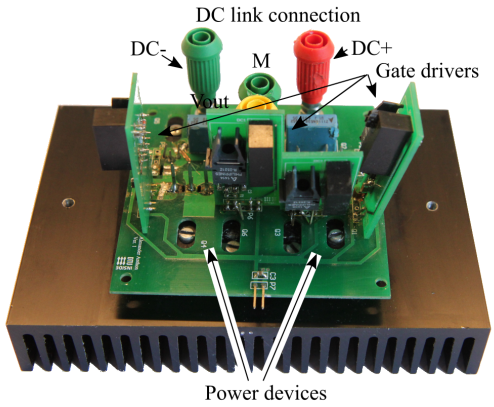
(b) Forward voltages of Si IGBT and SiC MOSFET at 175 °C junction temperature



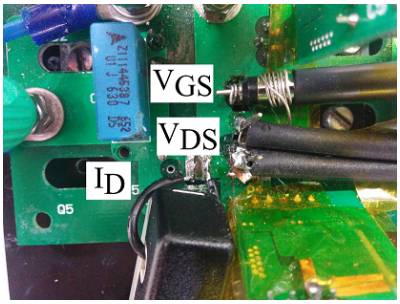
(c) SiC MOSFET on-resistance R_{DS} versus junction temperature

Fig. 3: Si IGBT forward voltage and SiC MOSFET on-resistance at different current levels and junction temperatures

The current measurements were made using a Tektronix TCP305 current probe having a bandwidth of 50 MHz. The gate-emitter voltage for the IGBT and the gate-source voltage for the MOSFET were measured using a Textronx



(a) Prototype of the T-Type inverter

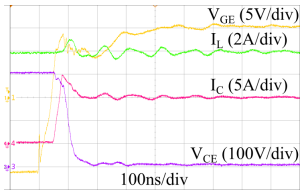


(b) Switching energy measurements on the T-Type prototype

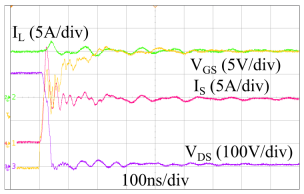
Fig. 4: Prototype in (a) and current measurement in (b)

P220 voltage probe with a bandwidth of 200 MHz. The collector-emitter voltage for the IGBT and the drain-source voltage for the MOSFET were measured using a high voltage differential probe with a bandwidth of 50 MHz. Compensation was included into the waveform analysis procedure to allow for the specified delay times of 19 ns for the current probe and 15 ns for the differential voltage probe. Waveforms of the measured turn on and turn off switching transitions at 400 V and 10 A for both the Si IGBT and the SiC MOSFET in the T-Type inverter are shown in Fig. 5, since this is the identified switching conditions for this inverter as discussed above. From these figures it is clear that the SiC MOSFET has superior switching characteristics in terms of di/dt and dv/dt. For example, at the turn off transition in Fig. 5c and Fig. 5d, the SiC MOSFET switches at almost 16 kV/µs whereas the Si IGBT switches at less than 3 kV/µs. Table III quantifies the turn on and turn off switching characteristics shown in Fig. 5 for the two devices. Measuring the voltage and current transitions in this way for a variety of operating conditions, such as different current levels and junction temperatures, switching energies can then be obtained by numerically integrating the product of the measured voltages and currents.

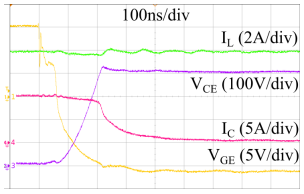
Fig. 6 presents the turn-on and turn-off energies for the Si IGBT and the SiC MOSFET determined using this approach



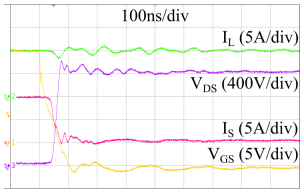
(a) Turn on Si IGBT



(b) Turn on SiC MOSFET



(c) Turn off Si IGBT



(d) Turn off SiC MOSFET

Fig. 5: Turn on and turn off switching transitions for a voltage of 400 V and 10 A

for operation at both low and high temperatures. Note that while the turn-on energy magnitudes for both the Si and the SiC devices are relatively low, the Si IGBT still must dissipate more than twice the turn-on switching energy of the SiC MOSFET. From these results it can be seen that the major benefit of the SiC MOSFET is its very low turn off energies which are almost constant over the current and temperature range of interest. In contrast the IGBT has much larger switching energies that increase linearly with current. It is further worthy of comment that the temperature majorly influences only the turn off energies of the Si IGBT, while hardly affecting any of the other switching energies (especially the SiC MOSFET). From the measurements, it can be seen that the turn off switching energies of the IGBT are more than 17 times higher than those of the SiC MOSFET at a current of 3 A and more than 22 times higher at a current of 7 A. These very low SiC MOSFET switching energies are a very attractive characteristic as switching frequency is usually the limiting factor for higher frequency operation of a T-Type inverter due to the large turn-off energy loss of a Si IGBT [11].

C. Semiconductor Loss Modeling

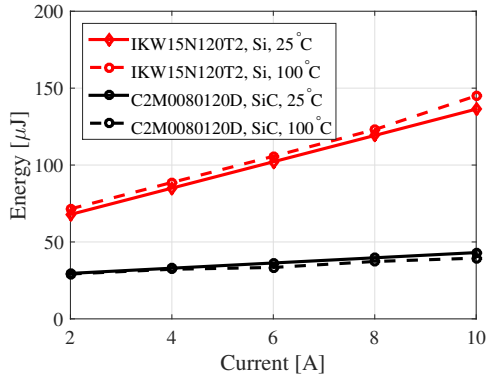
Based on these results, a model for the semiconductor losses can now be obtained. Piece-wise linear models for the IGBTs and diodes are commonly used to model conducting losses for such studies, and so are used in this work, i.e.

$$P_{con,IGBT} = V_0 I_{AV} + r_{on} I_{rms}^2 \quad (1)$$

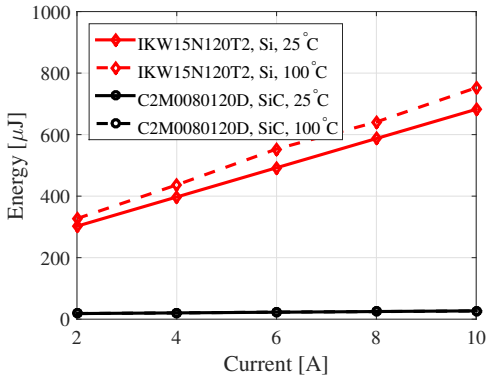
$$P_{con,Diode} = V_T I_{AV} + r_{on} I_{rms}^2 \quad (2)$$

TABLE III: Switching evaluation

	Turn on		Turn off	
	IGBT	MOSFET	IGBT	MOSFET
dv/dt in kV/µs	7.8	13.3	2.84	15.9
di/dt in A/µs	0.45	1.33	0.05	0.2



(a) Turn on energies



(b) Turn off energies

Fig. 6: Measured turn on and turn off switching transitions for a voltage of 400 V and 2 A to 10 A

where V_0 is the zero on-state voltage of the IGBT, V_T is the diode's threshold voltage, I_{AV} is the average current, r_{on} the dynamic on-state resistance and I_{rms} the root-mean-square (rms) value of the current that is flowing through the particular semiconductor device. For the SiC MOSFET, only the on-resistance $R_{DS(on)}$ is used to determine the conduction losses, i.e.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2 \quad . \tag{3}$$

From Fig. 6, the switching energies have a linear relationship with current and hence they can be modeled as

$$E_{on,S1,4} = a_{onS1,4} i_{out}(t) mod(t) + b_{onS1,4} \tag{4}$$
$$E_{off,S1,4} = a_{offS1,4} i_{out}(t) mod(t) + b_{offS1,4} \tag{5}$$

where $a_{on,off,S1,4}$ and $b_{on,off,S1,4}$ are the curve fitting constants obtained from Fig. 6. $i_{out}(t)$ is the load current (assumed to be pure sinusoidal with an electrical angular frequency ω and a phase shift of φ), i.e.

$$i_{out}(t) = \hat{I} sin(\omega t - \varphi) \tag{6}$$

and the modulation function $mod(t)$ is defined for a sinusoidal output in the usual way as

$$mod(t) = M sin(\omega t) \tag{7}$$

where M is the modulation index. The mean switching losses for S_1 and S_4 are then given by Eq. (8).

$$P_{sw,S1,4} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{T/2} (E_{on,S1,4} + E_{off,S1,4})\, dt \tag{8}$$

D. Consolidation of Device Losses into overall Semiconductor Losses

Using the concepts of Section A-C, a loss breakdown analysis for the T-Type inverter with various switching devices was developed using Eq. (1)-(7). For the inverter specifications shown in Table IV, the resulting loss distribution between the two semiconductor devices is shown in Fig. 7, and identifies that the use of SiC MOSFETs for the outer switches does significantly reduce both the conduction losses and the switching losses. For example, at a switching frequency of 16 kHz, which is commonly used in unity power factor grid-tie applications, the switching losses for the IGBT alternative are 7.4 W whereas the switching losses for the SiC MOSFET alternative are only 0.9 W. This gives a switching loss reduction of more than 85 % and a conduction loss reduction of almost 50 %. Total semiconductor losses are therefore 20.87 W for the IGBT based converter and 9.4 W for the SiC MOSFET based converter. The benefits of the SiC MOSFETs become even more obvious as the switching frequency increases, for example at a switching frequency of 32 kHz as shown in Fig. 7.

IV. Predicted Loss Model Validation by Thermal Measurements

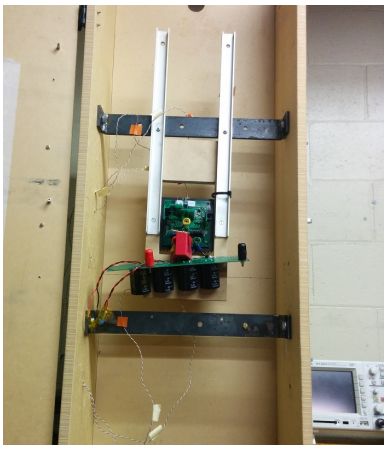
The predicted IGBT and SiC based T-Type inverter losses were then validated experimentally to confirm the modeling approach presented in Section III. This was done using thermal measurements taken from the (calibrated) heat sink used for the prototype shown in Fig. 4a to determine the overall experimental power stage losses, and then comparing this result with the predicted overall losses obtained by summing the individual device losses shown in Fig. 7.

A. Heat sink calibration

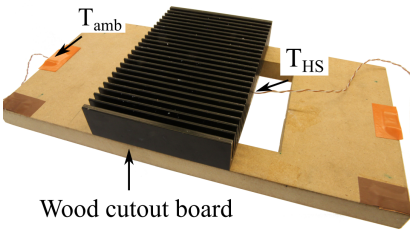
The semiconductor devices were mounted on a common heat sink. The converter and the heat sink were then placed

TABLE IV: Specifications

Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 µF
M	Modulation index	0.85

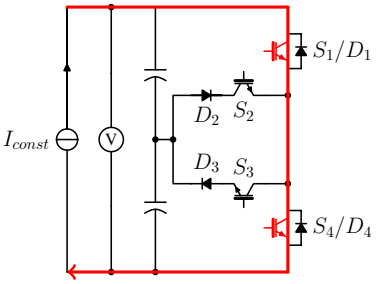


(a) Converter and heat sink in closet

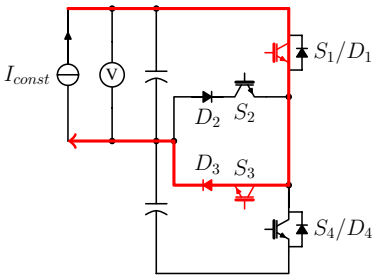


(b) Backside of the converter. Thermal measurements performed directly on the heat sink T_{HS} and below the heat sink T_{amb}

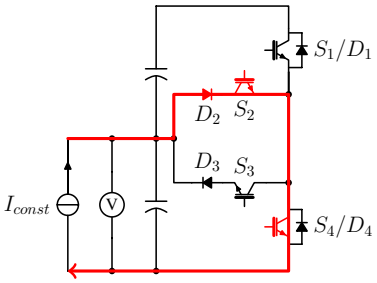
(c) Closed closet to avoid influences from the surroundings



(d) Switch pair 1: S_1 and S_4 conducting



(e) Switch pair 2: S_1 and S_3 and D_3 conducting



(f) Switch pair 3: D_2 and S_2 and S_4 conducting

Fig. 8: Closet (open ended chimney) for thermal measurements

inside an open-ended (timber) chimney to minimize the influence of transient air flow changes caused by external disturbances, as shown in Fig. 8a and Fig. 8c. Two thermocouples were used to measure the heat sink temperature T_{HS} and the ambient temperature T_{amb}, placed as shown in Fig. 8b. The relative temperature difference between the input ambient temperature and the heat sink temperature was then obtained using

$$\Delta T = T_{HS} - T_{amb} \quad . \tag{9}$$

To avoid any substantial thermal influence from the gate driver circuit and the DC link capacitors (or more accurately their balancing resistors which are connected in parallel with the capacitors), the heat sink was thermally decoupled from this circuitry using a wood cutout board as shown in Fig. 8b. The heat sink was calibrated by passing a known DC current through three different pairs of semiconductors as shown in Fig. 8, and measuring the overall voltage drop across these devices. The product of these DC voltages and currents is the steady state thermal energy that was injected into the heat sink to cause the measured temperature rise. This procedure was repeated for the three different switching pairs shown in Fig. 8d-Fig. 8f, with the results shown in Fig. 9a. The test outcomes for the different switching pairs at a particular power level was averaged and the procedure repeated for different

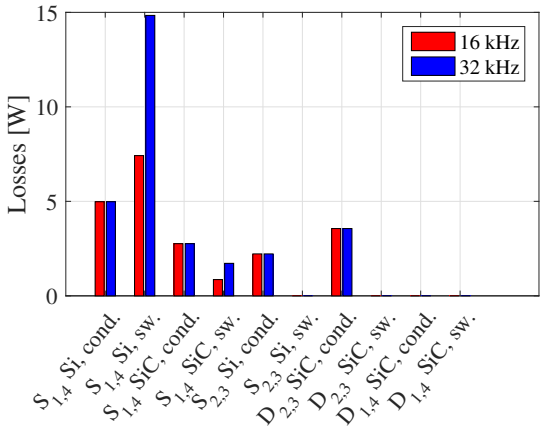
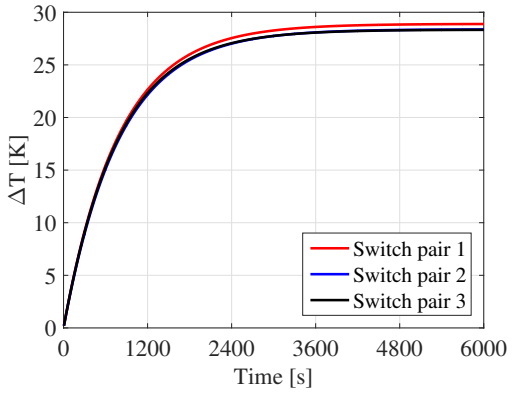
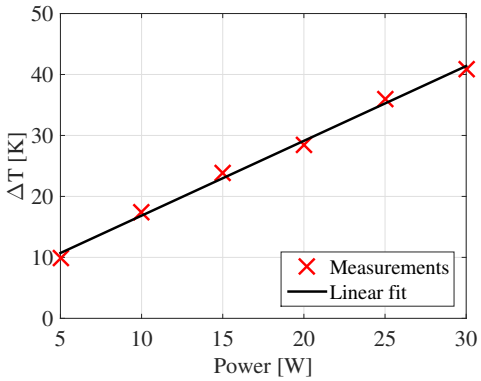


Fig. 7: Loss breakdown analysis for an output power of 1.5 kW, unity power factor and two different switching frequencies

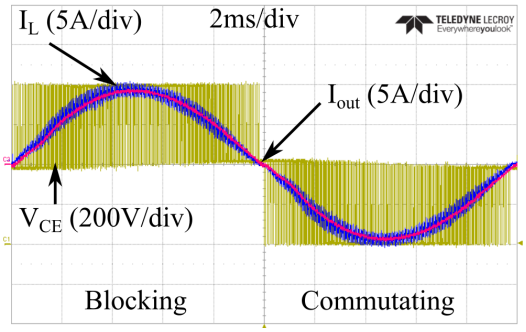


(a) Relative temperature rise versus time for different switch pairs

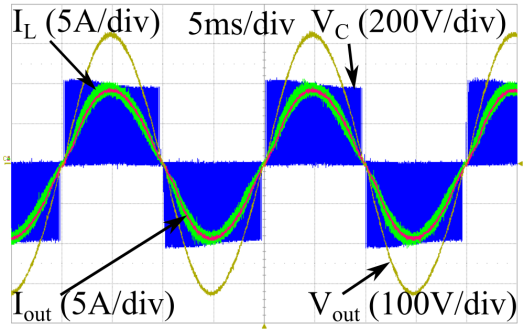


(b) Averaged heat sink calibration curve

Fig. 9: Calibrated heat sink temperature rise versus time for different conducting semiconductor pairs



(a) Collector-Emitter voltage of S_4 during inverter operation



(b) Experimental waveforms for $P_{out} = 1.5\,\text{kW}$, $\hat{V}_{out} = 325\,\text{V}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor

Fig. 10: T-Type inverter experimental waveforms

power levels to obtain the resultant (essentially linear) heat sink calibration curve shown in Fig. 9b, which directly relates heat sink temperature rise to overall power stage device losses.

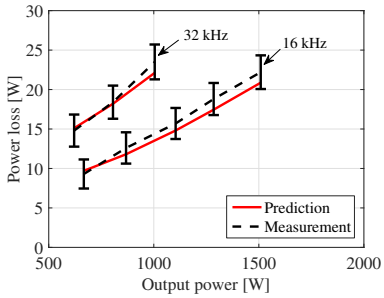
B. Experimental results and discussion

Using the calibrated heat sink, the inverter as specified in Table IV was operated using PD PWM according to Fig. 1b. Experimental waveforms of the converter inductor current $i_L(t)$, the load current $i_{out}(t)$ and the collector-emitter voltage V_{CE} of S_4 operating at 1.5 kW and 16 kHz are shown in Fig. 10a, detailing in particular how switch S_4 commutates with $V_{DC}/2$ when the output current is negative, but must block the full DC link voltage (i.e. 800 V) when the output current is positive. The total power stage semiconductor losses at any particular operating point were then determined by measuring the steady state heat sink temperature rise using Eq. (9), and translating this back to injected thermal power using Fig. 9b. Note that care must be taken with this approach to ensure that the heat sink reaches a steady state temperature rise before each measurement is taken - for the experimental system used in this paper, approximately 60 minutes of operation were required at each operating condition before measuring the heat sink temperature rise. Working on the basis that the heat sink temperature rise is essentially caused only by power stage semiconductor power losses, this temperature rise measurement then identifies the total semiconductor operating losses of the T-Type inverter at any particular operating point.

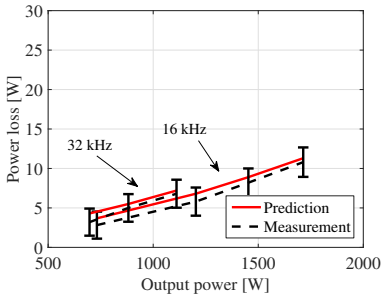
Using this approach, the inverter was operated for a variety of different switching frequencies and power levels. Fig. 11a and Fig. 11b show the resultant match between the measured semiconductor losses and the predicted losses for the inverter operating with either IGBT or SiC MOSFET switches connecting to the outer DC link buses, where it can be seen that the match between the semiconductor loss predictions and the measured results is well within the measurement bounds of the experimental thermal measurement technique. Figure 11c shows the resultant comparison between the two alternatives. Hence the analytical prediction model developed in Section III can be used with confidence across a wide range of operating conditions.

V. Potential Benefits of SiC MOSFETs in T-Type Inverter

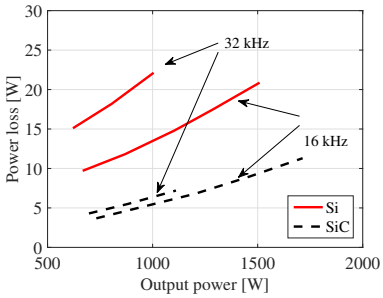
The potential benefits of replacing the outer switches of a T-Type inverter with SiC MOSFETs can clearly be seen from Fig. 11c, which shows that when using SiC MOSFETs, the overall semiconductor losses can be decreased by more than



(a) Si IGBT based inverter

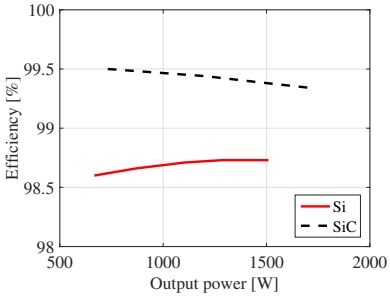


(b) SiC MOSFET based inverter

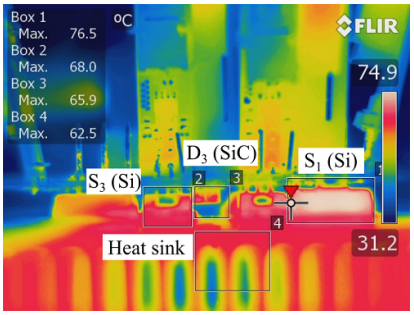


(c) Semiconductor losses for Si and SiC in T-Type inverter at two different switching frequencies

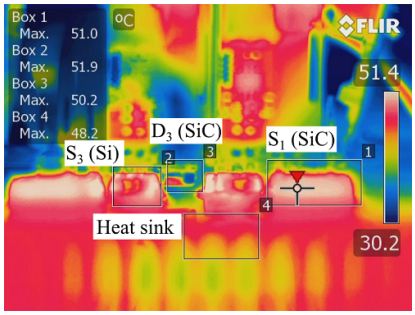
Fig. 11: Semiconductor losses for Si and SiC switches in the T-Type inverter



(a) Improved semiconductor efficiency (16 kHz)



(b) Case temperatures for Si based inverter, $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor



(c) Case temperatures for SiC based inverter, $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor

Fig. 12: Improved efficiency and reduced device case temperatures with SiC device substitution

50 % at a switching frequency of 16 kHz, and considerably more as the switching frequency increases to 32 kHz. From these results, three options for re-designing a T-Type inverter using SiC switching devices in this way can be considered

1) For a given inverter, retain its electrical design and use the increased overall efficiency to reduce the heat sink requirement;
2) Increase the power rating of the inverter for the same heat sink design in order to increase its power density;
3) Increase the inverter switching frequency, with a consequential reduction in filter component sizes.

A. *Efficiency improvements*

Semiconductor losses directly influence overall inverter efficiency across the entire operating range of the inverter. As identified in Section III, the SiC MOSFET has a resistive output behavior and hence a low voltage drop at low currents (light load) which leads to small conduction losses under these conditions. In contrast, an IGBT has a bipolar output characteristic and hence a rather constant voltage drop at low currents. Hence just replacing S_1 and S_4 with SiC devices instead of IGBT devices will reduce the overall semiconductor losses as shown in Fig. 11, and consequently improve inverter efficiency (particularly under light load conditions). Neglecting passive component losses (which will remain essentially unchanged for either switching device), Fig. 12a shows this improved inverter efficiency at a switching frequency of 16 kHz as the output power varies, with a nearly 1 % improvement achieved when using the SiC devices at light loads. Figs 12b and 12c show the corresponding reduction in device case and heat sink temperature that is achieved when using SiC devices with the same heat sink design.

B. *Power rating improvements*

From Fig. 11c it can be proposed that the loss reduction benefits of using SiC devices could be used to increase the power rating of a given inverter, by increasing the available output power for the same cooling effort. Fig. 13 illustrates this potential by identifying that the output power can be increased from 1.5 kW using Si devices, up to 2500 W using SiC devices, for the same total semiconductor losses at a switching frequency of 16 kHz. For the particular inverter

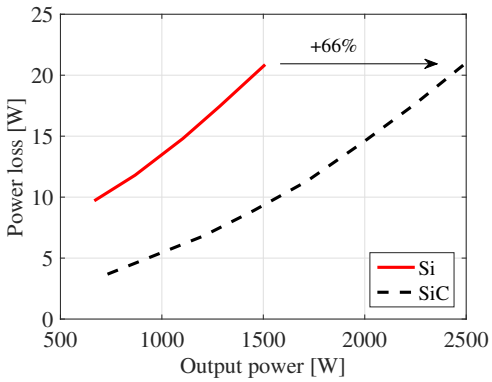


Fig. 13: Increased output power with SiC devices for the same semiconductor losses

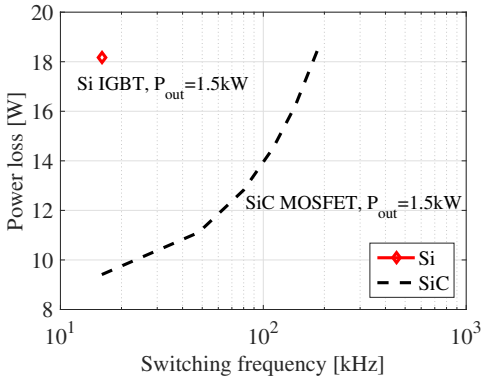


Fig. 14: Increased switching frequency with SiC devices for the same semiconductor losses

system investigated in this paper, this achieves an inverter power rating increase of more than 60 %.

C. Increased switching frequencies

Finally, using the semiconductor loss modeling concepts presented in this paper, the inverter switching frequency when using SiC devices has been increased until the SiC semiconductor losses are the same as the Si semiconductor losses. The results are shown in Fig. 14, and show that for an output power of 1.5 kW, the switching frequency can be increased up to 192 kHz before this balance point is reached. This represents a 12 fold increase in switching frequency for the same losses.

VI. Conclusion

This paper has presented the results of an investigation into the benefits of using SiC MOSFETs in a three-level T-Type inverter. The paper develops an analytic loss model based on conduction losses derived from device datasheets, and switching losses based on experimentally measured switching transitions to take into account the unusual switching characteristic of a T-Type inverter, which is that the outer devices switch at a voltage which is only half of their required voltage blocking capacity. The loss model has been verified using thermal measurements taken from an experimentally calibrated heat sink at different power levels and switching frequencies for both Si and SiC based inverters. The results of the investigation identify that the major benefit when operating at or near unity power factor is achieved by replacing Si with SiC devices for only the two outer switches that connect the AC output to the positive and negative DC bus rails. With this substitution, the use of SiC MOSFETs can reduce the semiconductor losses by more than 50 % for similar rated devices operating under the same load conditions and switching frequency. Such a loss reduction gain offers several design opportunities. Firstly, if the inverter design specifications are kept the same, the reduced semiconductor losses can increase the overall inverter efficiency by up to 1 %. Alternatively, if the switching frequency is kept the same as for an IGBT based inverter, the output power can be increased by up to 66 % for the same semiconductor losses. Finally, taking advantage of the superior switching characteristics of the SiC MOSFETs, the switching frequency can be increased by a factor of 12 while still achieving the same semiconductor losses as for an IGBT based inverter.

Of course it must be kept in mind that that the analysis presented here has only considered semiconductor losses for similarly rated devices, and there are many other factors such as device costs, passive filter components and packaging that must be taken into account when designing a complete inverter system. Nevertheless, the substantial loss benefits offered by the simple substitution of only two active switches per phase leg for the T-Type converter, and the relatively low cost implication of this substitution compared to the overall inverter cost, make it an attractive alternative to consider for this inverter topology.

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Appendix J

Analysis and Comparison of Si and SiC Power Devices on a Grid-Tie Fuel Cell Energy Storage System

2014 International Electronics and Application Conference and Exposition (PEAC), Nov 2014, pp. 296-301

Analysis and Comparison of Si and SiC Power Devices on a Grid-Tie Fuel Cell Energy Storage System

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***Abstract*—In renewable energy applications power conversion efficiency is major concern. This is especially true for grid-tie energy storage systems based on bidirectional dc-dc and dc-ac converters where power flows through these system components. Latest developments in power semiconductors technology significantly reduced switching and conduction losses in dc-dc and dc-ac converters allowing efficiencies above 98%. This paper analyzes the efficiency improvement that is achieved by the introduction of SiC power semiconductors in dc-dc and dc-ac converters. The analysis is focuses on fuel cell grid-tie energy storage systems. Results highlight dc-dc conversion efficiencies up to 98.2% with an isolated topology and dc-ac conversion efficiencies up to 97.7%. Overall system efficiency improvements above 1% are achieved compared to traditional Si devices. Results on efficiency improvement are analyzed based on two laboratory converter prototypes of an isolated full bridge boost converter (IFBBC) and a three level T-type inverter (BSNPC).**

Keywords*—Silicon carbide (SiC); energy storage, power semiconductors, dc-dc converter, dc-ac converter.

I. Introduction

Energy produced from renewable energy sources is fluctuating depending on the availability of the energy source [1]. For this reason, grid-tie energy storage systems are expected to play an important role in the future energy systems. Different energy storage technologies are nowadays available, such as pumped hydro, compressed air systems, battery systems and other chemical-based processes. In these applications, bidirectional fuel cells represent a very attractive technology since they allow storing energy in a fuel form (high energy density) [2]. For all energy storage systems efficiency is an important aspect in power conversion especially in dc-dc converters and dc-ac inverters in which power semiconductor devices are key components. Apart from different converter topologies, loss contributions are mainly determined by the choice of the power semiconductors. One way to increase efficiency in converters with voltage levels in the 600 V-1200 V range is to replace commonly used silicon (Si) devices with silicon carbide (SiC) devices [3].

The introduction of SiC Schottky diodes represented a first breakthrough for SiC technology. Even though SiC Schottky diodes are significantly more expensive compared to their equivalent Si devices, they have been widely employed in multi-kW power converters due to their nearly-zero reverse recovery current. Since then, SiC power semiconductors have become more attractive, more mature and more accessible. SiC MOSFETs have extremely low switching losses [4] compared to Si IGBTs which, whether possible, makes SiC MOSFETs the preferred power semiconductors over Si IGBTs. Their performance has been evaluated in previous work [5][6] however, it is always challenging to quantify the real expected efficiency increase without proper full power converter prototypes.

This paper presents the results achieved with dc-dc and dc-ac converters designed for an energy storage system based on bidirectional fuel cells. The designed converters have been characterized in efficiency terms with both Si IGBTs and SiC MOSFETs power semiconductors. Efficiencies achieved with the converter prototypes are presented and analyzed taking into account the entire system efficiency. Efficiency improvements up to 1% are achieved for the entire operating range of the system. While for the single converters, efficiencies improvements up to 1%-3% range were observed depending on the converter operating point.

II. Energy Storage System Based on Bidirectional Fuel Cells

Grid-tie energy storage systems require power conditioning units (both dc-dc and dc-ac) to process the energy to and from the grid. System topology is strongly influenced by the maturity of the candidate fuel cell technology and by the economic feasibility of the system. The fuel cell technology determines also the power conditioning unit operating conditions (I-V characteristics [7] for the dc-dc converters in Fig. 1a and 1b). The system topology and the dc-dc /dc-ac converters efficiency will strongly affect the overall system performance, since both in power generation mode and power regeneration mode energy flows through the power conditioning units. In order to ensure long term system reliability and high efficiency, it is desired to operate the cells stacks in optimal conditions in terms of cells current density, temperature and fuel distribution. Therefore, a dc-dc converter is required for each cells stack. The system in Fig. 1a has a single dc-ac inverter unit which minimized the system complexity and cost. However, at light systems loads the overall system efficiency is limited by the light load efficiency of the inverter unit. The system in Fig. 1b can provide higher efficiency especially

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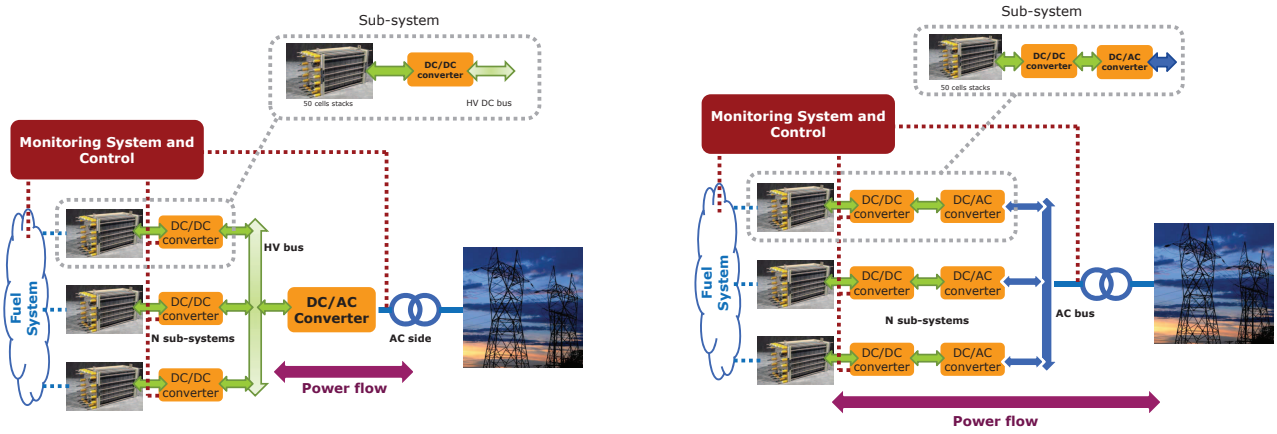


(a) Centralized DC/AC converter

(b) Distributed DC/AC converter

Fig. 1: SOEC/SOFC system topologies.

at light loads. In fact, light load efficiency of a large dc-ac converter is typically lower than the efficiency of a small inverter unit operating in mid or high load conditions.

The analysis of the overall system efficiency is based on Fig. 1b system topology where a single sub-system is considered. The I-V characteristics of a 50-cells stack of bidirectional fuel cells is summarized in Table I. Multi-kW dc-dc and dc-ac converter prototypes have been established according to the characteristics of cells stack of solid oxide fuel cells /electrolyzer cells (SOFC /SOEC). The cells stack electric specifications determine the dc-dc converter characteristics, while the dc-ac inverter characteristics are determined by the grid specifications.

III. Si and SiC Power Devices

The introduction of SiC power semiconductors in dc-dc and dc-ac converters significantly increases the cost of the converter power devices. This increase has to be justified by an efficiency improvement or by a cost reduction of other converter components, such as magnetic and capacitive components.

The investigation performed on Si IGBTs (IGW15N120H3 and IKW12N120T2) and SiC MOSFETs (Cree C2M0080120D and ST SCT30N120) considered both conduction and switching losses. Switching losses are the most challenging to model and to estimate, therefore, switching measurements based on double pulse tests (DPTs) have been performed. Switching waveforms for SiC MOSFET at 800 V and 20 A are presented in Fig. 2a for device turn-on and in Fig. 2b for device turn-off. Even though of the highly optimized layout, the devices have a strong tendency to gate oscillations due to extremely high *dV/dt* and large package stray inductances (TO-247). A complete view of the reduction of switching losses achieved with SiC devices is shown in Fig. 3a. The largest reduction of switching losses is achieved at high current levels; in this case, the reduction can reach up to ∼80%. This is explained by analyzing the switching losses: even though the latest generations of Si IGBTs can operate with switching frequencies up to 100 kHz, the tail current gives a large contribute in the turn-off switching losses.

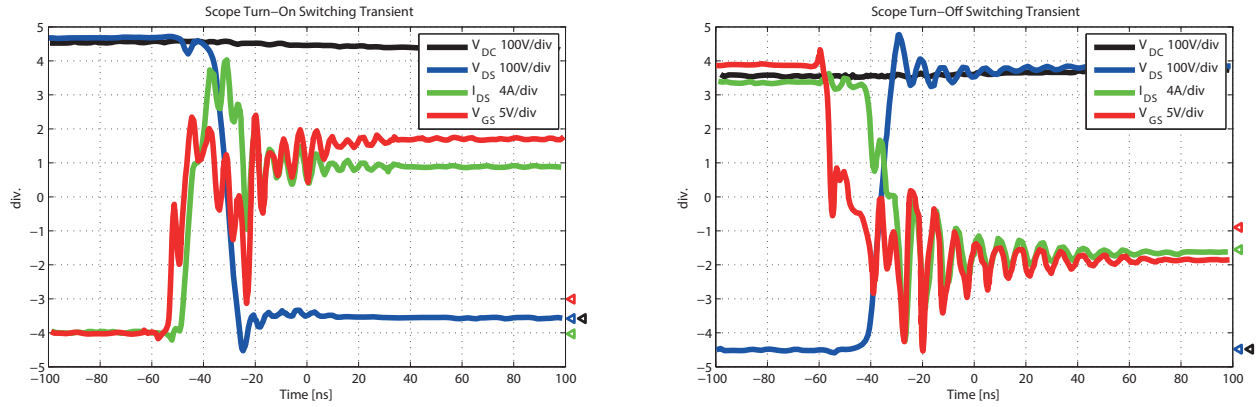
TABLE I: SOEC/SOFC cells and converter specifications

Specification	SOEC	SOFC	Converter
Voltage LV-side	50-80 V	30-50 V	30-80 V
Current LV-side	0-80 A	0-40 A	0-80 A
Power	0-6000 W	0-1500 W	0-6400 W
Power flow	⇐ from the grid	⇒ to the grid	⇔ bidirectional

For both Si IGBTs and SiC MOSFETs the conduction losses can easily be characterized with information retrieved from the devices datasheets. The reduction of conduction losses achieved with SiC MOSFETs (C2M0080120D) over Si IGBTs (IGW15N120H3) is represented by the device forward voltage drop show in Fig. 3b. In this case the largest reduction is observed at low current levels where the IGBT forward voltage drops dominates. As the current increases the difference is progressively reduced by the higher on-state resistance of SiC MOSFETs compared to IGBTs. The gap between IGBTs and SiC MOSFETs is also reduced at high junction temperatures. In this case for both devices the on-state resistance increases however, for the IGBTs this is compensated also by the lower threshold voltage V_{T0} (bipolar behavior).

IV. DC-DC Power Converter

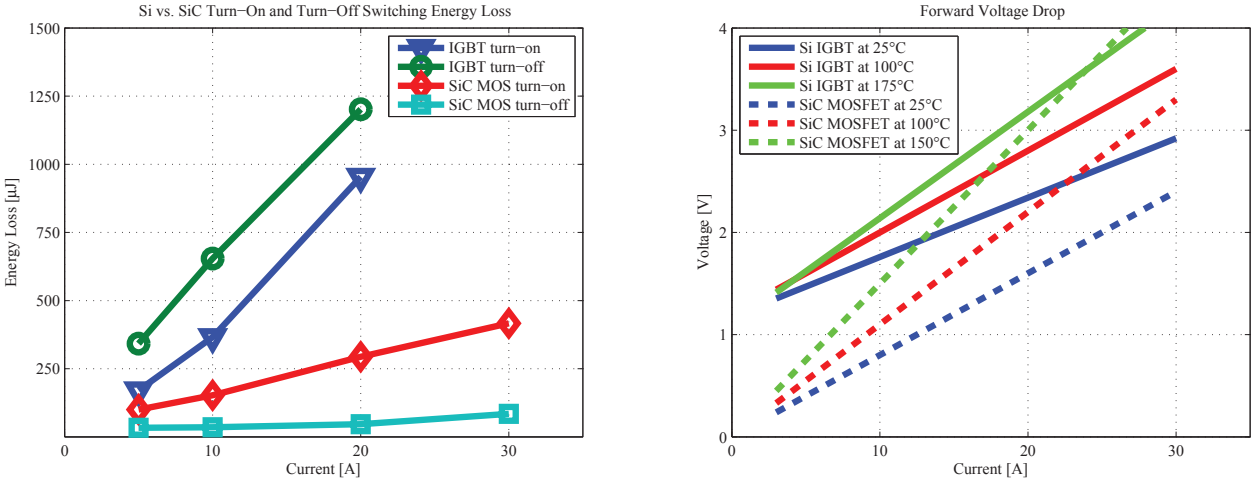
The dc-dc converter in the system in Fig. 1a and 1b is designed based on an isolated full bridge boost converter (IFBBC) topology [8]. The converter prototype is shown



(a) Turn-on

(b) Turn-off

Fig. 2: SiC MOSFET switching transients.



(a) Switching losses

(b) Conduction losses - Forward voltage drop

Fig. 3: Si IGBTs and SiC MOSFETs loss comparison

in Fig. 4 where its main components are highlighted. The converter low-voltage side (30-80 V) power stage is based on Si MOSFETs (120 V $4.1\,m\Omega$ two devices in parallel for each switch of the full bridge) and is connected to the cells stack. The converter high voltage side (700-800 V) represents the dc-link bus for the dc-ac converter. The full bridge of the high voltage side of the dc-dc converter has been tested with Si IGBTs (IGW15N120H3) and with SiC MOSFETs (ST microelectronics SCT30N120 which are equivalent to Cree C2M0080120D). The dc-dc converter magnetic components are designed based on high current planar cores for an operating switching frequency of 40 kHz. The transformer cores are two E64 pairs in Magnetics R-type material while the boost inductor uses three E6030 stacked core pairs in KoolMu material. The test setup for measuring the system efficiency is based on four $6\frac{1}{2}$ high precision multimeters synchronized and connected with a PC. Two multimeters measured the LV-side and the HV-side voltages while the other two measured the converter currents through calibrated precision shunt resistors. The absolute error on the measured efficiency is less than 0.1%.

The absolute dc-dc conversion efficiency of the converter based on SiC MOSFETs for both power flow directions is presented in Fig. 5a. In this case, the efficiency takes into account also the gate driver and the cooling losses. With SiC MOSFETs the dc-dc converter was just above 96% at 30 V on the converter LV-side and reached a peak of 98.2% at 80 V. Converter efficiency based on SiC MOSFETs is compared with the first converter prototype based on Si IGBTs in Fig. 5b.

The efficiency improvement is presented at 30 V, 50 V and 80 V, but it has been investigated for the entire converter operating range (30-80 V). A limited improvement is observed

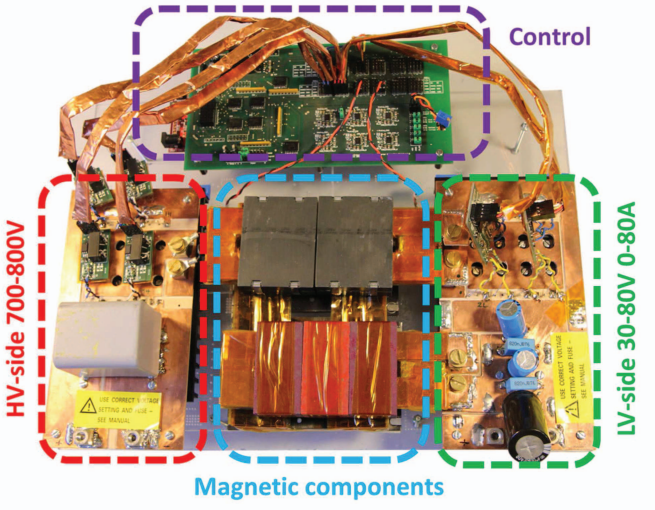


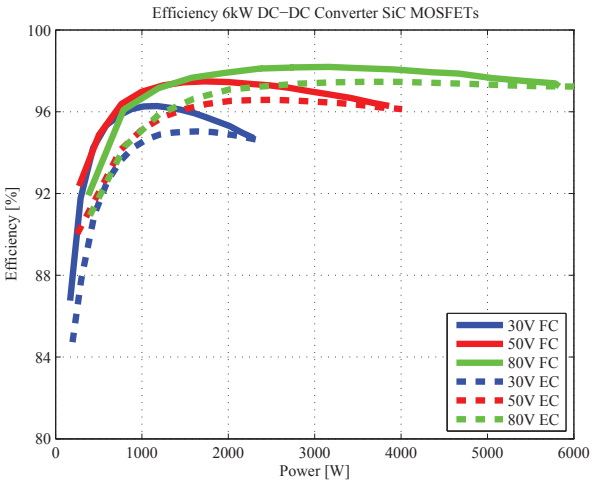
Fig. 4: 6 kW bidirectional isolated full bridge boost dc-dc converter. Highlighted its main components: low voltage side (LV-side), high voltage side (HV-side), control board, boost inductor and high frequency isolation transformer (magnetic components).

in fuel cell mode (FC-mode) in Fig. 5b (continuous lines). In this mode, the SiC MOSFETs are operating in active rectification; the efficiency improvement (monotonic function trend) is mostly noticeable at light converter loads and it slowly decreases at high power levels. At light loads, IGBTs antiparallel diodes have significant losses due to the forward voltage drop while SiC MOSFETs have only resistive voltage drop. For this reason, higher efficiency improvements are observed at converter light load. Large efficiency improvement is observed in electrolyzer cell mode (EC-mode) in Fig. 5b (dashed lines). In EC mode, the high voltage power semiconductors are operating in hard switching conditions, therefore, the major improvement is given by the large difference in switching losses between the IGBTs and SiC MOSFETs switching losses [9]. The efficiency improvement is in the 1-3% range (dashed lines in Fig. 5b) with a peak at converter light load.

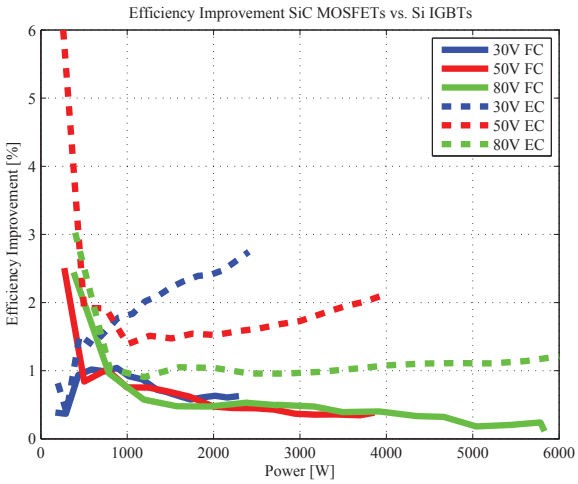
V. Dc-ac Power Converter

The dc-ac converter is the second power stage in the conversion process. The dc-ac converter is designed as a 3 kW single phase low-power variant, the dc-link is specified as 700-800 V to comply a 230 V_{RMS} grid with a fundamental frequency of 50 Hz. Several different inverter topologies could be considered however, for low voltage grid, two- and three-level topologies are the most common ones due to their good trade-off between cost, complexity and efficiency. Multi-level topologies are mostly interesting because it is possible to reduce the size of filtering components [10].

A converter prototype of a 3 kW single phase T-type inverter [11] (also known as Conergy or BSNPC) has been developed and tested [12], the prototype is shown in Fig. 6. The T-type inverter is a three level topology derived from the neutral point clamped (NPC) topology. The topology has the middle branch switches connected to the mid-point of the dc-link and they operate at the same frequency as the grid (50 Hz). For this horizontal branch, the conduction losses are dominating and the switching losses can be neglected. Devices employed in this branch are Si IGBTs (IKP15N60T) rated at 600 V. The vertical branch of the T-type single phase inverter has been tested with both Si 1200 V (IKW15N120T2) and with SiC MOSFETs (C2M0080120D). These are the high frequency devices of the dc-ac inverter, in this case the switching frequencies have been 16 kHz and 30 kHz for Si IGBTs and



(a) Measured dc-dc converter efficiency with SiC MOSFETs, bidirectional power flow



(b) Dc-dc converter efficiency improvement

Fig. 5: Dc-dc converter efficiencies measured with Si IGBTs and with SiC MOSFETs.

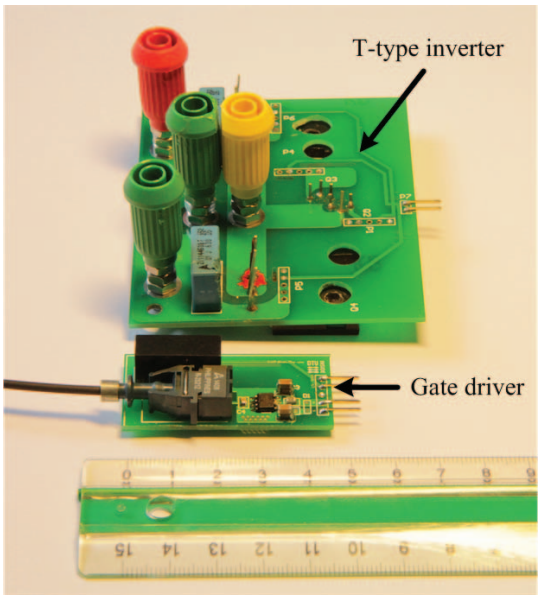


Fig. 6: 3 kW dc-ac inverter based on T-type (BSNPC) topology [11]. Heatsink is removed.

up to 60 kHz for SiC MOSFETs. In this case, to measure the efficiency of the dc-ac converter a N4L PPA5500 power analyzer was used. The instrument has a basic accuracy of 0.01% and can measure harmonics up to 2 MHz.

Dc-ac conversion efficiencies are measured up to the nominal converter power with an LC output filter (3 mH, 4.4 µF). Results from the measurements are presented in Fig. 7 at different switching frequencies for both Si IGBTs and SiC MOSFETs. An overall, the adoption of SiC MOSFETs can provide an efficiency improvement of ∼0.8% for a major part of the converter operating range. This results that at 30 kHz at full converter power (3 kW) the total power semiconductor losses (conduction and switching) of the vertical leg are reduced by 72% and of the total converter power semiconductor losses by 70%. This efficiency improvement is mostly due to the reduction in switching losses rather than conduction losses [12]. This also allows reducing the size of the converter cooling system by a similar amount. From Fig. 7 it is also observed that with SiC MOSFETs it is possible to almost double the converter switching frequency and achieve a similar efficiency as achieved with Si IGBTs. This results that the size of the converter filtering components can be reduced.

VI. System Efficiency

The overall system efficiency is determined by the series efficiency of the dc-dc and dc-ac converter stages. From the system operating point, the fuel cell mode represents the most critical. In fact, in this mode the system provides power to the grid and the fuel cell efficiency is limited to ∼50%. The remaining power from the fuel cell is dissipated as heat (used for distributed heating). Moreover, in this operating mode, the maximum cells stack current is limited to ∼40 A to limit the cells degradation (as presented in Table I).

The fuel cell operating mode limits are 30-50 V on the low voltage side of the dc-dc converter. The total dc-ac system efficiency of the two stages presented in Fig. 8. The system efficiency improvement given by the introduction of SiC MOSFETs as replacement of Si IGBTs is above 1% for the entire range in Fig. 8. At 1.5 kW the efficiency gain is ∼1.5% and at light load reaches a peak of 3% at 50 V. At converter light load the gain is more pronounced this is due to the large reduction of switching losses and forward voltage drop (conduction losses) achieved with SiC MOSFETs. However, in light load conditions efficiency is also strongly influenced by the losses in the magnetic components (e.g. high frequency transformer

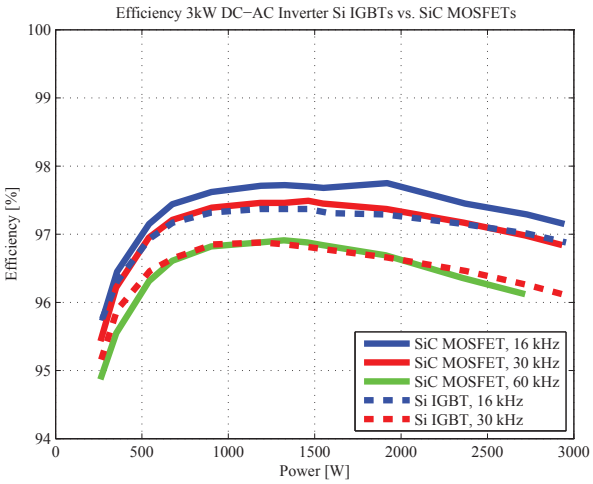


Fig. 7: Measured dc-ac converter efficiency comparison with Si IGBTs (dashed lines) and SiC MOSFETs (continuous lines) at 30 kHz and 60 kHz.

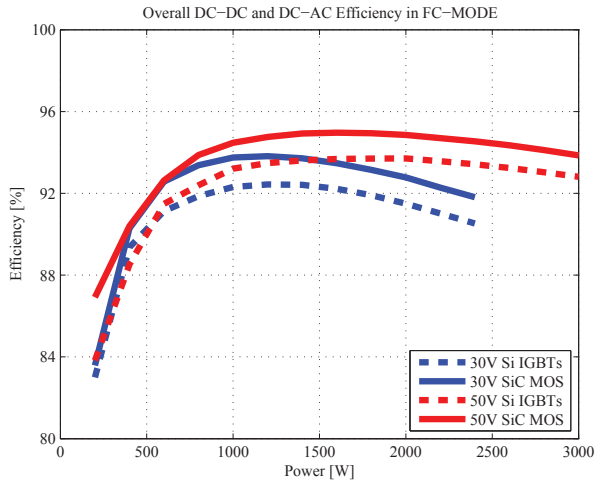


Fig. 8: Comparison of the total system efficiency with Si IGBTs and SiC MOSFETs when the system power flows from the fuel cells stack to the grid.

in the dc-dc stage and filtering components in the dc-ac stage) which are not affected by the power semiconductor type. This efficiency improvement can be used to estimate the economic gain given by SiC power semiconductors. It should be also considered that the cost reduction in size terms of passive components and raw materials is a major advantage.

VII. Conclusion

In this paper, efficiency investigations on a grid-tie energy storage system for bidirectional fuel cells have been conducted. Efficiency improvements for both the dc-dc and the dc-ac power stages are investigated when the 1200 V Si IGBTs are replaced by SiC MOSFETs.

In fuel cell mode (SiC MOSFETs operating in active rectification mode), the dc-dc converter maximum efficiency improvement of 2.5% is achieved, this is due to the rather large forward voltage drop of the SiC antiparallel diodes. In electrolysis cell-mode (SiC MOSFETs in hard switching conditions), maximum efficiency improvements of 3% are achieved thanks to the significant reduction of the switching losses of SiC MOSFETs compared to Si IGBTs. On overall, the dc-dc converter with SiC MOSFETs was capable of achieving a absolute maximum efficiency of 98.2% in fuel cell mode. The dc-ac converter based on a T-type topology achieved a maximum efficiency 97.7% with SiC MOSFETs. Compared to Si IGBTs this has been an efficiency improvement of $\sim$0.8% over almost the entire converter operating range, this also allows to significantly reduce the size of the converter cooling system (easily up to 50%). It is also observed that SiC MOSFETs can be used to double the switching frequency of the dc-ac converter and, therefore, reduce the size and cost of the filtering components.

On a system point of view, the introduction of SiC MOSFETs allowed to increase the overall system efficiency of $\sim$1% over the entire power range in fuel cell mode with peaks up to 1.5-3% depending on the converter operating point.

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Appendix K

Comparative Evaluation of the Loss and Thermal Performance of Advanced Three Level Inverter Topologies

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Applied Power Electronics Conference and Exposition (APEC), March 2016, accepted

Comparative Evaluation of the Loss and Thermal Performance of Advanced Three Level Inverter Topologies

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***Abstract*—This paper presents a comparative evaluation of the loss and thermal performance of two advanced three-level inverter topologies, namely the SiC based T-Type and the Hybrid-NPC, both of which are aimed at reducing the high switching losses associated with a conventional Si based T-Type inverter. The first solution directly replaces the 1200 V primary Si IGBT switches with lower loss 1200 V SiC MOSFETs. The second solution strategically adds 600 V CoolMos FET devices to the conventional Si T-Type inverter to reduce the primary commutation losses. Semiconductor loss models, experimentally verified on calibrated heat sinks, are used to show that both variations can significantly reduce the semiconductor losses compared to the Si based T-Type inverter. The results show that both alternatives are attractive if high efficiencies and reduced thermal stress are major requirements for the converter design.**

***Index Terms*—T-Type, Hybrid-NPC, SiC MOSFET, Si IGBT, CoolMos**

I. Introduction

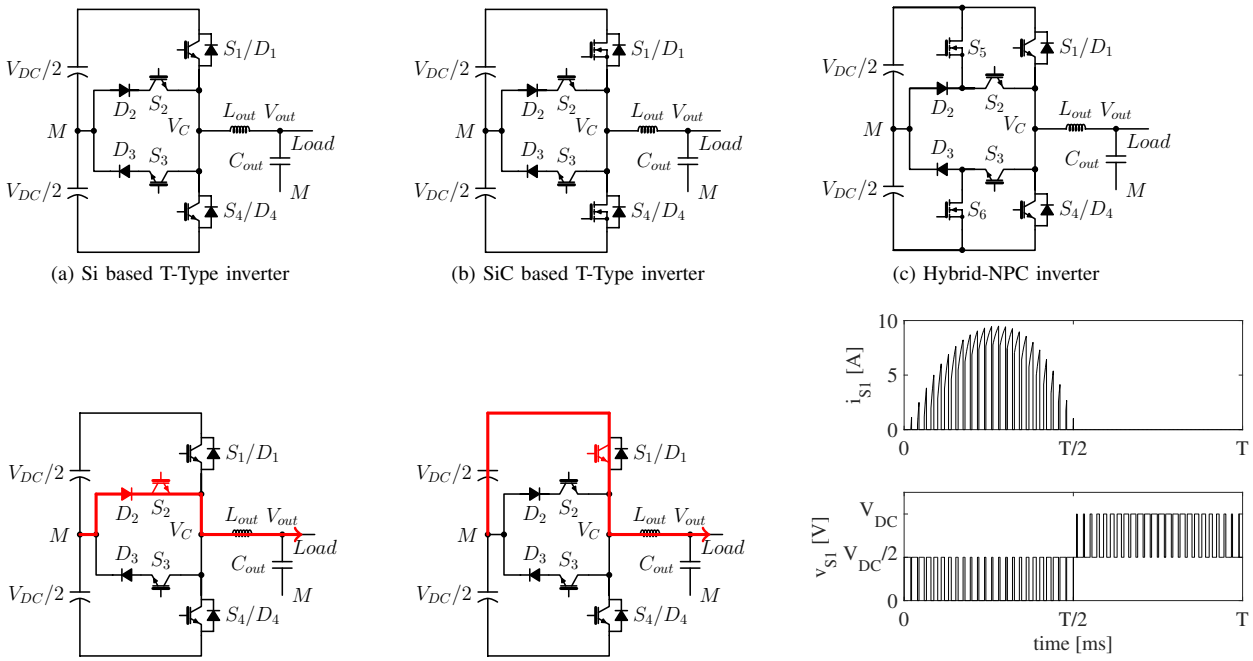
Transformerless photovoltaic (PV) systems are becoming favored in the residential sector due to their reduced size, cost and higher efficiencies compared to transformer based alternatives [1]. To further improve low cost PV systems, previous research has intensively investigated the trade-offs between two- and three-level inverters and has found that three-level inverters have lower total semiconductor losses as the switching frequency increases, and also allow a significant size reduction in the AC filter [2], [3]. Within the three-level inverter alternatives, the Neutral-Point-Clamped (NPC) [4] and the T-Type [5] topologies are widely used, each with particular advantages and drawbacks. For example, since the NPC inverter can use semiconductor devices that need to block only half the DC link voltage, its switching losses are always lower at any given switching frequency compared to the T-Type inverter, whose outer switches must block the whole DC link voltage and hence incur higher switching losses. Nevertheless, the T-Type converter can still achieve lower total semiconductor losses compared to the NPC alternative due to its reduced conduction losses. Hence switching frequency is clearly a crucial parameter in this comparison [3]. Due to recent advances in new semiconductor devices such as silicon carbide (SiC), switching losses in a power converter can be significantly reduced compared to standard Si IGBT alternatives using these devices [6], [7]. However, while the benefits and potential of these devices have been well reported [8]–[12], they are not yet in commonplace usage within commercial converter systems.

A further way to reduce the high switching losses in the T-Type inverter is to strategically add lower voltage switching devices in addition to the conventional T-Type circuit in order to manage the primary commutation events. This approach, called a Hybrid-NPC inverter, has been found to achieve higher efficiencies compared to a conventional T-Type structure with higher voltage (1200 V) Si IGBTs [13]. But to date, only few references are available on this topology alternative [14], [15]. In particular a topological comparative evaluation of the loss and thermal performance between the Hybrid-NPC and the T-Type inverter using next generation switching devices such as SiC under exactly the same operating conditions is not known to the authors. This work therefore presents such a detailed loss comparison for these two advanced inverter alternatives, using semiconductor loss models based on datasheet information (to calculate conduction losses), switching transition measurements (to calculate switching losses) and verification of the loss models thermally on calibrated heat sinks.

II. T-Type and Hybrid-NPC Inverter

The three inverter alternatives considered in this paper are shown in Fig. 1, with the conventional Si based T-Type structure shown in Fig. 1a as a reference. Its operational principle is illustrated in Fig. 1d-Fig. 1e. Initially, as shown in Fig. 1d, when a zero output voltage is required with a positive output current, diode D_2 and switch S_2 conduct this load current and the blocking voltage across both S_1 and S_4 is $V_{DC}/2$.

Then, to achieve a positive output voltage, switch S_1 turns on with a commutation voltage of $V_{DC}/2$ and the



(a) Si based T-Type inverter (b) SiC based T-Type inverter (c) Hybrid-NPC inverter

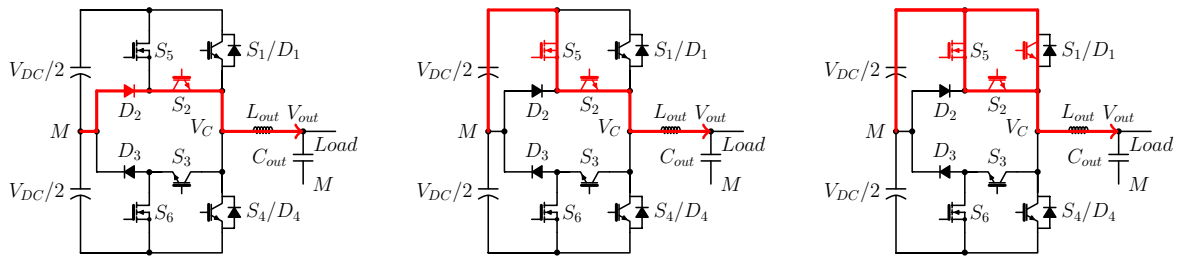
(d) Zero output voltage and positive output current (e) Positive output voltage and positive output current (f) Voltage across and current through S_1

Fig. 1. Inverter alternatives used in this study in (a) - (c), commutation from zero output voltage to positive output voltage in (d)-(e) and voltage and current through device S_1 in (f)

switching losses associated with this transition. Finally, a zero output voltage is re-established by turning switch S_1 off, with associated turn off losses for this transition. This process repeats throughout the positive fundamental half cycle as shown in Fig. 1f. Note that when the converter output voltage is switched to the positive DC rail, switch S_4 must block the whole DC link voltage, i.e. V_{DC}, which therefore requires S_4 to be rated to accommodate the full DC link voltage.

A similar process occurs for the negative fundamental half cycle, with diode D_3 and switch S_3 conducting current to achieve a zero output stage and switch S_4 turning on to achieve a negative converter output stage. Note that when the converter is switching during the negative half cycle, switch S_1 must now block the whole DC link voltage, as shown on the right half side of Fig. 1f. Since S_1 and S_4 need a higher voltage rating to block the whole DC link voltage, in contrast to the inner bi-directional devices D_2/D_3 and S_2/S_3, which need to block only half the DC link voltage, their switching losses are a major contributor to the overall semiconductor losses. Hence they can be directly replaced with SiC switching devices as shown in Fig. 1b to reduce these switching losses, with the inverter's topological structure and thus its modulation principles unchanged.

Alternatively, additional low voltage rated switching devices S_5 and S_6 can be added into the circuit, as shown in Fig. 1c, to make a Hybrid-NPC structure. The switching principle of this inverter is a little different as shown in Fig. 2, in that one of either S_5 or S_6 turn on first to create the positive or negative output voltage as required. Since these devices need only be



(a) Zero output voltage and positive output current (b) Positive output voltage and positive output current (c) Positive output voltage and positive output current

Fig. 2. Operation principle of Hybrid-NPC converter

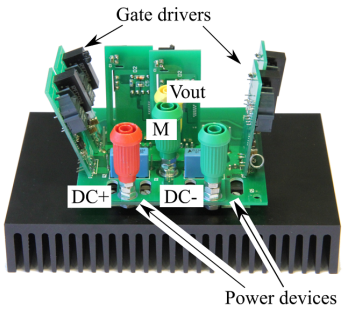
rated to half the DC link voltage, their switching losses will be less than for a conventional T-Type inverter (600 V CoolMos FET devices are used in this work to minimize these switching losses). Once the switching transition is complete, current flows through the two devices S_5 and S_2 as shown in Fig. 2b (for a positive output voltage and current), which increases their conduction losses to a level similar to a conventional NPC inverter. Switch S_1 is then turned on (with almost zero switching losses), and the current flow changes to share between the two conduction paths as shown in Fig. 2c to achieve a similar conduction loss as for a standard T-Type inverter (since the forward voltage drop across S_1 is much the same as before).

The turn-off sequence for the Hybrid-NPC is in the reverse order, i.e. S_1 first turns off with essentially zero switching losses, and then S_5 turns off with appropriate losses against a commutation voltage of $V_{DC}/2$.

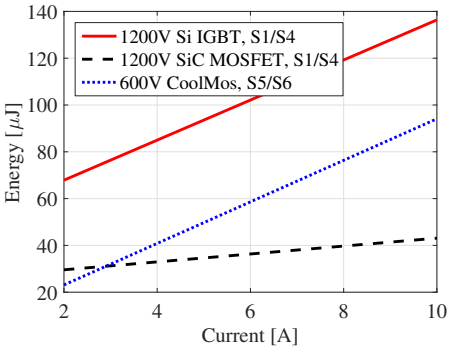
III. Semiconductor Device Selection

With the operation principles of the three inverter topologies identified, the selection of appropriate semiconductor devices for the topology comparison can now proceed. Since the targeted application for this topology is a grid-connected PV inverter system, the DC link voltage can go up to over 800 V. Thus a 1200 V rated device for S_1/S_4 is required. For this voltage range, the usual semiconductor device choice is Si IGBTs, which are known to have higher switching losses than either SiC or CoolMos devices, particularly because of their relatively large turn off energies caused by their long delay tail currents. Fig. 3b and Fig. 3c illustrate this difference, showing the turn on and turn off switching energies for a 1200 V Si IGBT (S_1/S_4 in Fig. 1a), a 1200 V SiC MOSFET (S_1/S_4 in Fig. 1b) and a 600 V CoolMos (S_5/S_6 in Fig. 1c) that were directly measured at appropriate voltages and currents for their T-Type inverter context, using the laboratory prototype shown in Fig. 3a. It can be seen from these results that while the 1200 V Si IGBT turn on energies are not so much larger than the CoolMos device, both the CoolMos FET and the SiC MOSFET show a superior turn off switching loss behavior. This is a particularly interesting observation since the turn off energies have been found to be the limiting factor for high efficient high switching frequency operation of the T-Type inverter [16]. Note also that since PV inverters operate mainly at unity power factor [17], the inner bi-directional device (S_2/S_3 in all topologies) switching losses will be essentially negligible and are therefore not included in this switching energy comparison.

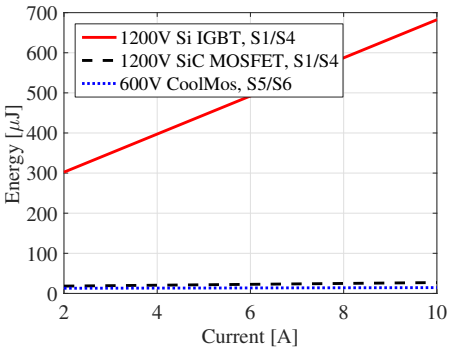
To complete the switching device loss comparison, their forward conduction voltages can be taken from the manufacturer's datasheets. The results are presented in Fig. 4, and show that the SiC MOSFET as a direct replacement to the 1200 V Si IGBT can also greatly reduce conduction losses over the current range of interest. Particularly at low currents, the SiC MOSFET shows a large voltage drop reduction due to its low on-state resistance, while the Si IGBT has a bipolar output characteristic and therefore a more constant and larger voltage



(a) Laboratory prototype



(b) Turn on energies



(c) Turn off energies

Fig. 3. Laboratory prototype and measured switching energies

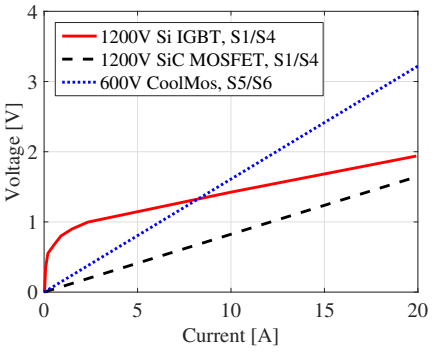


Fig. 4. Forward voltages of the primary devices

drop. Fig. 4 also shows that the 600 V CoolMos device has a relatively large forward voltage compared to the SiC MOSFET due to its Si based semiconductor substrate. Table I lists all semiconductor devices used in this comparison evaluation.

IV. Loss breakdown analysis

Once the device forward conduction and switching losses have been characterized, a loss breakdown analysis for their operation in the T-Type and Hybrid-NPC converter structures can be conducted. The IGBT conduction loss model is obtained using its dynamic on-resistance r_{on} and zero on-state voltage V_0, i.e.

$$P_{con,IGBT} = V_0 I_{AV} + r_{on} I_{rms}^2 \quad , \tag{1}$$

where I_{AV} and I_{rms} are the average and root-mean-square currents through the device. For the SiC MOSFET and the CoolMos FET, only their on resistance $R_{DS(on)}$ is needed to determine conduction losses, i.e.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2 \quad . \tag{2}$$

The conduction losses for the diodes are based on their threshold voltage V_T and dynamic on-resistance r_{on}, i.e.

$$P_{con,Diode} = V_T I_{AV} + r_{on} I_{rms}^2 \quad . \tag{3}$$

For the switching energies, Fig. 3b and Fig. 3c show that the switching losses for each device have a linear relationship to the switched current. Therefore, all switching energies can be modeled as a linear equation according to

$$E_{on,S1,4,5,6} = a_{on} i_{out}(t) mod(t) + b_{on} \tag{4}$$

$$E_{off,S1,4,5,6} = a_{off} i_{out}(t) mod(t) + b_{off} \tag{5}$$

where a_{on}, a_{off}, b_{on} and b_{off} are curve fitting constants for each device derived from the plots shown in Fig. 3. $i_{out}(t)$ is the AC load current and $mod(t)$ is the output voltage modulation function which is defined in the usual way as

$$mod(t) = M sin(\omega t) \tag{6}$$

where M is the modulation index. The overall averaged switching losses can then be calculated as

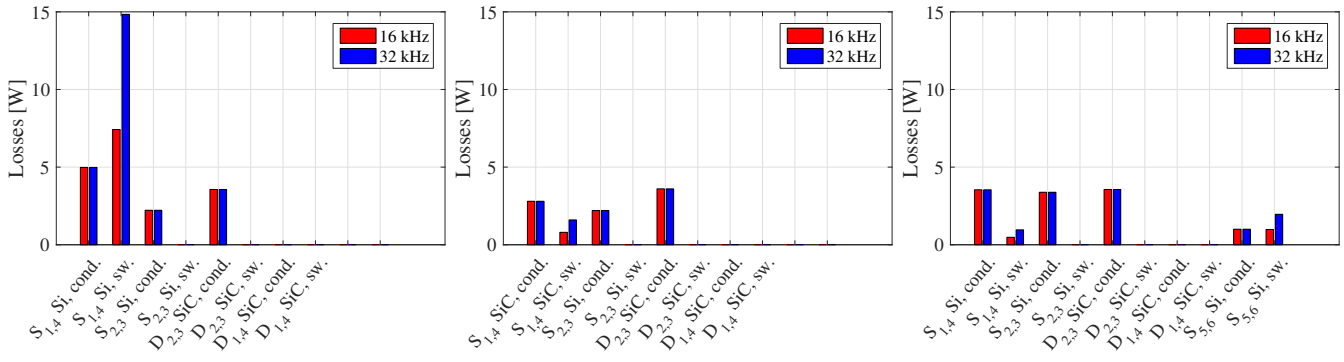
$$P_{sw,S1,4,5,6} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{T/2} (E_{on,S1,4,5,6} + E_{off,S1,4,5,6})\, dt \tag{7}$$

Once these equations are established and the average and rms currents are determined either analytically or via simulations, the total semiconductor losses can be calculated for any given operating point, with an associated device loss breakdown. Fig. 5 shows this loss breakdown for the Si based T-Type, the SiC MOSFET based T-Type and the Hybrid-NPC inverters with the specifications given in Table II, and operating at an output power of 1.5 kW.

From this result, it can immediately be seen that even though the outer switch commutation voltage is only $V_{DC}/2$, switching losses in the 1200 V Si IGBT are the largest loss contributor to the overall semiconductor losses. Obviously, this effect becomes more severe as the switching frequency increases. Both the SiC based T-Type and the Hybrid-NPC substantially reduce these switching losses as shown in Fig. 5b and Fig. 5c. In fact, for this particular example, at a switching frequency of 16 kHz, the switching losses in the 1200 V Si IGBT are 7.4 W while the switching losses in the 1200 V SiC MOSFET are only 0.8 W and the switching losses using the 600 V CoolMos FET device are 1.1 W. Note also that semiconductor losses are more evenly distributed among the devices for these two more advanced arrangements. Thus, both inverter variations are attractive alternatives compared to a conventional T-Type inverter structure when reduced semiconductor losses are an important factor.

TABLE I
Semiconductor devices used

	Si T-Type	SiC T-Type	Hybrid-NPC
S_1/S_4	IKW15N120T2	C2M0080120D	IKW15N120T2
S_2/S_3	IKP15N60T	IKP15N60T	IKP15N60T
D_2/D_3	C3D10060A	C3D10060A	C3D10060A
S_5/S_6			SPP20N60S5



(a) Si T-Type (b) SiC T-Type (c) Hybrid-NPC

Fig. 5. Loss breakdown analysis for different inverter alternatives. DC link voltage $V_{DC} = 800$ V, filtered output voltage $V_{out,RMS} = 230$ V, output power $P_{out} = 1500$ W

TABLE II
INVERTER SPECIFICATIONS

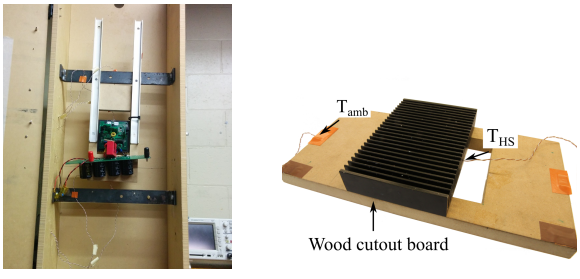
Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 µF
M	Modulation index	0.85

V. Loss Model Validation by Thermal Measurements

Since the losses and the loss reduction discussed in this paper relate only to the semiconductor devices, they can be readily validated experimentally. This was done using thermal measurements on the device heat sink since semiconductor device losses lead directly to an increased heat sink temperature. To accurately match these temperature measurements to the semiconductor losses, the converter power stage was located inside an open ended chimney as shown in Fig. 6a. To minimize any thermal influence from the surrounding of the power stage (for instance gate driver circuitry), the heat sink was thermally decoupled from the rest of the power stage circuitry using a wooden panel as shown in Fig. 6b. Then, two temperatures are measured, one at the top of the heat sink T_{HS} and one below the heat sink giving T_{amb}, as shown in Fig. 6b. The difference between these readings gives the relative heat sink rise according to

$$\Delta T = T_{HS} - T_{amb} \quad . \tag{8}$$

The measurement was used to carefully calibrate the heat sink using known DC loads. This was achieved by supplying the inverter with a known DC voltage and current (and hence power) with inverter switch states selected such that the semiconductor devices absorb all of the power supplied from the controlled DC source. This is illustrated in Fig. 7 for the switches of the Hybrid-NPC converter, i.e. S_5, S_1 and S_4. Similar results were taken for as many different switch pair combinations as possible (e.g. S_1, S_3 and D_3 as a combination and D_2, S_2 and S_4 as another combination), to achieve a well-defined temperature profile of the heat sink. The injected power corresponds to the thermal energy forced into the heat sink, and is thus responsible for the heat sink temperature rise. Note that several calibration runs are necessary for different power levels to achieve a relation between the injected power and the heat sink temperature rise over a wide range of power loss points, as shown in Fig. 8. The resultant loss profile is linear, as could be expected for a constant heat sink thermal impedance.



(a) Converter placed in chimney

(b) Thermal measurements location

Fig. 6. Thermal measurement setup

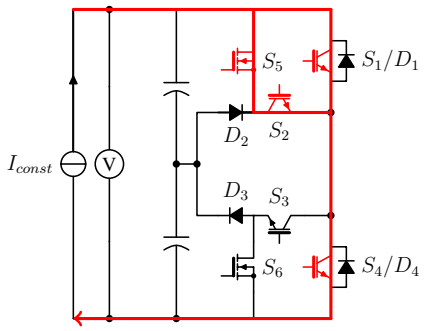


Fig. 7. Switch pair S_5, S_2, S_1 and S_4 are conducting

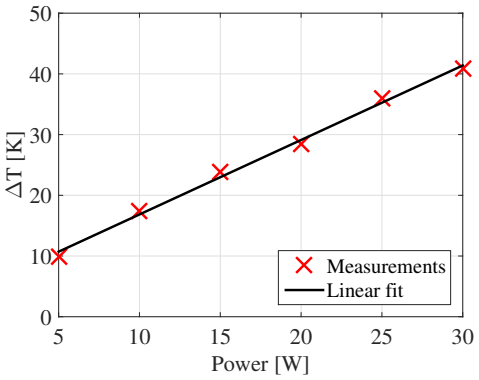


Fig. 8. Device losses versus heat sink temperature rise

VI. Experimental Results

Once the calibration procedure was completed, the converter was then operated at a number of operating conditions to determine the aggregate semiconductor device losses. Operating the converter using phase disposition (PD) PWM [18], [19] with the parameter specifications provided in Table II, the resulting experimental output waveforms for a 230 V, 50 Hz system at 1.5 kW are shown in Fig. 9. The loss results for different operating conditions such as varying output power and switching frequency are shown in Fig. 10, where the predicted semiconductor losses are compared against the measured semiconductor losses. The results are clearly well within the measurement bounds of the experimental thermal measurement technique, and confirm that both the SiC based T-Type inverter and the Hybrid-NPC inverter achieve a major loss reduction compared to the conventional Si based T-Type inverter. More specifically, at 1.5 kW and 16 kHz, the Si T-Type inverter has total semiconductor losses of 22 W while the SiC based alternative

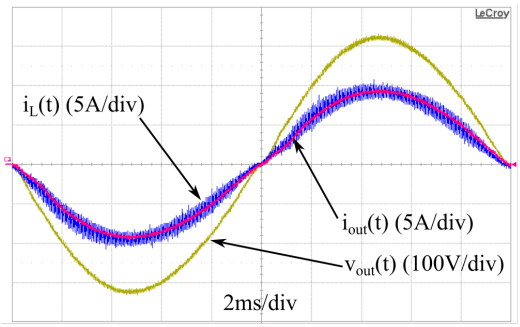
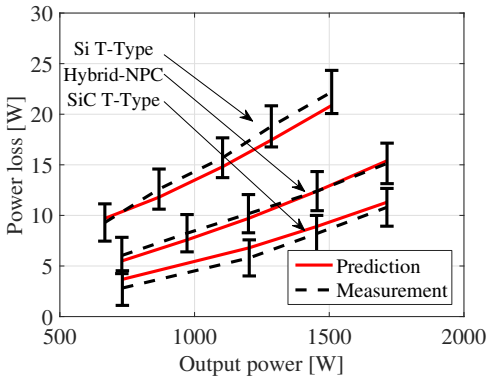
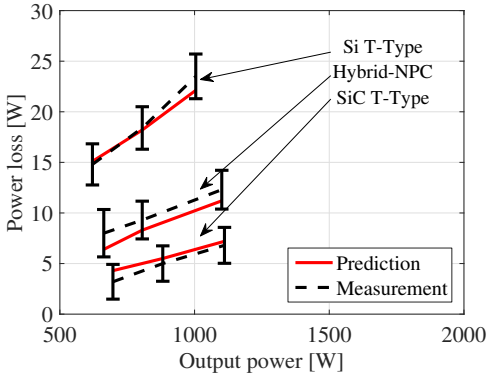


Fig. 9. Experimental output waveforms

has only 9 W losses and the Hybrid-NPC converter shows semiconductor losses of about 13 W. This results in a loss reduction of around 60 % for the SiC based converter and 42 % for the Hybrid-NPC. Hence the Si based T-Type inverter has the highest heat sink temperature rise above ambient at that operating point, shown in Fig. 11, where the heat sink temperature rises for each alternative are presented. In particular, for the conventional T-Type inverter, the temperature rise of the heat sink above ambient is 31.8 °C compared to only 14.6 °C for the SiC alternative and 19.8 °C



(a) Semiconductor losses at 16 kHz



(b) Semiconductor losses at 32 kHz

Fig. 10. Semiconductor losses experimentally obtained via thermal measurements

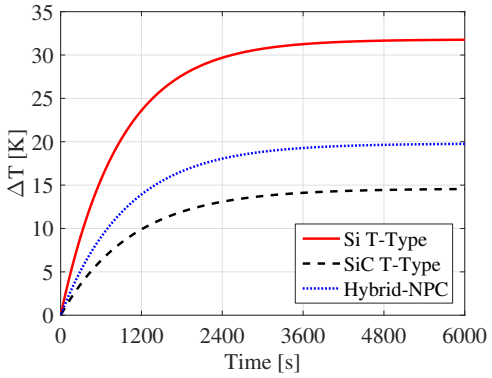


Fig. 11. Heat sink temperature rise of different inverter alternatives

for the Hybrid-NPC. Thus the loss reduction can not only be interpreted in terms of higher efficiency, but there is potential for further cost reduction by using a smaller heat sink.

VII. Discussion

Two observations from Fig. 10 are worthy of further comment regarding the two converter alternatives. Firstly, while the Hybrid-NPC can substantially reduce its total semiconductor losses compared to the conventional T-Type inverter, its loss reduction is not as good as the SiC based T-Type structure. This can be explained by recognizing that although the switching losses are greatly reduced for the Hybrid-NPC converter, its total semiconductor conduction losses are larger compared to the SiC based T-Type inverter because of the very low on-state resistance of the SiC MOSFETs as shown in Fig. 4. Furthermore, from Fig. 2c, the conduction losses in the inner bi-directional switches S_2/S_3 are increased because they conduct current during both the zero converter output period and positive/negative converter output period.

The second observation relates to switching losses. As the switching frequency is increased, the power loss increase is larger for the Hybrid-NPC alternative compared to the SiC based T-Type converter. This can be explained from Fig. 3b, which identifies larger turn on energies for the CoolMos FET relative to the SiC MOSFET. Therefore, at any particular switching frequency, switching losses in the Hybrid-NPC will be higher than the SiC MOSFET based T-Type structure.

VIII. Conclusion

This paper has compared two promising three-level inverter topologies that aim to reduce switching losses compared to a conventional T-Type inverter structure. The first alternative is to simply replace the lossy 1200 V Si IGBTs with low loss 1200 V SiC MOSFETs. The second alternative strategically adds 600 V CoolMos FET devices to better support the switching transitions. A loss breakdown analysis using a loss model obtained from datasheet information and in-circuit measurement of switching events quantifies the loss reduction for both alternatives. In order to verify these semiconductor

loss models, a simple thermal measurement technique was used based on calibrated heat sinks. The experimentally confirmed results show that a total semiconductor loss reduction of up to 60 % can be achieved using SiC MOSFETs and 42 % for the Hybrid-NPC inverter. Furthermore, this loss reduction for both alternatives has the additional benefit of operating at a significantly lower temperature, which offers further potential for reduced heat sink costs and/or increased inverter life expectancy.

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