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Published in:
I E E E Transactions on Power Electronics

Link to article, DOI:
10.1109/TPEL.2016.2582344

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2582344, IEEE Transactions on Power Electronics

The Benefits of SiC MOSFETs in a T-Type Inverter for Grid-Tie Applications

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***Abstract*—It is well known that multilevel converters can offer significant benefits in terms of harmonic performance and reduced switching losses compared to their two-level counterparts. However, for lower voltage applications the Neutral-Point-Clamped (NPC) inverter suffers from relatively large semiconductor conduction losses because the output current always flows through two switching devices. In contrast, the T-Type multilevel inverter has less conduction losses because only a single outer loop switching device is required to connect the converter output to the upper and lower DC buses, albeit at the expense of increased switching losses since these outer switches must now block the full DC link voltage. Silicon Carbide (SiC) MOSFET devices potentially offer substantial advantage in this context with their lower switching losses, but the benefit of replacing all switching devices in a T-Type inverter with SiC MOSFETs is not so clear-cut. This paper now explores this issue by presenting a detailed comparison of the use of Si and SiC devices for a three-level T-Type inverter operating in grid-tie applications. The study uses datasheet values, switching loss measurements and calibrated heat sink thermal measurements to precisely compare semiconductor losses for these two alternatives for a T-Type inverter operating at or near unity power factor. The results show that replacing only the DC bus connection switches with SiC devices significantly reduces the semiconductor losses, allowing either the converter power level or the switching frequency to be significantly increased for the same device losses. Hence the use of SiC MOSFETS for T-Type inverters can be seen to be an attractive and potentially cost effective alternative, since only two switching devices per phase leg need to be upgraded.**

***Index Terms*—Photovoltaic, Semiconductor losses, Si IGBT, SiC MOSFET, T-Type Inverter**

I. Introduction

RENEWABLE energy generation has been gaining increasing interest in the last two decades. Among the renewable energy alternatives, photovoltaic (PV) generation is one of the most significant with a total global capacity of 177 GW in 2014 [1]. In the residential sector, single- and three phase PV systems are widely used and are typically grouped into systems with and without galvanic isolation. The latter approach has the particular benefits of higher efficiency, higher power density and lower cost due to the absence of the transformer [2], which are important design criteria for low cost PV systems. Recent studies [2]–[4] have compared in detail two- and three-level inverter topologies based on semiconductor losses and filter considerations, and have identified that in particular for higher switching frequencies, three-level inverter topologies can have lower semiconductor losses than their two-level counterparts because each switching event needs only commutate half the DC link voltage at each transition [3], [4]. Furthermore, since the AC output of a three-level inverter has a lower harmonic content because of its improved harmonic cancellation [5], significant size reductions of the AC filter components are possible [3].

Of the various three-level inverter topologies available, the most mature configuration is the Neutral-Point-Clamped (NPC) inverter [6], which has been intensively researched since its introduction in 1981. The particular benefit of this converter is that it can be realized with semiconductor devices that need to block only half the DC link voltage. However, while this reduces switching losses [4], the topology suffers from higher conduction losses and an uneven device loss distribution because current must always flow through two semiconductor devices [7], [8]. A more recent alternative is the T-Type inverter [9], [10], which achieves the same converter harmonic output performance but only requires a single switch to connect its output to the upper and lower DC buses. However, the T-Type topology must consequently use semiconductors with higher voltage ratings for its outer switches since they now have to block the full DC link voltage, which means that its semiconductor switching losses are generally higher compared to a NPC converter at the same switching frequency [4]. Thus the choice of switching frequency becomes a crucial parameter in selecting between a NPC and T-Type inverter for any particular application [4]. Essentially, T-Type inverters have lower semiconductor losses at lower switching frequencies because of their reduced conduction losses, while NPC inverters become more advantageous at higher switching frequencies where switching losses become more significant.

Recent work has explored in some detail various ways to minimize T-Type three level inverter losses. For example the loss benefit of optimized discontinuous modulation (DPWM) [9] can be traded off against its increased AC output harmonic content [5]. Another alternative is to replace the Si diodes in the inner bi-directional path with SiC diodes to reduce reverse recovery losses [11] or to use wide bandgap (WBG) switching devices in the inner bi-directional path to reduce

Manuscript received May 29, 2015; revised November 05, 2015 and April 05, 2016; accepted June 10, 2016; date of current version MONTH, DAY, 2016. Recommended for publication by Associate Editor ADD.

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Digital Object Identifier ADD

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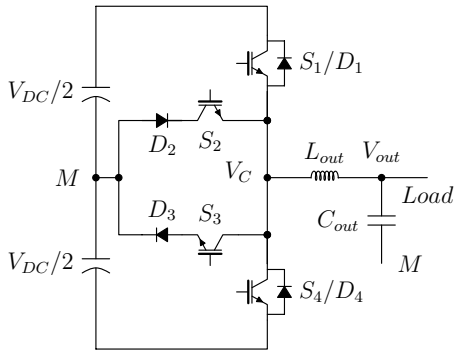
conduction and switching losses [12]. However further work has identified that the primary limiting factor for efficient high switching frequency operation at unity power factor (as is generally required for residential PV inverter systems [13]) are still the switching losses in the DC bus connection switches [11]. [14] compares an optimally designed hard switched SiC based T-Type inverter against an optimally designed Zero-Voltage-Switching (ZVS) T-Type inverter, and concludes that the latter can only slightly increase the system efficiency at the cost of considerably more complexity. Essentially, the focus of most approaches to date has been to attempt to work around the basic T-Type inverter switching frequency limitation, which is that the outer DC bus connection switches have higher switching losses compared to a NPC inverter because they must have higher voltage rating to block the full DC link voltage.

This paper now presents the investigation results for the more direct approach of simply replacing the T-Type inverter outer switch 1200 V Si IGBTs (higher switching loss) with 1200 V SiC MOSFETs (lower switching loss). Of course the loss reduction advantages in principle of SiC devices compared to Si devices are already well established [15]–[26], but their benefit in the context of a T-Type inverter is not so clear-cut. This is because while the outer switches of a T-Type inverter must be rated to block the full DC link voltage, they only commutate at half the DC link voltage when actively switching. Thus their switching losses are substantially reduced compared to their normal rated operating conditions and hence analysis is required to determine the level of benefit to be gained by moving to SiC devices in this context. Furthermore, since one phase leg of the T-Type topology comprises of four active switching devices, it may lead to the misconception that an upgrade of all active devices to SiC is necessary to achieve efficient high frequency operation of the converter irrespective of the converter operating point. In these terms, the most commonly reported methodology of validating potential loss benefits on a topological or semiconductor level is to measure overall converter efficiency by means of electrical input and output power measurements using a power analyzer or digital oscilloscope. However, it can be challenging to get accurate results with this approach for high efficiency converters [27]–[29] because of the difficulty of measuring the high speed pulse width modulated voltages and currents of the converter with adequate precision, and overall converter losses (including losses in the DC link capacitor bank as well as the AC output filter) are obtained rather than semiconductor losses only.

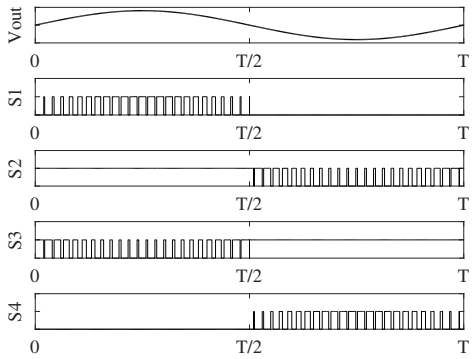
Due to the aforementioned reasons, this paper presents a comprehensive loss analysis for the T-Type structure and investigates the potential benefits of using next generation switching devices targeting a typical single phase residential PV inverter application. This work furthermore presents an alternative loss validation methodology that enables direct access to the semiconductor device losses alone while actively operating in T-Type inverter context. Using a carefully calibrated heat sink, semiconductor device losses can be obtained and thereby potential benefits of upgrading the converter to SiC evaluated.

II. T-Type Inverter Description and Device Selection

Figure 1a shows the basic structure of one phase leg of a three-level T-Type inverter, comprising a HV DC link with split bulk capacitors, four switching devices, four diodes and an AC filter to obtain the target AC output voltage. The converter switches are operated as the complementary pairs S_1/S_3 and S_2/S_4 in accordance with Table I to achieve the required switched output voltages of $+V_{DC}/2$, 0 and $-V_{DC}/2$ that produce a three level AC output voltage. Note that the switching states shown in Table I achieve the same switched output voltages as a NPC inverter (i.e. switch S_1 is closed to achieve a positive output voltage, S_2 or S_3 needs to be closed for a zero output voltage, and switch S_4 is closed for a negative output voltage) even though the detail switch usage is different for the two converter topologies. Figure 1b shows the switch commands created when the converter is controlled using the optimum phase disposition (PD) PWM strategy [30], [31], where the characteristic discontinuous operation of the two switch pairs can be clearly seen. Fig. 2a-Fig. 2c present a more detailed illustration of the switching transition between



(a) Single phase schematic of the T-Type inverter



(b) PD PWM for three level inverter with a fundamental frequency of 50 Hz

Fig. 1: Schematic of T-Type inverter topology in (a) and its modulation principle in (b)

TABLE I: Switching states for T-Type inverter

Output voltage	S_1	S_2	S_3	S_4
$V_{DC}/2$	1	1	0	0
0	0	1	1	0
$-V_{DC}/2$	0	0	1	1

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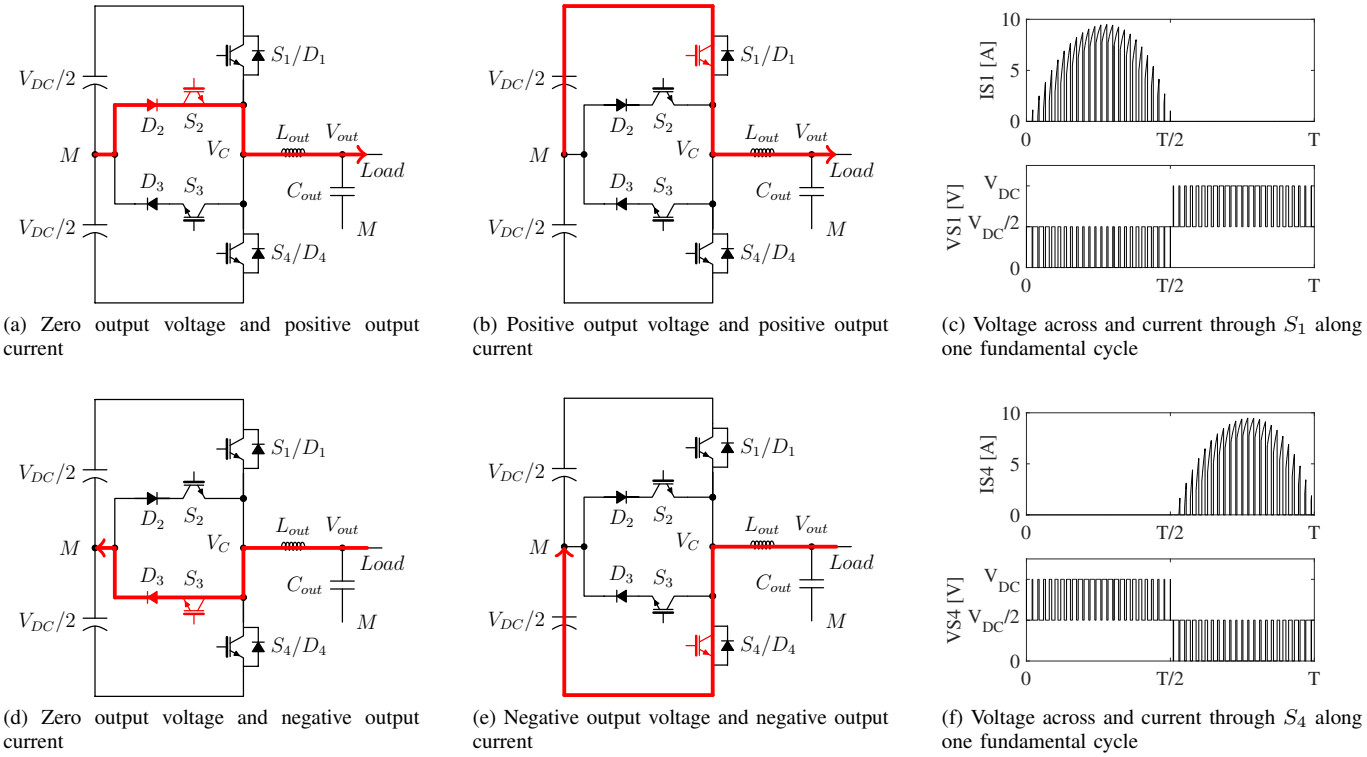

(a) Zero output voltage and positive output current

(b) Positive output voltage and positive output current

(c) Voltage across and current through S_1 along one fundamental cycle

(d) Zero output voltage and negative output current

(e) Negative output voltage and negative output current

(f) Voltage across and current through S_4 along one fundamental cycle

Fig. 2: Switching states for T-Type inverter operating at unity power factor

the zero output state and the positive output state for unity power factor operation during the fundamental positive half cycle. During the zero output state, the positive output current flows from the midpoint M through diode D_2 and switch S_2 to the load as shown in Fig. 2a, and the voltages blocked by switches S_1 and S_4 are both $V_{DC}/2$. Switch S_1 then turns on to create the positive output state, commutating the output current from D_2/S_2 to S_1 against an off-state voltage of $V_{DC}/2$ with associated switching losses, as shown in Fig. 2b. Outer switch S_4 now blocks a voltage of V_{DC}, depicted in Fig. 2f. This cycle repeats throughout the fundamental positive half cycle as shown in the left hand side of Fig. 2c. By symmetry, a similar switching process occurs during the fundamental negative half cycle as shown in Fig. 2d-Fig. 2f, with a switching commutation between D_3/S_3 and S_4 against an off-state voltage of $V_{DC}/2$, and with switch S_1 alternately blocking a voltage of $V_{DC}/2$ and V_{DC} as the output voltage changes from zero to negative, as shown in Fig. 2c. Thus outer switches S_1 and S_4 must have a voltage blocking rating in excess of V_{DC}, even though their commutation switching voltage is only $V_{DC}/2$. This complicates their overall loss calculation since their on-state voltages will be typically higher than a lower voltage rated device [3], but their switching losses need to be determined at only half their rated voltage because of the operating sequence described above. In contrast, the inner switches S_2 and S_3 see only a reduced voltage blocking rating of $V_{DC}/2$ with corresponding lower forward conduction losses [3]. Also, since these switches do not have to commutate current when operating at unity power factor, they will have negligible switching losses irrespective of the type of switching device used. Furthermore, even with a near unity load power factor, their switching losses will still be quite small since they are commutating only low magnitude currents close to the fundamental current zero crossing transition.

Since for a typical residential PV system the DC link voltage can reach up to 1000 V, 1200 V rated devices are required for the outer switches S_1 and S_4 for a T-Type inverter operating in this application, while 600 V semiconductor devices are adequate for the inner parallel-connected devices $D_{2,3}$ and $S_{2,3}$. Among the various switching devices to date, IGBTs have found commonplace usage within power converter systems operating at voltages in the range of 1000 V and currents of several amperes because of their relatively low on-state voltage compared to a Si FET device, whose specific on-resistance is proportional to the square of the breakdown voltage V_B according to [32]

$$R_{DS(on),spec} \propto V_B^2 \quad . \tag{1}$$

An IGBT's drawback, however, is its slower switching capability due to its bipolar output characteristic. This is illustrated in Fig. 3a and Fig. 3b, which show forward voltages and switching energies of several IGBT devices from different manufacturers, and that are optimized for either low switching energies or low saturation voltage. All devices are in the 1200 V range and have a similar current capability for a fair comparison, and it can be noted that switching loss optimized devices have the tendency to show larger forward voltages, thereby trading off their lower switching losses in a converter operating context against larger conduction losses. In this

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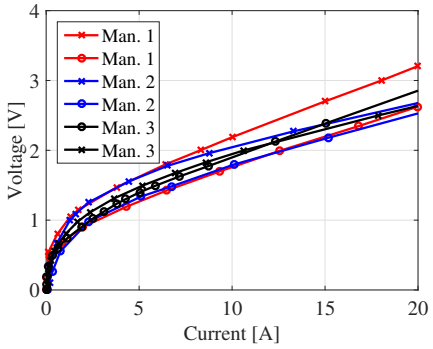
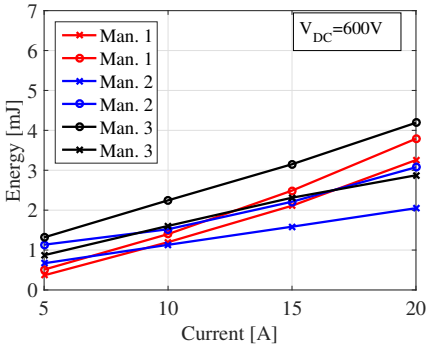
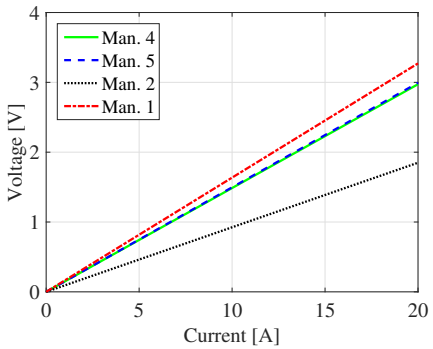


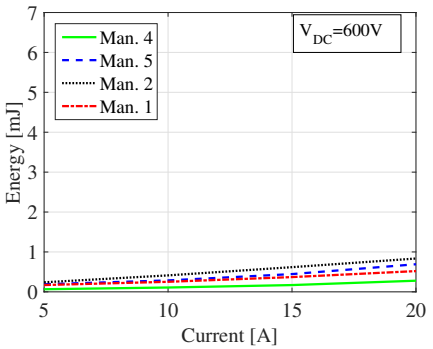
(a) Forward voltages of several Si IGBTs at 175 °C junction temperature



(b) Switching energies of several Si IGBTs at 175 °C junction temperature



(c) Forward voltages of several SiC FETs at 175 °C junction temperature



(d) Switching energies of several SiC FETs at 175 °C junction temperature

Fig. 3: Forward voltages and switching energies of different Si IGBT and SiC FET devices. The colors relate to the particular manufacturer whereas the sign relates to the device optimization. A cross is a device optimized for low switching energies whereas a circle stands for a device optimized for low saturation voltages

context, SiC based semiconductors are an attractive alternative combining low on-resistance and low switching energies, as demonstrated in Fig. 3c and Fig. 3d showing forward voltages and switching energies for several available 1200 V SiC FET devices (either through distribution channels or as samples). With the investigation of several state-of-the-art Si IGBTs, the choice between an IGBT optimized for low switching losses or low saturation voltages for the study was made on the following basis. Since a T-Type inverter typically switches at a relatively low switching frequency, and the outer devices also only need to commutate current at less than half their rated voltage as previously described, an IGBT showing a good compromise between switching energies and forward voltage was selected as the more appropriate alternative for the comparison against the SiC MOSFET presented in this paper. The choice of semiconductor devices is listed in Table II, suiting a typical residential single phase PV inverter system connected to the low voltage grid, i.e. 230 V/50 Hz, and operating at a nominal output power of 1.5 kW (approx. 10 A peak current) with a 20 % overload capacity and a conservative 30 % to 40 % de-rating factor for long life reliability. Also SiC devices were used for all diodes to minimize the influence of reverse recovery charge on the switching device loss evaluation.

III. Loss Evaluation of Si and SiC Switching Devices

Evaluation of the semiconductor loss profiles for Si IGBTs and SiC MOSFETs requires quantification of the conduction and switching characteristics for both switch families in the context of the T-Type inverter application. For conduction losses it is sufficient to use manufacturer's datasheets which provide detailed performance data for the IGBT saturation voltages, the MOSFET $R_{DS(on)}$, and the forward voltage of the anti-parallel diodes [4]. However it is more difficult to determine the switching loss behavior of these devices from datasheets, particularly when they are operated well outside the test conditions that are used to obtain the datasheet

TABLE II: Semiconductors used

Semiconductors	Device	Voltage [V]	Current at 25 °C [A]	Price (June 2016) [USD]
$S_{1,4,Si}$	IKW15N120T2	1200	30	4.6
$S_{1,4,SiC}$	C2M0080120D	1200	36	16.67
$D_{2,3,SiC}$	C3D10060A	600	29.5	4.82
$S_{2,3,Si}$	IKP15N60T	600	30	1.95
$S_{2,3,SiC}$	SCT2120AF	650	29	9.07
$D_{1,4,SiC}$	C4D15120A	1200	41	16.88

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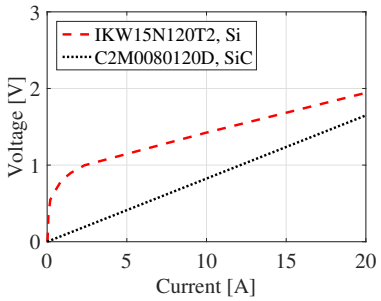
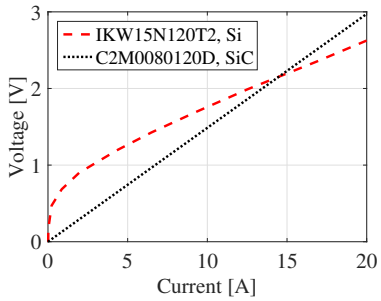
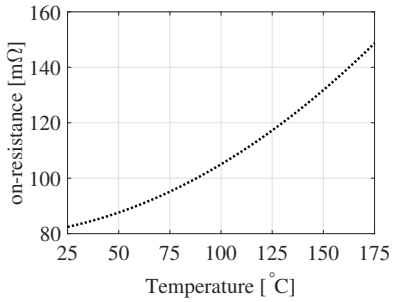


(a) Forward voltages of Si IGBT and SiC MOSFET at 25 $°C$ junction temperature



(b) Forward voltages of Si IGBT and SiC MOSFET at 175 $°C$ junction temperature



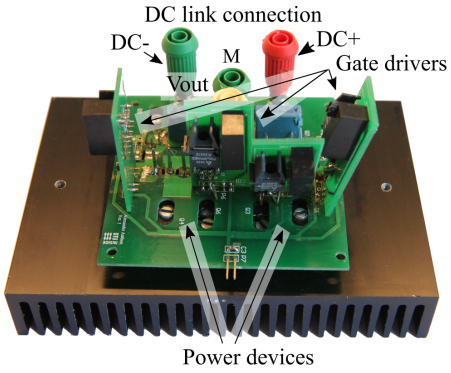
(c) SiC MOSFET on-resistance $R_{DS(on)}$ versus junction temperature

Fig. 4: Si IGBT forward voltage and SiC MOSFET on-resistance at different current levels and junction temperatures

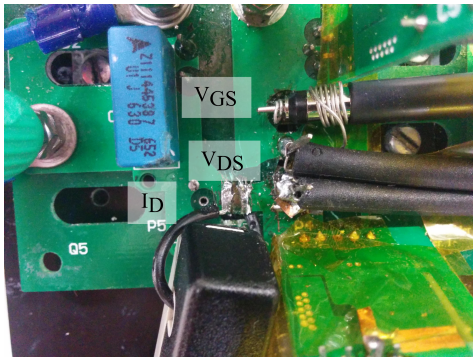
results. Typically, switching energies need to be determined for particular operating conditions such as gate resistances, gate drive voltage, junction temperature and different types of free-wheeling diodes [4]. Hence to obtain a fair comparison for the switching loss behavior between Si IGBT and SiC FET devices, their switching energies were experimentally measured using the prototype T-Type inverter developed for this study.

A. Conduction Losses of the S_1 and S_4 devices

Conduction losses are determined by the voltage drop across the device and the current that is flowing through the device whilst turned on. These losses represent a major contribution to the overall semiconductor loss profile. The specified forward voltages of the selected IKW15N120T2 Si IGBT, and the C2M0080120D SiC MOSFET at different current and temperature levels as shown in Fig. 4 can be used to determine these conduction losses. Note that the SiC MOSFET has a significantly smaller voltage drop than the IGBT over most of the inverter's operating current range, which leads to smaller conduction losses. This is because the SiC MOSFET is an unipolar device with a resistive output characteristic. Thus a smaller current flowing through the device will cause a smaller voltage drop according to Ohm's law. In contrast an IGBT is a device with a bipolar output characteristic. This results in a larger voltage forward drop, especially for low currents.



(a) Prototype of the T-Type inverter



(b) Switching energy measurements on the T-Type prototype

Fig. 5: Prototype in (a) and current measurement in (b)

B. Switching Characteristics

In order to adequately assess the switching characteristics and hence the switching energies of the devices, their switching transitions were measured directly using the laboratory prototype shown in Fig. 5a, with the switching voltages measured using oscilloscope probes places as shown in Fig. 5b. The current measurements were made using a Tektronix TCP305 current probe having a bandwidth of 50 MHz. The gate-emitter voltage for the IGBT and the gate-source voltage for the MOSFET were measured using a Textronx P220 voltage probe with a bandwidth of 200 MHz. The collector-emitter voltage for the IGBT and the drain-source voltage for the MOSFET were measured using a high voltage differential probe with a bandwidth of 50 MHz. Compensation was included into the waveform analysis procedure to allow for the specified delay times of 19 ns for the current probe and 15 ns for the differential voltage probe. Waveforms of the measured turn on and turn off switching transitions at 400 V and 10 A for both the Si IGBT and the SiC MOSFET in the T-Type inverter are shown in Fig. 6, since this is the identified switching conditions for this inverter as discussed above. From these figures it is clear that the SiC MOSFET has superior switching characteristics in terms of di/dt and dv/dt. For example, at the turn off transition in Fig. 6c and Fig. 6d, the SiC MOSFET switches

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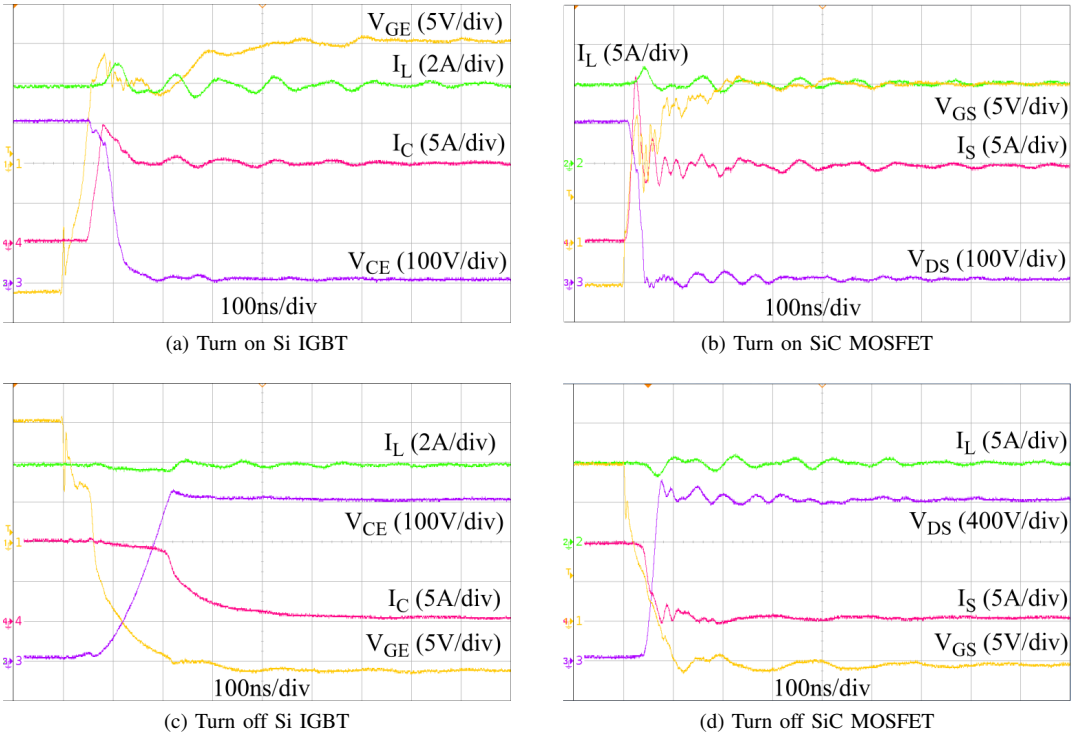

(a) Turn on Si IGBT

(b) Turn on SiC MOSFET

(c) Turn off Si IGBT

(d) Turn off SiC MOSFET

Fig. 6: Turn on and turn off switching transitions for a voltage of 400 V and 10 A

TABLE III: Switching evaluation

	Turn on		Turn off	
	IGBT	MOSFET	IGBT	MOSFET
dv/dt in kV/µs	7.8	13.3	2.84	15.9
di/dt in kA/µs	0.45	1.33	0.05	0.2

at almost 16 kV/µs whereas the Si IGBT switches at less than 3 kV/µs. Table III quantifies the turn on and turn off switching characteristics shown in Fig. 6 for the two devices. Measuring the voltage and current transitions in this way for a variety of operating conditions, such as different current levels and junction temperatures, switching energies can then be obtained by numerically integrating the product of the measured voltages and currents. Using this approach, the resulting turn on and turn off energies for the Si IGBT and SiC MOSFET are shown in Fig. 7 for operation at both low and high temperatures, and Table IV lists the numerical values of the applied methodology for a case temperature of 100 $°C$. Note that while the turn on energy magnitudes for both the Si and the SiC devices are relatively low, the Si IGBT still must dissipate more than twice the turn on switching energy of the SiC MOSFET. From these results it can be seen that the major benefit of the SiC MOSFET is its very low turn off energies which appear to be almost constant over the current and temperature range of interest. In contrast the IGBT has much larger switching energies that increase linearly with current. It is further worthy of comment that the temperature majorly influences only the turn off energies of the Si IGBT, while hardly affecting any of the other switching energies (especially the SiC MOSFET). From these measurements, it can be seen that the turn off switching energies of the IGBT are more than 17 times higher than those of the SiC MOSFET at a current of 3 A and more than 22 times higher at a current of 7 A. These very low SiC MOSFET switching energies are a very attractive characteristic as switching frequency is usually the limiting factor for higher frequency operation of a T-Type inverter due to the large turn off energy loss of a Si IGBT [11].

TABLE IV: Switching energies at 100 $°C$

	Si IGBT		SiC MOSFET	
Current [A]	E_{on} [µJ]	E_{off} [µJ]	E_{on} [µJ]	E_{off} [µJ]
2	71.5	327	29.2	18.3
4	88.7	436.7	32.3	20.5
6	105.7	553.1	33.4	23
8	123.1	641.2	37.3	24.7
10	145	752.3	39.5	27

C. Semiconductor Loss Modeling

Based on these results, a model for the semiconductor losses can now be obtained. Piece-wise linear models for the IGBTs and diodes are commonly used to model conducting losses for such studies, and so are used in this work, i.e.

$$P_{con,IGBT} = V_f I_{AV} + r_{on,IGBT} I_{rms}^2 \tag{2}$$

where V_f is the zero on-state voltage, I_{AV} the average current, $r_{on,IGBT}$ the dynamic on-state resistance and I_{rms}

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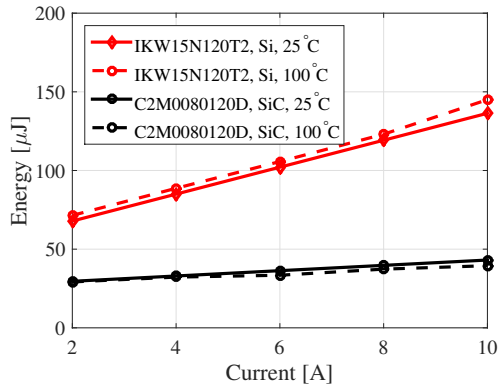
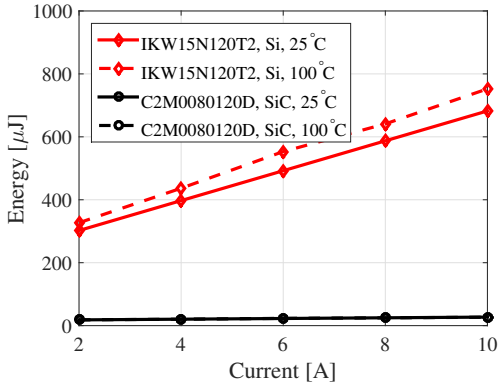


(a) Turn on energies



(b) Turn off energies

Fig. 7: Measured turn on and turn off switching transitions for a voltage of 400 V and 2 A to 10 A

the root-mean-square (rms) value of the current. Conduction losses for the diodes are obtained in a similar way, i.e.

$$P_{con,Diode} = V_0 I_{AV} + r_{on,Diode} I_{rms}^2 \tag{3}$$

where V_0 is the diode's threshold voltage and $r_{on,Diode}$ is the dynamic on-resistance of the diode. For the SiC MOSFET, only the on-resistance $R_{DS(on)}$ is used to determine the conduction losses, i.e.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2 \quad . \tag{4}$$

From Fig. 7, the switching energies have a linear relationship with current and hence they can be modeled as

$$E_{on,S1,4} = a_{on,S1,4} i_{out}(t) mod(t) + b_{on,S1,4} \tag{5}$$

$$E_{off,S1,4} = a_{off,S1,4} i_{out}(t) mod(t) + b_{off,S1,4} \tag{6}$$

where $a_{on,S1,4}$, $a_{off,S1,4}$, $b_{on,S1,4}$ and $b_{off,S1,4}$ are the curve fitting constants. $i_{out}(t)$ is the load current (assumed to be pure sinusoidal with an electrical angular frequency ω and a phase shift of φ), i.e.

$$i_{out}(t) = \hat{I} sin(\omega t - \varphi) \tag{7}$$

and the modulation function $mod(t)$ is defined for a sinusoidal output in the usual way as

$$mod(t) = M sin(\omega t) \tag{8}$$

where M is the modulation index. The mean switching losses for S_1 and S_4 are then given by Eq. (9).

$$P_{sw,S1,4} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{T/2} (E_{on,S1,4} + E_{off,S1,4})\, dt \quad . \tag{9}$$

D. Consolidation of Device Losses into overall Semiconductor Losses

Using the concepts of Section A-C, a loss breakdown analysis for the T-Type inverter with various switching devices was developed using Eq. (2)-Eq. (9). For the inverter specifications shown in Table V, the resulting loss distribution between the two semiconductor devices is shown in Fig. 8, and identifies that the use of SiC MOSFETs for the outer switches does significantly reduce both the conduction losses and the switching losses. For example, at a switching frequency of 16 kHz, which is commonly used in unity power factor grid-tie applications, the switching losses for the IGBT alternative are 7.4 W whereas the switching losses for the SiC MOSFET alternative are only 0.9 W. This gives a switching loss reduction of more than 85 % and a conduction loss reduction of almost 50 %. Total semiconductor losses are therefore 20.87 W for the IGBT based converter and 9.4 W for the SiC MOSFET based converter. The benefits of the SiC MOSFETs become even more obvious as the switching frequency increases, for example at a switching frequency of 32 kHz as shown in Fig. 8.

TABLE V: Specifications

Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 µF
M	Modulation index	0.85

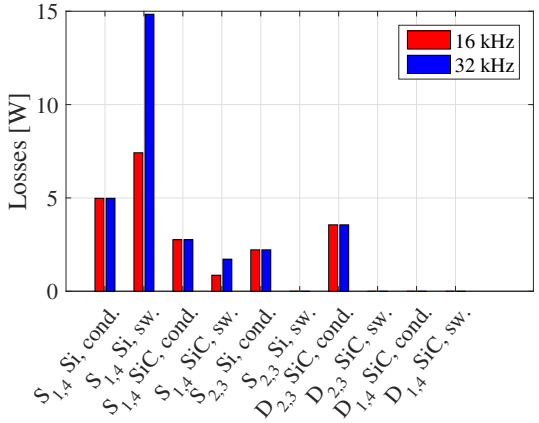


Fig. 8: Loss breakdown analysis for an output power of 1.5 kW, unity power factor and two different switching frequencies

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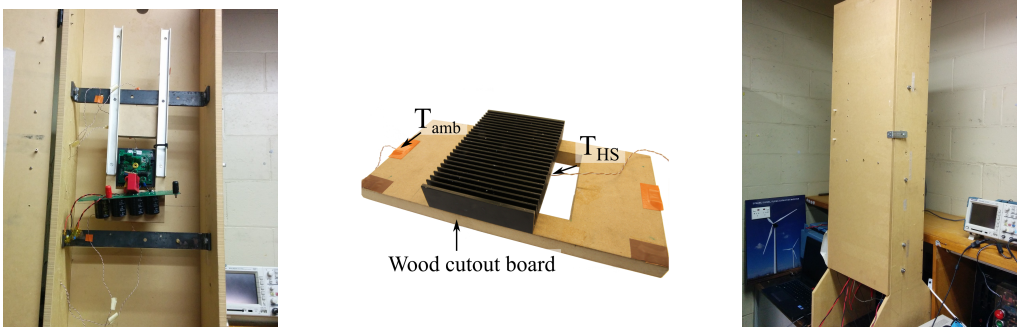


(a) Converter and heat sink in closet

(b) Backside of the converter. Thermal measurements performed directly on the heat sink T_{HS} and below the heat sink T_{amb}

(c) Closed closet to avoid influences from the surroundings

Fig. 9: Closet (open ended chimney) for thermal measurements

IV. Predicted Loss Model Validation by Thermal Measurements

The predicted IGBT and SiC based T-Type inverter losses were then validated experimentally to confirm the modeling approach presented in Section III. This was done using thermal measurements taken from the (calibrated) heat sink used for the prototype shown in Fig. 5a to determine the overall experimental power stage losses, and then comparing this result with the predicted overall losses obtained by summing the individual device losses shown in Fig. 8.

A. Heat sink calibration

The semiconductor devices were mounted on a common heat sink. The converter and the heat sink were then placed inside an open-ended (timber) chimney to minimize the influence of transient air flow changes caused by external disturbances, as shown in Fig. 9a and Fig. 9c.

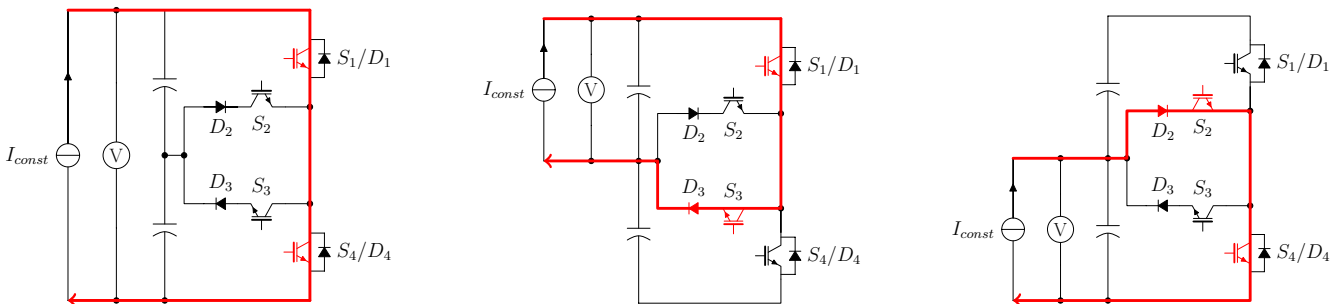
Two thermocouples were used to measure the heat sink temperature T_{HS} and the ambient temperature T_{amb}, placed as shown in Fig. 9b. The relative temperature difference between the input ambient temperature and the heatsink temperature was then obtained using

$$\Delta T = T_{HS} - T_{amb} \quad . \tag{10}$$

To avoid any substantial thermal influence from the gate driver circuit and the DC link capacitors (or more accurately their balancing resistors which are connected in parallel with the capacitors), the heat sink was thermally decoupled from this circuitry using a wood cutout board as shown in Fig. 9b. The heat sink was calibrated by passing a known DC current through three different pairs of semiconductors as shown in Fig. 10, and measuring the overall voltage drop across these devices. The product of these DC voltages and currents is the steady state thermal energy that was injected into the heat sink to cause the measured temperature rise. This procedure was repeated for the three different switching pairs shown in Fig. 10a-Fig. 10c, with the results shown in Fig. 11a. The test outcomes for the different switching pairs at a particular power level were averaged and the procedure repeated for different power levels to obtain the resultant (essentially linear) heat sink calibration curve shown in Fig. 11b, which directly relates heat sink temperature rise to overall power stage device losses.

B. Experimental results and discussion

Using the calibrated heat sink, the inverter as specified in Table V was operated using PD PWM according to Fig. 1b. Experimental waveforms of the converter inductor current $i_L(t)$, the load current $i_{out}(t)$ and the collector-emitter voltage V_{CE} of S_4 operating at 1.5 kW and 16 kHz are



(a) Switch pair 1: S_1 and S_4 conducting

(b) Switch pair 2: S_1, S_3 and D_3 conducting

(c) Switch pair 3: D_2, S_2 and S_4 conducting

Fig. 10: Calibration procedure for heat sink

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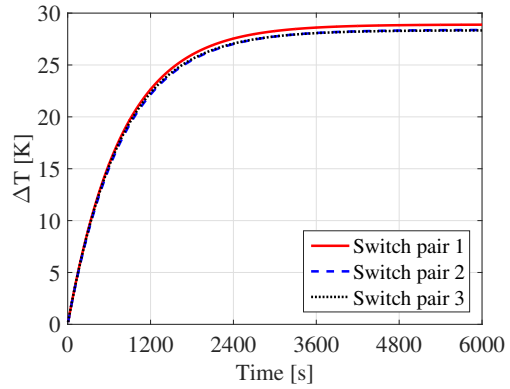
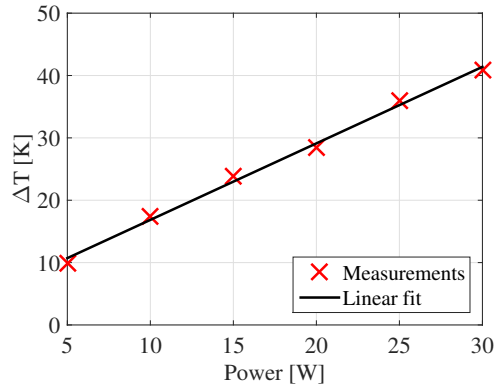
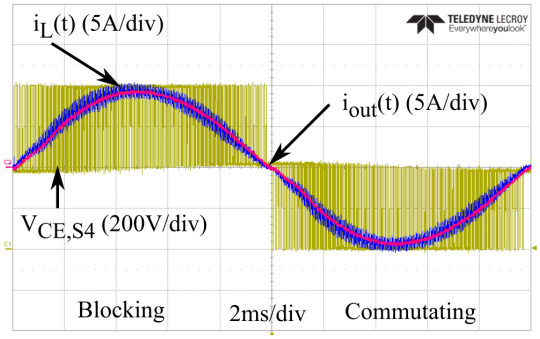


(a) Relative temperature rise versus time for different switch pairs

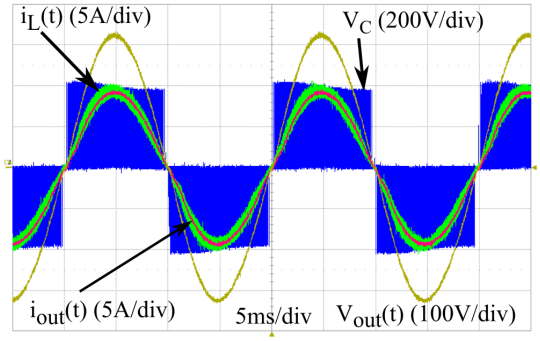


(b) Averaged heat sink calibration curve

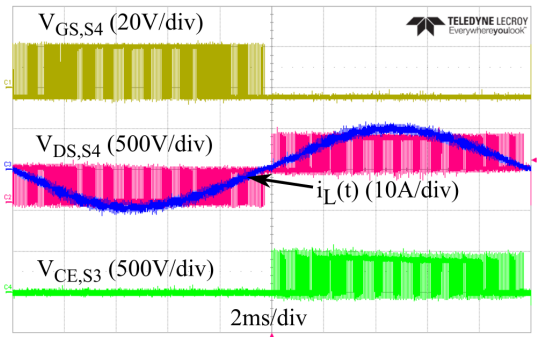
Fig. 11: Calibrated heat sink temperature rise versus time for different conducting semiconductor pairs and resultant curve fit for different power levels



(a) Collector-Emitter voltage of S_4 during inverter operation



(b) Experimental waveforms for $P_{out} = 1.5\,\text{kW}$, $\hat{V}_{out} = 325\,\text{V}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor



(c) Collector-Emitter voltage of S_3 during inverter operation

Fig. 12: T-Type inverter experimental waveforms

shown in Fig. 12a, detailing in particular how switch S_4 commutates with $V_{DC}/2$ (i.e. 400 V) when the output current is negative, but must block the full DC link voltage (i.e. 800 V) when the output current is positive. Figure 12c shows the collector-emitter voltage V_{CE} of S_3 during inverter operation at unity power factor, and verifies that during the negative fundamental half cycle, i.e. when S_3 is turned on according to Fig. 1b, no hard switched commutation losses occur in S_3. By symmetry, the same principle applies to S_2 during the positive fundamental cycle. The total power stage semiconductor losses at any particular operating point were then determined by measuring the steady state heat sink temperature rise using Eq. (10), and translating this back to injected thermal power using Fig. 11b. Note that care must be taken with this approach to ensure that the heat sink reaches a steady state temperature rise before each measurement is taken - for the experimental system used in this paper, approximately 60 minutes of operation were required at each operating condition before measuring the heat sink temperature rise. Working on the basis that the heat sink temperature rise is essentially caused only by power stage semiconductor power losses, this temperature rise measurement then identifies the total semiconductor operating losses of the T-Type inverter at any particular operating point. Using this approach, the inverter was operated for a variety of different switching frequencies and power levels. Fig. 13a and Fig. 13b show the resultant match between the measured semiconductor losses and the predicted losses for the inverter operating with either IGBT or SiC MOSFET switches connecting to the outer DC link buses, where it can be seen that the match between the semiconductor loss predictions and the measured results are well within the measurement bounds of the experimental thermal measurement technique. Figure 13c shows the resultant comparison between the two alternatives. Hence the analytical prediction model developed in Section III can be used with confidence across a wide range of operating conditions. For instance, the T-Type converter operating at non-unity power factors can be investigated, which will now result in switching losses in the bi-directional switching devices $S_{2,3}$. Therefore, switching energies for the 600 V

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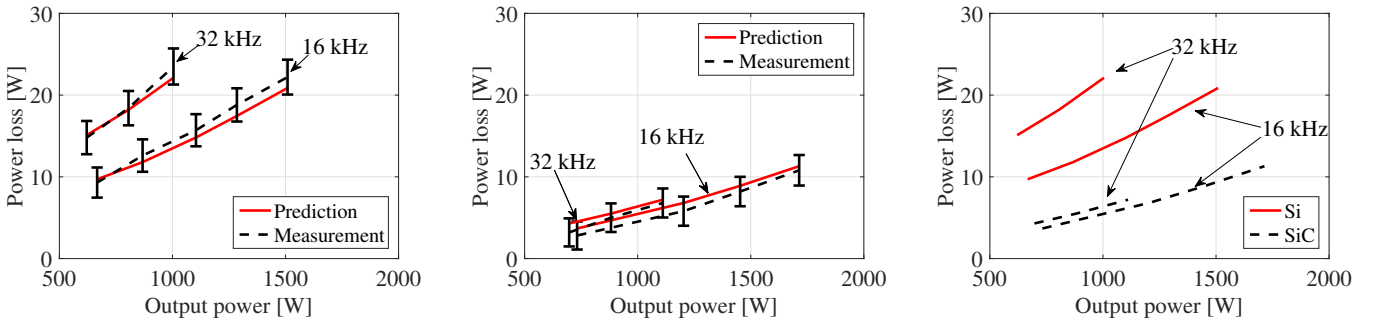


(a) Si IGBT based inverter (b) SiC MOSFET based inverter (c) Semiconductor losses for Si and SiC in T-Type inverter at two different switching frequencies

Fig. 13: Semiconductor losses for Si and SiC switches in the T-Type inverter

devices in the inner bi-directional path according to Table II are determined as explained in Section III, and the results are presented in Fig. 14a and Fig. 14b showing that the turn on energies for the 650 V SiC MOSFET are actually slightly higher at both low and high temperatures, and that the main benefit would be gained from its much lower turn off energies compared to the 600 V Si IGBT. The results identify that among the active switching devices utilized in the T-Type inverter, the switching losses in the 600 V Si IGBTs in the bi-directional path are so much lower compared to the 1200 V Si IGBT connecting to the DC bus, such that an upgrade from a 600 V Si IGBT to a fast switching device (whether it may be a WBG device or a switching loss optimized Si based device) does not offer a significant benefit in terms of switching loss reduction when operating at or near unity power factor, particularly with the current prices for these devices as indicated in Table II.

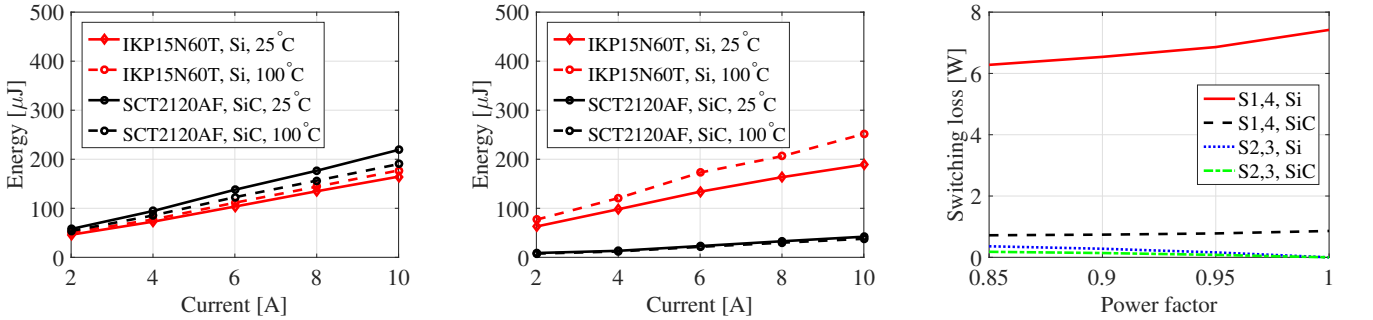
V. Potential Benefits of SiC MOSFETs in T-Type Inverter

The potential benefits of replacing only the outer switches of a T-Type inverter with SiC MOSFETs can clearly be seen from Fig. 13c, which shows that when using SiC MOSFETs, the overall semiconductor losses can be decreased by more than 50 % at a switching frequency of 16 kHz, and considerably more as the switching frequency increases to 32 kHz. From these results, four options for re-designing a T-Type inverter using SiC switching devices in this way can immediately be considered:

(A) For a given inverter, retain its electrical design and use the increased overall efficiency to reduce the thermal stress;
(B) Reduce the heat sink requirement to reduce the converter volume;
(C) Increase the power rating of the inverter for the same heat sink design in order to increase its power density;
(D) Increase the inverter switching frequency, with a consequential reduction in filter component sizes.

A. Efficiency improvements

Semiconductor losses directly influence overall inverter efficiency across the entire operating range of the inverter. As identified in Section III, the SiC MOSFET has a resistive output behavior and hence a low voltage drop at low currents (light load) which leads to small conduction losses under these conditions. In contrast, an IGBT has a bipolar output characteristic and hence a rather constant voltage drop at low currents. Therefore, just replacing S_1 and S_4 with SiC devices instead of IGBT devices will reduce the overall



(a) Turn on energies for 600 V devices (b) Turn off energies for 600 V devices (c) Switching losses against power factor. $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$

Fig. 14: Switching energies for 600 V Si and SiC switches in the T-Type inverter in (a) and (b) and converter switching losses for different power factors in (c)

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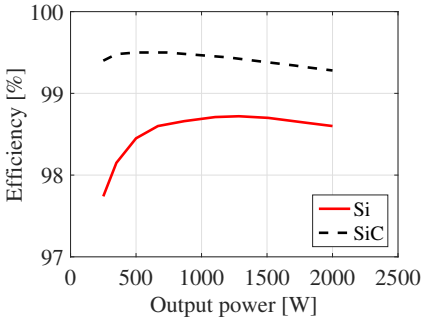
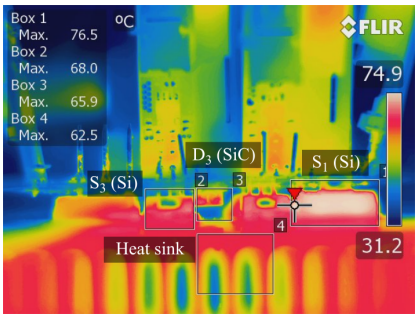
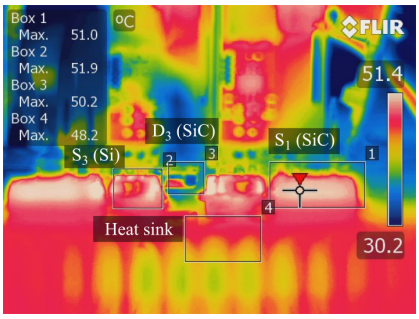


(a) Improved semiconductor efficiency from light load up to overload conditions (16 kHz)



(b) Case temperatures for Si based inverter, $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor



(c) Case temperatures for SiC based inverter, $P_{out} = 1.5\,\text{kW}$, $f_{sw} = 16\,\text{kHz}$ and unity power factor

Fig. 15: Improved efficiency and reduced device case temperatures with SiC device substitution

semiconductor losses as shown in Fig. 13, and consequently improve inverter efficiency (particularly under light load conditions). Neglecting passive component losses (which will remain essentially unchanged for either switching device), Fig. 15a shows this improved inverter efficiency at a switching frequency of 16 kHz as the output power varies, with more than 1 % improvement achieved when using the SiC devices at light loads. Fig. 15b and Fig. 15c show the corresponding reduction in device case and heat sink temperature that is achieved when using SiC devices with the same heat sink design.

B. Reduced cooling effort

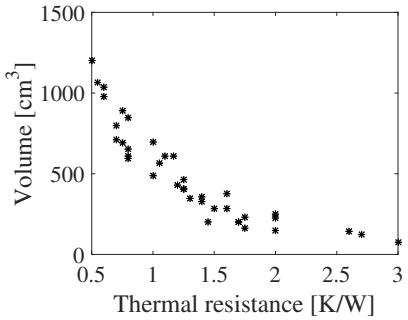
The increased efficiencies can be used to determine the cooling effort reduction and thereby consequently reducing the heat sink volume. Figure 16a shows a statistical representation of several naturally cooled heat sinks, with their volume plotted against the thermal resistance. In this work, the initial heat sink has a thermal resistance of 1.25 K/W resulting in a volume of 405 cm^3 , and the thermal resistance is increased up to 2 K/W. A direct size comparison of the two heat sinks used in this study is shown in Fig. 16b, with a thermal imaging of the corresponding device case temperatures operating at 1.5 kW presented in Fig. 16c. In particular, the heat sink volume is reduced by more than 60 % still ensuring safe thermal operation of all devices directly linking to increased inverter life expectancy at a smaller system volume.

C. Power rating improvements

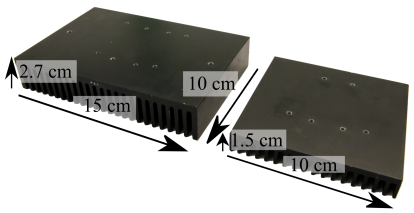
As it has been pointed out in this work, the DC bus connecting switching devices S_1 and S_4 represent the major loss contributor in overall device losses, thus they are a major limiting factor for the achievable converter output power. The loss reduction benefits of using SiC devices could therefore be used to increase the power rating of a given inverter, by increasing the available output power for the same cooling effort. Fig. 17a illustrates this potential by identifying that the output power can be increased from 1.5 kW using Si devices up to 2.5 kW using SiC devices for the same total semiconductor losses at a switching frequency of 16 kHz. For the particular inverter system investigated in this paper, this achieves an inverter power rating increase of more than 60 %, still ensuring all semiconductor devices operating within the thermal limits of 80 $^\circ C$ as shown in Fig. 17b.

D. Increased switching frequencies

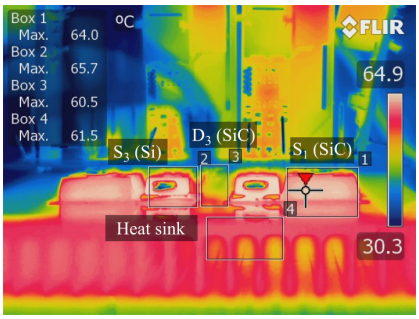
Finally, using the semiconductor loss modeling concepts presented in this paper, the inverter switching frequency when using SiC devices has been increased until the SiC semiconductor losses are the same as the Si semiconductor



(a) Heat sink volumes versus heat sink resistances



(b) Reduced heat sink size. 405 cm^3 against 150 cm^3



(c) Case temperatures for the SiC based inverter with the smaller heat sink

Fig. 16: Reduced heat sink size and resulting case temperature measurements

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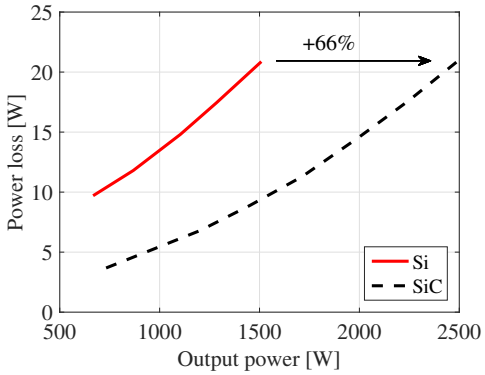
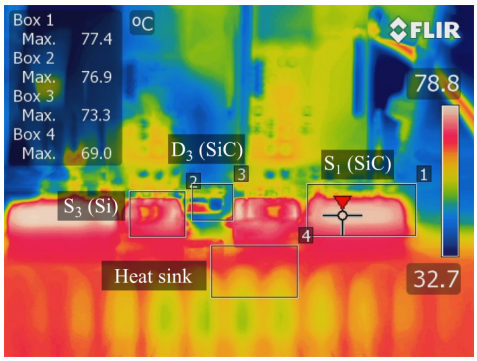
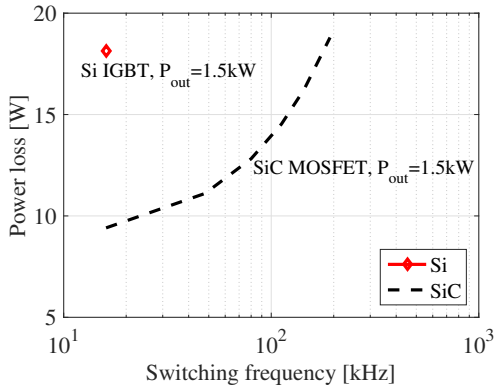


(a) Increased output power with SiC devices for the same semiconductor losses

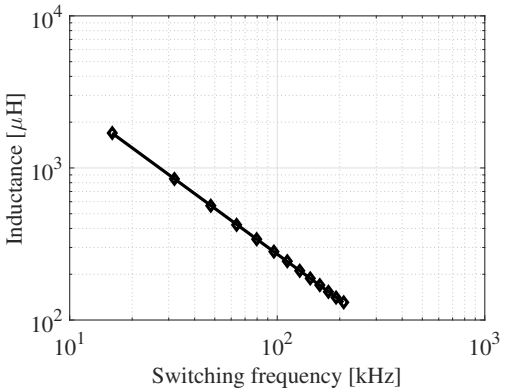


(b) Case temperatures for the SiC based inverter operating at 2.5 kW

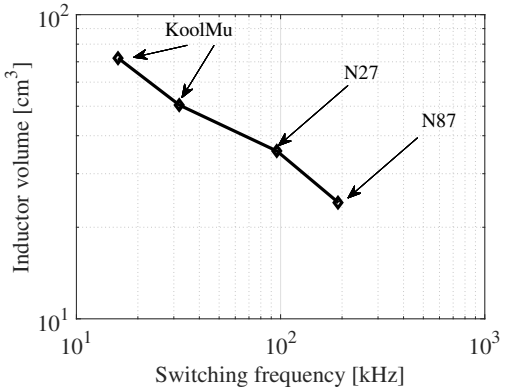
Fig. 17: Case temperatures for the SiC based inverter operating at increased output power levels



(a) Increased switching frequency with SiC devices for the same semiconductor losses



(b) Reduction of inductance against switching frequency



(c) Magnetic core volume reduction using different magnetic materials at different switching frequencies

Fig. 18: Converter side inductance reduction against switching frequency and possible magnetic core volumes for different switching frequencies

losses. The results are demonstrated in Fig. 18a, and show that for an output power of 1.5 kW, the switching frequency can be increased up to 192 kHz before this balance point is reached. This represents a 12 fold increase in switching frequency for the same losses. Such an increase in switching frequency can reduce the size of the filter inductance according to [33]

$$L = \frac{V_{DC}}{16 f_{sw} 0.2 \hat{I}} \quad , \tag{11}$$

following the conventional approach of limiting the inductor ripple current to 20 % of the peak load current $\hat{I}$. The results of this investigation are presented in Fig. 18b showing a reduction from initially 1.7 mH down to less than 140 µH which consequently reduces the inductor storage requirement. It must be kept in mind, though, that several trade-offs have to be made in the inductor design such as material dependent core losses, DC and AC copper losses and window utilization area which all affect the effective inductor volume, and that an optimized inductor considering all these parameters is beyond the scope of this work. Nevertheless, using core materials recommended for the operating frequency of interest in this work, Fig. 18c shows that the increase in switching frequency can have a significant effect on the magnetic core volume. For the considered cases, the magnetic core volume of initially 73 cm^3 when operating at 16 kHz can be reduced down to 24 cm^3 when increasing to a switching frequency of 192 kHz. A direct comparison for the two final inductors at low and high switching frequencies (the inductor for 16 kHz uses a thicker conductor attempting to reduce the expected dominant DC copper losses while the inductor for 192 kHz operation is designed with a minimum layer structure to reduce the AC resistance by reducing the layer to layer winding resistance) is shown in Fig. 19a, detailing an effective inductor volume reduction from 339 cm^3 down to 124 cm^3.

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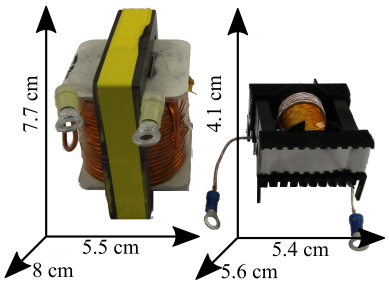
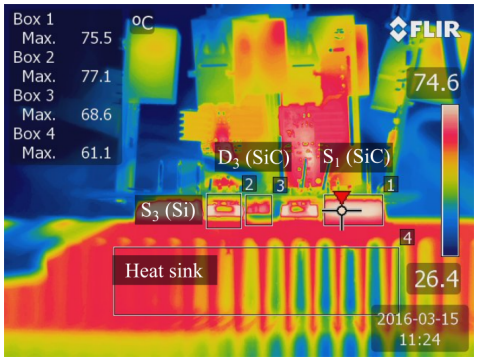


(a) Final inductor volume comparison



(b) Device case temperatures when operating at 192 kHz

Fig. 19: Inductor volume for low and high switching frequencies and device performance at 192 kHz

This consequently results in an inductor weight reduction; in this work from 950 g down to 174 g. A thermal imaging of the semiconductor device cases operating at 192 kHz is presented in Fig. 19b highlighting that the switching frequency can be significantly increased with an upgrade of only two semiconductor devices to SiC. Note that, although there are essentially no hard switched commutation losses in the inner bi-directional switches $S_{2,3}$ when the converter operates at unity power factor, there are still capacitive switching losses present due to a charge and discharge of the output capacitance, which becomes more visible at increased switching frequencies. Nevertheless, all devices (i.e. also the 600 V Si IGBTs) stay well within their thermal limits when the converter operates at a 12 fold increase in switching frequency.

VI. Conclusion

This paper has presented the results of an investigation into the benefits of using SiC MOSFETs in a three-level T-Type inverter. The challenge of measuring semiconductor losses within converter operating context, and thus validating established semiconductor loss models, has been addressed in this paper by presenting an alternative methodology of using thermal measurements taken from an experimentally calibrated heat sink at different power levels and switching frequencies for both Si and SiC based inverters. With the results of the thermal investigation, the major benefit of replacing the Si IGBT switching devices with SiC FETs for only two out of four total semiconductor switching devices per phase leg is verified when operating at or near unity power factor. With the substitution of only the DC bus connecting switching devices, the use of SiC MOSFETs can reduce the semiconductor losses by more than 50 % for similar rated devices operating under the same load conditions and switching frequency. Such a loss reduction gain offers several design opportunities. Firstly, if the inverter design specifications are kept the same, the reduced semiconductor losses can increase the overall inverter efficiency. Alternatively, if the switching frequency is kept the same as for an IGBT based inverter, the output power can be increased by up to 66 % for the same semiconductor losses. Finally, taking advantage of the superior switching characteristics of the SiC MOSFETs, the switching frequency can be increased by a factor of 12 while still achieving the same semiconductor losses as for an IGBT based inverter.

Of course it must be kept in mind that that the analysis presented here has only considered semiconductor losses for similarly rated devices, and there are many other factors such as device costs, passive filter components and packaging that must be taken into account when designing a complete inverter system. Nevertheless, the substantial loss benefits offered by the simple substitution of only two active switches per phase leg for the T-Type converter, and the relatively low cost implication of this substitution compared to the overall inverter cost, make it an attractive alternative to consider for this inverter topology.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2582344, IEEE Transactions on Power Electronics

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