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# Fabrication of Capacitive Micromachined Ultrasonic Transducers Using a Boron Etch-Stop Method

Søren Elmin Diederichsen\*, Filip Sandborg-Olsen\*, Mathias Engholm\*, Anders Lei\*,  
Jørgen Arendt Jensen†, and Erik Vilain Thomsen\*

\*Department of Micro and Nanotechnology, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

†Center for Fast Ultrasound Imaging, Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

**Abstract**—Capacitive Micromachined Ultrasonic Transducers (CMUTs) fabricated using Silicon-On-Insulator (SOI) wafers often have large thickness variation of the flexible plate, which causes variation in both pull-in voltage and resonant frequency across the CMUT array. This work presents a bond and boron etch-stop scheme for fabricating the flexible plate of a CMUT. The proposed fabrication method enables precise control of the plate thickness variation and is a low cost alternative to the SOI-based process. N-type silicon wafers are doped with boron to a surface concentration of  $> 10^{20} \text{ cm}^{-3}$  using solid planar diffusion predeposition at  $1125^\circ\text{C}$  for 30, 60, and 90 min. Process simulations are used to predict the boron doping profiles and validated with secondary ion mass spectrometry measurements. The doped wafers are fusion-bonded to a silicon dioxide surface and thinned down using an  $80^\circ\text{C}$ , 20 wt% potassium hydroxide solution with isopropyl alcohol added to increase the etch selectivity to the highly doped boron layer. The resulting plate thickness uniformity is estimated from scanning electron micrographs to a mean value of  $2.00 \mu\text{m} \pm 2.5\%$ . The resonant frequency in air for a 1-D linear CMUT array is measured to  $12 \text{ MHz} \pm 2.5\%$ . Furthermore, hydrophone measurements show that the fabricated devices can be used to emit sound pressure in the ultrasonic frequency domain.

## I. INTRODUCTION

The operation of Capacitive Micromachined Ultrasonic Transducers (CMUTs) for medical imaging essentially relies on the two-way energy transduction between the mechanical and electrical domains. During a pulse-echo sequence, this sets the need for a mechanical part that is able to exert a force on a medium and moreover convert the echoed pressure waves to a signal on the terminals. The mechanical component of a CMUT cell is a flexible plate in the  $0.1\text{-}20 \mu\text{m}$  thickness range [1], [2], [3], [4], [5].

CMUTs fabricated using the direct silicon fusion bonding technique [3] is prone to large thickness variations of the flexible plate, due to the chemical-mechanical polishing process used to define the device layer of certain Silicon-On-Insulator (SOI) wafers. For CMUT devices fabricated using the fusion bonding method, the flexible plate is typically made by etching away the handle and buried oxide layers of an SOI wafer (bonded to a substrate). Thus, any variance in the device layer will result in performance differences from one array and element to another and even on an intra-element level. Therefore, being able to predict and control the thickness variation of the plate is of great importance to fabricate devices with a predictable, uniform performance.

The influence of the plate thickness is directly seen in relation to the resonant frequency and pull-in voltage of a CMUT. In the case of an isotropic circular plate, the resonant frequency is directly proportional to the plate thickness,  $h$ , and the pull-in voltage depends on the plate thickness as  $\sqrt{h^3}$  [6], [7]. For an SOI wafer device layer thickness specified to  $2 \pm 0.5 \mu\text{m}$  ( $\pm 25\%$ ) this, theoretically, translates to a relative deviation of up to 25% in resonant frequency and 40% in pull-in voltage. For CMUT plates in the few-micrometer thickness range this means that the relative thickness variation becomes considerably large.

Several SOI wafer types are commercially available, including the Separation by Implantation of Oxygen (SIMOX), the SmartCUT™ and the bond and etch-back SOI wafer types. However, all of the aforementioned types limit the CMUT design space in some aspect, e.g. the impractically high implantation energies associated with thick device layers for the SIMOX type. This work presents an alternative method for fabricating the flexible silicon plate of a CMUT. The objective is to demonstrate the fabrication of CMUTs with excellent silicon plate thickness uniformity using a low-cost, bond and boron etch-stop technique.

## II. METHODS

The proposed CMUT fabrication method is illustrated as a simplified three-step procedure in Fig. 1. First, a  $p^{++}$  layer is made in a silicon wafer by means of diffusion. Next, the wafer is bonded to a substrate wafer containing cell cavities. Finally, the bonded wafer pair is submersed in a potassium hydroxide (KOH) solution to selectively remove the handle layer, leaving a highly conductive plate.

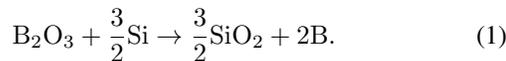
### A. The Boron Etch-Stop Layer

It has been shown that a highly doped p-type region in silicon serves as an etch-stop layer to some alkaline solutions [8]. A boron doped layer in silicon can be made using ion implantation, however, its applicability for deep implantations ( $> 2 \mu\text{m}$ ) is limited due to the very high energies required. In this work, the p-type etch-stop layer is created in double-side polished, 100 mm n-type silicon wafers by means of solid source doping with boron. Silicon wafers and boron source wafers are alternately placed in a silicon carbide carrier. This arrangement ensures doping on both sides of the silicon



Fig. 1. Three-step principle illustration of a boron-etch stop method for fabricating CMUTs.

substrate, allowing a symmetrical stress through the wafer, keeping the wafer bow at an acceptable level for the fusion bonding step. The carrier is placed in a furnace and heated to 1125 °C, at which the source wafers evolve boron trioxide ( $B_2O_3$ ) at a well-controlled rate. As this compound reaches the silicon surface, a borosilicate glass (BSG) layer is created. The boron oxide compound diffuses through the BSG layer and reacts with silicon at the Si/BSG-interface to create atomic boron [9]:



After the diffusion process, the BSG layer is removed with buffered hydrofluoric acid.

Fig. 2 shows the diffusion depths at various processing times at a constant temperature of 1125 °C and assuming a constant gas-source concentration. The data are extracted from a series of boron doping profiles using the process simulator ATHENA (Silvaco, Inc., USA). A spline interpolation is applied to each simulation to find the depth at which the simulated concentration reaches  $1 \times 10^{19} \text{ cm}^{-3}$ ,  $5 \times 10^{19} \text{ cm}^{-3}$  and  $1 \times 10^{20} \text{ cm}^{-3}$ , respectively. Notice the  $\sqrt{t}$  scale on the first axis and that the correlation between depth and time up to around  $t = 40$  min differs from the linear dependency expected from the diffusion-controlled nature of the physics governing the simulations. This is caused by an offset in dopant concentration due to temperature ramping before the actual diffusion step begins. The contribution is accounted for by adding a term,  $t_0$ , to the total diffusion time. Fits of  $\sqrt{k(t + t_0)}$  are included in the graph as dashed lines. Knowing the dopant concentration at which the etch-stop is consistently effective, the fitted relation in the figure can be used to predict the diffusion time required to achieve a certain diffusion depth, i.e. predict the resulting plate thickness.

From the work of Seidel et al. [8], a boron concentration of  $> 2 - 3 \times 10^{19} \text{ atoms/cm}^3$  is needed to achieve an effective etch-stop layer.

### B. Potassium Hydroxide Wet Etching

KOH is used as an etchant due to its high selectivity to highly doped p-type regions and was chosen over other etchants, because of its relative safety and availability. After

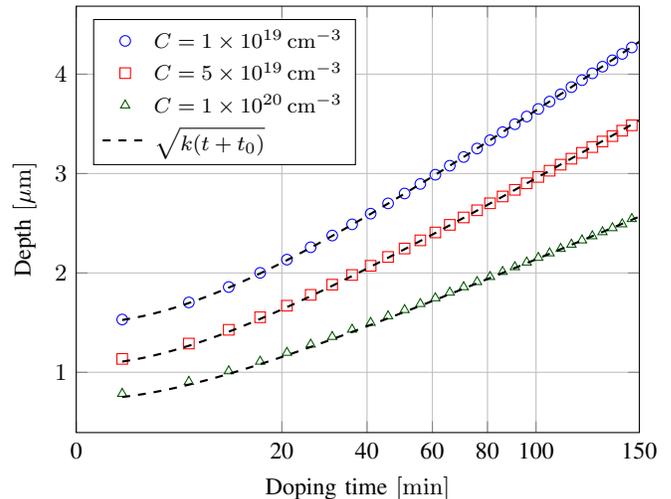


Fig. 2. ATHENA process simulations of the boron diffusion process at 1125 °C. Interpolation is used to find the depth at which the concentration is  $1 \times 10^{19} \text{ cm}^{-3}$ ,  $5 \times 10^{19} \text{ cm}^{-3}$  and  $1 \times 10^{20} \text{ cm}^{-3}$ , respectively. The data are plotted as the diffusion depth as function of  $\sqrt{t}$ . The non-linear relation for times up to  $t = 40$  min is due to dopant diffusion during the temperature ramping.

fusion bonding, the doped top wafer is thinned down in three steps (of which the first two are performed to lower the processing time): A reactive ion etch effectively removes the highly doped layer resulting from the double-side doping. Then, a rough thin-down is carried out using a 28 wt% KOH solution heated to 80 °C. Finally, the selective etch is achieved with a 20 wt% KOH solution heated to 80 °C and saturated with isopropyl alcohol (IPA) to increase the selectivity even further. The underlying theory behind the etching mechanism is treated in more detail in [8].

As the etching solution reacts with the silicon, hydrogen is evolving from the surface. Thus, visual inspection of when the hydrogen evolution stops reveals when the  $p^{++}$  layer has been reached.

Adding IPA to the solution has been reported in [10] to increase the  $p/p^{++}$  selectivity to the excess of 1:100 (at etching conditions comparable to those in this work). When etching with an IPA-saturated KOH solution it was observed that pyramidal hillocks occurred on the etched surface. This has also been observed by Peeters [11] and explained with the fact that a lowering in the etch rate between  $\langle 110 \rangle$  and  $\langle 100 \rangle$  planes is a natural consequence of the etching mechanism. This will allow small residues to initiate a pyramidal growth, which becomes larger as the etch progresses. In this context, the cleanliness of the deionised water used in the KOH solution has a significant effect. For this reason, the best results in terms of minimal pyramidal hillock formation was observed when the solution only was used for the processing of a single wafer.

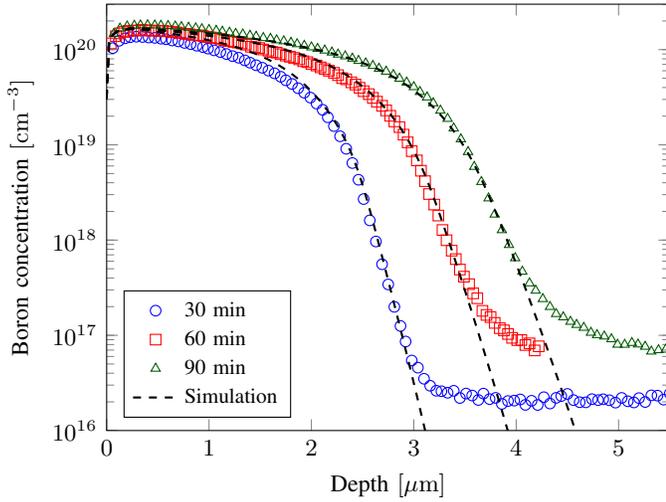


Fig. 3. SIMS measurements and ATHENA simulations of the boron diffusion profiles at a temperature of 1125 °C for diffusion times: 30, 60, and 90 min.

### III. RESULTS AND DISCUSSION

#### A. Doping Characterization

The resulting boron doping depth profiles and electrical properties are measured to assess the feasibility of the proposed method. Secondary Ion Mass Spectrometry (SIMS) is used to detect the surface composition of the doped silicon substrates. Fig. 3 shows the measured as well as simulated doping profiles at 1125 °C for three different predeposition times, namely 30, 60, and 90 min. The simulations show good agreement with the experimental observations, particularly on the steep part of the tail.

Furthermore, the sheet resistance of the boron-doped layer was measured at five different locations across a wafer with an average of approx.  $3.5 \Omega/\square$ , making it suitable to use as a top electrode of a CMUT.

#### B. Fusion Bonding Considerations

The diffusion process might introduce surface defects as well as surface stresses. Thus, to ensure a successful direct wafer fusion bonding it is necessary to assess the surface roughness and wafer bow.

A difference in covalent radii between silicon and boron atoms will result in a mismatch strain, which inevitably will cause the wafer to bow. To address this problem, the substrate wafers are doped on both surfaces to obtain a measured wafer bow of  $< 25 \mu\text{m}$ , which, from experience, is acceptable in order to achieve a successful fusion bonding.

The surface roughness after diffusion and BSG film removal was measured with Atomic Force Microscopy (AFM) to  $R_a = 0.16 \text{ nm}$ . It is worth noticing that the flow of oxygen during diffusion greatly influences the surface properties; a high oxygen flow rate will lower the surface roughness, but at the expense of reduced doping uniformity.

#### C. Plate Thickness

The plate thickness across a wafer was measured to  $2.00 \mu\text{m} \pm 2.5\%$  from Scanning Electron Microscope (SEM)

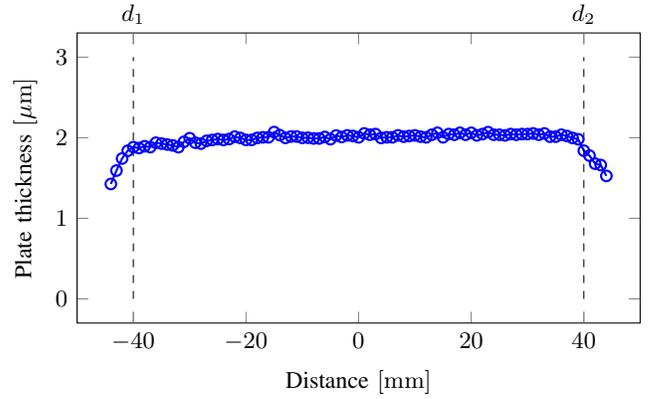


Fig. 4. SEM measured thickness of boron bond and etch-back fabricated CMUT plate across a 100 mm wafer. The mean thickness is  $2.00 \mu\text{m} \pm 2.5\%$  (extracted values between  $d_1$  and  $d_2$ ).

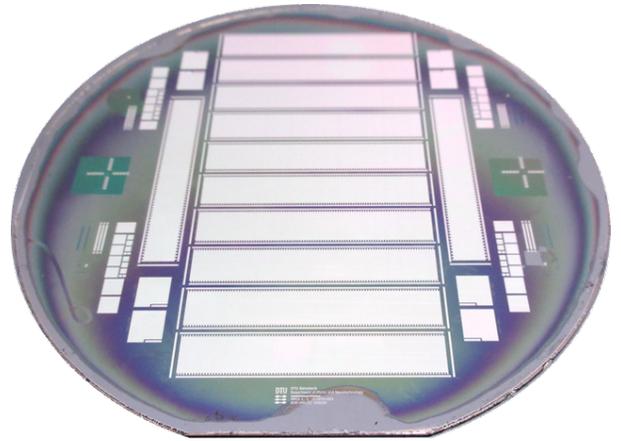


Fig. 5. CMUT device wafer fabricated using the proposed boron etch-back method. The wafer contains twelve 192-element, 1-D linear CMUT arrays.

images of cross sections near the bonding interface. The values are extracted between points  $d_1$  and  $d_2$  in Fig. 4. The distance between points  $d_1$  and  $d_2$  is 80 mm and represents the wafer area containing devices.

### IV. CMUT CHIP CHARACTERIZATION

Wafers with twelve 192-element, 1-D linear CMUT arrays were fabricated using the proposed boron etch-stop method in combination with two LOCOS processes [1]. Fig. 5 shows a photo of such a wafer. The CMUT element width is  $196 \mu\text{m}$  and the elevation height is 6 mm, each containing 450 closely packed CMUT cells of radius  $23.5 \mu\text{m}$  and a fill-factor of 67%. Each cell bump is  $2/3$  of the cell plate radius. A CMUT plate thickness of  $2 \mu\text{m}$  was desired to give a center frequency of 5 MHz in immersion and a pull-in voltage of 240 V. A CMUT array is mounted on a printed circuit board and coated with a flat 1 mm PDMS layer for electrical insulation (no lens effect), as previously described in [4]. This array is used for the acoustic characterization.

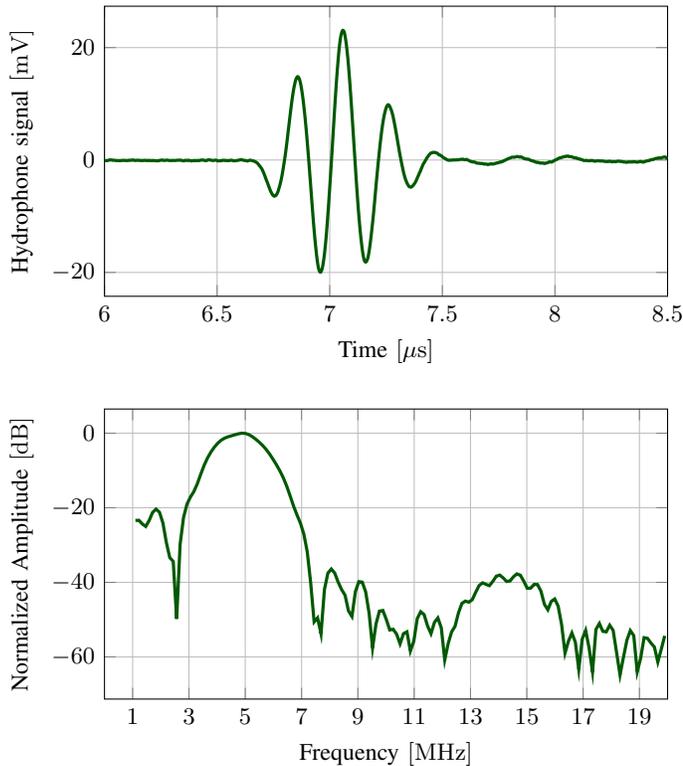


Fig. 6. Acoustic characterization of a CMUT fabricated with the proposed boron etch-stop method. A two-period, 5 MHz square pulse is used to excite a single element.

### A. Array Uniformity

A 4294A Precision Impedance Analyzer was used to measure the array uniformity on a bare CMUT array (no coating) in terms of the variation in resonant frequency in air for fifteen elements across the array. The result is  $12 \text{ MHz} \pm 2.5\%$  for the resonant frequency. This shows good agreement with the measured thickness, as it is within the plate thickness variation of  $\pm 3\%$ .

### B. Acoustic Performance

Hydrophone measurements were performed in a small water tank setup, using an Optel 10 MHz hydrophone (Optel Ultrasonic Technology, Poland). The CMUT is placed at a distance of 1 cm from the hydrophone surface. A bipolar square pulser from Hitachi (HDL6V5582) was used to send a two-period, 5 MHz excitation pulse for single-element emission. The resulting hydrophone response together with the fast fourier transform is plotted in Fig. 6. The high mechanical impedance of the CMUT results in almost no ringing. Notice the second harmonic suppression of approx.  $-50 \text{ dB}$  caused by the excitation pulse-shape, as explained in [5].

## V. CONCLUSION

An alternative method for fabricating the flexible plate of a CMUT is proposed. Process simulations are used to predict the boron doping profiles and subsequently supported by SIMS measurements. N-type silicon wafers are doped with boron

to a surface concentration of  $> 10^{20} \text{ cm}^{-3}$  and bonded to a substrate containing CMUT cell cavities. The handle part of the doped wafer is removed in a selective etch consisting of KOH saturated with IPA. The AFM-measured surface roughness of the doped silicon surface is  $R_a = 0.16 \text{ nm}$ , and the bow of the doped wafer before the fusion bonding step is  $< 25 \mu\text{m}$  across the wafer. SEM images of cross-sections near the bonding interface show a silicon plate mean thickness of  $2.00 \mu\text{m} \pm 2.5\%$ . Wafers containing CMUT devices are fabricated and acoustical characterization of the fabricated devices confirms the validity of the method. The resonant frequency in air is measured to  $12 \text{ MHz} \pm 2.5\%$ , showing excellent agreement with the variation of the plate thickness.

The proposed method enables precise control of the plate thickness variation and is a low-cost alternative to other methods prone to a large plate thickness variation. Furthermore, with a high degree of cleanliness this wet etch procedure allows for batch processing, making it a suitable method for large-scale production of highly doped flexible plates used as CMUT plate electrodes.

## VI. ACKNOWLEDGEMENT

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