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Comparative Evaluation of the Loss and Thermal Performance of Advanced Three Level Inverter Topologies

Alexander Anthon, *Member, IEEE*, Zhe Zhang *Senior Member, IEEE*, Michael A. E. Andersen, *Member, IEEE*, Donald Grahame Holmes, *Fellow, IEEE*, Brendan McGrath, *Member, IEEE*, Carlos A. Teixeira, *Member, IEEE*

Abstract—This paper presents a comparative evaluation of the loss and thermal performance of two advanced three-level inverter topologies, namely the partial SiC T-Type and the Hybrid-NPC, both of which are aimed at reducing the high switching losses associated with a conventional Si T-Type inverter. The first solution directly replaces the 1200 V primary Si IGBT switches with lower loss 1200 V SiC MOSFETs. The second solution strategically adds 600 V CoolMos FET devices to the conventional Si T-Type inverter to reduce the primary commutation losses. Semiconductor loss models, experimentally verified on calibrated heat sinks, are used to show that both variations can significantly reduce the semiconductor losses compared to the Si T-Type inverter. The results show that both alternatives are attractive if high efficiencies and reduced thermal stress are major requirements for the converter design.

Index Terms—T-Type, Hybrid-NPC, SiC MOSFET, Si IGBT, CoolMos

I. INTRODUCTION

Transformerless photovoltaic (PV) systems are becoming favored in the residential sector due to their reduced size, cost and higher efficiencies compared to transformer based alternatives [1]. To further improve low cost PV systems, previous research has intensively investigated the trade-offs between two- and three-level inverters and has found that three-level inverters have lower total semiconductor losses as the switching frequency increases, and also allow a significant size reduction in the AC filter [2], [3]. Within the three-level inverter alternatives, the Neutral-Point-Clamped (NPC) [4] and the T-Type [5] topologies are widely used which have the same voltage commutation requirements for their outer semiconductor devices, but their voltage blocking requirements are different, thus resulting in particular advantages and drawbacks for each topology. For example,

since the NPC inverter can use semiconductor devices that need to block only half the DC link voltage, its switching losses are always lower at any given switching frequency compared to the T-Type inverter, whose outer switches must block the whole DC link voltage; therefore, higher voltage class devices must be used, and hence incur higher switching losses. Nevertheless, the T-Type converter can still achieve lower total semiconductor losses compared to the NPC alternative due to its reduced conduction losses. Hence switching frequency is clearly a crucial parameter in this comparison [3]. Due to recent advances in new semiconductor devices such as silicon carbide (SiC), switching losses in a power converter can be significantly reduced compared to standard Si IGBT alternatives using these devices [6]–[8]. However, while the benefits and potential of these devices have been well reported [9]–[16], they have not become the standard choice in commercial systems yet and their utilization is still on-going process.

Another way to reduce the high switching losses in the T-Type inverter is to strategically add lower voltage switching devices in addition to the conventional T-Type circuit in order to manage the primary commutation events. This approach, called a Hybrid-NPC inverter, has been found to achieve higher efficiencies compared to a conventional T-Type structure with higher voltage (1200 V) Si IGBTs [17]. But to date, only few references are available on this topology alternative [17]–[19]. In particular a topological comparative evaluation of the loss and thermal performance between the Hybrid-NPC and the T-Type inverter using next generation switching devices such as SiC under exactly the same operating conditions is not known to the authors. This work therefore presents such a detailed loss comparison for these two advanced inverter alternatives targeting a residential PV system, using semiconductor loss models based on datasheet information (to calculate conduction losses), switching transition measurements (to calculate switching losses) and verification of the loss models thermally on calibrated heat sinks.

II. T-TYPE AND HYBRID-NPC INVERTER

The three inverter alternatives considered in this paper are shown in Fig. 1. Note that all topologies have in common to comprise a high voltage DC link with split bulk capacitors to obtain the required zero output state, and typically an

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A. Anthon, Z. Zhang and M. A. E. Andersen are with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark, (e-mail: jant@elektro.dtu.dk; zz@elektro.dtu.dk; ma@elektro.dtu.dk)

D. G. Holmes, B. McGrath and C. A. Teixeira are with the School of Electrical and Computer Engineering, RMIT University, Melbourne, VIC 3000, Australia (email: grahame.holmes@gmail.com; brendan.mcgrath@rmit.edu.au; carlos.teixeira@rmit.edu.au)

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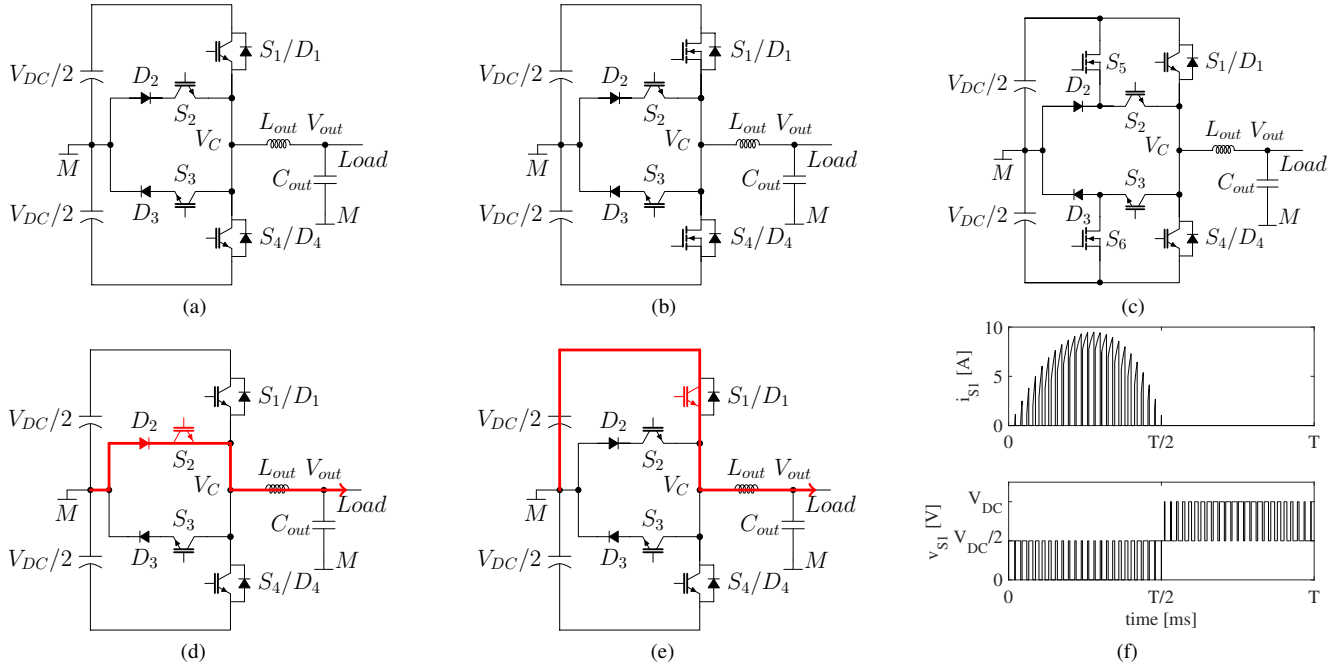


Fig. 1. Inverter alternatives used in this study, commutation scheme in T-Type inverter and voltage across and current through S_1 in T-Type inverter. (a) Si T-Type inverter. (b) Partial SiC T-Type inverter. (c) Hybrid-NPC inverter. (d) Zero output voltage and positive output current. (e) Positive output voltage and positive output current. (f) Voltage across and current through S_1 .

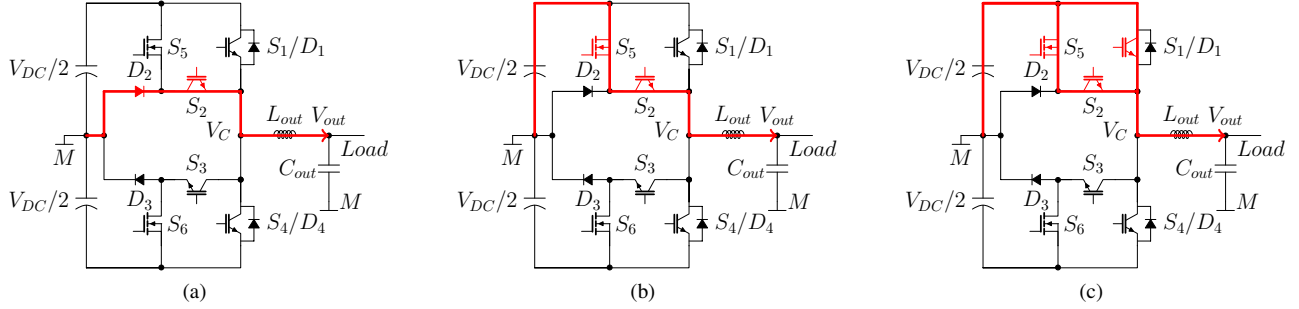


Fig. 2. Operation principle of Hybrid-NPC converter. (a) Zero output voltage and positive output current. (b) Positive output voltage and positive output current (NPC operation). (c) Positive output voltage and positive output current (Hybrid-NPC operation).

active voltage balancing control is thus required to stabilize the midpoint M which clearly increases complexity compared to their two-level alternative. The conventional Si T-Type structure shown in Fig. 1a is used as a reference. Its operational principle is illustrated in Fig. 1d-Fig. 1e. Initially, as shown in Fig. 1d, when a zero output voltage is required with a positive output current, diode D_2 and switch S_2 conduct this load current and the blocking voltage across both S_1 and S_4 is $V_{DC}/2$.

Then, to achieve a positive output voltage, switch S_1 turns on with a commutation voltage of $V_{DC}/2$ and the switching losses associated with this transition. Finally, a zero output voltage is re-established by turning switch S_1 off, with associated turn off losses for this transition. This process repeats throughout the positive fundamental half cycle as shown in Fig. 1f. Note that when the converter output voltage is switched to the positive DC rail, switch S_4 must block the whole DC link voltage, i.e. V_{DC} , which therefore requires S_4 to be rated to accommodate the full DC link voltage. A similar process occurs for the negative fundamental

half cycle, with diode D_3 and switch S_3 conducting current to achieve a zero output stage and switch S_4 turning on to achieve a negative converter output stage. Note that when the converter is switching during the negative half cycle, switch S_1 must now block the whole DC link voltage, as shown on the right half side of Fig. 1f. Since S_1 and S_4 need a higher voltage rating to block the whole DC link voltage, in contrast to the inner bi-directional devices D_2/D_3 and S_2/S_3 , which need to block only half the DC link voltage, their switching losses are a major contributor to the overall semiconductor losses. Hence they can be directly replaced with SiC switching devices as shown in Fig. 1b to reduce these switching losses, with the inverter's topological structure and thus its modulation principles unchanged.

Alternatively, additional low voltage rated switching devices S_5 and S_6 can be added into the circuit, as shown in Fig. 1c, to make a Hybrid-NPC structure. The switching principle of this inverter is a little different as shown in Fig. 2, in that one of either S_5 or S_6 turn on first to create the positive or negative output voltage as required. Since these devices need only be

rated to half the DC link voltage, their switching losses will be less than for a conventional T-Type inverter (600 V CoolMos FET devices are used in this work to minimize these switching losses). Once the switching transition is complete, current flows through the two devices S_5 and S_2 as shown in Fig. 2b (for a positive output voltage and current), which increases their conduction losses to a level similar to a conventional NPC inverter. Switch S_1 is then turned on (with almost zero switching losses), and the current flow changes to share between the two conduction paths as shown in Fig. 2c to achieve a similar conduction loss as for a standard T-Type inverter (since the forward voltage drop across S_1 is much the same as before).

The turn-off sequence for the Hybrid-NPC is in the reverse order, i.e. S_1 first turns off with essentially zero switching losses, and then S_5 turns off with appropriate losses against a commutation voltage of $V_{DC}/2$. The Hybrid-NPC converter shows a higher complexity, but can be advantageous in some cases. For instance, since the converter can generally be operated in both NPC and T-Type mode, a gate driver supply loss in S_1/S_4 would still have the converter operating in NPC mode. Also, as demonstrated in [17], a loss balancing control can be implemented to achieve an even temperature profile among the switching devices.

III. SEMICONDUCTOR DEVICE SELECTION

With the operation principles of the three inverter topologies identified, the selection of appropriate semiconductor devices for the topology comparison can now proceed. Since the targeted application for this topology is a grid-connected PV inverter system, the DC link voltage can go up to over 800 V. Thus a 1200 V rated device for S_1/S_4 is required. For this voltage range, the usual semiconductor device choice is Si IGBTs, which are known to have higher switching losses than either SiC based devices or CoolMos devices, particularly because of their relatively large turn off energies caused by their long delay tail currents. Fig. 4a and Fig. 4b illustrate this difference, showing the turn on and turn off switching energies for a 1200 V Si IGBT (S_1/S_4 in Fig. 1a), a 1200 V SiC MOSFET (S_1/S_4 in Fig. 1b) and a 600 V CoolMos (S_5/S_6 in Fig. 1c) for a junction temperature of 25°C and that were directly measured at appropriate voltages and currents for their T-Type inverter context, using the laboratory prototype shown in Fig. 3. The basis for the results presented in Fig. 4a and Fig. 4b is to measure voltage and current waveforms during a switching transition using an oscilloscope, and then to numerically integrate the product of these two waveforms to obtain the required switching energies. It is also advisable to conduct these measurements at different junction temperatures to account for the influence of the temperature on the switching energies, whose results for a temperature of 100°C are shown in Fig. 4d and Fig. 4e. It can be seen from these results that while the 1200 V Si IGBT turn on energies are not so much larger than the CoolMos device, both the CoolMos FET and the SiC MOSFET show a superior turn off switching loss behavior, and that mainly the turn off energies of the Si IGBT are affected by an increase in junction temperature. This is a

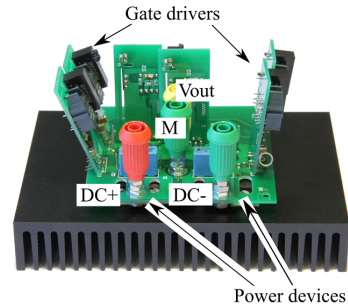


Fig. 3. Laboratory prototype

TABLE I
SEMICONDUCTOR DEVICES USED

	Si T-Type	SiC T-Type	Hybrid-NPC
S_1/S_4	IKW15N120T2	C2M0080120D	IKW15N120T2
S_2/S_3	IKP15N60T	IKP15N60T	IKP15N60T
D_2/D_3	C3D10060A	C3D10060A	C3D10060A
S_5/S_6			SPP20N60S5

particularly interesting observation since the turn off energies have been found to be the limiting factor for high efficient high switching frequency operation of the T-Type inverter [20]. Note also that since PV inverters operate mainly at unity power factor [21], the inner bi-directional device (S_2/S_3 in all topologies) switching losses will be essentially negligible and are therefore not included in this switching energy comparison.

To complete the switching device loss comparison, their forward conduction voltages can be taken from the manufacturer's datasheets. The results are presented in Fig. 4c, and show that the SiC MOSFET as a direct replacement to the 1200 V Si IGBT can also greatly reduce conduction losses over the current range of interest. Particularly at low currents, the SiC MOSFET shows a large voltage drop reduction due to its low on-state resistance, while the Si IGBT has a bipolar output characteristic and therefore a more constant and larger voltage drop. Fig. 4c also shows that the 600 V CoolMos device has a relatively large forward voltage compared to the SiC MOSFET due to its Si based semiconductor substrate, and that its on-resistance increases much more with an increase in junction temperature, as illustrated in Fig. 4f. Consequently, using the 600 V CoolMos device together with the 600 V Si IGBT to operate them in the conventional NPC converter (whose switching state is depicted in Fig. 2b) would result in large conduction losses compared to either the Si IGBT based T-Type structure or partial SiC T-Type structure. This is shown in Fig. 5, which details the forward voltages of 600 V CoolMos together with 600 Si IGBT operating in NPC mode against the 1200 V Si IGBT and the 1200 V SiC MOSFET for different current levels. Thus the Hybrid-NPC operation from Fig. 2c can reduce this large forward voltage by creating a current divider that clamps the total forward voltage to the voltage drop of the 1200 V Si IGBT (S_1/S_4) in Fig. 2c. Table I lists all semiconductor devices used in this comparison evaluation.

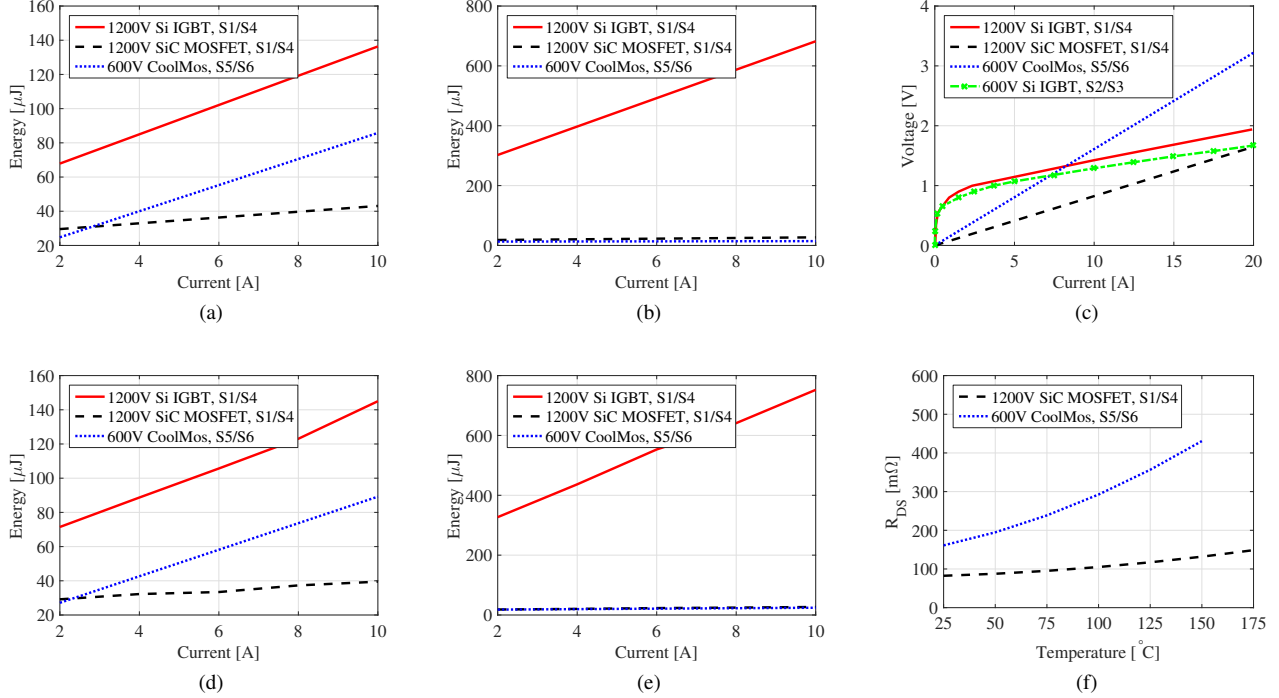


Fig. 4. Device characterizations for both low and high junction temperatures. (a) Turn on energies, 25 °C. (b) Turn off energies, 25 °C. (c) Forward voltages of the switching devices at 25 °C junction temperature. (d) Turn on energies, 100 °C. (e) Turn off energies, 100 °C. (f) On-resistance $R_{DS(on)}$ of both FET devices versus junction temperature.

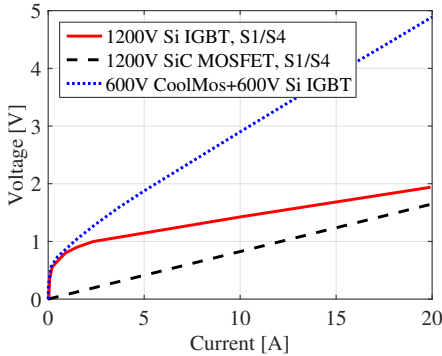


Fig. 5. Forward voltages for the different switch combinations at 25 °C junction temperature

IV. LOSS BREAKDOWN ANALYSIS

Once the device forward conduction and switching losses have been characterized for low and high junction temperatures, a loss breakdown analysis for their operation in the T-Type and Hybrid-NPC converter structures can be conducted. The IGBT conduction loss model is obtained using its dynamic on-resistance $r_{on,IGBT}$ and zero on-state voltage V_0 , i.e.

$$P_{con,IGBT} = V_0 I_{AV} + r_{on,IGBT} I_{rms}^2, \quad (1)$$

where I_{AV} and I_{rms} are the average and root-mean-square currents through the device. For the SiC MOSFET and the CoolMos FET, only their on-resistance $R_{DS(on)}$ is needed to

determine conduction losses, i.e.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2. \quad (2)$$

The conduction losses for the diodes are based on their threshold voltage V_T and dynamic on-resistance $r_{on,Diode}$, i.e.

$$P_{con,Diode} = V_T I_{AV} + r_{on,Diode} I_{rms}^2. \quad (3)$$

For the switching energies, Fig. 4a and Fig. 4b show that the switching losses for each device have a linear relationship to the switched current. Therefore, all switching energies can be modeled as a linear equation according to

$$E_{on,S1,4,5,6} = a_{on} i_{out}(t) mod(t) + b_{on} \quad (4)$$

$$E_{off,S1,4,5,6} = a_{off} i_{out}(t) mod(t) + b_{off} \quad (5)$$

where a_{on} , a_{off} , b_{on} and b_{off} are curve fitting constants for each device derived from the plots shown in Fig. 4. $i_{out}(t)$ is the AC load current and $mod(t)$ is the output voltage modulation function which is defined in the usual way as

$$mod(t) = M \sin(\omega t) \quad (6)$$

where M is the modulation index. The overall averaged switching losses can then be calculated as

$$P_{sw,S1,4,5,6} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{T/2} (E_{on,S1,4,5,6} + E_{off,S1,4,5,6}) dt \quad (7)$$

where φ is the phase shift (which is typically set to zero since PV inverters mainly operate at unity power factor [21]). Once these equations are established and the average and rms currents are determined either analytically or via simulations,

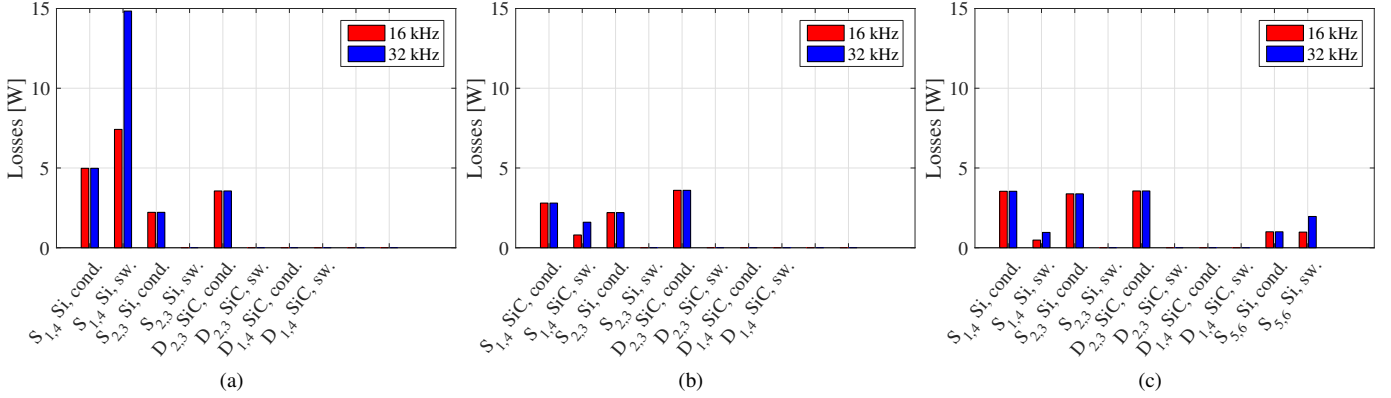


Fig. 6. Loss breakdown analysis for different inverter alternatives. DC link voltage $V_{DC} = 800$ V, filtered output voltage $V_{out,RMS} = 230$ V, output power $P_{out} = 1500$ W. (a) Si T-Type. (b) Partial SiC T-Type. (c) Hybrid-NPC.

the total semiconductor losses can be calculated for any given operating point, with an associated device loss breakdown. Fig. 6 shows this loss breakdown for the Si T-Type, the partial SiC T-Type and the Hybrid-NPC inverters with the specifications given in Table II, and operating at an output power of 1.5 kW. From the results presented in Fig. 6a, it can immediately be seen that even though the outer switch commutation voltage is only $V_{DC}/2$, switching losses in the 1200 V Si IGBT are the largest loss contributor to the overall semiconductor losses. Obviously, this effect becomes more severe as the switching frequency increases. Both the partial SiC T-Type and the Hybrid-NPC substantially reduce these switching losses as shown in Fig. 6b and Fig. 6c. In fact, for this particular example, at a switching frequency of 16 kHz chosen to reduce audible noise while keeping switching losses low, the switching losses in the 1200 V Si IGBT are still 7.4 W while the switching losses in the 1200 V SiC MOSFET are only 0.8 W and the switching losses using the 600 V CoolMos FET device are 1.1 W. The limitation of the switching frequency on the conventional T-Type structure becomes more evident as demonstrated in Fig. 6 for a switching frequency of 32 kHz. In order to adequately evaluate both topological alternatives, the total power stage losses for a particular operating point can then be obtained by summing up the individual device loss from the loss breakdown analysis in Fig. 6. For instance, total power stage losses at 16 kHz and 1.5 kW output power for the Si T-Type, the partial SiC T-Type and the Hybrid-NPC are 20.87 W, 8.8 W and 12.9 W, respectively. Note also that semiconductor losses are more evenly distributed among the devices for these two more advanced arrangements. Thus, both inverter variations are attractive alternatives compared to a conventional T-Type inverter structure when reduced semiconductor losses are an important factor.

V. LOSS MODEL VALIDATION BY THERMAL MEASUREMENTS

Since the losses and the loss reduction discussed in this paper relate only to the semiconductor devices, they can be readily validated experimentally. This was done using thermal measurements on the device heat sink since

TABLE II
INVERTER SPECIFICATIONS

Symbol	Meaning	Value
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, rms	230 V
f_{out}	Fundamental frequency	50 Hz
L_{out}	Filter inductor	3 mH
C_{out}	Filter capacitor	4.4 μ F
M	Modulation index	0.85

semiconductor device losses lead directly to an increased heat sink temperature. The semiconductor devices were mounted on a common heat sink, SK 58/100, which has a nominal thermal resistance of $R_{th} = 1.25$ K/W. To accurately match these temperature measurements to the semiconductor losses, the converter power stage was located inside an open ended chimney as shown in Fig. 7a. To minimize any thermal influence from the surrounding of the power stage (for instance gate driver circuitry), the heat sink was thermally decoupled from the rest of the power stage circuitry using a wooden panel as shown in Fig. 7b. Then, two temperatures are measured, one at the top of the heat sink T_{HS} and one below the heat sink giving T_{amb} , as shown in Fig. 7b. The difference between these readings gives the relative heat sink rise according to

$$\Delta T = T_{HS} - T_{amb} \quad (8)$$

To reduce the affect of sudden changes in the ambient temperature compared with the large time constant of the heat sink, a closed chimney for the measurements is recommended as shown in Fig. 7c. The measurement was used to carefully calibrate the heat sink using known DC loads. This was achieved by supplying the inverter with a known DC voltage and current (and hence power) with inverter switch states selected such that the semiconductor devices absorb all of the power supplied from the controlled DC source. This is exemplary illustrated in Fig. 8 for the switches of the Hybrid-NPC converter, i.e. S_5 , S_2 , S_1 and S_4 . The measurements were repeated for as many different switch pair combinations as possible (e.g. S_1 , S_3 and D_3 as a possible combination and D_2 , S_2 and S_4 as another possible combination), and the results for the different device pairs are

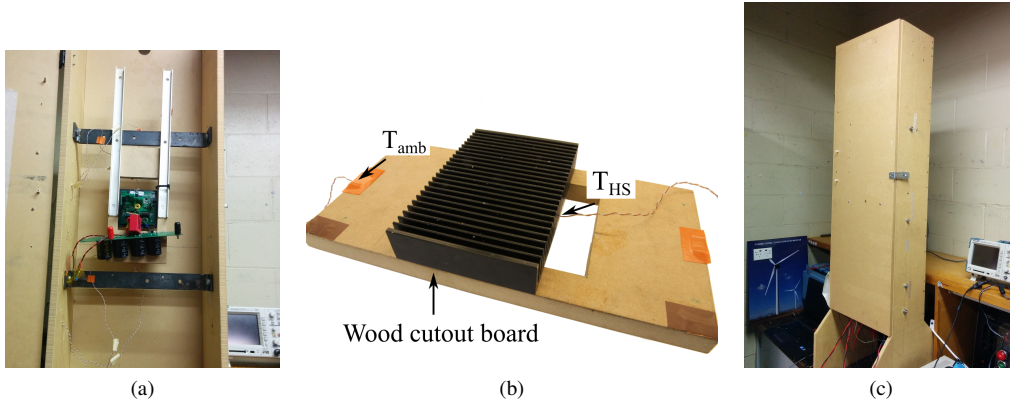


Fig. 7. Thermal measurement setup. (a) Converter placed in chimney. (b) Thermal measurements location. (c) Closed chimney to perform thermal measurements.

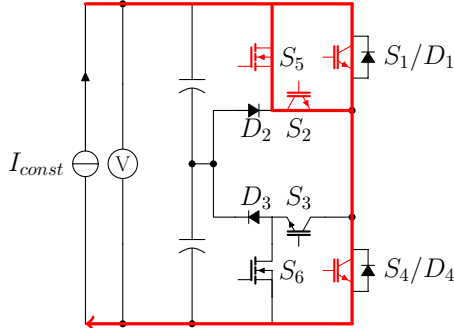


Fig. 8. Switch pair S_5 , S_2 , S_1 and S_4 are conducting

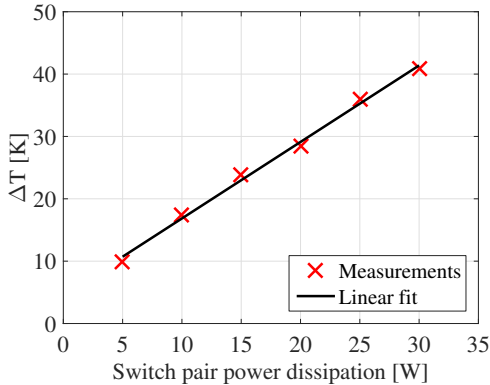


Fig. 9. Steady state heat sink temperature rise versus switch pair power dissipation

then averaged for a given power rating in order to achieve a well-defined temperature profile of the heat sink. The injected electrical power into the devices corresponds to the thermal energy forced into the heat sink, and is thus responsible for the heat sink temperature rise above ambient according to Eq. (8). Note that several calibration runs are necessary for different power levels to achieve a relation between the heat sink temperature rise and the power stage loss over a wide range of operating points. The results of this calibration procedure for device stage power losses up to 30 W are shown in Fig. 9 which will be used later to identify the device power stage losses when the topologies are operating in inverter mode.

VI. EXPERIMENTAL RESULTS

Once the calibration procedure was completed, the converters were then operated at a number of operating conditions to determine the aggregate semiconductor device losses. Operating the converter using phase disposition (PD) PWM [22], [23] with the parameter specifications provided in Table II, the resulting experimental output waveforms for a 230 V, 50 Hz system at 1.5 kW are shown in Fig. 10, where in particular Fig. 10b and Fig. 10c show the turn on and turn off commutations of the SiC MOSFET in the partial SiC T-Type inverter. The loss results for different operating conditions such as varying output power and switching frequency are shown in Fig. 11, where the predicted semiconductor losses are compared against the measured semiconductor losses. The results are clearly well within the measurement bounds of the experimental thermal measurement technique (the differential measurements from Eq. (8) with the thermocouples used are as accurate as $\pm 2^\circ\text{C}$ which translate to a measurement bound of up to ± 2.2 W). The results confirm that both the partial SiC T-Type inverter and the Hybrid-NPC inverter achieve a major loss reduction compared to the conventional Si T-Type inverter. More specifically, at 1.5 kW and 16 kHz, the Si T-Type inverter has total semiconductor losses of 22 W while the partial SiC alternative has only 9 W losses and the Hybrid-NPC converter shows semiconductor losses of about 13 W. This results in a loss reduction of around 60% for the partial SiC T-Type converter and 42% for the Hybrid-NPC. The results furthermore show that the Si T-Type inverter has the highest heat sink temperature rise above ambient at that operating point, shown in Fig. 12, where the heat sink temperature rises for each alternative are presented. In particular, for the Si T-Type inverter, the temperature rise of the heat sink above ambient is 31.8°C compared to only 14.6°C for the partial SiC T-Type alternative and 19.8°C for the Hybrid-NPC. Table III summarizes the losses, the loss reduction and the thermal performance for each topological alternative. Thus the loss reduction can not only be interpreted in terms of higher efficiency, but there is potential for further cost reduction by using a smaller heat sink. From a solely semiconductor device cost point of view, the loss reduction benefits of both advanced inverter alternatives are traded-off against an increased cost for the semiconductor devices. While the Hybrid-NPC structure

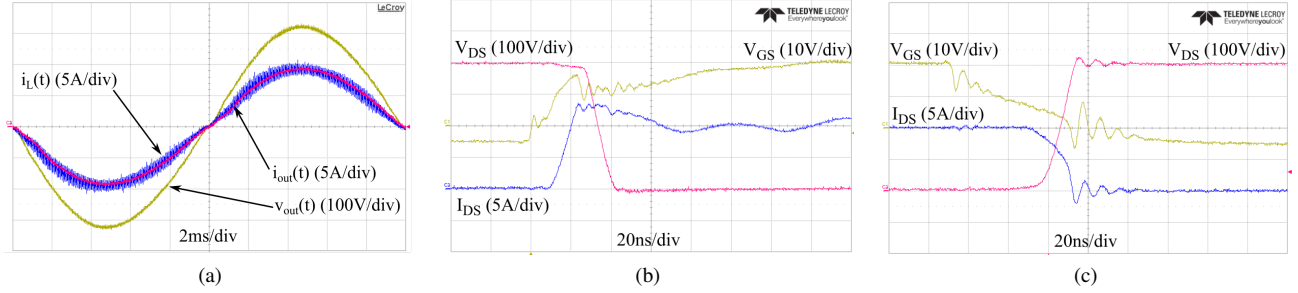


Fig. 10. Experimental converter waveforms. (a) Filtered output voltage and current waveforms. (b) Turn on transition of the 1200 V SiC Mosfet device in the partial SiC T-Type inverter. (c) Turn off transition of the 1200 V SiC Mosfet device in the partial SiC T-Type inverter.

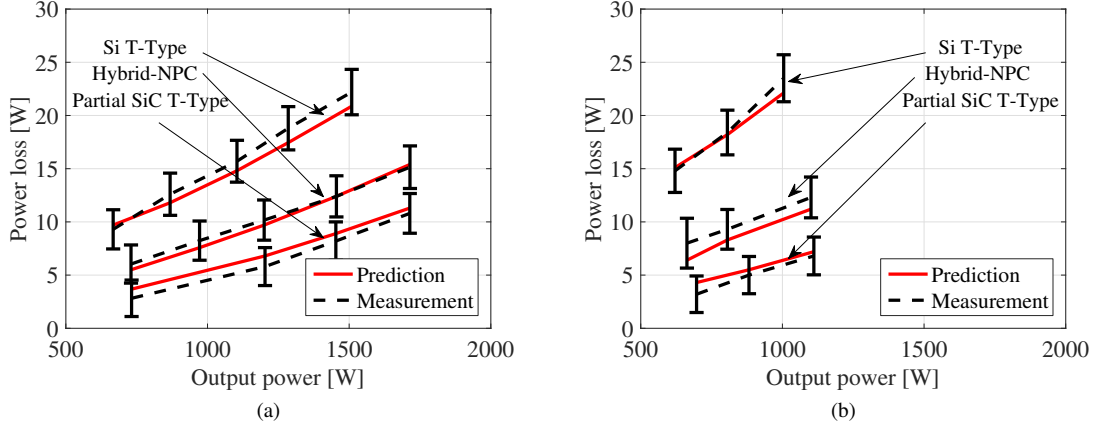


Fig. 11. Semiconductor losses experimentally obtained via thermal measurements. (a) Semiconductor losses at 16 kHz. (b) Semiconductor losses at 32 kHz.

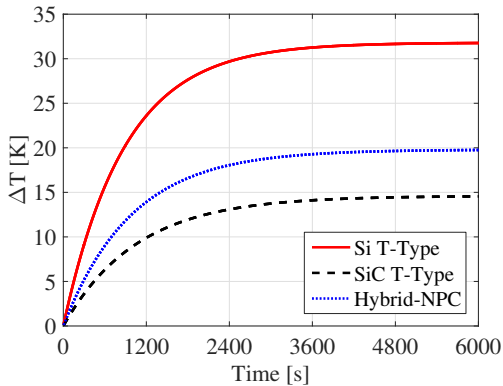


Fig. 12. Heat sink temperature rise of different inverter alternatives operating at 1.5 kW output power and 16 kHz switching frequency

TABLE III

SUMMARY OF EXPERIMENTAL RESULTS FOR DIFFERENT CONFIGURATIONS AT $P_{out} = 1.5$ kW AND $f_{sw} = 16$ kHz

	Losses [W]	Loss reduction [%]	Temp. rise [K]
Si T-Type	22.2	0	31.8
Partial SiC T-Type	9	-58	14.6
Hybrid-NPC	12.9	-42	19.8

is configured with silicon based devices only, the increased cost is caused by an increase in semiconductor device count as two additional semiconductor devices per converter leg are inserted. The partial SiC T-Type structure, on the other hand,

TABLE IV
PRICE CONFIGURATION FOR THE DIFFERENT ALTERNATIVES (OCTOBER 2016)

	Si T-Type	Partial SiC T-Type	Hybrid-NPC
$S_{1,4}$	IKW15N120T2 2x2.90 \$	C2M0080120D 2x15.62 \$	IKW15N120T2 2x2.90 \$
$S_{2,3}$	IKP15N60T 2x1.1 \$	IKP15N60T 2x1.1 \$	IKP15N60T 2x1.1 \$
$D_{2,3}$	C3D10060A 2x3.44 \$	C3D10060A 2x3.44 \$	C3D10060A 2x3.44 \$
$S_{5,6}$			SPP20N60S5 2x3.6 \$

shows the same device count as the conventional Si T-Type structure. However, the increased device cost is caused by the more expensive SiC material compared to Si to date [24]. This is illustrated in Table IV which shows the device cost for the configurations as presented in this paper.

VII. DISCUSSION

Two observations from Fig. 11 are worthy of further comment regarding the two converter alternatives. Firstly, while the Hybrid-NPC can substantially reduce its total semiconductor losses compared to the conventional T-Type inverter, its loss reduction is not as good as the partial SiC T-Type structure. This can be explained by recognizing that although the switching losses are greatly reduced for the Hybrid-NPC converter, its total semiconductor conduction losses are larger compared to the partial SiC T-Type inverter

because of the very low on-state resistance of the SiC MOSFETs as shown in Fig. 4c. Furthermore, from Fig. 2c, the conduction losses in the inner bi-directional switches S_2/S_3 are increased because they conduct current during both the zero converter output period and positive/negative converter output period.

The second observation relates to switching losses. As the switching frequency is increased, the power loss increase is larger for the Hybrid-NPC alternative compared to the partial SiC T-Type converter. This can be explained from Fig. 4a, which identifies larger turn on energies for the CoolMos FET relative to the SiC MOSFET. Therefore, at any particular switching frequency, switching losses in the Hybrid-NPC will be higher than the partial SiC T-Type inverter.

VIII. CONCLUSION

This paper has compared two promising three-level inverter topologies that aim to reduce switching losses compared to a conventional T-Type inverter structure. The first alternative is to simply replace the lossy 1200 V Si IGBTs with low loss 1200 V SiC MOSFETs. The second alternative strategically adds 600 V CoolMos FET devices to better support the switching transitions. A loss breakdown analysis using a loss model obtained from datasheet information and in-circuit measurement of switching events quantifies the loss reduction for both alternatives. In order to verify these semiconductor loss models, a thermal measurement technique was used based on calibrated heat sinks. The experimentally confirmed results show that a total semiconductor losses of 22.2 W for the Si T-Type inverter can be reduced down to 9 W for the partial SiC T-Type and 12.9 W for the Hybrid-NPC alternative. This yields a loss reduction of up to 58% using SiC MOSFETs and 42% for the Hybrid-NPC inverter. Furthermore, this loss reduction for both alternatives has the additional benefit of operating at a significantly lower temperature, which offers further potential for reduced heat sink costs and/or increased inverter life expectancy. The partial SiC T-Type converter could achieve the lowest losses in this analysis while keeping the converter complexity the same as for the Si T-Type structure, but it also showed the highest device cost for the given specifications for the achieved losses. The Hybrid-NPC comes with an increased level of complexity compared to the conventional T-Type structures, but can achieve a significant loss reduction with silicon devices only, which to date are less expensive compared to their similarly rated SiC devices.

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Alexander Anthon (S'10-M'15) received the B.Eng. degree from Flensburg University of Applied Sciences, Flensburg, Germany, in 2010, and the M.Sc. and the Ph.D. degrees from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2012 and 2015, respectively. During his Ph.D. studies, Dr. Anthon was a Visiting Scholar at the School of Electrical and Computer Engineering at RMIT University in Melbourne, Australia. His research interests include efficiency optimized DC/AC and DC/DC conversion using wide bandgap devices and digital control of grid-connected power conversion systems.



Zhe Zhang (M'11-SM'16) received the B.Sc. and M.Sc. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2010. He is currently an Associate Professor with the Department of Electrical Engineering, at the Technical University of Denmark. From 2005 to 2007, he was an Assistant Professor with Yanshan University. From June 2010 to August 2010, he was with the University of

California, Irvine, CA, USA, as a visiting scholar. He was a Postdoctoral Researcher and Assistant Professor at the Technical University of Denmark during 2011 and 2014. Since 2016 he has been an adjunct professor at Fuzhou University, China. He has authored or co-authored more than 100 transaction and international conference papers in his technical field. His current research interests include multiple-input dc-dc converters and multi-level dc-ac inverters for renewable energy systems (RES), hybrid electric vehicles (HEV) and uninterruptible power supplies (UPS); soft-switching power converters; piezoelectric actuator and transformer based power conversion systems.



Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark. Since 2009, he has been Deputy Head of Department at the Department of Electrical Engineering. He is the author or coauthor of more than 300 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor

correction, very high frequency power converters and switch-mode audio power amplifiers.



Donald Grahame Holmes (M'88-SM'03-F'13) received the B.S. degree and the M.S. degree in power systems engineering from the University of Melbourne, Melbourne, Australia, in 1974 and 1979, respectively, and the Ph.D. degree in PWM theory for power electronic converters from Monash University, Clayton, Australia, in 1998. In 1984, he joined Monash University, where he established and directed the Power Electronics Group for over 25 years. In 2010 he moved to RMIT University to take up a professorial chair in Smart Energy.

Professor Holmes has a strong commitment and interest in the control and operation of electrical power converters. His research interests include fundamental modulation theory and its application to the operation of energy conversion systems, current regulators for drive systems and PWM rectifiers, active filter systems for quality of supply improvement, resonant converters, current-source inverters for drive systems, and multilevel converters. He has made a significant contribution to the understanding of PWM theory through his publications and has developed close ties with the international research community in the area. He has been a member of the IEEE since 1987, has published well over 200 papers at international conferences and in professional journals, and regularly reviews papers for all major IEEE transactions in his area. He has also co-authored a major reference textbook on PWM theory with Prof. Thomas Lipo of the University of Wisconsin-Madison, Madison, WI, USA. Prof. Holmes is a member of the Industrial Power Converter and the Industrial Drive Committees of the IEEE Industrial Applications Society, and has held a number of positions on the Adcom of the IEEE Power Electronics Society over many years.



Brendan McGrath (M'99) received the BE degree in Electrical and Computer Systems Engineering (1997), the BSc degree in Applied Mathematics and Physics (1997), and the Ph.D. degree (2003) from Monash University, Victoria, Australia. Assoc. Prof. McGrath is with the school of electrical and computer engineering at RMIT university in Melbourne Australia. He has previously worked at Monash University, also in Melbourne, from 2007-2010, and the University of Newcastle in Australia from 2005-2006. Prior to this he was

a post-doctoral researcher with the Laboratoire d'Electrotechnique et d'Electronique Industrielle (LEEI), Toulouse, France. His research interests include the modulation and control of power electronic converters, with a particular emphasis on multilevel conversion systems. He has published over 100 journal and conference articles, and in 2004 was awarded the Douglas Lampard research medal from Monash University for his Ph.D. thesis. Assoc. Prof. McGrath is a member of the IEEE Power Electronics, Industry Applications and Industrial Electronics Societies, and is an associate editor for the IEEE Transactions on Power Electronics and the IEEE Transactions on Industry Applications.



Carlos Alberto Teixeira (S'11-M'14) received the B.S. and M.S. degrees in Electrical Engineering (2000 and 2008, respectively) from Santa Catarina State University (UDESC), Joinville, Brazil, and the Ph.D. degree in Electrical and Computer Engineering (2014) from RMIT University, Melbourne, Australia. Dr Teixeira is with the School of Electrical and Computer Engineering at RMIT University in Melbourne Australia. From 2000 to 2008, he was a Researcher at Whirlpool Corporation, Joinville, Brazil. From 1995 to 1999,

he was a member of the Tutorial Education Program (PET/SESu) in Electrical Engineering of UDESC. His research interests include the modulation and control of power electronic converters and the modeling and control of discrete event systems. He has published over twenty conference and journal articles and has coauthored two international patents.