An etching mask and a method to produce an etching mask

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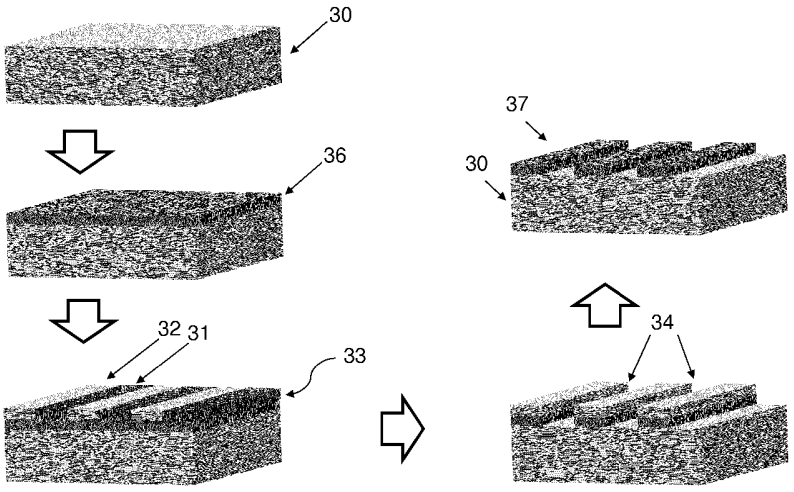

FIG. 1B

(57) Abstract: The present invention relates to an etching mask comprising silicon containing block copolymers produced by self-assembly techniques onto silicon or graphene substrate. Through the use of the etching mask, nanostructures having long linear features having sub-10 nm width can be produced.

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AN ETCHING MASK AND A METHOD TO PRODUCE AN ETCHING MASK

FIELD OF THE INVENTION

The present invention relates to an etching mask comprising silicon containing block copolymers, a system comprising the mask, a method to produce the etching mask, a nanolithographic method for producing nanostructures using the etching mask and a nanostructured substrate obtainable by the nanolithographic method.

BACKGROUND OF THE INVENTION

Block Copolymer (BCP) self-assembly techniques have been at the focus of R&D by micro and nanoelectronics semiconductor industries during the past 1-2 decades. BCPs are considered to be promising candidates for producing low cost and efficient electronic devices at small length-scales that begin to be both challenging and time consuming for conventional top-down nanolithography processes. It may be foreseen that highly expensive lithographic techniques will be replaced by the use of block copolymers in the form of soft masks in the production of electronic devices.

Generally, BCP systems need brush layers of either random copolymers or homopolymers in order to facilitate their directed self-assembly. In particular, brush layers may facilitate vertical alignment onto the underlying substrate. The vertical alignment allows for the formation of nanopatterns having lamellar (LAM) morphology and it facilitates a smooth etching process and the subsequent transfer of the desired pattern onto the substrate.

Normally, the deposition of brush layers is very time consuming, i.e. it needs at least a minimum of 3-4 hours including the annealing time required to anneal the brush polymer. Prior to that, the surface of the substrate, typically oxidized upper layer of Silicium wafers, needs to be activated by piranha solution to allow for the attachment of the brush layer. This also requires a minimum of 1 hour.

Thus, one of the main disadvantages of producing etching mask via self-assembly techniques is that a time consuming step in order to produce a brush layer is always needed to ensure a proper self-assembly and thus formation of the etching mask in itself.

Furthemore, while the surface modification with a brush layer is feasible on the oxidized upper layer of Silicium wafers or on other oxide surfaces, for a number of important substrates this is not even possible without compromising essential substrate properties. This is the case for example for graphene substrates. In such cases the general strategy has been to add a further step in the fabrication procedure, that is to cover the substrate with a 3-5 nm layer of SiO_2 by e.g. electron beam deposition prior to the application of the brush layer.
An additional step may be further needed in the case of nonoxide substrate surfaces, e.g. graphene.

A further disadvantage in producing nanostructured substrate by using soft etching masks is that this process can lead to formation of defects, such as poor protection of the substrate under the mask, presence of blunt edges and broadening of the sharp edges produced. These defects are created either during the etching process or following the removal of the etching mask. Nanostructured substrates presenting several defects may be not suitable for application within the semiconductor industry.

In general for applications within the semiconductor industry, nanostructured substrates having long linear features, e.g. silicon nanowires, which are easy and fast to produce, e.g. requiring less steps, are preferable. However, production of nanostructures having long linear features is not straightforward.

In particular, prior art within the field requires long annealing periods, of the order of magnitude of several hours, leading to long and inefficient method of production.

Hence, an improved etching mask would be advantageous, and in particular, an etching mask that is easier to be fabricated and that when used in a nanolitographic method is capable to produce narrow and defect free nanostructured substrates, would be advantageous.

OBJECT OF THE INVENTION

It is an object of the invention to provide an etching mask that is easy to produce.

It is a further object of the invention to provide an etching mask that when used in a nanolitographic process allows for production of nanostructured substrates suitable for applications in microelectronic industry.

It may be seen as another object of the invention to provide an etching mask that allows for the production of a nanostructured substrates that are defect free.

It is a further object of the present invention to provide an alternative to the prior art.

In particular, it may be seen as an object of the present invention to provide an etching mask, a method to produce the mask and a nanostructured substrate produced using the etching mask solving the above mentioned problems of the prior art.

SUMMARY OF THE INVENTION

Thus, the above described object and several other objects are intended to be obtained in a first aspect of the invention by providing a method of producing an etching mask on a surface of a substrate, the etching mask consisting of a silicon containing block copolymer, the method comprising: coating the surface of the substrate with a layer of a silicon containing block copolymer; controlling temperature in a range between 20 and 50 °C to the coated surface under a solvent environment; thereby producing said etching mask having a vertical structure, such as a vertical lamellar structure.

The specific steps of the method allow for the self-assembly of the etching mask having specific characteristics that allow the formation of a nanostructured substrate having a desired structure with specific length, width and period.

It can be appreciated that the method of the invention does not require the presence of a brushing layer onto the substrate before the self-assembly step. This provides a great advantage as reducing the complexity of the process required to produce the etching mask.

Thus in some embodiments the method of producing an etching mask on a surface of a substrate, consists of:

- coating said surface of said substrate with a layer of a silicon containing block copolymer;

- applying heat in a temperature range between 20 and 50 °C to said coated surface under a solvent environment; thereby producing said etching mask having a vertical structure such as a vertical lamellar structure.

Vertical structure is defined as a structure having a vertical alignment. For example vertically aligned cylinders with hexagonal dot morphology, may be a vertical structure. Vertical aligned lamellar structures, i.e. vertical lamellar structures may be also an example of vertical structures.

In some embodiments according to the first aspect the method produces a etching mask having a vertical and straight lamellar structure comprising lamellae having a orientational correlation length longer than 10 μm.

The etching mask is thus a layer or a coating deposited or located onto a surface of a substrate.

In a second aspect, the invention provides an etching mask consisting of a silicon containing block copolymer, the etching mask having a vertical lamellar structure In some embodiments, the etching mask comprises a vertical lamellar structure. In some other embodiments, the etching mask consists of a vertical lamellar structure.

In some embodiments according to the second aspect the etching mask has a vertical and straight lamellar structure comprising lamellae having a orientational correlation length longer than 10 μm.

In some further embodiments according to the second aspect the etching mask has a vertical and straight lamellar structure consisting of lamellae having a orientational correlation length longer than 10 μm.

The lamellar structure is composed of fine, alternating layers of polymers of the block copolymer system, in the form of lamellae.

The lamellar structure is vertical, thus comprising or consisting of lamellae that are perpendicular to the surface of the substrate on which the etching mask is deposited, i.e. by self assembling.

The vertical lamella structure or vertical alignment is essential to allow the production of a nanostructure on the surface of the substrate on which the etching mask is deposited. Indeed if the lamellar structure would self-assamble horizontally, thus parallel to the surface of the substrate on which the etching mask is deposited, no nanopatterning would be possible.

The lamellar structure may be straight, thus at least 90% of the mask comprises or consist of alternating parallel straight, i.e. linear, lamellae of the two polymers of the block copolymer.

The lamellar structures may be linear, thus has the form of a line, i.e. straight. The lamellar structure may not be curved or have a zero degree of curvature.

Straight may be also defined as a lamellar structure having lamellae having a high persistant or correlation length. For example a orientational correlation length longer than 50 times the thickness of the single lamellae. For example the orientational correlation length may be longer than 100 times the thickness of the single lamellae, such as longer than 1000 times the thickness of the single lamellae.

The orientational correlation length is related to the average of cos $\theta(s)$, where θ is the angle between unit tangent vectors in 2 points (0 and s) of the middle axisis of a lamella perpendicular to the substrate. The average of cos $\theta(s)$ is shown by $<\cos \theta(s)>$ and it generally decays exponentially with the contour distance s:

$$<\cos \theta(s)> = \exp(-s/l_0).$$

Where l_0 is defined as the orientational correlation length.

In other words the orientational correlation length is the length that until which a segment completely loses it starting direction.

An advantage of the straight lamellar structure of the etching mask of the invention is that through the use of the etching mask of the invention it is possible to produce on a substrate nanostructures having "high orientational correlation length". This is a key feature for application in electronic industry where nanostructures having straight and parallel linear structures at length scale exceeding few micrometers are crucial for electronic applications.

The silicon containing block copolymer comprises at least one polymer containing silicon, e.g. an organosilicon compound, commonly referred to as silicone.
The silicon containing block copolymer may have a low molecular weight.
The presence in the silicon containing block copolymer of a polymer having a low molecular weight allows for a unique self-assembly arrangement that lead to the formation of a monolayer characterized by a vertical and straight lamellar structure having lamellae of a orientational correlation length longer than 10 μm and having sub-10 nm width features.
Thus, the etching mask may consist of a self-assembled monolayer of the silicon containing block copolymer arranged in a lamellar fashion.
The self-assembled monolayer shows alternating lamellae of the two polymers, e.g. alternating lamellae of both polymers.

For example, the at least one polymer containing silicon of the silicon containing block copolymer may comprise a siloxane, such as Polydimethylsiloxane (PDMS).
The other polymer may be an aromatic polymer, such as polystyrene (PS).
Thus, the silicon containing block copolymer may be PS-*b*-PDMS.
Silicon containing block copolymers and in particular, PS-*b*-PDMS allow for the creation of a self-assembling structure comprising regular patterns, e.g. straight lamellar structures at very small scale.

In the silicon containing block copolymer, such as PS-PDMS, each block, i.e. PS or PDMS, may have a molecular weight between 1000 g/mol and 10000 g/mol, i.e. between 1K (kg/mol) and 10K, for example between 5000 and 5500, i.e. between 5K and 5.5K.
In the silicon containing block copolymer, such as PS-PDMS, each block, i.e. PS or PDMS may also have a molecular weight between 1000 g/mol and 25000 g/mol, i.e. between 1K (kg/mol) and 25K, e.g. between 1K and 10K.

In a preferred embodiment, the silicon containing block copolymer, such as PS-PDMS, may have a molecular weight between 10000 g/mol and 11000 g/mol, i.e. between 10K and 11K as the PS block has a molecular weight of 5K and the PDMS block has a molecular weight of 5.5 K.

Molecular weight for the block copolymer, accounting for the molecular weight of both polymers is herein referred to as the weight average molecular weight (Mw), also referred to as mass average molar mass or weight average molar mass.

Thus in some embodiments, the block copolymer PS-PDMS has a weight average molecular weight between 10000 and 11000.

In some other embodiments, the block copolymer PS-PDMS has a weight average molecular weight between 1000 and 25000.

The molecular weight of the block copolymer determines the width of the lamellar structured produced by the self-assembly.
Thus, the etching mask may consist of a self-assembled monolayer of PS-PDMS arranged in a lamellar fashion.
The self-assembled monolayer shows alternating lamellae of the two polymers, e.g. alternating PS and PDMS lamellae.
When the etching mask deposited on a substrate is exposed to plasma etching, plasma etching parameters may be controlled so as to remove only one of the two polymer, e.g. PS. Consequently, the area of the surface of the substrate underneath the removed polymer is exposed to plasma and thus subsequently etched.
When exposed to plasma PDMS has the further advantage of turning into a harder material. In this way PDMS turns into a hard and glassy mask that can better protect the surface of the substrate on which is deposited.
By using PDMS, only the area of the surface of the substrate underneath the removed polymer is etched by the plasma, while the area underneath the PDMS remain protected.
A regular and clear pattern is thus created on the surface of the substrate, which has the length and width of the removed PS polymer.

Due to the chemical nature of PDMS, which is quite different for carbon-based polymers, it is possible to obtain self-assembled monolayer even at rather low molecular weights (MW) of the block copolymers. And thus in turn, as molecular weight (MW) is connected to the width (d) of the lamellae, the presence of PDMS

allows for the formation of straight lamellar structure where the width of the PS polymer may be very limited, e.g. less than 10 nm, such as between 5 and 6 nm. As the width of the PS lamellae depends on its molecular weight, for lower molecular weights, pattern features of sub 10 nm may be foreseeable.

Thus, the PS-PDMS employed having low molecular weight, i.e. herein defined as PS-PDMS having a weight average molecular weight between 1000 and 25000, such as between 10000 and 11000, induce the formation of the desired straight vertical lamellar structure.

Phase separation in block co-polymers is a function of the product of the Flory-Huggins miscibility parameter multiplied by the total degree of polymerization N. The higher the value of this product the sharper interface between the two blocks, i.e. stronger segregation.

Thus, block co-polymers having a low Flory-Huggins miscibility parameter requires high total degree of polymerization, i.e. long chain and thus high molecular weight to produce ordered self assembled structure.

It has been found that in the case of PS-PDMS, the Flory-Huggins miscibility parameter is relatively high. Thus, the combination of PDMS with PS leads to a regular nanostructure having a vertical and straight lamellar structure having lamellae of a orientational correlation length longer than 10 μm, even very low molecular weight. This surprising effect allows in turn to produce linear patterns having very narrow width, i.e. sub 10-nm, orientational correlation length longer than 10 μm and periods below 20 nm, on a substrate where the self-assembled monolayer is used as etching mask.

In conclusion, the use of PDMS in this case has the further advantage when the etching mask is used in a nanolithographic process. PDMS exposed to oxygen plasma turn into a hard mask by partial oxidation, thus further protecting the area of the substrate located underneath. This allows for the production of nanostructured substrates that present very low defects.

The particular combination of a silicon containing block copolymer with PS allows for formation of self-assembled layers also at low molecular weight.

In some embodiments, according to the first aspect of the invention, the solvent environment is toluene environment.

In toluene environment, it was possible to obtain self-assembled structures showing straight lamellar structures having lamellae of a orientational correlation length longer than 10 μm.
Other solvent may be also used, e.g. other hydrocarbons, ethers or ketones.

In some embodiments according to the first aspect of the invention, the temperature range is between 30 and 50 °C, such as between 42 and 47 °C.

In some further embodiments, the temperature range is applied for a period of time between 10 seconds and 40 minutes, such as between 10 and 20 minutes. For example, the temperature range may be applied for not more than 15 minutes.
The application of the temperature within the period of time specified insure the formation of the desired straight lamellar structure having lamellae of a orientational correlation length longer than 10 μm. Application of the temperature range for shorter time period would not allow the formation of the desired structure. The possibility of producing the desired structure within the short time period specified is of great advantage as it allows reducing the time needed for the production.

In particular, annealing at 45 °C for 15 minutes under toluene environment have shown to be an optimal solvo-thermal technique procedure for the PS-PDMS self-assembly tested, providing the desired structure.

In a third aspect the invention relates to a system comprising: a substrate having a surface; an etching mask according to the second aspect of the invention deposited or located directly on the surface, thereby avoiding the need or presence of a brush layer.

The etching mask is deposited or located directly on the surface, i.e. no other layers are deposited or present between the substrate and the etching mask. Thus, the system may be referred to also as brushless.
As mentioned above, this provides a great advantage as reducing the complexity of the system that does not require the presence of a brushing layer onto the substrate before the self-assembly of the etching mask.

The substrate may be a semiconductor material, such as silicon.
An advantage of using a semiconductor material as a substrate is that through the mask of the invention it is possible to produce patterned features of the order of magnitude of 10 nm or below, with a period below 20 nm, and of a orientational correlation length of more than 10 μm; characteristics that are very relevant for electronic applications.

In a fourth aspect the invention relates to a nanolithography method of producing nanostructures having sub-10 nm feature size comprising: producing an etching mask on a substrate according to method of the first aspect of the invention; applying the etching mask to substrate to produce the nanostructures.

In some embodiments in the nanolithography method according to the forth aspect applying the etching mask to substrate to produce the nanostructures comprises: etching the substrate by means of plasma, such as oxygen plasma; and removing the etching mask.

In a further aspect the invention relates to a nanolithography method for producing nanostructures having sub-10 nm feature size comprising: producing an etching mask on a substrate according to method of the first aspect of the invention; using the etching mask for producing the nanostructures.

In a fifth aspect the invention relates to a nanostructure substrate obtainable by the nanolithography method of the fourth aspect of the invention, wherein the nanostructure substrate comprises linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 40 nm, such as below 20 nm.
The widths may be in the range between 1 and 20 nm ,such as between 9 and 15 nm, for example 10 nm.
The period may be below 20 nm, such as between 20 and 2 nm, for example between 15 and 7 nm.

In some other embodiments the substrate is graphene.
One of the advantages of the invention is that the method and the etching mask of the invention allow for graphene nanopatterning. Generally, graphene

nanopatterning using etching mask of block copolymer encounters several difficulties. In particular, nanopatterning using sacrificial soft mask templates is quite challenging. Firstly, lamellar self-assembly of block copolymers on top of a graphene surface is not easily achievable. Secondly, graphene is very sensitive to oxygen plasma and thus it is very difficult to selectively etching one of the polymers, e.g. PS, without creating defects in the pattern generated in the graphene. Thirdly, the further removal of the second polymer, e.g. PDMS, can produce further defects.

Through the etching mask, the system and the method of the invention it is possible to obtain a nanostructured graphene substrate having nanostructures with a very low level of defects as shown by Raman Spectroscopy spectra.

In some embodiments of the fifth aspect, the nanostructure substrate obtainable by the method of the fourth aspect of the invention the substrate is a graphene substrate and the nanostructure graphene substrate, when characterized by Raman Spectroscopy, shows a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2, thereby showing absence of defects.

Raman spectroscopy is a well known spectroscopic technique used to observe vibrational, rotational, and other low-frequency modes in a system.
Raman spectra of graphene surfaces are characterized by the presence of characteristic peaks.
Change of shape and intensity before and after the etching process is an indication of formation of defects; i.e. structural defects, such as broadening of the edges of the nanostructures produced.
On the contrary, formation of specific peaks, such as the D peak, having similar intensity of the G peak, following the etching process is in indication of lack of defects in the nanostructured graphene substrate.

In sixth aspect the invention relates to a nanostructure graphene substrate comprising linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 20 nm and wherein the nanostructure graphene substrate, when characterized by Raman

Spectroscopy, shows a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2, thereby showing absence of defects.

Defects are defined as depression throughout the surface area of the graphene that was previously protected by the PDMS hard mask.

The width of the G peaks is proportional to the width of the graphene nanoribbons produced on the substrate. Thus, the broader the G peak the smaller the width of the graphene nanoribbons produced due to the presence of defects on the graphene substrate.

In another aspect the invention relates to the use of an etching mask according to the second aspect of the invention in producing a nanostructured substrate comprising linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 20 nm.

In a further aspect the invention relates to the use of an etching mask according to second aspect of the invention in producing a nanostructured graphene substrate showing a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2, when characterized by Raman Spectroscopy.

The first, second, third and other aspects and/or embodiments of the present invention may each be combined with any of the other aspects and/or embodiments. These and other aspects and embodiments of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE FIGURES

The etching mask comprising silicon containing block copolymers, a system comprising the mask, a method to produce the etching mask, a nanolithographic method for producing nanostructures using the etching mask and a nanostructured substrate obtainable by the nanolithographic method according to the invention will now be described in more detail with regard to the accompanying figures. The figures show one way of implementing the present invention and is not to be construed as being limiting to other possible embodiments falling within the scope of the attached claim set.

Figure 1A is a graphical representation of the formation of the etching mask and of the nanostructure substrate according to some embodiments of the invention.

Figure 1B is a graphical representation of the formation of the etching mask on a graphene layer and the following nanostructure graphene substrate according to some other embodiments of the invention.

Figure 1C is a graphical representation of a top view of the nanostructed graphene surface produced on a silicon substrate as shown in figure 1B.

Figure 1D is a graphical representation of a top view of the nanostructed graphene surface showing defects.

Figure 2A is a Scanning Electron Microscopy (SEM) image of the etching mask of a brushless Lamellar phase self-assembly of PS-PDMS (5K-5.5k) deposited on a silicon substrate after PS removal.

Figure 2B is a SEM image of nanostructures on a silicon surface produced by using the etching mask of figure 2A.

Figure 3 shows Raman spectra of a graphene surface used as substrate, the same graphene surface after the deposition of the etching mask, and following the oxygen plasma etching process.

Figure 4 is a flow-chart of a method according to one aspect of the invention.

DETAILED DESCRIPTION OF AN EMBODIMENT

Figure 1A is a graphical representation of the formation of the etching mask and of the nanostructure substrate according to some embodiments of the invention.

Figure 1A shows a substrate 10, such as a silicon substrate, coated with a self-assembly monolayer of PS 11 and PDMS 12 alternating lamellae, thereby producing the etching mask 13.
Following plasma treatment, the PS 11 is removed and the silicon substrate 10 is etched producing trenches 14.
PMDS lamellæ 12 are then removed leaving a nanostructed silicon substrate 15.

Figure 1B is a graphical representation of the formation of the etching mask on a graphene layer and the following nanostructure graphene substrate according to some other embodiments of the invention.

Figure 1b shows a substrate 30, such as a silicon substrate, coated with a graphene mono-layer 36. The graphene surface is then coated with a self-assembly monolayer of PS 31 and PDMS 32 alternating lamellae, thereby producing the etching mask 33 on graphene 36.
Following plasma treatment, the PS 11 is removed and the graphene substrate 36 is etched producing trenches 14.
PMDS lamellæ 12 are then removed leaving a nanostructed graphene surface 37 on a silicon substrate 30.

Figure 1C is a top view of the nanostructed graphene surface 37 on a silicon substrate 30. It can be seen that the graphene nanoribbons 37 produced on the substrate 30 are continuos and without defects.

Figure 1D is a top view of the nanostructed graphene surface 47 on a silicon substrate 40. It can be seen that the graphene nanoribbons 47 produced on the substrate 40 have several defects 48.
It can be seen from figure 1C that defects are depression throughout, i.e. holes on, the surface area of the graphene that was previously protected by the PDMS hard mask.

Figure 2A is a Scanning Electron Microscopy (SEM) image of the etching mask of a brushless Lamellar phase self-assembly of PS-PDMS (5K-5.5k) deposited on a silicon substrate after PS removal.

Figure 2B is a SEM image of nanostructures on a silicon surface produced by using the etching mask of figure 2A.

Figure 3 shows Raman spectra of a graphene surface used as substrate, the same graphene surface after the deposition of the etching mask, and following the oxygen plasma etching process.
In figure 3 Raman spectrum 1 shows the initial Raman spectrum of a graphene substrate, showing only residual D and D' peaks due to the fabrication process, i.e. Chemical Vapour Deposition (CVD) technique. Spectrum 1 shows also G peak 4. The etching mask is then produced on the graphene surface by spin coating and annealing according to the method of one of the aspect of the invention. Raman spectrum 2 is then recorded, showing a decrease the 2D peak 5 due to doping effects and the deposits of amorphous carbon on top of the monolayer. After that the etching process by oxygen plasma is performed. Raman spectrum 3 shows a considerably increases the D peak 6 as a result of the ribbon creation. However, the graphene crystallinity within the ribbon is preserved as indicated by the robust 2D peak 7.
From Raman spectrum 3 it can be clearly seen that D peak 6 has an intensity similar to the one of G peak 7, thus the shows a ratio between D peak and G peak between 0.8 and 1.2. This confirm that even after etching and removal of the etching mask, the graphene surface is properly patterned and does not show presence of substantial defects.

Figure 4 is a flow-chart of a method according to one aspect of the invention. The nanolithography method 20 for producing nanostructures having sub-10 nm feature size comprises: S1 producing an etching mask on a substrate; S2 etching said substrate by means of plasma and S3 removing said etching mask.

Although the present invention has been described in connection with the specified embodiments, it should not be construed as being in any way limited to the presented examples. The scope of the present invention is set out by the accompanying claim set. In the context of the claims, the terms "comprising" or "comprises" do not exclude other possible elements or steps. Also, the mentioning of references such as "a" or "an" etc. should not be construed as excluding a plurality. The use of reference signs in the claims with respect to elements

indicated in the figures shall also not be construed as limiting the scope of the invention. Furthermore, individual features mentioned in different claims, may possibly be advantageously combined, and the mentioning of these features in different claims does not exclude that a combination of features is not possible and advantageous.

CLAIMS

1. A method of producing an etching mask on a surface of a substrate, said etching mask consisting of a silicon containing block copolymer, wherein said silicon containing block copolymer is Polystyrene- Polydimethylsiloxane (PS-PDMS), said method consisting of:

- coating said surface of said substrate with a layer of a silicon containing block copolymer;

- applying heat in a temperature range between 20 and 50 °C to said coated surface under a solvent environment;

thereby producing said etching mask having a vertical structure, such as a vertical lamellar structure, wherein said temperature range is applied for a period of time between 5 and 40 minutes, such as between 10 and 20 minutes.

2. A method according to claim 1, wherein said solvent environment is toluene environment.

3. A method according to any of the preceding claims wherein said temperature range is between 30 and 50 °C, such as between 42 and 47 °C.

4. A method according to any of the preceding claims, wherein said PS-PDMS has a weight average molecular weight between 1000 and 25000.

5. A method according to claim 4, wherein said PS-PDMS has a weight average molecular weight between 10000 and 11000.

6. An etching mask consisting of a silicon containing block copolymer said mask having a vertical structure,wherein said silicon containing block copolymer is Polystyrene- Polydimethylsiloxane (PS-PDMS).

7. An etching mask, according to claim 6, wherein said PS-PDMS has a weight average molecular weight between 1000 and 25000.

8. An etching mask, according to claim 7, wherein said PS-PDMS has a weight average molecular weight between 10000 and 11000.

9. A system comprising:

- a substrate having a surface;

- an etching mask according to any of the claims 6-8 deposited directly on said surface, thereby avoiding the need of a brush layer, wherein said substrate is graphene.

10. A nanolithography method of producing nanostructures comprising:

- producing an etching mask on a substrate according to method of any of claims 1-5;

- applying said etching mask to substrates to produce said nanostructures.

11. A nanolithography method according to claim 10, wherein said applying said etching mask to substrates to produce said nanostructures comprises:

- etching said substrate by means of plasma

- removing said etching mask.

12. The use of an etching mask according to any of the claims 6-8 in producing a nanostructured substrate comprising linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 20 nm.

13. The use of an etching mask according any of the claims 6-8, in producing a nanostructured graphene substrate showing a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2, when characterized by Raman Spectroscopy.

14. A nanostructured substrate obtainable by the method according to any of the claims 10 or 11, comprising linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 20 nm.

15. A nanostructured substrate obtainable by the method according to any of the claims 10 or 11, wherein said substrate is a graphene substrate and wherein said nanostructure graphene substrate, when characterized by Raman Spectroscopy,

shows a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2.

16. A nanostructured graphene substrate comprising linear structures having widths in the range between 5 and 20 nm, orientational correlation length longer than 10 μm and a period below 20 nm and wherein said nanostructure graphene substrate, when characterized by Raman Spectroscopy, shows a ratio of the D peak over the G peak between 0.2 and 4, such as between 0.8 and 1.2.

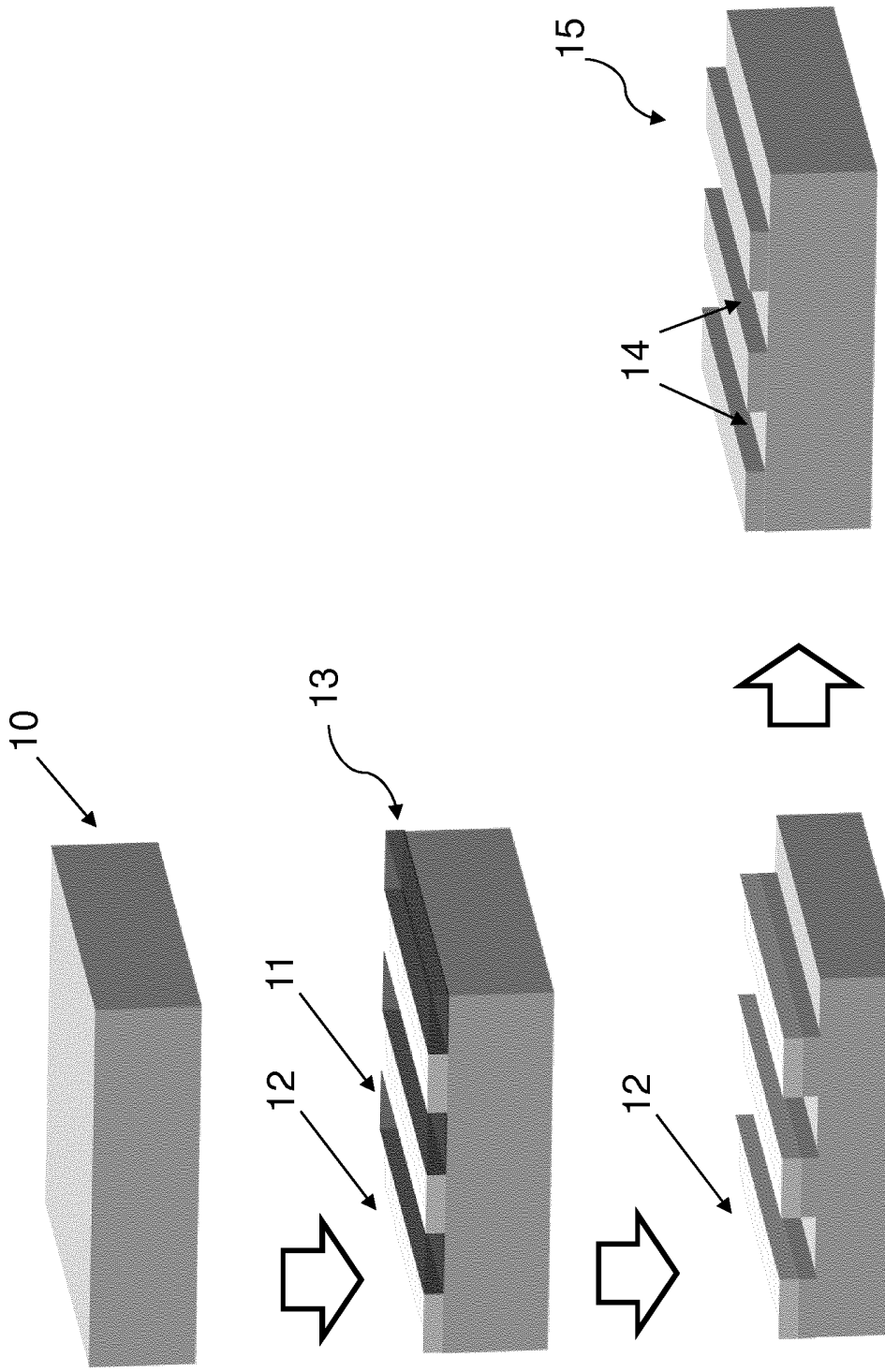

FIG. 1A

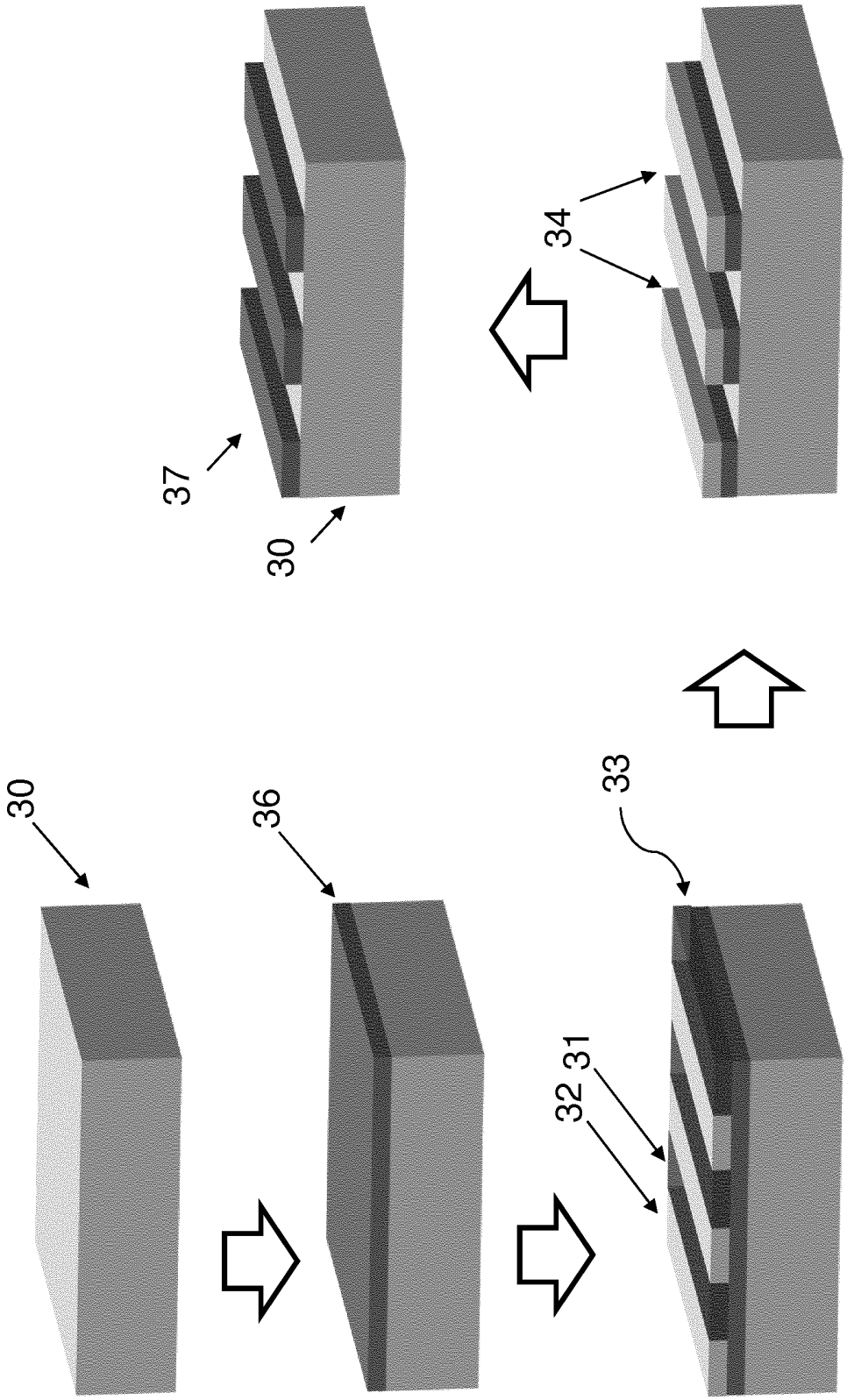

FIG. 1B

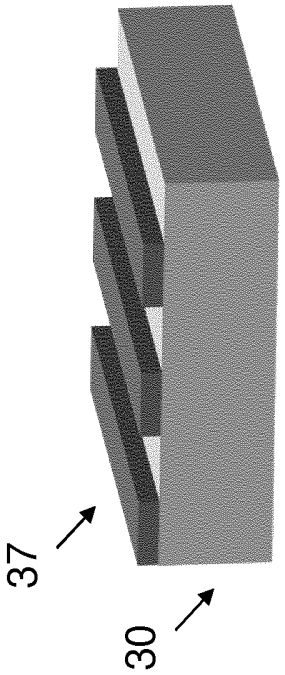

FIG. 1C

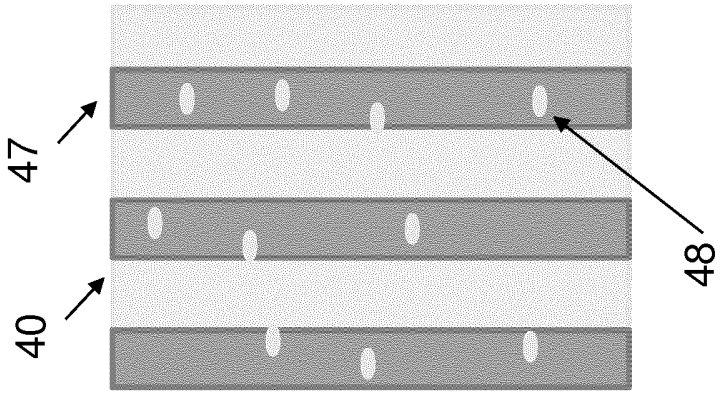

FIG. 1D

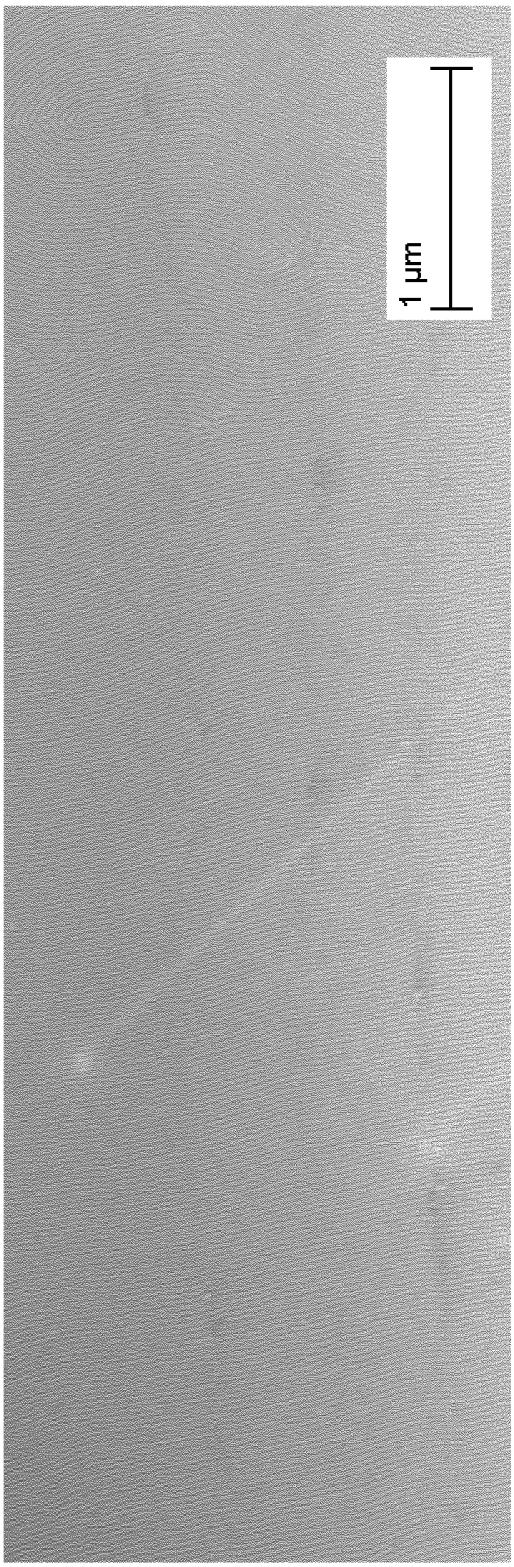

FIG. 2A

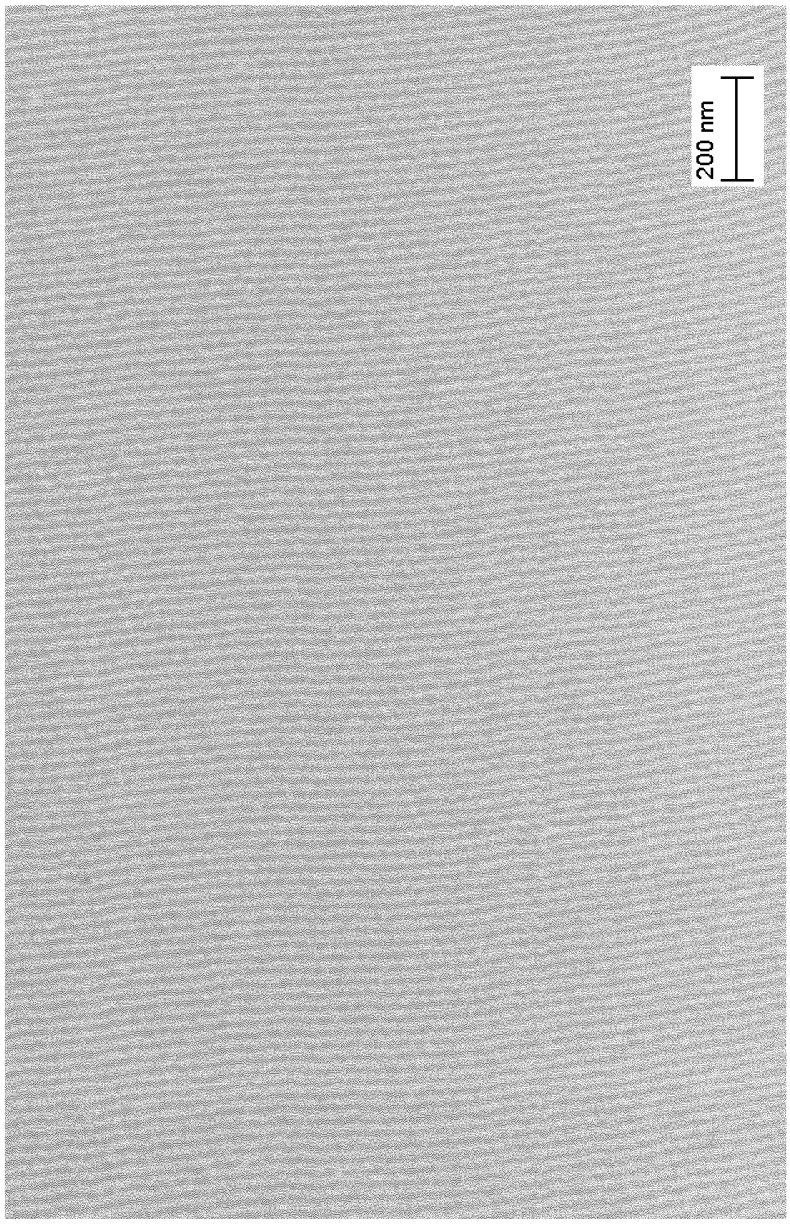

FIG. 2B

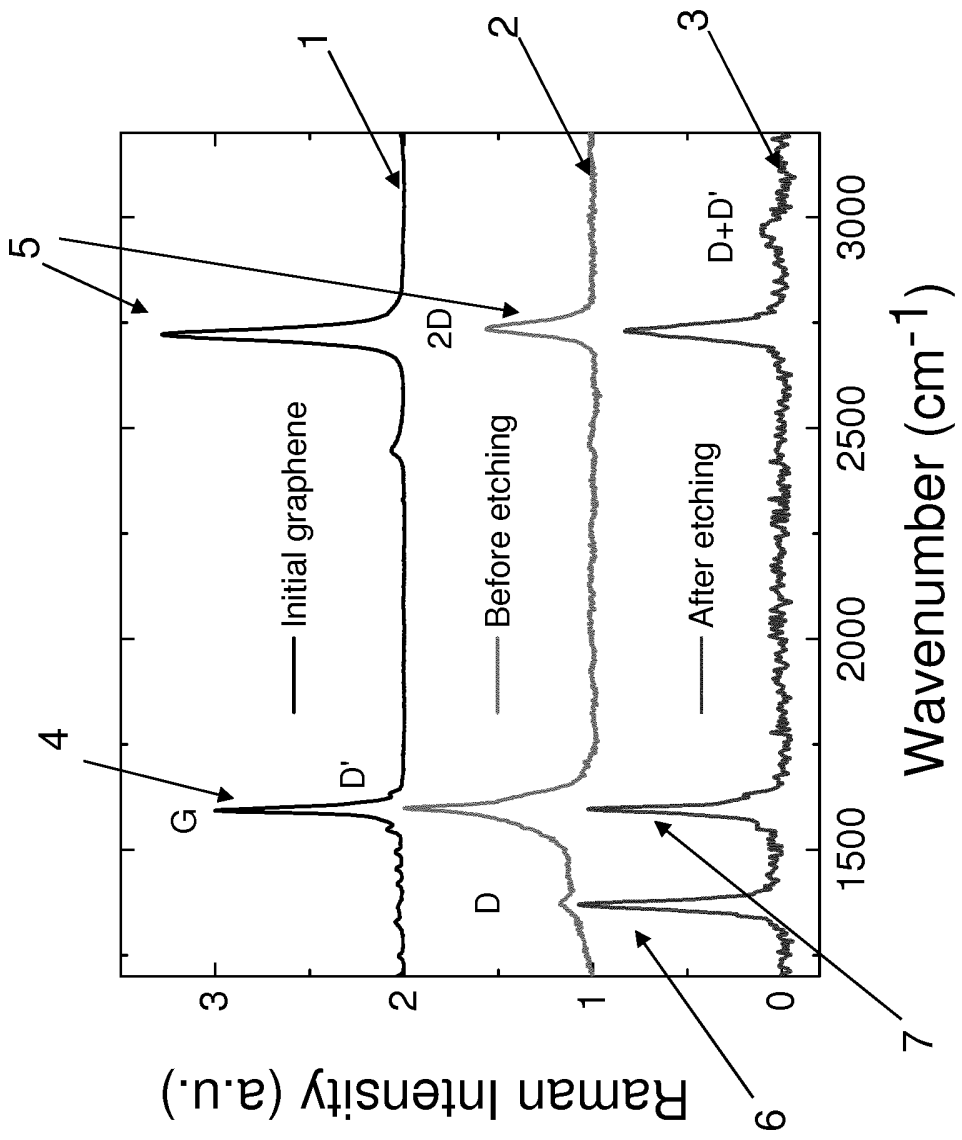
Raman Intensity (a.u.)
Wavenumber (cm-1)
Initial graphene
Before etching
After etching
G
D'
2D
D
D+D'
1
2
3
4
5
6
7
0
1
2
3
1500
2000
2500
3000

FIG. 3

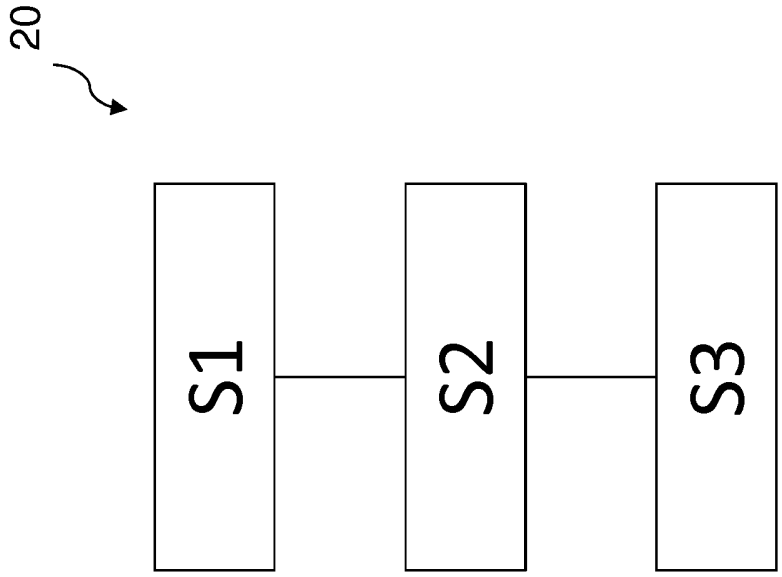

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/060205

A. CLASSIFICATION OF SUBJECT MATTER
INV. C08L83/00 C09D153/00 G03F7/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C08L C09D G03F B82Y

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 2012/071330 A1 (DOW CORNING [US]; KIM GINAM [US]; SWIER STEVEN [US]) 31 May 2012 (2012-05-31) paragraphs [0059], [0069], [0071], [0075], [0079] -----	1-3,6, 10-12 4,5,7,8
X	BORAH D ET AL: "Block Co-Polymers for Nanolithography: Rapid Microwave Annealing for Pattern Formation on Substrates", POLYMERS MDPI AG SWITZERLAND, vol. 7, no. 4, April 2015 (2015-04), pages 592-609, XP002758706, ISSN: 2073-4360 paragraph [03.2]; figure 2 -----	1,6,10
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2016	17/08/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Pérennès, Frédéric

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/060205

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/209755 A1 (HUSTAD PHILLIP DENE [US] ET AL) 15 August 2013 (2013-08-15) page 7, lines 12,13 page 8, lines 3,4	4,5,7,8
X	KR 2012 0112924 A (KOREA ADVANCED INST SCI & TECH [KR]) 12 October 2012 (2012-10-12) paragraph [0014]; figures 2,4	9,13,15
X	NILADRI PATRA, BOYANG WANG, AND PETR KRA'L: "Nanodroplet Activated and GuidedFolding of Graphene Nanostructures", NANOLETTERS, vol. 9, no. 11, 23 October 2009 (2009-10-23), pages 3766-3771, XP002758707, page 3766, column 1	14,15

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2016/060205

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15

An etching mask consisting of
Polystyrene-Polydimethylsiloxane copolymer having a weight average molecular weight between 1000 and 25000 g/mol.

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2. claim: 16

A nanostructured graphene substrate.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2016/060205

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2012071330 A1	31-05-2012	CN 103221487 A	24-07-2013
		EP 2643413 A1	02-10-2013
		JP 2014505119 A	27-02-2014
		KR 20140024256 A	28-02-2014
		US 2013231438 A1	05-09-2013
		WO 2012071330 A1	31-05-2012
US 2013209755 A1	15-08-2013	CN 103304725 A	18-09-2013
		JP 2013166934 A	29-08-2013
		KR 20130094264 A	23-08-2013
		TW 201343691 A	01-11-2013
		US 2013209755 A1	15-08-2013
KR 20120112924 A	12-10-2012	NONE	