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Soprani, Stefano; Haertel, Jan Hendrik Klaas; Lazarov, Boyan Stefanov; Sigmund, Ole; Engelbrecht, Kurt

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A Design Approach for Integrating Thermoelectric Devices Using Topology Optimization

S. Soprani^{*a}, J. H. K. Haertel^a, B. S. Lazarov^b, O. Sigmund^b, K. Engelbrecht^a

^a Department of Energy Conversion and Storage - Technical University of Denmark.

^b Department of Mechanical Engineering - Technical University of Denmark.

* Frederiksborgvej 399 - Building 778, 4000 Roskilde, Denmark, stefs@dtu.dk

ABSTRACT

Efficient operation of thermoelectric devices strongly relies on the thermal integration into the energy conversion system in which they operate. Effective thermal integration reduces the temperature differences between the thermoelectric module and its thermal reservoirs, allowing the system to operate more efficiently. This work proposes and experimentally demonstrates a topology optimization approach as a design tool for efficient integration of thermoelectric modules into systems with specific design constraints. The approach allows thermal layout optimization of thermoelectric systems for different operating conditions and objective functions, such as temperature span, efficiency, and power recovery rate. As a specific application, the integration of a thermoelectric cooler into the electronics section of a downhole oil well intervention tool is investigated, with the objective of minimizing the temperature of the cooled electronics. Several challenges are addressed: ensuring effective heat transfer from the load, minimizing the thermal resistances within the integrated system, maximizing the thermal protection of the cooled zone, and enhancing the conduction of the rejected heat to the oil well. The design method incorporates temperature dependent properties of the thermoelectric device and other materials. The 3D topology optimization model developed in this work was used to design a thermoelectric system, complete with insulation and heat sink, that was produced and tested. Good agreement between experimental results and model forecasts was obtained and the system was able to maintain the load at more than 33 K below the oil well temperature. Results of this study support topology optimization as a powerful design tool for thermal design of thermoelectric systems.

KEYWORDS: Topology Optimization; Thermoelectric Devices; Thermoelectric Cooling; System Integration; Thermal Management; Downhole Electronics Cooling.

1. INTRODUCTION

Over the past decades, thermoelectric devices (TEDs) have become competitive solutions for waste energy recovery, heat pumping, and cooling applications [1-5]. Advantages of TEDs include compactness, gas-free solid-state operation, lack of moving parts, and long life-span. However, a lower energy conversion efficiency compared to other well established technologies [6] can limit their application. In order to increase energy conversion efficiency, optimization of thermoelectric devices is an active research topic, both in terms of the thermoelectric materials employed [7-10], and the architecture of devices [11-16]. Additionally,

efficient TED operation strongly relies on the integration into the overall energy conversion system [17-21]. Effective heat transfer at the cold and hot plates, minimization of thermal resistances within the system, and reduction of heat leakages each improves overall efficiency. These features depend on the thermal layout of the integrated system and should be taken into account during the design phase to maximize effectiveness.

Here, we present a novel automated method, using topology optimization, to design thermal interfaces and insulation solutions for a TED to be integrated in a system with design constraints. Topology optimization has not previously been applied to thermoelectric systems, but this technique has great potential as a powerful design tool, as it can be used to optimize the topology of heat sinks, heat exchangers, and to define optimized distributions of thermally conducting and insulating material based on a set of design constraints. We show that the method can be implemented using commercial software, is robust, and is suitable for TED applications that must be packaged in a defined space. The method can be used to optimize a thermoelectric system for a variety of objective functions, such as efficiency, power recovery rate, temperature span, etc. Contrary to size and shape optimization approaches, topology optimization requires no initial design concept or a priori parametrization [22, 23]. This flexibility is especially important in the early design phase, as it saves development time and can yield unintuitive optimized structures. Density-based topology optimization methods are particularly promising, since they consider the systematic distribution of material within a design domain, while aiming to optimize a certain objective function.

Topology optimization was first developed and established for structural mechanics applications and was subsequently applied to various other disciplines [24, 25]. Prior studies on heat transfer using topology optimization have mainly focused on pure 2D heat conduction problems [22, 26, 27] as well as heat conduction with convective heat transfer to an ambient fluid [28-32]. Later works have included the explicit modeling of the fluid flow within the optimization domain in thermo-fluid models with forced convection in 2D [33-38] and 3D [39]. More recent applications of the approach have extended models to consider 2D topology optimization of natural convection [40] and radiation as the dominant heat transfer mechanism [41]. The design, manufacturing and subsequent experimental testing of optimized forced-convection heat sinks have also been presented [42-44].

Building on previous studies, this work addresses an existing industrial challenge and applies topology optimization to a thermoelectric system for the first time. Here, it is used to design the thermal integration of a thermoelectric cooler (TEC) in a downhole tool for oil well interventions. The space constraints imposed by the application and the clearly defined thermal boundary conditions make this an attractive case for topology optimization [45]. In the studied application, the TEC maintains a specific group of electronics at a temperature below the outside well temperature to prevent overheating issues that occur when the borehole exceeds the maximum temperature rating of the electronics (175 °C). Topology optimization is used to optimize the distribution of the insulating material, which thermally protects the cooled electronics, and of the conducting material, which aids in rejecting heat from the TEC to the well. The objective of the optimization is to minimize the temperature of the cooled electronics. A more detailed discussion regarding well interventions, active cooling, and thermal management of downhole electronics, is given in Ref. [46-51].

A model of the thermoelectric device was developed for this application, implemented in a 3D finite element model of the system, and coupled with the optimization algorithm. Temperature dependent properties of the TEC were implemented in order to capture the effects of the real material properties during the optimization process. The topology optimization model was used to optimize the design of the system for different operating conditions and to define the optimal working conditions of the TEC. The improvements in

performance for the optimized systems were assessed and used to define a final design of the electronics unit, which is also practical from a manufacturing and assembly standpoint. The defined setup was then manufactured and experimentally tested at different operating conditions, and the results compared to the model predictions.

2. DESCRIPTION OF THE SYSTEM

This chapter briefly introduces the electronics unit system, its main components and the overall thermal management principle. A 3D model of the longitudinal section of the system is illustrated in Figure 1.

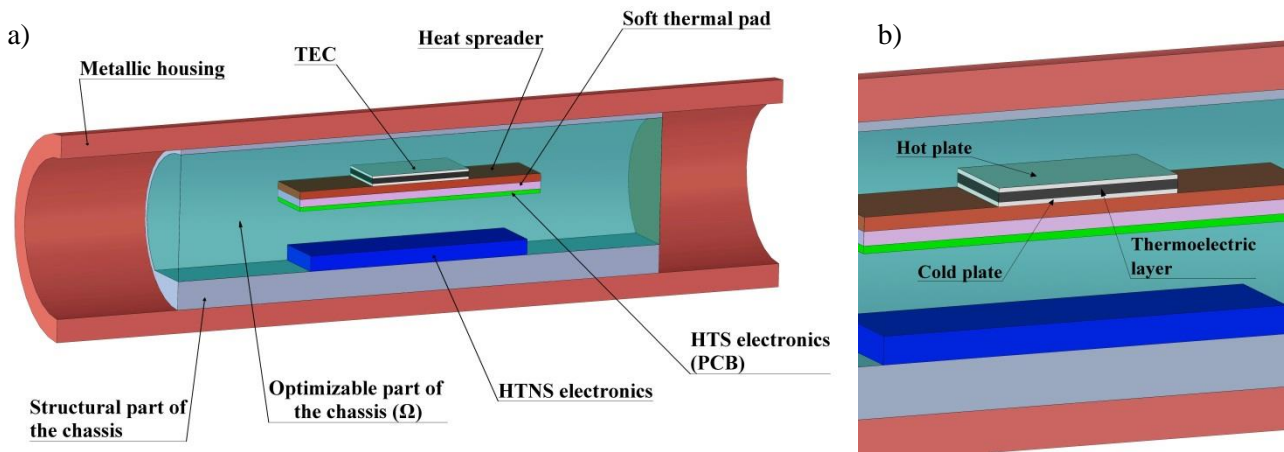


Figure 1. Representation of the axial section of the downhole tool (1a, left side); the domain of the optimizable chassis is represented as partially transparent and colored in light blue. Particular of the TEC device (1b, right side).

The analyzed downhole electronics unit is composed of the following parts:

- *Metallic cylindrical housing:* a hollow cylinder that shields and seals the inner components from the harsh well environment.
- *Chassis:* a rigid metallic support used for final assembly, on which the electronics are mounted and slid into the housing. It is divided in a structural part, which mechanically supports the system; and an optimizable part, which surrounds the components within the structural chassis and is the object of the topology optimization.
- *Electronic components:* they can be split into high temperature-sensitive (HTS) and high temperature-non-sensitive (HTNS) components. The former are likely to fail when their operating temperature exceeds 175 °C, the latter can even operate above 200°C. The HTS electronics are mounted on a printed circuit board (PCB) and are characterized by a power dissipation rate of 1 W; the HTNS electronics are mounted directly on the chassis and dissipate an estimated 5 W.

Additional components, used for the integration of the active cooling system into the tool, are:

- *Thermoelectric cooler:* the cooling system is connected to an electric power source and transfers a heat flux from the cold to the hot plate, when an electric current is applied. The TEC cold plate needs to be thermally coupled to the HTS electronics, while the hot plate requires a thermal link to the hot reservoir, represented by the well environment.

- *Metallic heat spreader*: a rigid plate attached to the TEC cold plate that, together with the thermal pad, constitutes the thermal interface between the PCB and the cooler.
- *Soft thermal pad*: a soft silicone sheet, which is inserted between the PCB and the copper plate to create a thermal path between the irregular surface of the PCB and the heat spreader.

The heat management strategy aims at maintaining the HTS electronics at 175 °C or below when the tool is operating in a 200 °C environment. It is based on the passive cooling of the HTNS components, which can withstand high temperatures, and the active cooling of the HTS components through the Peltier module. The PCB is therefore thermally coupled, through the heat spreader and the thermal pad, with the cold plate of the Peltier module so the cooling load can be absorbed by the cooler. The TEC hot plate, in turn, needs to be thermally connected to the chassis; in this way, the excessive heat can flow through the housing and be rejected to the well fluid that laps the outer surface of the housing, through convective heat transfer. A tight mechanical contact is ensured between the structural chassis and the housing, to reduce the contact thermal resistance.

It is important to note that the thermal connection between the TEC hot plate and the chassis, as well as the distribution of insulating material, will be the result of the topology optimization process. The optimization is expected to define an optimized distribution of thermally conducting material and thermal insulation inside the unit, so the refrigerated electronics are properly protected from the hot surroundings and the excessive heat is effectively rejected to the well fluid. These two phenomena both act towards the minimization of the HTS electronics temperature, which is the objective of the optimization. While the optimization is focused on the thermal integration of the TEC, the topology of the TEC module itself is not the object of the optimization. The finite-element model of the TEC is implemented to simulate the performance of a commercial high-temperature module to be integrated into the downhole tool. The freedom to optimize the electronics unit is limited by three factors: the tool needs to fit a specific well piping size, so its dimensions are constrained to the values reported in Table 1; the position and the design of the components inside the system are constrained by the application; the structural part of the chassis cannot be optimized because of its mechanical function.

Table 1. List of the components with their dimensions and properties.

<i>Component</i>	<i>Length (mm)</i>	<i>I.D. (mm)</i>	<i>O.D. (mm)</i>	<i>Thermal conductivity (Wm⁻¹K⁻¹)</i>
Metallic housing	300	62	80	150
Structural chassis	200	58	62	138
Optimizable chassis	200	-	58	(Eq. 16)
<i>Component</i>	<i>Length (mm)</i>	<i>Depth (mm)</i>	<i>Height (mm)</i>	<i>Thermal conductivity (Wm⁻¹K⁻¹)</i>
TEC plates	40	40	0.95 each	27
TEC thermoelectric layer	40	40	2.0	(Eq. 8)
Heat spreader	100	40	3.0	400
Soft thermal pad	100	40	3.0	12
HTNS electronics	90	42	6.0	130
HTS electronics (PCB)	100	40	1.6	0.3

3. FINITE ELEMENT MODEL

3.1 Governing equations

The geometry shown in Figure 1 was implemented in the finite element software COMSOL Multiphysics [52] and divided in domains, each of them characterized by different material properties and governing equations. In order to simulate the heat transfer within the system, mainly driven by heat conduction, the heat transfer PDE (Eq. 1) was solved in all the domains, except for the thermoelectric material layer.

$$\nabla(-k\nabla T) = Q_{source} \quad (1)$$

where k is the material thermal conductivity, T is the temperature, and Q_{source} is a volumetric heat source. Eq. 1 was not applied to the thermoelectric material domain, as the heat transport related to the thermoelectric effect also needed to be taken into account. A modified heat transfer PDE (Eq. 2) was used instead.

$$\nabla(\mathbf{J}S'T - k'\nabla T) = Q'_{JouleHeating} \quad (2)$$

where \mathbf{J} is the electric current density vector, S' is the material Seebeck coefficient, and $Q'_{JouleHeating}$ is the heat source associated with the Joule heating effect.

3.2 Boundary conditions

The boundary conditions were set in order to simulate the operating and external conditions that could occur in a well during a downhole intervention. A convective heat flux was set on the outer surface of the housing, to reproduce the interaction between the well fluid and the tool.

$$-\mathbf{n} \cdot (-k\nabla T) = h(T - T_{ext}) \quad (3)$$

Furthermore, the tool electronics unit would be assembled in the middle of a tool string, composed of several sections, and the heat transfer with the well is expected to mainly occur radially. For this reason, adiabatic boundaries were set at the two ends of the cylindrical setup.

$$-\mathbf{n} \cdot (-k\nabla T) = 0 \quad (4)$$

where \mathbf{n} is the surface normal vector, T_{ext} is the well fluid temperature and h is the heat transfer convection coefficient. Concerning the interface between the thermoelectric material domain, where Eq. 2 is solved, and the rest of the geometry, where Eq. 1 is solved, a Dirichlet boundary condition was defined to provide consistency to the temperature distribution. Heat sources were set in the HTNS electronics domain (5 W), and at the interface between the PCB and the soft thermal pad (1 W), to simulate the power dissipation of both electronics modules. Thermal resistances, $R_{th1,2} = 2.5e-5 \text{ m}^2\text{KW}^{-1}$, were modelled at the interface between the HTNS electronics and the structural chassis, and on the outer boundaries of the TEC hot/cold plates; they simulated the contribution of a 0.1 mm thick layer of thermal grease, with a thermal conductivity of $4 \text{ Wm}^{-1}\text{K}^{-1}$. An additional thermal resistance, $R_{th3} = 1.1e-3 \text{ m}^2\text{KW}^{-1}$, was set at the interface between the structural chassis and the housing in order to simulate the contact resistance given by the assembly. The value of this thermal resistance was estimated through the comparison between simulation results and experimental data from thermal tests on an analogue setup.

The operating conditions of the cooler were characterized by the TEC feed current I_{feed} , which represents the electric current which is supplied to the module and is given to the model as an input. The correlation between this parameter and the current density vector \mathbf{J} (see Eq. 2) is explained in more detail in the next section.

3.3 TEC model

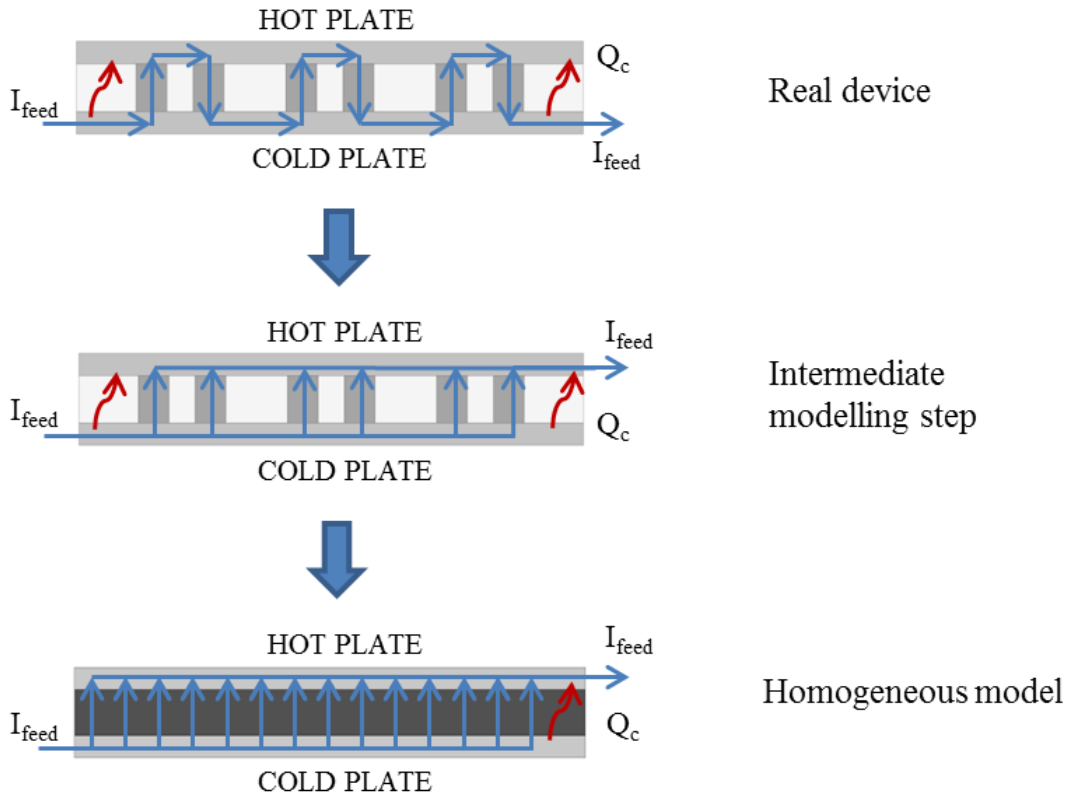


Figure 2. Illustration of the simplification process for the TEC model. The longitudinal section and the working principle of the *real device* and of the *homogeneous model* are included. For the sake of a better understanding, an intermediate step of the model development, called *intermediate modelling step*, is also included.

A particular focus was put on the modelling of the thermoelectric cooler. Its main components are two aluminum oxide plates, between which leg pairs of semiconducting material (p-n junctions) are mounted, electrically connected in series, and separated by air. Reproducing the detailed geometry of the module would have drastically increased the complexity and the computational time of the 3D topology optimization model. Therefore a simplified model of the TEC was developed: the intermediate semiconductor layer was modelled as homogeneous and isotropic, and equivalent material properties were weighted on the properties of Bi_2Te_3 and air. In this way, the cooling effect driven by a given TEC feed current could be approximated to the real case, while the geometry could be significantly simplified.

As a consequence of the homogenization process, the electric and thermal transport phenomena could not be differentiated within the Bi_2Te_3 and air domains, and the inhomogeneous temperature gradient across the module could not be reproduced. However, this approximation was considered acceptable as it preserves the average heat fluxes that drive heat transfer in the integrated system.

Figure 2 illustrates the steps that were used to develop the homogeneous model and that are explained in the following sub-sections.

3.3.1 Effective current density

In the *real device*, the thermoelectric leg pairs are fed in series. The current density through the legs \mathbf{J} can be expressed, in good approximation, as the 3D vector $[0, 0, \pm J_z]$. The only non-zero contribution is along the z-axis, perpendicular to the TEC plates, and can be equal to $-J_z$ or $+J_z$. The scalar current density can be defined as:

$$J_z = \frac{I_{feed}}{A_{leg}} \quad (5)$$

where J_z is the scalar current density along the z-axis, I_{feed} is the TEC feed current and A_{leg} is the cross sectional area of the single thermoelectric leg.

In the *intermediate modelling step*, the thermoelectric legs are all doped p-type and are fed in parallel and the current density vector is now equal to $[0, 0, +J_z]$. Given the parallel configuration, and in order to maintain the same thermoelectric effect in each leg as the *real device*, the TEC feed current becomes N times bigger, where N is the number of thermoelectric legs installed in the module.

In the *homogeneous model*, there is no distinction between thermoelectric legs and air. The homogeneous layer is supplied by a uniform electric current equal to $N \cdot I_{feed}$, in the positive z-axis direction. A different current density needs to be defined:

$$J_z' = \frac{NI_{feed}}{A_{tot}} = \frac{NI_{feed}}{A_{tot}} \cdot \frac{NA_{leg}}{NA_{leg}} = \frac{I_{feed}}{A_{leg}} \cdot \frac{A_{BiTe}}{A_{tot}} = J_z x_{BiTe} \quad (6)$$

where J_z' is the equivalent scalar current density for the homogeneous model, A_{tot} is the total cross sectional area of the thermoelectric module, A_{BiTe} is equal to N times A_{leg} and represents the cross sectional area occupied by the thermoelectric legs in the *real device*, and x_{BiTe} is the ratio between A_{BiTe} and A_{tot} . x_{BiTe} is also equal to the volume ratio between bismuth telluride and the total volume of the intermediate layer.

3.3.2 Effective Seebeck coefficient

Given the TEC PDE for the homogeneous layer in Eq. 2, we want to maintain the same thermoelectric cooling effect $\mathbf{J}'S$ as the *real device*. First, it is assumed that the Seebeck coefficient of the layer does not change with the homogenization process. However, the current density has changed and it can be imposed:

$$J_z'S = J_zS' \rightarrow S' = S x_{BiTe} \quad (7)$$

More intuitively, one could think that the thermoelectric cooling effect is now generated with the same scalar current density J_z as the *real device*, but only by a portion of the layer (x_{BiTe}), ideally occupied by the Bi_2Te_3 legs. Although the cooling effect is maintained to be the same, the homogeneous approximation spreads it equally along the whole layer.

3.3.3 Effective thermal conductivity of the layer

The heat transfer within the intermediate layer occurs mainly from a cooler plate to the other, while the temperature gradient along the direction parallel to the plates is expected to be negligible. It is therefore assumed that the effective thermal resistance of the layer is equal to the parallel coupling of the thermal resistances, of air and Bi_2Te_3 , between the hot and cold plate.

$$k' = k_{air} \frac{A_{air}}{A_{tot}} + k_{BiTe} \frac{A_{BiTe}}{A_{tot}} = k_{air}(1 - x_{BiTe}) + k_{BiTe} x_{BiTe} \quad (8)$$

where k' is the thermoelectric layer equivalent thermal conductivity for the homogeneous model, and t is the thermoelectric layer thickness.

3.3.4 Effective electrical conductivity of the layer

In analogy with the effective thermal conductivity calculation, and neglecting the air electrical conductivity:

$$\sigma' = \sigma_{BiTe} x_{BiTe} + \sigma_{air} x_{air} = \sigma_{BiTe} x_{BiTe} \quad (9)$$

where σ' is the thermoelectric layer equivalent electric conductivity for the homogeneous model. Consequently the Joule heating term can be calculated as:

$$Q'_{JouleHeating} = \frac{x_{Bi2Te3}}{\sigma_{Bi2Te3}} \mathbf{J} \cdot \mathbf{J} = \frac{J_z^2}{\sigma_{Bi2Te3}} x_{Bi2Te3} \quad (10)$$

Again, the original Joule losses are maintained, but are spread uniformly along the layer because of the homogeneous approximation.

A suitable high-temperature commercial cooler was disassembled and analyzed, so the main geometric features could be measured. They are summarized in Table 2.

Table 2. Geometric features of the modelled thermoelectric cooler.

<i>Parameter</i>	<i>Description</i>	<i>Value</i>
h_{TEC}	Total height of the module	3.90 mm
l_{TEC}	Edge length of the module	40.0 mm
h_{Al2O3}	Height of the hot/cold plate	0.95 mm
N	Number of thermoelectric legs	254
h_{Bi2Te3}	Height of the single thermoelectric leg	2.00 mm
l_{Bi2Te3}	Edge length of the single thermoelectric leg	1.30 mm
A_{leg}	Cross sectional area of a thermoelectric leg	1.69e-6 m ²
x_{Bi2Te3}	Volume fraction of semiconductor materials	0.27

The properties of Bismuth Telluride S_{BiTe} , k_{BiTe} and σ_{BiTe} from [53] were implemented as non-linear functions of temperature. In order to better match the performance of the high-temperature commercial cooler, a linear coefficient was multiplied to the expressions of the Bi₂Te₃ Seebeck coefficient, thermal conductivity, and electrical conductivity. The linear coefficients are the result of a best fit analysis based on experimental data and are respectively equal to $S_I=1.30$, $k_I=0.80$, and $\sigma_I=1.15$.

3.4 Topology optimization and SIMP method

The topology optimization approach was used to assess which distribution of aluminum/thermal insulation inside the electronics unit minimized the temperature of the HTS electronics. Filling the electronics unit with only thermal insulation would maximize the thermal protection of the cooling zone from heat leakages, but

would not provide an effective thermal path for the rejected heat to flow to the well environment. The Peltier module would therefore not be able to work within the cooling design conditions. Filling the electronics unit with aluminum, instead, would enhance the heat rejection process, but would not protect the cooling zone from heat leakages, making the cooling process ineffective. A tradeoff needs to be reached and the Solid Isotropic Material with Penalization (SIMP) method allowed looking for an optimized solution.

The main goal of the SIMP method, as part of the density-based topology optimization approaches, is to achieve a binary design within the optimizable domain, where the design variable can be equal to 0, representing thermal insulation, or to 1, representing aluminum. The topology optimization problem can be stated as follows:

$$\text{minimize:} \quad f_{obj}(T, \rho_{design}) = \frac{1}{A_{PCB}} \int_{\Omega_{PCB}} T \, d\Omega_{PCB} \quad (11)$$

$$\text{subject to:} \quad 0 \leq \rho_{design} \leq 1 \quad (12)$$

$$\mathbf{r}(T, \rho_{design}) = \mathbf{0} \quad (13)$$

where f_{obj} is the objective function to minimize, equal to the integral average of the temperature distribution along the PCB surface Ω_{PCB} ; A_{PCB} is the PCB area surface; ρ_{design} is the design variable that can range between 0 (thermal insulation) and 1 (aluminum), and the distribution of which needs to be optimized; $\mathbf{r}(T, \rho_{design})$ is the residual of the state governing equations within the discretized system.

A PDE-based density filter [54] was used to smooth the interfaces between aluminum and insulator and to introduce a minimum length scale into the design. The PDE-based filter was used because it can be implemented in the optimization model with little additional effort and it offers a computationally efficient method of density filtering. The PDE that was used for filtering is stated in Eq. 14.

$$-r^2 \nabla^2 \tilde{\rho} + \tilde{\rho} = \rho_{design} \quad (14)$$

where $\tilde{\rho}$ is the filtered density field and r is a filter parameter, defined as 1.5 times the maximum element size and equal to 3e-3 m. Since density filtering inherently introduces a band of intermediate densities between aluminum and insulator, the filtered design variable field $\tilde{\rho}$ was then projected towards 0 and 1 to obtain a crisp design. For this purpose a smoothed threshold projection [55] was used.

$$\bar{\tilde{\rho}}_i = \frac{\tanh(\beta\eta) + \tanh(\beta(\tilde{\rho}_i - \eta))}{\tanh(\beta\eta) + \tanh(\beta(1 - \eta))} \quad (15)$$

where $\bar{\tilde{\rho}}_i$ is the projected density field, η is the projection threshold, equal to 0.5, and β defines the steepness of the projection.

When applying the topology optimization SIMP method, it is not possible to theoretically guarantee the convergence to a global optimum. Nevertheless, it is possible to tune the optimization parameters through the continuation method to ensure that the solution is close to the global optimum [56]. In this study, using a steep projection at the beginning of the optimization could result in convergence to local minima. Therefore, a continuation approach [55] was used to ramp β , which means that the optimization was started with an almost linear projection ($\beta = 1$) and β was subsequently gradually increased to steepen the projection

function. Thus, one could ensure that the optimization problem is convexified at the beginning of the optimization, while ending up with a crisp design.

The difference of thermal conductivity between aluminum and thermal insulation was accounted by an interpolation function k_{SIMP} that defined the effective thermal conductivity of the optimizable chassis.

$$k_{SIMP} = k_{ins} + (k_{Al} - k_{ins})\bar{\rho}^p \quad (16)$$

where k_{SIMP} is the effective thermal conductivity, $k_{ins} = 0.17 \text{ Wm}^{-1}\text{K}^{-1}$ and $k_{Al} = 138 \text{ Wm}^{-1}\text{K}^{-1}$ are respectively the thermal conductivities of the insulator and of the aluminum, $\bar{\rho}$ is the projected design variable, and p is the penalization coefficient. When performing topology optimization for continuous design variables, intermediate regions (areas where the design variable assumes intermediate values between 0 and 1) can appear in the final distribution; these transition zones are not physically meaningful for the analyzed problem and need to be reduced as much as possible. Classically, a penalization coefficient $p = 3$ is used in topology optimization in combination with an active volume constraint [30] to make intermediate regions unattractive with respect to the optimization problem, and to drive the control variable towards either 0 or 1. In this work, no active volume constraint was used, nevertheless a faster convergence was found for $p = 3$, compared to a linear interpolation ($p = 1$). Therefore $p = 3$ was used for the simulations. The globally convergent version of the Method of Moving Asymptotes (GCMMA) [57] was finally used to solve the optimization problem; this algorithm is implemented in COMSOL Multiphysics [52] with the solver name *MMA*.

In this study, the structural and design constraints limited the optimization possibilities to the chassis domain only and did not require or allow the optimization of other components (e.g. metallic housing, heat spreader, TEC). However, the topology optimization approach can be used to simultaneously optimize multiple geometrical features by implementing additional interpolation functions for different optimizable domains. This process would increase the non-linearity of the optimization problem, consequentially increasing the computation cost and the risk of converging to local minima. Thus, in these cases, a more careful solution of the problem through the continuation method should be adopted.

4. RESULTS

4.1 Definition of the optimized design concepts

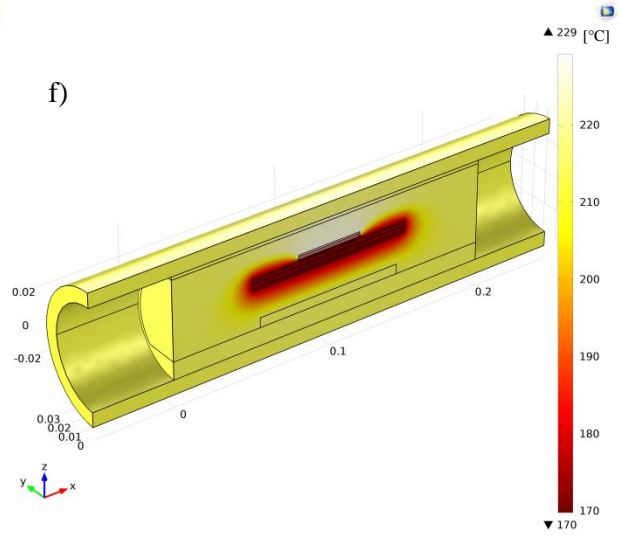
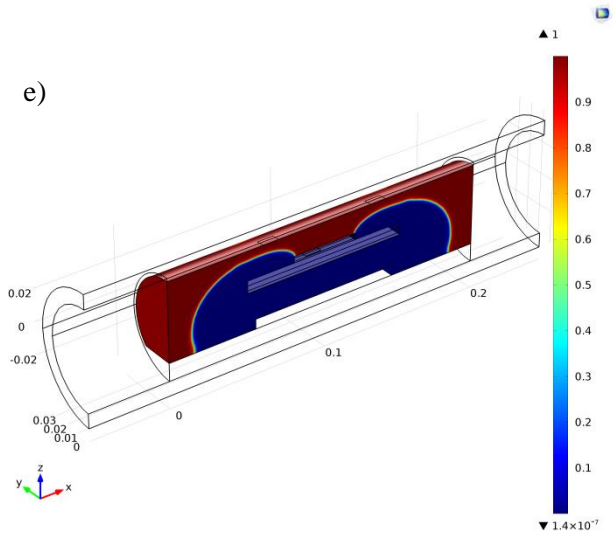
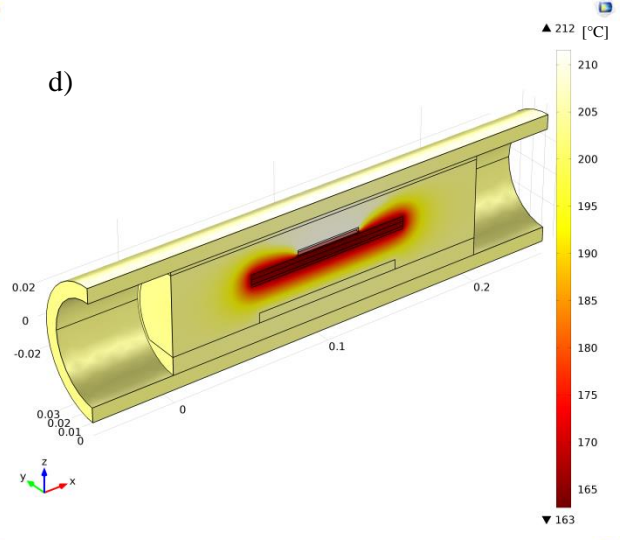
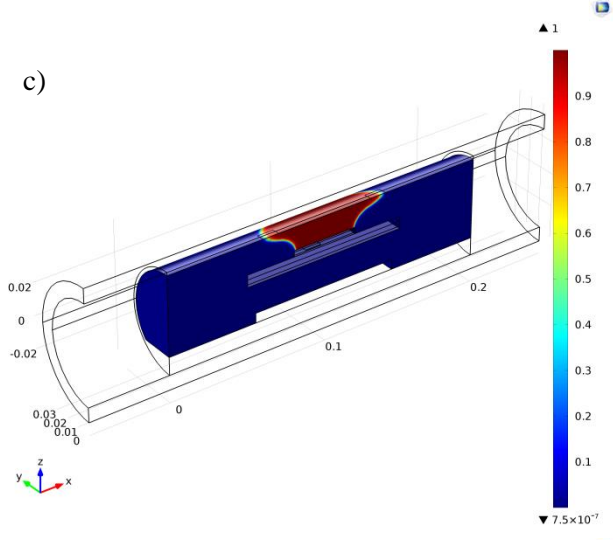
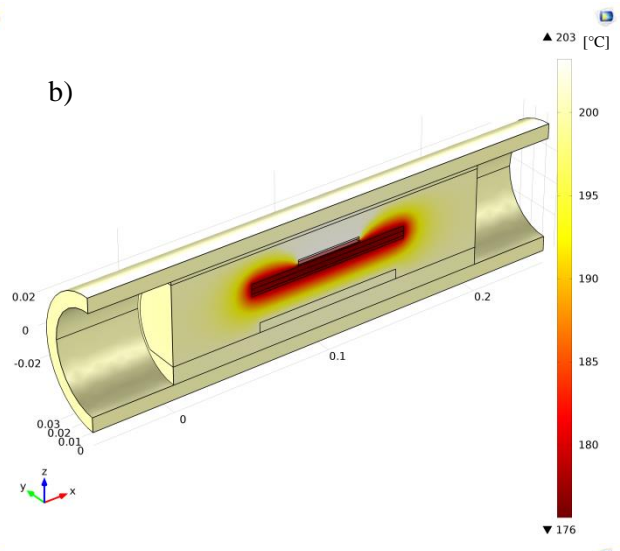
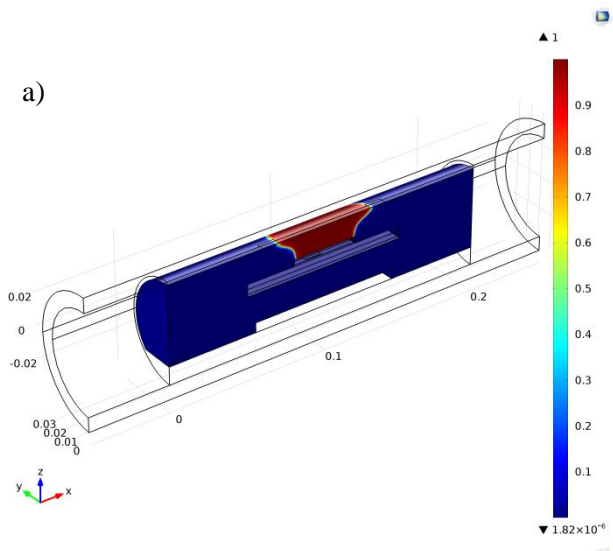
The model was used to optimize the topology of the electronics unit for different boundary conditions of TEC feed current and well fluid convective heat transfer coefficient. The system was optimized for TEC feed currents $I_{feed} = 1, 2, 3$ and 4 A , where the maximum feed current stated by the analyzed commercial TEC supplier is 6 A ; and for convective heat transfer coefficients $h = 10, 25, 50, 100$ and $500 \text{ Wm}^{-2}\text{K}^{-1}$, in order to reproduce very low, low, and medium well fluid convection regimes. The well temperature T_{ext} was set to $200 \text{ }^\circ\text{C}$, as the maximum temperature at which the system is expected to operate.

The optimized structure was found to be a function of the boundary conditions. Various boundary conditions led to different tradeoffs between thermal protection of the cooled electronics and excessive heat rejection from the cooler to the well. The model proved to optimize the unit according to three different design configurations: *Design 1*, where the thermal insulation of the cooled electronics is prioritized; *Design 2*, where the conduction of the excessive heat towards the well is equally important as the thermal protection; and *Design 3*, where the excessive heat rejection is crucial for the operation of the system. A more detailed illustration of the three design concepts is given in the following paragraphs.

Low feed currents and high well fluid convection coefficients led to an optimized system (*Design 1* concept), where only an aluminum pad links the cooler hot plate to the structural chassis and provides a thermal path for the excessive heat to be dissipated radially. The remaining volume of the unit is filled with thermal insulation (Figure 3a, 3b, 3c and 3d). In this case the thermal protection of the electronics is prioritized, as the heat rejection from the cooler to the well is not challenging. Low currents generate small Joule losses across the cooler and the high convection coefficients provide an effective heat rejection towards the well. The length of the aluminum plate increases when the TEC feed current grows and when the external convection coefficient decreases, so the heat can be better spread through the structural chassis and housing, towards the well.

When the feed current is increased and the well fluid convection coefficient lowered, the optimized system (*Design 2* concept) aims at better spreading the excessive heat, coming from the cooler hot plate, around the structural chassis and housing. A better distribution of the heat enhances, in fact, the heat exchange with the well, limits the temperature gradients due to the thermal resistances, and reduces the heat backflow to the cooled electronics. This is done by adding an aluminum layer, around the structural chassis, that spreads the heat not only radially, but also along the longitudinal direction of the tool (Figure 3e and 3f). A thermally insulating layer still protects the cooled components from the hot surroundings. The thickness of the aluminum layer grows when the feed current, and the Joule losses, increase or when the well fluid convection coefficient decreases.

A third type of optimized design (*Design 3* concept) appeared for $I_{feed} = 4$ A and $h = 10$ Wm⁻²K⁻¹, which respectively correspond to the highest feed current and the lowest convection coefficient that were simulated. In this case the power dissipation rate, due to Joule heating, proves to be much higher than the capability of the well fluid to remove heat through the convective mechanism. The generated heat flux increases the HTS electronics temperature above the well temperature, making active cooling infeasible at these operating conditions. The optimization process hence strongly prioritizes the heat rejection by creating a thermal path between the PCB and the well fluid, while two thin insulating layers protect the electronics from the cooler hot plate and from the HTNS electronics (Figure 3g and 3h).



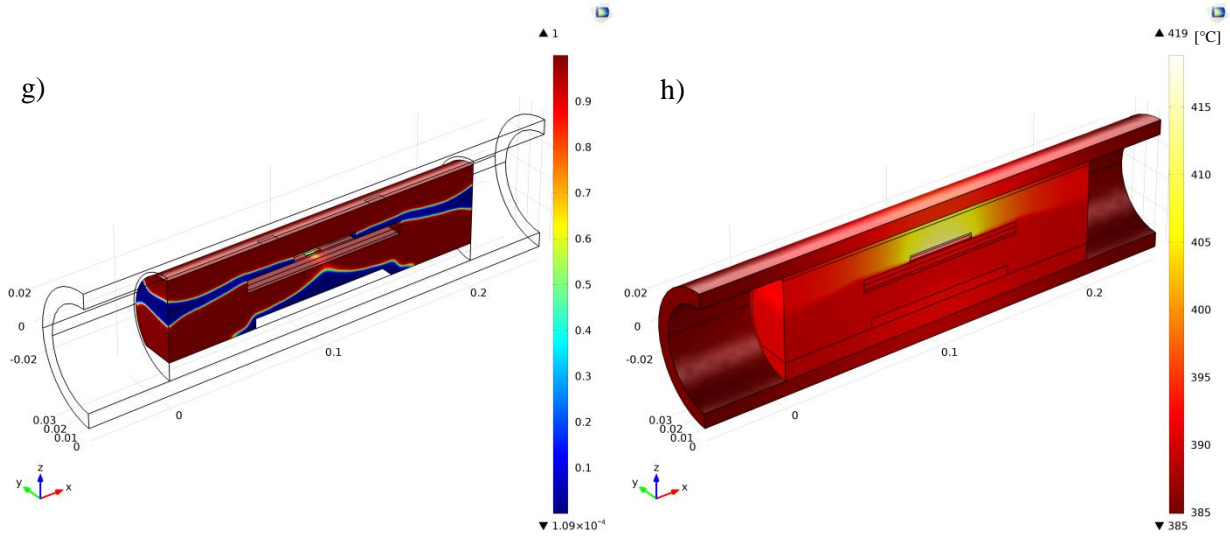


Figure 3. Density field (left) and resulting temperature distribution (right) of the optimized *Design 1* concept at $I_{feed} = 1 \text{ A} / h = 500 \text{ Wm}^{-2}\text{K}^{-1}$ (a, b), and at $I_{feed} = 2 \text{ A} / h = 100 \text{ Wm}^{-2}\text{K}^{-1}$ (c, d); of the optimized *Design 2* concept at $I_{feed} = 3 \text{ A} / h = 50 \text{ Wm}^{-2}\text{K}^{-1}$ (e, f), and of the optimized *Design 3* concept at $I_{feed} = 4 \text{ A} / h = 10 \text{ Wm}^{-2}\text{K}^{-1}$ (g, h). The density fields illustrate the different distributions of aluminum (red) and thermal insulation (blue), for the four optimized systems.

The balance between thermal protection of the cooled electronics and rejection of the excessive heat is reached differently for each set of boundary conditions and with different aluminum-thermal insulation ratios. Computing the volume percentage of employed aluminum, over the total optimizable volume, helps to have a clearer picture of the optimized designs trend with the boundary conditions. That can be calculated with the following expression:

$$R = \frac{1}{V_{\Omega}} \int_{\Omega} \bar{\rho} d\Omega \quad (17)$$

where V_{Ω} is the volume of the optimizable domain and $\bar{\rho}$ is the projected design variable.

The amount of employed aluminum decreases with the convection coefficient and increases with the feed current (Figure 4); more in general, more aluminum is employed when a better heat rejection to the well is needed.

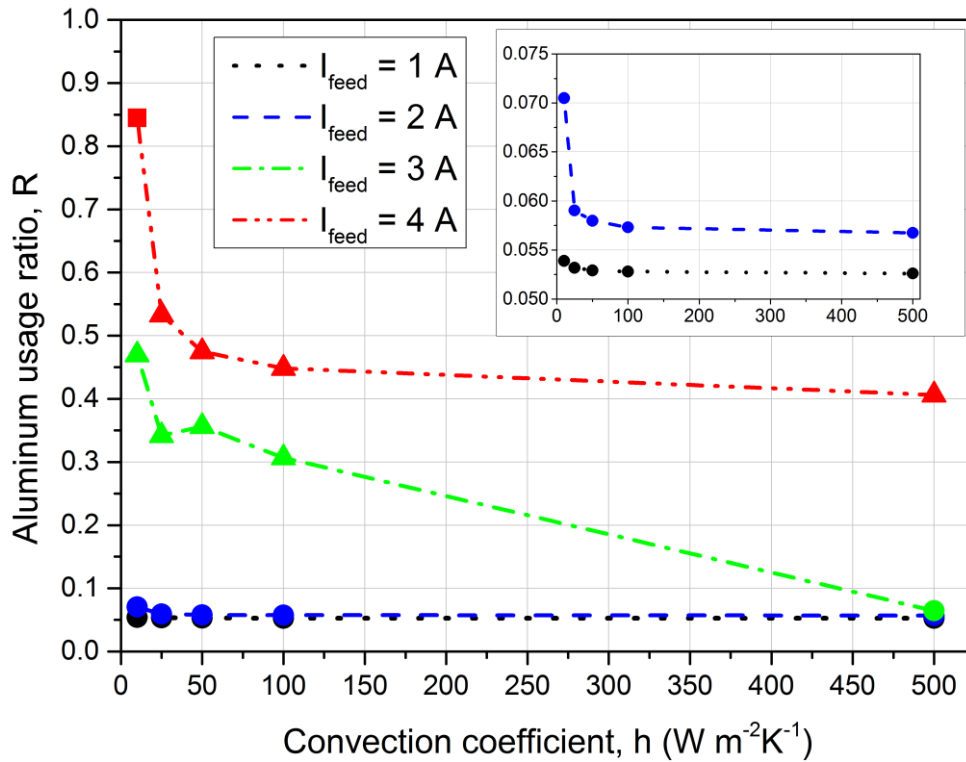


Figure 4. R vs. well fluid convection coefficient, for different TEC feed currents. The three different symbols correspond to the three obtained design configurations: ● = *Design 1*, ▲ = *Design 2*, ■ = *Design 3*.

4.2 Comparison of the optimized designs

Defining the categories of the optimized topologies is only the first step towards the selection of a final design for the actively cooled electronics unit. The performance of the optimized designs, at conditions they were not optimized for, is also an important feature to take into account. Furthermore, a cross-validation between the resulting topologies can be used to check for convergence to local minima. It can be detected if an optimized design does not show the best performance at the boundary condition it was optimized for.

A first sensitivity analysis was carried out to evaluate how the performance of an optimized system would change at different well fluid convection regimes. The electronics section was first optimized for a certain value of feed current and well fluid convection; the optimized design was then simulated at different values of convection coefficient, maintaining the TEC feed current constant. The resulting performances were compared as illustrated in Figure 5. The performance of the system was evaluated in terms of HTS electronics average temperature, computed through the objective function reported in Eq. 11.

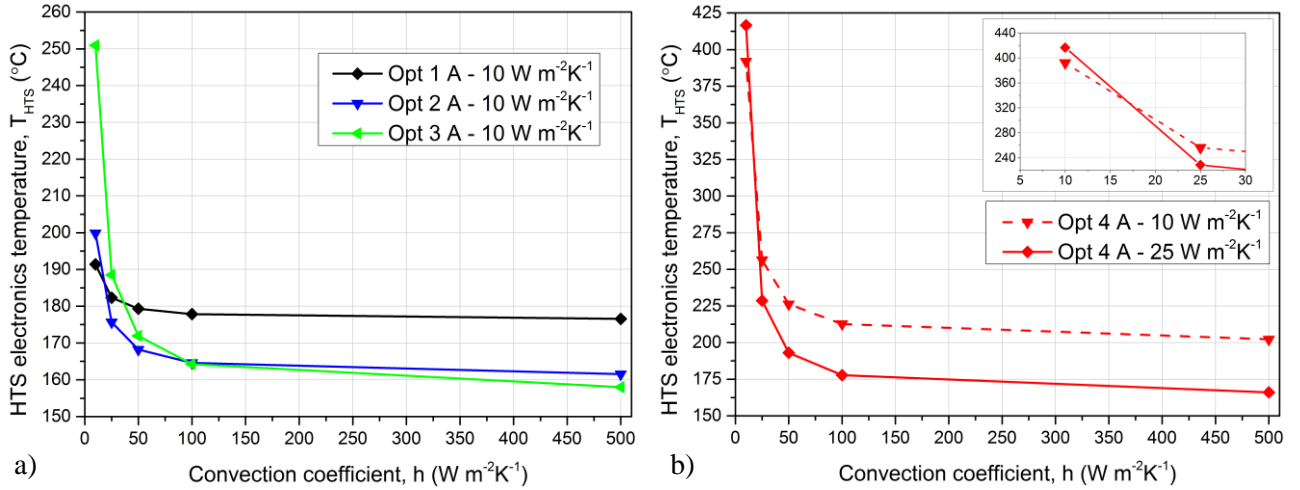


Figure 5. HTS electronics temperature vs. Convection coefficient for three different systems, optimized for $h = 10 \text{ Wm}^{-2}\text{K}^{-1}$ and $I_{feed} = 1, 2, 3 \text{ A}$ (5a, left side). HTS electronics temperature vs. Convection coefficient for two systems optimized for $h = 10, 25 \text{ Wm}^{-2}\text{K}^{-1}$ and $I_{feed} = 4 \text{ A}$ (5b, right side).

Figure 5a reports the performance trend with h of the systems optimized for $h = 10 \text{ Wm}^{-2}\text{K}^{-1}$ and $I_{feed} = 1, 2,$ and 3 A . As forecast, the HTS electronics is maintained colder at higher h values, when the heat rejection to the well is enhanced. Furthermore, higher feed currents are able to keep the electronics colder only if the well fluid is able to absorb the additional excessive heat, generated by the higher Joule losses. The lowest T_{HTS} , at a certain convection regime, is given by the system that was optimized for it.

Unexpectedly, it was found that the systems optimized for the same feed current operate very closely to each other, independently on the value of h they were optimized for. The performance trends of the systems optimized for $I_{feed} = 1, 2$ and 3 A , and $h > 10 \text{ Wm}^{-2}\text{K}^{-1}$, would in fact overlap with the corresponding three curves illustrated in Figure 5a. A maximum mismatch of only $0.05 \text{ }^\circ\text{C}$, $0.01 \text{ }^\circ\text{C}$, and $1.47 \text{ }^\circ\text{C}$ was found between the performance trends of the systems optimized for $I_{feed} = 1, 2,$ and 3 A , respectively. This analysis proved that the optimization process is not significantly sensitive to the considered well fluid convection range. In other words, the length of the aluminum pad, which characterizes the *Design 1* concept, as well as the thickness of the aluminum layer, which characterizes the *Design 2* concept, do not significantly affect the performance of the optimized systems between 1 A and 3 A .

On the contrary, not all the topologies optimized for 4 A have a similar behavior. As Figure 5b shows, the system optimized for 4 A and $10 \text{ Wm}^{-2}\text{K}^{-1}$ (*Design 3* concept) maintains the electronics at a significantly lower temperature at low convection coefficients, compared to the one optimized for 4 A and $25 \text{ Wm}^{-2}\text{K}^{-1}$. However, above $25 \text{ Wm}^{-2}\text{K}^{-1}$ the system optimized for 4 A and $25 \text{ Wm}^{-2}\text{K}^{-1}$ (*Design 2* concept) is able to maintain the HTS electronics down to a $37 \text{ }^\circ\text{C}$ lower temperature. In analogy with the previous cases, the other designs optimized for 4 A and $h > 25 \text{ Wm}^{-2}\text{K}^{-1}$ were found to operate similarly to the case optimized for 4 A and $h = 25 \text{ Wm}^{-2}\text{K}^{-1}$, with a maximum mismatch between the performance trends of $6.67 \text{ }^\circ\text{C}$.

In an analogue way, the sensitivity of the optimized topologies to the TEC feed current was studied. The electronics unit was initially optimized for a certain value of well fluid convection coefficient and of TEC feed current; the resulting optimized design was then simulated at different values of feed current, while maintaining the value of h constant.

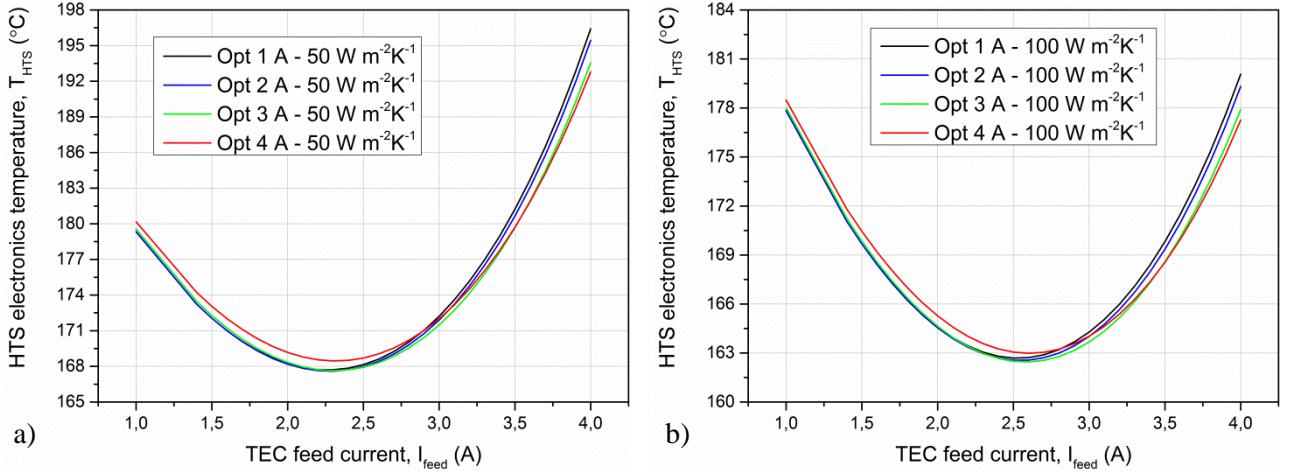


Figure 6. HTS electronics temperature vs. TEC feed current of four different designs, optimized for $I_{feed} = 1, 2, 3$ and 4 A, and $h = 50 \text{ W m}^{-2}\text{K}^{-1}$ (6a, left side) and $100 \text{ W m}^{-2}\text{K}^{-1}$ (6b, right side).

Figure 6 shows that the optimization process is more sensitive to the feed current than to the external convection coefficient. The mismatch between the curves is now larger and can go up to several degrees Celsius. As expected, the lowest T_{HTS} , at a certain TEC feed current, is given by the system that was optimized for it.

An optimal feed current I_{opt} , which minimizes the HTS electronics temperature, can be individuated. Increasing the TEC feed current enhances the thermoelectric effect and the heat transport from the cold to the hot plate. However, that makes the Joule losses within the module larger, in turn causing a larger excessive heat flux that needs to be rejected to the wellbore, and a higher heat backflow to the HTS electronics through the thermal insulation. The optimal current I_{opt} can be defined as the TEC feed current at which the marginal gain in absorbed heat flux from the cold plate, due to an infinitesimal increase of the TEC feed current, becomes smaller than the heat flux that leaks back to the cooled electronics through the insulation. I_{opt} varies slightly for each optimized design, and depends mainly on h .

I_{opt} is equal to ~ 1.2 A for $h = 10 \text{ W m}^{-2}\text{K}^{-1}$, to ~ 1.9 A for $h = 25 \text{ W m}^{-2}\text{K}^{-1}$, to ~ 2.3 A for $h = 50 \text{ W m}^{-2}\text{K}^{-1}$, to ~ 2.6 A for $h = 100 \text{ W m}^{-2}\text{K}^{-1}$, and to ~ 2.9 A for $h = 500 \text{ W m}^{-2}\text{K}^{-1}$. With respect to the considered operations at non-optimal current, working at I_{opt} can reduce the electronics temperature by a maximum ~ 244 °C at $h = 10 \text{ W m}^{-2}\text{K}^{-1}$, ~ 59 °C at $h = 25 \text{ W m}^{-2}\text{K}^{-1}$, ~ 29 °C at $h = 50 \text{ W m}^{-2}\text{K}^{-1}$, ~ 17 °C at $h = 100 \text{ W m}^{-2}\text{K}^{-1}$, and ~ 20 °C at $h = 500 \text{ W m}^{-2}\text{K}^{-1}$. The designs that prove to maintain the HTS electronics at the lowest temperature, around the optimal current, are the ones optimized for 2 A and 3 A.

4.3 Design of the actively cooled electronics section

The results from the topology optimization study were used to define the final design of the actively cooled electronics unit (Figure 7); practical assembly constraints were also taken into account. The heat transfer analysis of the system revealed that the ideal operating condition for the device to work is a combination of high TEC feed current, that guarantees a strong cooling effect, and a high well fluid convection regime, which guarantees an effective removal of the excessive heat. Unfortunately the well fluid convection regime can vary significantly in operation, and therefore the tool needs to be designed for the worst-case design convection coefficient, which was set to $25 \text{ W m}^{-2}\text{K}^{-1}$. *Design 3* can be immediately discarded from the

suitable topologies, as it was optimized for a convection regime that is outside the design conditions and for a TEC feed current that is far from the optimal ones. As mentioned previously, the optimal feed current for $h = 25 \text{ Wm}^{-2}\text{K}^{-1}$ is $\sim 1.9 \text{ A}$; the optimized design for these conditions corresponds to the *Design 1* concept (see Figure 4). However, *Design 2* proved to have a very similar performance around the optimal feed current (see Figure 6), which means that there is some freedom in the design of the aluminum pad and/or layer. The lower mass of aluminum that characterizes *Design 1* would make the tool lighter, though, which is preferable from a logistic and operational point of view. Furthermore, the aluminum pad, which provides the radial thermal path from the cooler hot plate to the structural chassis, proved to be the fundamental feature for effective operation of the system: an aluminum pad was therefore implemented in the final design. No aluminum layer was included, except for two walls, 10 mm thick, at the two ends of the chassis: they provide mechanical stability, an additional thermal path to better spread the heat in the case of a poor heat rejection rate, and are suitable for the installation of pins for the assembly of the system. The chassis would be in fact split into a top half, where the cooling system and the PCB are installed, and a bottom half, on which the HTNS electronics are mounted. Two smaller pads, with threaded holes, were designed in the top part of the chassis: they support a plastic screw system that clamps the cooler between the heat spreader and the chassis, while ensuring effective thermal contacts. The remaining volume was filled with thermal insulation, for thermal protection of the cooled electronics.

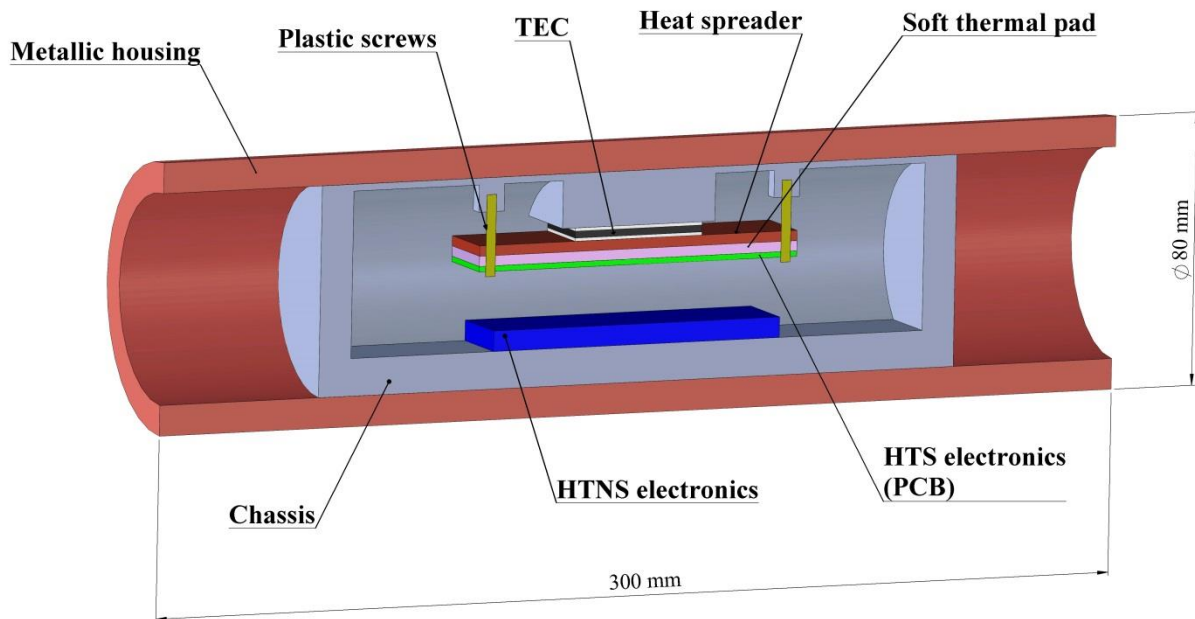


Figure 7. Illustration of the longitudinal section of the final design. The thermoelectric cooler is clamped between the aluminum pad and the heat spreader through two plastic screws (in yellow). The remaining volume within the chassis is filled with thermal insulation.

Simulations showed the chosen design operates very similarly to the optimized systems (Table 3). The difference in HTNS electronics temperature is very small when operating at 1 A or 2 A, as the final design is very similar to the *Design 1* concept. The HTNS electronics are in fact maintained maximum $0.11 \text{ }^\circ\text{C}$ above the optimized case. When operating at 3 A and 4 A, the mismatch becomes larger, since the *Design 2* concept would perform better at higher feed currents. However, when operating at 3 A, the HTS components are always maintained less than $1 \text{ }^\circ\text{C}$ above the optimized system. The mismatch becomes larger than $1 \text{ }^\circ\text{C}$

for operations at 4 A; that can be considered irrelevant, since $I_{feed} = 4$ A is far from the observed optimal TEC settings and the system would always aim at operating between 2 A and 3 A, close to the optimal conditions.

Table 3 also shows the final system fulfills the design conditions and the electronics can be maintained below 175 °C for every well fluid convection regime, as far as a control system can regulate the TEC feed current around the optimal one. The only exception occurs for the case at $h = 25$ $Wm^{-2}K^{-1}$, where the heat rejection is very poor and the electronics can only be maintained between at an average temperature of 175 °C and 176 °C; this result is still considered acceptable given the small mismatch.

Table 3. Comparison between the performance of the final design (Design) and the optimized systems (Opt). $\Delta T = T_{HTS,design} - T_{HTS,opt}$.

h ($Wm^{-2}K^{-1}$)	Opt - 1A T_{HTS} (°C)	Design - 1A T_{HTS} (°C)	ΔT (°C)
25	182.31	182.41	0.10
50	179.32	179.43	0.11
100	177.83	177.94	0.11
500	176.56	176.67	0.11
h ($Wm^{-2}K^{-1}$)	Opt - 2A T_{HTS} (°C)	Design - 2A T_{HTS} (°C)	ΔT (°C)
25	175.63	175.68	0.05
50	168.18	168.23	0.05
100	164.54	164.57	0.03
500	161.46	161.48	0.02
h ($Wm^{-2}K^{-1}$)	Opt - 3A T_{HTS} (°C)	Design - 3A T_{HTS} (°C)	ΔT (°C)
25	188.22	188.93	0.71
50	171.48	171.87	0.39
100	163.68	163.90	0.22
500	157.12	157.35	0.23
h ($Wm^{-2}K^{-1}$)	Opt - 4A T_{HTS} (°C)	Design - 4A T_{HTS} (°C)	ΔT (°C)
25	228.62	233.59	4.97
50	192.79	195.71	2.92
100	177.25	179.29	2.04
500	165.23	166.37	1.14

In order to have a clearer overview of the operation of the final design, a characteristic curve that displays the HTS average temperature as a function of the TEC feed current and of the well fluid convection coefficient is illustrated in Figure 8. As already observed in the previous analyses, the performance of the system is enhanced when high well fluid convection regimes occur. At high TEC feed currents the performance of the system is more sensitive to the convection coefficient than at low I_{feed} , as it can be noticed from the curve slopes on the h - T_{HTS} plane. On the I_{feed} - T_{HTS} plane, instead, it can be observed the HTS electronics temperature reaches a minimum at I_{opt} , which varies for different conditions of well fluid convection. The I_{opt} front is highlighted with red line. The optimal operating current changes more rapidly

with h at low convection regimes, where the excessive heat rejection is crucial, and engages a flatter trend while the convection coefficient grows.

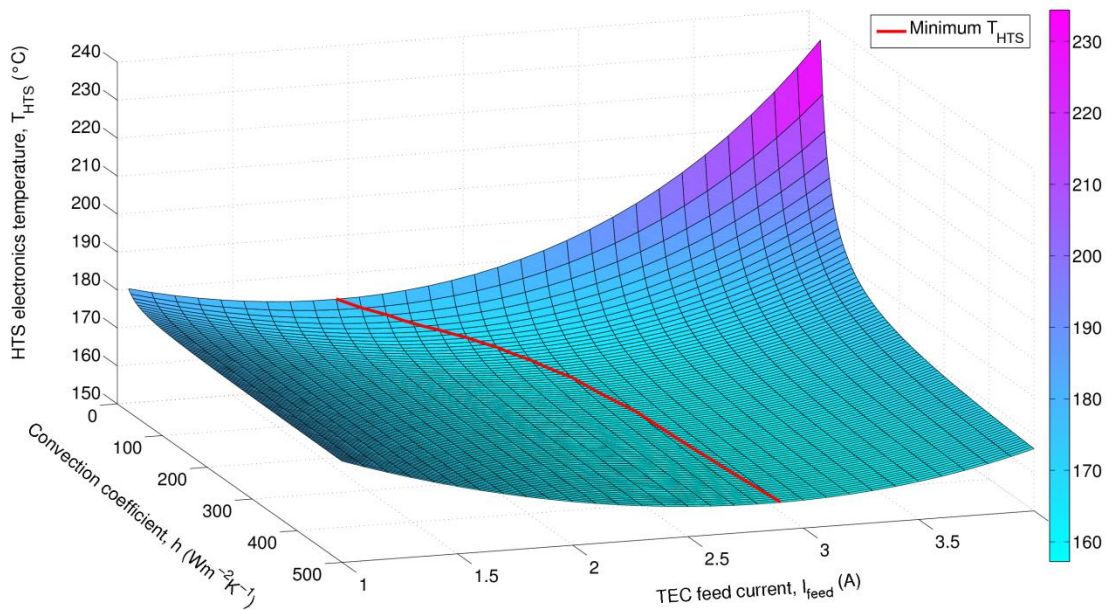


Figure 8. Characteristic curve of the finally designed TEC integrated system. The plot reports the simulated performance of the cooling system, in a $200\text{ }^{\circ}\text{C}$ environment, as HTS electronics temperature vs. convection coefficient and TEC feed current. The minimum HTS electronics temperature, for each operating condition, is highlighted by a red line. The color bar expresses the HTS electronics temperature in degrees Celsius.

4.4 Model validation

The system illustrated in Figure 7 was manufactured and assembled as shown in Figure 9. Thermal grease was used to interface the heating components to the chassis, lead wires were installed to feed the two sets of electronics through external power supplies, and type-K thermocouples were installed to monitor the temperature profile within the tool.

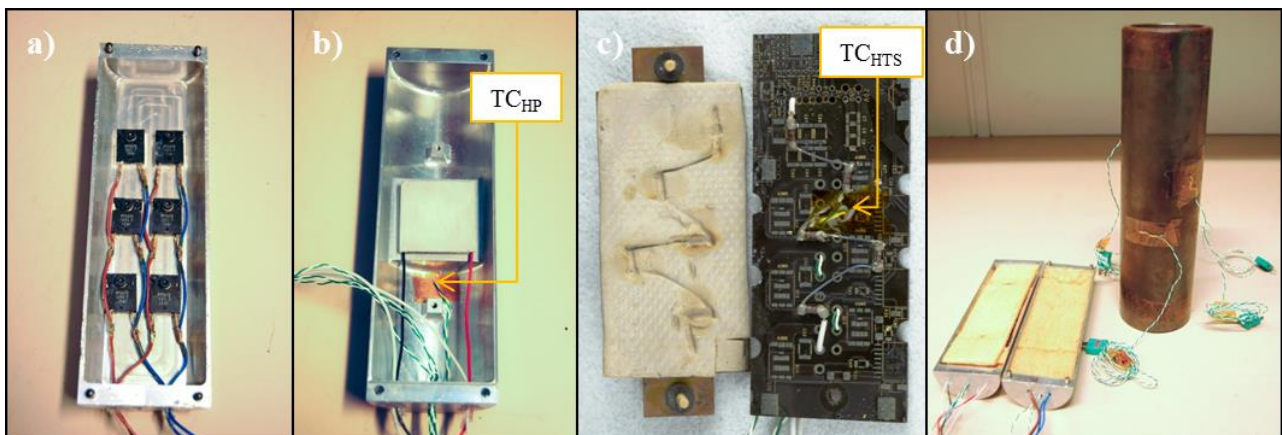


Figure 9. Illustration of the manufactured components. Six resistors were installed on the chassis bottom half to reproduce the HTNS electronics (a). The TEC was located in the chassis top half, with two threaded holes for implementing the clamping system; the

thermocouple TC_{HP} measured the temperature on the hot side of the TEC(b). Five resistors were soldered onto the PCB, to simulate the HTS electronics, and coupled with the soft thermal pad and the heat spreader (c); the thermocouple TC_{HTS} measured the temperature of the PCB. The two halves of the chassis were finally filled with thermally insulating foam and inserted into the metallic housing; the temperature of the housing was monitored by four thermocouples (d).

The assembled tool was tested in a dry and ventilated hot environment, where a fan recirculated air at the set-point temperature T_{oven} . *Power Supply 1* provided the electric power to the TEC, while a voltmeter and a current meter measured the feed voltage and current, respectively. *Power Supply 2* provided the feed power to the test electronics. A *Data Acquisition System* monitored and recorded the temperature distribution within the tool. The schematic of the experimental setup is reported in Figure 10.

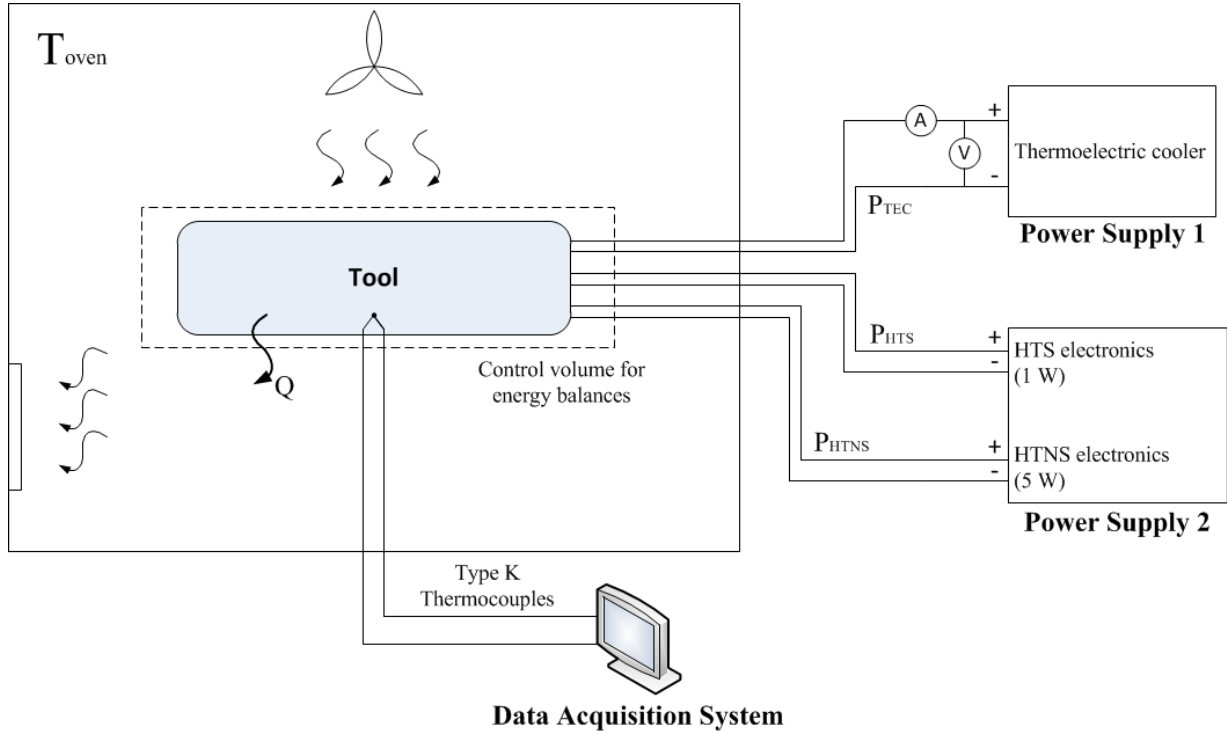


Figure 10. Schematic of the experimental setup. The main components characterizing the experimental validation of the model are illustrated.

Two different ovens, in size and air flow capacity, were used to test the tool at 180 °C, 190 °C, and 200 °C. For every oven temperature, the TEC feed current was varied between 1 A and 4 A, and the steady state temperature distribution across the tool was recorded. Furthermore, each test was characterized by the calculation of the average heat transfer coefficient \bar{h}_{exp} , which described the heat transfer, mainly driven by convection, occurring at the steady state between the tool housing and the oven environment. Equation 18 was calculated from the balance of the energy fluxes through the control volume shown in Figure 10, and was used for this purpose. The term \bar{h}_{exp} provides the reference boundary condition for the model validation process.

$$\bar{h}_{exp} = \frac{(P_{TEC} + P_{HTS} + P_{HTNS})}{A_{housing} \cdot (\bar{T}_{housing} - T_{oven})} \quad (18)$$

where \bar{h}_{exp} is the average heat transfer coefficient at the tool housing surface; P_{TEC} , P_{HTS} , and P_{HTNS} are respectively the electric feed powers of the cooler, of the HTS electronics, and of the HTNS electronics;

$A_{housing}$ is the outer surface area of the housing; $\bar{T}_{housing}$ is the average of the readings from the four thermocouples installed on the outer surface of the housing (see Figure 9d); and T_{oven} is the measured oven temperature.

The experimental temperatures were measured with type-K thermocouples and compared with the predictions from the model. An accuracy of ± 1.5 °C was used for the thermocouples, according to *IEC 584 Class 1*. Model data points were obtained from the corresponding 1 cm² square location within the finite-element geometry; actual measurements were compared with the average temperatures, while lower and higher error bands were introduced according to the model prediction for the maximum and minimum temperatures within the 1 cm² square.

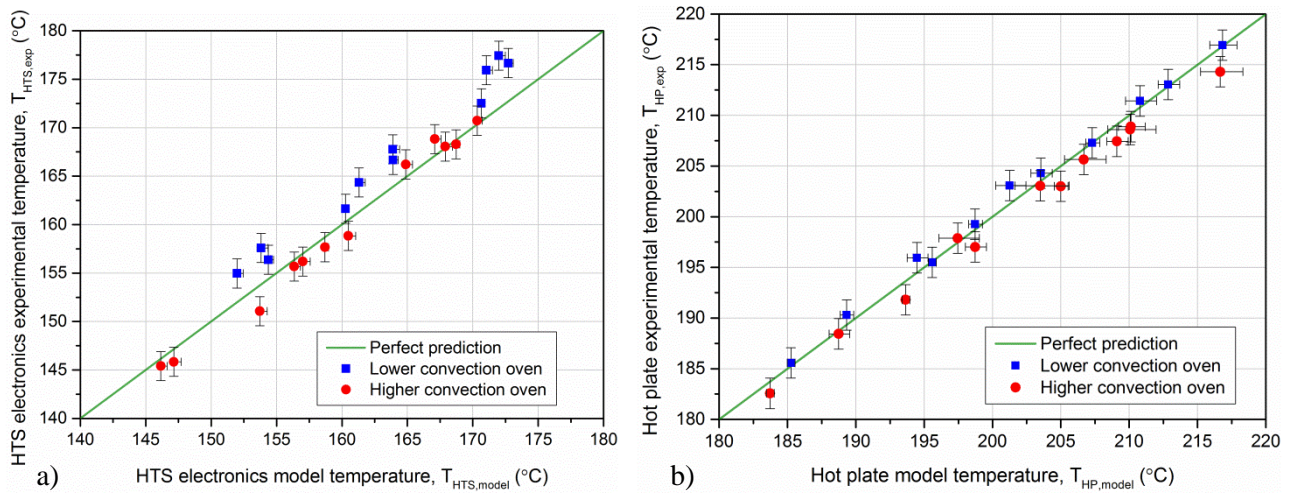


Figure 11. Comparison between experimental data and model prediction. HTS electronics temperatures are reported on the left (a) and hot plate temperatures are reported on the right (b). Results from all the tests from both the ovens are illustrated, and compared to the perfect prediction scenario.

Figure 11 shows the comparison between the experimental and the model temperatures, from the TEC hot plate (probe shown Figure 9b) and HTS electronics (probe shown in Figure 9c), which represent the most relevant temperatures for the system operation.

Table 4. Temperatures and parameters characterizing both the experimental procedure and the model validation. The first three columns define the boundary conditions of each test, while the last four columns summarize the TEC hot plate (HP) and HTS electronics temperatures, at stationary operations.

	T_{oven} (°C)	I_{feed} (A)	\bar{h}_{exp} ($Wm^{-2}K^{-1}$)	$T_{HTS,model}$ (°C)	$T_{HTS,exp}$ (°C)	$T_{HP,model}$ (°C)	$T_{HP,exp}$ (°C)
<i>Lower convection oven</i>	180.4	1.0	35.1	160.3	161.6	185.3	185.6
	180.7	1.5	30.9	154.4	156.4	189.3	190.3
	180.5	2.0	29.1	152.0	155.0	194.5	196.0
	180.3	2.5	28.2	153.8	157.6	201.3	203.1
	190.8	1.0	36.8	170.7	172.5	195.6	195.5
	189.9	1.5	31.0	163.9	166.7	198.7	199.3
	190.1	2.0	31.1	161.3	164.4	203.5	204.3
	190.6	2.5	30.3	163.9	167.8	210.8	211.4

	199.3	1.5	35.6	172.7	176.7	207.3	207.3
	199.5	2.0	32.3	171.0	175.9	212.9	213.0
	199.7	2.3	31.7	172.0	177.4	216.8	216.9
	T_{oven} ($^{\circ}C$)	I_{feed} (A)	\bar{h}_{exp} ($Wm^{-2}K^{-1}$)	$T_{HTS,model}$ ($^{\circ}C$)	$T_{HTS,exp}$ ($^{\circ}C$)	$T_{HP,model}$ ($^{\circ}C$)	$T_{HP,exp}$ ($^{\circ}C$)
<i>Higher convection oven</i>	180.7	1.0	65.7	158.7	157.7	183.7	182.6
	181.0	2.0	62.4	146.2	145.4	188.7	188.4
	180.7	3.0	57.7	147.1	145.8	197.5	197.9
	181.1	3.5	59.0	153.7	151.1	203.5	203.1
	190.8	1.0	72.9	168.7	168.3	193.6	191.8
	191.0	2.0	64.8	156.4	155.7	198.7	197.0
	190.2	3.0	60.8	157.0	156.2	206.7	205.7
	190.8	3.3	61.1	160.5	158.8	210.1	208.6
	200.4	1.5	75.9	170.3	170.7	205.0	203.0
	201.8	2.0	73.4	167.1	168.8	209.1	207.4
	200.3	2.3	66.3	164.9	166.2	210.1	208.9
	200.1	3.0	62.6	167.9	168.1	216.7	214.3

As indicated in Figure 11, experimental data and model forecasts revealed a good match, and proved the model can reproduce the performance of the real system with a good degree of accuracy. Figure 11a shows the majority of the data points for the HTS electronics temperature are close to the perfect prediction. Points from the tests at lower convection show a slightly worse match with the model, which predicts slightly lower HTS electronics temperatures. Based on the thermocouple readings and visual inspection of the system, no degradation at the cold side of the TEC was observed after the tests. No visible breakdown of the thermal interface material, which is rated for a maximum operating temperature of 200 °C, or change in the thermal resistances were detected. The mismatch in the model results can be attributed to the degradation of the TEC itself, which occurred in the ~50 hours of testing at high temperature in the higher convection oven, which were carried out first chronologically. The degradation of the module consists of a decrease in the thermoelectric effect and was detected as a drop in the temperature span across the TEC and a decrease of the TEC feed voltage at constant current [58]. The lower heat transport between the plates could therefore have led to higher experimental HTS electronics temperatures. The effects of the degradation are also accentuated when operating in low convection environments and high feed currents.

Figure 11b, instead, shows a very good match between experiments and model predictions for the hot plate temperatures, both for the lower and higher convection scenarios.

The previously described behavior can also be observed in Figure 12, where a comparison between model and experiments is reported as a function of the TEC feed current. Experimental results show a good agreement with the model predictions and are able to reproduce the forecast trends with I_{feed} . Furthermore, the experimental data confirm the presence of an optimal operating current I_{opt} , as described in the section 4.3, and the trend is reproduced by the model. Although Figure 12c shows a slightly larger mismatch between predictions and experiments, for the lower convection scenario, the convex trend and the value of

I_{opt} are reproduced with good approximation. The observed I_{opt} values varied with the outer fluid convection regime, confirming the behavior predicted by the model. As expected and previously shown, lower electronics temperatures were obtained in the higher convection scenario.

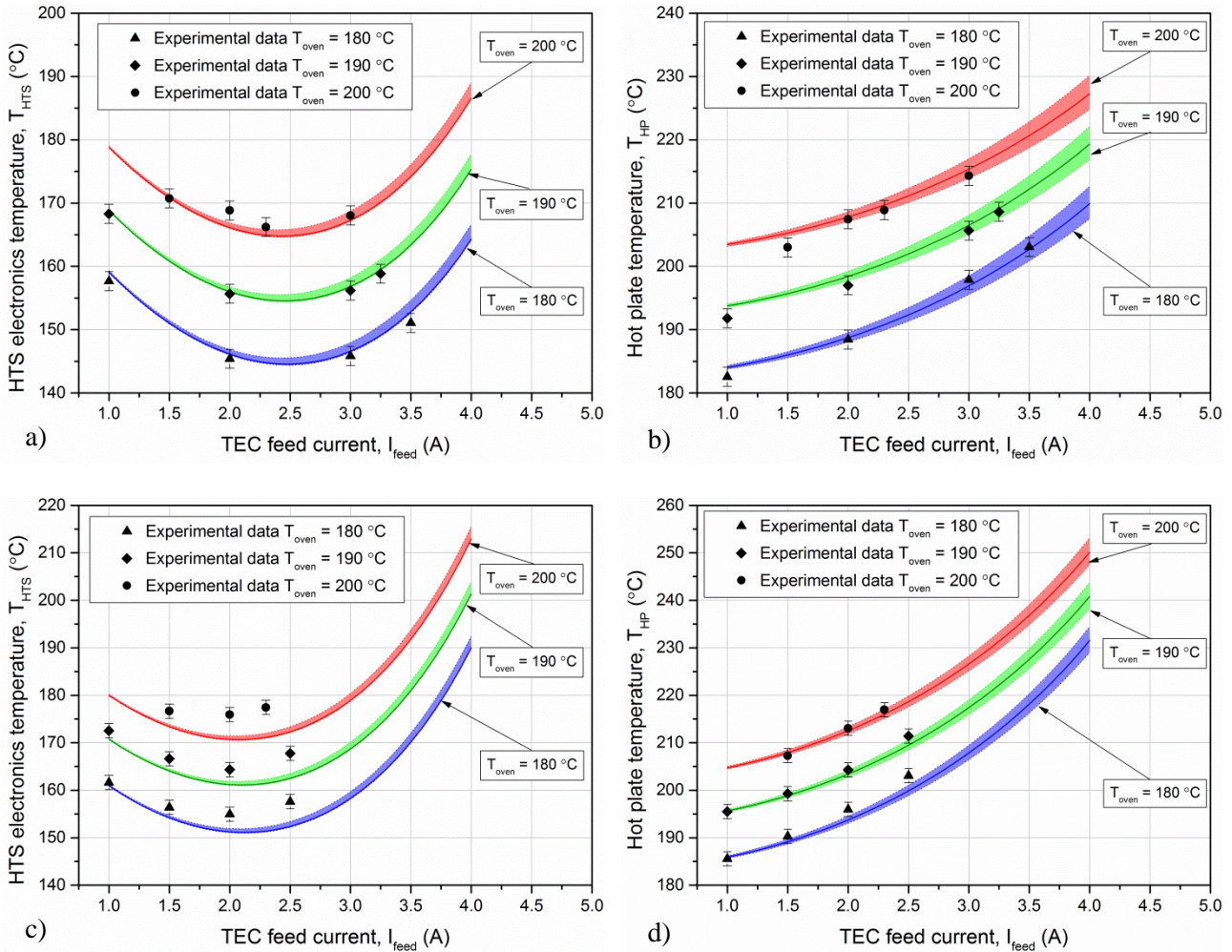


Figure 12. Comparison between experimental and modelling temperatures vs. TEC feed current, at different oven temperatures. The two figures on the top (a, b) report respectively the HTS electronics and the hot plate temperatures trends vs. TEC feed current, for the higher convection oven. The two figures on the bottom (c, d) report respectively the HTS electronics and the hot plate temperatures vs. TEC feed current, for the lower convection oven. The colored lines show the trends predicted by the model, defined by the maximum and minimum temperatures from the 1cm²-square model probe. The single points represent the experimental data.

5. CONCLUSIONS

This work presented and demonstrated a method of integrating a TEC into a system with specific design constraints, using topology optimization combined with a 3D finite element model of the system. This technique allows efficient integration of TECs by optimizing how they interact thermally with their surroundings, and is suitable for any TED application where the module must be mounted in a fixed volume. As a specific application, the optimization method was used to aid in the design of an actively cooled

electronics unit for a downhole oil well intervention tool, and to optimize the integration setup of a commercial thermoelectric cooler. The geometry to be optimized and the problem-related governing equations were implemented in COMSOL Multiphysics, together with the SIMP topology optimization approach. The model was used to optimize the distribution of aluminum and thermally insulating material within the unit, so the temperature-sensitive electronics could be maintained at a minimum temperature. The system was optimized for several well conditions and for the TEC feed current, and different design concepts were generated and analyzed. When heat rejection was critical (high TEC feed currents and low convection regimes) the mass of aluminum increased for better conduction out of the tool to the well; when the heat rejection was not critical (low TEC feed currents and high convection regimes) the thermal protection of the cooled electronics was prioritized, and the use of aluminum was significantly lower than the previous cases in favor of the thermal insulator. Optimized systems were found to cool the electronics down to a temperature 37 °C colder than before optimization. Furthermore, the optimization process proved to be not significantly sensitive to the convection range, but highly sensitive to the operating current of the TEC. An optimal operating current, which minimizes the temperature of the HTS components and depends on the well fluid convection regime, was found. This analysis highlighted the importance of a control system that would always seek the best operating conditions for the cooler.

Topology optimization was used to implement the final design of the electronics unit, which simulations predicted to perform very closely to the optimized systems. The final design was manufactured and tested in an experimental setup, at different operating conditions. Model predictions reproduced experimental results with good agreement, replicated the predicted optimal feed currents, and demonstrated the effectiveness of the design method. Topology optimization was shown to be a powerful design tool that can be combined with a TED model to yield optimized designs for thermoelectric integrated systems.

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