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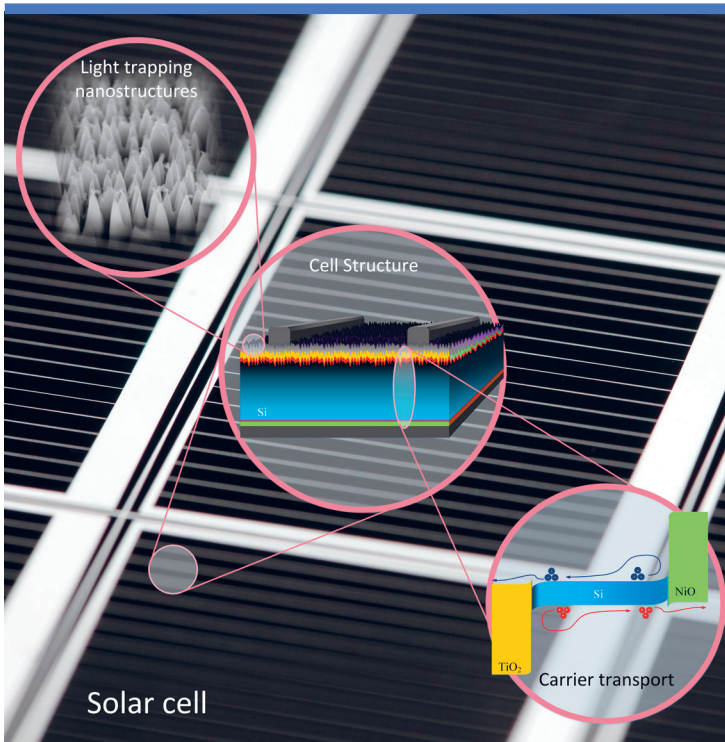
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Light trapping nanostructures

Cell Structure

Si

Solar cell

TiO₂   Carrier transport   NiO   Si

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Maksym M. Plakhotnyuk
PhD Thesis May 2018

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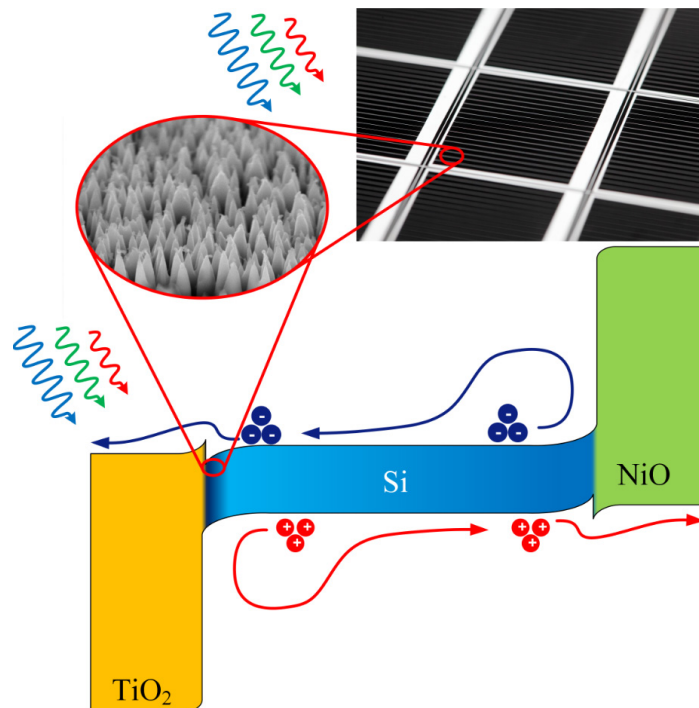Department of Micro- and Nanotechnology

Nanostructured Heterojunction Crystalline Silicon Solar Cells with Transition Metal Oxide Carrier Selective Contacts

Maksym M. Plakhotnyuk

THESIS FOR DOCTOR OF PHILOSOPHY DEGREE

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The title of the Ph.D. thesis:

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UiO : **University of Oslo**

Freiberg Instruments

Preface

This document concludes my last three years as a Ph.D. student at the Silicon Microtechnology group, Department of Micro- and Nanotechnology (Nanotech), Technical University of Denmark (DTU). It also summarizes more than three years of intensive learning, laboratory work, and personal search, challenging trails, falls, and rises. This work was funded by DTU internal fund as a proof of concept Ph.D. project. The scope of the project has been to explore new conceptual transition metal oxide carrier selective contacts in high-efficiency crystalline silicon solar cells with improved light trapping black silicon nanostructures and graphene top contact. After many experiments, tests, discussions I soon realized that it was a very ambitious plan considering the projects goals and realization period, available equipment at the time. Nevertheless, I think I ended up with very interesting results and promising new concepts.

Fortunately for me, I was responsible for carrying all the process development, device fabrication, and characterization. It gave me a chance to choose the interesting direction in my research, explore new ideas, and find collaborators in different parts of the world as well as within DTU and deliver this work to you.

Shortly, this work is about testing new concepts in the fabrication of crystalline silicon solar cell that could lead to a much cheaper solar cell with low toxic materials and with the simplified process flow. One of the concepts, transition metal oxide carrier selective contacts, such as TiO_2 and NiO films, deposited by atomic layer deposition technique and RF sputtering, will be discussed in Chapter 3 and 5. In Chapter 4, I will present the results on highly efficient light trapping nanostructures, so-called black silicon. All the tested processes were applied in the fabrication of heterojunction silicon solar cells and these results are briefly presented in Chapter 5. Even though most process development had remarkable results, the final fabricated solar cells displayed some severe defects that requires further analysis and device optimization.

Many of these results were possible to achieve only with support of other experts and friends from the DTU Nanotech, Danchip, Energy and Physics, bachelor and master students, external collaborators from the University of Oslo, Martin Luther University Halle-Wittenberg, Fraunhofer CSP, SASTRA University, University of New South Wales and Freiberg Instruments Inc. Since the goal of this Ph.D. thesis is to show what my contribution has been, I will underline my personal input and contributions from others.

While on this project, I attended the QUANTSOL Ph.D. summer school on photovoltaics in Austria. The results of this thesis were presented as an oral and visual presentation at the international conferences on nanotechnology and photovoltaics in Stockholm, Singapore, Munich (EAMC, PVSEC-26, EU PVSEC-32, respectively). Two applications for patents were filed with the design of high-efficiency silicon solar cells with metal oxides carrier selective contacts. Two articles were submitted for publications and two other articles are under preparation. Hence, the knowledge attained while working on this project is transferred to other researchers in the Silicon Microtechnology group for use in recent and future projects on solar cells.

Finally, I would like to express my best gratitude to my family and friends who believed in me and provided support all the time.

"If You Want To Go Fast, Go Alone. If You Want To Go Far, Go Together."

Chinese proverb

*To my beloved wife Lesia, son Maksym Junior and daughter Anna -
for their support, patience, and belief in me during this time. . .*

*To my parents who will never see this work, but have always been
proud of. . .*

Abstract

One of the most severe challenges man is facing today is to satisfy the need for energy without harmful environmental consequences. This complicated, grand challenge must be met by a wide range of solutions; among these are more efficient use of resources and replacement of fossil fuels by renewable energy sources. Any sustainable, renewable energy system must directly or indirectly rely on solar energy. Photovoltaic or solar cells are already efficient and reliable sources of electricity from solar light, but even though their cost has decreased significantly in recent years, solar cells are still far too costly for a competitive production of bulk grid power. The challenge within the solar cell field is thus to reduce the costs involved in solar cell production without sacrificing efficiency and reliability; actually, the efficiency should better improve towards 25 % or more, since the cell efficiency strongly affects the overall economy of a solar cell power plant. Currently, most of the solar cell market is based on 180-300 micrometer thick crystalline silicon wafers, and approximately 50 % of the cost is due to the cost of the material. To reduce material costs, introducing thin-film cells is a promising alternative, but a limitation in thin film solar cell technologies is that the absorptivity of light is quite weak, in particular for indirect band gap materials like silicon. This limitation may be lifted by application of photon trapping strategies that can increase the absorptivity of thin photo-absorbers by orders of magnitude at longer wavelengths. Another proven approach in solar cell optimization is carrier selective contacts, such as conventional amorphous silicon, or wide bandgap metal oxide semiconductor.

In this Ph.D. thesis, I present several new ideas for novel silicon-based solar cells to develop efficient solar cells that can be fabricated in a low thermal budget, and with the low-cost fabrication procedure using only abundant ecocompatable materials. The main photo-absorber is lightly doped p-type silicon (1.12 eV band gap) with a thin n-type TiO_2 (3.2 eV band gap) film on top. This structure forms a p-n heterojunction that effectively separates the photo-generated electron hole-pairs since the TiO_2 and silicon conduction bands are aligned facilitating electron transport, while a ~2 eV valence band energy barrier prevents hole transport.

The electrons transported in the conduction band through the TiO_2 to the surface are conducted laterally by a metal grid or continuous transparent conductive oxides (TCO) such as Aluminum Zinc Oxide (AZO) with high conductivity, highly transparency (optical losses 10%) electrode layer. On the backside, silicon was coated with complementary to TiO_2 thin film of NiO. NiO is a p-type wide bandgap (3.6 eV) semiconductor. In connection to silicon it forms a p-p isotype heterojunction with excellent valence band matching and creating hole conducting and electron blocking layer. As a back contact, I used high work-function metals to form an additional potential barrier against electron transport, while the holes could easily conduct to the metal. This basic structure was combined with micro-and nanostructuring of the silicon surface prior to fabrication to reduce optical reflectance below 1 % and to enhance light trapping inside the absorber layer. All fabrication procedures were completed at temperatures close to room temperature with a maximum of ~200 °C in a single step, and thus the thermal budget became unusually low.

The overall Ph.D. thesis project had four main research phases. In the first phase, the basic TiO_2-Si heterostructure was investigated on planar silicon wafers. Here, I focused on development and optimization of fabrication procedures for obtaining excellent TiO_2 passivation quality, high-performance junctions and efficient lateral transport. In addition, I found that the atomic layer of Al_2O_3 between TiO_2 and silicon enhanced passivation properties and junction performance. Using atomic layer deposition (ALD) techniques, thickness and material composition of TiO_2 and Al_2O_3 were highly precisely controlled. The fabricated test structures of TiO_2 and Al_2O_3 showed high open circuit voltage V_{OC}=0.63 V) and short-circuit

current J_{SC}=20 mA/cm^2. Other metals with close by work function (Al, Ti, Ni) were tested to minimize current blocking effects in diode structure.

In the second stage, NiO-Si isotype heterostructure was tested and optimized to meet the best ohmic (hole conductive) properties. I fabricated and characterized NiO-Si structure similar to the TiO$_2$-Si structure. Using sputtering from NiO target and ALD techniques, I obtained conformal NiO films with excellent ohmic behavior but modest passivation quality.

Next stage, I optimized nanostructuring process for silicon surfaces with reactive ion etching (RIE) and obtained a so-called black silicon. Using low surface damage RIE strategy, nanostructured surfaces I obtained low reflectivity (~1 %) and surface recombination velocity (*SRV*~4 cm/s) in comparison to KOH-textured and plane silicon. Black silicon nanostructured surfaces were passivated with ALD Al$_2$O$_3$ grown at 200 °C and annealed at 400 °C.

Finally, after the previous three stages were completed, I applied our process development results in HIT-type architecture on the recent record silicon solar cell type. However, due to a combination of many new concepts the fabricated solar cells did not show excellent performance and needed further investigation and optimization.

Dansk Resume

En af de mest alvorlige udfordringer, som menneskeheden står over for idag, er at møde behovet for energi uden skadelige, miljømæssige konsekvenser. Denne enorme, komplicerede udfordring skal mødes med en bred vifte af løsninger; blandt disse et mere effektivt forbrug af ressourcer og en erstatning af fossile brændsler med vedvarende energikilder. Enhver vedvarende, bæredygtig energikilde er baseret direkte eller indirekte på solenergi. Fotovoltaiske celler eller solceller er allerede en effektiv og pålidelig kilde til elektricitet fra sollys, men selvom prisen på energi fra solceller er faldet markant de seneste år, er solceller stadig alt for dyre til fuldt ud konkurrencedygtig produktion af primær energi i elnettet. Udfordringen inden for solcelle-området er derfor at reducere produktionsomkostningerne uden at ofre effektivitet eller pålidelighed; faktisk skal effektiviteten helst forbedres til over 25 % eller mere, da solcelle-effektiviteten påvirker økonomien i et 'solcelle-kraftværk' markant. I dag er størstedelen af solcellemarkedet baseret på 180-300 mikrometer tykke krystallinske silicium skifer og ca. 50 % af omkostningerne skyldes rå-materiale alene. Tynd-films teknologi er et lovende alternativ med henblik på at reducere materiale-omkostningerne, men en begrænsning for tynd-films solcelle-teknologier er, at absorbansen af lys er lav, især for indirekte båndgabs-materialer, som silicium. Denne begrænsning kan måske blive overvundet ved at anvende strategier til at fange fotoner, såkaldt 'light trapping', og dermed øge absorptiviteten af tynde foto-absorbere med flere størrelsesordener for lange bølgelængder. En anden veldokumenteret tilgang i solcelle-optimering er ladningsbærer-selektive kontakter, som konventionel amorf silicium eller metal-oxid halvleder-materialer med bredere båndgab.

I denne Ph.D. afhandling præsenterer Jeg adskillige nye ideer til nye, silicium-baserede solceller med henblik på at udvikle effektive solceller, der kan blive fabrikeret i en billig proces med et lavt termisk budget og kun ved at bruge øko-venlige materialer, der findes i rigelige mængder. Den primære foto-absorber er let-doteret p-type silicium (1.12 eV båndgab) med en tynd n-type TiO_2 (3.2 eV båndgab) film på toppen. Denne struktur former en p-n hetero-overgang, der effektivt separerer de foto-genererede elektron-hul par, idet TiO_2 og siliciums ledningsbånd er tilpasset hinanden, så de faciliterer elektron-transport, mens et 2 eV valensbånd udgør en energi-barriere, der forebygger hul-transport.

De elektroner, der bliver transporteret i ledningsbåndet gennem TiO_2 til overfladen, bliver ledt lateralt af et metal-gitter eller et elektrode lag bestående af en kontinuer transparent ledende oxid (TCO) som fx aluminium zink oxid (AZO) med høj ledningsevne, høj transparens (optiske tab på 10 %). På bagsiden blev silicium dækket med NiO, som en komplementær tynd film til TiO_2. NiO er en p-type halvleder med et bredt båndgab (3.6 eV), som - forbundet til silicium - former en p-p isotype hetero-overgang med fremragende valensbånd match og som udgør et hul-ledende og elektron-blokerede lag. Som bagside-kontakt brugte Jeg metal med høj arbejdsfunktion for at forme en ekstra potential-barriere mod elektron-transport, mens huller nemt ledes til metallet. Denne basale struktur blev kombineret med mikro- og nanostrukturering af silicium-overfladen med henblik på at reducere den optiske reflektans til under 1 % og forøge 'light trapping' i absorber-laget. Alle fabrikationsprocesser blev udført ved temperaturer på maksimalt 200 °C i et enkelt trin og det termiske budget bliver derfor usædvanlig lavt.

Ph.D.-projektet havde fire primære faser. I første fase blev den basale TiO_2-Si hetero-struktur undersøgt på planare silicium skiver. Her fokuserede Jeg på udvikling og optimering af fabrikations-processer, der resulterer i fremragende TiO_2 passiverings-kvalitet, overgange

med høj ydeevne og effektiv lateral ladnings–transport. Desuden fandt Jeg ud af, at et atom-art lag af Al_2O_3 mellem TiO_2 og silicium forstærkede passiverings-egenskaberne og overgangens ydeevne. Ved at bruge 'atom-lags deposition' (ALD) kunne tykkelse og materiale-komposition kontrolleres meget præcist. Fabrikerede strukturer med TiO_2 og Al_2O_3 resulterede i høj tomgangs-spænding, (V_{OC} = 0.63 V) og kortslutningsstrøm (J_{SC} = 20 mA/cm^2). Andre metaller med lignende arbejdsfunktioner (Al, Ti, Ni) blev testet med henblik på at minimere blokering af strømmen i diode-strukturen.

I anden fase blev NiO-Si isotype heterostrukturer testet og optimeret med henblik på at opnå de bedste ohmske (hul-ledende) egenskaber. Jeg fabrikerede og karakteriserede NiO-Si strukturer svarende til TiO_2-Si strukturerne. Ved at bruge 'sputtering' fra et NiO target og ALD teknikker opnåede Jeg konforme NiO film med fremragende ohmsk opførsel, men moderat passiverings-kvalitet.

I næste fase optimerede Jeg nanostruktureringen af silicium overflader med reaktiv ion æts (RIE) og opnåede såkaldt 'sort silicium'. Ved at bruge en strategi fokuseret på lav overflade-beskadigelse i RIE opnåede Jeg lav reflektivitet (<1 %) og overflade-rekombinationshastighed (SRV~4 cm/s) sammenlignet med KOH-tekstureret og planar silicium. Overfladerne med sort silicium nanostrukturer blev passiveret med ALD Al_2O_3 groet ved 200 °C og varmebehandlet ved 400 °C.

Slutteligt, efter de første tre faser blev færdiggjort, anvendte Jeg vores proces-optimerede resultater i en HIT-type arkitektur, som er solcelletypen bag seneste rekord for effektivitet af silicium solceller. Men grundet en kombination af adskillige nye koncepter viste de fabrikerede solceller ikke fremragende ydeevne og der er behov for yderligere undersøgelse og optimering.

Acknowledgements

Maksym M. Plakhotnyuk

May 14, 2018

Kongens Lyngby

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Physical Constants

Avogadro's constant	$N_A = 6.022\,140\,857\,74 \times 10^{23}$ 1/mol
Boltzmann constant	$k = 1.380\,648\,8 \times 10^{-23}$ J K^{-1}
Dirac constant (Planck's reduced)	$\hbar = \frac{h}{2\pi} = 1.054\,58 \times 10^{-34}$ J$\cdot$s
Electronic Charge	$q = 1.602\,176\,62 \times 10^{-19}$ C
Planck constant	$h = 6.626\,070\,04 \times 10^{-34}$ J$\cdot$s
Electron rest mass	$m_0 = 9.108 \times 10^{-31}$ kg
Permittivity of vacuum	$\epsilon_0 = 8.854\,187\,817 \times 10^{-14}$ F m^{-1}
Permeability of vacuum	$\mu_0 = 1.256\,637\,061\,4 \times 10^{-6}$ V$\cdot$s
Thermal voltage at 300 K	$kT/q = 0.025\,86$ V
Wavelength of 1 eV photon	$\lambda_0 = 1.24\,\mu$m
Bohr radius	$a_0 = 0.529\,17$ Å
Speed of Light	$c_0 = 2.997\,924\,58 \times 10^8$ m s^{-1}

Nomenclature

AFM Atomic Force Microscopy

ALD Atomic Layer Deposition

$AM1.5$ air mass 1.5 global reference solar spectrum (ASTM G173-03)

AR anti-reflective

ARC Anti-reflective Coating

$a-Si$ amorphous silicon (Si)

AZO Aluminum Zinc Oxide

bHF buffered HydroFluric acid

BP British Petroleum (company)

BSF Back Surface Field

bSi Black Silicon (Si)

CCP Capacitively Coupled Plasma

CSC Carrier Selective Contact

$c-Si$ mono-crystalline silicon (Si)

$DRIE$ Dry Reactive Ion Etching

DT Direct Tunneling

DTU Danmarks Tekniske Universitet (Technical University of Denmark)

EDX Energy-Dispersive X-ray spectroscopy

EQE External Quantum Efficiency

FF Fill Factor

FNT Fowler-Nordheim Tunneling

FSF Front Surface Field

HCC Hole Conducting Contact

HIT Heterojunction with Intrinsic Thin layer technology

IBC Interdigitated Back Contact *silicon solar cell technology*

ICP Inductively Coupled Plasma

IPA Isopropyl Propanol Alcohol

IQE internal quantum efficiency

$Fraunhofer ISE$ Fraunhofer Institute for Solar Energy

IV Current-Voltage

J_{SC} Short-Circuit Current Density

JV Current Density-Voltage

KOH Potassium Hydroxide

LT light trapping

$MACE$ Metal-Assisted Chemical Etching

$mc-Si$ multi-crystalline or poly-crystalline silicon (Si)

MDP Microwave Detected Photoconductivity

MPP Maximum Power Point

$NOCT$ Nominal Operating Cell Temperature

$PECVD$ Plasma Enhanced Chemical Vapor Deposition

$PERC$ Passivated Emitter Rear diffused Contact

$PERL$ Passivated Emitter Rear Locally Diffused

PFE Poole-Frenkel Emission

PV Photovoltaic

PVD Physical Vapor Deposition

QE Quantum Efficiency

$QSSPC$ Quasi-Steady-State PhotoConductivity

RF Radio Frequency

RIE Reactive Ion Etching

SE Schottky Emission

SEF Surface Enhancement Factor

SEM Scanning Electron Microscope

SHJ Silicon Heterojunction

SRH Shockley-Read-Hall (recombination)

SRV Surface Recombination Velocity

UV ultraviolet

TAT Trap-Assisted Tunneling

TCO Transparent Conductive Oxide

TMA TriMethylAluminum

TMO Transition Metal Oxide

$UNSW$ University of New South Wales

V_{OC} Open Circuit Voltage

WBS Wide Bandgap Semiconductor

WEO World Energy Outlook

WKB Wentzel–Kramers–Brillouin approximation

XPS X-ray Photoelectron Spectroscopy

List of Symbols

A	absorptance	%
A_c	cell area	m^2
A_nano	nanostructure surface area	m^2
A_proj	projected surface area from nanostructured surface	m^2
B_rad	radiative recombination coefficient	cm^3 s^{-1}
C_n	electron Auger coefficient	cm^3 s^{-1}
C_p	hole Auger coefficient	cm^3 s^{-1}
d	thickness of anti-reflective coating	nm
D_it	density of interface states	1/cm^2
D_n	electron diffusivity	cm^2/s
D_p	hole diffusivity	cm^2/s
E_p	energy bandgap	eV
E_ph	photon energy	eV
f_p	photon frequency	Hz
f_i	fraction of silicon to air in the i'th layer	-
G	generation rate	cm^{-3} s^{-1}
g_sp	spectral generation rate	cm^{-3} s^{-1}
h	sheet thickness	m
I	current	Ampere
I_L	photo-current	Ampere
I_0	thermal recombination current	A
I_p	photo-current	A
J_diff	total diffusion current density through pn-junction	mA/cm^2
J_rec	total recombination current density	mA/cm^2
J_tun	total tunneling current density	mA/cm^2
J_D	dark current density through pn-junction	mA/cm^2
J_0	saturation current density	mA/cm^2
J_gen	generation current density	mA/cm^2
J_n	electron current density	mA/cm^2
J_p	hole current density	mA/cm^2
J_Σ	total current density through pn-junction	mA/cm^2
J_0	thermal recombination current density	mA/cm^2
J_SC	short-circuit current density	mA/cm^2
L_n	diffusion length of electrons	m
L_p	diffusion length of holes	m
N_C	effective density of states in conduction band	cm^{-3}
N_V	effective density of states in valence band	cm^{-3}
N_A	acceptor concentration	cm^{-3}
N_D	donor concentration	cm^{-3}
N_ph	spectral photon flux density	-
n	electron density	cm^{-3}
$n_\mathrm{z(k+n),eff}$	refractive index of effective medium	-

n_{air}	refractive index of air	-
n_{i}	intrinsic carrier density	cm^{-3}
n_{id}	ideality factor	-
n_{r}	refractive index	-
$n_{i=1,2,..}$	refractive index of layers $i = 1, 2..$	-
n_{int}	refractive index of intermediate layer	-
n_{Si}	refractive index of silicon	-
N_{S}	sheet carrier density	cm^{-2}
p	hole density	cm^{-3}
p_{c}	contact pitch	$\mu\mathrm{m}$
P_{in}	incident power density	$\mathrm{W/m}^2$
P	incident optical power	W
P_0	optical power at normal incidence	W
P_{el}	electrical output power	W
R	reflectance	%
R_{s}	series resistance	Ω
R_{sh}	shunt resistance	Ω
r_{sp}	rate of spontaneous emission	$\mathrm{cm}^{-3}\mathrm{s}^{-1}$
S_{eff}	effective surface recombination velocity	cm/s
S_{rear}	effective rear surface recombination velocity	cm/s
S_{front}	effective front surface recombination velocity	cm/s
T	absolute temperature	K
T_{r}	transmittance	%
T_{tun}	tunneling probability	%
U	recombination rate	$\mathrm{cm}^{-3}\ \mathrm{s}^{-1}$
U_{Auger}	Auger recombination rate	$\mathrm{cm}^{-3}\ \mathrm{s}^{-1}$
U_{rad}	radiative recombination rate	$\mathrm{cm}^{-3}\ \mathrm{s}^{-1}$
V	voltage	V
V_{j}	junction voltage	V
V_{OC}	open-circuit voltage	V
W	wafer thickness	$\mu\mathrm{m}$
W_{e}	edge length of cell	m
α	absorption coefficient	cm^{-1}
α_{a}	absorption coefficient with photon absorption component	cm^{-1}
α_{e}	absorption coefficient with photon emission component	cm^{-1}
α_{BB}	black-body absorptivity	%
$\Delta\eta$	separation of quasi Fermi levels	eV
ε	dielectric permittivity of material	-
η	power conversion efficiency	%
η_{g}	generation quantum efficiency	%
λ	wavelength	nm
μ_{n}	electron mobility	$\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$
μ_{p}	hole mobility	$\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$
ρ	resistivity	$\Omega\mathrm{cm}$
ρ_{b}	density	$\mathrm{g/cm}^3$
τ_{eff}	effective minority carrier lifetime	s
τ_{bulk}	bulk minority carrier lifetime	s
τ_{surface}	surface minority carrier lifetime	s
τ_{rad}	radiative minority carrier lifetime	s
τ_{Auger}	Auger minority carrier lifetime	s

τ_{SRH}	Shockley-Read-Hall minority carrier lifetime	s
τ_{p}	minority carrier lifetime of holes	s
τ_{n}	minority carrier lifetime of electrons	s
Φ_{ph}	spectral photon flux density	W/m^2
Φ_0	incident photon flux density	W/m^2
χ_{s}	electron affinity of semiconductor	eV

Chapter 1

Introduction

"How wonderful it is that nobody need wait a single moment before starting to improve the world."

Anne Frank, Anne Frank's Tales from the Secret Annex

In this chapter, the motivation for photovoltaics materials and device research will be discussed. This is followed by a global demand for solar cells as clean and renewable energy sources along with a discussion of commercial and emerging silicon PV technologies. Next, the carrier selective concept would be explained exemplified in recent record power conversion efficiencies in silicon photovoltaic cells. It will be introduced, followed by a discussion of doped and amorphous junction technology and atomic layer deposited transition metal oxides in solar cells. Finally, the outline of the thesis will be provided.

1.1 Personal motivation

The most important choices can shape our future far ahead. I made a choice – to make a difference, to keep this planet a clean and safe place for living for our kids and ourselves. How to make it clean and safe? We have to change our attitude to nature, to each other and think how we consume resources – it is all our common culture and it is atrocious in the majority. It needs to be changed, but it is a matter of change in our personal and social behavior.

I was just 3-year old and just two months before my sister was born in 1983 at a distance of 400 km from Chernobyl nuclear plant exploded. The radioactive cloud covered almost all Ukraine, neighbor countries and even reached Scandinavia. Within few years thousands of families, including mine, were diagnosed with different diseases related to radiation exposure. The consequences caused by harmful technologies to our environment in a big run for energy and technological domination can lead us to total degradation.

As a human being, I want to promote sustainable culture to people I can influence. As an electrical and nanotechnology engineer, with my knowledge I can also affect and work on the development of future technologies and make our environment cleaner and safer! For this and other reasons, I devoted last three years and most probably more in future to renewable technology development and promotion. From my perspective, solar cell technology can change the way we live and make our civilization more sustainable. Moreover, this thesis is about the path and effort I spent on making the world more sustainable with cheaper and more affordable solar cells.

1.2 Global demand for photovoltaic energy

1.2.1 Global energy

Modern society largely depends on consumption. Energy for civilization is like food for human. We use energy for heating in our houses, transport, goods production, communication, food and even for reading this thesis.
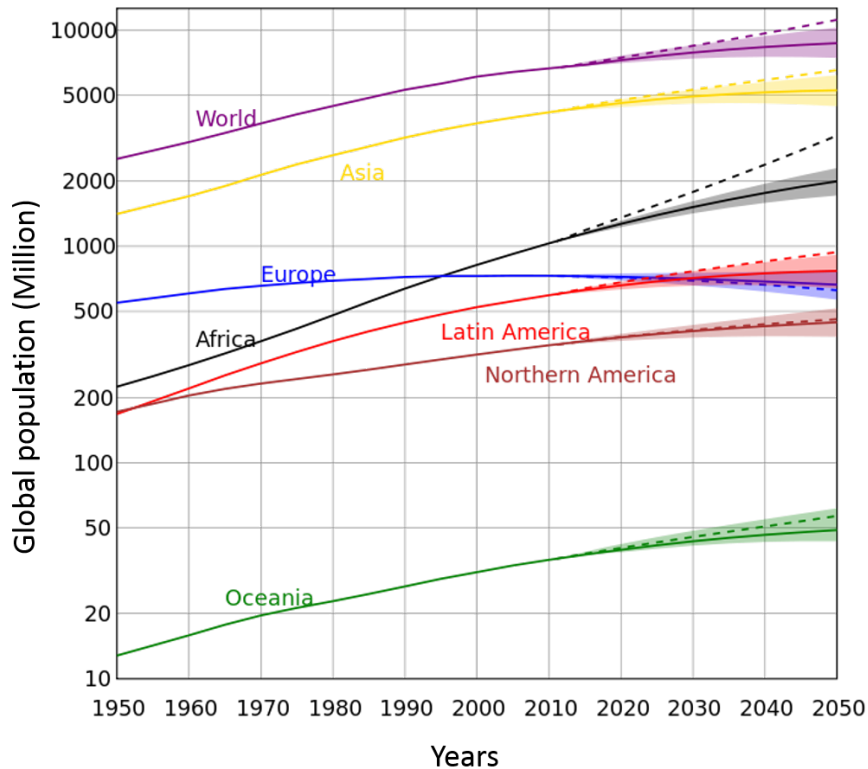
FIGURE 1.1: World population growth rate across the globe for all the continents: past, present and future [1]

Energy is never produced - it is always converted from one form to another. We convert it from one form to another, a more usable form of energy. Humanity developed many different methods for energy conversion. The most prosperous and technologically developed countries consume the most energy per inhabitant [2]. However, the economies are relatively stable and do not show rapid growth and, therefore, increase in power consumption. While developing countries, according to the World Energy Outlook (WEO) [3], display 30 % growth of energy consumption and at the same time these countries have the highest birth rate leading to increase in the global population. In May 2017, the world population was 7.5 billion people [4] and consumed 12.3 TW[1] of power [5], by 2050 the world population would be around 10 billion [1, 6] with the projected energy need for 18-20 TW or 16-18 billion toe[2] as shown in Fig. 1.1 and Fig. 1.2 [5]. It is the so-called supply-demand energy challenge and it could be and would be solved by increasing the total energy production [2].

A second challenge is that our energy infrastructure heavily depends on fossil fuels, like oil, coal, and gas. Fossil fuels resources, due to our intensive use, would be depleted in a while

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[1]TW – terra watts = 10^{12} Watt
[2]toe – tonne of oil equivalent (1 toe = 11.63 MW)
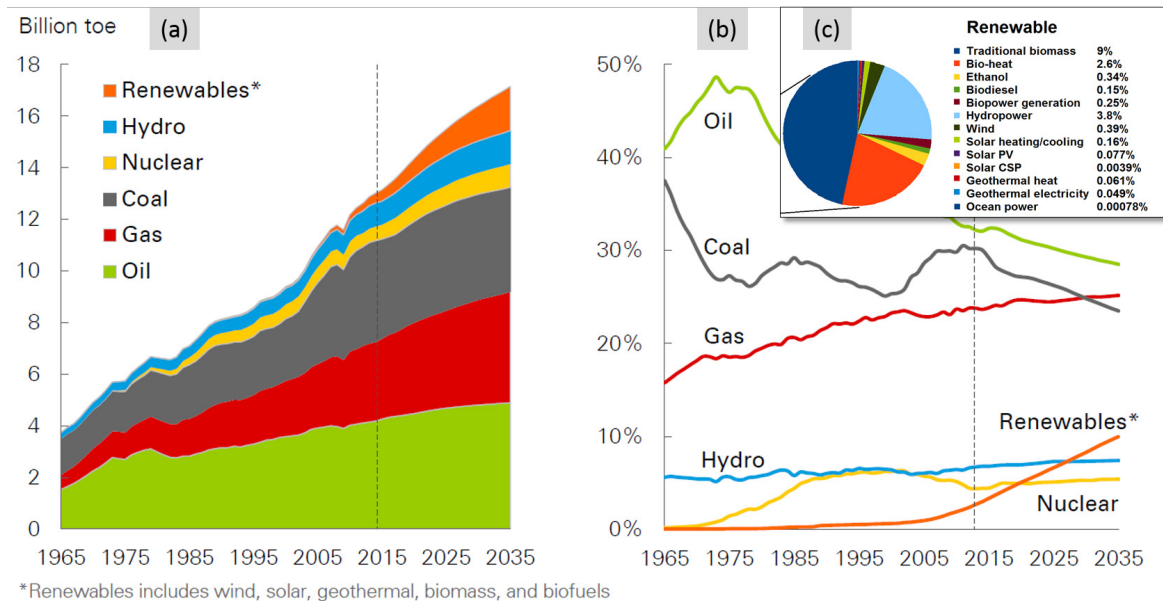
FIGURE 1.2: Energy consumption by sources from 1965 with forecast until 2035 according to BP Energy Outlook 2017 [5]. (a) primary energy consumption by fuel, (b) shares of primary energy sources, (c) shares of renewables (Note: Solar PV in the global energy market is only 0.077 %)

and require unconventional extraction methods, such as tar sands rectification, off-shore drilling, and fracking [2]. These methods use more energy to get fuel out of the ground and lead to catastrophic consequences for the environment.

Furthermore, by burning fossil fuels, we produce greenhouse gases like carbon dioxide (CO_2). Carbon dioxide accumulates in ocean and atmosphere forcing global warming and climate change. According to the carbon dioxide variation records (Fig. 1.3)[7] for the last 400 years, our civilization released two times more carbon dioxide in the last two centuries from industrial revolution than for the previous 100,000 years [8].

1.2.2 Role of photovoltaics as an energy source

In contrast, renewable energy could solve all of the above challenges. Renewable energy carriers are energy carriers that can be replenished by natural processes at the rate comparable to or faster than human consumption. Consequently, hydro-, wind, and solar energy are renewable energy resources. However, let us focus on solar energy. The surface of the Earth receives between 89-120 PWh[3] from the Sun, which is 10000 times more than we consume now for the whole year.

In other words, we can satisfy our energy needs only with solar energy if we install enough solar energy converters to electrical energy, like photovoltaic (PV) cells. Imagine that the territory of Spain covered with PV panels would suffice to cover all our energy needs without any CO_2 emission!

However, to compete in the energy market, the cost of converted solar energy should be comparable to the cost of fossil fuel energy. Therefore, levelized cost of electricity should be lower than the average cost of power in the grid, and it is known as 'grid parity'. The average levelized cost of PV-generated electricity for PV is still higher than the cost of electricity

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[3]PW – peta watt = 10^{15} Watt
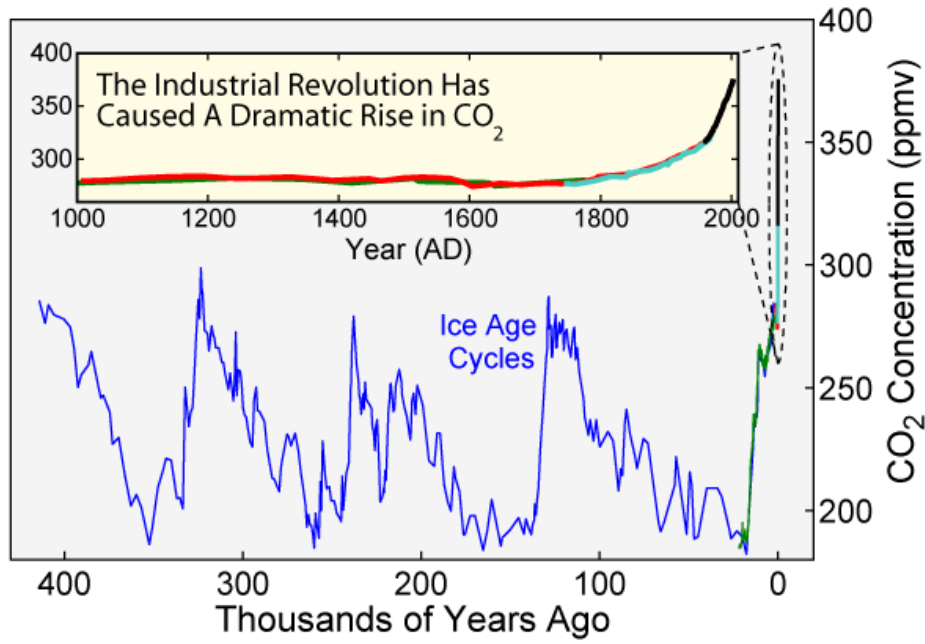
FIGURE 1.3: CO_2 concentration over the last 400,000 years [7]

generated from fossil fuels. An example of such levelized cost for different energy carrier is presented in Fig. 1.4 and given as Euro per kWh.

The cost of solar cell electricity can be lowered by decreasing the production cost increasing power output. For PV to be competitive, the cost of modules should be below 1\$/W and cells price – below 30 cents/W as shown in Fig. 1.5 (a). According to previous market trends and thankfully to lowering of production, PV market exhibits exponential growth potential as shown in Fig. 1.4. The highest growth rate, which is expected, is demonstrated in China and overall Asia-Pacific region.
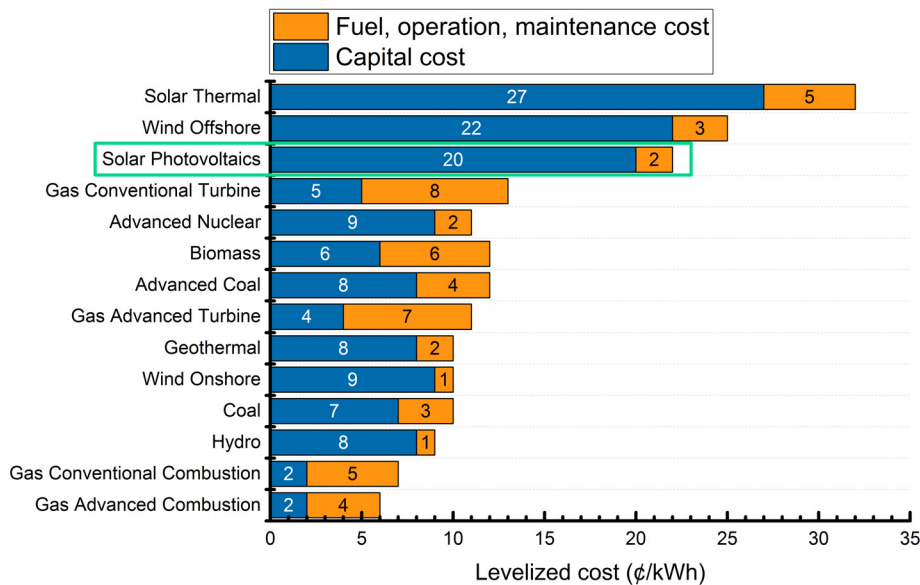
FIGURE 1.4: Levelized cost of electricity from different power sources for comparison [9]
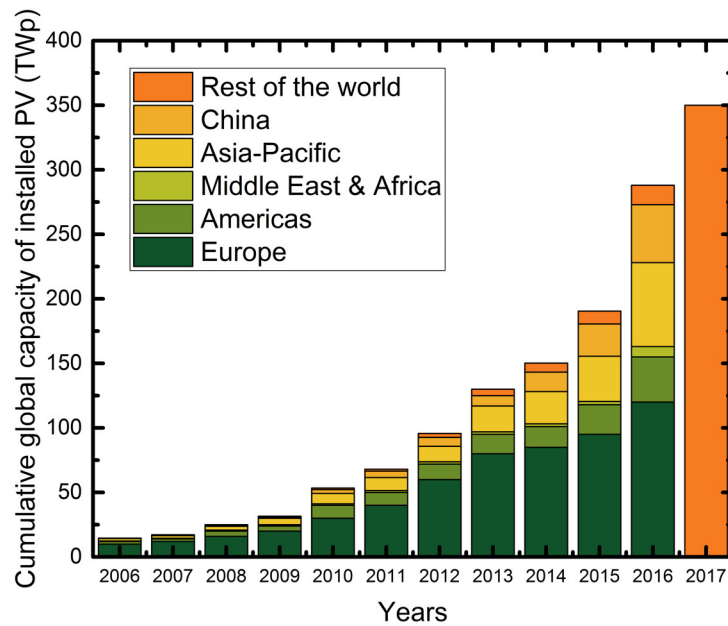
FIGURE 1.5: Cumulative installation capacity of photovoltaic systems in MWp grouped by region with from 2006 until 2015 and projection for 2016-2017. The data was adopted from Global Market Outlook for Solar Power [10]

1.2.3 Why silicon photovoltaic?

Nowadays, only silicon based solar cell technology fits these two requirements. Silicon is an abundant and heavily used element in the semiconductor industry and therefore has a relatively low market price and well-developed technology. At the same time, a silicon solar cell possesses the high enough efficiency among all other technologies and is approaching to 26.3 % power conversion efficiency [11]. In spite of once high production prices in the last decades, the PV market has grown at an average rate of 30 % annually since 1998, and in 2017 it will reach cumulatively 368 GW peak power with $35 billion in global revenue as shown in Fig. 1.5 [10]. The PV oriented business seems to have reached high maturity, i.e. moving from governmental subsidized activities towards the truly market-based industry. In addition, recent tremendous interest in renewable energy, caused by demand for reduction of global warming effect, leads to increasing shares of electric driven cars. While the electric driven car industry has already contributed to the increased demand for installation of solar cell modules all over the world. Moreover, for this reason, famous futurist Ray Kurzweil predicts solar cell industry dominance in 12 years [12]. Figure 1.6 (a) shows the price trend for silicon-based solar cells, and it has exponentially decreased since 1977. The cumulative PV capacity over the last decades allowed PV module cost reduction. This dependency is represented as logarithmic Swanson's Law learning curve in Fig. 1.6 (b).

The price drop for silicon over time became possible due to another reason – for several decades Si had been dominating materials and technology in semiconductor industry as well as in photovoltaic industry. Si shared more than 90 % of the total PV market splitting it shares between different Si-based technologies: multi-crystalline Si (mc-Si) (54.9 %), mono-crystalline Si (c-Si) (36 %), amorphous Si (a-Si) (2 %) in 2013 according to Fig. 1.7. Such significant market shares led to the development of different Si-based PV technologies and
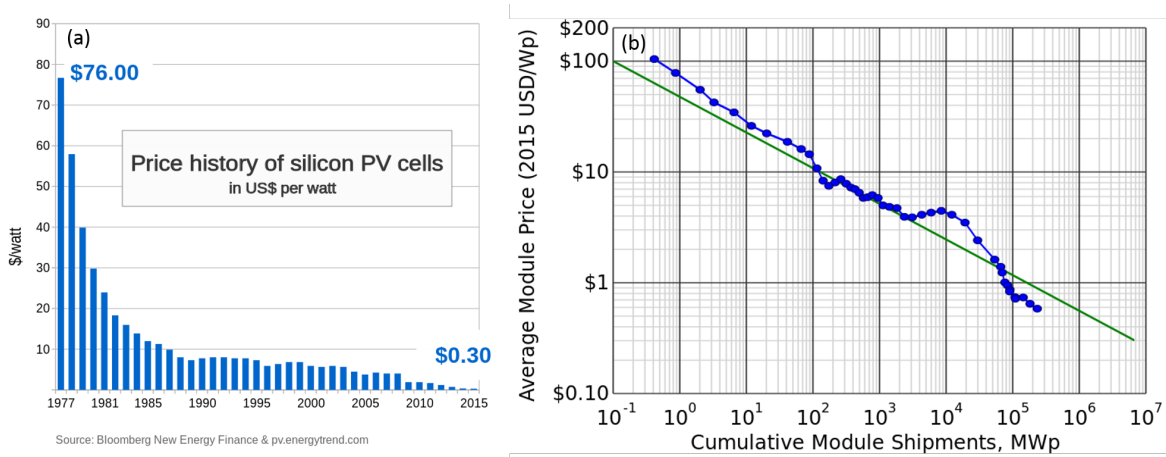
FIGURE 1.6: (a) Price reduction for silicon PV cells since mass production
started in 1977 till 2015, (b) Swanson's learning curve for silicon Si PV modules
[9]

cell designs with efficiency above 22 % up to 26.3 %.
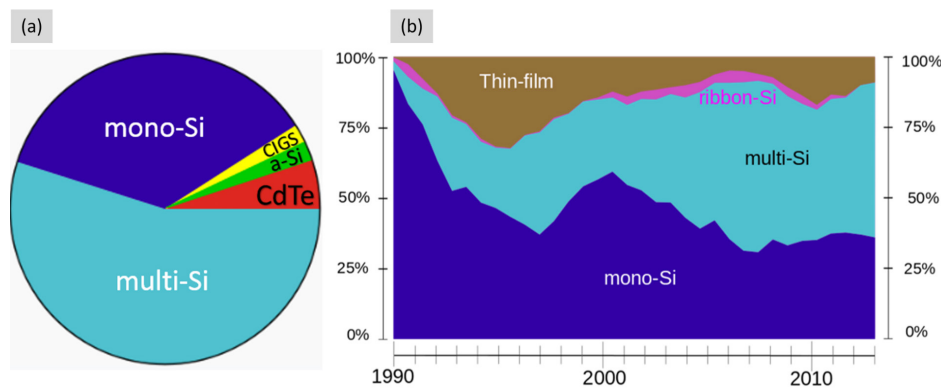
FIGURE 1.7: Global PV market shares by technology: (a) recent (2016) PV mar-
ket shares by dominating material technologies, (b) historical market shares
trends for PV material technologies [13]

Nevertheless, many different promising PV technologies could promise a combination of
high power conversion efficiency and low production cost, but Si has a huge potential for
its further usage in PV industry. Development of new technologies that could optimize one
or another parameter (improve efficiency or reduce production cost) will keep Si as a PV
market dominant further at least for several decades.

In summary, since the industrial revolution humanity extensively exploited non-renewable
fossil energy resources to satisfy its growing needs with growing population and, conse-
quently, a demand. Such policy resulted in numerous environmental problems, including
global warming and biosphere pollution. Luckily, renewables can help to change the culture
we, as inhabitants of Earth, have developed over the last 200 years. Thus, Si solar cells are
the most promising technology as a renewable energy source that can guarantee sustainable
future for and our future generations.

1.3 Physics behind solar energy conversion

1.3.1 Solar radiation

Every second our planet receives an enormous amount of energy from our star, the Sun, that is generated by nuclear fusion of hydrogen nuclei into helium. Every second the Sun generates approximately 3.846×10^{26} W, however, the Earth receives the much smaller amount of this energy equal to 1.7×10^{18} W. It is due to Sun's photosphere that we can see the Sun and feel the heat. The Sun's photosphere has around 6000 K temperature and emits a broad range of wavelengths radially directed around the Sun and of course towards the Earth. However, the most intense solar radiation follows Plank's Law of black-body radiation and has a maximum at 500 nm according to Wien's displacement law [14].

Propagation of sunlight depends on earth's atmosphere. The atmosphere attenuates many parts of the spectrum due to air molecules, dust, particularly water (H_2O), oxygen (O_2), ozone (O_3) and carbon dioxide (CO_2). Ozone absorbs hard ultraviolet light below 300 nm and protects live species from harmful UV effect. CO_2 absorbs radiation above 1 μm and thus preserving infrared radiation from dissipation creating a greenhouse effect.
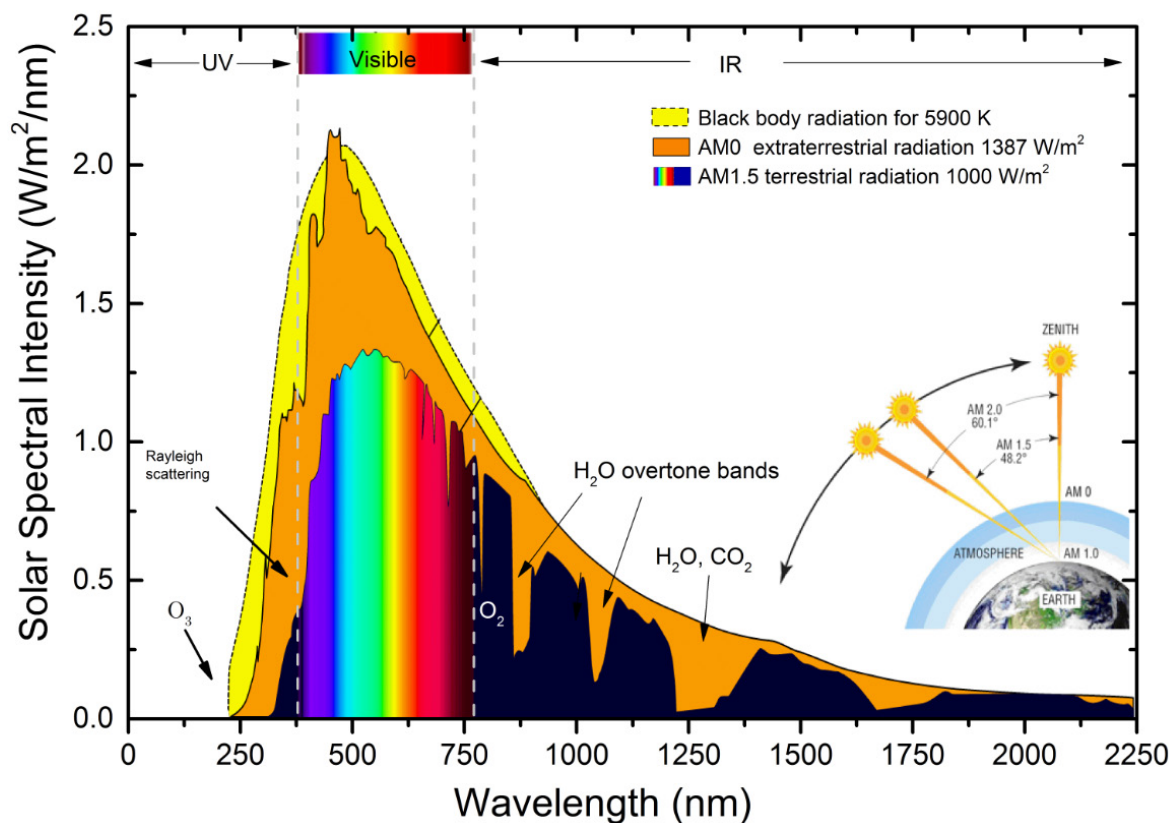
FIGURE 1.8: Solar spectral intensity for black-body radiation at 5900 K (yellow filled shape), AM0 extraterrestrial radiation (orange filled shape) and AM1.5 terrestrial radiation (dark blue and rainbow filled shape). AM1.5 radiation intensity is affected by atmospheric gases and suspended particles that reflect light back to the cosmos. Plotted data was adopted from National Renewable Energy Laboratory (NREL) data file [15] and the insert image was adopted from Newport company website [16].

It is valuable to relate the amount of sunlight at the earth's surface to air mass (AM) of the atmosphere due to the angle and atmosphere effect (insert in Fig. 1.8). Before entering the Earth atmosphere solar irradiance or sunlight intensity is equal to 1387 W/m^2 and noted as AM0 as is shown in Fig. 1.8. The sunlight power intensity that passes atmosphere and reaches earth's surface is equal to 1000 W/m^2 at the sea level and This sunlight power intensity is known as AM1.5 global standard and accepted by major research and industrial agencies.
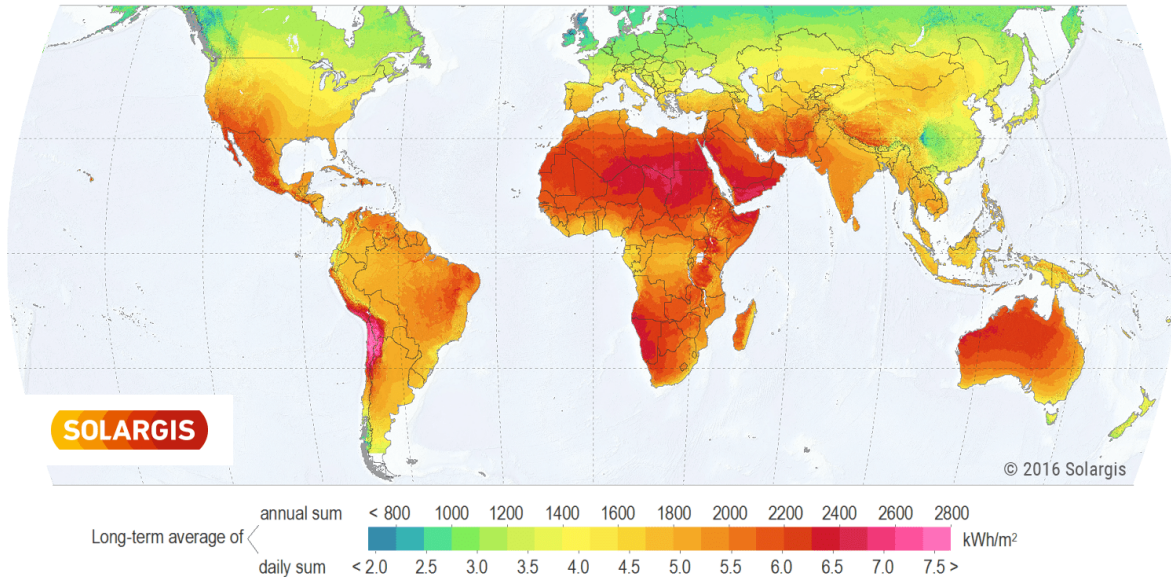
FIGURE 1.9: Map of solar global horizontal irradiation intensity represented in kWh per square meter [17]

Depending on the global position, the solar irradiance differs, but it is evident that the maximum values are found in tropical zones, elevated altitudes (mountains) and in deserts close to tropical and equator zones, however almost all the Earth surface has solar irradiance and therefore possibility to install solar cells. In Figure 1.9 the global solar irradiation intensity is shown with position and altitude effect.

1.3.2   Photovoltaic effect

Visible light is only a small fraction of the vast radiation spectrum as seen in Fig. 1.9. As known, light moves as a wave and it is useful to characterize light radiation by parameters associated with waves and have its frequency and energy according to Planck-Einstein relation:

$$E = h\nu = h\frac{c}{\lambda} \tag{1.1}$$

where h is Planck's constant, ν is photon frequency, c is the speed of light and λ is the photon wavelength. This relation is the foundation of photovoltaic effect; French physicist Alexander-Edmond Becquerel was the first to discover that [18]. He was the first who observed current and voltage bias on illuminated platinum electrode immersed in an acidic solution. He called this phenomenon as the photovoltaic effect and, therefore, in his experiment he invented the first solar cell. Of course, at that time, he did not think about

its efficiency. Now, it is known that photovoltaic effect occurs in various systems made of semiconductors, electrochemical substances, organic materials, dyes and others.

Modern solar cells in their majority are based on semiconductor junctions, complicated structure, and theory behind. In order to understand photovoltaic cell operation and to design one, we will briefly explain the most important principles of conversion of photon energy into electrical energy in the semiconductor. The first principle states that there must be at least a two-level system, where electrons can make a transition from lower (relaxed) to the upper (excited) energy state when they observe light [18, 19]. In a semiconductor, each atom has a certain energy level and since the bulk material has 10^{22} atoms/cm^3, these energy levels form continuous energy bands. The lower band is called valence band, the upper – conduction band. The gap between these bands is called a bandgap, and electrons cannot exist there.
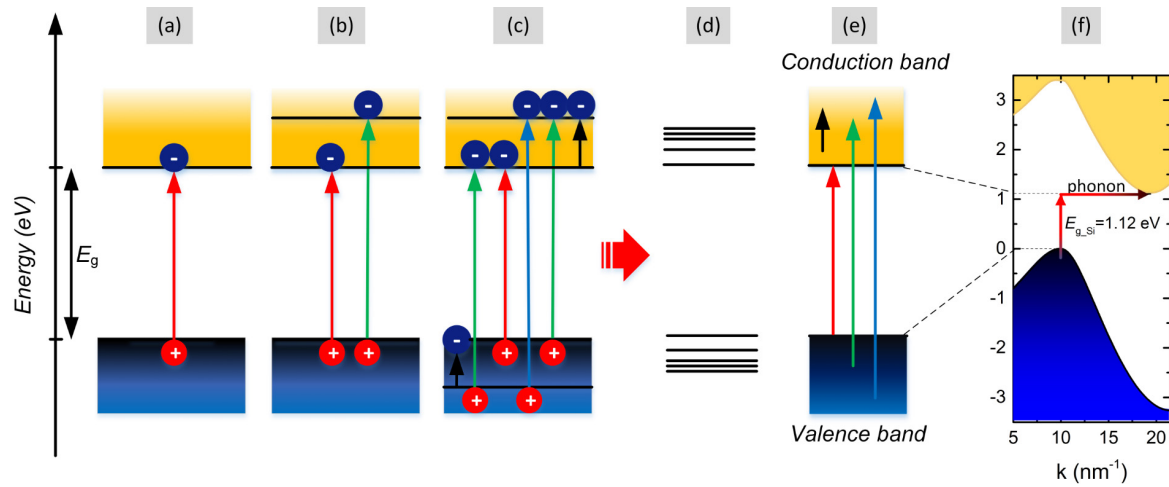
FIGURE 1.10: A two-level system can absorb photon only at a certain energy (wavelength) (a-e) with an increasing number of energy levels (towards the right). The color of arrows corresponds to the color of absorbed light, while (f) is band structure of Si. Note: black arrow corresponds to infrared radiation. The image was inspired by Altermatt Lectures series [14].

A semiconductor, like Si, can absorb light only for photon energy larger than energy bandgap E_g (for Si E_g=1.12 eV). Photon energies below E_g cannot be absorbed since these photons do not excited electrons enough to jump over the bandgap. Since the 1.12 eV Si bandgap corresponds to infrared radiation, Si solar cells cannot produce much electricity from heat, but only from visible light and near-infrared radiation. Also, generated electrons are affected with crystal structure and energy – momentum in the crystal plane (see Fig. 1.10 (e-f)). This effect creates a difference between valence and conduction band and is related to wave vector. Therefore, there are two types of semiconductor with the direct bandgap and the indirect like Si. In the case of a direct semiconductor, an electron can easily pass from valence to conduction band (Fig. 1.10 (e)), but in the indirect semiconductor, in our case Si, the excited electron requires also an energy momentum provided by vibrations in the crystal lattice (called phonon) (Fig. 1.10 (f)). Phonon is generated with the absorption of low energy photons (>1 eV), lattice vibration energy or heat.

If we assume each absorbed photon excites one electron, and all of these electrons flow to the contacts, we can calculate the maximum photon generated current density:

$$J_{\text{gen}} = q \int_{E_g}^{\infty} \Phi_{\text{ph}(E)} dE \qquad (1.2)$$

where q is electron charge, Φ_{ph} is the spectral photon flux density. The maximum generated current density for a Si solar cell is 46 mA/cm^2, i.e., there are about 10^{17} photons/cm/sec absorbed Si solar cells. The Si bandgap energy is equal to 1.12 eV and according to Eq. (1.1) it corresponds to the wavelength of 1.11 μm. Thus, Si is an indirect semiconductor; it absorbs a photon with 1.12 eV to excite an electron from the valence band and some additional energy to compensate momentum and reach conduction band. This explains why Si has broad absorption in comparison to direct bandgap semiconductors from II-VI, III-IV groups compound semiconductors like GaAs, etc. as shown in Fig. 1.13.

When a photon is absorbed in a semiconductor, its energy is converted to electrochemical potential and electrical energy through the generation of electron and hole pair or opposite charge carriers and electric current flow. The electron is a negative charge. An excited electron transfers to the conduction band leaving behind a positive covalent bond, called a hole. Since the electron and the hole have opposite charges, they tend to annihilate or recombine and create quanta of energy. Consequently, the main characteristic of the solar cell is to effectively separate electron and holes to avoid recombination to do useful work.

1.3.3   Principles of charge separation

Since this work is based on Si technology, most of the discussions and illustrations display and discuss Si based concepts, however most of the charge separation concepts are also transferable to other solar cell technologies. Conventional Si solar cells employ several charge separation mechanisms. The most commonly used mechanisms, since the first invention of the solar cell, is doped p-n homojunction with field effect and diffusion induced charge current (Fig. 1.11 (b-d, e, g). In other words, Si bulk material with n-type doping (for instance Phosphorous) is doped with p-type dopant (like Boron) to form different doping levels and a p-n junction close to one of the surfaces. A difference in doping levels leads to energy split in charge concentration in conduction and valence band known as quasi-Fermi levels for electron $E_{\mathrm{F_n}}$ and holes $E_{\mathrm{F_p}}$ and form an energy barriers in semiconductor leading to separation of electron and holes as depicted in Fig. 1.11 (h, g).

The second and more advanced charge separation mechanism is a heterojunction, formed by deposition of material with different energy bandgaps. Heterojunction on Si could be formed with deposition of another wider bandgap material such as amorphous Si (a-Si) with bandgap between 1.5-1.7 eV [20], transition metal oxides with bandgaps between 2.6-3.6 eV [21], dielectric tunneling films with bandgap above 4 eV [22] etc.) (see Fig. 1.11 (f, h)).

Effective charge separation leads to efficient charge transport to electrical terminals under electric field bias and efficient performance of a solar cell. All the charge separation mechanisms in solar cells introduce a junction that turns a solar cell into a diode device or more specifically into a photodiode. Therefore, to evaluate solar cell performance, its internal processes and external characteristics, a set of different diode parameters are used. Most important parameters that characterize solar cell performance are the total electric current density J (Eq. (1.3)), short-circuit current density J_{SC} (Eq. (1.4)), dark current density J_{D} (Eq. (1.5)), open circuit voltage V_{OC} (Eq. (1.7)), maximum generated power P_{max} (Eq. (1.8)), power conversion efficiency η (Eq. (1.9)) and nominal operating cell temperature (NOCT). More detailed discussion about solar cell parameters is described in Sect. 2.5. Brief description of these parameters are given below and visualized on Fig. 1.12.

The total electric current density in a solar cell is a difference between the short circuit current density J_{SC} and the dark current J_{D}
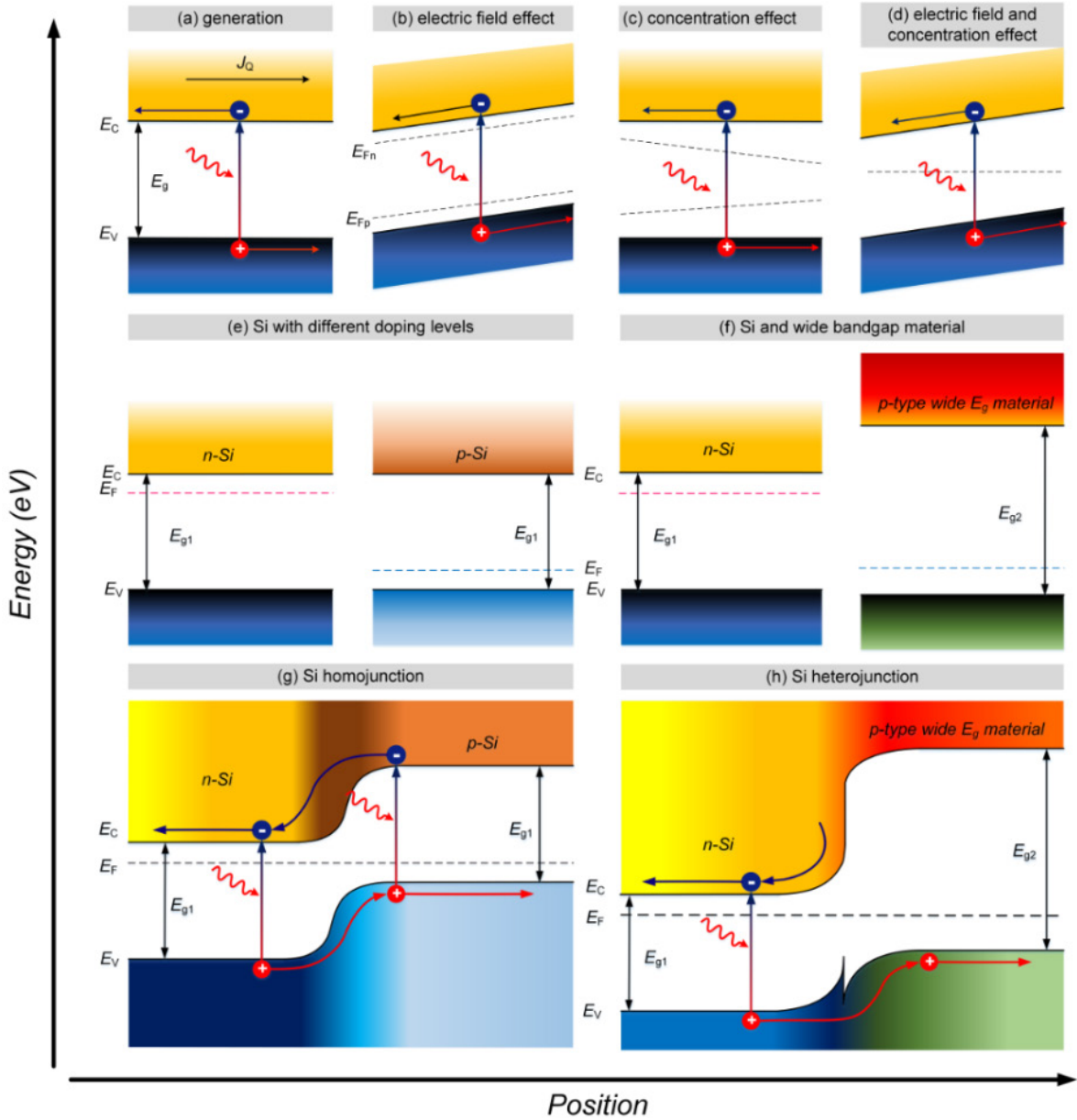
FIGURE 1.11: Charge transport and separation mechanisms in Si solar cells and principle of homo- and heterojunction formation. Note: each sub-Figure has explanation to its content

$$J(V) = J_{\text{SC}} - J_{\text{D}}(V) \tag{1.3}$$

The short-circuit current density J_{SC} is the maximum current from a solar cell when the voltage across the cell is equal to zero [23]. J_{SC} is related to the absorbed photon spectrum by measurement of cell's quantum efficiency (QE), which is the probability of the incident photon of energy E to be absorbed and converted to collected charge carriers.

$$J_{SC} = q \int_{E_g}^{\infty} \Phi_{ph}(E) \, EQE(E) \, dE \tag{1.4}$$

where E is the photon energy, E_{g} is the bandgap of the absorber (i.e. Si), $\Phi_{ph}(E)$ is the
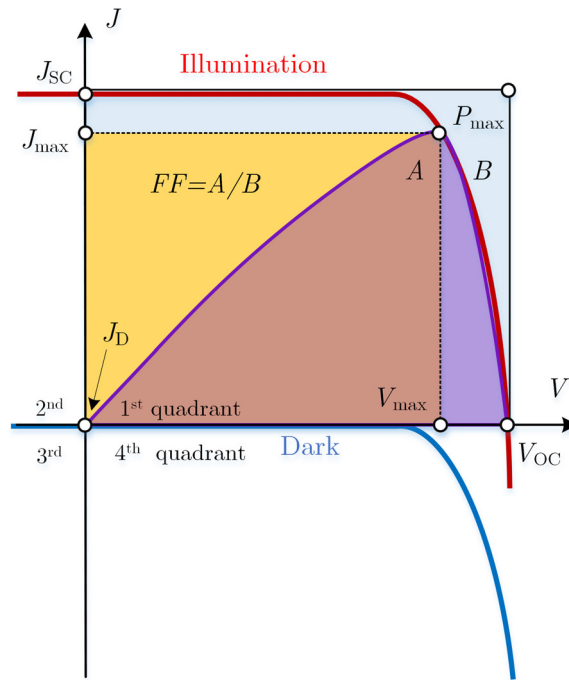
FIGURE 1.12: General current density-voltage characteristic curves of a solar cell under illumination and dark.

incident spectral photon flux density, $EQE\,(E)$ - is the external quantum efficiency. Obvious that the short circuit current density allows diagnosing absorption behavior of the solar cells.

While, the dark current density J_D is a voltage-dependent recombination current density.

Ideally, the short-circuit current J_{SC} is a quantity greater than zero at zero voltage. At dark conditions, J_{SC}=0 and the current-voltage behavior of the solar cell is the same as p-n–junction diode.

$$J\,(V) = -J_D\,(V) \tag{1.5}$$

The open circuit voltage, V_{OC}, is the maximum voltage available from a solar cell at zero current flow (J=0). The open-circuit voltage V_{OC} is defined as

$$V_{OC} = \frac{nk_B T}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right) \tag{1.6}$$

Here, T - nominal operating cell temperature (NOCT), J_0 and n are dark saturation current and diode ideality factor, respectively.

The NOCT is the temperature of cell operation in the field and is defined as the temperature reached by open circuited cells in a module under the certain conditions (for more details please follow the reference [24]).

The maximum power can be extracted by biasing the solar cell at a certain voltage where the JV product would be maximized. This voltage is labeled as V_{max}, and the corresponding current density is labeled as J_{max}. Note, that maximum current density and voltage values are not the same as short circuit current density and open circuit voltage values and correspondingly lower. Then, the maximum power point (MPP) is defined as

$$P_{\max} = A V_{\max} J_{\max} \tag{1.7}$$

where A is the areas of the solar cell.

Another important parameter of the solar cell performance is Fill Factor FF. The FF is defined as the ratio of the maximum power from a solar cell to the product of the open circuit voltage V_{OC} and the short-circuit current J_{SC}. According to the Fig. 1.12, the FF is a value that defines the sharpness of the JV curve [25]. The fill factor is defined by

$$FF = \frac{J_{\max} V_{\max}}{J_{SC} V_{OC}} \tag{1.8}$$

The power conversion efficiency or simply efficiency of a solar cell η is the most commonly used parameter to evaluate a solar cell performance and compare with another cells. Efficiency is given as a relation of a converted electric power to the incoming power from the sun:

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{A V_{\max} J_{\max} FF}{P_{in}} \tag{1.9}$$

The latest solar cell efficiency records could be found on a National Renewable Energy Laboratory website and efficiency chart [26] or as a semiannual report in Progress in Photovoltaics: Research and Applications journal [27, 28].

More detailed explanation and derivation above-mentioned solar cell parameters are found in Chapter 2 or elsewhere [20].

1.3.4 Silicon as a dominating energy material

As mentioned above in Sect. 1.2.3, more than 90 % of all commercial solar cells are made from Si even though other materials, i.e. III-V semiconductor, are theoretically more preferred because of direct bandgap absorption (See Fig. 1.10 (a)). The reasons why Si is still the dominating solar cell production material are that it is the second most abundant material on Earth (28 %), it offers material stability, well-developed industrial production and solar cell fabrication technology. And more important, it has relatively high power conversion efficiency. These facts lead to the competitive lowest cost of Si solar cells if compared to other solar cell technologies. The record efficiency for mono-crystalline Si solar cells was just recently reported equal to 26.3 % [11] and 20.8 % for multi-crystalline Si solar cell. These record efficiencies are very close to the theoretical limit of Si efficiency, known as the Shockley-Queisser limit and equal to 29 % in Si single-junction under one sun illumination at the room temperature [29].

Any increase in power conversion efficiency above theoretical limit is not possible. A semiconductor single-junction solar cell illuminated at AM1.5 spectral irradiance can only absorb a photon within this limit. Due to fundamental material properties such as Boltzmann, Carnot, internal emission, thermalization, transmission (photons with energy below energy bandgap) and fill factor losses are the reasons that solar cells cannot be 100 % efficient as shown in Fig. 1.13 (b).

Mono-crystalline silicon (c-Si) solar cell efficiency is limited with 29 % due to fundamental thermodynamic and quantum mechanics limitations as mentioned above and according to
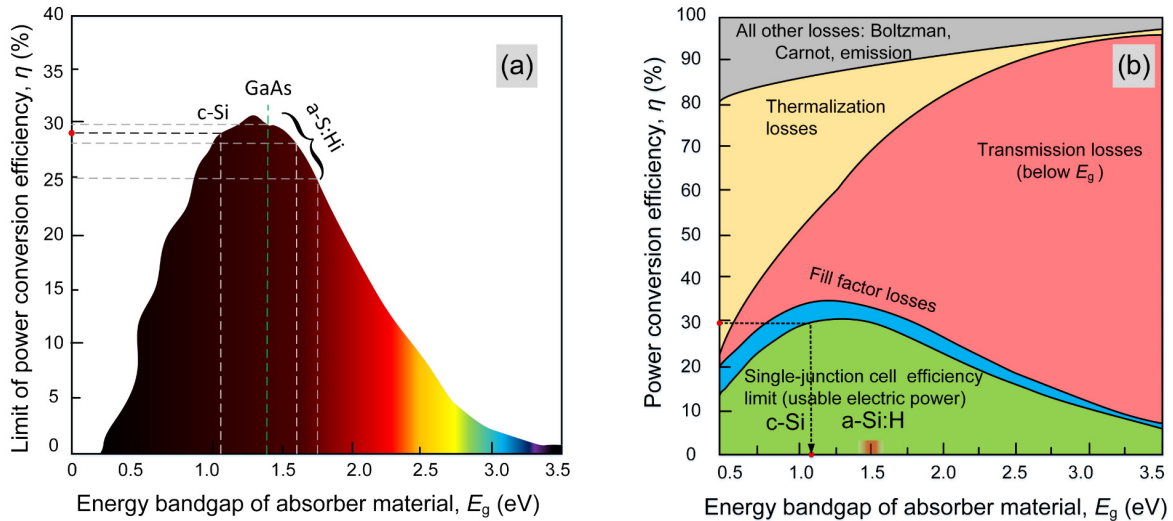
FIGURE 1.13: Theoretical power conversion efficiency limit of solar cells as a function of band gap energy at 300 K and AM1.5 spectral intensity. (a) Limits of power conversion efficiency that has the highest probability to be absorbed in semiconductor (usable part of photon energy) (The data is adopted from [29]), (b) total conversion potential and losses in semiconductor materials including Si (inspired by [30]).

Fig. 1.13. However, the limit of 29 % can be reached if we assume that all the losses are idealized, e.g. absorptivity approaches unity with ideal internal quantum efficiency (IQE[4]) and lossless charge separation and transport mechanism besides intrinsic radiative and Auger recombination. Keeping this in mind, real limitations in Si solar cells are presented below.

One of the significant limitations in Si solar cell is a very high refractive index of c-Si (~3.5). A polished Si wafer, on average, has more than 30 % of reflected incident light. In all the solar cell structures (Figs. 1.14-1.15) presented further, including homojunction and heterojunction high-efficiency solar cells this problem is solved with deposition of effective antireflective (AR) coatings. Second, Si as an indirect semiconductor with the weak absorption of light closes the energy bandgap. The solution is to incorporate an effective light trapping (LT) mechanism to reach the maximum possible absorptivity, with internal multi-reflectance until the light is totally absorbed in Si bulk. With efficient light trapping mechanism, optical absorptivity is maximized leading to main losses contribution from charge transport. Besides, the above-mentioned intrinsic limits, surface and crystal defects are the strong roots of losses due to the recombination. Crystal defects losses could be neglected with thinner and high-quality wafers. However, front and rear surface interface quality gain significance.

The second major limitation, according to Green [31], in c-Si solar cells is intrinsic limitation by Auger recombination. Solar cell efficiency can be improved with reduction of surface recombination velocity (SRV). The SRV depends on the recombination rate at the surfaces and excess minority carrier density and is expected to be small (S = 4 cm/s) for thick wafers (400 μm) with high bulk lifetimes (10 ms). Open circuit voltage, V_{OC}, has a logarithmic dependency on recombination within the solar cell active area and strong dependency on SRV above 10 cm/s, but it is entirely independent of optical absorption. In opposite, the short-circuit current density J_{SC} depends on optical absorption and is constant if SRV is below 10^3 cm/s. It means that optical absorption becomes a limiting factor in silicon solar cells. Then the product of $V_{OC} \times J_{SC}$, which contributes to maximum power and efficiency depends on

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[4]IQE – the fraction of absorbed photons contributing to the output current.

optical absorption and Auger recombination, i.e. SRV. The optical absorption of c-Si wafers can be improved with texturing of Si surface. Anisotropic alkaline etching is state of the art in the industrial production of high-efficiency Si solar cells. Alkaline etching creates micro-structures that utilize geometrical light trapping, but it retains surface reflection about 10 % [32]. Therefore, anti-reflective coatings (ARC) are applied on top of micro-textures to reduce reflectance to few percent [33]. However, due to the half wavelength condition for destructive interfering waves, ARC is efficient only for the narrow range of Si absorption spectra. A solution is to use a stack of multiple film coatings with different refractive indexes. However, such stacking films are quite costly. In addition, geometrical structures with ARC coatings require multi-step processing including photolithography and various films deposition techniques [34]. However, there is a more simple one-step processing solution to overcome optical losses of alkaline texturing. Dry reactive ion etching of Si satisfies the demand and offers anti-reflective properties and light trapping properties for Si surfaces, creating optically black nanostructures, the so-called black Si [35]. In this work, black Si was tested as an alternative to standard texturing technology for Si solar cell fabrication with objectives to achieve optical reflectance below 1% and low surface recombination velocity.

1.4 State of the art in Si solar cell technology

1.4.1 Conventional p-n doped homojunction technology

Homojunction Si solar cell technology has been dominant for several decades since 1954 and the first efficiency of 6 % and allowing to achieve 25 % efficiency in 2000 in University of New South Wales (UNSW) after many trials and research with their well-known Passivated Emitter Rear Locally Diffused (PERL) and later PERC (Passivated Emitter Rear diffused Contact) architectures solar cells [31] structure as shown in Fig. 1.14 (a). The PERL cell with 25 % record was significant achievement in silicon photovoltaics. The PERL cell had several key technology features:

- n-p homojunction was formed at a high-temperature (900-1000°C) diffusion of phosphorus atoms into p-type Si at the top of the PERL cell (Fig. 1.11 (b), (d)).

- Local anode contacts at the rear of the cell were formed with optical lithography.

- With a high-temperature diffusion of boron atoms to the back of Si, a p^+-p back surface field (BSF) junction was formed.

- Phosphorus diffusion is utilized to form a n^+p junction and front surface field (FSF).

- Enhanced light trapping was achieved with optical lithography and anisotropic etching techniques to form inverted pyramids on the surface of the solar cell.

- Selective emitter approach was realized with a formation of openings for contacts in a high quality, thermally grown silicon dioxide for that worked as excellent surface passivation.

1.4.2 Amorphous silicon heterojunction technology

However, due to these complicated technological steps, such as diffusion, oxide passivation, photolithography and high processing temperature (up to 1000 ^{o}C), most current Si solar cell utilizes heterojunction Si technology (Fig. 1.11 (f, h), Fig. 1.14 (b, d)). First successful

heterojunction Si solar cell achieved 20 % power conversion efficiency and was fabricated by Sanyo based on Heterojunction with Intrinsic Thin (HIT) layer technology in 2000 as shown in Fig. 1.14 (b) [36] and then 23 % efficiency to 24.7 % in 2014 with the application of hydrogenated amorphous Si (a-Si:H) as passivating and heterojunction formation material. That was the point of no return. Since 2000 many private companies and research institutions start to focus on heterojunction Si solar cell technology. It was and is highly promising technology allowing to cut production cost dramatically and allow to compete for solar cells with fossil fuel.
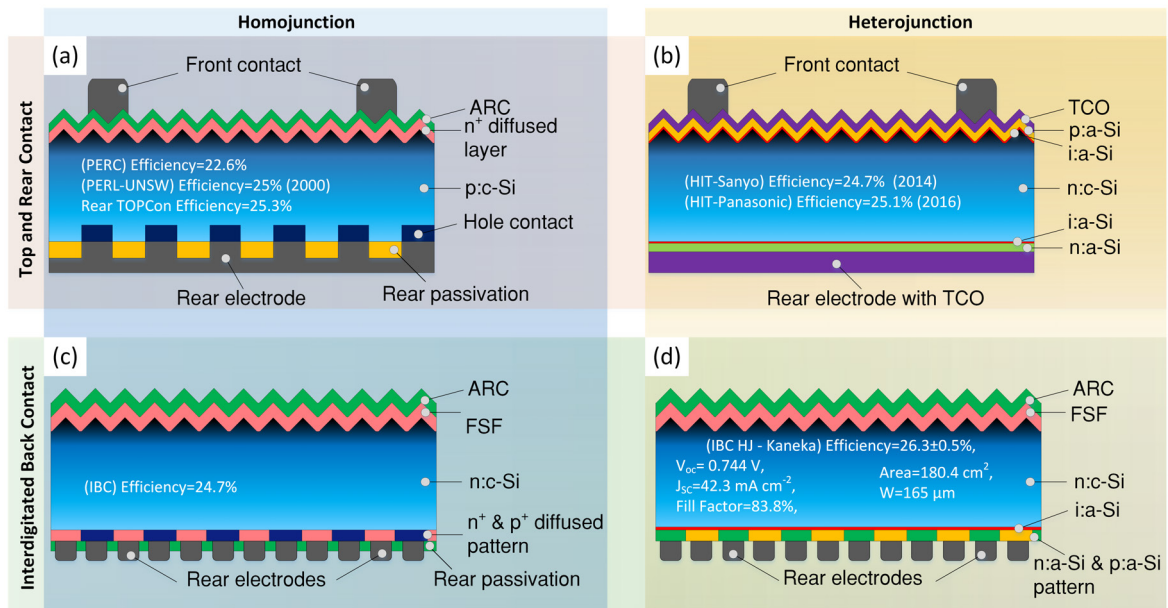
FIGURE 1.14: Schematic images of typical c-Si solar cells and records efficiency. The image was adopted and modified according to Yoshikawa et al. publication in Nature Energy [11]

Next HIT cell record was presented by Panasonic with 25.6 % efficiency in the same 2014 [37] and kept this record for over 2 years. The reason why Panasonic appeared on solar cell scene is simple – Sanyo technology was overtaken by Panasonic after its patent expired in 2010. Since that time new solar cell research race was started. Moreover, heterojunction c-Si solar cell technology keeps surprising us further. The Japanese company Kaneka, in the middle of 2016, reported that they established a new record of 26.3 % using large-area (180 cm^2 cell) c-Si solar cell with interdigitated back contact (IBC) structures and a-Si/c-Si carrier selective contacts. The Fraunhofer ISE certified the record efficiency of this 180 cm^2 large record cell, and finally, it upheld a breaking record that over-performed the previous record by 0.7 % and in March 2017 it was published in Nature Energy [11].

Kaneka predicts that with their current IBC technology record they can decrease the levelized cost to 0.13 \$/kWh before 2020 and to 0.06 \$/kWh [11]. This record proves that heterojunction becomes dominating technology and grant us a possibility to use affordable renewable solar energy. It can be explained with a recent device sketch comparing homojunction, and heterojunction solar cell structure reported by Kaneka in Nature Energy and presented here in Fig. 1.14 (a-d).

Heterojunction cell technology is successful due to many factors and offers not only high efficiencies; it also provides much-simplified production process sequence consisting of six process steps compared to 9 steps in standard homojunction Si cell technology. Heterojunction processing technology has as a core plasma enhanced chemical vapor deposition
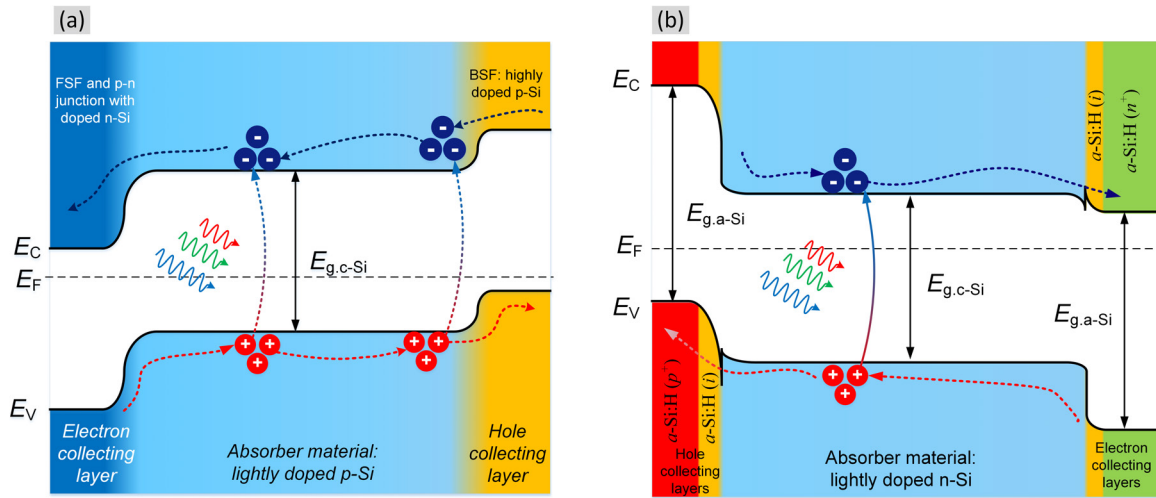
FIGURE 1.15: Charge separation schemes in (a) homojunction Si solar cells energy band diagram based on PERC technology from UNSW and (b) hetero-junction a-Si:H/Si solar cell energy band diagram based on HIT technology from Panasonic and Kaneka

(PECVD) technique that allows depositing a-Si layers and physical vapor deposition (PVD) technique for deposition of the transparent conductive oxide layer (TCO). Heterojunction Si solar cell records technology from Sanyo, then Panasonic and finally Kaneka companies became possible to achieve via implementation of carrier selective contacts (CSCs) [38–40] based on a-Si:H/c-Si type of charge carriers (electrons or holes) from the absorber (e.g., silicon). Such carrier separation scheme is slightly different from conventional diffused p-n homojunction since the motion of electrons and holes corresponds to the same physical laws as shown in Fig. 1.15. However, these schemes are different in processing technologies, and according to the records reported above, heterojunction technology seems like allows to achieve high power conversion efficiency for a lower price.

Currently, the most widely used CSC in Si photovoltaic technology amorphous hydrogenated Si (a-Si:H) deposited by PECVD technique at around 200 °C over thin passivation interlayers (intrinsic a-Si:H, or SiO_2) [41–43]. High-quality CSCs are conductive films (for the selected carrier) with excellent surface passivation properties. The incorporation of CSCs into Si solar cells provides excellent surface passivation, simplified design, and process robustness [44]. Although a-Si:H and SiO_2 -based CSCs have shown remarkable performance, these technologies have some fundamental challenges related to thermal stability and parasitic photon absorption in a-Si:H films, a complicated deposition process, and quite high production costs. Therefore, there is an interest in developing high-quality CSCs that can be easily deposited, at low cost and with minimal use of hazardous materials [44].

1.4.3 Transition metal oxide–silicon heterojunction technology

One of the most promising material groups for CSC is transition metal oxides (TMOs). TMOs were first used in organic and perovskite solar cells [46]. These CSCs have shown potential as alternative CSCs in silicon photovoltaics [47] due to the low cost of processing steps involved (atomic layer deposition, thermal evaporation, sputtering, spin-coating, or
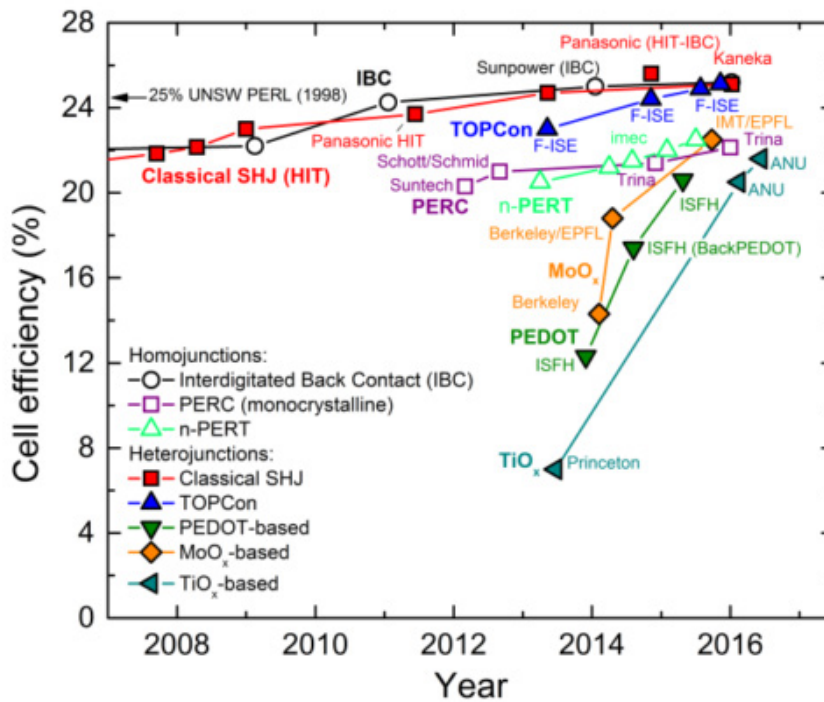
FIGURE 1.16: Summarizing chart of the record efficiencies for selected c-Si photovoltaic technologies including new concepts based on transition metal oxide passivating carrier selective contacts [45]

spray methods). As a hole-selective CSC's molybdenum oxide (MoO_x) [48–55], nickel oxide (NiO_x) [56–60], vanadium oxide (VO_x) and tungsten oxides (WO_x) [47] have been investigated as replacements for a-Si:H p-type layer in silicon solar cells with a record efficiency of 22.5 % [48] and show further positive progress as seen from Fig. 1.16. For the n-type electron selective CSC, TiO_2 is the most promising materials in SHJ solar cells [50–61]. TiO_2 has a 3.2 eV band gap energy. TiO_2 as a hole-blocking layer in silicon solar cells is intensively investigated. A single heterojunction silicon solar cell with a TiO_2 backside hole blocking layer achieved an efficiency of 21.6 % [61]. All the above success records with TMO CSCs are summarized in a chart below in Fig. 1.16. According to this chart TMO CSCs already successfully compete with homojunction and amorphous silicon heterojunction technologies. In about 3 years, solar cells based on TMO CSCs advances in development with record efficiencies from 7 % to 21 % for TiO_2 and MoOx base devices. Also, atomic layer deposition (ALD) coated metal oxide films guarantee excellent passivation properties on surfaces with complex morphology. In few words, it becomes possible to fabricate solar cells using ALD or other low process temperature techniques and decrease levelized cost [62, 63]. In combination with advanced light trapping techniques such as reactive ion etching for black silicon nanostructures, heterojunction Si solar cells with CSC can be a strong competitor to a-Si:H heterojunction technology. The main advantages are mostly based on a deposit of these materials with ALD technique that also leads to low toxicity and a low deposition temperature of the process and in principle possibility to deposit all functional thin films in one ALD machine. Such benefits can simplify the process flow, reduce production cost within production line and thermal budget.

1.5 Thesis outline and objectives

The objectives of this work are to investigate the use of low-temperature heterojunction formed with metal oxide (TiO$_2$ and NiO) thin films as passivating carrier selective contacts on nanostructured Si surfaces. Such approach has a potential to replace diffused junction technology and might be a cheaper alternative to amorphous Si heterojunction technology. Metal oxide based carrier selective contacts in Si solar cell works based on a physical principle similar to HIT technology solar cells with doped p- and n-type doped a-Si:H. However, due to lack of technological solutions to deposit high-quality metal oxide films, this technology had a slow development phase until the 2000's. ALD technology allowed to speed up research with metal oxide thin films and its applications in photovoltaics.

Therefore, in this project, the main goal was to investigate metal oxide carrier selective, passivating, tunneling and conductive films in fabrication of c-Si solar cells with nanostructured absorber surfaces. Particular focus was dedicated to TiO$_2$ and NiO transition metal oxides as carrier selective passivating contacts on nanotextured black silicon (bSi) surface with a metal grid and transparent conductive oxides such as AZO. AZO process was skipped in this thesis due to incomplete process development and preliminary raw results. Main passivation layer is Al$_2$O$_3$. The schematic image of proposed c-Si solar with carrier selective passivating contacts is illustrated in Fig. 1.17. All the functional layers (TiO$_2$, NiO, Al$_2$O$_3$) were deposited mainly with ALD technique or with RF sputtering (NiO) as ultra-thin 5-30 nm thick films. Before any solar cell fabrication, process optimization was conducted to achieve best diode and passivation properties of functional layers and low surface recombination velocity on nanostructured Si surfaces. After final optimization, two batches of solar cells with TiO$_2$, NiO, Al$_2$O$_3$ layers were fabricated, characterized. The corresponding results of the solar cell tests were presented in this thesis.

In **Chapter 2** theoretical foundations of light trapping, surface texturing and passivation, charge separation with heterojunctions are presented. Further, selected solar cells operation theory and their important characterization parameters are discussed.

In **Chapter 3** the experimental and simulation results of passivation and diode properties of TiO$_2$-Si hole blocking heterojunction are discussed. The experiments data is presented for thermal ALD TiO$_2$ films growth at different temperatures (80-300 $^\circ C$) and investigation of surface morphology, film thickness (5-20 nm), different tunneling interlayers (SiO$_2$, Al$_2$O$_3$) and annealing conditions on TiO$_2$-Si(p) test structures and devices.

Chapter 4 discusses optical and light trapping properties of black silicon nanostructures fabricated with one-step maskless reactive ion etching. Also, best passivation schemes with ALD Al$_2$O$_3$ on planar and corrugated surfaces are presented.

Chapter 5 presents the outlook for nanostructured Si solar cells with TMO passivating carrier selective contacts and their potential in for future industrial applications. It also summarizes all the presented results and observation and provides some directions for future work, experimental concept tests in progress, particularly, NiO-Si heterojunction with electron blocking properties, transparent conductive layers such as Aluminum Zinc Oxide and concept of Si solar cell with TiO$_2$ and NiO carrier selective contacts and advanced light trapping texturing.
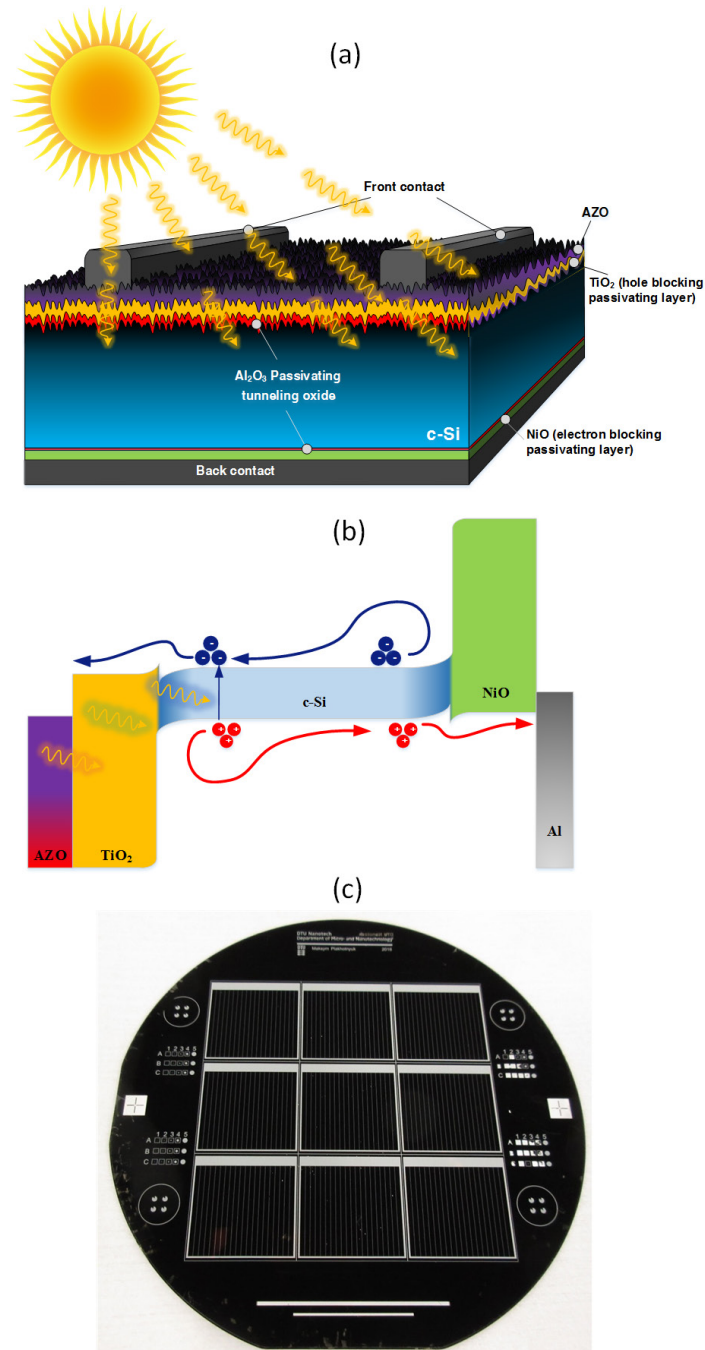
FIGURE 1.17: Schematic image of fabricated nanostructured black c-Si solar with TiO_2, NiO carrier selective passivating contacts, transparent conductive oxide (AZO) contact and passivating Al_2O_3 layers: (a) 3D illustration of the solar cell, (b) energy band diagram, (c) photoimage of the fabricated solar cell

Chapter 2

Theory

"One day I will find the right words, and they will be simple."

Jack Kerouac, The Dharma Bums

In this chapter, a brief introduction of all theoretical concept applied in this thesis are presented. First, a carrier transport (Sect. 2.1) based on Boltzmann Transport Equation, drift and diffusion theory, Continuous and Poisson's equations are discussed. In the 2.2 section, a light absorption concept and its effect on carrier generation in semiconductors are introduced. In the 2.3 section, different recombination mechanisms and their effect on the current in the solar cell are discussed. In the 2.4 section, light trapping mechanisms and structures in solar cells are described. In the 2.5 section, solar cell operating principles and equivalent circuits are derived and explained. At last, the 2.6 section focuses on the heterojunction theory of carrier selective contacts.

2.1 Carrier transport

2.1.1 Boltzmann transport equation

Boltzmann transport equation is a fundamental physics for the analysis of carrier transport in semiconductors and solids in general. The equation represented the probability distribution of a free particle in a wave vector and physical space as a function of time and given below as a 3-dimensional (3D) standard semi-classical transport equation:

$$\frac{\partial f}{\partial t} + v\nabla_r f + \frac{q\vec{E}}{\hbar}\nabla_k f = \sum \left[S\left(k',k\right) f\left(r,k',t\right)\left[1 - f\left(r,k,t\right)\right] - S\left(k,k'\right) f\left(r,k,t\right)\left[1 - f\left(r,k',t\right)\right]\right]$$

(2.1)

where r is the position, $\mathbf{k}$ is the momentum, $f\left(k,t\right)$ is the distribution function (in the case semiconductors – a Fermi-Dirac distribution function in equilibrium), $\mathbf{v}$ is the group velocity, $\mathbf{E}$ is the electric field, q is absolute value of the electric charge, $S\left(k',k\right)$ is the transition probability between the momentum states k and k', and $\left[1 - f\left(k',t\right)\right]$ is the probability of non-occupation for a momentum state k'. The summation on the right-hand side is the collision term, which accounts for all the scattering events. The terms on the left-hand side indicate, respectively, the dependence of the distribution function of time, space (explicitly related to velocity), and momentum (specifically related to the electric field).

The Boltzmann equation is valid under assumptions of semi-classical transport: effective mass approximation; Born approximation for the collisions, in the limit of small perturbation for the electron-phonon interaction and instantaneous collisions; no memory effects, i.e., no dependence on initial condition terms. The phonons are usually treated as in equilibrium, although the condition of non-equilibrium phonons may be included through an additional equation [64, 65]. Analytic solutions of the Boltzmann equation are possible only under very restrictive assumptions. The vast majority of device simulations are normally based on the numerical solution of approximate models which are related to the Boltzmann equation, coupled with Poisson's equation for self-consistency. The collision term on the right-hand side of Eq. (2.1) is substituted with a phenomenological term $\frac{f_{eq} - f(r,k,t)}{\tau}$, where f_{eq} is the local equilibrium distribution function, τ is a relaxation time. For simplicity of electric current calculations, the distribution function is expressed regarding velocity, rather than momentum. In equilibrium state, the Maxwell-Boltzmann distribution function is used and therefore the overall equilibrium distribution function that is represented as

$$f_{\text{eq}}(r, v) = n(r) \left(\frac{2\pi k_{\text{B}} T_0}{m^*} \right)^{-3/2} \exp\left(-\frac{m^* |v|^2}{2k_{\text{B}} T_0} \right) \tag{2.2}$$

where $n(r)$ is the carrier density, T_0 is the lattice temperature, m^* is the effective mass and k_B is the Boltzmann constant. Equation (2.2) is valid only in an equilibrium state in the non-degenerate material. The carrier density $n(r)$ is directly related to the distribution function and represented general expression below:

$$n(r) = \int dv \, f(r, v) \tag{2.3}$$

The relaxation time plays a significant role charge transport and helps to evaluate charge transport in the semiconductor material. If the electric field is switched off instantaneously, space independent distribution function could be considered. Therefore, the resulting Boltzmann equation is then rewritten as:

$$\frac{\partial f}{\partial t} = \frac{f_{\text{eq}} - f}{\tau} \tag{2.4}$$

This equation shows the relaxation time as a characteristic decay constant required for the system to return to the equilibrium state.

2.1.2 Drift and diffusion

Electron and hole motion in semiconductors and particularly in Si leads to an electric current flow. The electric charge carriers transport can be caused by an electric field, due to external bias. This carrier transport is a carrier drift. Under external bias (electric field) the force acts on charge carriers in a semiconductor accelerating positive charges, i.e., holes, in the direction of the electric field and negative charges, i.e., electrons, in the opposite direction to the electric field as shown in Fig. 2.1 (a). Meanwhile, carrier motion from regions with higher carrier density to the area with lower carrier density in a random order is known as carrier diffusion as shown in Fig. 2.1 (b). The driving force of diffusion is a gradient of charge concentration. In both cases, carrier concentration is defined by the quasi-Fermi levels for electron E_{F_n} and holes E_{F_p} as depicted in Fig. 2.1. Quasi-Fermi levels represent

a separate population of electrons and holes displaced from equilibrium in conduction and valence bands, respectively. For drift transport quasi-Fermi levels perturbed by applied electric field, while for diffusion transport quasi-Fermi levels have a gradient across the bulk the semiconductor due to doping gradient. If both transport mechanisms are combined, the total carrier transport in the semiconductor can be described by the sum of drift-diffusion currents, which could be easily derived from the Boltzmann equation.
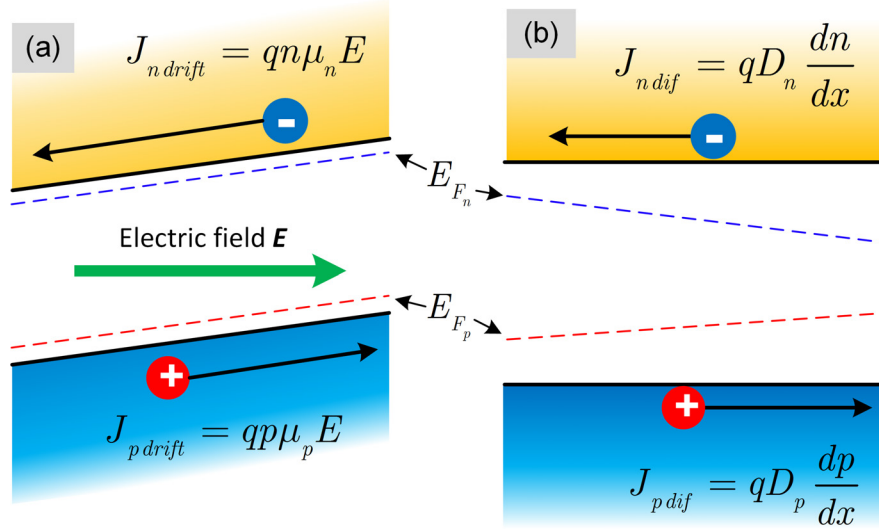
FIGURE 2.1: Visualization of (a) drift transport and (b) diffusion transport in a semiconductor with corresponding current components with electron and hole

In a steady-state and 1-D geometry with consideration of relaxation time approximation (see Eq. (2.4)) the Boltzmann equation becomes

$$v\frac{\partial f}{\partial x} + \frac{q\vec{E}}{m^*}\frac{\partial f}{\partial v} = \frac{f_{\text{eq}} - f(v,x)}{\tau} \tag{2.5}$$

Since a parabolic energy bandis considered, then the relaxation could be represented as $m^*v = \hbar k$. Meanwhile, the current density in general definition is given by

$$J(x) = q \int vf(v,x)\,dv \tag{2.6}$$

where the right-hand integral represents the first moment of the distribution function. The current density can be related to 1D Boltzmann equation (2.5) after multiplication both sides by v and integrate over v. Taking into consideration that the equilibrium distribution function is symmetrical in v and its integral is equal to zero, one obtains the current density equation:

$$J(x) = -q\frac{q\tau}{m^*}E \int v\frac{\partial f}{\partial v}\,dv - q\tau\frac{d}{dx} \int v^2 f(v,x)\,dv \tag{2.7}$$

After integration by parts one obtains

$$\int v\frac{\partial f}{\partial v}\,dv = \underbrace{[vf(v,x)]_{-\infty}^{\infty}}_{0} - \int f(v,x)\,dv = -n(x) \tag{2.8}$$

moreover, one can write

$$\int v^2 f(v,x)\, dx = n(x)\langle v^2 \rangle \tag{2.9}$$

where $\langle v^2 \rangle$ is the average of the square of carrier velocity defined as

$$\langle v^2 \rangle = \frac{1}{n} \int v^2 f(v,x)\, dx \tag{2.10}$$

For 1D geometry case, the exponent $-\frac{3}{2}$ in Eq. (2.3) may be replaced with $-\frac{1}{2}$ and the thermal kinetic energy component becomes $\frac{k_B T}{2}$ instead of $\frac{3k_B T}{2}$.

The drift-diffusion equation then is derived with substitution the mobility as $\mu = \frac{q\tau}{m^*}$ and replacing $\langle v^2 \rangle$ with its average equilibrium value $\frac{k_B T}{m^*}$ and neglecting thermal effects. The relation between carrier mobility and diffusivity is called Einstein relation and only valid for non-degenerate carrier concentration:

$$D_{n,p} = \mu_{n,p} kT/q \tag{2.11}$$

Therefore, the total current density is the sum of the drift and diffusion current densities:

$$J_n = \underbrace{q\mu_n n(x) E(x)}_{drift} + \underbrace{qD_n \frac{dn}{dx}}_{diffusion} \tag{2.12}$$

$$J_p = \underbrace{q\mu_p p(x) E(x)}_{drift} - \underbrace{qD_p \frac{dp}{dx}}_{diffusion} \tag{2.13}$$

where μ_n and μ_p are carrier electron and hole mobilities D_n and D_p are electron and hole diffusivities, p and n are the carrier charge densities on each side of the junction. Electron and hole concentrations are computed using Boltzmann approximation:

$$n = n_i \exp\left[\frac{q(E - E_{F_n})}{k_B T}\right] \tag{2.14}$$

$$p = n_i \exp\left[\frac{-q(E - E_{F_p})}{k_B T}\right] \tag{2.15}$$

where E_{F_n} E_{F_p} are the Quasi-Fermi levels and n_i is the intrinsic charge carrier density which in Boltzmann approximation follows in the next equation:

$$n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{2.16}$$

where N_C, N_V are the effective density if states of conduction and valence bands respectively. These Eqs. (2.12)-(2.13) are the foundation for analysis of Si solar cells in most operating conditions. Considering electron and hole currents the total current in semiconductor

devices is the sum of the electron and hole current densities multiplied with the area, A, perpendicular to the current flow:

$$I_\Sigma = A\left(J_\mathrm{n} + J_\mathrm{p}\right) \qquad (2.17)$$

Important to note that represented equations for drift-diffusion current densities in Eqs. (2.12) and (2.13) lack assumptions on the non-equilibrium distribution function $f\left(v, x\right)$. The choice of equilibrium (thermal) velocity means that the drift-diffusion equations are only valid for minuscule perturbations of the equilibrium states or at low field conditions. The drift-diffusion equations can be "upgraded" if field-dependent mobility $\mu\left(E\right)$ and diffusivity $D\left(E\right)$ are introduced.

2.1.3 Continuity and Poisson equation

The Continuity equation is one of the most important fundamental laws of semiconductor device physics. It states that charge is conserved quantities and the total amount of charges in volume V only can be changed via charge flow through the boundary surface S of the volume V. This law in more general form was discovered by J.L. Lagrange in 1762, later and independently by several mathematicians in France by C.F. Gauss in 1813, in Great Britain by G. Green in 1825 and then independently by Ukrainian mathematician M.V. Ostrogradsky in 1831. Know as the conservation law; it is applied in fluid mechanics, quantum mechanics, other fields of physics and in electrodynamics. For electric charge flow the conservation law is known as a Continuity equation in a differential formulation and represented as follows:

$$\nabla J + \frac{\partial \rho}{\partial t} = 0 \qquad (2.18)$$

or as

$$\left(\frac{\partial J_\mathrm{x}}{\partial x} + \frac{\partial J_\mathrm{y}}{\partial y} + \frac{\partial J_\mathrm{z}}{\partial z}\right) + \frac{\partial \rho}{\partial t} = 0 \qquad (2.19)$$

where J_x, J_y, J_y – components of current density vector **J,** ρ is a charge density. In a semiconductor solar cell, the Continuity equation accounts sunlight absorption regarding electron-hole pair generation and recombination and charge contribution to the electric current collected at the electrodes. This equation is transformed into the following equations for electron and hole components:

$$\begin{aligned} \frac{\partial n}{\partial t} &= G_\mathrm{n} - U_\mathrm{n} + \frac{1}{q}\nabla J_\mathrm{n} \\ \frac{\partial p}{\partial t} &= G_\mathrm{p} - U_\mathrm{p} + \frac{1}{q}\nabla J_\mathrm{p} \end{aligned} \qquad (2.20)$$

where G is the generation and U is recombination rates.

To find dependency between charge density and electric field the Poisson equation as a special case of Maxwell equation with no magnetic field contribution should be used:

$$\begin{aligned} \nabla E &= \frac{1}{\varepsilon}\rho \\ &\text{or} \\ \frac{\partial E_\mathrm{x}}{\partial x} + \frac{\partial E_\mathrm{y}}{\partial y} + \frac{\partial E_\mathrm{z}}{\partial z} &= \frac{\rho}{\varepsilon \varepsilon_0} \end{aligned} \qquad (2.21)$$

where $E = (E_x, E_y, E_z)$ is electric field vector with its Cartesian components.

Finally, the Continuity (2.20) and Poisson equations (2.21) contribute to the Boltzmann transport equation (2.5) regarding current density Eqs. (2.12) and (2.13). There three sets of equations are the fundamentals of semiconductor device physics and particularly Si solar cells.

2.2   Generation

As mentioned above generation of electron-hole pairs contribute to the charge conservation, and mathematically is shown in the Continuity equation (2.20). Depending on the type of semiconductor energy bandgap, light absorption in the semiconductor can be absorbed either directly or indirectly.

In direct semiconductors, crystal momentum for valence and conduction bands have the same value allowing the electron to be excited from valence band to conduction band, leaving a hole in a valence band (Fig. 2.2 (a)). Both energy and momentum are conserved in a direct transition.

In the case of an indirect-band-gap semiconductor, like Si, minimum of conduction band energy and the maximum of valence band energy have a different value of crystal moment (Fig. 2.2 (b)). This crystal momentum difference leads to the much higher energy required for direct transition of an electron from valence to conduction band. However, electron transition process at lower excitation energy in if a photon-phonon mechanism is involved. Phonon energy compensates crystal momentum difference for an electron to transit to the conduction band minimum, and phonon represents lattice vibrations. Therefore, the minimum energy required to excite an electron from valence to conduction band is represented as:

$$h\nu = E_g - E_p \tag{2.22}$$

where E_p is a phonon absorption energy.

2.2.1   Light absorption and electron-hole pair generation

When light penetrates into a material, it is absorbed as it propagates through the material. Light absorption depends on the absorption coefficient of the material, in our case Si, which is wavelength and momentum dependent. The attenuation of photon flux density $\Phi(x, \lambda)$ with account of surface reflection that decreases exponentially with the distance x that it travels through semiconductor absorber can be expressed using Lambert-Beer's Law:

$$\Phi(z, \lambda) = (1 - R(E))\Phi_0 \exp(-\alpha(\lambda)z) \tag{2.23}$$

where Φ_0 incident photon flux density and $\alpha(\lambda)$ is the absorption coefficient. The photon flux density is related to the spectral power density $P(\lambda)$ and associated with the solar radiation via

$$\Phi_0(\lambda) = P(\lambda)\frac{\lambda}{hc} \tag{2.24}$$
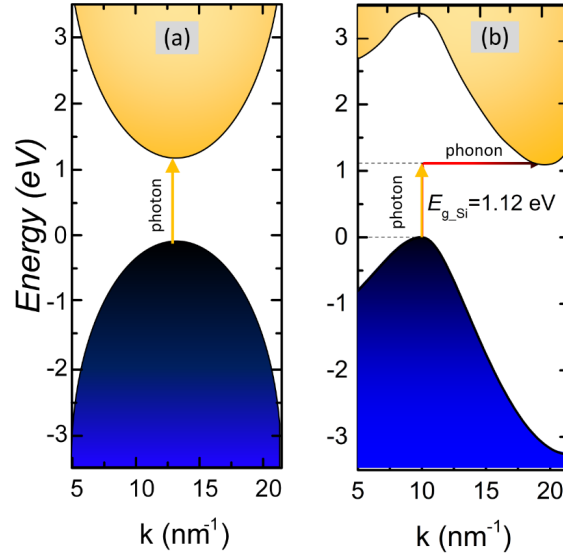
FIGURE 2.2: Excitation mechanism in (a) a direct (like GaAs and (b) indirect (like Si) semiconductors with different energy-crystal moment diagrams showing photon absorption.

Moreover, the theoretical value of absorption coefficient for indirect bandgap semiconductor, like Si, is a sum of two components of absorption coefficient including phonon absorption $\alpha_a(h\nu)$ and involving phonon emission $\alpha_e(h\nu)$ and possible under the condition that $h\nu > E_g + E_p$:

$$\alpha(h\nu) = \underbrace{\alpha_a(h\nu)}_{\swarrow} + \underbrace{\alpha_e(h\nu)}_{\searrow} \qquad (2.25)$$

$$\overbrace{\alpha_a(h\nu) = \frac{A(h\nu - E_g + E_p)^2}{\exp\left(\frac{E_p}{k_B T}\right) - 1}} \qquad \overbrace{\alpha_e(h\nu) = \frac{A(h\nu - E_g - E_p)^2}{1 - \exp\left(-\frac{E_p}{k_B T}\right)}}$$

The experimental absorption coefficient and absorption depth for Si are shown in Fig. 2.3 as a function of the wavelength of incident light. The weak absorption region at a wavelength of 500 nm corresponds to indirect bandgap processes. Below 400 nm region corresponds to high-energy photons that can excite electrons for direct transition from valence to conduction band and therefore lead to high absorption in this wavelength region. The penetration depth of long wavelength photons ($\lambda \geq 800\,\text{nm}$) is vastly significant and drops over a few orders of magnitude. Therefore, the optical path length or absorption depth weakly absorbed photons has to be increased enough to maximize absorption. Absorption depth as a function of photon wavelength is shown in Fig. 2.3 in red. As could be concluded, to achieve higher absorption probability the thick Si wafers should be used.

The spectral generation rate $g_{sp}(z, \lambda)$ is the number of electron-hole pairs generated at the depth z in the semiconductor material per time in a volume per unit wavelength including surface reflection:

$$g_{sp}(z, \lambda) = (1 - R(E))\, \eta_g \Phi_0(\lambda)\, \alpha(\lambda) \exp(-\alpha(\lambda) z) \qquad (2.26)$$

where η_g is the generation quantum efficiency, usually equal to unity and it brings the assumption that one photon generates only one electron-hole pair. However, for high-energy
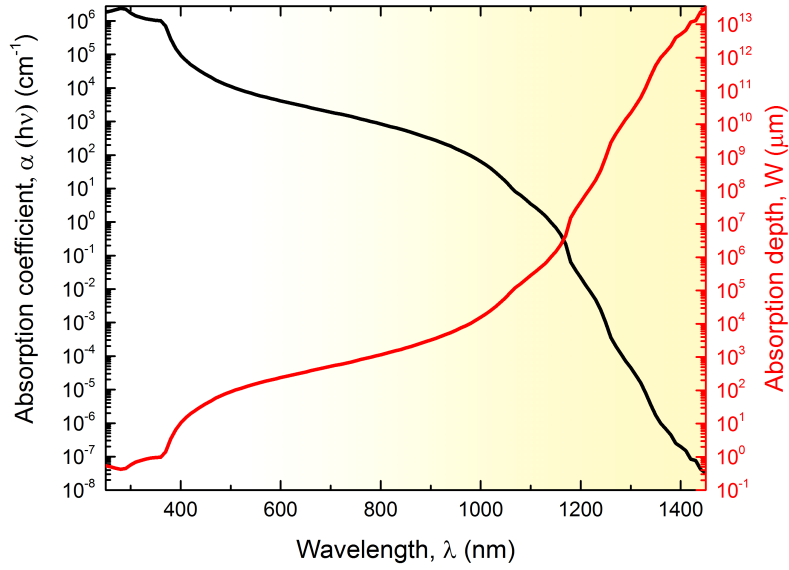
FIGURE 2.3: Absorption coefficient and absorption depth of Si as a function of wavelength of incident light (experimental data taken from PVeducation portal [66] and [67])

photons, a generation quantum efficiency can exceed unity and reach maximum value 1.3 for Si. Then the optical generation rate $G_{\mathrm{L}}(z)$ is calculated as integral of spectral generation rate over wavelength spectrum:

$$G_{\mathrm{L}}(z) = \int_{\lambda_1}^{\lambda_2} g_{\mathrm{sp}}(z, \lambda)\, d\lambda = (1 - R(E))\, \eta_{\mathrm{g}} \int_{\lambda_1}^{\lambda_2} \underbrace{\Phi_0(\lambda)\, \alpha(\lambda) \exp(-\alpha(\lambda)\, z)}_{A(z)}\, d\lambda \qquad (2.27)$$

where $A(z)$ is an absorption depth in a semiconductor. Finally, the generated excess charges concentration per time are equal for electrons and holes and can be written as follows:

$$\left.\frac{\partial n}{\partial t}\right|_{\mathrm{light}} = \left.\frac{\partial p}{\partial t}\right|_{\mathrm{light}} = G_L \qquad (2.28)$$

2.3 Recombination

In the thermal equilibrium, the product of the electron and hole concentration is constant and known as intrinsic carrier concentration:

$$n_{\mathrm{i}}^2 = n_0 p_0 \qquad (2.29)$$

Thermal equilibrium conditions suppose to have the temperature above 0 K at which the crystal lattice is vibrating, leading to thermal generation and simultaneous recombination $G = U$. Recombination is the relaxation or decay process of electrons from conduction to

valence band and occurs only when a convenient hole is available in the valence band. According to the conservation law, the relaxation energy of the electron is then either released by spontaneous emission of a photon, known as radiative recombination, and mostly dominating for direct bandgap semiconductors, or indirect energy transfer, know as nonradiative recombination dominating in indirect bandgap semiconductors like Si. Since Si is an indirect semiconductor, almost all recombination processes involve momentum conservation regarding phonon and require some additional time. The average duration between charge carrier generation and recombination is called carrier lifetime τ. Lifetime is an essential theoretical and experimental parameter that qualitatively represents recombination channels given by extrinsic factors.

As written in the Eq. (2.27) light excitation leads to the generation of excess charge densities of electrons and holes

$$\begin{aligned} \Delta n &= n - n_0 \\ \Delta p &= p - p_0 \end{aligned} \tag{2.30}$$

That will decay over time. Under charge neutrality, assumption and absence of trap state, i.e., $\Delta n = \Delta p$, only one type of charge carrier is considered and known as minority charge carriers. The net recombination rate of excess minority charge carriers in a general form is defined as

$$\begin{aligned} U\left(\Delta n\left(t\right), n_0, p_0\right) &= -\frac{\partial \Delta n(t)}{\partial t} \\ U\left(\Delta p\left(t\right), n_0, p_0\right) &= -\frac{\partial \Delta p(t)}{\partial t} \end{aligned} \tag{2.31}$$

in the case of a spatially homogeneous generation. In thermal equilibrium, the total generation and recombination compensate each other and thus $U_{(\Delta n, \Delta p=0)} = 0$. Δn and Δp decay over time if the net recombination rate is only proportional to the excess carrier densities. Then the minority charge carrier recombination lifetime (shortly, lifetime) can be defined as the following ratio:

$$\begin{aligned} \tau\left(\Delta n, n_0, p_0\right) &= \frac{\Delta n}{U(\Delta n, n_0, p_0)} \\ \tau\left(\Delta p, n_0, p_0\right) &= \frac{\Delta p}{U(\Delta p, n_0, p_0)} \end{aligned} \tag{2.32}$$

In the case of $U \sim \Delta n$ the resulting lifetime is constant over excess carrier density or injection level Δn. In general case, lifetime τ depends on the injection level Δn. Lifetime τ also depends on the intrinsic carrier density related to the doping level.

Total recombination in the semiconductor consist of different recombination mechanisms that occur simultaneously, however, the effective minority carrier lifetime is determined by the loosest recombination channel. The effective lifetime is limited by the shortest lifetime in the process. In summary, the effective lifetime is defined by the sum of all recombination process:

$$\frac{1}{\tau_{\text{eff}}} = \sum_{i=1}^{m} \frac{1}{\tau_{\text{i}}} \tag{2.33}$$

2.3.1   Recombination mechanisms

Recombination is the inverse process to generation when the electron-hole pairs decay. Recombination mechanism can be classified as radiative and nonradiative decay, also with the intrinsic and extrinsic mechanism. Intrinsic (band-to-band) recombination occurs via direct band-to-band transition of an electron. Depending on electron-hole pair combination, intrinsic mechanisms can be divided into two categories: radiative band-to-band recombination and Auger band-to-band recombination (Fig. 2.4 (a), (b)).
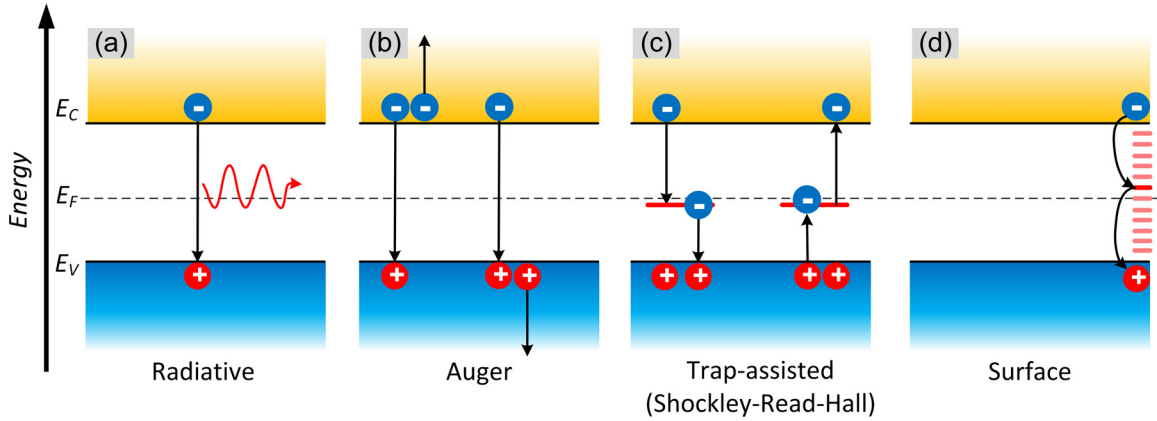
FIGURE 2.4: Recombination mechanisms in semiconductors. The direct radiative and Auger band-to-band decays are intrinsic processes, whereas the Shockley-Read-Hall (SRH) and surface recombination are extrinsic processes assisted by a defect level in the bandgap. The black arrows indicate the direction of the electron (blue circuit with minus sign) transitions. The holes (red circle with plus sign) travel against the arrow direction. (a) depicts the schematic of spontaneous radiative recombination, (b) depicts the (*eeh*) and (*ehh*) Auger recombination processes, (c) shows the four basic transitions that may occur during SRH recombination, (d) represents surface recombination through one of gap state within defect density D_{it}

Extrinsic (band-to-bound, trap-assisted, surface) recombination occurs via defects within energy bandgap. Defect recombination type is known as the SRH recombination. All the recombination mechanisms are depicted in Fig. 2.4.

2.3.2   Radiative recombination

Radiative recombination involves spontaneous recombination of an electron-hole pair, resulting in an emission of a photon with energy approximately equal to bandgap ($E_{\mathrm{ph}} \approx E_{\mathrm{g}}$) (Fig. 2.4 (a)). The net radiative recombination rate is given by

$$U_{\mathrm{rad}} = B_{\mathrm{rad}} \left(np - n_i^2 \right) \tag{2.34}$$

Here B_{rad} is radiative recombination coefficient or quantum mechanical transition probability[1] and depends directly on absorption coefficient. As a result, it is dominating for direct bandgap semiconductors and can be defined as

---

[1]The indirect transition in Si requires a high momentum transfer. Thus, at a recombination transition probability $B = 4.73 \times 10^{-15} cm^{-3} s^{-1}$ is very small.

$$B_{\text{rad}} = \frac{1}{n_{\text{i}}^2} \frac{2\pi}{h^3 c^2} \int_0^\infty n_s^2 \alpha\left(E\right) \exp\left(-\frac{E}{k_{\text{B}}T}\right) E^2 dE \tag{2.35}$$

where n_{s} is the refractive index of the semiconductor. Considering charge neutrality $\Delta n = \Delta p$ and non-equilibrium concentrations of $n = n_0 + \Delta n$ and $p = p_0 + \Delta p$, radiative recombination lifetime can be written as

$$\tau_{\text{rad}} = \frac{1}{B_{\text{rad}}\left(n_0 + p_0 + \Delta n\right)} \tag{2.36}$$

2.3.3   Auger recombination

For high charge carrier concentrations, three charge processes dominate the recombination rate. In such case, energy and momentum conservation are preserved by the generation of a second electron or hole, which can carry the excess amounts of energy in the recombination process. These intrinsic processes are illustrated in Fig. 2.4 (a). The second electron or hole relax back to original energy state by emitting phonons. Auger recombination is the reverse process to impact ionization or collision effect, when a high-energy electron collides with an atom, breaking a bond and creating an electron-hole pair. The Auger recombination rate increases with increasing carrier concentration and therefore it is a dominating recombination process in highly doped or high injection Si:

$$U_{\text{Auger}} = C_{\text{n}}\left(n^2 p - n_0^2 p_0\right) + C_{\text{p}}\left(np^2 - n_0 p_0^2\right) \tag{2.37}$$

where the Auger coefficients for *eeh* and *ehh* process[2]. Then, Auger lifetime can be expressed under low injection level and high injection level condition as follows:

$$
\begin{array}{c|c|c}
 & \underline{\text{Low injection}} & \underline{\text{High injection}} \\
\text{n} - \text{type} & \tau_{\text{Auger.LLI}} = \frac{1}{C_{\text{n}} N_{\text{D}}^2} & \tau_{\text{Auger.HLI}} = \frac{1}{(C_{\text{n}} + C_{\text{p}})\Delta n^2} \\
\text{p} - \text{type} & \tau_{\text{Auger.LLI}} = \frac{1}{C_{\text{p}} N_{\text{A}}^2} &
\end{array}
\tag{2.38}
$$

Thus, Auger recombination is stronger than radiative recombination in doped c-Si or both low and high injection. As a result, the Auger recombination is the most severe physical limitation to the long charge carrier lifetime in c-Si and therefore to the solar cell efficiency. The Auger recombination process can be additionally enhanced by Coulomb interactions between charges, which leads to even lower Auger lifetime in low-doped Si.

2.3.4   Shockley-Read-Hall recombination

Except for the two intrinsic recombination mechanisms that theoretically represent a physical upper limit to the lifetime. Practically, a more severe limitation in Si solar cell absorber is controlled by impurity related recombination. In 1952 Shockley, Read and Hall [69, 70] formulated the theory of recombination through defects from purely statistical consideration and determined the recombination rate from a single defect level as a function of defects,

---

[2]Auger coefficients were determined by Dziewior and Schmidt [68] on n-type and p-type doped c-Si at 300 K for high doping concentration level have values of $C_{\text{n}} = 2.8 \times 10^{-31} cm^6/s$ and $C_{\text{p}} = 9.9 \times 10^{-32} cm^6/s$, respectively

material, and excitation parameters. In the Shockley-Read-Hall recombination process, illustrated in Fig. 2.4 (c), does not occur as a direct decay process from one band to another. The recombination process is facilitated by impurities or defects in Si. The defect and impurities in Si may arise from impurities incorporated into the Si, from crystallographic defects or apparently certain defects at semiconductor surfaces. The concentration of these defects is usually small compared to the acceptor or donor doping concentration. The original SRH model assumes only one type of defect state in the middle of the bandgap, but in general SRH lifetime τ_{SRH} depends on the trap state energy. The net SRH recombination rate through defects can be written as:

$$U_{\mathrm{SRH}} = \frac{np - n_{\mathrm{i}}^2}{\tau_{\mathrm{n0}}\left(p + p_1\right) + \tau_{p0}\left(n + n_1\right)} \tag{2.39}$$

where τ_{n0} and τ_{p0} are the capture time constants of electrons and holes, which are related to the thermal velocity v_{th}, the defect concentration N_{t} and the capture cross-section of the electron and hole, σ_{n} and σ_{p}, respectively.

$$\tau_{n0,p0} = \frac{1}{\sigma_{\mathrm{n,p}} v_{\mathrm{th}} N_{\mathrm{t}}} \tag{2.40}$$

where thermal velocity for Si $v_{\mathrm{th}} \approx 10^7 \mathrm{cm/s}$.

The full SRH lifetime further depends on the equilibrium and excess carrier concentration and the density if carriers in the traps p_1 and n_1 under charge neutrality and thermal equilibrium conditions

$$\tau_{\mathrm{SRH}} = \frac{\tau_{\mathrm{p0}}\left(n + n_1 + \Delta n\right) + \tau_{\mathrm{n0}}\left(p + p_1 + \Delta p\right)}{p_0 + n_0 + \Delta n} \tag{2.41}$$

The density of carriers in the trap states p_1 and n_1 are defined as

$$n_1 \equiv N_{\mathrm{C}} \exp\left(-\frac{E_{\mathrm{C}} - E_{\mathrm{t}}}{k_{\mathrm{B}} T}\right) \ \text{ and } \ p_1 \equiv N_{\mathrm{V}} \exp\left(-\frac{E_{\mathrm{t}} - E_{\mathrm{V}}}{k_{\mathrm{B}} T}\right) \tag{2.42}$$

2.3.5 Surface recombination

Semiconductor surfaces represent rather severe defects in the crystal structure, and it is a space for many defect states within the forbidden gap, as shown in Fig. 2.4 (d). The surface of an ideal semiconductor has a large crystal disorder that gives rise to a huge number of SRH-like recombination centers or interfaces traps. SRH formalism can describe such recombination mechanism. However, the interface trap density should be defined as the number of defects per unit area. Surface defects states are continuously distributed over the bandgap and presented as interface defect density D_{it} and given per unit area and energy interval. Consequently, the surface recombination rate with extended SRH formalism is given as

$$U_{\mathrm{S}} = \left(n_{\mathrm{s}} p_{\mathrm{s}} - n_i^2\right) \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} \frac{v_{\mathrm{th}} D_{\mathrm{it}}\left(E_{\mathrm{t}}\right)}{\frac{n_{\mathrm{s}} + n_1(E_t)}{\sigma_{\mathrm{p}}(E_t)} + \frac{p_{\mathrm{s}} + p_1(E_t)}{\sigma_{\mathrm{n}}(E_t)}} dE_{\mathrm{t}} \tag{2.43}$$

where n_s and p_s are the electron and hole density at the surface. To evaluate the recombination activity at the surface directly, surface recombination velocity (SRV) is given as

$$S\left(\Delta n, n_0, p_0\right) \equiv \frac{U_S\left(\Delta n, n_0, p_0\right)}{\Delta n} \tag{2.44}$$

The full expression for SRV can be expressed in the particular case of flat band condition after substituting (2.43) into (2.44) would be as

$$S\left(\Delta n, n_0, p_0\right) \equiv \int_{E_V}^{E_C} \frac{\left(\Delta n_s + n_0 + p_0\right) v_{th} D_{it} dE}{\frac{n_0+n_1+\Delta n_s}{\sigma_p} + \frac{p_0+p_1+\Delta n_s}{\sigma_n}} \tag{2.45}$$

The integral in Eq. (2.45) may only be solved numerically, however, in most cases, an upper limit of S could be estimated for the cases of low and high injection. Additionally, surface defect density D_{it} is assumed homogeneous over the bandgap. Then, the remaining integral $\int_{E_g} D_{it} dE$ can be replaced by an equivalent effective density of interface defects per unit area, N_{it}, and according to Eq. (2.35) SRV will be as

$$S_{n0,p0} = \sigma_{n,p} v_{th} N_{it} \tag{2.46}$$

Finally, to evaluate and interpret the experimental data the bulk recombination model of Richter [71] and the surface recombination model simplified by Olibet [72] were used. The combination of these two models allows calculating carrier injection level dependent effective lifetime and surface recombination velocity. Therefore, the overall recombination rate with the contribution of intrinsic and extrinsic recombination mechanisms can be defined as the effective lifetime (τ_{eff}):

$$\frac{1}{\tau_{eff}} = \underbrace{\left(\frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}}\right)}_{bulk} + \frac{1}{\tau_{surface}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \tag{2.47}$$

$\tau_{surface}$ can be used for calculation of the SRV:

$$\frac{1}{\tau_{surface}} = \frac{S_{front}}{W} + \frac{S_{rear}}{W} \tag{2.48}$$

where W is the thickness of Si wafer, S_{front}- the front SRV and S_{rear}- rear side SRV. Depending on the effective lifetime's values, the most exact expression for SRV was used. For symmetrically passivated structures, S_{front} is expected to be equal to S_{rear} and then the equation can be rewritten

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \tag{2.49}$$

$$S_{eff} = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right) \tag{2.50}$$

Bulk lifetime (τ_{bulk}) then can be calculated based on the model according to Richter [73] provided at PVEducation online platform (`www.pveducation.org`). Based on bulk lifetime,

one more critical parameter can be derived. Diffusion length, L, the average distance that charge carriers diffused before their recombine and defined as following

$$L = \sqrt{D\tau_{\text{bulk}}} \tag{2.51}$$

For the p-type Si wafer, the bulk lifetime is in the order of 3297 μs. If the bulk material quality is high, charge carrier recombination at the surfaces is the dominating recombination mechanisms, since surfaces represent an abrupt termination of the crystal lattice. Lattice termination leads to the creation of energy states in the bandgap energy region, which creates unique recombination centers.

2.3.6   Effect of surface enhancement on generation and recombination processes

Surface energy states could be incorporated with surface modification to enhance light trapping properties in Si. Different texturing techniques are applied to modify the Si surface. More details about such techniques and its results would be presented in this thesis in Chapter 4. Here, a general idea of surface enhancement and its effect on SRV and effective lifetime will be represented. The surface enhancement factor (SEF) γ is involved in the nanostructuring process as the ratio of top surface area of the nanostructure A_{nano} related to the projected area A_{proj} [74],

$$\gamma = \frac{A_{\text{nano}}}{A_{\text{proj}}} \tag{2.52}$$

In Figure 2.5, SEF concept for RIE etch black Si and pyramidal Si surfaces are discussed. Each of these surfaces has different surface area and as a result SEF.
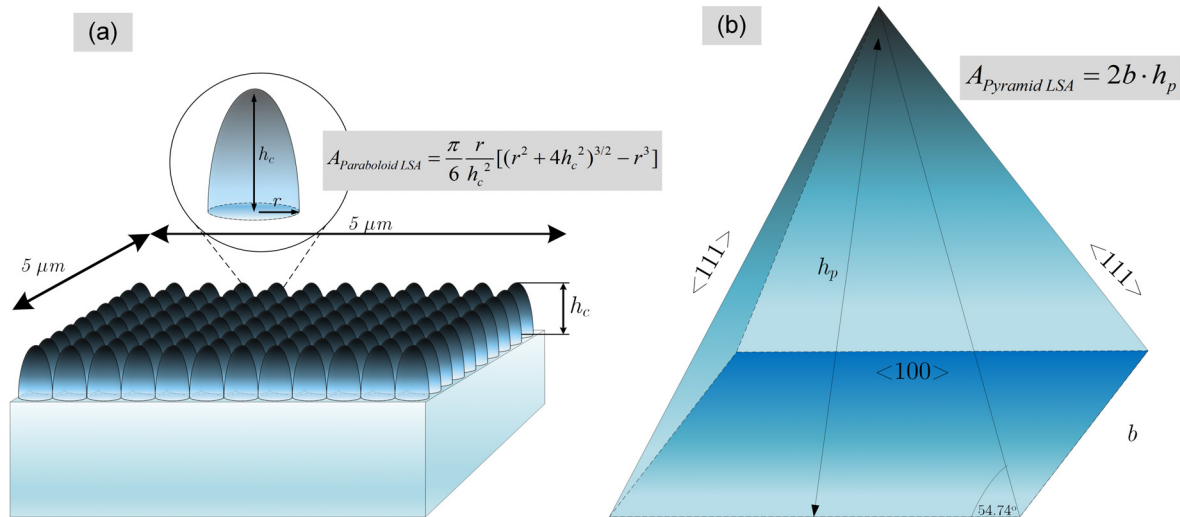
FIGURE 2.5: Surface enhancement area concept for (a) RIE black Si nanostructures with conical shapes and calculated according to intake formula and (b) alkaline etched pyramidal shape Si structures (typical height of Si pyramids is 5 μm)

The SEF is directly related to SRV. If the SRV is not too high the excess carrier concentration n at the surface may be assumed constant, and thus the surface recombination current magnitude is

$$I_{\mathrm{p}} = qnS_{\mathrm{loc}}A \tag{2.53}$$

where S_{loc} is the real recombination velocity at the surface which has the real area A. This current passes, first, through nanotextured area A_{nano} and then through the projected area A_{proj} just below the surface, and thus one may define an effective (projected) SRV S_{eff} such that

$$I_{\mathrm{p}} = qnS_{\mathrm{eff}}A_{\mathrm{proj}} = qnS_{\mathrm{loc}}A_{\mathrm{nano}} \tag{2.54}$$

Solving for the effective SRV yields

$$S_{\mathrm{eff}} = \frac{A_{\mathrm{nano}}}{A_{\mathrm{proj}}}S_{\mathrm{loc}} = \frac{A_{\mathrm{nano}}}{A_{\mathrm{proj}}}\frac{S_{\mathrm{loc}}}{S_{\mathrm{pol}}}S_{\mathrm{pol}} \tag{2.55}$$

where S_{pol} is the SRV of a polished Si surface. Surface modification increases the defect density at the interface D_{it}, and thus enhances the SRV since $S = v_{\mathrm{th}} \times \sigma D_{\mathrm{it}}$ [75]. Since a textured Si surface has a SEF γ as discussed in above and shown in Eq. (2.55), thus one may write

$$S_{\mathrm{eff}} = \frac{A_{\mathrm{nano}}}{A_{\mathrm{proj}}}\frac{D_{\mathrm{loc}}}{D_{\mathrm{pol}}}S_{\mathrm{pol}} = \gamma\varsigma S_{\mathrm{pol}} \tag{2.56}$$

where ς is the ratio of defect densities, showing that two mechanisms increase the SRV. Let's consider the dependency of an effective lifetime on surface recombination on both sides of samples when the bulk lifetime is assumed infinitely large. Then the effective lifetime equation will be according to [72] as

$$\frac{1}{\tau_{\mathrm{eff}}} = \frac{S_{\mathrm{eff}}^{\mathrm{F}} + S_{\mathrm{eff}}^{B}}{W} \tag{2.57}$$

Since in this work, the results of a single-sided, double-sided textured and polished samples are tested, the appropriate equations for each type of samples are given below in Eqs. (2.58)-(2.61) .

Textured front surface, $S_{\mathrm{F}} \neq S_{\mathrm{B}}$

$$\tau_{\mathrm{eff}} = \frac{W}{S_{\mathrm{eff}}} + \frac{4}{D}\left(\frac{W}{\pi}\right)^2 \tag{2.58}$$

$$S_{\mathrm{eff}} = \frac{W}{\tau_{\mathrm{eff}} - \frac{4}{D}\left(\frac{W}{\pi}\right)^2} \tag{2.59}$$

Double side (polished or textured) surfaces, $S_{\mathrm{F}} = S_{\mathrm{B}}$

$$\tau_{\mathrm{eff}} = \frac{W}{2S_{\mathrm{eff}}} + \frac{4}{D}\left(\frac{W}{\pi}\right)^2 \tag{2.60}$$

$$S_{\text{eff}} = \frac{W}{2\left(\tau_{\text{eff}} - \frac{1}{D}\left(\frac{W}{\pi}\right)^2\right)} \tag{2.61}$$

2.4 Light trapping

In the ideal solar cell, all light rays enter the solar cell through the front surface and could be absorbed in the absorber layer. However, in real solar cells light rays pass several material layers before entering the absorber materials. Typically, industrial solar cells have a glass cover, EVA or PVB encapsulation, ARC and passivation coating and absorber material with planar top surface or textures as shown in Fig. 2.6. More advanced techniques help to extend the path of light inside the cell, and they are known as optical confinement or light trapping. As it was presented in Sect. 2.2, the intensity of light decreases exponentially as it propagates through absorber material. Light trapping consists of different physical concepts for photon management to enhance solar cell efficiency by maximizing surface to volume ratio or surface enhancement factor as shown in Eq. (2.52) and explained in Sect. 2.3.6. When light impinges on the top surface of Si, it is affected by a combination of reflection, refraction, and diffraction effects. Only refraction and diffraction can enhance the light trapping process, while reflection should be minimized. Light trapping concepts intended to enhance the optical depth for absorption and open circuit voltage and reduce cell thickness. Several concepts are well known and widely used in Si photovoltaics. Among them are non-diffractive, refractive and diffractive approaches.
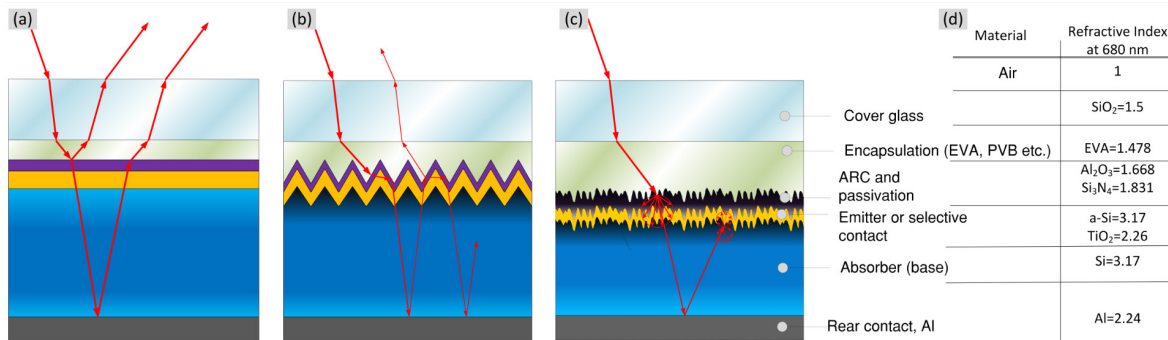
FIGURE 2.6: Sketches of light path in (a) a planar, (b) pyramidal textures and (c) randomly textured solar cell with ARC, encapsulation and glass cover. (d) a table with refractive index data for different layers was adopted from [76]
.

All of these concepts rely on Si optical properties. As known, Si has a high refractive index of 3.5, and in the case of a flat surface, it has high reflectivity (above 30 %) for any incident angle. The reflectivity of a bare Si for incident light at the interface air-Si is given as

$$R = \frac{(1 - n_{\text{Si}})^2 + k_{\text{Si}}^2}{(1 + n_{\text{Si}})^2 + k_{\text{Si}}^2} \tag{2.62}$$

where n_{Si} is the refractive index and k is the extension coefficient of the Si. Both coefficients are functions of the photon wavelength λ as shown in Fig. 2.7. The extension coefficient depends on Si absorption coefficient, and it is represented as

$$k_{\text{Si}} = \frac{\alpha\lambda}{4\pi n} \tag{2.63}$$

As seen from the Eqs. (2.25) and (2.62) reflectivity of Si depends on light incident wavelength and absorption coefficient of Si. There are two types of AR schemes presented below.
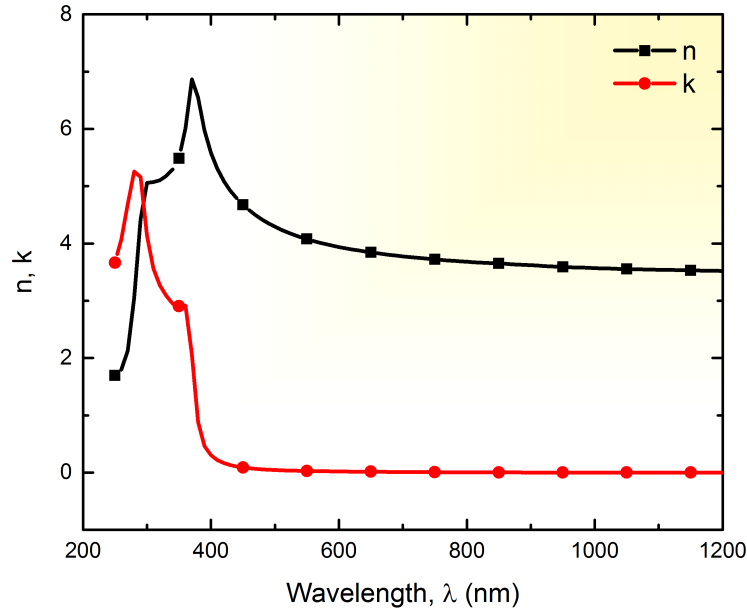
FIGURE 2.7: Refractive index, *n*, and the extension coefficient, *k*, as a function of light wavelength for bare Si calculated according to Eq. (2.63)

2.4.1 Anti-reflective coating

Most recent solar cells rely on a thin layer of a dielectric that works as an ARC [77]. ARC is based on interference of light waves uses destructive suppression of reflectivity over a wavelength range determined by the index of refraction variation and ARC thickness. Such scheme can be realized via deposition a stack with an optical thickness of $\lambda/4$ resulting in an optical path difference of $\lambda/2$ at the interface air-ARC. This concept is known as a quarter-wavelength rule. Figure 2.8 shows reflection as a function of wavelength for bare c-Si; Si coated with glass, and Si with coated with glass and ARC [33]. For single-layer ARC of refractive index n_{ARC} between a top layer or refractive index n_0 (for example, glass or air) and semiconductor, reflection coefficient becomes as:

$$R = \frac{r_0^2 + r_{\text{sc}}^2 + 2r_0 r_{\text{sc}} \cos 2\beta}{1 + r_0^2 + 2r_0 r_{\text{sc}} \cos 2\beta} \tag{2.64}$$

where $r_0 = \frac{n_{\text{ARC}} - n_0}{n_{\text{ARC}} + n_0}$; $r_{\text{sc}} = \frac{n_{\text{sc}} - n_{\text{ARC}}}{n_{\text{sc}} + n_{\text{ARC}}}$; $\beta = \frac{2\pi}{\lambda} n_{\text{ARC}} d$ where d is the thickness of the coating. While transmission coefficient is known as

$$T = 1 - R \tag{2.65}$$

In most cases, r_{sc} and r_0 are positive, and R reduces when

$$d = \frac{\lambda}{4n_{ARC}}; \quad \frac{3\lambda}{4n_{ARC}}; \quad \frac{5\lambda}{4n_{ARC}}; \quad \dots \quad (2.66)$$

mentioned earlier and known as a quarter-wavelength rule, and where

$$n_{ARC} = \sqrt{n_0 n_{sc}} \quad (2.67)$$

Reflection from the top surface can be reduced further by deposition of multilayer coatings. More detailed theory for oblique incident light can be found elsewhere [78]. In Figure 2.8 compares the reflectivity of the bare (polished) Si surface, polished Si coated with ARC single and double layers and textured Si surface coated with single layer ARC.
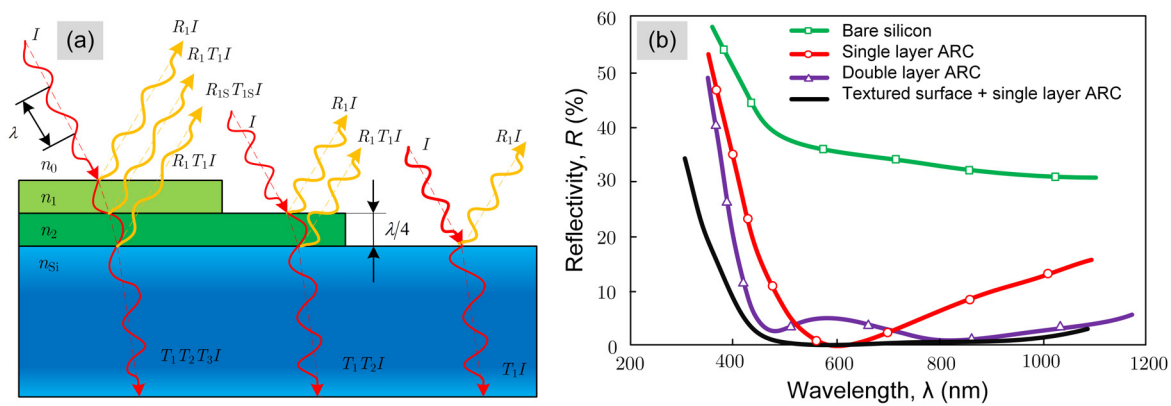
FIGURE 2.8: (a) Interference effect in quarter-wave ARCs; (b) Reflection (Reflectivity) as a function of wavelength λ for bare Si, single, double layer ARC and textured Si surface with ARC
. The data on graph was adopted from [79]

Deposition on multilayer ARC is often too expensive for the most commercial solar cell, it also very sensitive to the layers thickness and incident angle [79]. Therefore, the second concept is widely used to suppress reflectivity on the Si surface and aims to manipulate with the refractive index function at the air-Si interface. To enhance light trapping in the cell with ARC additional texturing is applied that allows to achieve reflectivity below 2 % (using triple ARC system of $ZnS/MgF_2/SiO_2$) as shown in Fig. 2.8 (b) [79]. This may be achieved by modification of top Si surface and obtaining textured surface. In the ideal case, the refractive index could increase continuously in the transition region from air to Si, since single or double layer coating cannot meet the requirements for a broad spectral range. Depending on the shape of textures and material fraction, refractive index became a function of material fraction and called as a density-graded index profile [80–82]. It was demonstrated previously and would be proved once again in this work, that diverse texture morphology can produce the density-graded index.

2.4.2 Geometrical light trapping

Geometrical light trapping relies on trapping of light wavelengths much smaller the typical features sizes leading to light bouncing onto the textured surface multiple times as illustrated in Fig. 2.9. It relies on artificial light trapping schemes based on ray optics [83, 84].

Alkaline etched pyramidal textured surfaces with double-layer ARC are used in most record high-efficiency single-junction Si solar cells with power conversion efficiency over 22 % and as illustrated in Chapter 1 in Fig. 1.14 and it represents the state of the are in Si PV technology.
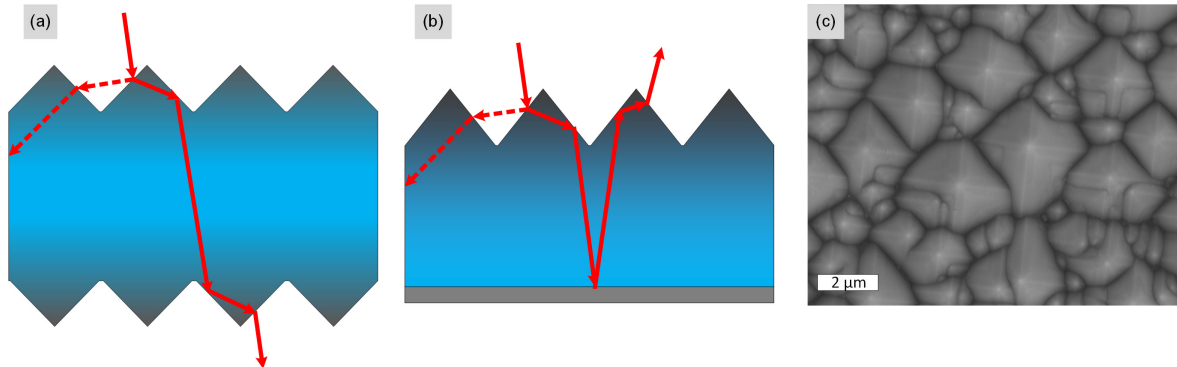
FIGURE 2.9: Geometrical light trapping scheme: (a) bifacially pyramidal structured wafer, (b) single-side structured wafers with a back-side mirror, (c) SEM image of the pyramidal textured Si surface. Structures are not to scale

Initially reflected from the surface light can impinge the absorber several times. However, in most Si solar cell architectures, such as PERC, PERT, etc., the top textured surface is covered with a 110 nm SiO_2 single layer ARC to reduce surface reflectance and improve a short-circuit current I_{SC}. Parameters of pyramidal structure geometry have to be carefully optimized to obtain yield with thinner Si wafers. Otherwise, the light may exit the device if the back reflected ray hits perpendicular facets. These conditions require many lithographic steps to achieve the best geometrical light trapping design including ARC deposition. Important, geometrical light trapping structures are angular selective [85] On the other hand, randomly structured pyramids possess much better light trapping properties due to randomizing effect. Pyramidal Si structures are a cheap industrial method of surface texturing, however, even with an optimized SiN_x ARC on top, it does not allow every reflected ray to hit another pyramid facet. The best light trapping in pyramidal structures could be achieved with bifacial randomized pyramidal structures, backside mirror, and ARC coatings. Even though these structures with additional ARC are used in all record high-efficiency Si solar cells, there are more efficient light trapping concept available and would be presented further in this chapter, and with deep experimental and theoretical studies in Chapter 4.

2.4.3 Randomly structured surfaces

Randomized surface structures are the most efficient light trapping mechanism. It covers the whole optical phase space. The randomizing concept relies on diffractive scattering, consequently leading to a longer light path through the absorber. Yablonovich et al [83] were the first who calculated 50 times light trapping enhancement with the Lambertian scheme. Later Green [67] generalized Yablonovitch formalism to apply it for arbitrary absorption coefficients. Figure 2.10 represents most possible cases of light trapping in single and double side structured slabs with randomizing or Lambertian light trapping scheme and is summarized as following according to indexes in circles:

1. The randomizing or Lambertian scattering scheme is defined as operates fully independent of the angle of incidence due to diffractive multi-scattering centers in the scattering layer.

2. The randomizing structuring scheme is applied only on a single side of the slab, it does not follow $4n^2$ limit but follows the $2n^2$ limit, and in some cases, light can escape through the rear surface even with back reflector layer or create parasitic absorption.

3. Due to multi-scattering in double-sided structured slabs, path length enhancement factor for Si is close to 50 according to Yablonovitch model [83] and Eq. (2.69). Randomizing scattering scheme has a very broadband light trapping for almost all angles of incidence and re-scattering. It shows high scattering probability for wide spectra of wavelengths of light, particularly for visible and near infrared (NIR) spectra (see Chapter 4).

4. Due to refractive index difference between Si and air and multi-scattering centers at the surface, the escape probability at the randomized structured surface is very low.

5. The Lambertian approach utilizes so-called "Yablonovitch" light path enhancement limit of $4n^2$ in the case of double-side structured wafer with perfect white background [83].

6. In case of double-side structuring and re-scattering events on both surfaces, the light escape probability is very low

The light path length enhancement in a double side structured slab which is coupled out after each successive rear reflection can be calculated by following a power series as

$$P = \frac{2W}{n^2} + \frac{6W\left(n^2 - 1\right)}{n^4} + \frac{10W\left(n^2 - 1\right)^2}{n^6} + ... \tag{2.68}$$

where W is slab or wafer thickness. Using power series expansion law, the above equation can be simplified to the expression for the path-length enhancement factor B:

$$B = 4n^2 - 2 \tag{2.69}$$

Since for randomized scheme, the refractive index can become a function of material fraction and gain different value, it is worth to introduce graded refractive index model. As illustrated in the circular intake in Fig. 2.10 the refractive index value between air-silicon media changes if the material fraction differs. In most randomizing schemes, a fraction of the material increases with the material depth and consequently leading to increasing of refractive index or graded refractive index (effective refractive index $n_{z(k+i),eff}$ as a function of a material fraction between air and Si medium) and can be represented as follows:

$$n_{z(k+i),eff} = f_i n_{Si} + \left(1 - f_i\right) n_{air} \tag{2.70}$$

where f_i is the fraction of Si in an i-th layer. In Figure 2.10 square intake a typical refractive index function are represented. Each function corresponds to different shapes of structures. Step-function corresponds to the abrupt interface between air-silicon (polished samples), linear function corresponds to conical or pyramidal shapes of structures, cubic and quantic functions correspond to needle-like, Mie-type structures, and black Si nanostructures.

In this work, the main focus is on black Si as excellent light trapping concept in solar cell. Its theoretical concept is presented further in Subsect. 2.4.4 and in [86, 87].
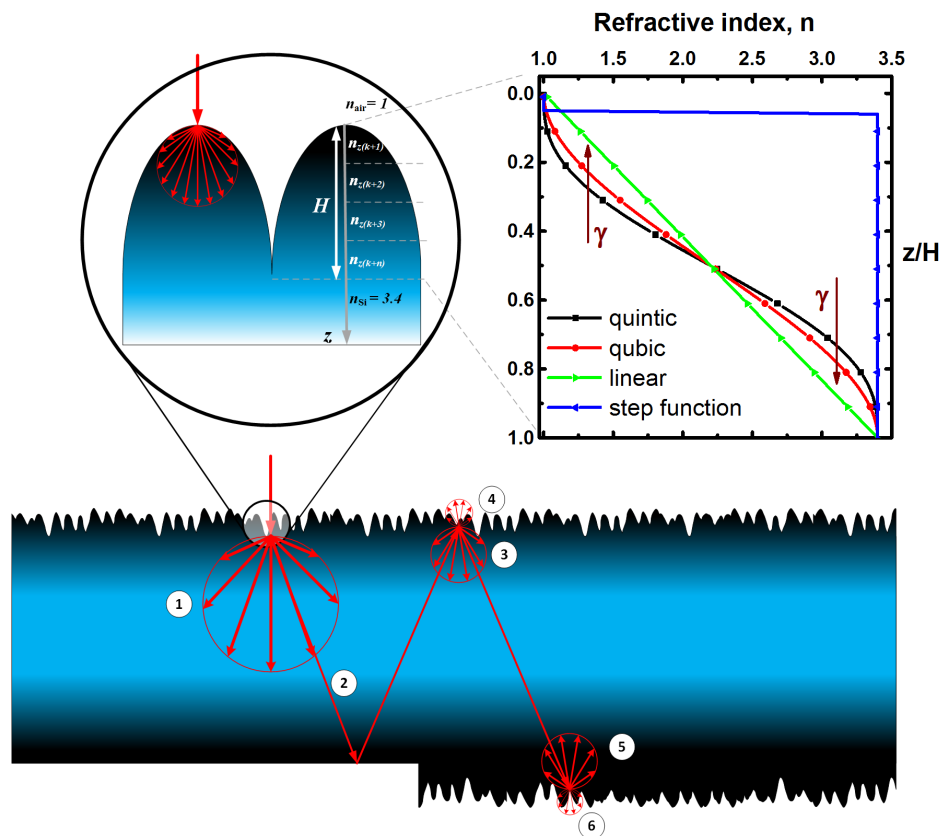
FIGURE 2.10: Randomized light trapping scheme: (1) randomizing scheme is entirely independent of incident angle and creates cosine light distribution due diffractive scattering, (2) single-sided structure path length enhancement factor corresponds to $2n^2$ limit, (3) double-side structures path length enhancement factor corresponds to $4n^2$ limit, (4) due to structuring light escape probability is low, (5) due to multi-scattering in double side structured slabs, path length enhancement factor for Si is close to 50 according to Yablonovitch model, (6) in case of double-side structuring and re-scattering events on both surfaces, the light escape probability is very low. Intake pictures represent a graded refractive index concept: refractive index changes as a function of material fraction or shape and effects light scattering

2.4.4 Black silicon concept

This section will introduce to a brief overview of black Si theoretical concept that lays behind its unique optical properties. Black Si due to its nanostructured surface morphology has excellent AR properties, but more important and often disregarded by other ARC, enhanced light trapping properties [88]. Black Si is randomly textured nanostructures, based on Lambertian light trapping scheme, which appear visibly black because of effective suppression of reflection and simultaneous enhancement of absorption and scattering of light in bulk Si. The reflectivity of the black Si depends on the nanostructures shape and dimensions and the color of the surface changes from silver-gray typical for planar Si surface to black. A graded refractive index may explain optical effect induced by a nanostructured surface, i.e., the nanostructured surface region has a gradual change of Si fraction and air-filled voids surrounding the nanostructures. Consequently, the effective refractive index in the nanostructure region gradually changes from the refractive index of Si and the refractive index of air as shown in Fig. 2.10. This leads to unique optical properties of black Si, e.i. almost zero

reflectivity as it would be discussed in detail in Chapter 4. For short wavelengths (below 800 nm), the light penetrates crystalline Si only in the shallow top layer of nanostructures with almost 99 % absorption. As mentioned above in Subsect. 2.4.3, Yablonovitch describes the ideal AR surface as light trapping surface with a rough surface and inner bulk multi-scattering [83]. Multi-scattering is particularly important for thin wafer and the wavelength with absorption lengths above 800 nm. This concept becomes an important enhancement to the thin film Si solar cells, since it could enhance absorption in the NIR spectral region significantly by 28.4 % I_{NIR}=19.56 mA/cm^2) [89, 90]. Therefore, it is important to control the surface morphology of black Si nanostructures to comply with excellent AR and LT properties. More detailed optical and electro-optical properties of black Si, its optimization strategy to achieve lower RIE damage are presented in Chapter 4.

2.4.5   Other light management concepts: non-diffractive approaches

Examples of non-diffractive approaches are Si nanowires [91, 92], plasmonic resonance metal nanoparticles [93], and structures, dielectric Mie resonators [94–96]. Silicon nanowires exhibit extreme SEF but suffer stability of junction, surface passivation and issues with nanowire integration into modules. Plasmonic resonance metal particles absorb at resonance wavelength and efficiently scatters the incident light into the thin film. Important to note, the particles dimensions affect resonance conditions. Solar cells with plasmonic nanostructures were reported to enhance power conversion efficiency by 30 %. Spinelli et al. [94] proposed dielectric Mie resonators, where they demonstrated almost perfect impedance matching from ultraviolet (UV) to the NIR spectral range using arrays of 150 nm long Si nanopillars with less than 3 % reflectivity for the entire spectral range 450-900 nm. All above concept are discussed only for acquaintance purposes and will not be discussed further.

2.5   Solar cell operating principles and device physics

The first solar cell used for power energy conversion of solar light into electric energy was first reported in 1954 [97] and was based on a diffused Si p-n–junction. Since that times Si solar cells have a slight difference in their working principles and physical concept behind. A solar cell converts sunlight photon energy directly to electric energy, using photovoltaic effect. Each solar cell has three essential components: light absorption and conversion material (for example Si etc.), conductive contact layers on front and back (metal grid, TCO, etc.) and built-in electric field in p-n–junction as shown in Fig. 2.11. Each photon, absorbed in a material, excites an electron from valence energy band to conduction energy band, leaving a hole in the valence band. Under electric field electron and hole pulled in the different direction in the solar cell to the external circuit via conductive contacts as shown in Fig. 2.11.

2.5.1   Solar cell parameters

The basic performance characteristics of solar cells have been described by many authors [20, 34, 98, 99]. Every solar cell can be characterized and evaluated by a set of its parameters. These parameters can tell if the solar cell functions with the highest efficiency or if it has any problems causing efficiency or performance drop. Most important parameters that account for solar cell performance are total electric current J, short-circuit current J_{SC}, dark current J_D, open circuit voltage V_{OC}, maximum power P_{max}, power conversion efficiency η. The external net-current in the solar cell can be written as
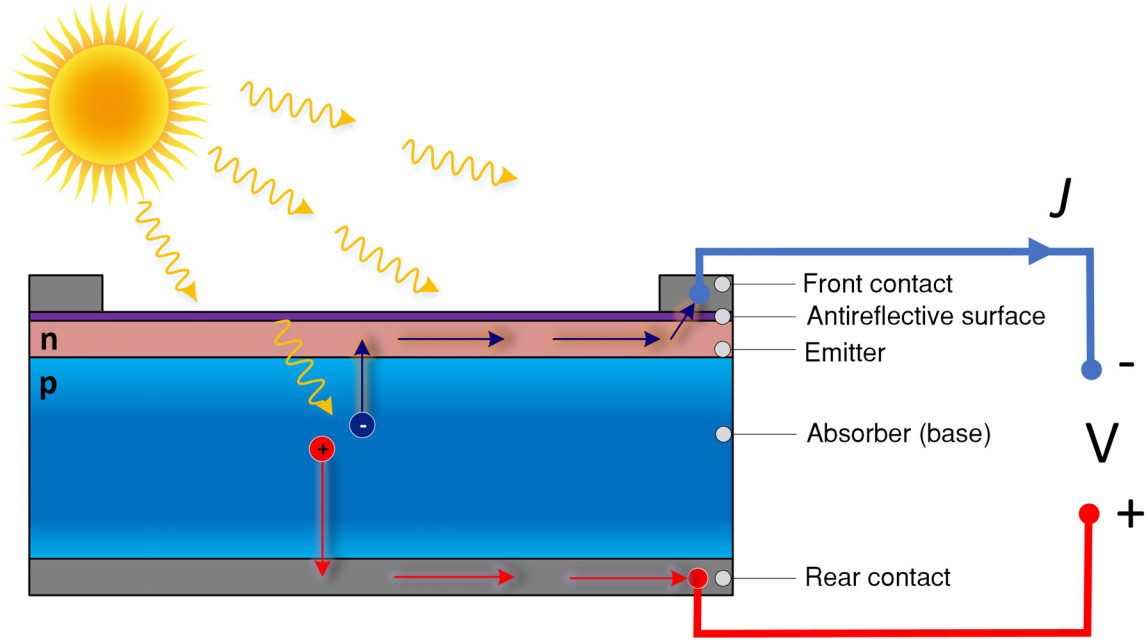
FIGURE 2.11: Cross section of one of the typical solar cell consisting of a p-type absorbing base, a p-n–junction and metal contacts

$$J(V) = J_{\mathrm{SC}} - J_{\mathrm{D}}(V) \tag{2.71}$$

where the short-circuit current J_{SC} is related to the absorbed photon spectrum by measurement of cell's quantum efficiency (QE), which is the probability of the incident photon of energy E to be absorbed and converted to charge carriers.

$$J_{SC} = q \int_{E_g}^{\infty} \Phi_{\mathrm{ph}}(E) A(E) C(E)\, dE \equiv q \int_{E_g}^{\infty} \Phi_{\mathrm{ph}}(E)\, EQE(E)\, dE \tag{2.72}$$

where E is the photon energy, E_{g} is the bandgap of the absorber (i.e. Si), $\Phi_{\mathrm{ph}}(E)$ is the incident spectral photon flux density, $A(E)$ is the photon absorbance, $C(E)$ is the collection efficiency (i.e. the fraction of photogenerated electron-hole pairs that are collected at their respective contacts, $EQE(E)$ - is the external quantum efficiency. Consequently, short circuit current allows diagnosing absorption behavior of the solar cells.

Dark current J_{D} is voltage-dependent recombination current:

$$J_{\mathrm{D}}(V) = J_0 \left[\exp\left(\frac{qV_{\mathrm{j}}}{n_{\mathrm{d}} k_{\mathrm{B}} T} \right) - 1 \right] \tag{2.73}$$

Here, J_0 and n_{D} are dark saturation current and diode ideality factor, respectively.

For the ideal case n=1 and from diffusion theory [100] J_0 is given as

$$J_0 = q n_i^2 \left[\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p} \right] \tag{2.74}$$

where n_i^2 is defined by Eq. 2.26, L_n and L_p are diffusion lengths of minority carriers and defined by Eq. 2.51, N_A and N_D are the acceptor and donor concentrations, D_n and D_p are diffusivities. The Einstein relation relates the diffusivity D and the mobility μ:

$$D = \frac{k_B T}{q} \mu \tag{2.75}$$

In Equation 2.74 the intrinsic carrier concentration n_i is given as

$$n_i^2 = N_V N_C \exp\left(\frac{-E_g}{k_B T}\right) \tag{2.76}$$

where E_g is the semiconductor energy bandgap (i.e. Si E_{gSi}=1.2 eV), N_V and N_C are the valence and conduction band density of states.

V_j is the voltage across the junction given by

$$V_j = V - J(V) R_S \tag{2.77}$$

where V is the total voltage across the solar cell and R_s is the series resistance.

Plots of Eqs. 2.71 and 2.73 are shown in Fig. 2.12 for the illuminated and dark case in linear and semilog graphs.
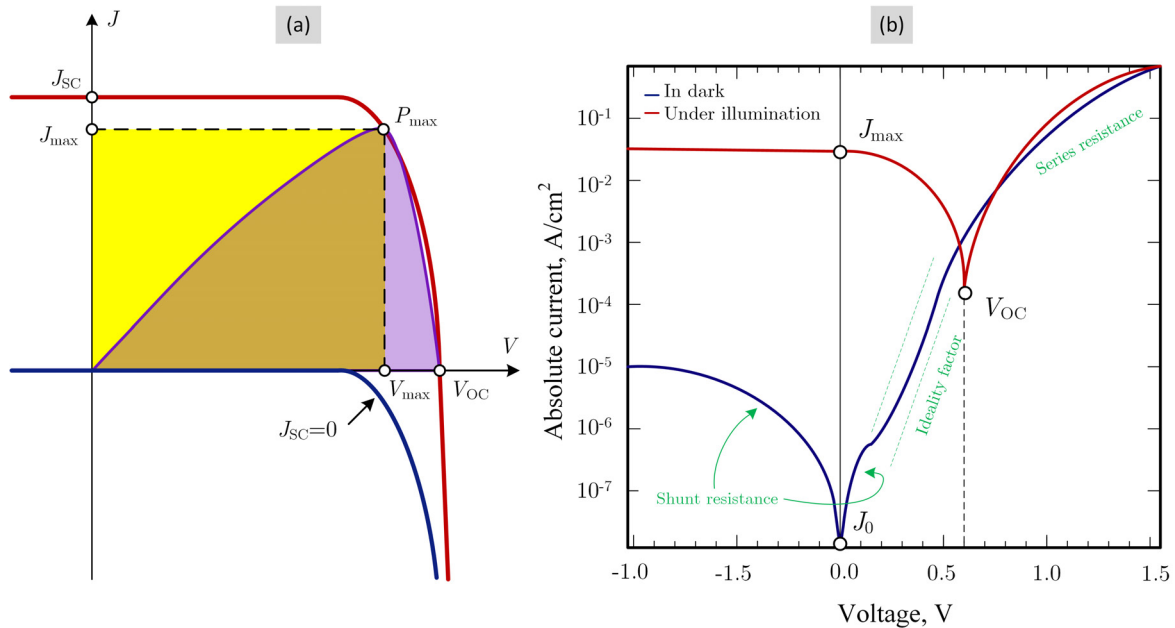
FIGURE 2.12: Current density-voltage characteristics of the solar cell under illuminated and dark conditions: (a) linear scale graph and (b) semilog graph

Ideally, short-circuit current J_{SC} is a quantity greater than zero at zero voltage. At dark conditions, J_{SC}=0 and the current-voltage behavior of the solar cell is the same as p-n–junction diode.

$$J(V) = -J_D(V) \tag{2.78}$$

As it is seen, the maximum power can be extracted by biasing the solar cell at a certain voltage where the JV product would be maximized. This voltage is labeled as $V_{\max}$, and the corresponding current density is labeled as $J_{\max}$. Then, the maximum power point (MPP) with the power is

$$P_{\max} = A V_{\max} J_{\max} \tag{2.79}$$

where A is the areas of the solar cell.

Another important parameter of the solar cell performance is Fill Factor FF that defines the sharpness of the JV curve. The fill factor is defined by

$$FF = \frac{J_{\max} V_{\max}}{J_{\mathrm{SC}} V_{\mathrm{OC}}} \tag{2.80}$$

The efficiency of the solar cell η is given as a converted electric power to the incoming power from the sun:

$$\eta = \frac{P_{\max}}{P_{\mathrm{in}}} = \frac{A V_{\max} J_{\max}}{\int \Phi_{\mathrm{ph}}(E) E dE} \tag{2.81}$$

Substituting Eq. 2.79 into 2.80, the efficiency η will be given as

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{A V_{\max} J_{\max} FF}{P_{\mathrm{in}}} \tag{2.82}$$

When $J=0$ in the Eq. 2.71 the open circuit voltage V_{OC} can be defined as

$$V_{OC} = \frac{n k_{\mathrm{B}} T}{q} \ln\left(\frac{J_{\mathrm{SC}}}{J_0} + 1\right) \approx \frac{n k_{\mathrm{B}} T}{q} \ln \frac{J_{\mathrm{SC}}}{J_0} \tag{2.83}$$

Equation 2.71 can be expressed more detailed as

$$J(V) = J_{SC} - (J_{\mathrm{diff}} + J_{\mathrm{rec}} + J_{\mathrm{tun}}) \tag{2.84}$$

$$J(V) \approx J_{\mathrm{SC}} - \left[J_{0,\mathrm{diff}}\left(\exp\left(\frac{q V_{\mathrm{j}}}{k_{\mathrm{B}} T}\right) - 1\right) + J_{0,\mathrm{rec}}\left(\exp\left(\frac{q V_{\mathrm{j}}}{k_{\mathrm{B}} T}\right) - 1\right) + J_{\mathrm{tun}} \right] \tag{2.85}$$

where the tunneling component J_{tun} will be described later in Sect. 2.6.5. At high forward voltage, ideality factor is equal to 1 and can be neglected. At lower voltages, the recombination current J_{rec} will dominate at the maximum power point and thus reduce the fill factor of the cell.

The tunneling current J_{tun} contributes for the structures with TiO_2, Al_2O_3, and SiO_2, NiO layers. In the case of TiO_2-SiO_2 and TiO_2-Al_2O_3 structures, the tunneling current has two components. The details of this concept will be discussed in Subsect. 2.6.5 and in Chapters 3.

The external quantum efficiency $EQE(\lambda_0)$ is the fraction of incident photon flux on the solar cell that generates electron-hole pairs in absorber material. EQE is wavelength dependent and measured by illuminating the solar cell with a very narrow or monochromatic light of

wavelength λ_0 and simultaneously measuring the photogenerated current I_{SC}. The external quantum efficiency is given then as

$$EQE\left(\lambda_0\right) = \frac{J_{SC}\left(\lambda_0\right)}{-q\Phi_{ph}\left(\lambda_0\right)} \tag{2.86}$$

The J_{SC} is dependent on the bias voltage. Therefore, the bias voltage is fixed during the measurements.
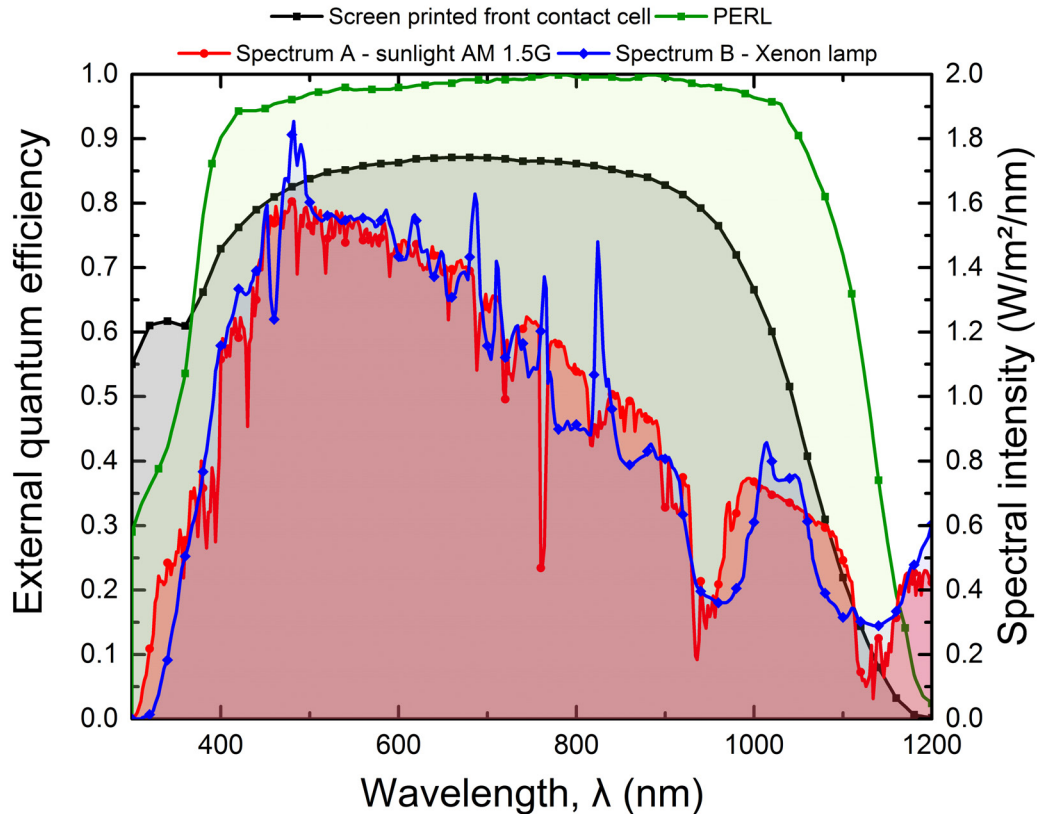
FIGURE 2.13: External quantum efficiencies of screen printed front contact and PERL overlapped with standard sun spectrum AM1.5G and spectrum from xenon lamp used in typical solar simulator source [76]

Figure 2.13 illustrates a typical EQE for screen printed front contact solar cell (from Aecusoft WPVS reference cell) and PERL cell from UNSW reported in 1998 [101]. Additionally, the Fig. 2.13 includes irradiance spectrum of sun AM1.5G and xenon lamp spectrum.

2.5.2 Equivalent Solar Cell Circuit

Any Si solar cell under illumination can be represented as an ideal p-n–junction diode in parallel with a current source in the proximity of the junction as shown in Fig. 2.14 and described by Eq. (2.87).

$$J\left(V\right) = J_{SC} - J_0\left[\exp\left(\frac{qV_j}{n_d k_B T}\right) - 1\right] \tag{2.87}$$

This behavior can be explained according to the Fig. 2.14, however, without series and shunt resistance components. In such a case a diode and current source are connected in parallel. A p-n–junction forms the diode. The dark current density J_D is given in Eq. (2.73). If series and shunt resistance are included in the model that the equation will be modified. The current density source J_{SC} represents the photo-generated current density, which flows in the opposite direction to the diode current density J_D. The equivalent electric circuit contains a shunt resistor R_{sh} in parallel and series resistor R_s in series with a diode as a schematic of the equivalent circuit in Fig. 2.14. The internal voltage drops are represented by series and shunt resistances and the resulting load current is than J_{SC}–J_D–(V/R_{sh}). Under forward bias the current in a such diode flows in the opposite direction and hence one can write resulting load current as $-J = J_{SC} - J_D$–(V/R_{sh}). If the series resistance is inserted before the shunt resistance, then the voltage drop across the p-n–junction is according to [98]:

$$V \approx V + JR_s + \left(\frac{R_s}{R_{sh}}\right)V \qquad (2.88)$$

In practice the fill factor (FF is effected by the series R_s and shunt R_{sh} resistances of the solar cells. These parameters can be studied by using the equivalent circuit represented in Fig. 2.14. This equivalent circuit is a one diode equivalent circuit with series and shunt resistance and can be represented as:

$$J(V) = J_{SC} - J_0\left[\exp\left(\frac{V_j - AJR_S}{n_d k_B T}\right) - 1\right] - \frac{V_j - AJR_S}{R_{sh}} \qquad (2.89)$$
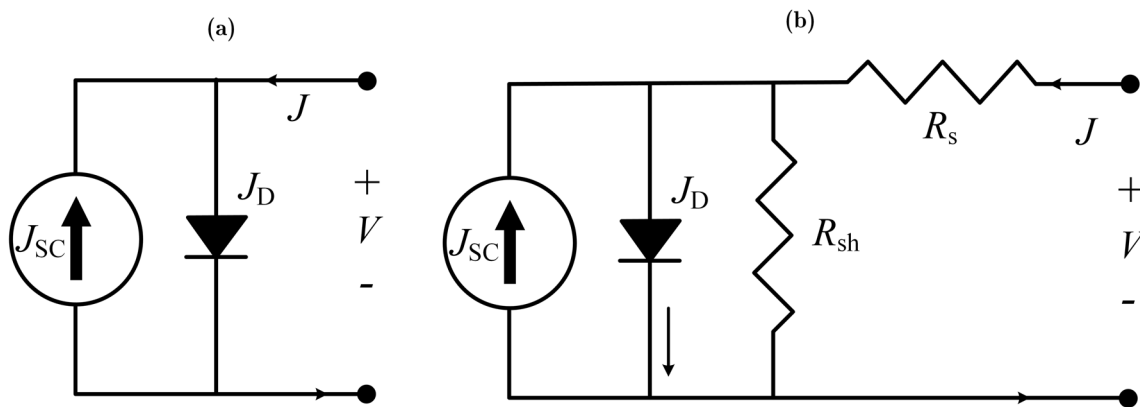
FIGURE 2.14: Equivalent electric circuit of (a) an ideal solar cell and (b) a solar cell with parallel to the p-n–junction shunt resistor and in series resistor

Shunt R_{sh} and series R_s resistances demonstrate the effect on output characteristics of the solar cells. Shunt resistance is expected to be as high as possible, while series resistance is projected to be opposite. The effect of R_{sh} and R_s on $J - V$ characteristic is illustrated in Fig. 2.15

As seen from the Fig. 2.15 shunt and series resistances influence on FF. These effects depend on recombination processes in the p-n junction. In such a case one deals with a non-ideal diode as shown in Fig. 2.14 (b) with ideality factor larger than unity. However, the equivalent circuit of a practical solar cell is much more complicated and represented as a two-diode model in Fig. 2.16. The corresponding analytic equation of the two-diode model is the following
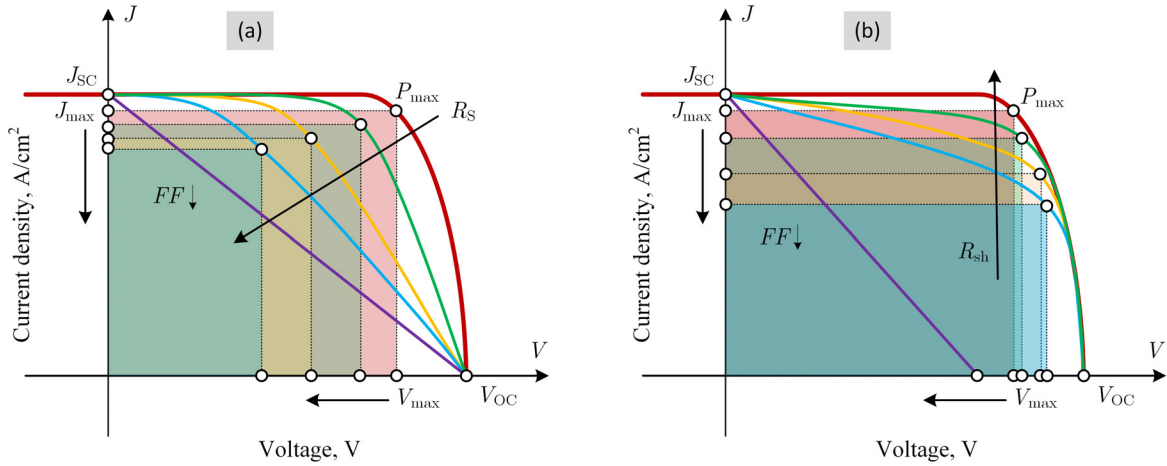
FIGURE 2.15: Effect of parasitic resistances on the $J - V$ characteristic of a solar cell: (a) series resistance effect (R_{sh}=const), (b) shunt resistance effect (R_s=const)

$$J(V) = J_{SC} - J_{01}\left[\exp\left(\frac{V_j - JR_S}{n_1 k_B T}\right) - 1\right] - J_{02}\left[\exp\left(\frac{V_j - JAR_S}{n_2 k_B T}\right) - 1\right] - \frac{V_j - JAR_S}{R_{sh}} \quad (2.90)$$

where J_{01} and J_{02} are the saturation currents of the two diodes, respectively, and n_1 and n_2 are corresponding ideality factors.
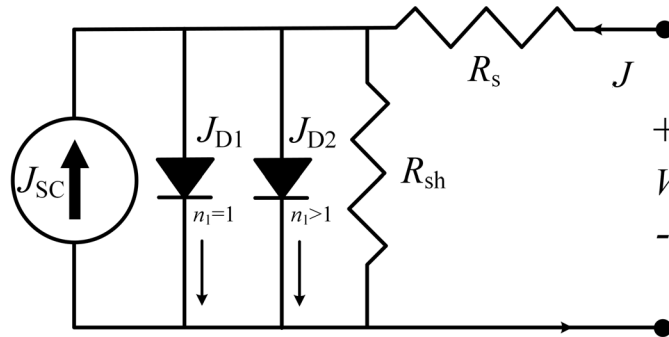
FIGURE 2.16: The equivalent electric circuit of a solar cell based on a two-diode model

2.6   Heterojunction carrier selective contacts

The junction between two semiconductors with different energy bandgap materials is denoted as a heterojunction. Heterojunctions have unique electrical or electro-optical properties between two different materials.There are two types of heterojunctions namely the anisotypical and the isotypical heterojunctions. Anisotypical junctions are the combination of two semiconductors with different conduction types, i.e., a p-n–junction. The isotypical junction is a mix of identical conduction type materials. (n-n or p-p junction).

To understand the nature of the heterojunctions, different models were developed that effectively predict heterojunction properties based on geometrical and structural parameters.

The most commonly used models are Andersen energy band model [102], Frensley and Kroemer model that predicts mean potential and includes interface dipoles [103]. Harrison LCAO model that helps to calculate valence band maxima based on linear combination of atomic orbitals [104]. Adams and Nussbaum's model contributes to defining the intrinsic level of the semiconductor [105]. Ross model [106] considers the total difference of the bandgaps as valence band offset and the conduction band as a reference potential. Tersoff model [107] considered midgap as a common reference potential, and interface states and dipoles characterize the junction. Even though these models define heterojunction theory, they all lack agreement with experimental data. Milnes [108] summarized different heterojunctions in his book, and some part of it is applied to the heterojunctions in this work.

2.6.1 Requirements for effective heterojunctions on c-Si

This section discusses the requirements for effective heterojunction on c-Si solar cells. The first requirement is to have a valence (preferred for hole transport) or conduction (preferred for electron transport) band alignment for semiconductor materials depending on the type of junction. The band alignments of a heterojunction create conditions for carrier selectivity by creating one type of carrier transport in valence or conduction band and blocks another carrier flux out of the absorber.

Such conditions allow avoiding interface defects recombination. However, heterojunction tends to form energy offset spikes that can work as a block to carrier transport. Therefore, the second requirement is to keep band offset spikes as low as possible (≤ 0.2 eV) in the designated carrier transport band. On the opposite, the energy band offset for carrier blocking should be as high as possible (≥ 0.5 eV).

The third requirement is effective interface passivation of defects and dangling bond. The defects can be passivated by the formation of new bonds to the heterojunction material.

2.6.2 Construction of a heterojunction band diagram

In the first step, the various semiconductor materials are connected to close contact (Fig. 2.17). According to Andersen model, a common Fermi level is established, and space charge is built up. In the case of an anisotypical homojunction (Fig. 2.17 (a) and (c)), two materials create p-n–junction without any defects, band spikes or discontinuities under no voltage bias applied. The energy band diagram of a heterojunction is complicated somewhat more than that of a homojunction because of the presence of the discontinuities in either conduction or valence bands and denoted as ΔE_{C} and ΔE_{V}. In the case of heterojunctions, two materials have different energy bandgap and crystal lattice, that create abrupt heterojunction with spikes and discontinuities and possible interface defects (Fig. 2.17 (b) and (d)).

Examples of heterojunctions diode that widely used in Si solar cell are Si/TiO$_2$ [109], Si/NiO [110], Si/a-Si [36], Si/Mo$_2$O$_3$ [48], Si/TaO$_2$ [111], Si/WO$_3$ [47], Si/V$_2$O$_5$, Si/ZnO [112], etc. Four cases of abrupt heterojunction type are discussed in this thesis: isotypical n-n and p-p heterojunction and anisotypical n-p and p-n as shown in Fig. 2.18. These energy band diagrams fit well for heterojunctions of TiO$_2$/Si (Fig. 2.18 (a)-(b)) and NiO/Si (Fig. 2.18 (c)-(d)). Both TiO$_2$ and NiO are wide bandgap semiconductors and form II-nd type of heterojunction.
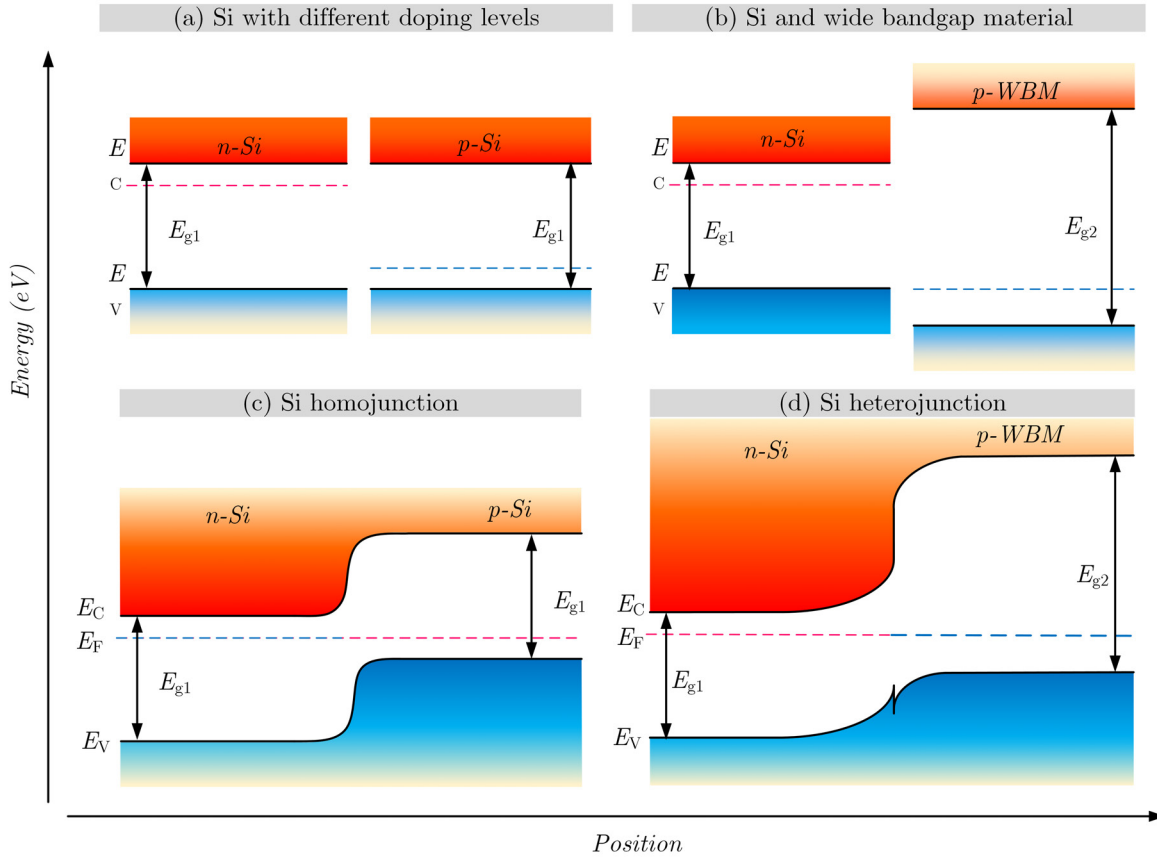
FIGURE 2.17: Energy-band diagram for Si homojunction and heterojunction: before the establishment of the thermal equilibrium for (a) homojunction and (b) heterojunction; after the establishment of the thermal equilibrium for (c) homojunction and (d) heterojunction

2.6.3 Derivation of p-n–heterojunction theory

Based on Anderson model [102] the conduction and valence band offsets ΔE_{C} and ΔE_{V} can be obtained from the energy band diagram shown in Fig. 2.18 and are given by

$$\Delta E_{\mathrm{C}} = q\left(\chi_{\mathrm{Si}} - \chi_{\mathrm{WBS}}\right) \tag{2.91}$$

$$\Delta E_V = \left(E_{\mathrm{g\,WBS}} - E_{\mathrm{g\,Si}}\right) - \Delta E_{\mathrm{C}} \tag{2.92}$$

The total built-in potential V_{bi} is defined as Fermi displacement and

$$V_{\mathrm{bi}} = E_{\mathrm{F_n}} - E_{\mathrm{F_p}} = \left(\chi_{\mathrm{Si}} + E_{\mathrm{g\,Si}} - \delta_{\mathrm{Si}}\right) - \left(\chi_{\mathrm{WBS}} + \delta_{\mathrm{WBS}}\right) = V_{\mathrm{D_n}} + V_{\mathrm{D_p}} \tag{2.93}$$

where $V_{\mathrm{D_n}}$ and $V_{\mathrm{D_p}}$ are the band bending potentials in Si and WBS, respectively. It is noted that the discontinuity of the electrostatic field at the interface is due to the difference in dielectric constants of these materials. Using Poisson's equation (2.21) in the depletion region of the heterojunction diode and the two boundary conditions, one can write
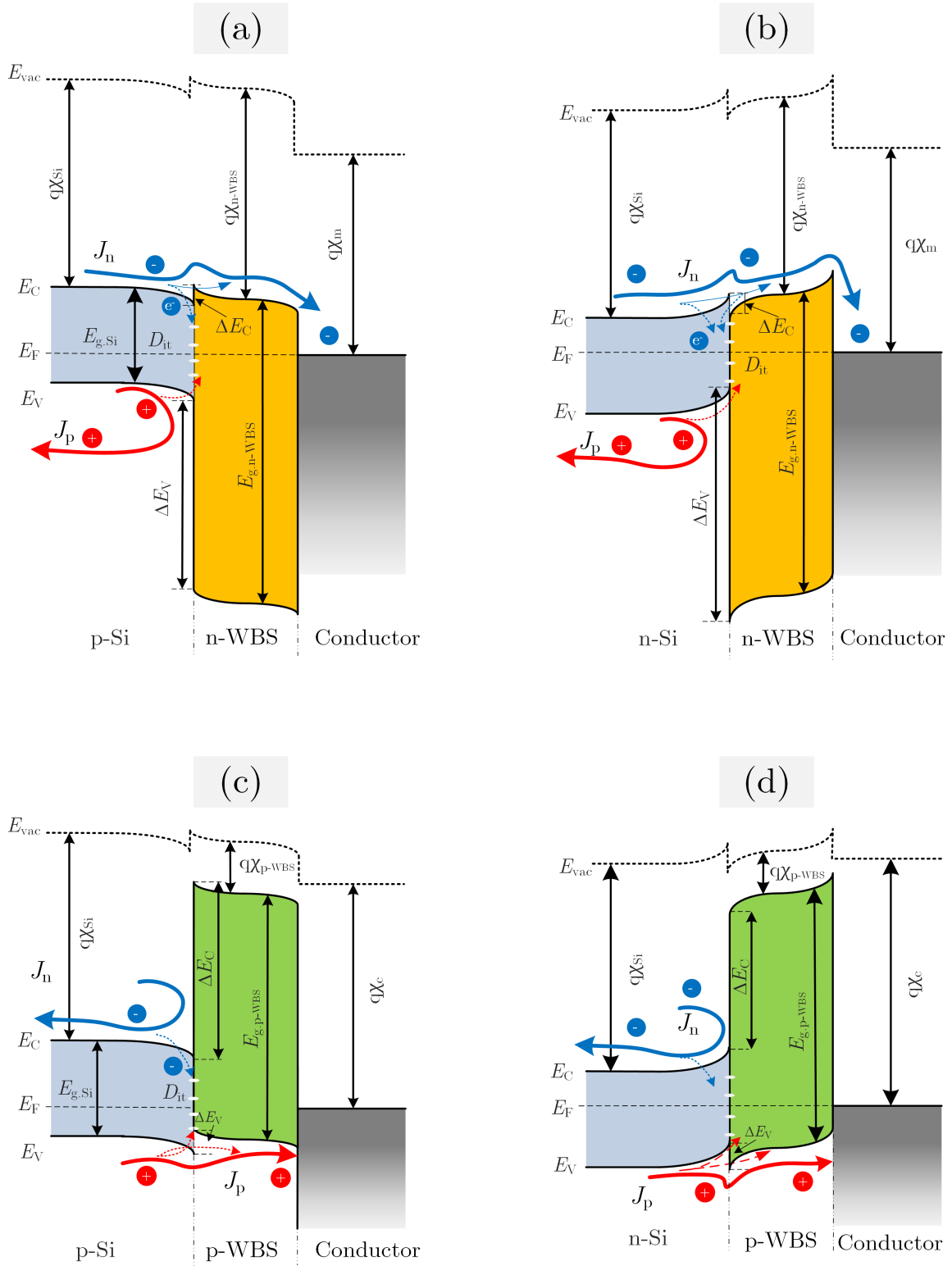
FIGURE 2.18: Energy band diagram for (a) n-WBS-p-Si, (b) n-WBS-n-Si, (c) p-WBS-p-Si, (d) p-WBS-n-Si heterojunctions. Note: WBS stands for wide bandgap semiconductor

$$\frac{\chi_{\text{WBS}}}{\chi_{\text{Si}}} = \frac{N_{\text{A}_{\text{WBS}}}}{N_{\text{D}_{\text{Si}}}} \tag{2.94}$$

$$\varepsilon_{\text{Si}} E_{\text{Si}} = \varepsilon_{\text{WBS}} E_{\text{WBS}} \tag{2.95}$$

Using Poisson's equation (2.21) one can derive the following relations

$$V_{\text{D}_\text{n}} = \frac{N_{\text{D}_\text{Si}} \chi^2_{\text{WBS}}}{2\varepsilon_{\text{WBS}}} \tag{2.96}$$

and

$$V_{\text{D}_\text{p}} = \frac{N_{\text{A}_\text{WBS}} \chi^2_{\text{Si}}}{2\varepsilon_{\text{Si}}} \tag{2.97}$$

$$\frac{V_{\text{D}_\text{n}}}{V_{\text{D}_\text{n}}} = \frac{N_{\text{A}_\text{WBS}} \varepsilon_{\text{Si}}}{N_{\text{D}_\text{Si}} \varepsilon_{\text{WBS}}} \tag{2.98}$$

The depletion approximation enables V_{D_n} and V_{D_p} in the p-Si and n-TiO$_2$ region to be expressed respectively by

$$V_{\text{D}_\text{n}} = \frac{\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}}}{\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}}} V_{\text{bi}} \tag{2.99}$$

$$V_{\text{D}_\text{p}} = \frac{\varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}}}{\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}}} V_{\text{bi}} \tag{2.100}$$

Under assumption of a Schottky barrier at the interface, the solution of Poisson's equation yields the depletion layer widths on either both sides of the abrupt heterojunction diode under bias conditions and then given, respectively, as

$$W_{\text{Si}} = \sqrt{\frac{2N_{\text{A}_\text{WBS}} \varepsilon_{\text{Si}} \varepsilon_{\text{WBS}} (V_{\text{bi}} - V)}{q N_{\text{D}_\text{Si}} (\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}})}} \tag{2.101}$$

$$W_{\text{WBS}} = \sqrt{\frac{2N_{\text{D}_\text{Si}} \varepsilon_{\text{Si}} \varepsilon_{\text{WBS}} (V_{\text{bi}} - V)}{q N_{\text{A}_\text{WBS}} (\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}})}} \tag{2.102}$$

Therefore, the total depletion layer width of the heterojunction is a sum of depletion layer widths from Eqs. (2.101) and (2.102) as

$$W_{\text{d}} = W_{\text{Si}} + W_{\text{WBS}} = W_{\text{Si}} = \sqrt{\frac{2\varepsilon_{\text{Si}} \varepsilon_{\text{WBS}} (V_{\text{bi}} - V) \left(N^2_{\text{A}_\text{WBS}} + N^2_{\text{D}_\text{Si}}\right)}{q N_{\text{D}_\text{Si}} N_{\text{A}_\text{WBS}} \left(\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}}\right)}} \tag{2.103}$$

The transition capacitance per unit area for the p-n–heterojunction can be derived from Eq. (2.103) and the result yields

$$C_{\text{j}} = \sqrt{\frac{q N_{\text{D}_\text{Si}} N_{\text{A}_\text{WBS}} \varepsilon_{\text{Si}} \varepsilon_{\text{WBS}}}{2 \left(\varepsilon_{\text{Si}} N_{\text{D}_\text{Si}} + \varepsilon_{\text{WBS}} N_{\text{A}_\text{WBS}}\right) (V_{\text{bi}} - V)}} \tag{2.104}$$

The current-voltage ($I - V$) characteristics for n-p heterojunction diode can be derived using the energy band diagram and thermionic emission theory for a Schottky barrier diode. Under thermal equilibrium condition, the two oppositely directed fluxes of the carrier must be equal since the net current flow is zero. Then, one can write

$$A_{\text{Si}} \exp\left[-\frac{(\Delta E_v - qV_{\text{bSi}})}{k_B T}\right] = A_{\text{WBS}} \exp\left(-\frac{qV_{\text{bWBS}}}{k_B T}\right) \tag{2.105}$$

where A_{Si} and A_{WBS} are constants that depend on the doping levels and carrier effective masses on materials in the diode.

Under forward-bias voltage V_a across the junction, the voltage drops on the two sides of the junction are determined by the relative doping densities and dielectric constants of the materials and given as

$$V_{\text{WBS}} = \underbrace{\frac{N_{\text{D}_{\text{Si}}}\varepsilon_{\text{Si}}}{N_{\text{D}_{\text{Si}}}\varepsilon_{\text{Si}} + N_{\text{A}_{\text{WBS}}}\varepsilon_{\text{WBS}}}}_{K_2} V_a \tag{2.106}$$

and

$$V_{\text{Si}} = \underbrace{\left(1 - \frac{N_{\text{D}_{\text{Si}}}\varepsilon_{\text{Si}}}{N_{\text{D}_{\text{Si}}}\varepsilon_{\text{Si}} + N_{\text{A}_{\text{WBS}}}\varepsilon_{\text{WBS}}}\right)}_{1-K_2} V_a \tag{2.107}$$

By using Eq. (2.105) the net carrier flux from right to the left under forward-bias conditions can be expressed by

$$\phi_n = A_{\text{WBS}} \exp\left(-\frac{qV_{\text{bSi}}}{k_B T}\right)\left(\exp\left(\frac{qV_{\text{bWBS}}}{k_B T}\right) - \exp\left(\frac{qV_{\text{bSi}}}{k_B T}\right)\right) \tag{2.108}$$

If thermionic emission dominates the conduction mechanism, the current density due to electron injection from p to n of the n-p–heterojunction diode shown in Fig. 2.18 (a) has a similar form as that given by Eq. (2.108). Then, the electron current density can be written as

$$\begin{aligned}
J_n &= A \exp\left(-\frac{qV_{\text{bSi}}}{k_B T}\right)\left(\exp\left(\frac{qV_{\text{bWBS}}}{k_B T}\right) - \exp\left(\frac{qV_{\text{bSi}}}{k_B T}\right)\right) \approx \\
&\approx J_0 \left(1 - \frac{V_a}{V_{\text{bi}}}\right)\left(\exp\left(\frac{qV_a}{k_B T}\right) - 1\right)
\end{aligned} \tag{2.109}$$

where

$$J_0 = \left(\frac{qA^* T V_{\text{bi}}}{k_B}\right)\exp\left(-\frac{qV_{\text{bi}}}{k_B T}\right) \tag{2.110}$$

It is important to note that Eq. (2.109) was obtained under approximation that $\exp\left(\frac{q(V_{\text{hSi}} - V_{\text{Si}})}{k_B T}\right) \approx \left(\frac{q}{k_B T}\right)(V_{\text{bi}} - V_a)$, and the total applied voltage. From Eq. (2.109) is seen that the current-voltage relation for n-p heterojunction diode is different from that of a metal-semiconductor Schottky diode.

2.6.4   Interface passivation

One of the fundamental problems of the heterojunction is the interrupted periodicity of the crystalline semiconductors at the interface. Such interruptions lead to electronic defects, particularly surface states. These state (white dots at the interface of heterojunction in Fig. 2.18 are capable of capturing electron and holes during their transport across the interface and act as recombination centers. The effect of interface recombination centers was studied in this work in Chapters 3 and 4. The recombination centers represented as dangling bonds and can be passivated with either chemical passivation with atomic hydrogen or charges induced electric field generated by the strong charges in wide bandgap material. Chemical passivation is mainly based on hydrogen passivation or termination. In the heterojunction Si solar cell technology, the hydrogen passivation is applied via annealing in a forming gas or with materials decomposing the complex molecules containing hydrogen, for example, organic precursors in ALD or CVD processes. Another passivation technique is HF solution dip. Electrostatic passivation is based on depletion, accumulation and inversion modes. The energy band diagram has a Si bending that creates a barrier for charge transport to the interface and therefore, recombination at the interface.

2.6.5   The effect of tunneling oxide on carrier selectivity

In the case of heterojunction Si solar cell the diode Eq. (2.85) will obtain another form. Most contributions to the equation would be distinguished by the diffusion $J_{0,\mathrm{diff}}$ and depletion layer $J_{0,\mathrm{rec}}$ recombination-generation components of the reverse saturation current density. Additional tunneling component is also included into equation due to several tunneling mechanisms. Ultra thin oxides of SiO_2 and Al_2O_3 are used as passivation layers in heterojunctions. One of the critical parameters for selection of such passivating films is tunneling probability. To evaluate carrier tunneling through oxide films nonlocal tunneling model can be used [113, 114]. It is assumed that the tunneling current can completely support the total transport through the ultra-thin oxide layer and current transport through pinholes in the oxide layer is not considered. Tunneling probability is calculated as

$$T_{\mathrm{tun}}(E_x) = \exp\left[-2\int_{x_1}^{x_2} k\left(x, E_x\right) dx\right] \tag{2.111}$$

$$k_{\mathrm{C}}\left(x, E_x\right) = \sqrt{2m_{\mathrm{t,e}}\left(E_x - E_{\mathrm{C}}\right)/\hbar^2} \tag{2.112}$$

$$k_{\mathrm{V}}\left(x, E_x\right) = \sqrt{2m_{\mathrm{t,e}}\left(E_{\mathrm{V}} - E_x\right)/\hbar^2} \tag{2.113}$$

where $m_{\mathrm{t,e}}$ and $m_{\mathrm{t,h}}$ are the tunneling mass of electron and holes respectively, E_{C} and E_{V} are the energies of conduction and valence band edges of the rectangular tunnel oxide barrier. The tunneling mass for SiO_2 $m_{\mathrm{t,e}}$ and $m_{\mathrm{t,h}}$ are $0.3m_0$ and $0.45m_0$ [115], respectively, and for Al_2O_3 $m_{\mathrm{t,e}}$ and $m_{\mathrm{t,h}}$ are $0.3m_0$ and $0.58m_0$ [116]. Then the tunneling current can be calculated according to Tsu-Esaki formula [117]:

$$J_{\mathrm{tun}} = \frac{qm^*}{2\pi^2\hbar^3}\int T_{\mathrm{t}}\left(E_x\right) N\left(E_x\right) dE_x \tag{2.114}$$

where m^* is the effective mass of the parabolic band edges and $N(E_x)$ is the supply function, that depends on the Fermi-Dirac distribution function on each side of the tunneling barrier:

$$J_{\text{tun}} = \frac{qm^*k_{\text{B}}T}{2\pi^2\hbar^3} \int T_{\text{t}}(E_x) \ln\left(\frac{1 + \exp\left[\left(E_{f,1} - E_x\right)/k_{\text{B}}T\right]}{1 + \exp\left[\left(E_{f,2} - E_x\right)/k_{\text{B}}T\right]}\right) dE_x \qquad (2.115)$$

Chapter 3

TiO$_2$ as n-Type Carrier Selective Contact

"If the facts don't fit the theory, change the facts."

Albert Einstein

In this chapter, titanium dioxide (TiO$_2$) will be presented as a carrier selective contact with Si bulk as heterojunction. Atomic layer deposition (ALD) TiO$_2$ experiments were carrier out to investigate the best heterojunction properties to apply in Si solar cell. The design of experiments included thermal ALD TiO$_2$ film growth at different temperatures (80-300 °C), investigation of surface morphology, film thickness (5-20 nm), different passivating tunneling interlayers (SiO$_2$, Al$_2$O$_3$), and annealing conditions on TiO$_2$-Si(p) test structures and devices. It was shown that TiO$_2$ films could provide extremely low SRV approaching 16 cm/s. Excellent surface passivation of c-Si with ALD TiO$_2$ provides opportunities to optimize heterojunction Si solar cells with CSC as either an electron collector or a surface passivation layer. The TCAD simulation model allow to predict the current density-voltage behavior of TiO$_2$-Si devices and explained S-shape diode behavior as well as optimize the experiment. The results presented in this chapter were recently published in Japanese Journal of Applied Physics [118] in collaboration with SASTRA University and Freiberg Instruments GmbH.

3.1   Introduction: TiO$_2$-Si heterojunction and its band alignment

Titanium oxide (TiO$_2$) is already widely used in PV industry as AR coating [119]. However it further applications were limited by thin film deposition technology until chemical vapor deposition (CVD) techniques, particularly ALD [120], were applied. ALD technology is based on self-limiting growth process, that allows to obtain high film thickness precision, uniformity and conformity, homogeneity, pin-hole free and in general excellent crystal properties of ultra-thin TiO$_2$ films [121]. As consequence, TiO$_2$ became an interesting candidate as carrier selective contact with its wide energy bandgap and almost perfect match of conduction band with Si. As a n-type electron-selective contact in Si heterojunction (SHJ) solar cells technology, TiO$_2$ has already proved to be an excellent carrier selective contacts [58–61, 109, 122–128].

TiO$_2$ has a 3.2 eV bandgap energy with a small conduction band offset to silicon (ΔE$_c$=0.05 eV), which allows the electron to pass from the silicon conduction band through a TiO$_2$ layer via the conduction band; in addition, it has a large valence band offset (above ΔE_v=2 eV), which blocks hole transport through the TiO$_2$ layer [129, 130] as shown in Fig. 3.1 and compiled according to data in Tab.   5.2. A single SHJ cell with a TiO$_2$ backside hole blocking
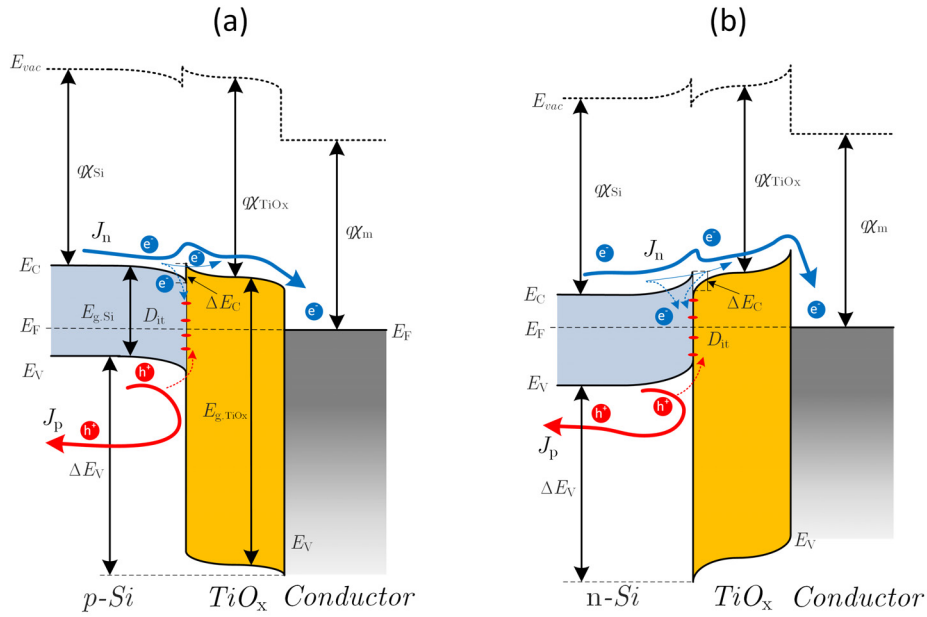
FIGURE 3.1: Anderson energy band diagram of TiO$_2$-Si heterojunction: (a) n-p structure, (b) n-n structure

layer achieved an efficiency of 21.6 % [61]. In addition, TiO$_2$ has also shown excellent passivation properties on c-Si surfaces [78, 131–136]. The best TiO$_2$ passivation films are ALD grown at low-temperatures in the range of 80-150 °C and annealed at 200-250 °C. ALD TiO$_2$ is highly compatible with the simultaneous deposition of Al$_2$O$_3$ in the same deposition system [132, 137]. Both films, TiO$_2$ and Al$_2$O$_3$, are fixed negative charge materials with ideal optical properties (low optical absorption in the visible range and refractive indexes of 2.4 and 1.65, respectively).
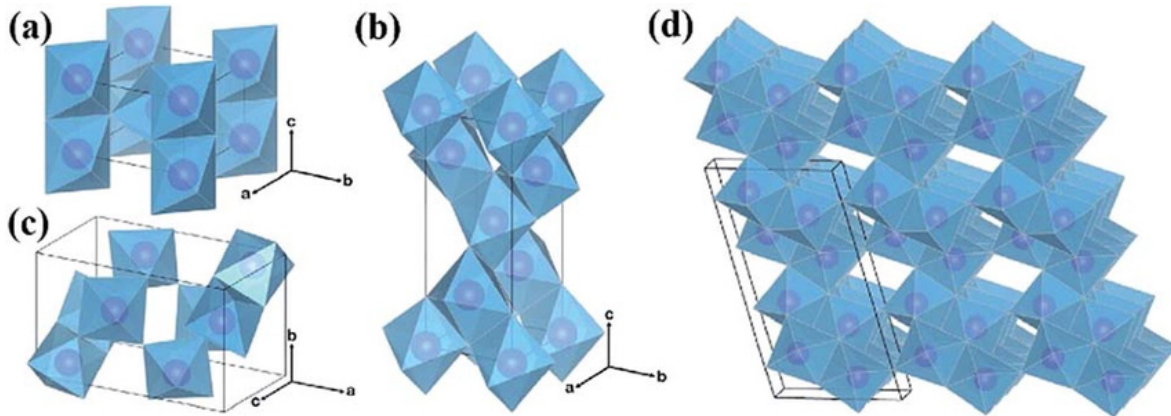
FIGURE 3.2: Schematic crystal structure of the TiO$_2$ polymorphs: rutile (a), anatase (b), brookite (c) and TiO$_2$ (d). Purple spheres represent Ti atoms, and the blue octahedra represent TiO 6 blocks. Oxygen atoms at the corner of the octahedra are omitted for clarity [138]

TiO$_2$ has high electric resistivity, but as ultra-thin film it has excellent transverse electric conductivity [139], mechanical [140], chemical stability and optical high refractive index (up to 2.70-2.71 at a wavelength of 600 nm) with excellent transmittance in the visible range [141]. TiO$_2$ possesses complex material properties: it has four crystal phases (amorphous, anatase, rutile and brookite shown in Fig. 3.2).

Each of this crystal phases has different, optical, electrical and chemical properties. Nevertheless, this study was only limited to amorphous and anatase phases of TiO$_2$ due to their low-temperature growth and processing conditions and simplicity to apply in the fabrication of solar cell devices. Other phases, rutile and brookite, require high-temperature growth or annealing conditions (above 450 $^{\circ}$C). Brookite phase is also highly unstable. Therefore, rutile and brookite titania films are not be discussed in this work.

On other hand, TiO$_2$ thin films are not fully investigated with respect to optimization for the best passivation properties and effect of interface defects on diode properties. In this work, TiO$_2$ study is presented on ALD TiO$_2$ applications as carrier selective contacts in Si solar cell.

3.2 TiO$_2$-Si devices fabrication

3.2.1 ALD process

ALD technology was developed and patented back to 1970's by Suntola and co-workers in Finland [142]. The purpose was to develop thin film coating in electroluminescent displays. As an alternative to conventional methods, ALD offered the capability to produce high-quality, dense and pinhole-free films with excellent uniformity and conformality with great thickness and composition control at an atomic level.

The extensive review of ALD processes and applications are well described by Puurunen and many other experts in the field [121, 143, 144]. The ALD process consists of the sequence of precursor reactant gas purge and evacuation steps of gases. Each precursor gas purge pulses are separated by inert gas purging or evacuation of the reaction chamber (Fig. 3.3 (b)) to maintain separate half-reaction for each precursor. Such half-reaction makes one cycle that creates on a monolayer of desired materials. To grow certain thickness, growth process should be repeated by a number of cycles determined by deposition rate per cycle. The ALD principle diagram is depicted in Fig. 3.3 (a), where the process consists of two precursors purged separately with inert gas purging impulses.

The first step, the ALD process chamber is stabilized at a required temperate in order to maintain stable, acceptable deposition window. Next, the chamber is flushed several time to remove any contaminating gases and particles. A chemical process starts with exposure of a substrate surface to the pulse of the first precursor and its chemisorption on the available surface sites ($^-$OH groups) until the surface saturated with the precursor radicals. Saturation of chemisorption leads to self-limited reaction allowing to grow the film with stable monolayer thickness at a certain temperature. After inert gas purging, the excess precursor and reaction by-products are removed from the chamber. Second, half-reaction starts with the surface exposed to the second precursor with similar saturation effect leading to self-limited second half-reaction. Finally, after the full cycle, the chamber is purged with inert gas to remove remaining second precursor and by-products. Important to note, that a process containing only one precursor alone is not qualified as ALD. The total growth process consists of n-cycles and is relatively slow due to the purging periods. The temperature range with a constant deposition rate is known as an acceptable window as shown in Fig. 3.3 (c) [145, 146]. The ALD acceptable window is a recommended deposition regime, but it is not strictly required. More important success factor in ALD process is a proper precursor chemistry match, e.g. fast and complete surface reactions. Ritala et al. [144] summarized some features that could lead to a reliable ALD process. A self-limiting growth process gives:
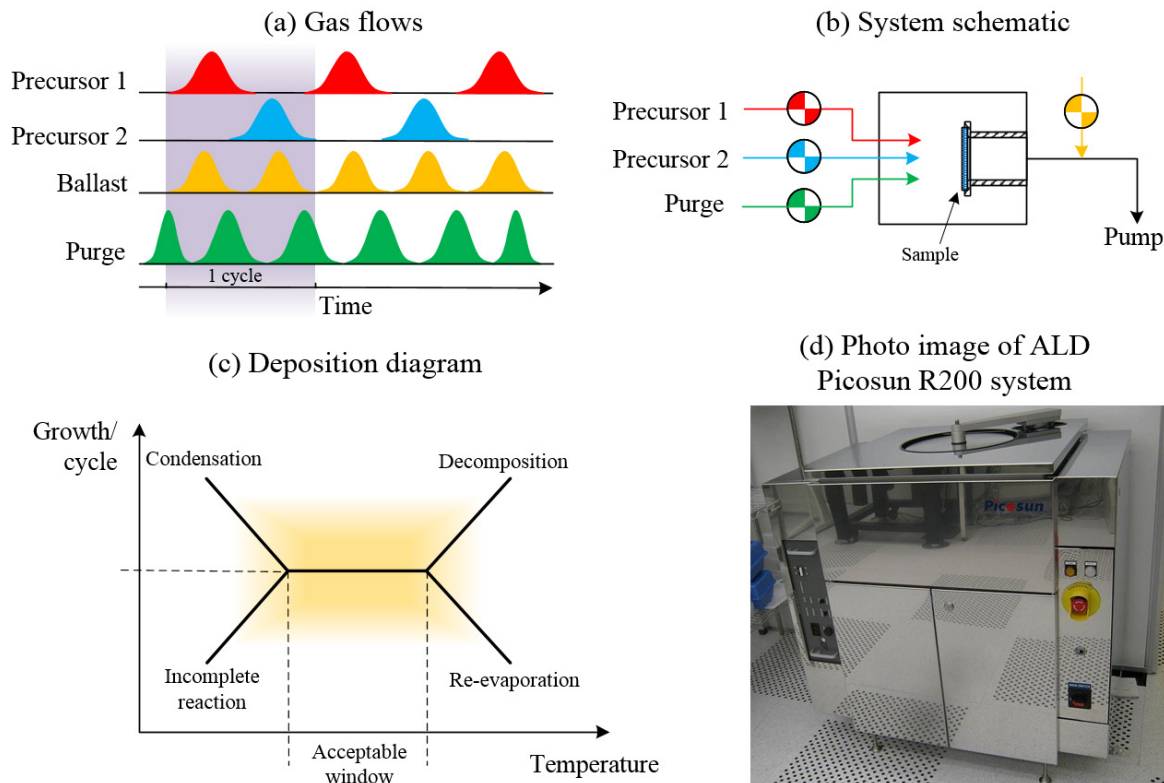
FIGURE 3.3: ALD process fundamentals: (a) precursor purge and timely reaction scheme, (b) system schematics of ALD process chamber, (c) deposition diagram depicting process acceptable window in temperature regime, (d) photoimage of ALD system of Picosun model R200

- precise film thickness control by the number deposition cycles

- no need to control reactant flux

- excellent uniformity and conformality

- capability to process large-area samples and batches

- dense, homogeneous and pin-hole free films

- atomic layer composition control

- excellent reproducibility and high-quality film

- wide range of operating temperatures (from root temperature up to 400 $^\circ$C and higher)

3.2.2   ALD growth of TiO$_2$

ALD Titanium dioxide (TiO$_2$) process is well described in many publications [147–152]. In this study, TiO$_2$ films were deposited onto both sides of c-Si wafers by thermal ALD (Picosun R200) [1]. Undiffused double-side-polished CZ wafers [100 mm diameter, (100) orientation, 5 Ωcm resistivity, and 350 μm thickness] were used as substrates. Before any processing, all wafers from the box received standard buffered HF etch for 30 s to remove the native oxide, followed by DI water rinsing and drying. For chemical SiO$_2$ layer growth, HNO$_3$ acid was

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[1]ALD Picosun R200 http://www.picosun.com/en/home/

used as oxidizer, heated to 95 °C in a glass beaker to oxidize the wafers for 10 min. The final 1.38 nm thickness of the SiO_2 layers was measured by ellipsometry with fitting Tauc-Lorentz model. For Al_2O_3 interlayer growth, the same ALD Picosun R200 system was used. Al_2O_3 film was synthesized from a trimethylaluminum (TMA) precursor and H_2O oxidant in 10 cycles at 200 °C, which resulted in 1 nm thickness according to ellipsometry measurements. After all preparations, three groups of wafers samples were defined: bare hydrogenated Si (from bHF etch), and interlayers SiO_2– and Al_2O_3–coated Si wafers (Figs. 3.4-3.5).
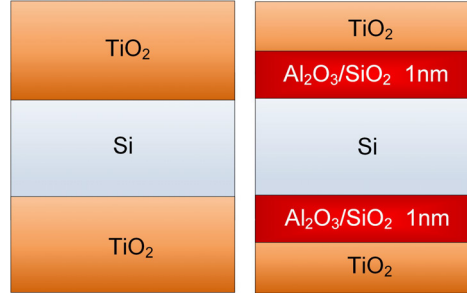
FIGURE 3.4: Schematic of ALD TiO_2 surface passivation with Al_2O_3 or SiO_2 interlayers and with hydrogenated surfaces on c-Si wafers
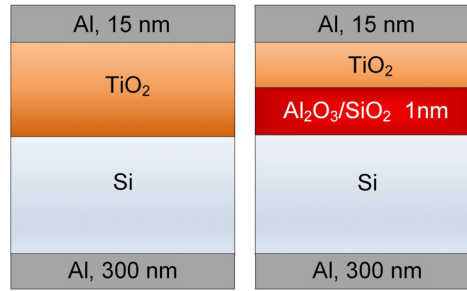
FIGURE 3.5: Schematic illustration of three types of TiO_2-film-based diode devices

TiO_2 films were synthesized on all wafers using a $TiCl_4$ precursor and DI H_2O as the oxidant and presented as a diagram in Fig. 3.6. The ALD TiO_2 process is based on the following chemical reaction, which occurs in cycles after each precursor was dosed into the chamber. In reality, this reaction is accomplished by divided binary reactions into separate half-reactions (step (2) in Fig. 3.6):

$$TiOH^* + TiCl_4 \rightarrow TiOTi\,(Cl)_3 + HCl \uparrow \qquad (3.1)$$
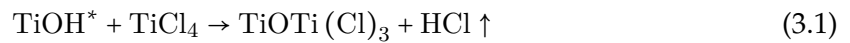
After the first half-reaction is finished, the surface is passivated by $TiCl^*$ groups (step (3) in Fig. 3.6). Next, the purge step (4) removes the excess of $TiCl_4$ and hydrogen chloride (byproduct), the next reaction step (5) is

$$TiCl^* + H_2O \rightarrow TiOH^* + HCl \uparrow \qquad (3.2)$$

Here, H_2O reacts with $TiCl^*$ groups, while HCl leave the chamber and TiO_2 is synthesized. The overall sequence is repeated until the film with required thickness is grown. The net reaction, therefore, is:

$$TiCl_4 + 2H_2O \longrightarrow TiO_2 + 4HCl \qquad (3.3)$$
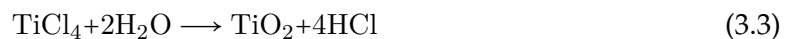
TABLE 3.1: ALD TiO$_2$ process parameters

Precursor	Pulse time, s	N2 flow, sccm	N2 purge time, s
TiCl$_4$	0.1	150	0.5
TiCl$_4$	0.1	150	20
H$_2$O	0.1	200	0.5
H$_2$O	0.1	200	20

Each surface reaction is self-limited and the deposition recipe is shown in Table 3.1.
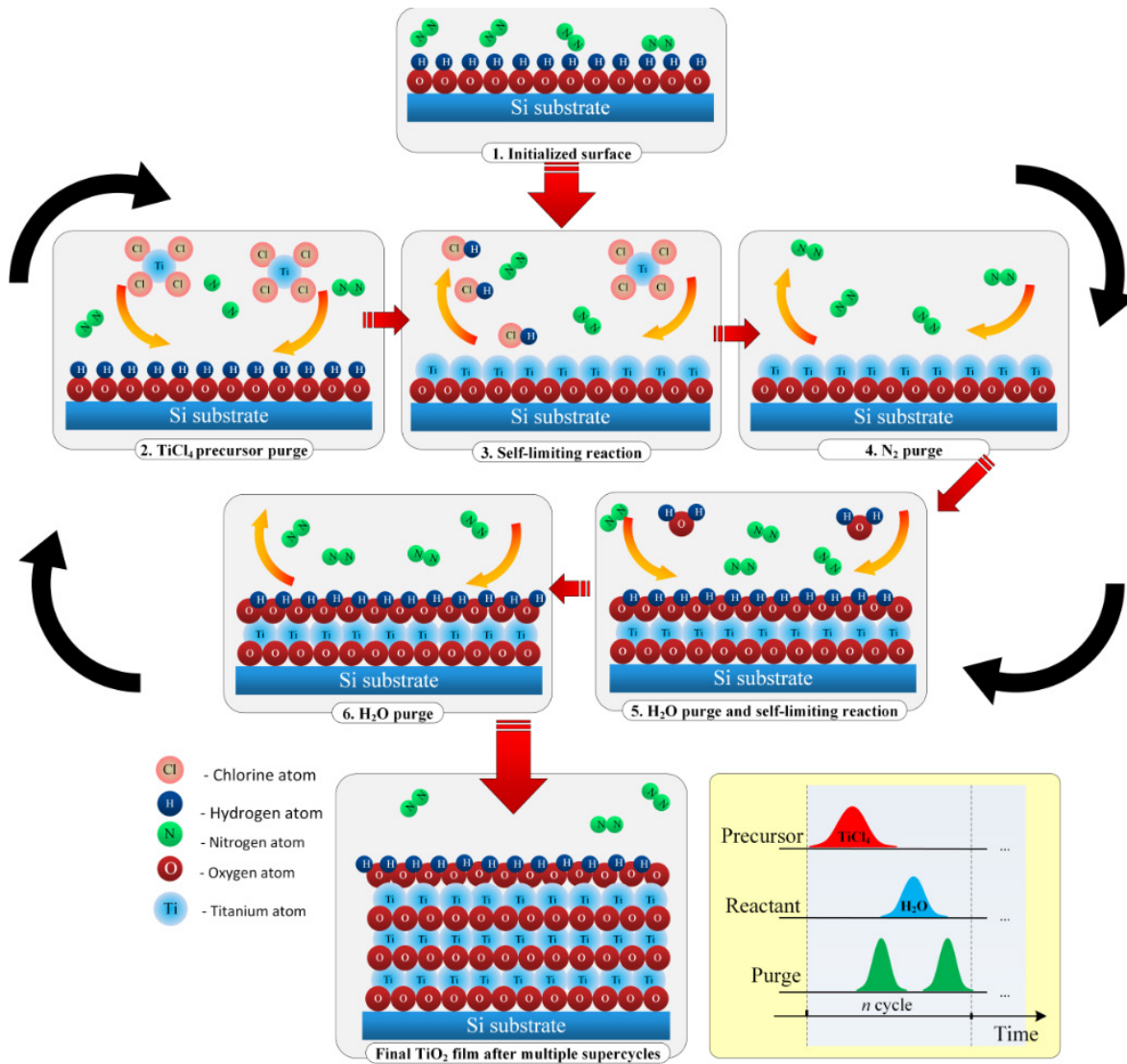
FIGURE 3.6: Schematic representation of the ALD TiO$_2$ deposition process.
Yellow inlet represented time dependent chemical process sequence

The inlet and by-product are in the gas phase, and the rate of chemical reaction is slightly temperature dependent (Fig. 3.7). The full ALD process is described elsewhere [73, 153–155]. The first experiment included ALD TiO$_2$ with a constant thickness of 20 nm on the wafers with interlayers. It was found that the deposition rate was a function of ALD growth temperature, as shown in Fig. 3.7. Moreover, the TiO$_2$ growth rate remained stable at all temperatures, according to our observation and other reports [153].
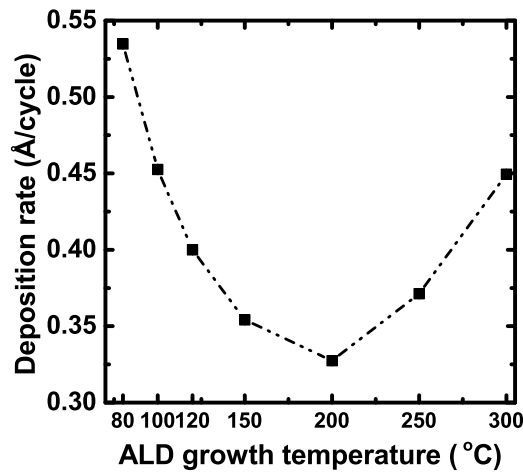
FIGURE 3.7: ALD TiO₂ deposition rate as a function of ALD temperature

Before ALD TiO₂ deposition, TiO₂-Si diode devices had 300 nm of Al (electron beam deposited) on the full backside of the samples. After ALD TiO₂ deposition, 15 nm of semi-transparent Al film was deposited as shown in Fig. 3.5. Top Al contact was formed with either electron beam or thermal evaporation of Al through a shadow mask with a circular shape of 8 mm diameter. Initially, the electron beam technique was used for Al deposition; however, to reduce radiation damage to the thin TiO₂ film, Al was later deposited by thermal evaporation.

The thicknesses and optical properties of the TiO₂, SiO₂, and Al₂O₃ layers were measured by spectroscopic ellipsometry (J.A. Woollam VASE) at 5-10 different spots on the samples. The TiO₂ layers discussed in the manuscript were found to be 5-20 nm thick with a standard deviation of less than 5 % across each wafer. The refractive index of the deposited films was usually around 2.2-2.7 at a wavelength of 632.8 nm. The TiO₂ film with thickness below 25 nm had close to 100 % transmittance on a silicon wafer and around 92 % on a fused silica substrate and limited only by transmittance of the the base material (Fig. 3.8, (a)). The TiO₂ films grown or annealed at different temperatures had different crystalline phases, i.e., amorphous, anatase, etc. The bandgap energy was calculated from measured values of absorption coefficient and corresponded to 3.25 eV for amorphous (80, 100, 120 °C and 3.4 eV for anatase phase samples (150 and 200 °C) (Fig. 3.8, (b-c)). X-ray photoelectron spectroscopy (XPS Thermo Fisher Scientific K_α) was used to determine the surface composition of the TiO₂. XPS measurements were performed at an angle of 20° with the base pressure of 10^{-9} mbar with a monochromated microfocused Al K_α radiation source. The crystal phase of TiO₂ films was studied by Raman spectroscopy using a DXR Raman Microscope excited with a DXR 455 nm laser having a DXR 455 nm filter.

The surface morphology of deposited samples was investigated by scanning electron microscopy (SEM) (Zeiss SEM Supra 40 instrument) and atomic force microscopy (AFM) using Bruker AFM Dimension Icon. The roughness of the samples was also investigated by AFM. Recombination properties were studied by the microwave detected photoconductivity (MDP) method on the MDPmap from Freiberg Instruments. The illuminated current density–voltage ($J - V$) characteristics of the fabricated heterojunction TiO₂-Si solar cell were measured with Newport 1 sun (AM1.5G) illumination and a Keithley 2400 sourcemeter; dark $J - V$ measurements were carried out using a Keysight B1500A semiconductor device analyzer.
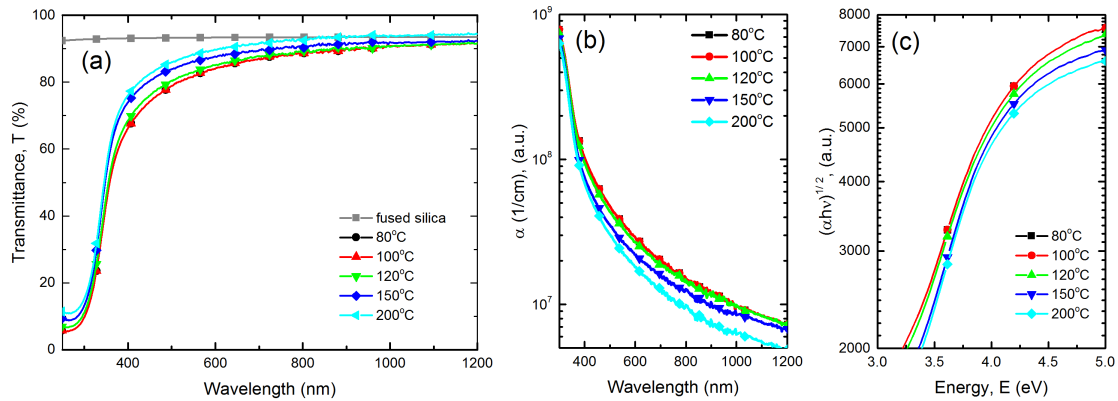
FIGURE 3.8: The variation of spectral transmittance of ALD TiO$_2$ 20 nm thick films grown at different temperatures

3.2.3 Influence of ALD deposition temperature on growth kinetics of TiO$_2$ films and their properties

In order to establish the effect of the deposition temperature on the passivation and diode properties of TiO$_2$ films on Si, different characterization techniques and methods were performed on the samples grown at 75-80, 100, 120, 150, 200, 250, and 300 °C. In order to understand the effect of crystal grains and there morphology, top-view SEM and AFM imaging were employed in Fig. 3.9 and Fig. 3.10, correspondingly.
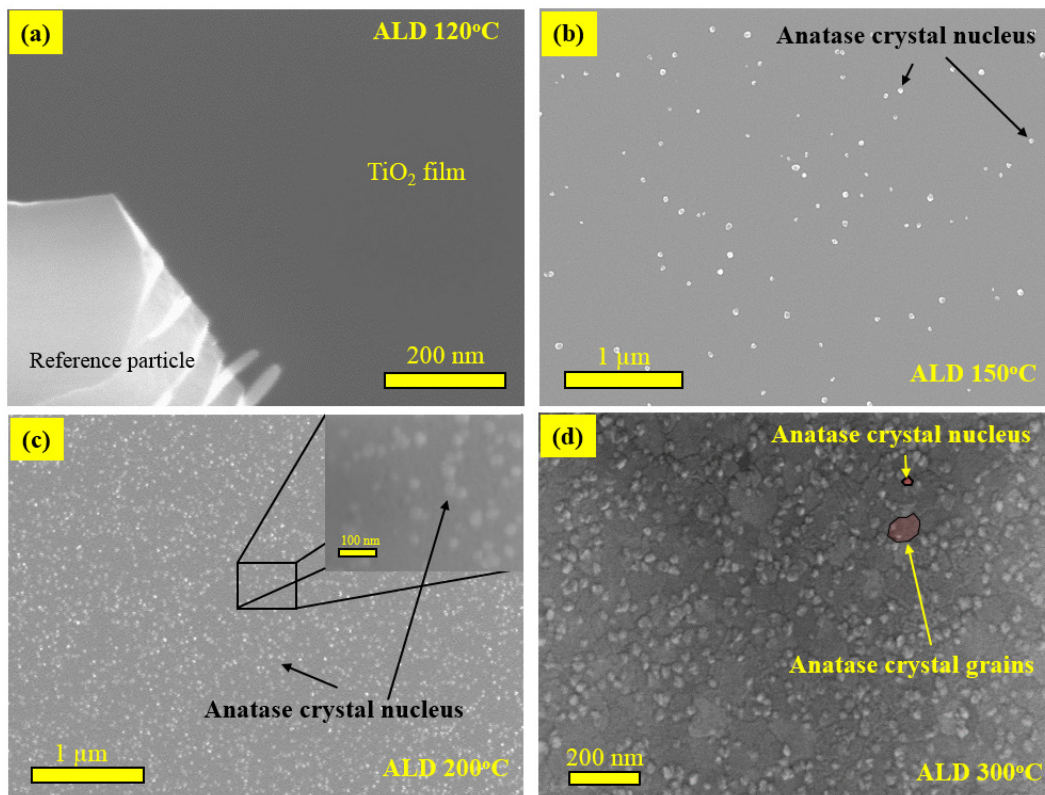
FIGURE 3.9: SEM images of selected TiO2 films grown at 120 °C, 150 °C, 200 °C, and 300 °C

In Fig. 3.9 top-view SEM images of the samples deposited at 120, 150, 200 and 300 °C are shown.

Difficulties to focus with SEM (Fig. 3.9) for samples grown below 120 °C were noticed owing to continuous amorphous TiO$_2$ films and the absence of any grain structure. Thus, for the as-grown TiO$_2$ films grown at ALD temperature above 150 °C SEM images confirm the presence of anatase nuclei (Figs. 3.9 (b) and (c)). At 150 °C, the anatase nuclei have a random nature, while at 200 °C, they have a high density. In this regime, the amorphous phase is dominant over the anatase phase. All the TiO$_2$ films contained small embedded crystal nucleus which appeared as bright dots on Fig. 3.9 (b). The higher crystal brightness was observed in the SEM images owing to additional surface roughness that enhance secondary electron yield from these nucleus. At the higher growth temperatures above 200 °C crystal grains were fully formed and shown as a very large grains in the order of hundreds of nm in Fig. 3.9 (c-d). At the same time AFM scan images confirmed presence and dimensions of the crystal nucleus and grains as shown in Fig. Fig. 3.10 (a-h).

Full analysis of AFM scan measurements were conducted with extraction of the arithmetical mean height S_a, root mean square height S_q, maximum height S_z, maximum pit height S_v, and maximum peak height S_p and shown in Fig. 3.11. In fact, from AFM scans it was deduced that the crystal nucleus and crystallites protruded up 30 nm at 200 °C and according to Fig. 3.11. Since the AFM scanning was conducted on the films with thickness 30 nm, it suggests an enhancement of deposition rate at least 50 % on the crystal grain surfaces. This tendency is easily observed from Fig. 3.11 for samples grown above 150 °C.

To understand and identify crystal phase modification, Raman measurements were conducted on all the samples grown at 80, 100, 120, 150, 200, 250, and 300 °C. In each temperature regime, different TiO$_2$ films are formed with amorphous, anatase, and combined amorphous-anatase phases. In region I (80-120 °C), amorphous TiO$_2$ formation was confirmed with Raman spectra measurements and corresponded to the report by Niilisk et al. [156].

Raman measurement confirmed anatase TiO$_2$ peaks at 141, 396, 525, and 640 cm^{-1} only for samples grown above at 250 °C (Fig. 3.12). It means that these samples have continuous anatase crystalline phase films, while samples grown at 150 and 200 °C most probably were measured on amorphous phase film part.

Only XPS measurements of the TiO$_2$ film grown at 120 and 300 °C are presented, owing to the small difference in the element content observed at other temperatures. All the XPS spectra confirm the presence of TiO$_2$ films with Ti^{4+} valence. For samples grown at 120 °C, Cl peaks were detected at 202 and 270 eV. 202 eV peak corresponds to Cl 2p$_{3/2}$ to Ti or TiCl$_4$. These peaks are probably caused by the remaining Cl reaction byproducts (maybe TiCl$_x$O$_y$) due to incomplete ALD chemical reaction (Fig. 3.13). Only XPS measurements of the TiO$_2$ film grown at 120 and 300 °C are presented, owing to the small difference in the element content observed at other temperatures. According to Fig. 3.13(c), several Ti peaks were detected that corresponded to different bonds in the material. The Ti 2p3/2 peak with the range of 458.6 – 459.2 eV for Ti$_{4+}$ and TiO2 molecular. Slight overlap in the ranges 454.9 – 455.2 eV particularly for 300 °C in depth corresponds to the Ti$_{2+}$, Ti0 molecule and Ti 2p3/2 peaks within 453.7 – 454.2 eV range. [157, 158] The most intensive peak was Ti 2p3/2 peak located at 459.7 eV that corresponded to Ti$_{4+}$ bonded in TiO$_2$ or TiSi$_2$. At 465.3 additional peak appeared for all samples and corresponded to the Ti 2p1/2 peak. This peaks also implied a spin-orbit splitting of 5.6 eV and corresponded to the Ti$_{4+}$ and a bond with O and Si. In summary, the XPS spectra confirms the presence of Ti$_{4+}$ species bonded in TiO$_2$
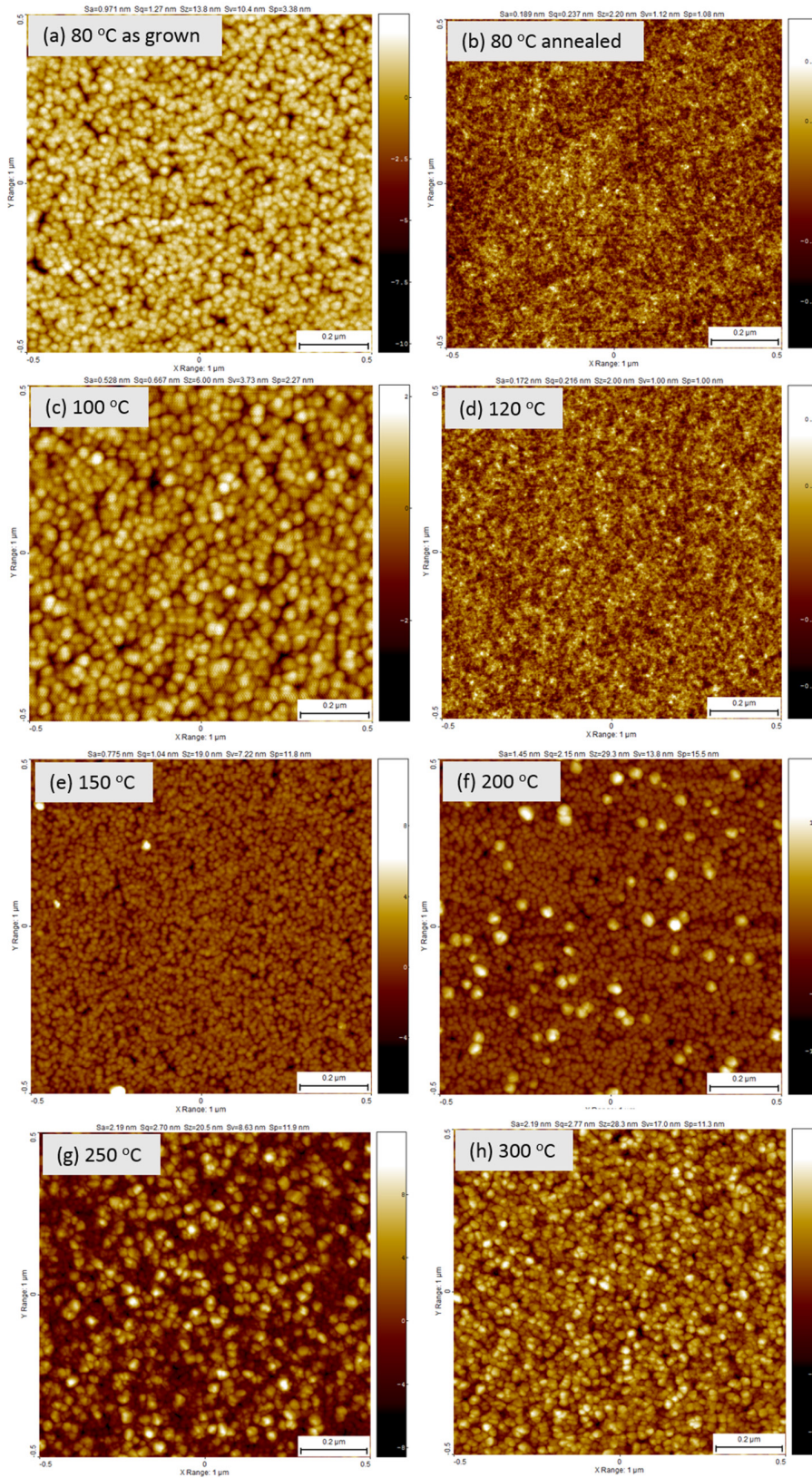
FIGURE 3.10: AFM scan images of TiO₂ films grown on a Si wafer in the 80-
300 °C temperature range (All the samples except image (b) were scanned as
grown films). Scale bar is 200 nm, scanning area is 1×1 μm
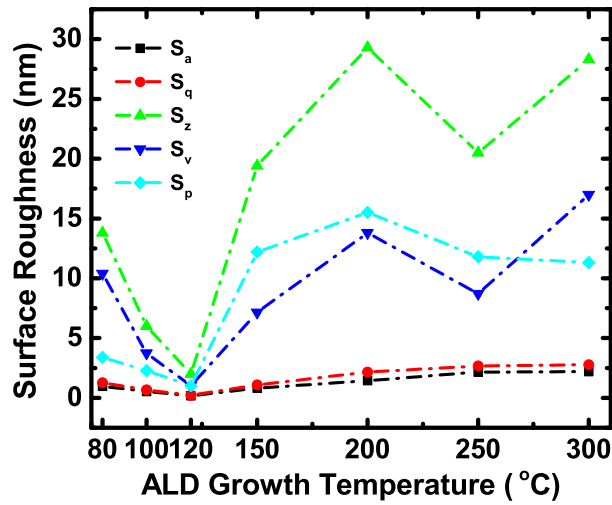
FIGURE 3.11: Surface roughness dependence calculated from AFM images for TiO₂ films grown at different temperatures
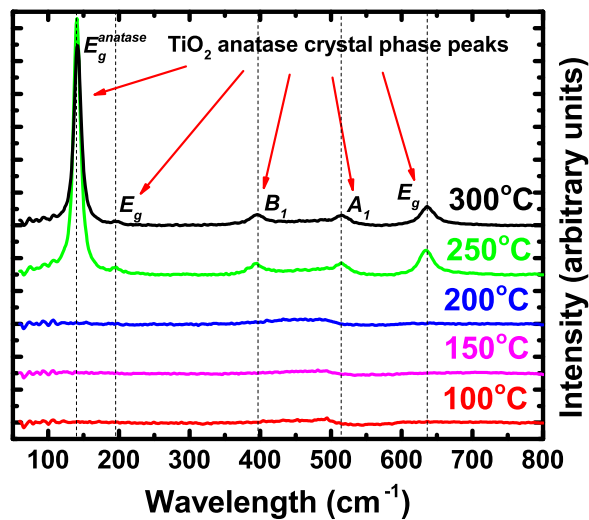
FIGURE 3.12: Raman spectra of ALD TiO₂ films on glass substrates

molecules with some traces of TiOSix complex and Cl. Fig. 3.13(c) confirmed presence of Cl only in samples grown at 120 °C.

Interestingly, that Macco et al.[159] observed similar nucleation tendency for ALD grown ITO films in a similar temperature regime. Macco et al. even proposed a model that describes the crystallization process for ITO ALD process. Here, the Macco model was adopted for TiO₂ films and presented in Fig. 3.11.

This model describes the crystallization process of the ALD TiO₂ films. The schematic view of the model is shown in Fig. 3.14. During the ALD process, the process temperature plays a major role in crystal nucleation and film growth. At lower temperature (80-120), an amorphous incubation layer develops (A.1). At higher process temperatures (150-200), crystal nucleus start to form in a random order with increased growth rate on crystal nucleus and
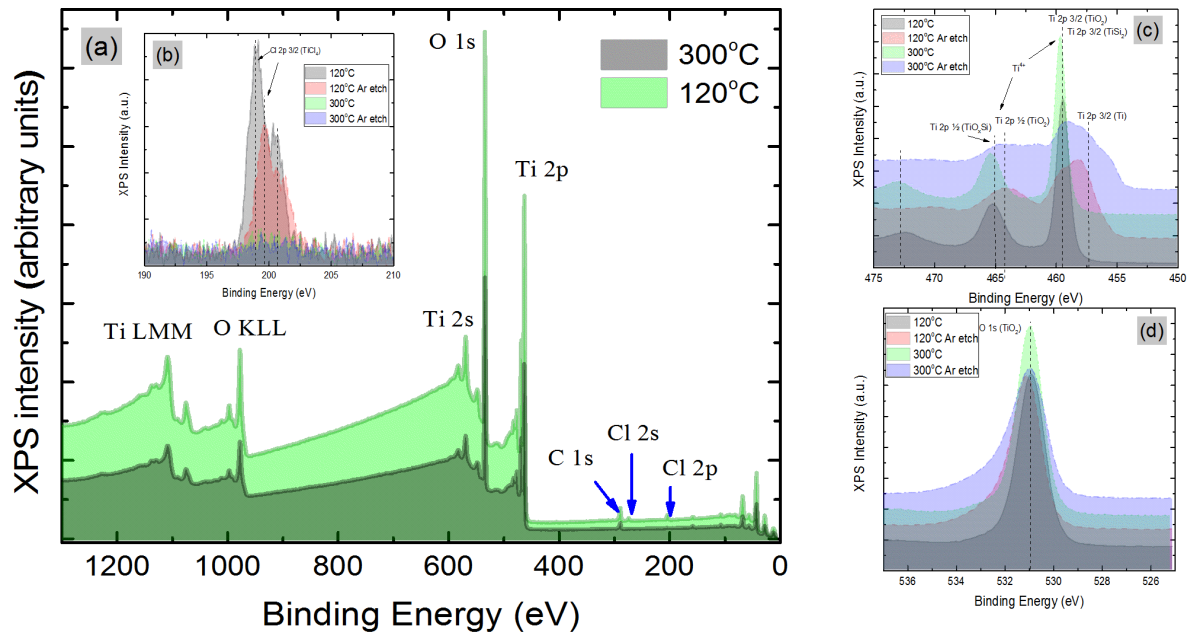
FIGURE 3.13: XPS spectra of ALD TiO$_2$ films grown at 120 and 300 °C: (a) XPS survey with all the spectra peaks, (b) Cl 2p peak, (c) Ti peaks, (d) O 1s peaks
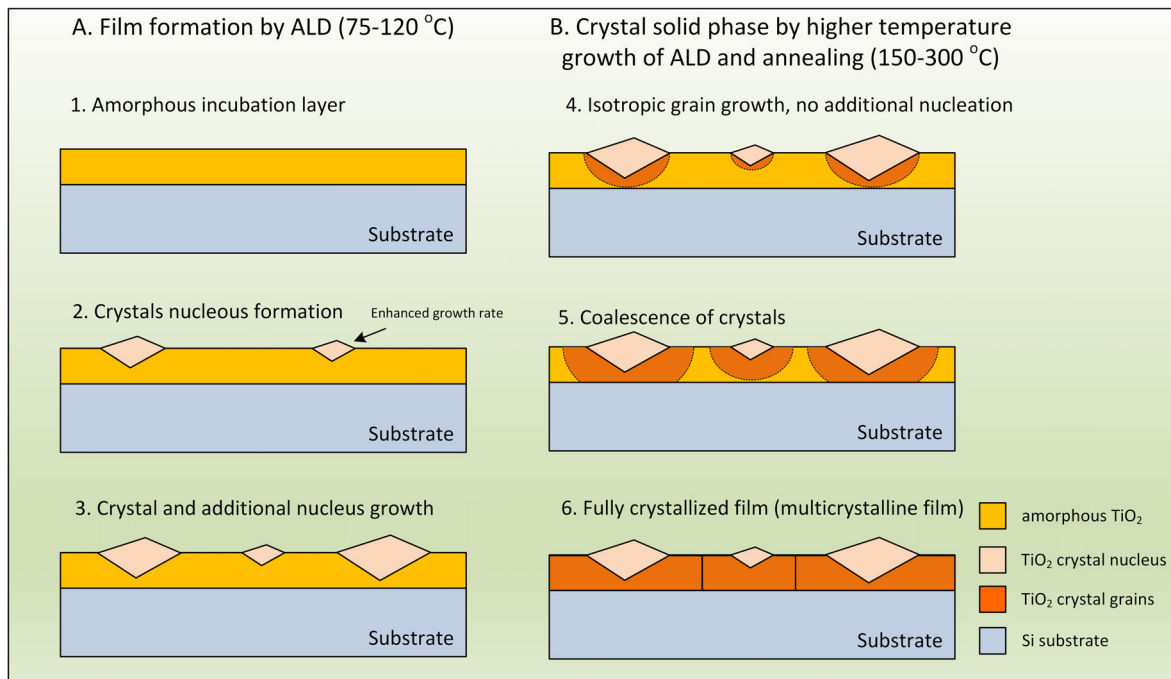
FIGURE 3.14: Schematic of the nucleation and crystal growth model for ALD TiO$_2$ (A) during ALD film formation at lower temperature (75-120 °C) and (B) during solid phase ALD and annealing (150-300°C). Adopted from ITO model presented by Macco et al. [159]

elevation above the amorphous film. At even higher ALD process temperatures or annealing solid phase crystallization occurs with isotropic growth of the crystal nucleus into large

grains without the formation of new nucleus according to a top-view SEM, respectively (B.1). The grain growth proceeds until the nuclei coalesce (B.2.) and until the TiO₂ film is fully crystallized (B.3).

3.2.4 Passivation properties of TiO₂ films on hydrogenated Si surface: Effect of ALD growth temperature

The effective carrier lifetime (τ_{eff}) of each sample was determined by MDP measurements under steady-state conditions. The measurements were performed as either injection dependent at a single point in the middle of the samples or spatial dependent as a map with a 500 μm resolution and at an injection level of 10^{15} cm^{-3}. All measurements were conducted with a laser excitation using the following parameters: 980 nm, pulse/pause duration: 500-8000 μs, laser power: 10-50 mW. To evaluate and interpret the experimental data, the bulk recombination model of Richter et al.[154] and the surface recombination model simplified by Olibet et al.[155] were used. The final model is summarized in the Sect. 2.3-2.3.6.
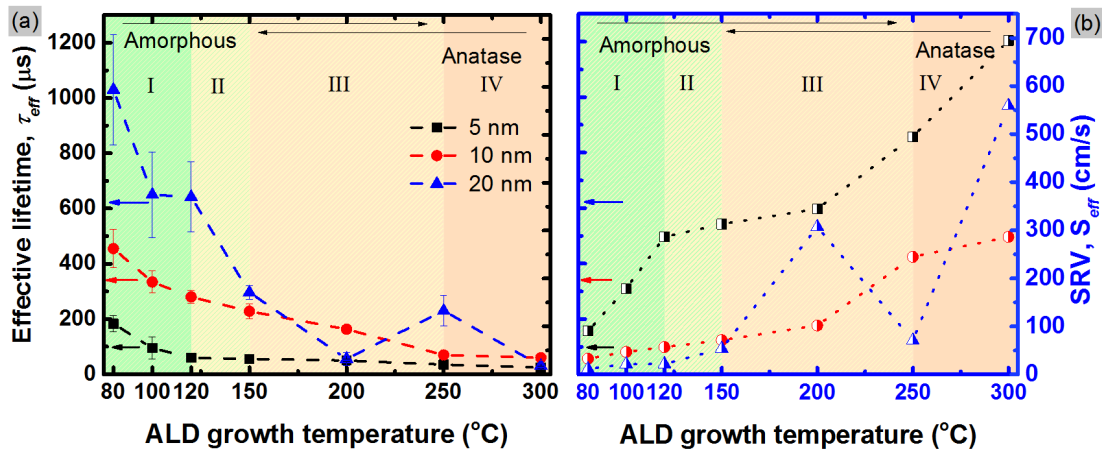
FIGURE 3.15: Carrier lifetime @ 10^{15} cm^{-3} (a) and surface recombination velocity (b) as functions of ALD temperature for 5-, 10-, and 20 -nm TiO₂ films on p-type c-Si samples. [Note: the legend color and shapes are valid for both graphs]

Figure 3.15 shows the single point effective lifetimes (τ_{eff}) at the 10^{15} cm^{-3} injection level of p-type silicon wafers passivated by 5, 10, and 20 nm TiO₂ films grown at different ALD temperatures. The calculated upper limit of effective SRV (S_{eff}) is also shown in Fig. 3.15. Figure 3.15 shows that the passivation properties are dependent on the ALD deposition temperature and, as a consequence, on the crystal phase of TiO₂ films. Let us define four regions from I to IV as indicated in Fig. 3.15 (a).

In region I, the effective lifetime has the highest values of $\approx$ 450 μs and the lowest SRV of $\approx$ 33 cm/s. In regions II-IV, the effective lifetime decreases and SRV increases. Owing to a higher SRV (above 100 cm/s), the calculation model for samples grown above 250 °C was optimized. The results demonstrate that the passivation quality of TiO₂ films depends on the deposition temperature. AFM and SEM measurements showed smooth films in region I as shown in Fig. 3.11 and AFM images in Fig. 3.10 (a-h).

In region II (150-200 °C), the effective lifetime decreases to the order of 150-250 μs and SRV increases to 70-100 cm/s, while for 5 nm TiO₂ film samples, the lifetime drops to 10-30 μs,

and for 20 nm TiO$_2$, from 200 to 10 μs (Fig. 3.15). In this region, AFM images (Fig. 3.11 and Fig. 3.10 (i-h)) show increased surface roughness caused by random anatase TiO$_2$ nucleation according to Figs. 3.9.

In region III (200-250 $^\circ$C), the effective lifetime for all TiO$_2$ thicknesses remains low (10-30 μs) owing to the low passivation quality caused by dominant anatase grain formation according to SEM (Figs. 3.9), AFM (Fig. 3.10) scan images and Raman peaks at at 141, 396, 525, and 640 cm^{-1} for samples grown at 250 $^\circ$C. Anatase crystals have a random nature and create dense interface defects at the silicon surface. Dense anatase crystals were detected by SEM images and Raman measurement and confirmed with appropriate anatase TiO$_2$ peaks at 141, 396, 525, and 640 cm^{-1} for samples grown at 250 $^\circ$C (Fig. 3.12).

In the last region IV (250-300 $^\circ$C), the TiO$_2$ films are fully anatase phase with coalesced crystal grains according to AFM and SEM (Fig. 3.10(g-h), Fig. 3.9(d) and Raman spectra (Fig. 3.12). Such surface morphology causes further deterioration of passivation properties and effective lifetime degradation.

3.2.5   Diode properties of TiO$_2$-Si devices

First, TiO$_2$-Si devices only without any interlayers were fabricated. The design of experiments for the TiO$_2$-Si device relied on the definition of the best passivation conditions and the definition of the best diode parameters. On the basis of the reference analysis, it was found that several reports stated that 5-10 nm TiO$_2$ films exhibited the best diode properties [126, 128, 160]. Therefore, the initial experiments with 10-nm-thick, and later, with 5-nm-thick TiO$_2$ films. were conducted. Devices with 10-nm-thick TiO$_2$ films have shown promising diode properties and are presented in the following subsection and Fig. 3.16.

On the other hand, devices with 5-nm-thick TiO$_2$ films had S-shaped $J - V$ behavior. As a consequence, additional theoretical and simulation studies were performed and and compared with experimental data to understand the nature of such behavior and to identify the cause of the irregular behavior. For the ALD temperature effect on TiO$_2$-Si heterojunction diodes, only a 10-nm-thick TiO$_2$ film were grown at 80-300 $^\circ$C on p- and n-type Si wafers. Next, Al 15 nm thick contacts of 8mm diameter circular shape were deposited by electron beam technique. In Figures 3.16 (a) and (b), the $J - V$ curves of TiO$_2$-Si(p) and TiO$_2$-Si(n) devices are shown, respectively. It could be concluded that TiO$_2$-Si(p) devices show rectifying behavior and therefore have hole-blocking properties. The expected open circuit voltage V_{OC} and the series resistance R_S from Fig. 3.16 (b) and the values are shown in Fig. 3.16 (d). A dependence of V_{OC} and R_S on TiO$_2$ growth temperature was found as a consequence of TiO$_2$ crystal phase and morphology changes. Relying on the previous analysis in this manuscript, it can be concluded that the highest V_{OC} is due to continuous amorphous films.

A higher ALD temperature (above 150 $^\circ$C) causes anatase phase transformation and therefore reduction in R_S. The V_{OC} drops at higher temperatures owing to the morphology of TiO$_2$ films, which changes significantly with ALD growth temperature and as confirmed in Figs. 3.10, 3.13 and 3.12. According to Fig. 3.16 (b), TiO$_2$-Si(n) devices show almost perfect resistive behavior, which proves electron transport in the conduction band. Some nonlinear $J - V$ behavior is observed for samples grown above 200 $^\circ$C, probably due to the effect of the anatase TiO$_2$ films on devices. This effect needs further investigation.
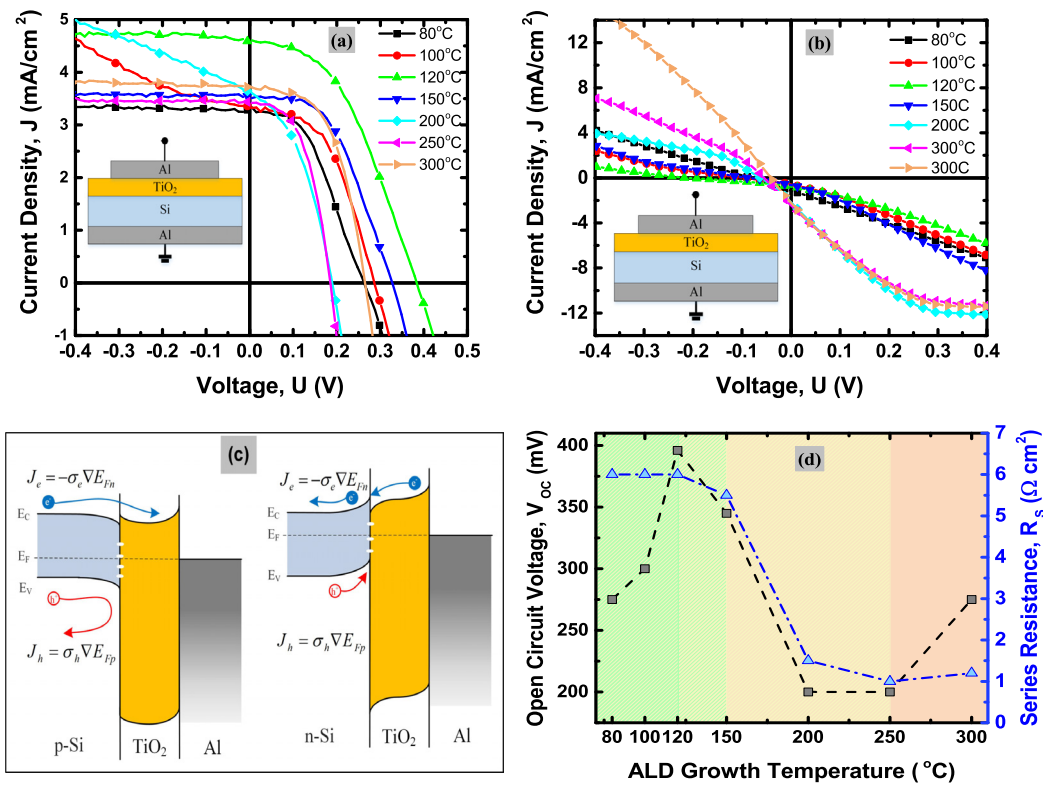
FIGURE 3.16: Illuminated $J - V$ characteristics of (a) TiO2-Si(p) and (b) TiO2-Si(n) devices; (c) illustration of energy band diagram of TiO2-Si(p) and TiO2-Si(n); (d) V_{OC} and R_S dependencies on ALD growth temperature for TiO2-Si(p) devices

TCAD simulation and experiment comparison for 5 nm TiO₂ devices

Simulation (details in the next paragraph) predicts that the TiO₂ film with a low carrier density exhibits an S-shaped $J - V$ curve. Experimentally, the reduction in carrier density inside the TiO₂ film could be due to damage during aluminum deposition, which creates additional trap states significantly reducing the carrier density. To understand the degradation mechanism for the diode devices, TiO₂-Si devices were fabricated. Al contacts were deposited with the commonly used e-beam evaporation and later replaced it with the thermal evaporation technique. Such replacement allowed us to fabricate more reliable and promising devices with 5 nm TiO₂. The experimental data and simulation results for both e-beam and thermally evaporated Al are shown in Fig. 3.17 (a) and explained in the this subsections.

A possible effect on J-V S-shape behaviour of TiO₂-Si heterojunction devices could be due to metal induced gap states (MIGS). Dedicated discussion on effect of MIGS on TiO₂-Si heterojunction is well presented by Islam et al. [161] and supported by Winfried Mönch in his theoretical work on barrier heights of real Schottky contacts [162]. According to Islam et al., MIGS are created by the electron wave function in metal and penetrates into the bandgap of silicon. This leads to formation of a dipole charge at the interface. In equilibrium, the Fermi level of metals shifts close to the charge neutrality level of the silicon. At this point the MIGS switch from donorlike to acceptor like to compensate overall dipole charge. This effect is known as Fermi level pinning and causes the barrier height metal/semiconductor junction become less sensitive to the metal workfunction. A qualitative factor that defines how strongly metal Fermi level will be pinned toward charge neutrality level is defined as

empirical parameter pinning factor S and for TiO$_2$ S=0.58. The pinning factor leads to effective metal workfunction and for TiO$_2$ it is equal to 4.5 eV and align well with Al and Ti as contact metals [161].

The schematic structure of the TiO$_2$-Si stack shown as an inset in Fig. 3.16(a) was simulated and analyzed using Sentaurus TCAD [163]. The TiO$_2$ material parameters from Islam et al.[161] were used. Thermionic emission, trap-assisted, and direct tunneling models [164] were employed for the carrier transport simulation of TiO$_2$/Si(p) devices. A constant mobility model was assumed inside TiO$_2$. Fermi-Dirac statistics was used to determine the carrier density. The trap density inside the TiO$_2$ film is assumed as a uniform distribution for the sake of simplicity.
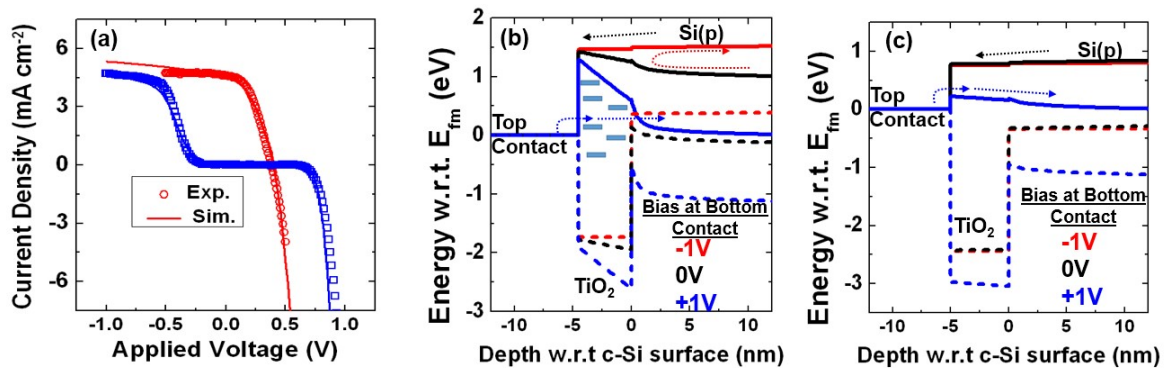
FIGURE 3.17: (a) Comparison of experimental (symbol) and simulation (line) data of TiO$_2$-Si(p) structure. 2.2×10^{17} cm^{-3} (blue line) and 1.2×10^{18} cm^{-3} (red line) are the assumed doping concentrations inside the TiO$_2$ film with a trap density of 1.25×10^{18} cm^{-3}. (b, c) Band diagrams simulated under illumination and different bias conditions magnified near the front contact (blue: +1 V, red: 0 V, and black: -1 V) for 2.2×10^{17} and 1.2×10^{18} cm^{-3} doping concentrations of the TiO$_2$ film, respectively. The conduction band edge is shown as a solid line and the valence band edge is shown as a dashed line. Electron flow is shown schematically in band diagrams

Figure 3.17 (a) shows the experimental and simulated $J - V$ curves. The S-shaped kink in the $J - V$ curve indicates the performance degradation. An improved $J - V$ curve without a kink is also shown in the same figure. Simulation predicts that the S-shaped kink is due to the lower carrier density inside the TiO$_2$ film, whereas a high carrier density improves the performance. The explanation of the kink under low carrier density and its improvement is provided below. Figures 3.17 (b) and (c) show the band diagrams of simulated structures that matched the experimental data in Fig. 3.17 (a) for different TiO$_2$ carrier densities of 2.2×10^{17} and 1.2×10^{18} cm^{-3}, respectively. These band diagrams are zoomed on the front region of the Al/TiO$_2$/Si(p) stack, which was simulated under 1-sun illumination and various biasing conditions (-1, 0, and +1 V). In the band diagram for low carrier density inside the TiO$_2$ film shown in Fig. 3.17 (b), a barrier for electrons (in addition to holes) is observed at ≈0 V. The barrier is reduced under a negative bias condition and thus more photogenerated electrons are collected. This is the reason for the enhanced photocurrent under the negative bias condition in Fig. 3.17 (a). However, the barrier becomes more pronounced under a positive bias condition. The barrier restricts photoelectron flow and causes a current drop in the $J - V$ curves, which is the reason for the S-kink in the $J - V$ curves. Under a large positive bias (>0.6 V) condition, band bending favors a trap-assisted tunneling (TAT) mechanism to inject electrons in the opposite direction to the photoelectron flow, which is shown schematically in Fig. 3.17 (b) (see Fig. 3.18 for the carrier motion picture).

The current density in TiO$_2$-Si heterojunction consists of five correlated charge carrier transport processes: Schottky emission (SE), direct tunneling (DT), Fowler-Nordheim tunneling (FNT), Poole-Frenkel emission (PFE) and TAT [165]. Three of five processes, i.e. SE, DT and FNT are included in Tsu-Esaki model [117] and described in Sect. 2.6. The TAT model employed in this work is actually proposed for near-interface oxide traps in the Si/SiO$_2$ interface. It accounts for both elastic and inelastic tunneling and depends on the tunneling probability density computed based on Wentzel–Kramers–Brillouin (WKB) approximation. TAT theory was used in device simulation using capture and emission rate which enables the traps inside the TiO$_2$ film to capture and emit electrons from the nearby interfaces according to Weiler et al. model [165]. It uses Fermi-Dirac statistics for occupation probability whereas, for multi-phonon assisted inelastic tunneling, capture rate also depends on the Bose-Einstein statistics. The full description of the model are given in the Sentaurus Manual [163].
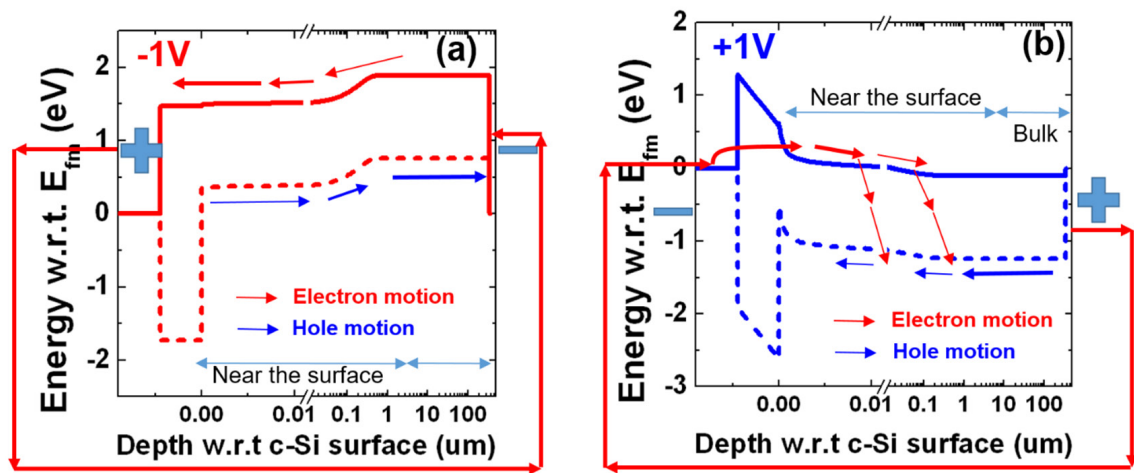
FIGURE 3.18: Electron and hole motion picture for (a) -1 V and (b) +1 V bias condition at the bottom contact of TiO$_2$-Si diode. Simulated TiO$_2$ film has a carrier density of 2.2×10^{17} cm^{-3} and a trap density of 1.25×10^{18} cm^{-3}

This becomes the transport mechanism under high positive bias condition, even under dark condition. Figure 3.17 (c) shows that the band alignment in the high-carrier-density TiO$_2$ film is weakly dependent on bias conditions, where no electron barrier is seen, and hence, no S-kink is observed in $J - V$ curves. Consequently, high-carrier-density TiO$_2$ films are preferable candidates for carrier-selective solar cell applications. Carrier and trap density variations in the TiO$_2$ film are shown in Subsect. 3.2.5.

3.2.6 Carrier and trap density variations of the TiO$_2$ film

Figure 3.19 shows the carrier and trap density variations of the TiO$_2$ film. The figures show that TiO$_2$ film with high carrier density or low trap density exhibits the desired performance. Otherwise, S-shaped $J - V$ curves are observed. It is due to the electron barrier (in addition to the hole barrier) which occurs at the specified biasing conditions for low carrier density films. The electron barrier occurs due to the highly sensitive TiO$_2$ band alignments with the biasing conditions for the low carrier density film.
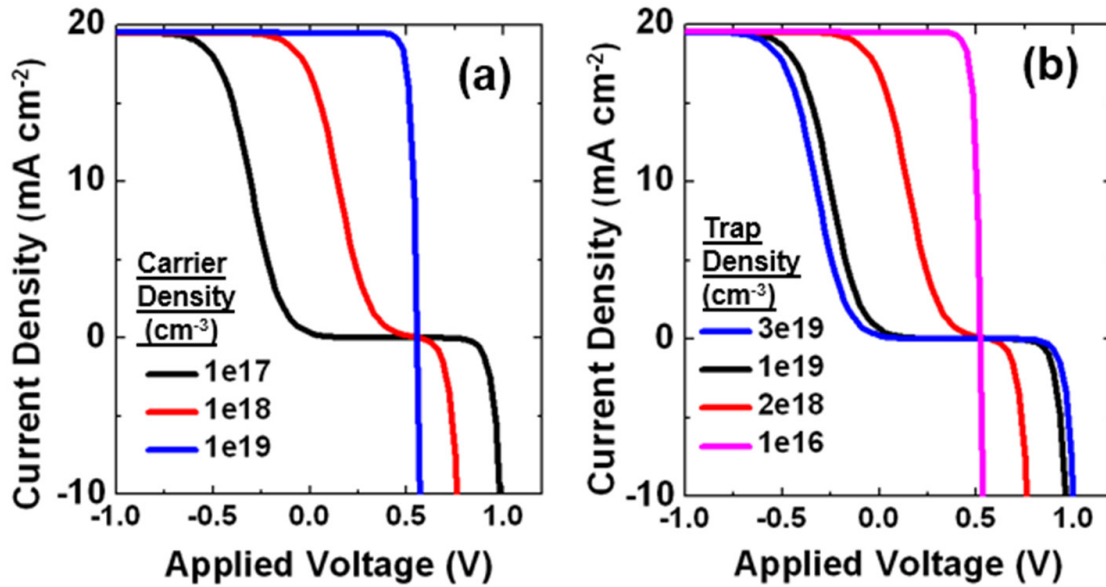
FIGURE 3.19: $J-V$ variations on TiO$_2$ carrier density for the assumed trap density of 2×10^{18} cm^{-3} (b) $J-V$ variations on TiO$_2$ trap density for the assumed carrier density of 10^{18} cm^{-3}

3.3   Interlayer and annealing effect

3.3.1   Passivation properties of TiO$_2$ films with interlayers on Si

The SiO$_2$ interlayer has shown excellent surface passivation and thermal stability in SiO$_2$-doped poly-Si CSC [22]. Al$_2$O$_3$ grown by ALD has also shown excellent passivation properties with a dual passivation mechanism: chemical surface and negative charge passivation schemes [166]. Therefore, these two material interlayers were introduced to test their effect on TiO$_2$ passivation and carrier-selective properties. Three groups of samples were prepared, as shown in Fig. 3.4. The measured effective lifetime is shown in Fig. 3.21 (a). For the annealing experiment, 5 nm TiO$_2$ films were tested since this thickness was reported as the optimal TiO$_2$ thickness with the best diode properties [126]. TiO$_2$-Si and TiO$_2$-SiO$_2$-Si stacks show almost similar effective lifetimes in the range of 150-300 μs (Fig. 3.20).

TiO$_2$-Al$_2$O$_3$-Si stacks show 2-3 times higher passivation quality than as-deposited samples, i.e., effective lifetimes around 600 μs. It is interesting that annealing in N$_2$ ambient of all samples improves passivation quality only until 200 $^{\rm o}$C while lifetime degraded at temperatures above 200 $^{\rm o}$C. Additionally, the annealing in forming gas (5 % H$_2$ and 95 % N$_2$) was tested. The annealing results in forming gas are slightly better than those with N$_2$ ambient annealing. For safety and practical reasons, the experiments with annealing in N$_2$ ambient only was selected to continue further. It was observed that annealing time also affects the passivation quality: annealing for 10 min has been proven as the best to achieve the highest passivation quality, while annealing for 30 min causes passivation quality degradation. Annealing-dependent passivation improvement could be explained by the assumption that at 200 $^{\rm o}$C the TiO$_2$ films transform to anatase phase and remain uniform and continuous (according to the AFM image as shown in Fig. 3.10 (d)), while a longer annealing time might create film cracks. An annealing temperature of above 200 $^{\rm o}$C causes the coalescence of anatase grains and film cracks and, as a consequence, lifetime degradation. SiO$_2$ and Al$_2$O$_3$

FIGURE 3.20: Annealing effect on TiO$_2$ passivation quality on Si wafers with and without SiO$_2$ and Al$_2$O$_3$ interlayers. (b) Time-dependent degradation and annealing effect on TiO$_2$ passivation films
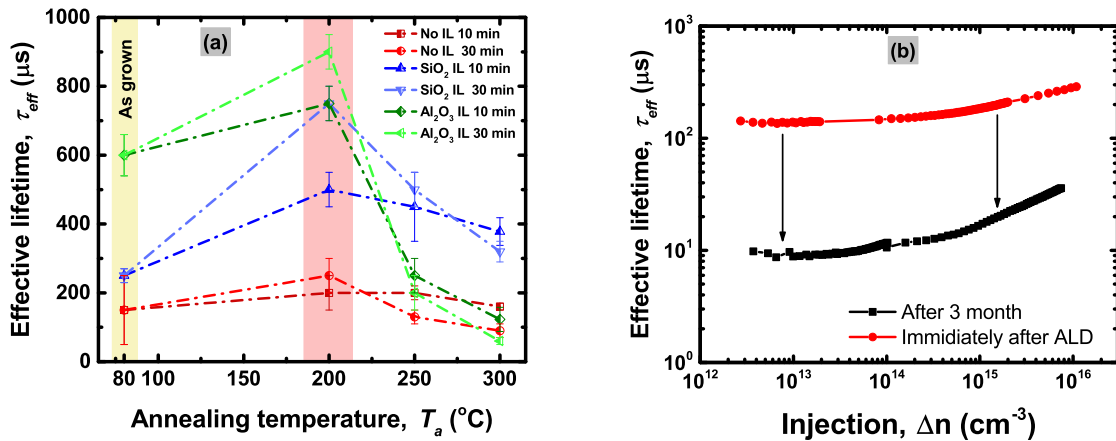
interlayers play a major role in passivation quality. In the case of the SiO$_2$, interlayer passivation is well reported [167–169]. For Al$_2$O$_3$ ALD growth, a TMA precursor was used. TMA precursor is a source of hydrogen and hydroxylic radicals, that chemically passivate dangling silicon bonds on the interface, whereas Al$_2$O$_3$ and TiO$_2$ provide negative charge passivation [169]. It is important to note, that the annealing process should occur immediately after the ALD deposition of TiO$_2$, since it has a time-dependent lifetime degradation as shown in Fig. 3.20 (b). It was noted that such lifetime degradation for all TiO$_2$-coated samples without and with Al$_2$O$_3$ and SiO$_2$interlayers. However, owing to a huge number of data, it was decided to focus only on the TiO$_2$-Si structure. Two types of TiO$_2$-Si samples were compared: samples after three months of lab storage and samples immediately after ALD deposition. The lifetime degradation corresponds to a factor of 7 (from 350 to 50 μs). This phenomenon is not studied well and will be investigated further. The probable reason for such behavior is TiO$_2$ moisture absorption, and slow crystal phase transformation and film cracks caused by different crystal phase grains.

3.3.2 TiO$_2$-Si diodes with interlayers: TCAD simulation and experiment comparison

Test structures were fabricated as described in Sect. 3.2 and according to Fig. 3.5. Figure 3.21(a) shows the simulated and experimental $J - V$ curves for TiO$_2$-SiO$_2$ (or) Al$_2$O$_3$-Si(p) devices. Test structures with interlayers did not show any improvement in illuminated $J - V$ curves [see Fig. 3.21 (a)], which is independent of carrier density inside a TiO$_2$ film despite carrier lifetime improvement. This effect was attributed to the very high recombination in the rear surface of the test structure owing to the direct aluminum contact on the Si(p) wafer (see Fig. 3.5). Hence, improvement by front surface passivation is nullified by the very high rear surface recombination velocity, and hence, the effective carrier lifetime of the metalized test structure is not enhanced with interlayers leading to poor V_{OC}.

In case of the TiO$_2$ film with a low carrier density, a mild degradation in performance is observed with interlayers when compared with that without any interlayers, as shown in Fig. 3.21 (a). Simulation predicts that degradation might be due to the tunneling transport and lesser availability of states for trap-assisted tunneling hindering the performance,
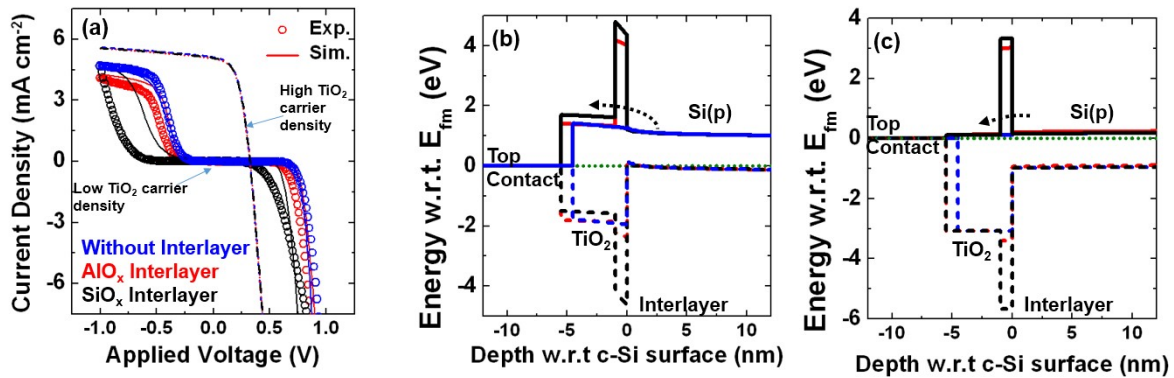
FIGURE 3.21: (a) Experimental (symbol) and simulated (lines) $J-V$ for interlayers, Al_2O_3 (red), and SiO_2 (black). The curves for without and with interlayers are overlapped for a high-carrier-density TiO_2 film. Correspondingly simulated equilibrium band diagrams with conduction band edge (solid line) and valence band edge (dashed line) for (b) low TiO_2 carrier density and (c) high TiO_2 carrier density, magnified near the front contact. Please note that the Si(p) is inverted near the surface in (c) due to the large work function difference between the high-carrier-density TiO_2 film and Si(p). Fitted TiO_2 carrier density was slightly lower for the SiO_2 interlayer, which can be seen from (b). TiO_2 carrier density significantly alters the front band alignment, and hence, the electron collection mechanism

which is shown in Fig. 3.21 (b). Such phenomenon is absent in high-carrier-density TiO_2 film shown in Fig. 3.21 (c). With different interlayers, in addition to a slight change in the fitted TiO_2 carrier density for the SiO_2 interlayer, the current density difference under the negative bias condition is attributed to the fixed charges in the interface of the passivation layer and Si(p). In the case of the positive bias condition, the difference in current density is due to the availability of states for trap-assisted transport.

To estimate the potential V_{OC} of the TiO_2-based electron contact, simulation was performed with passivated contacts on both sides, which shows that V_{OC} could reach 700 mV with improved optical transparency on the illuminated side (results not shown here). Please note that fixed charges and interface trap density at the interface of the substrate and interlayer play a significant role in the charge collection mechanism, which is notable only in the case of passivated contacts on both sides.

In summary, despite the increase in charge carrier lifetime due to interlayers, no improvement in $J-V$ curves is observed owing to a very low rear surface lifetime of the metalized test structure used in this study. It requires further work with passivated contact on both sides of the wafer to understand the role of interlayers in the performance of the carrier-selective solar cells.

3.4 Conclusions

In this chapter, comprehensive design, experimental process development, simulation and optimization of TiO_2-Si structures with and without SiO_2 and Al_2O_3 interlayers for applications in SHJ solar cells are presented. The TiO_2-Si structure for passivation and carrier-selective properties have been studied. The results suggest that TiO_2 and interlayer growth condition, surface passivation, TiO_2-Si energy band alignment, and the quality of interfaces play important roles in determining the performance of such devices. Consequently, the

following key factors, which improve the performance during fabrication of TiO_2-Si passivating carrier-selective contacts, are suggested:

- ALD temperature affects the passivation and diode properties of the TiO_2-Si devices. Low-temperature-grown TiO_2 films possess a much higher passivation quality owing to the continuous amorphous film. At higher temperatures, the TiO_2 films form preferentially in the anatase phase with increased roughness. At 80 °C, the V_{OC} has a low value equal to 275 mV. V_{OC} values increase either with a higher ALD growth temperature at 100-150 °C or with annealing at around 200 °C. Above 250 °C, the growth or annealing processes have a detrimental effect on passivation and diode properties. This effect is caused by the modification of the TiO_2 surface morphology, anatase crystal grain formation, and change in stoichiometry in TiO_2 films.

- Therefore, the best ALD grown TiO_2 films were obtained at low-temperature (80 °C) and further annealed at 200-250 °C for 10 min. These conditions allow transforming an amorphous film to anatase phase. Such treatment allows improving the lifetime even further and increasing V_{OC} without the degradation of TiO_2 film quality.

- Interlayers such as SiO_2 and Al_2O_3 markedly improve passivation quality by a factor 3-10. Note that Al_2O_3 interlayers show a significant enhancement of passivation properties. However, the nature of this phenomenon has not yet been investigated. Simulation predicts that TiO_2 with a high carrier density is a favored candidate. Despite the increase in carrier lifetime for TiO_2 with interlayers (SiO_2 or Al_2O_3), the $J - V$ performance has not improved for the metalized test structure used in this work. In contrast, mild degradation is observed for the case of a TiO_2 film with a low carrier density when compared with that without interlayers.

Chapter 4

Silicon Light Trapping Nanostructures

"Take it easy, but take it."

Woody Guthrie

This Chapter discusses a concept of texturing silicon surfaces for enhancing light trapping properties. Different texturing methods are compared, including metal assisted catalytic etching (MACE), alkaline KOH-etched pyramidal microstructures and reactive ion etching (RIE) nanostructured Si known as black Si. The main focus is on black Si optical and electro-optical properties optimization for heterojunction silicon solar cell application. Achievement of low surface recombination velocity (SRV) with low optical reflectivity are reported as a results of optimization of RIE process for Si texturing. Excellent passivation quality of ALD Al$_2$O$_3$ on black Si surfaces was reported here and in Journal of Applied Physics [170]. To understand the electro-optical properties of nanostructured Si, a theoretical model for effective lifetime of minority carrier in black Si was applied to experimental results presented here and in Semiconductor Physics, Quantum Electronics and Optoelectronics Journal [87]. Since conventional silicon solar cells rely on a doping process for junction formation, experiments were carried out and presented here on phosphorous doping on textured silicon surface under different ambient, including temperature and time variation.

4.1   Introduction

High-efficiency conventional silicon solar cells are based on wet alkaline etching for surface texturing with a feature size between 5 and 10 μm. This process has been adopted as a standard by the photovoltaic industry because of its cost-efficiency and good light trapping properties [171]. However, this surface texturing leads to a reflectivity of approximately 5-10 %, so single or multilayer ARCs are applied on top of the microstructures to reduce reflectance to 2 % [32]. Black Si nanostructured surfaces, which are textured using maskless RIE may be a replacement for wet-chemical texturing in silicon solar cell fabrication [172–176]. Black Si yields extraordinary low reflectance in a vast spectral range. Thus, an additional ARC is not required to reduce reflectance. Black Si RIE technology also enables reduction of the Si wafer thickness to below 100 μm [176], avoids the use of toxic materials [177] provides easy RIE process optimization through adjustment of plasma parameters and offers the possibility to texture any Si-based film or wafer, such as multi-crystalline [178], cast-mono, kerfless and diamond-wire sawed Si substrates. However, the first attempts to integrate black Si into a solar cell reached average conversion efficiency [175, 179], due to surface defects and surface recombination caused by ion impact damage [180] and increased effective surface area. A possible solution is to optimize the plasma texturing process with

a focus on reduction of surface recombination. To optimize the RIE process, black Si formation process was analyzed and defined as consisting of three steps [181]: 1) Isotropic Si etching with fluorine radicals to form volatile SiF_4. 2) The addition of O_2 causes a local masking layer of SiF_xO_y to build on the Si surface (mainly on sidewalls). 3) Etching of the SiOF passivation and Si layers. The etching process combines chemical and physical etching (ion-assisted etching). To further decrease surface recombination, a wet chemical RCA cleaning, and subsequently, ALD Al_2O_3 passivation layer should be applied [182–184]. Excellent surface passivation is known to be obtained with ALD Al_2O_3 on planar silicon due to the high fixed negative charge in Al_2O_3 and the low defect density at the interface between Si and Al_2O_3. In this chapter, results on testing different Si texturing techniques are presented. However, the main focus is devoted to optimization of RIE black Si process with reduced ion energy and flux density. Such approach allowed us to reduce surface damage, and consequently to improve the effective carrier lifetime.

4.1.1 Silicon nanostructuring methods

In this Subsection, different top-down silicon texturing techniques for photovoltaic devices are presented. These techniques are based on solution-liquid-solid (known as metal assisted catalytic etching and alkaline (KOH solution) based etching) and reactive ion etching methods. These texturing processes enable the fabrication of micro- and nanostructures with a highly ordered and alignment structures leading to enhance the light absorption. For photovoltaic application, textured surfaces should follow few parameters criteria: excellent light trapping properties and low surface recombination velocity. These two qualities are presented here as a set of parameters to qualify textured surfaces for photovoltaic applications.

Note: materials used for the experiments were 100 mm diameter CZ c-Si (100) n- and p-type (1-20 $\Omega \cdot cm$) wafers with thickness 350±25 μm and a bulk lifetime above 2 ms.

4.1.2 Wet chemical metal-assisted catalytic etching

Introduction to MACE. Metal-assisted catalytic etching (MACE) is a procedure for generating nanostructures on Si, which at first glance has low reflective properties and is typically referred as black Si. The idea is to deposit a very thin layer of metal that can catalyze a Si etching process in a chemical solution. The metal layer is so thin ($\approx$1 nm of gold) that it is deposited evenly and balls up in nanoparticles. In the area around the metal particles etching will be catalyzed, and etch very fast compared to areas without gold. MACE of Si occurs in the presence of HF and an oxidative agent, catalyzed by noble metals. Well presented review of this technique was published by Huang et al. in 2011 [185].

In MACE process, a Si substrate is covered by ultra-thin (5-10 nm) layer of noble metal nanoparticles, commonly gold (Au) and silver (Ag), and immersed in a solution of HF and an oxidative agent (H_2O_2) [185–187]. The noble metals can be deposited onto the surface by physical vapor deposition techniques (i.e., via thermal evaporation, sputtering and electron beam evaporation) or in solution (i.e., via electrolysis deposition and electro-deposition) [185–187]. In our experiments, an electron beam vacuum deposition was selected to catalytic metal layer deposition. This technique allows a higher degree of control over the metal film morphology. During the chemical reaction, noble metal ions acquire electrons from the silicon valence band and are reduced to form seed nuclei which develop into nanoparticles as shown in Fig. 4.1 (a). At the same instance, these ions inject holes underneath the silicon
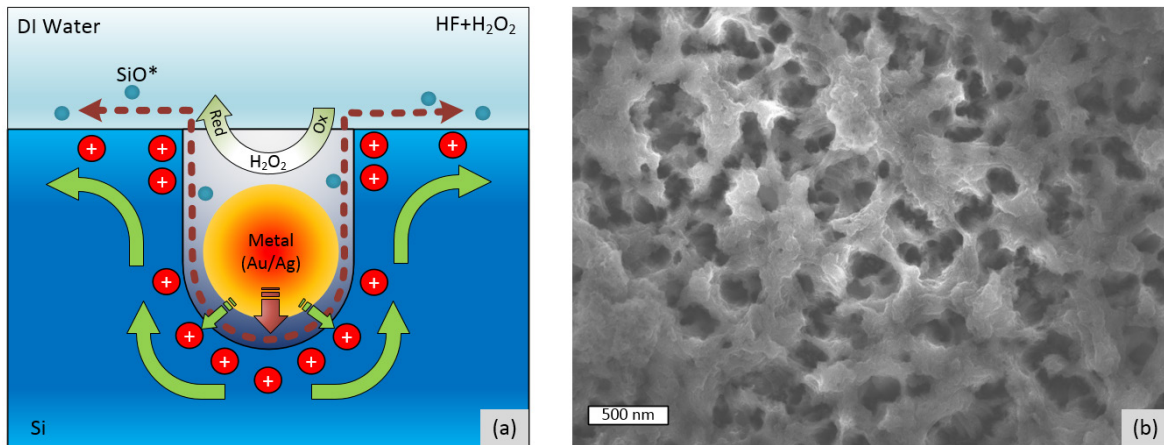
FIGURE 4.1: (a) Schematic illustration of metal-assisted catalytic etching process (inspired and adopted from [185]) and (b) SEM image of top view nanostructured surface

causing oxidation into SiO or SiO_2, which are then removed by HF [185, 188]. This process continuously removes Si and sinks the metal nanoparticles further into the Si creating porous structures (Fig. 4.1 (b)). The depth of these nanopores is directly proportional to the etching time [189]. Once the desired surface morphology obtained, the metal nanoparticles are removed by another etchant or neutralizing solution, such as HNO_3 or KI and followed by a cleaning process.

Figure 4.1 illustrated (a) schematic of the metal-assisted chemical etch process: first, a noble metal nanoparticle catalyze the reduction of an oxidative agent H_2O_2; second, generated holes are injected during the reduction reaction into the silicon substrate, with the highest hole concentration underneath the metal particle; third, holes migrate to silicon sidewalls and surfaces; and the fourth step the oxidizes silicon is removed with HF [185].

Koynov et al. [190] stated that the etching speed was deficient around 1 nm/min confirming the importance of metal catalyst in the etching process. Addition of Au increases the etching speed, and the size and shape of deposited metal particles largely define the morphologies of the etched surface. Thus, the Si underneath the metal catalyst is etched much faster, and by controlling the surface coverage and distance between metal particles, surface nanostructures can vary from black Si hillocks to nanowires [190, 191].

MACE texturing experiments. The results on MACE based nanostructuring process are presented. Morphology of formed nanostructures were studied with SEM and residues of gold in Si were studied with EDX technique. Optical properties of MACE etched black Si are compared with KOH-etch nanostructures and RIE black Si.

The MACE procedure was based on the method described in [35]. Plain n- and p-type Si wafers were acetone dipped, IPA rinsed, and bHF dipped for 30 sec in order to preclean and remove the native oxide layer. Next, 1 nm of gold was deposited with Alcatel electron beam system. It was found that the best thickness to obtained quick catalytic reaction and appropriate nanostructure depth was ≈1 nm of gold. Any above thickness of gold layer reduced chemical reaction speed and depths of nanostructures. After gold deposit, the next etching steps were introduced. First, a solution of HF (40 %)/H_2O_2 (30 %)/H_2O (volume ratio: 1.25:5:10) at room temperature was prepared. Second, gold coated samples were dipped in to the solution. The first sample was etched for 1 min, rinsed in bubble DI water for 1
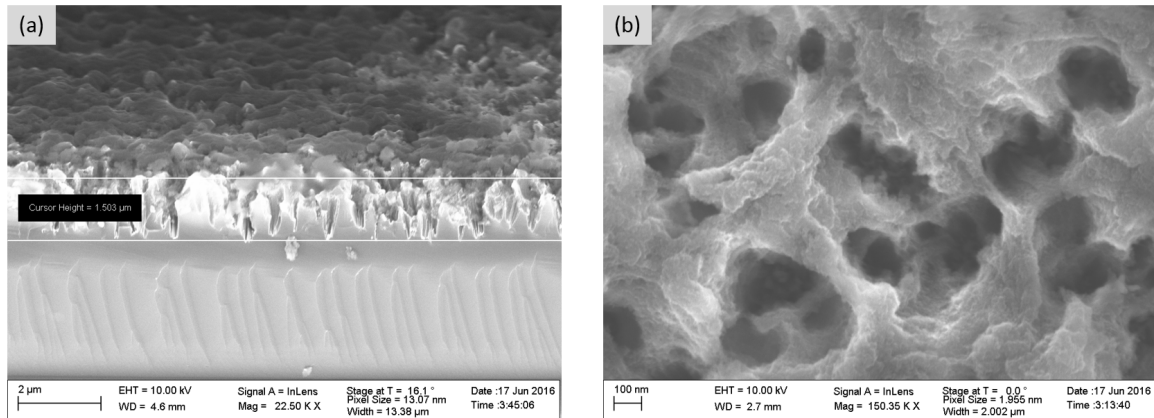
FIGURE 4.2: SEM image of side and top view wafer with MACE surface. The surface is very random and chaotic, but the etch depth is very uniform, most within a couple of hundred nm.(a) SEM image from the side of a snapped wafer with MACE surface. Height is approximately 1.5 μm; (b) SEM image with top view of MACE wafer

min, dried off with a nitrogen flow gun, inspected under the light, and then reemerged into the etching solution. This procedure was repeated five times, to achieve a total of 5 min etch time. Due to created nanostructures the surface obtained hydrophobic properties. It caused inhomogeneous surface etching due to trapped air bubbles on the surface. To solve this issue, the next samples were etch continuously for desired amount of time.

The second experiment consisted with a variation of gold thickness. Two wafer samples were immersed into a HF/H_2O_2/H_2O solution for 1.5 min etch. As a results, 1 nm Au-coated samples looked more black than the 5 nm Au-coated samples inspected with optical microscope. Afterwards, the wafers were dipped into an Iodine:KI:H_2O (weight ratio 1:4:40) solution for 30 - 80 s to remove metal particles. This was done on all the wafers except for one SEM and EDX reference wafer.
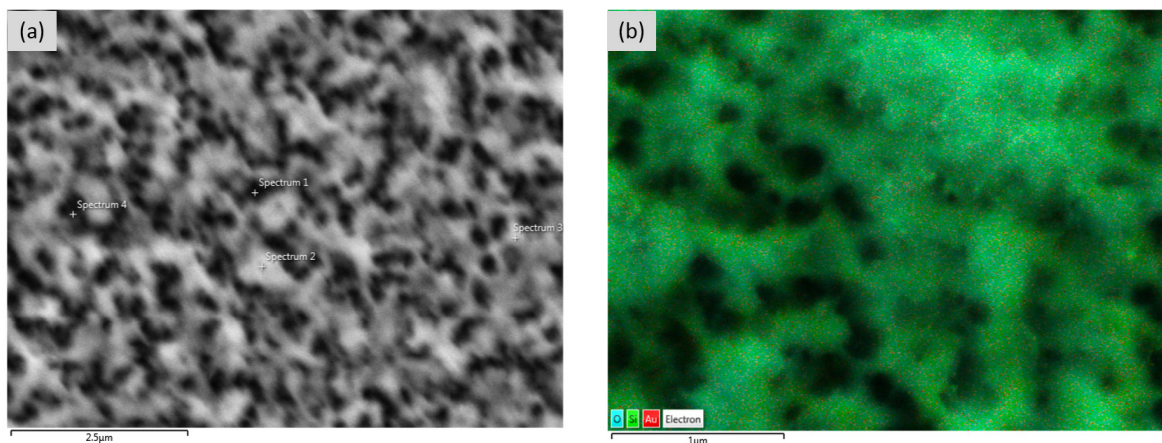
FIGURE 4.3: EDX images with detected materials highlighted in colors. It is apparent that the gold traces are still present. No big cluster were detected, however numerous small signals from various places on the wafer. (a) SEM image of top surface with indication of EDX analysis sites on the surface; (b) EDX map image, same as to the left with color overlay representing the different elements detected. Here, green corresponds to Si, blue to O, and red to Au.

Surface morphology analysis was conducted on SEM Zeiss Supra 40. The MACE etched wafer that still had a gold layer was placed in a SEM, and the EDX analysis method was used to detect gold traces on a surface. Figure 4.2 are the SEM images and Fig. 4.3 are the EDX spectra and Fig. 4.4 for an X-ray spectrum.
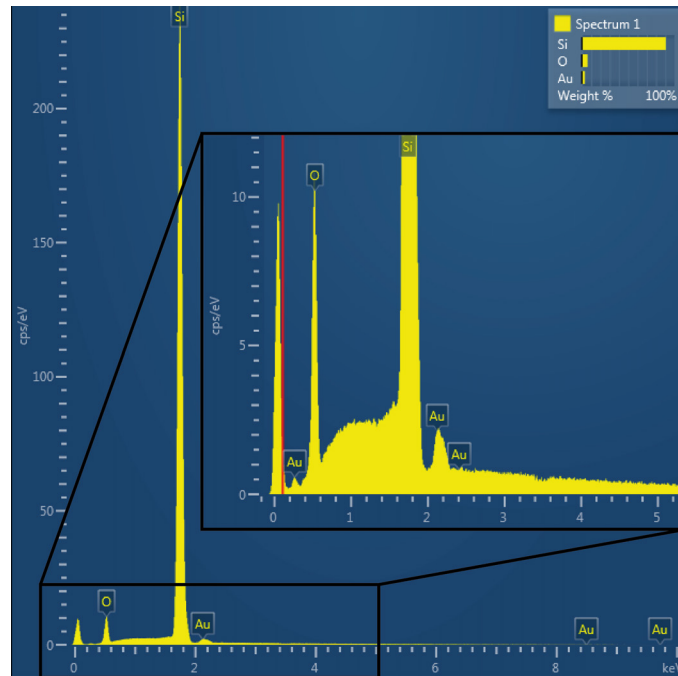
FIGURE 4.4: EDX spectrum showing Au and O traces in depth of Si surface. The samples had 1 nm gold coated layer. According to EDX picks traces of gold were detected even after Iodine:KI:H$_2$O solution cleaning

Conclusion on MACE method. In general, MACE texturing method is very promising which was proved by several reports [174, 192]. However, the method uses either Au or Ag metal particles that should be removed from the surface after texturing procedure. Metal traces cleaning procedure could be very complicated and as shown in our experiments could not guarantee 100% metal traces free surfaces. Such catalytic metals as Au and Ag could create mid energy gap recombination centers in Si, leading to high surface recombination. Our preliminary passivation tests showed a very low lifetime of MACE textured silicon (5-30 microsecond) and therefore, it was decided to skip further application of MACE textured samples in passivation experiments.

4.1.3 Alkaline chemical etching

Introduction to alkaline texturing. Alkaline etching based on potassium hydroxide (KOH) and isopropyl propanol alcohol (IPA) solution is the most widely used texturing method in silicon solar cell production and known as anisotropic etch process [85]. KOH-etching is a highly versatile and cheap way to obtain micro-structured silicon surface [193]. It provides low surface damage and interface defects. Depending on a Si crystal orientation, the etching process can alter due to the anisotropy stems from the different etch rates in different crystal directions as shown in Fig. 4.5. The (111)-planes are almost inert whereas the etch rates of, e.g. (100)- and (110)-planes are several orders of magnitude faster. In this work, standard (100) orientation wafers were used. The etching process followed (111) planes and

created pyramidal structures, which suppress reflectivity on silicon to 8-10 % [194]. However, it induces potassium contamination of the surface and can be non-uniformly textured if any traces of native oxide or other surface contamination left on the surface. Therefore, it is required to properly clean all the wafer in RCA solution before KOH processing. All alkaline etch samples require a wet post-clean ('7-up' or RCA-clean) if the samples are to be processed further.
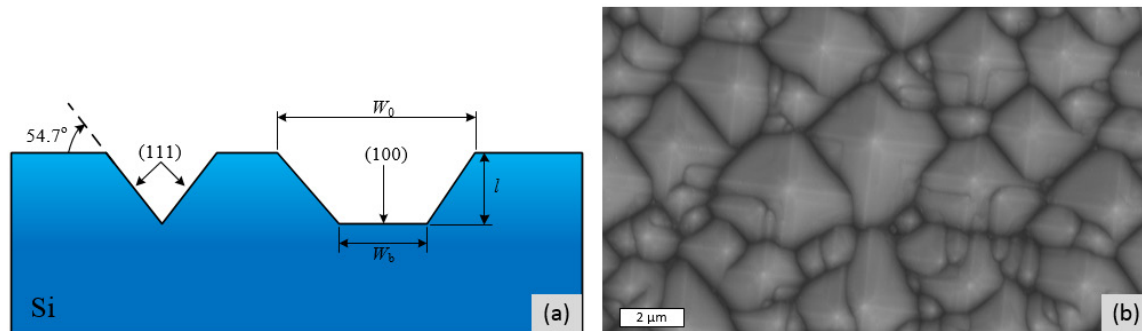

FIGURE 4.5: (a) Etched profile of silicon with (100) orientation and (b) SEM image of top view of KOH textured silicon with (100) orientation. SEM stands for scanning electron microscopy [1]

KOH-based texturing experiments.   A standard a 28 $wt\%$ KOH solution was used for Si etching. The KOH-based texturing process consisted of preparation of a KOH-based solution with 2 % concentration mixed with 7 % isopropyl alcohol (IPA) solution in deionized (DI) water, i.e., 120 ml KOH, 210 ml IPA and 3 liters of DI water. The etch rate and the selectivity towards a SiO_2 mask depend on the solution temperature. The obtained solution was heated to 70 °C which was the texturing process temperature. Addition of IPA solution to 28 $wt\%$ KOH etch solution at temperature of T=70 °C (reduce evaporation of IPA) allowed to achieve more homogeneous pyramidal micro-structures on a surface. Etching with IPA added to the KOH solution was conducted in a dedicated KOH fumehood.

The consistency of the solution was preserved with a magnetic stirring bar. When the solution reached the required temperature, Si wafers were immersed in the solution for 50 min for texturing. After completion of the texturing process, all wafers were post cleaned in the solution of sulfuric acid (98 %) and ammonium persulfate (known as 7-Up), then rinsed in DI water and spin-dried.

4.1.4   Reactive ion etching

Dry reactive ion etching (RIE) or also know as plasma etching process showed very promising results for replacement of wet etching methods. There are two main reasons for that. The first reason is reactive chemical species produced in plasma often more vigorous. The second reason is that plasma etching gives a high level of directional or anisotropic etching possibilities due to the presence of ionic species in plasma and electric field that controls the direction of etching process [195, 196]. Different industrial RIE systems available for plasma etching of silicon. In this project, the SPTS Pegasus deep reactive ion etching system shown in Fig. 4.6 was used.

The reactive ion etching process consists in the formation of ions, assisting radicals formed in the discharge, that provide etching. The RIE process allowed to create randomly ordered

nanostructured silicon surface with surface reflectivity (below 1 %) and obtain so-called black silicon (bSi). The maskless RIE black Si method first was developed by Jansen et al. [197], and more recent works presented by Otto et al. [183, 198], Gaudig et al. [199] and Davidsen et al. [175]

Since the main focus of this chapter is RIE black silicon, further RIE process details, its optimization experiment and black silicon characterization results are presented in the next separate section.
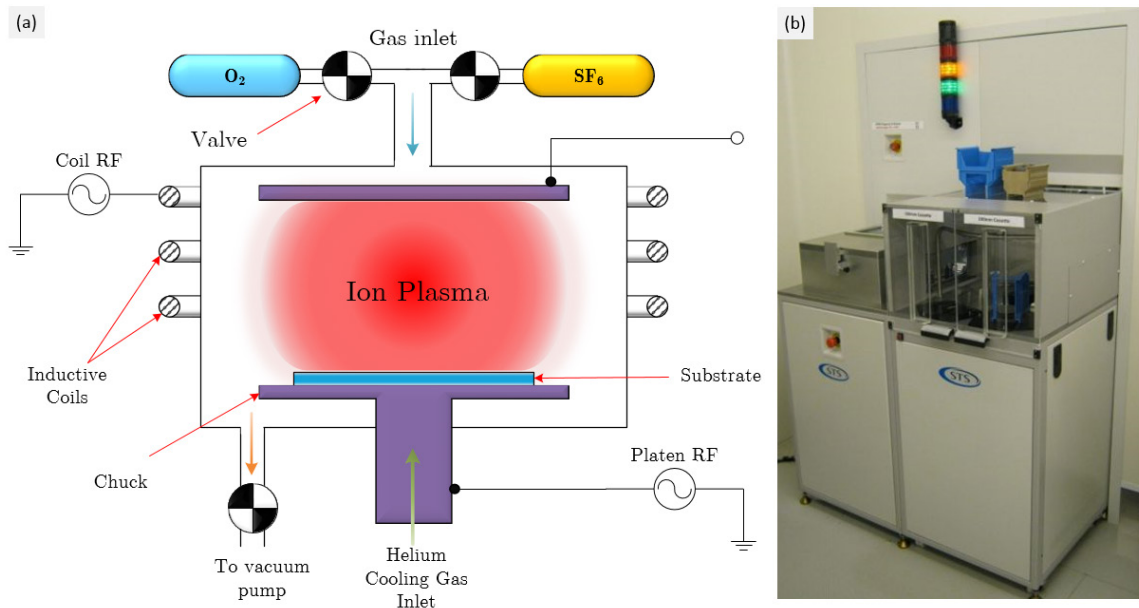

FIGURE 4.6: Inductively coupled plasma system used for the DRIE process: (a) RIE chamber schematic and (b) Photoimage of SPTS Pegasus DRIE system with load lock allowing to process a bath of 25 silicon wafer in automatic mode

4.2 RIE process for nanostructured black Si

4.2.1 RIE process parameters

As mentioned above, the RIE nanostructured Si surfaces were prepared in the SPTS Pegasus deep reactive ion etching system (Fig. 4.6). The setup can produce an ICP using external coils and a CCP using parallel plate internal electrodes with both power systems driven at 13.56 MHz. Each discharge type can be sustained separately or assist each other. In the ICP mode, the wafer stage is grounded, so that ions are accelerated towards the wafer in the potential difference given by the plasma potential, which is at most a few tens of volts.[198]

Ions are assisting radicals formed in the discharge thus providing a rather mild etching. The CCP mode builds up a positive sheath above the wafer, due to the large difference in mobility between ions and electrons. This causes a negative DC bias on the substrate holder in the range from tens of volts to above of 100 V, depending on the power and the pressure. Since the ICP discharge can provide much higher plasma density than the CCP discharge, [198] the simultaneous use of both sources provides perfect control of the RIE process such as to reduce or increase the ion energy and or flux. As a reactant gasses, SF_6 and O_2 were supplied

TABLE 4.1: RIE process parameters

RIE parameters	Ref. [183, 198] & [199]	Ref. [175]	This work
SF$_6$ flow (sccm)	47	37	70
O$_2$ flow (sccm)	55	37	100
Pressure (mTorr)	50	24	45
CC power (W)	20	100	10-70
IC power (W)	600	0	3000
Temperature ($^\circ$C)	20	-10	-20
Max. DC bias (V)	34	41	41

to the chamber while the substrate stage was kept at -20 $^\circ$C. The CCP power was kept low (10 to 50 W) to reduce the kinetic energy of ions while the ICP power was increased from 2500 to maximum 3000 W to create a homogeneous and high-density plasma to enhance the etch rate. The surface aspect ratio of nanostructures was controlled via the chamber pressure which was kept at 38 mTorr to provide the right balance between directionality of the ions and the necessary collisional frequency to produce radical species assisting the etching. As an experimental procedure, the maskless RIE black Si method developed by Jansen et al. [197] was used. A homogeneous black Si surface with reflectivity below 1 % was obtained base on the process developed by Davidsen et al. [175]. The effective lifetime at 10^{15} cm^{-3} injection level for p-type Si was below 50 μs for passivated wafers while reference untextured wafers had 600±200 μs. The optimization process was based on Gaudig et al. [199] and Otto et al. [183, 198] works. The final optimized parameters were as shown in Tab. 4.1.

4.2.2 Black Si nanostructures formation

The black Si nanostructuring process consists of three main steps occurring at low temperature: passivation layer formation, passivation layer etching, and Si etching, which were repeated with discrete time increments until the final process was reached. The nanostructuring process was conducted as illustrated in Fig. 4.7.

The black Si nanostructuring process consists of three main steps occurring at low temperature: passivation layer etching, and Si etching, passivation layer formation, which was repeated in cycles until the final process is reached. The nanostructuring process was conducted in the following order as shown in Fig. 4.7. The etching process is controlled by parameters such SF$_6$ and O$_2$ partial pressure, process temperature, and voltage DC bias measured at the wafer stage. To understand deeper black Si formation and plan further optimization, the RIE process was analyzed with a theoretical model presented by Saab et al. [181]. The passivation layer etching process can be described as following: a sample wafer is loaded into the RIE chamber and cooled to -20 $^\circ$C (Step (1) in Fig. 4.7). SF$_6$ gas was supplied to the chamber and fluorine radicals rapidly attacked the Si and destroyed native oxide on top of the wafer forming volatile SiF$_4$ (Steps (2)-(3) in Fig. 4.7). Then, a passivation layer formed again with oxygen and SF$_6$ supplied to the chamber (Step (4) in Fig. 4.7). Oxygen radicals with SF$_6$ form silicon-oxyfluoride that act as passivation layer:

$$\text{SiF}_4 + \text{O}* = \text{SiO}_x\text{F}_y \tag{4.1}$$

SiO$_x$F$_y$ acts as an etch stop for F* and passivated sample surface. After the passivation layer formed SF$_6$ gases is purged and etching F* radicals etch away silicon-oxyfluoride and
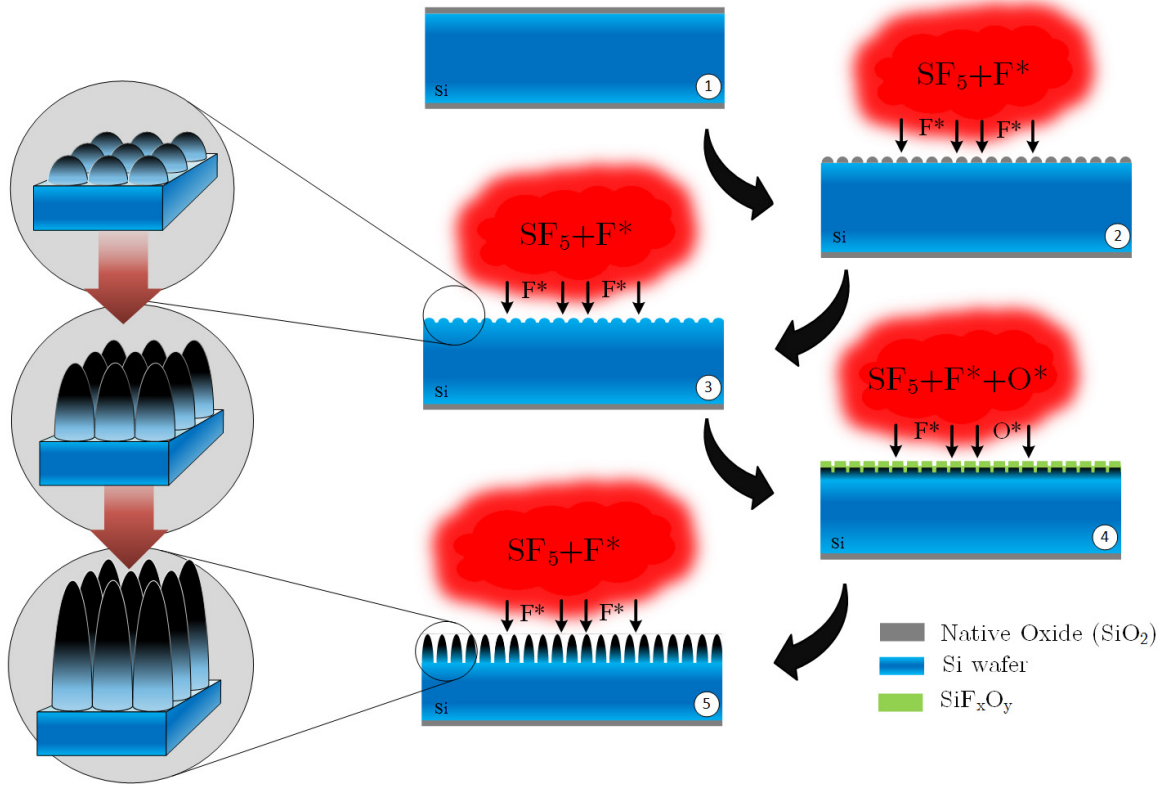
FIGURE 4.7: Schematic view of plasma etching based black Si nanostructure formation

silicon and forming structured surface (Step (5) in Fig. 4.7). Based on the model and experiment analysis, the passivation layer with thickness Z_{PL} can be calculated based on the self-limiting growth of SiO_xF_y and described below:

$$Z_{PL} = f\left(Z_{\mathrm{PL}}^{\mathrm{lin}}\right) = Z_{\mathrm{PL}}^{\mathrm{max}}\left[\frac{2}{1+\exp\left(\frac{-2Z_{\mathrm{PL}}^{\mathrm{lin}}}{Z_{\mathrm{PL}}^{\mathrm{max}}}\right)} - 1\right] \tag{4.2}$$

where $Z_{\mathrm{PL}}^{\mathrm{lin}}$ is the self-limiting thickness of passivation layer is, $Z_{\mathrm{PL}}^{\mathrm{max}}$ is a maximum passivation layer thickness. The passivation layer thickness at the end of the current time step can be calculated by the following expression:

$$Z_{\mathrm{PL}}(t+dt) = f\left(f^{-1}(Z_{\mathrm{PL}}(t)) + \frac{v_{\mathrm{pf}}\Omega dt}{4\pi}\right) - \cos\left(\alpha_{\mathrm{n}}\right)v_{\mathrm{pe}}dt \tag{4.3}$$

which includes the direction etching term that is dependent on normal angle α_{n}, v_{pf}- maximum passivation etching rate, Ω is plasma exposure solid angle everywhere on the surface. The passivation layer, SiO_xF_y has a fixed thickness, and SF_6 gas reacts with the passivation layer and etches until the bare silicon. On horizontal faces, this passivation layer is etched physically due to ion bombardment from the plasma. However, on vertical sidewalls, the sputtering of the passivation layer is weaker due to the directionality of the plasma ions, and the sidewalls, therefore, remain protected from chemical etching by fluorine radicals. As a result, the overall etching process becomes strongly anisotropic. In this regime, precipitates

from the gas phase can lead to the formation of random nanostructures. Passivation layer etching time to bare Si is defined as

$$\delta t = \frac{f\left(f^{-1}\left(Z_{\text{PL}}(t)\right) + \frac{v_{\text{pf}}\Omega dt}{4\pi}\right)}{\cos\left(\alpha_{\text{n}}\right)v_{\text{pe}}} \tag{4.4}$$

Silicon etching are only performed in an area where no passivation layer is present, for the time interval $dt - \delta t$ that is remaining in the current step. The silicon height at the end of the Si etching step is, therefore,

$$Z_{\text{Si}}\left(t + dt\right) = \begin{cases} Z_{Si}\left(t\right) - \frac{v_{se}\Omega(dt-\delta t)}{\cos(\alpha_{\text{n}})4\pi} & \text{if } Z_{\text{PL}}\left(t + dt\right) = 0 \\ Z_{\text{Si}}\left(t\right) & \text{otherwise} \end{cases} \tag{4.5}$$

where v_{se} is maximum silicon etching rate (related to SF_6 concentration).

SF_6 gas was supplied to the chamber and fluorine radicals rapidly attacked the silicon and destroyed native oxide on top of the wafer forming volatile SiF_4. Then, oxygen is supplied to the chamber. Oxygen radicals form silicon-oxyfluoride.

Each new cycle of main steps (Step (1)-(5) in Fig. 4.7) depends on the geometrical absorption and can be proportional to the local solid angle Ω of direct exposure to the plasma. On the other hand, passivation layer etching depends primarily on accelerated ions directed to the sample by the plasma self-biased DC voltage. These high energetic ions with vertical trajectories physically remove the passivation layer. Thus, the etch rate becomes a function of the plasma DC bias but not on geometric absorption. The effective passivation thickness depends on a local surface normal angle since the formation of the passivation layer is a conformal process with highly directional etching. Consequently, the passivation layer etching rate on horizontal surfaces is higher than on close-to-vertical walls [181, 199, 200].

The shapes of such nanostructures were observed by Jansen et al.[201] and can be modified depending on the process parameters. The shape can be changed from parabolic to randomly distributed etch pits that eventually overlap and leave needle-like Si features in-between in agreement with simulations conducted by Saab et al. [181] and observation from other works and in this report in Fig. 4.8. The aspect ratio of the nanostructures can be controlled via the gas pressure, which determines the directionality of ions. This directionality affects the physical etching component. The shape of nanostructures and their aspect ratio are discussed further in Sect. 4.2.3.

4.2.3 RIE process optimization strategy

The main goals of the black Si optimization process were low reflectivity (below 1 %) and improved effective lifetime. The starting process had a reflectivity of 0.5 % but a low effective carrier lifetime of 50 μs. After the process analysis of the etch recipe, it was found that the CCP power was too high leading to high DC bias causing ion impact damage which leads to the low effective minority carrier lifetime. By combining the analytical model and simulation program provided by Saab et al. [181] with the experimental results [SEM images in Fig. 4.8] CCP power was reduced during etching.

This modified etching process resulted in effective lifetimes as shown in Fig. 4.9. All the other parameters in this experiment were kept constant. Figure 4.9 shows that the effective
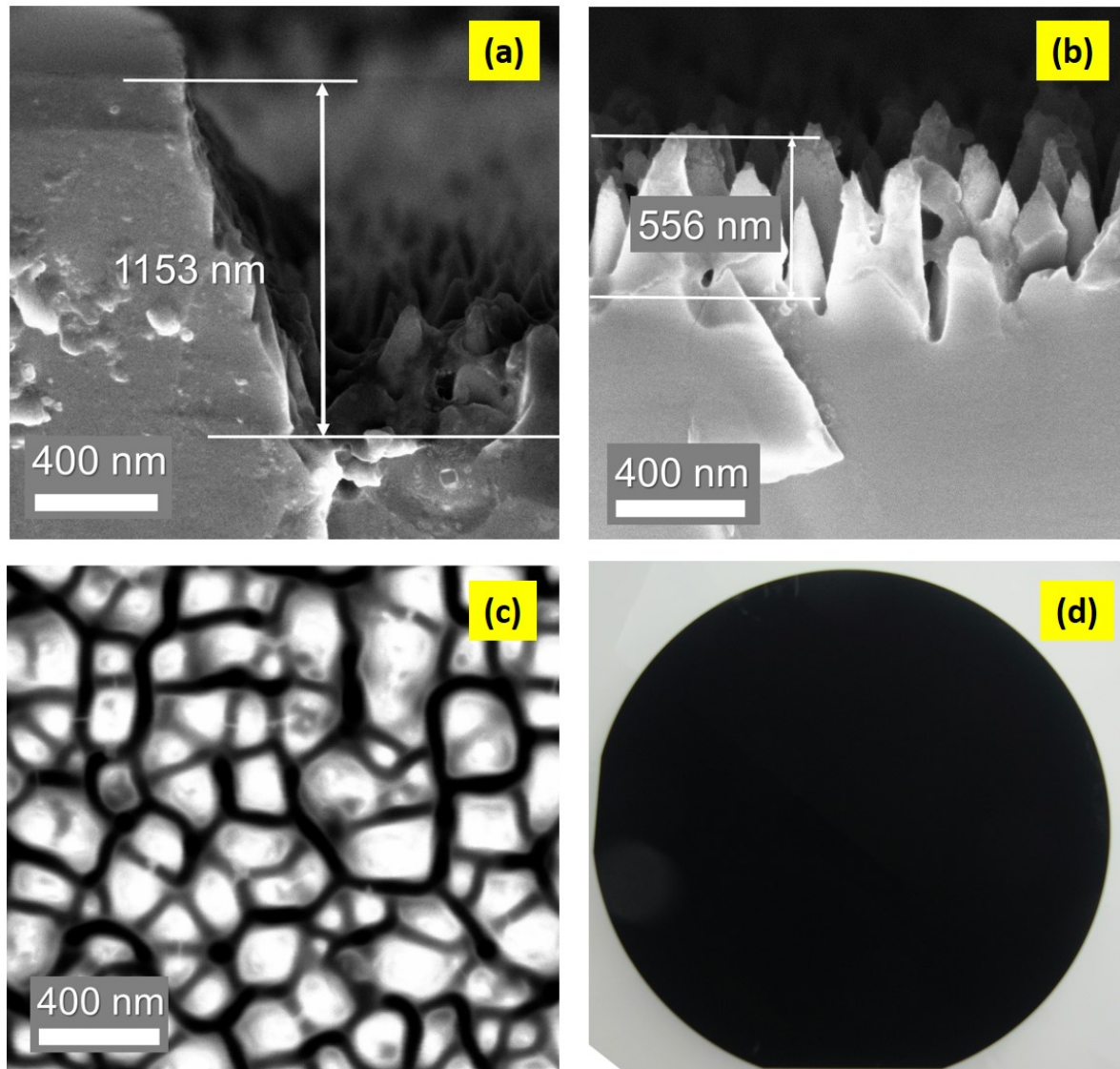
FIGURE 4.8: SEM micrographs and photographic image of nanostructured black Si surface: (a) cross-section view of the etch edge between polished and nanostructured surface; (b) cross-section view of nanostructures; (c) top-view of nanostructures; (d) photograph of a nanostructured black Si wafer

lifetime increased with decreased CCP power, while reflectivity was unaffected except at CCP power below 10 W.

Below 10 W, the reflectivity increased rapidly, and at 0 W the wafer had an almost polished surface morphology. The best trade-off between reflectivity and lifetime is found at 10 W CCP power and a reflectivity of 1 % [yellow zone in Fig. 4.9] results.

For this experiment, the MDP setup was used to measure lifetime at a carrier injection level of 10^{16} cm^{-3}. The MDP map setup uses a high injection level due to default miscalibration. However, it still allowed to identify the main data trends, compare samples at this injection level and select optimal parameters for the RIE process. All the trends were confirmed with test measurements on a QSSPC Sinton WCT-120 Instrument with an injection level of 10^{15} cm^{-3}. These experimental parameters were used for the etch time and double-sided (DS) nanostructuring effect studies presented below.
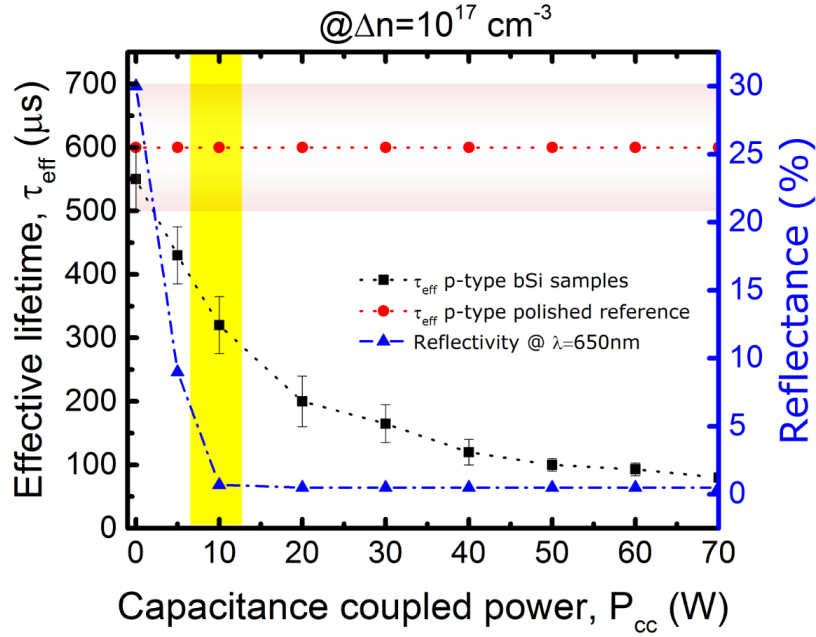
FIGURE 4.9: Black Si optimization based on balancing of a high effective life-
time and low reflectivity as a function of CCP

4.3   RIE black Si morphology: an origin of black Si unique optical properties

4.3.1   Black Si morphology

The origin of the optical effects of black Si nanostructures can be understood from morphology studies of the surfaces. Final nanostructures coated with 30 nm ALD Al_2O_3 are shown in Fig. 4.10 (a)-(c) as SEM cross-sections, SEM images at 30° tilt and drawn profile cross-sections. The RIE etching was conducted with 4 min increments starting from 8 min etch (8, 12, and 16 min) to find the minimum reflectivity of the Si nanostructures in the complete absorption spectral range of Si. For each etch time the height and pitch of nanostructures varied, and the variation agreed with an etch rate of 30 nm/min; a summary is presented in Tab. 4.2.

Black Si nanostructures represented as SEM images and drawn profile cross-sections, as well as SEM images at 30° tilt: (a) for 8 min etch, (b) for 12 min etch, (c) for 16 min etch.

TABLE 4.2: Etch time-dependent black Si nanostructure dimensions

Etch time	Height, nm	Pitch, nm	Al_2O_3 thickness, nm	SEF, γ
8 min	280±50	180±20	30±5	3.8
12 min	440±70	200±20	30±5	5.4
16 min	510±80	250±30	30±5	6.9

Si volume fraction as a function of normalized depth is shown in Fig. 4.11. Since the lateral features are smaller than the wavelength of the incident light, minimal reflection occurs; instead, the incident wave experiences a gradual change in refractive index that depends on the Si volume fraction. This effect is also known as an effective medium theory or moth-eye theory.
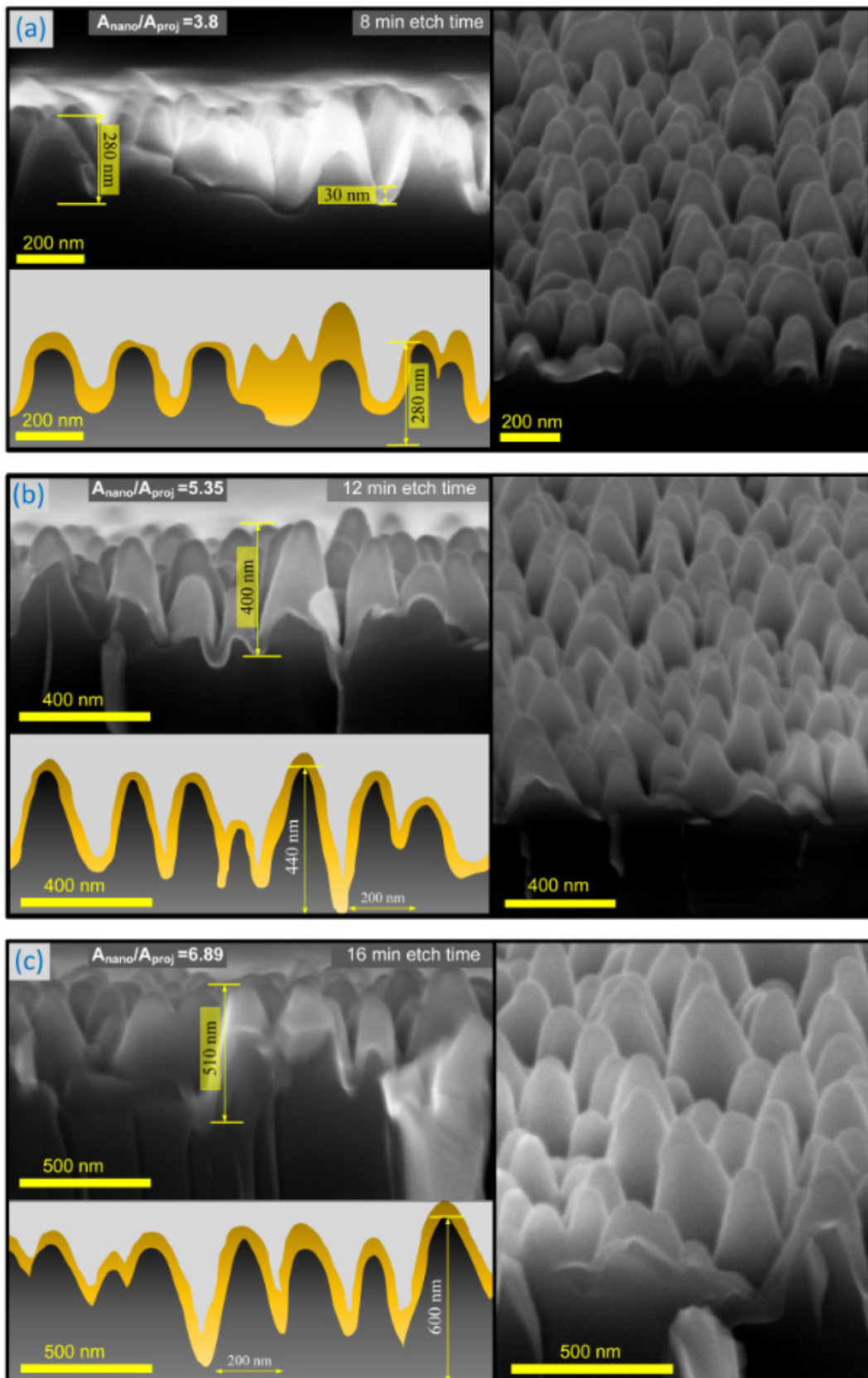
FIGURE 4.10: Black Si nanostructures represented as SEM images and drawn profile cross-sections, as well as SEM images at 30º tilt: (a) for 8 min etch, (b) for 12 min etch, (c) for 16 min etch

4.3.2 Surface area enhancement

The exact surface area of nanostructures is not known and can not be measured due to the random nature of the nanostructures. From SEM cross-section images in Fig. 4.10 the profile shape and the surface enhancement factor (SEF) γ were estimated. SEF was involved in the nanostructuring process as the ratio of top surface area of the nanostructure A_{nano} to the projected area A_{proj} [74]

$$\gamma = \frac{A_{\mathrm{nano}}}{A_{\mathrm{proj}}} \tag{4.6}$$

Obviously, γ becomes unity for the reference sample. From the reconstructed surfaces shown in Fig. 4.10, γ increases for higher aspect ratio nanostructures. The height of nanostructure depends on etch rate, while γ changes from 1 to 7 from planar to high aspect ratio nanostructures (above 12 min etch time). The shape of the nanostructures is more complex as discussed in the previous section. Hence, the statistical calculations of Si fraction variation within normalized depth based on the nanostructure shape are shown in Fig. 4.10 (a).

4.3.3 Si fraction and gradual refractive index

The Si fraction at a certain depth is defined as the integrated cross-sectional area of all protruding Si features that are traversed by a horizontal plain, normalized to the whole cross-section area [174]. The complement presents the fraction of the surrounding air medium. According to Fig. 4.11, the nanostructures have a shape profile between ideal parabolic and conical shapes. The corresponding Si fraction diagram shows three transition regions between the air medium and silicon.

The top layer (I) is defined as a vanishing small conical Si fraction since it contains only the very sharp tips of few nanometers. The second layer (II) depends on the etch time of the samples: for 8 and 12 min samples the second layer was characterized by the almost linear increase of Si fraction with slight variations in-depth; the 16 min samples have the parabolic Si fraction increase with depth. Such dependency corresponds to the transition across the major structural features of the texture, from the top of the conical or parabolic shapes to the bottom layer.

These layers can act as an effective optical medium because the Si nanostructures are not distinguished from the surrounding medium by light with effective wavelength higher than λ_{Si} ~100 nm, which is equivalent to λ_{air}>400 nm [190], since $\lambda_{\mathrm{Si}} = \lambda_{\mathrm{air}}/n_{Si}$. This is also known as the so-called 'zero order effective medium requirement'. The secondary texture features act like a zero order effective medium in the long wavelength region (>1000 nm) similar to a stack of plain surfaces with increased effective refractive index and effective diffractive scattering centers in the visible and NIR wavelength region (400-1000 nm).The third layer (III) has the lower increase of Si fraction for all nanostructures shown in Figs. 4.10 and 4.11. From SEM images, one can see that this layer contains sharp pits. The pits are separated laterally by a pitch from 180 to 280 nm with the aspect ratio close to one as shown in Table 4.2.

According to Fresnel and Snell laws, the reflectivity, absorptivity and transmittivity spectra depend on the effective refractive index of Si and air, and cosine of the propagation angle in each media and it also valid for nanostructures. To evaluate further the refractive index in the nanostructures, the statistical Si fraction curves shown in Fig. 4.11 and theoretical
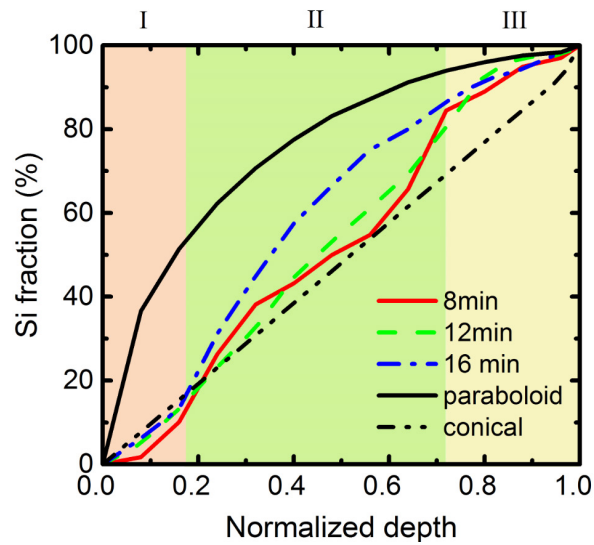
FIGURE 4.11: Depth profile of the Si fraction variation with the normalized depth of the nanostructures

functions approximated for different material and shape interfaces were used. To calculate the effective refractive index profile shown in Fig. 4.12 different material interface were presented with different theoretical functions: a step function for air-plain Si, a linear function for conical shaped structures of Si, cubic or quantic for parabolic-conical shapes function.
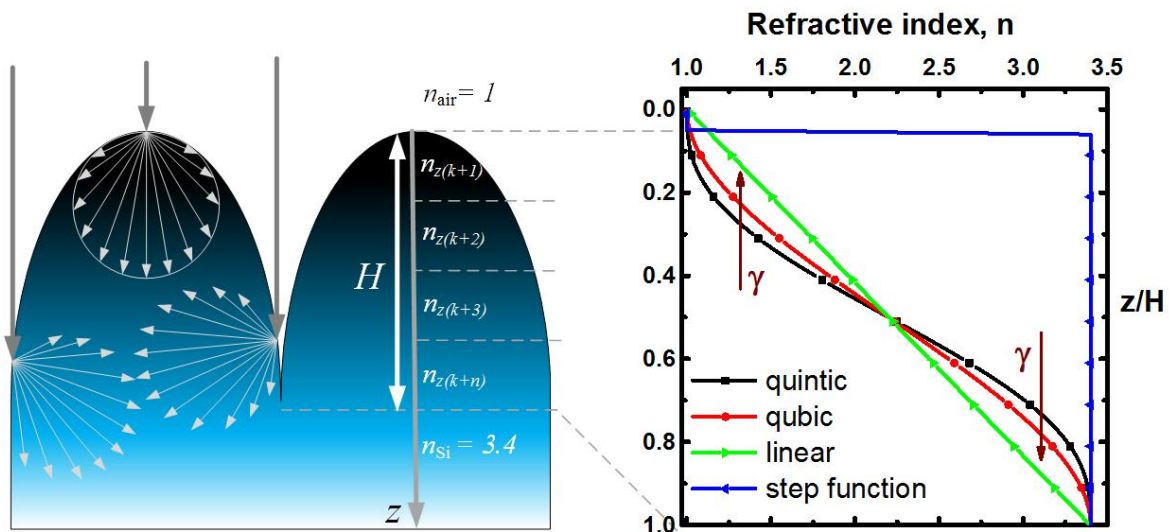

FIGURE 4.12: Profile of light trapping scheme and graded refractive index change in black Si nanostructures

Southwell defined these gradient index functions and showed the surface enhancement factors [81]. Due to the effective refractive index gradient, there is no abrupt interface between silicon ($n_{Si(pristine)}$ = 3.4), and air (n_{air} = 1) and Fresnel reflections are strongly reduced.

4.4   Light trapping mechanism in RIE black Si

Due to the variation of shape and size of nanostructures with etch time two light trapping mechanisms in black Si nanostructures based on effective medium approximation and diffraction mechanism were considered. Hence, the diffraction mechanism based on Lambertian randomized light trapping is the dominant mechanism according to Yablonovitch [83, 190, 202]. With diffraction, solar radiation is smoothly in-coupled from air to Si leading to nearly zero reflectance. According to Fig. 4.10 and Tab. 4.2, the pitch between nanostructures is in the range 180-280 nm, which smaller than or similar to the wavelength in the range (200-1100 nm), then light interferes and forms a transmissivity diffraction pattern behind the nanostructures acting as a diffraction slit. Following Koynov [190], the transmittivity diffraction grid of nanostructures is characterized by an average distance Δ between scatters. According to Bragg's equation, the direction of constructively interfering rays can be defined as $\lambda_{\mathrm{air}}/n_{\mathrm{Si}} = \Delta \sin(\beta)$ after passing the grid, where λ_{air} is the wavelength of the incident light in air $\lambda_{\mathrm{air}}/n_{\mathrm{Si}}$ and β are the effective light wavelength and the scattering angle within the Si layers, respectively. Efficient light trapping occurs for rays that enter the film (scattering angles $\beta < \pi/2$ in the direction of the incident beam) and reach the rear Si-air interface under angles β higher than the critical angle for total internal reflection. These assumptions are equivalent to the requirements $0 < \sin(\beta) < 1$ and $\sin(\beta) > 1/n_{\mathrm{Si}}$. Apply these conditions to Bragg's equation one could deduct

$$\lambda_{\mathrm{air}}/n_{\mathrm{Si}} < \Delta < \lambda_{\mathrm{air}} \tag{4.7}$$

Therefore, the efficient light trapping via diffractive scattering depends on the average distance between the scattering centers, i.e., black Si nanostructure peaks. The light absorption enhancement should occur at light wavelengths longer than the absorption edge of nanostructures layer, i.e., for typical Si layer with a thickness of ~1 μm in the range of $\lambda_{\mathrm{air}} \approx 700-1000$ nm. Thus, the best distance between the scattering structures on the surface of Si should be in the range of 150 nm$< \Delta <$1000 nm according to the Eq. (4.7). Spacing beyond this limit will be inefficient for light trapping by diffractive scattering. Smaller spacing leads to effective medium approximation, while bigger spacing (above 1000 nm) to geometrical ray optics [203]. According to Fig. 4.10, the spacing between the secondary features of the black Si films (pits and valleys spaced at 180 to 300 nm) match perfectly the favorable range. Such spacing resulted in rather high scattering angles (above the critical angle) that considerably increase the light path lengths, accounting for the near-perfect light trapping effects experimentally shown in the black Si nanostructures and reported in Fig. 4.13.

4.4.1   Optical properties of black Si

The spectral resolved reflectivity R and transmittivity T of the black Si were measured with Perkin Elmer Lambda 1050 UV/Vis/NIR Spectrophotometer in the wavelength range of 200-1100 nm. Figure 8 shows reflectivity, absorptivity and transmittivity spectra in the wavelength range of 200-1100 nm before Al$_2$O$_3$ deposition. The optical spectra change slightly after deposition of the thin Al$_2$O$_3$ layer. For comparison, a theoretical Yablonovitch limit [83] with the resulting absorptivity

$$A_{4n^2} = 1 - \frac{1}{1 + 4n_{\mathrm{Si}}^2 \alpha_{\mathrm{Si}} d} \tag{4.8}$$
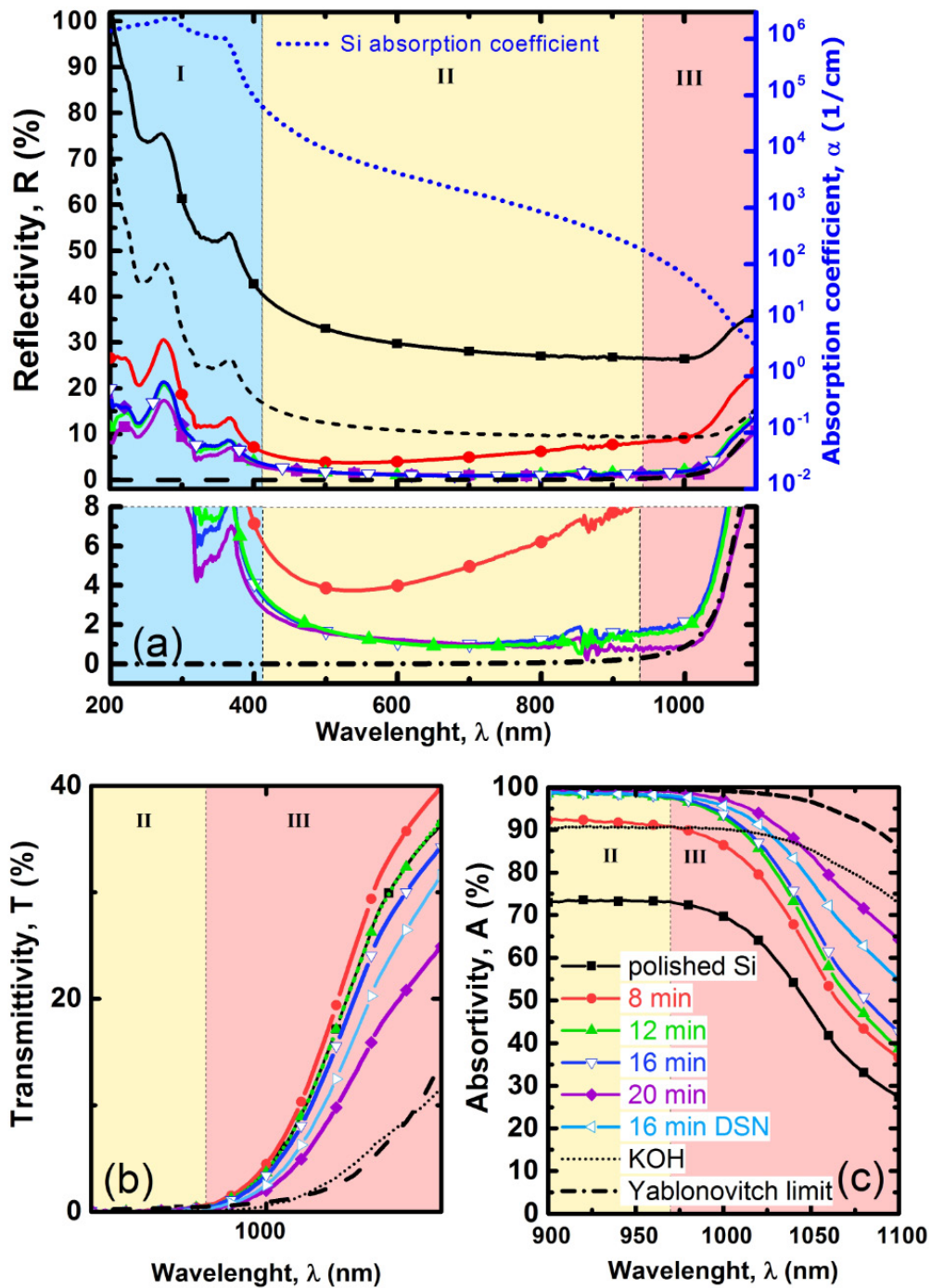
FIGURE 4.13: Measured optical properties of nanostructured black Si: (a) reflectivity, (b) transmittivity, (c) absorptivity. Note: the legend is valid for all three graphs

is also plotted. Here n_{Si} is a Si refractive index, α_{Si} is the absorption coefficient, and d is the wafer thickness.

Figure 4.13 (a) compares the total reflectance spectra of the polished (100) Si wafer, 8 min, 12 min, 16 min, 20 min, 16 min DS black Si textured samples with that of KOH-textured samples. The polished reference sample has around 30 % reflectivity, while the KOH-textured reference has the much lower average reflectance of ~8 %. All black Si (RIE) samples exhibit

very low reflectance in the 400-950 nm spectral range. Three regions were identified on the Fig. 4.13: I (UV), II (visible-NIR), and III (IR) regions. In region I (UV) all samples have a fluctuating reflectivity. These fluctuations are due to Si absorption coefficient fluctuations that agree with the reflectivity peaks. The sample etched for 8 min has a reflectance gradient in the 400-1000 nm range. The reflectivity gradient is analyzed based on the Si nanostructure shape, fraction and gradient refractive index shown in Figs. 4.10, 4.11 and 4.12 respectively. The nanostructures etched for 8 min have an average depth of 250-300 nm subject to transition from diffractive scattering to effective media conditions. This transition is especially important at increased wavelength (above 475 nm) and explains the increasing reflectivity shown in Fig. 4.13 (a) as the red curve. Most nanostructured samples, except those etched for 8 min, approach the Yablonovitch limit, particularly in the range from 450 to 1100 nm. In the case of the 16 min DS samples, low reflectivity is implied by conical nanostructures on both sides of the sample, while the 20 min samples have the lowest reflectivity due to enhanced surface morphology only at the front surface.

Figure 4.13 (b) illustrates the total transmittivity of the same set of samples. In general, transmittivity decreases for deeper nanostructures. The transmittivity for the sample etched for 8 min is higher than that of the reference polished Si sample. This is also valid for 12 min etched samples that overlap with the polished Si reference. On the other hand, KOH-textured samples have lower transmittivity almost in agreement with the ideal Yablonovitch limit. This effect can be explained by the 54.74^o angle of the KOH-etched facets.

The measured absorptivity and theoretical model are shown in Fig. 4.13 (c). Total internal absorptivity was calculated as $A_{\text{total}} = 1 - R - T$. The absorptivity spectra of all nanostructured samples follow similar trends to transmittivity measurements. The experimental absorptivity was compared with the theoretical model described above in Eq. (4.8) [204]. The highest absorptivity is reported for 20 min etch, and DS 16 min etch. However, the KOH-textured sample has higher absorptivity in the NIR region (red region) due to the front surface facets at an angle of 54.74^o. The absorptivity of the textured samples near the absorption edge, i.e., near the band gap of Si exceeds that of a polished wafer with perfect ARC and provides a light trapping effect due to light scattering at the black Si nanostructures.

4.5 Surface passivation of RIE black Si

4.5.1 ALD Al$_2$O$_3$ passivation scheme

Interfaces in crystalline silicon solar cell play a major role and if not passivated become the main reason for recombination and losses. Therefore, interface passivation is the key factor in achieving optimal device performance. Moreover, higher energy conversion efficiency. Passivation of nanostructured surfaces, i.e., black Si, becomes even more necessary since most nanostructuring processes induce additional damage to the surface and create interface defect. The ALD provides the solution and by application of various materials guarantees excellent interface passivation [205]. ALD Al$_2$O$_3$ passivation scheme provided the best chemical and enhanced field-effect passivation [168] based on different materials and their combinations in stacks.

Before the discussion of passivation schemes and results it is important to underline **requirements to passivation layers on black Si surfaces** summarized by Otto [90]. First, the

TABLE 4.3: Passivating carrier selective materials used in this work prepared
by ALD and their interface properties on c-Si [205]

ALD material or stack	T_{dep}	$D_{it}(*10^{11}eV^{-1}cm^{-2})$	$Q_f(*10^{12}cm^{-2})$	S_{eff}	Refs.
Al_2O_3	200	0.8	-5.6	2.8	[168]
SiO_2	200	10	0.6 [2]	25	[206]
SiO_2/Al_2O_3	200	1	-5.8-+0.6 [3]	3	[206]
TiO_2	100	n.a	negative	6.5	[118, 207]

TABLE 4.4: ALD Al_2O_3 process parameters suitable for high aspect ratio
nanostructures

| Precursor	Pulse time, s	N2 flow, sccm	N2 purge time, s
TMA	0.1	150	0.5
TMA	0.1	150	20
H_2O	0.1	200	0.5
H_2O	0.1	200	20

passivation materials should fit crystal orientation of c-Si and its doping level, provide excellent chemical passivation quality and induce strong field effect passivation. Second, nanostructured corrugated surfaces must be a highly conformal coating to avoid any pin-holes, inclusions or defects. Third, the coating should have minimal effect on optical properties of the nanostructures. Fourth, the highest ALD process temperature should be kept to avoid contaminants diffusion from the nanostructured surface into the bulk Si and to ensure complete ALD surface reactions. Fifth, silicon surface has to be cleaned, and the damage caused by etching process should be minimized [86].

In the Table 4.3 all the passivation schemes tested in this work were summarized. The passivation properties on both n- and p-type Si wafers with TiO_2 were presented in Chapter 3, while Al_2O_3 and SiO_2/Al_2O_3 stacks passivation schemes were presented in this Chapter. All the materials schemes above are well-known as a relatively high negative charge density dielectric. In the case of n-type wafers, negative surface charges repel majority carriers from the surface, leading to depletion or even inversion. Regarding p-type wafers, the high charge density leads to accumulation at the nanostructured surface; the effect of passivation due to charge was discussed by von Gastrow et al. [182].

Sample preparation and ALD passivation layer deposition

After the nanostructuring etching process, all samples were cleaned using the standard RCA procedure. Detailed RCA process parameters and steps could be found in [195, 208, 209]. Subsequently, wafers were coated with 380 cycles of ALD Al_2O_3 synthesized from TMA and H_2O mainly at 200 ^oC. Thus, for research purpose ALD deposition processes were conducted at 120 ^oC, 150 ^oC and 200 ^oC. For references, two polished Si wafers (p- and n-type) were also included in the ALD Al_2O_3 passivation process. ALD method parameters are given in Tab. 4.4 and details on chemical reaction are described below in Eqs. (4.9)-(4.11).

Puurunen et al. [143] gave a detailed description of the reaction mechanism in 2005. The deposition process is based on chemical sequential reactions as shown below:

$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2 + (CH_4) \uparrow \tag{4.9}$$
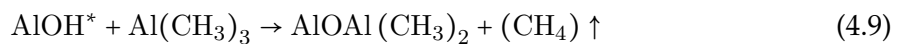
After the first half cycle is done, the surface is passivated by CH_3 groups. Next, the purge step removes the excess of TMA and methane, the next reaction step is

$$Al\left(CH_3\right)_2{}^* + H_2O \rightarrow AlOH^* + \left(CH_4\right)\uparrow \tag{4.10}$$

Here, H_2O reacts with CH_3 groups, while CH_4 leave the chamber and monolayer of Al_2O_3 is synthesized. The overall sequence is repeated until the film of required thickness is grown. The net reaction, therefore, is:
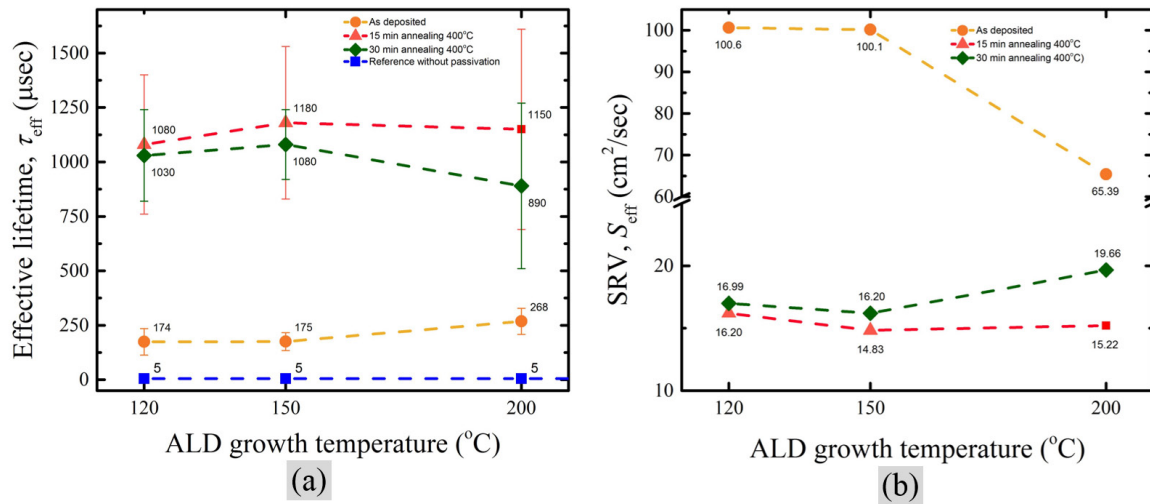
$$Al\left(CH_3\right)_2{}^* + 3H_2O \rightarrow Al_2O_3 + 3\left(CH_4\right)\uparrow \tag{4.11}$$
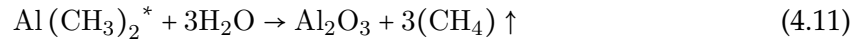
Post-deposition annealing

FIGURE 4.14: ALD Al_2O_3 passivation scheme development for films grown at 120 °C, 150 °C, 200 °C (a) effective lifetime τ_{eff} @10^{15} cm^{-3} injection level and (b) surface recombination velocity S_{eff}

ALD grown Al_2O_3 films, in the as-deposited state, demonstrate poor passivation quality [210, 211]. Additional post-deposition annealing at moderate temperatures around 370-420 °C or at 500 °C activate Al_2O_3 negative fixed charges [211] at the Si-SiO_2-Al_2O_3. Negative fixed charges affect silicon energy band bending and create either inversion (for n-type silicon) or depletion (for p-type silicon) region at the interface leading to decrease of interface density of states. Annealing or thermal activation of Al_2O_3 is essential for both field effect and chemical passivation schemes [212]. Annealing of the ALD deposited layers was conducted at 380-400 °C for 30 min and discussed in the Sect. 4.5.2. Annealing effect on ALD Al_2O_3 films is well studied by others [213, 214] and some of our results are presented in Fig. 4.14. However, the most significant results were obtained for samples annealed at 500 °C for 5 min in nitrogen or air ambient during. This conditions were used for annealing experiments and resulted into high effective lifetime presented in Fig. 4.16

4.5.2 Electro-optical properties of black Si

Effective lifetime of minority carrier on the passivated polished Si

The quality of surface passivation can be evaluated by measurements of effective lifetime of minority carrier on the passivated Si sample. In our study, the effective minority carrier lifetime τ_{eff} was measured using the MDP method in transient and injection dependent single point modes and the lifetime mapping mode using an MDP map setup from Freiberg Instruments and the quasi-steady-state photoconductivity (QSSPC) methods in an injection dependent mode with a Sinton WCT-120 Instrument.
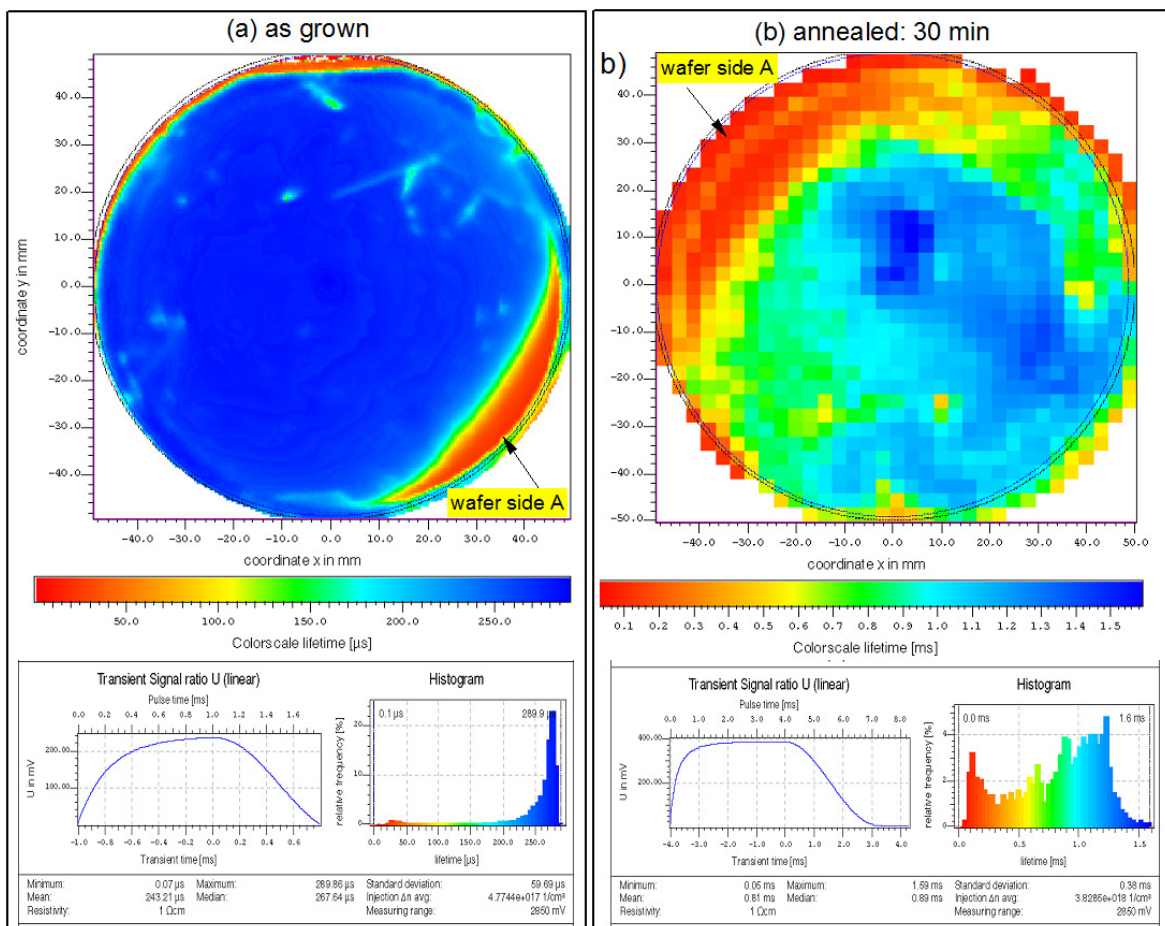

FIGURE 4.15: ALD Al_2O_3 passivation lifetime maps for samples (a) as grown at 200 °C and (b) annealed at 400 °C for 30 min

Based on the effective lifetime and the surface recombination velocity as a function of ALD deposition temperature, the best ALD Al_2O_3 passivation films were grown at 200 °C according to Fig. 4.14. SRV was calculated according to Eq. (2.61). ALD allows depositing highly conformal films. Film quality over the whole wafer was tested with lifetime mapping tool and presented in Fig. 4.15 only for 200 °C as grown (a) and annealed at 400 °C for 30 min (b). As one can see, the lifetime maps confirm conformality of Al_2O_3 films with some minor edge degradation. After annealing at 400 °C for 15 and 30 min the passivation quality of the film was improved, with preferred 30 min annealing, resulted to extremely high lifetime of 1800 μs for p-type silicon wafer and 16 cm^2/s for 200 °C grown films annealed at 400 °C for 30 min. Additionally, Fig. 4.15 contains insets for (a) as grown and (b) annealed for 30 min samples with transient signal ratio over transient time and histograms of effective

lifetime relative frequency over the lifetime map. This map data allows statistically estimate the quality of passivation over the whole wafer.
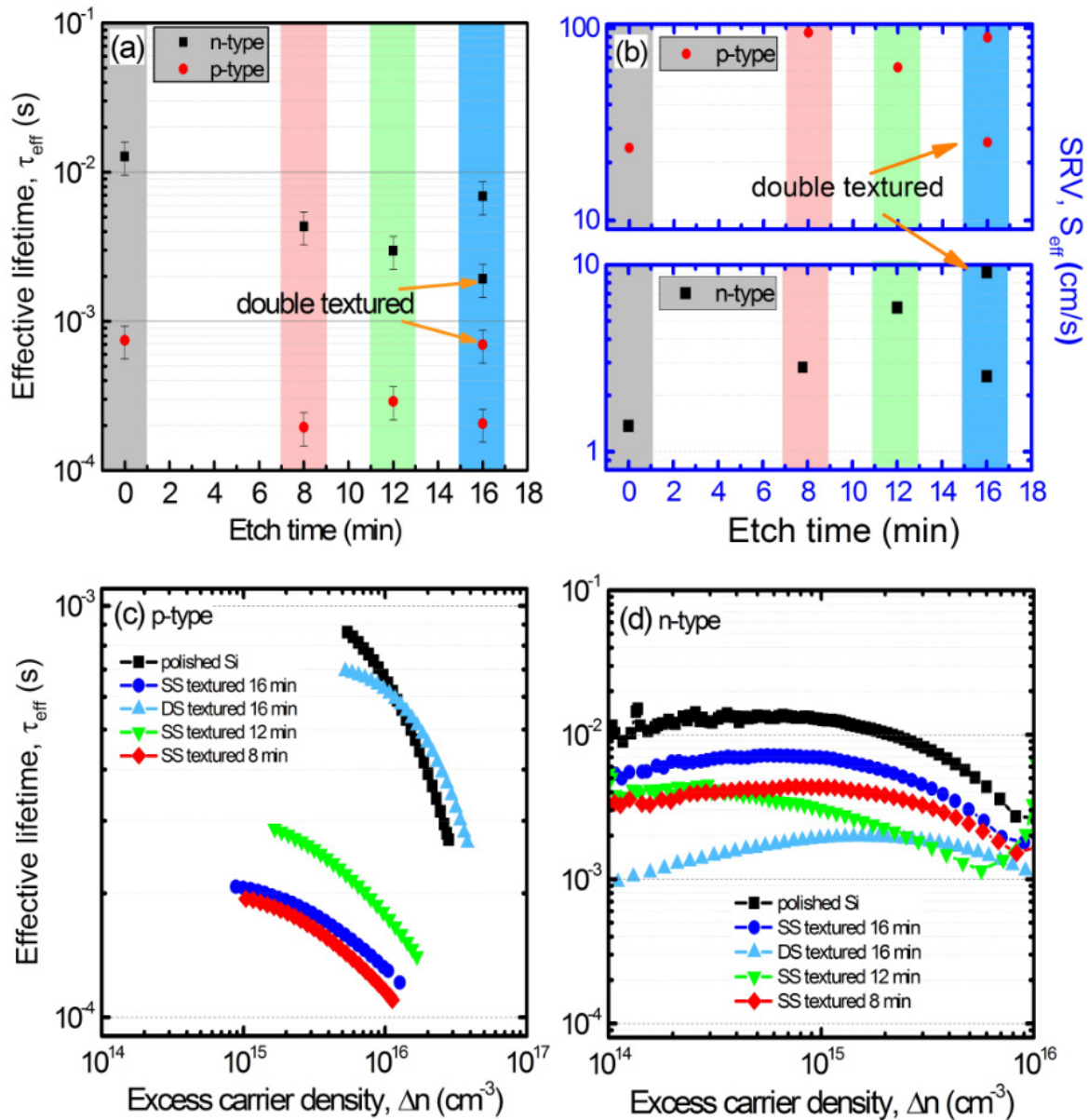

FIGURE 4.16: Measured effective lifetime (a) and surface recombination velocity (b) at an injection level $\Delta n = 10^{15}$ cm^{-3} and injection dependent effective carrier lifetime for (c) p-type and (d) n-type samples

Effective lifetime of minority carrier on the passivated black Si

Figure 4.16 (a) and (b) show etch time-dependent effective lifetime of n- and p-type samples. For polished Si samples τ_{eff}=12 ms for n-type, and τ_{eff}=800 μs for p-type Si were measured. For nanostructured for n-type samples, the best results were for 8 min etch τ_{eff}=4 ms, and for 16 min SS nanostructured τ_{eff}=7.5 ms, while p-type samples obtained τ_{eff}=400 μs for 12 min etch, and τ_{eff}=800 μs for 16 min DS textured samples. Figures 4.16 (c) and (d) display the effective minority carrier lifetime as a function of injection level for polished and nanostructured samples on p-type and n-type samples, respectively. The effective SRV S_{eff} was

determined according to Eqs. (2.59) and (2.61) and is shown in Fig. 4.16 (b). All n-type samples had extremely low S_{eff} values below 10 cm/s. The lowest value was for the polished reference samples (S_{eff} =1.5 cm/s), 8 min etch (S_{eff}=4 cm/s) and for 16 min SS textured (S_{eff} =3 cm/s) samples. The best results on p-type samples were obtained on the polished reference (S_{eff}=22 cm/s) samples; the 12 min etch samples (65 cm/s) and the 16 min DS textured samples (S_{eff}=25 cm/s). This difference in τ_{eff} and S_{eff} for n- and p-type samples is based on the inversion and depletion mechanism of electrostatic passivation of Si induced by ALD deposition of the Al_2O_3 layer. This scheme also worked well on DS textured black Si samples. It became possible with optimization of RIE process, i.e. with reduction of the CCP power. It was found that the optimal thickness for the Al_2O_3 layer was equal to 25-35 nm, which overlap with other referred report [214, 215] and provided excellent passivation quality without scarification of optical properties. The thickness of films was measured using ellipsometry [4] at 5-10 different spots on the samples. The Al_2O_3 layer had a thickness of 32 nm on polished samples for 350 cycles.

TEM and FFT spectroscopy of Al_2O_3 passivated black Si

To study potential damage occurring in silicon after a RIE process, conformality of the passivation layer on silicon and lattice match of silicon crystal place, the corresponding high resolution Transmission-Electron-Microscopy (TEM) measurement were conducted and presented in Fig. 4.17. Figure 4.17 illustrates a low magnification bright field TEM images, where a black silicon nanocone (Fig. 4.17 (a-e)) can be observed in dark grey, while ALD Al_2O_3 layer is observed as a lighter grey layer on top of Si base. TEM images confirmed that black Si nanocones uniformly passivated with 350 cycles of ALD Al_2O_3 and corresponded to 28-32 nm thick film. The Fast Fourier Transform (FFT) Spectroscopy in the Fig. 4.17 (f) shows that the the distance between silicon (111) plains was estimated 3.13 Å and absence of silicon plains damage. It means that the crystallographic structure of silicon was preserved during RIE process showing that RIE process is not harmful to the silicon surface. As a result, a good uniform ALD Al_2O_3 passivation was obtained with the high lifetime.

Evaluation of surface passivation: fitting the experimental data with theoretical model

To understand the effect of nanostructured surfaces on effective lifetime a simulation of effective carrier lifetime was conducted based on a conceptual model described by Onyshchenko et al. [216] and Ernest et al. [217]. The experimental data presented in Fig. 4.16 was analyzed and compared with a theoretical model as a fit in Fig. 4.18. The effective lifetime of minority carriers in black Si was calculated by the solution of the diffusion equation for minority carriers using models and methods of the lifetime calculation and the minority carrier distribution in macro-porous Si and c-Si [216, 217]. A system of equations includes the diffusion equation for minority carriers in a c-Si and boundary conditions. Black Si surface consists of cones and pyramids, which were divided into elementary cylinders. The elementary cylinders represented an effective medium and sewed to their bases. The stationary diffusion equation for minority carriers in elementary cylinders can be written as:

$$D_{\text{p}} \nabla^2 \delta p(x) - \frac{\delta p(x)}{\tau_{\text{eff}}} + g_{0p} exp(-\alpha x) = 0 \qquad (4.12)$$

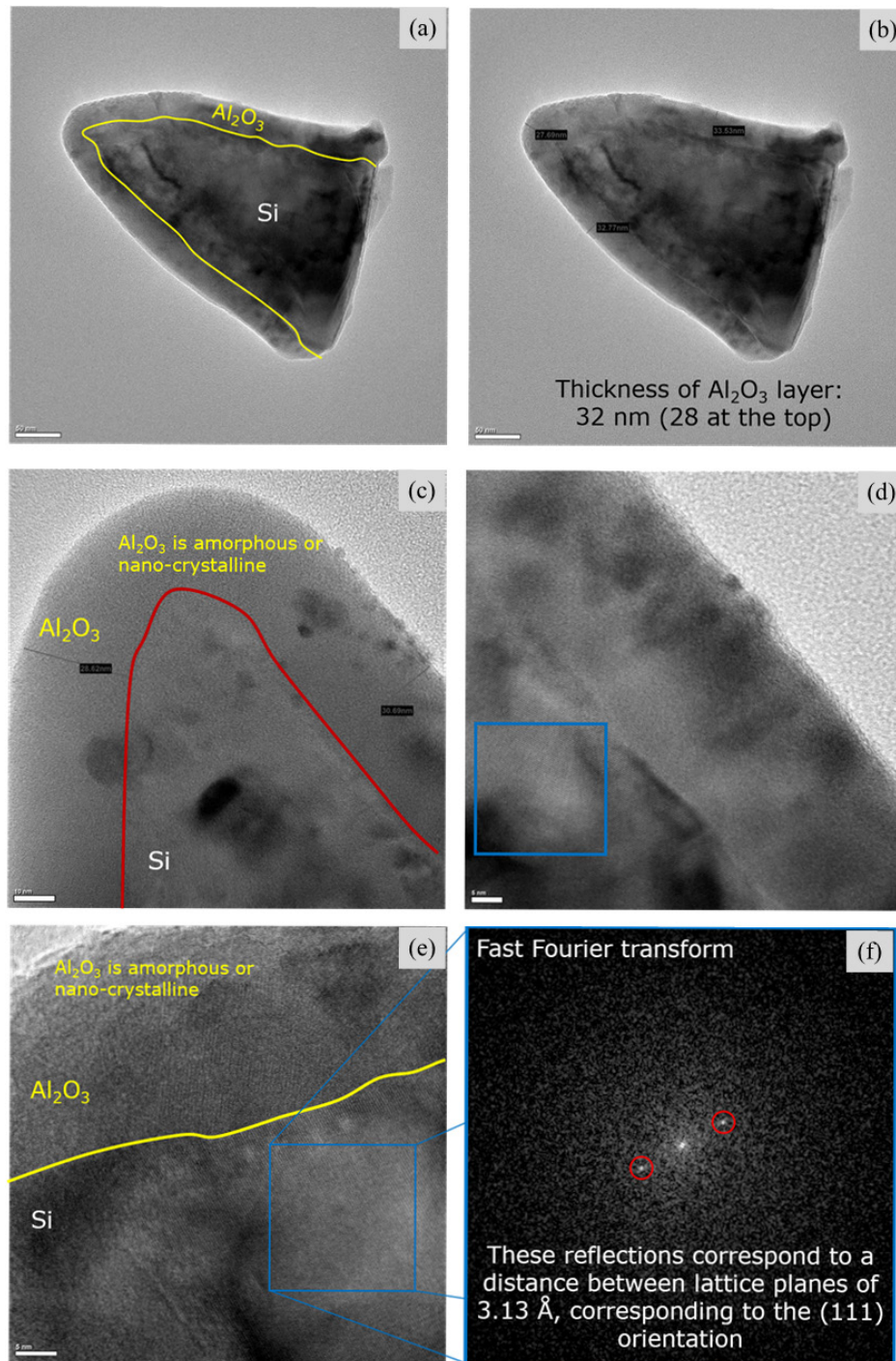[4]Spectroscopic ellipsometer VASE J.A.Woollam Co.

FIGURE 4.17: Transmission electron microscopy images of ALD Al_2O_3 passivation RIE black Si: (a)-(c) silicon nanocones coated with 28-32 nm Al_2O_3 with defined boundary between these two materials, (d)-(e) focus area (blue square) for Fast Fourier transform analysis, (f) Fast Fourier Transform analysis image confirming the lattice distance plains orientation. (Courtesy to Beniamino Iandolo)

where D_p – the hole diffusion coefficient, $\delta p(x)$ - the extra hole concentration, α - coefficient of light absorption of silicon, g_{0p}– bulk generation of excess holes, τ_{eff} – the effective minority carrier lifetime in elementary cylinder defined by the Eq. (4.12) according to [216, 217]. Stationary equation of the minority carrier diffusion in c-Si similar to Eq. (4.12), but it needs to put the volume lifetime instead the effective one. Boundary conditions are determined taking into account the balance of the excess carriers on the surface:

$$g_{\mathrm{s}} = \frac{j_p(x_{\mathrm{i}})}{q} + S_{\mathrm{p}}\delta p(x_{\mathrm{i}}) \tag{4.13}$$

where q – electron charge, g_{s} – speed of the surface generation of the excess charge carriers, δp - density of the hole current at the surface, S_{p} – surface recombination velocity for holes, $\delta p(x_{\mathrm{i}})$ – the concentration of excess holes on the surface, x_{i} – coordinate of the selected surface. Effective lifetime was obtained as follow:

$$\tau_{\mathrm{eff}} = \frac{1}{hg_{0p}} \int_0^h \delta p(x)dx \tag{4.14}$$

where h is the sample thickness.

For the numerical calculations, presented in Tab. 4.5, the data presented in Fig. 4.16 was used. The thickness of the polished c-Si and black Si wafer were 350 μm for n-type and p-type silicon, the injected carrier concentration was $5 \cdot 10^{15}$ cm^{-3}.

TABLE 4.5: Characteristics of polished and black Si nanocones

	$\tau_{\mathrm{s}} = \tau_{\mathrm{eff}}$, ms*	S_{eff}, cm/s*	S_2/S_1	τ_b**, ms	τ_s**, ms	s**, cm/s	S_2**/S_1**
n-Si	5.64	4.17	1	30	6,95	2.67	1
n-bSi	1.55	15.16	6.28	30	1.63	2.67	7.14
p-Si	1.24	19	1	1.75	4,26	4.35	1
p-bSi	0.75	31.3	2.31	1.75	1.32	4.35	9.65

*The values obtained experimentally and presented in Fig. 4.16.
**The values obtained by numerical calculations account the bulk lifetime.

The effective minority carriers lifetime and SRV for the polished wafers and black Si wafers are given in the Tab. 4.5.

To estimate relation between the concentration of recombining carriers on the side of the black Si and the polished side the following equation was applied:

$$\frac{S_2}{S_1} = \frac{2S_{\mathrm{eff}}(bSi)}{S_1 - 1} \tag{4.15}$$

where $S_{\mathrm{eff}} = h/(2\tau_{\mathrm{eff}})$, $\tau_{\mathrm{eff}} = \tau_{\mathrm{s}} = h/(2S_{\mathrm{eff}})$, $2S_{\mathrm{eff}} = S_1 + S_2$. Value S_1 is SRV on the polished side of black Si wafer. Value S_2 is marked SRV on the black Si side and S_{eff} (bSi) is effective SRV on the black Si at all. The relation S_2/S_1 is more than 6 for the black Si n-type wafer, whereas for p-type this relation is 2.3 according to Tab. 4.5.

Using numerical methods, models and techniques presented in [216, 217], the volume lifetime τ and the SRV S were fitted to the effective lifetime τ_{eff} of a polished Si wafer and black Si one. For black Si the distance between cylinder centers is 0.13 μm, the cylinder diameter is 0.11 μm, the cylinder height is 0.5 mm for black Si according to Fig. 4.16. In addition, instead

of the black Si square pyramids the base instead cylinders were considered. The pyramid height is equal to the cylinder one, the distance between pyramid centers is equal to the distance between cylinder centers. The base side of the pyramids is equaled to the cylinder diameter. The bulk lifetime for c-Si wafer and black Si were the same. The obtained τ_{eff}=0.03 ms for n-type Si and 1.75 ms for p-type Si (the concentration of excess carriers $5 \cdot 10^{15}$ cm^{-3}) were calculated by numerical methods and models presented in [216, 217]. The estimated rate of SRV on the material surface was of 2.67 cm/s for the n-type Si and 4.35 cm/s p-type one, taking into account the same rate of surface recombination for single crystal wafer and black Si (Tab. 4.5).

The SRV on the black Si n-type surface is 7.14 times higher than SRV on polished surface (see Tab. 4.5). This result is not different much from the calculations with valid values neglecting the volume lifetime. At the n-type black Si volume lifetime is higher (30 ms) and therefore it does not affect the effective minority carriers lifetime. At the same time, the SRV for the p-type black Si nanocones is 9.62 times higher than for polished one and higher S_2/S_1= 2.31 calculated for the effective values. In the last case, the volume lifetime plays an essential role in the charge carrier recombination. The table also contains also the lifetime of minority carriers on the surface, which shows the impact of the entire material surface on recombination processes.

The volume lifetime τ_{b} and the minority carrier lifetime τ_{s} are high in polished n-type c-Si indicating as volume and surface material purity. However, the table data show that the effective lifetime τ_{eff} is a little less than τ_{s}. In n-type black nanocones Si the effective lifetime τ_{eff} and the surface lifetime τ_{s} are almost identical. So very pure material volume does not influence on recombination processes. The minority carrier lifetime of in polished p-type bulk Si is lower than the surface lifetime τ_{s}, this indicates that the concentration of surface recombination centers is less than the volume one. The effective minority carrier lifetime of a p-type black Si is lower than the volume lifetime τ_{b}.

The effective minority carrier lifetime was presented as a dependence of the diameter of the cone base D_{c}, the base of the pyramid sides L_{p} on the height of cones H_{c} and pyramids H_{p}. Figure 4.18 presents these dependencies for n-type (a) and p-type (b) of black Si: the diameter of the cone base diameter D_{c} (curve 1), the base of the pyramid sides L_{p} (curve 2), the height of cones H_{c} (curve 3) and pyramids H_{p} (curve 4). The effective minority carrier lifetime are presented in Fig. 4.18 for black Si (see Fig. 4.16 and Table 4.5) for the diameter of the cone base D_{c} 0.11 μm (curve 1) and for the height of the cone 0.5 μm (curve 3).

Figure 4.18 shows that the effective minority carrier lifetime in the black Si wafer with cones (curves 1 and 3) is higher than the effective minority carrier lifetime on the surface with pyramids (curves 2 and 4). The effective photo carrier lifetime in the black Si wafer sharply decreases (curves 1, 2) with increasing diameter circle base of the cone, the sides, and base of the pyramid height difference between life times in the black Si cones and pyramids grows (curves 1, 2 and 3, 4). The effective lifetime of minority carriers in the silicon wafer heights curves sharply decreases (1), (2) with the cone diameter and the pyramid base increasing at the height of the cone or pyramid 0.5 μm. The effective photo carrier lifetime changes slightly at 0.05 μm, then abruptly drop at 0.2 μm and then gradually saturates at 0.5 μm (curves 1, 2 from Fig. 4.18 (b). Saturation is not observed in Fig. 4.18 (a), it will come at higher heights of cones and pyramids.

Experimental data for nanocones in Fig. 4.18 (signs) are in good correlation with calculations of the effective lifetime of minority carriers taking into account the volume recombination velocity 2.67 cm/s for n-type silicon and 4.35 cm/s for p-type silicon (Table 4.5). The same
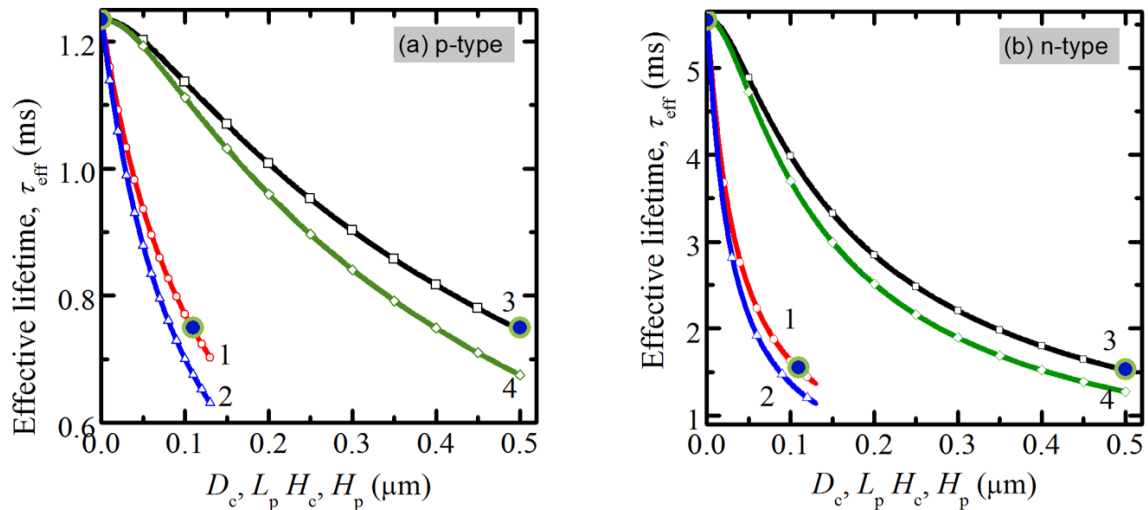
FIGURE 4.18: The dependence of the effective minority carrier lifetime from the shape of nanostructures: the cone diameter circle (1), the parties base of the pyramid (2), the height of the cone (3) and pyramid (4) for n-type (a) and p-type (b) black Si; circular big signs – experimental data from Fig. 4.16.

lifetime one can obtain for pyramids at 7-8 times lower the base square and 1.4 times lower heights in comparison with cones.

4.6 Doping of nanostructured surfaces

4.6.1 Introduction

The doping process of nanostructured black Si is different from doping of planar and other textured surfaces [218] due to the higher surface area of black Si nanostructures. Black Si to planar area ratio is in the order of 5 to 10 (see Fig. 2.5) that potentially leads to higher doping density, faster diffusion and modified p-n junction and emitter properties. To investigate phosphorous doping of nanostructured RIE black Si, the doping of planar and KOH textured samples were compared. Experiments were carried out in a Tempress diffusion furnace with $POCl_3$ dopant source. The diffusion furnace principle is illustrated in Fig. 4.19. It is ultra-purity horizontal oven capable of temperatures from 600-1200 °C and a simple gas distribution system capable of introducing O_2, H_2O, N_2 or dopant gas or vapor. In practice, such systems are far more complex because of the need for uniformity, reproducibility, and cleanliness in the process.

Gases from these liquid sources are carried to the furnaces through high-purity stainless steel lines. For boron p-type doping BCl_3 gas is used while for phosphor n-type doping $POCl_3$ is used.

Doping level and recombination properties are characterized by sheet resistance and effective carrier lifetime measurements. A schematic of the doping process on different surfaces, including plain, KOH etched pyramids, and black Si is shown in Fig. 4.20.

Doping is dominated by Fick's first law: The diffusion is driven by the concentration gradient. C is concentration, D is diffusivity, and F is flux.
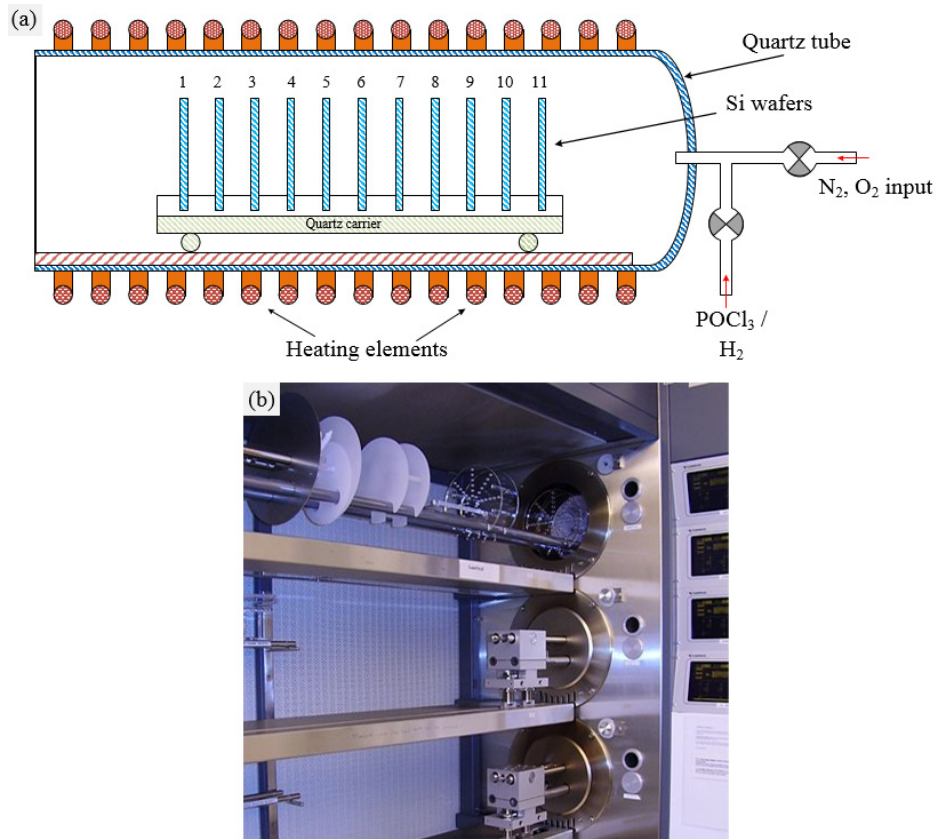
FIGURE 4.19: High-temperature oxidation, doping and oxide annealing furnace. (a) Schematics of the furnace, (b) photoimage of one of the stack of furnaces in Danchip cleanroom

$$F = -D\frac{\partial C}{\partial x} \qquad (4.16)$$

Moreover, together with Fick's second law: "... the divergence of the flux *F* gives the rate at which the concentration in a unit volume is being depleted" - [195], one gets the diffusion equation.

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \qquad (4.17)$$

This equation can be solved for simple symmetric cases, such as an entirely flat plain. This gives us a relation between the doping, *Q*, and the diffusion coefficient, *D*.

$$Q = C(x,t)\sqrt{\pi D t}\exp\left(\frac{x^2}{4Dt}\right) \qquad (4.18)$$

The diffusion coefficient for common impurities is found to depend exponentially on temperature as such, [195]

$$D = D_0 \exp\left(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right) \qquad (4.19)$$
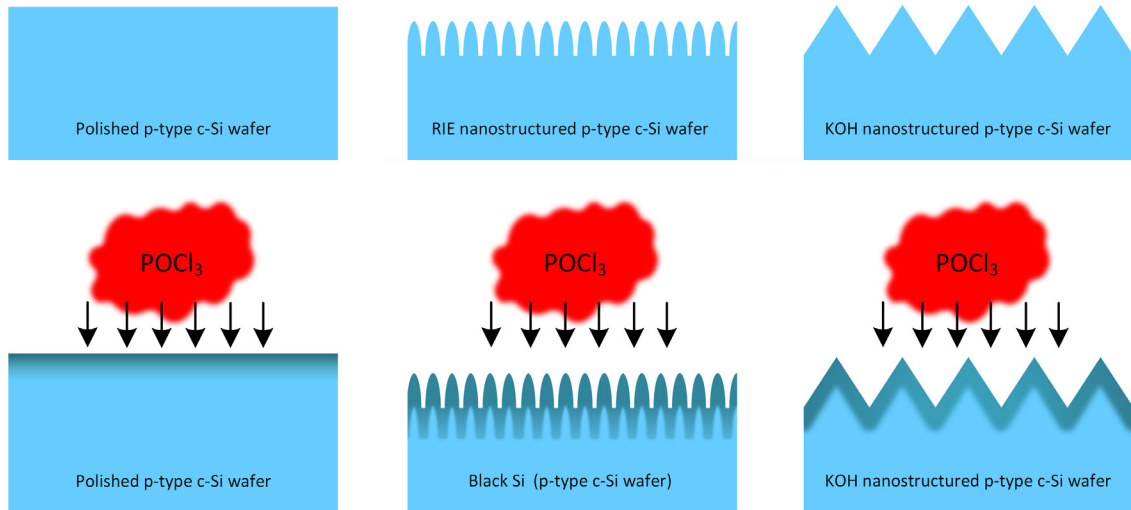
FIGURE 4.20: A schematic of the doping process on plain, KOH etched and black Si surfaces

This means that the doping is

$$Q = C(x,t)\sqrt{\pi D t}\exp\left(-\frac{x^2}{4Dt}\right) \propto \exp\left(-\frac{E_A}{2k_B T}\right) \tag{4.20}$$

The resistance has a dependence on, electron charge q, mobility μ_n and μ_p, and the doping Q_n and Q_p, [195]:

$$\rho = \frac{1}{q\left(Q_n\mu_n + p\mu_p\right)} \approx \frac{1}{qQ_n\mu_n} \tag{4.21}$$

Phosphor doping induces dominantly n-type doping in the wafers that compensate p-type dopants. The relation between resistance ρ and sheet resistance is [195]:

$$R_\square = \frac{\rho}{x} \tag{4.22}$$

where x is the thickness of the layer level. This layer thickness depends on the doping length, and it varies with approximately

$$x \propto \sqrt{Dt} \propto \exp\left(-\frac{E_A}{2k_B T}\right) \tag{4.23}$$

Moreover, the last parameter that also has a dependence on the furnace temperature T is the carrier mobility, by the same factor. Then, the temperature dependence of sheet resistance would be

$$R_\square \propto \exp\left(\frac{E_A}{2k_B T}\right) \tag{4.24}$$

4.6.2 Doping procedure

To understand the doping effect on electrical properties on the Si surfaces, different parameters were modified in a design of experiment. Wafer type, furnace temperature, and actual doping times were investigated with RIE black Si, KOH etched Si, and plain Si wafer samples. The process temperatures selected for experiments were 850 ºC, 900 ºC, 950 ºC, 1000 ºC, while the doping time was chosen to test for 15 min and 20 min.

The black Si was processed in DRIE setup according to the procedure described in Subsect. 4.2.1. The KOH etched wafers were prepared according to the procedure described in Subsect. 4.1.3. Important to note that the plain wafer and the black Si textured were on different sides of a single wafer. All the wafers were RCA cleaned as a requirement for the predep phosphor furnace. Each experiment was carried out with the black Si, plain, and KOH wafers and one set of temperature and time simultaneously. The black Si and KOH etched samples were placed into the furnace with a textured side toward the gas inlets, facing the flow direction. The distance between wafer samples was around 5 cm. An exception experiment was conducted at 850 ºC for 15 min to test a flow direction on 4 wafers. Two placed the same way as described above, and two other at the middle in different face directions.

All the wafers were annealed in oxygen and doped at the same temperature for 20 min. After that, the wafers were dipped into bHF solution for 2 min to remove the oxide layer. The measured oxide thickness was maximum of 105 nm, and with bHF having a SiO_2 etch rate was 75-80 nm/min [219]. To measure of the sheet resistance a four-probe measurements on the wafers were conducted. 5 different sheet resistivity position measurements were done on each wafer within ±2 cm from the center. An observation was that the sheet resistance was very homogeneous in the center, and less so on edge (~1 cm from the edge). However, this could also be the result of the geometry for the four probe measurement changing. No numbers of significance were recorded for the edge.

4.6.3 Results and discussions

The sheet resistance data for all the wafers at different temperatures and doping times are shown in Fig. 4.21. The error-bars represented one standard deviation of the sheet resistance measurements. For most of the values, the error bars were smaller than the actual dots to represent them.

There were six cases where the error-bars were larger than the dot sizes. For the 15 min, for temperatures 850 ºC and 900 ºC, for all types, there were fewer measurements, because of a planning error. This gives a higher uncertainty of the measurements. The depth of four-point probe measurement is limited to the thickness of the doping layer. This depth of the layer depends on the time and temperature of the furnace when the doping is done. It means that to get the accurate doping, the doping depth should be measured. Due to failure of of SIMS setup the depth of doping layer was estimated according to experiments details and simulation model.

From the theory, it was expected that the sheet resistance should decay with doping and that the doping increased with temperature and time in the furnace. However, the theory states that the general tendency of the system should be exponential increasing, with the inverse of temperature. The theory also predicts that the doping is proportional to square root of time, and since the sheet resistance is proportional to the inverse of doping. See Figure 4.22.
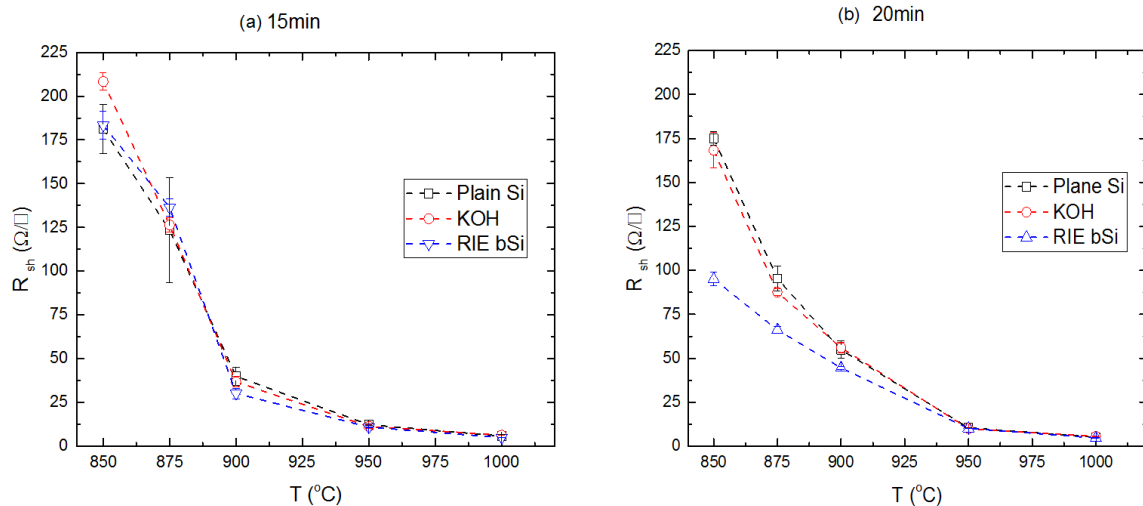
FIGURE 4.21: Sheet resistance versus temperature for plain silicon, KOH etched and black Si (bSi) samples: (a) doped for 15 min and (b) doped for 20 min. Also notice that there are error-bars on all the measurements, but that in most cases the error-bars are smaller than the actual dot sizes
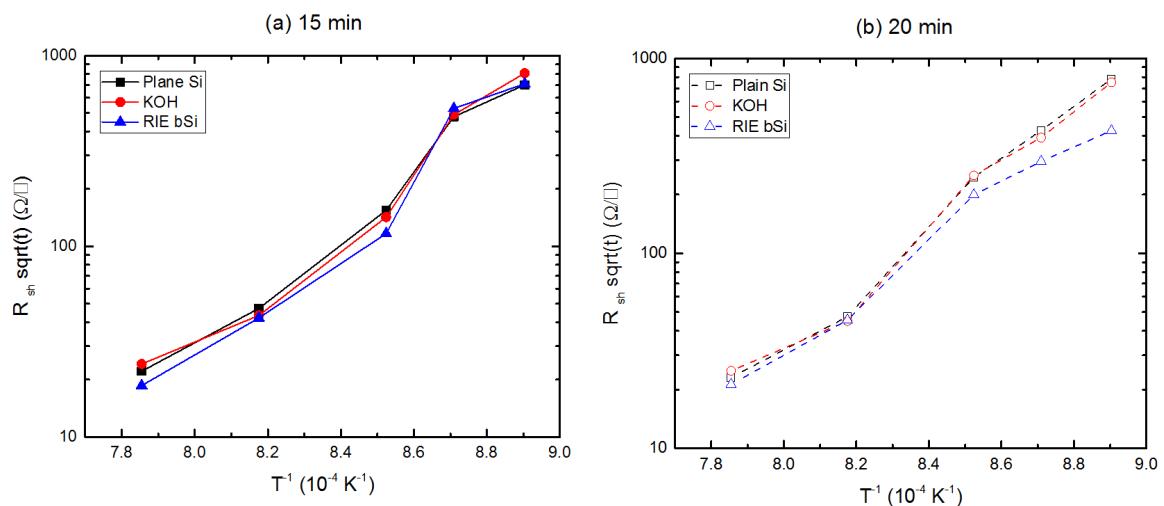

FIGURE 4.22: Semilog plot of sheet resistance times square root time versus inverse temperature in Kelvin: (a) doped for 15 min and (b) doped for 20 min

In Fig. 4.23 sheet resistance differentials between the different surfaces are shown as a function of doping temperature. In particular, for 20 min doping time it appears that the sheet resistance obtained on black Si is lower as those of the other two surfaces, which are very similar in sheet resistance value. Data from the 15 min experiment does not show the same unique tendency, perhaps because of lower total dose, which makes sheet resistance measurements more difficult and more prone to error.

Minority carrier lifetime measurements of the doped plain, KOH etched and RIE black Si surfaces. The measurements of effective minority carrier on doped samples was used MDP method. The resulting lifetime is shown in Fig. 4.24 may be a result of Auger recombination. Auger recombination is most likely the dominant process, since the emitter are relatively highly doped at the interface at lower temperatures (850 $^{\circ}$C) and further decreases for
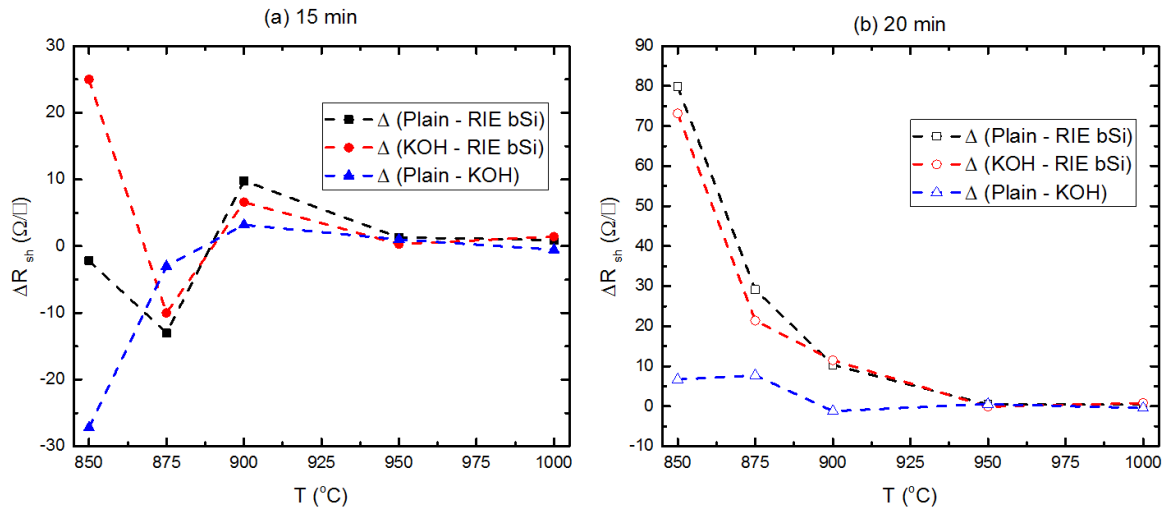
FIGURE 4.23: Sheet resistance difference between planar–KOH, planar–bSi and KOH–bSi samples depending on doping temperature and time: (a) doped for 15 min and (b) doped for 20 min

black Si compared to KOH-textured and plain Si due to even higher dopant concentration and therefore higher Auger recombination in higher doped emitters.
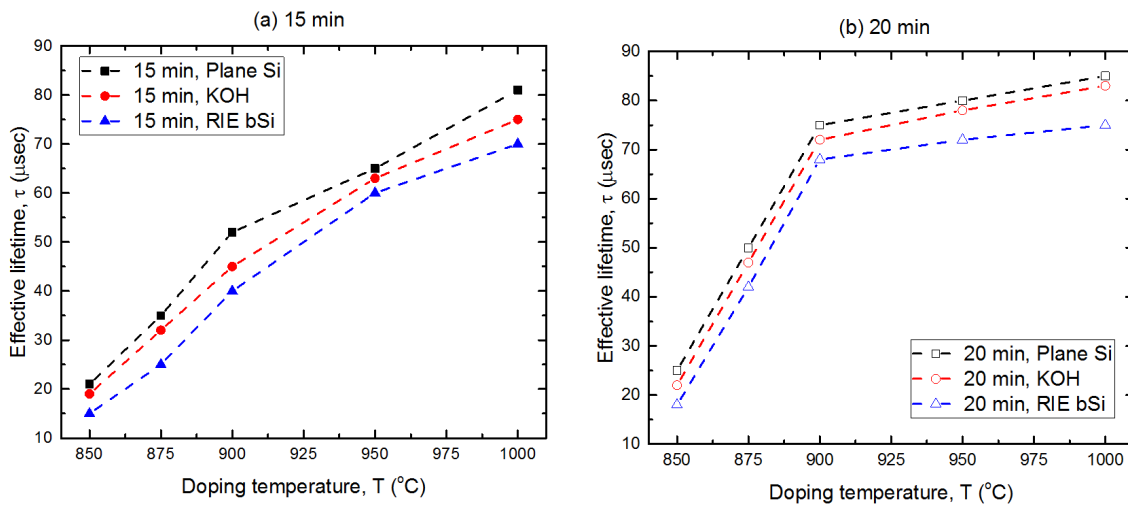

FIGURE 4.24: Minority carrier lifetime measurements of doped plain, KOH etched and black Si surfaces

Athena Silvaco doping process simulation.   To verify the results and investigate the observed differences may be explained solely by differences in the surface area and topology; simulations were carried out using the Athena Silvaco software. A simple phosphorus diffusion model was used, in which the dopant concentration was assumed constant and equal to the solid solubility at the Si surface. Defect-induced diffusion was not taken into account. The results in Fig. 4.25 confirms the experimentally measured tendency that sheet resistance is significantly lower on black Si to planar silicon. The relative difference in resistance between black Si and planar varies between 12 and 26 % for the 9 diffusion process simulations. The junction in all cases is deeper for black Si compared to planar Si. This shows that the

lower sheet resistance is not due to higher carrier density on a surface but also in a deeper junction.
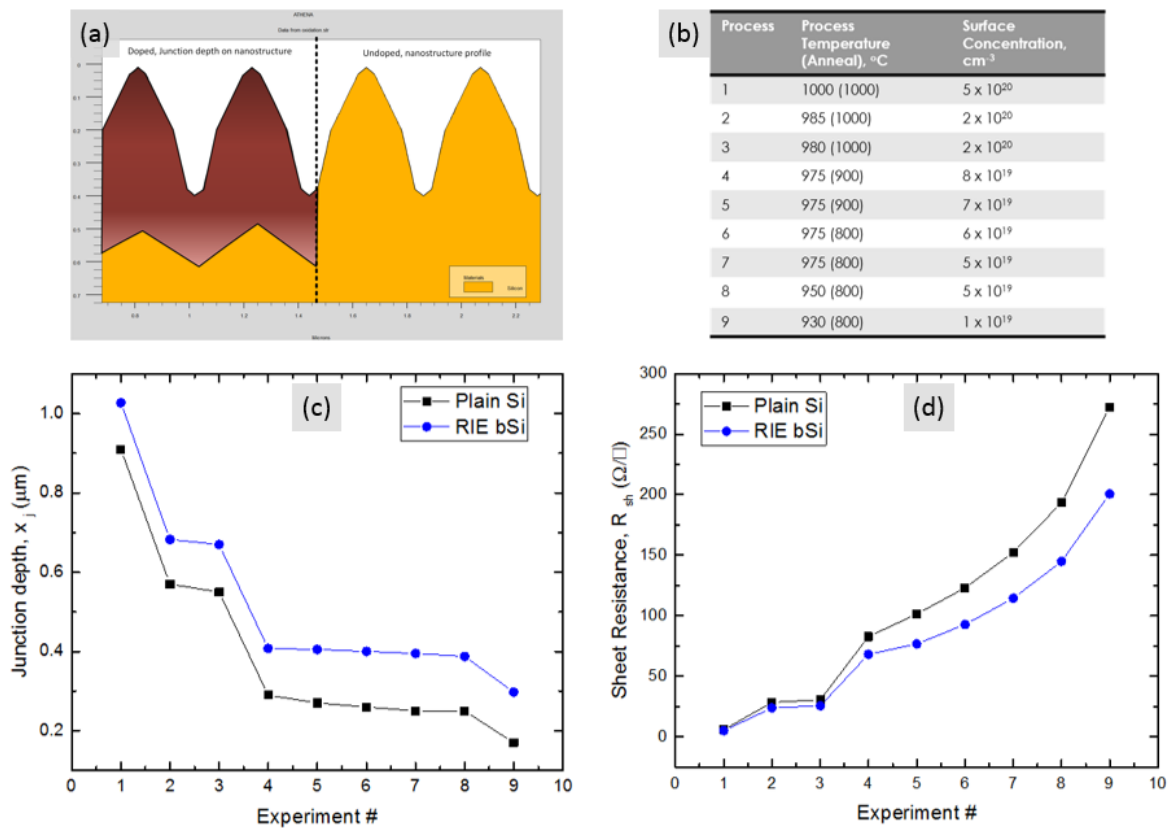
FIGURE 4.25: Athena simulation of the phosphorous doping process on plain and black Si surfaces: (a) Athena cross-section profile of the black Si surface, (b) a table with estimated surface dopant concentration, (c) junction versus experiments and their process temperature and (d) simulated sheet resistance versus experiments and their process temperature

In general, the doping experiment demonstrated that nanostructured surfaces tend to have lower sheet resistance and therefore higher doping concentration in comparison to planar and KOH structured Si. With geometrical calculations and simulations, the higher surface aspect ration caused higher doping and deeper junction. Due to dominating Auger recombination, doped black Si had a lower lifetime. To achieve the same order of doping as on planar surfaces, black Si doping process should be optimized.

4.7 Conclusions

By comparing different texturing methods (MACE, KOH-etched pyramidal surfaces, and RIE black Si) and their optical properties, passivation properties element analysis, it became apparent that black Si was the least reflective surface, almost by a factor of two compared to MACE, and around 7 times less reflective than KOH. EDX analysis of MACE samples confirmed the presence of Au contamination traces. Au is the element that supports mid-gap trap assisted recombination in Si. Therefore, it could not be used further until more effective cleaning procedure for MACE samples could be implemented. The further doping experiments were conducted on only KOH etched and RIE black Si samples. RIE black Si

method, on the other hand, was in the main focus of this thesis due to its unique optical and electronic properties and its potential to replace conventional texturing methods, such as alkaline etching. Low optical reflectivity and excellent passivation quality are key factors for black Si use in photovoltaics. The low reflectance and good surface passivation was possible to obtained with low CCP power used for black Si nanostructuring. it was found that lower CCP power (~10 W) reduces surface damage and improves effective minority carrier lifetime. The resulting nanostructures led to almost ideal reflectivity below 1 % approaching Yablonovitch limits in the visible and NIR ranges. With ALD Al_2O_3 passivation films deposited on a native oxide interlayer, the remarkably high effective lifetime of 12 ms for polished wafers, 4 ms for 8 min etched, 7.5 ms for 16 min etched on SS nanostructured n-type samples; and 800 μs for polished wafers and 400 μs for 12 min etch and 800 μs for 16 min DS nanostructured p-type samples were obtained. Effective SRVs below 10 cm/s were obtained, with the lowest value for polished reference samples (1.5 cm/s), while slightly larger values resulted (4 cm/s for 8 min etch and 3 cm/s 16 min etch) on SS nanostructured n-type samples. On p-type samples higher SRVs were measured (65 cm/s for 12 min etch and 25 cm/s for 16 min DS nanostructured sample). These findings show that high effective lifetime values can be obtained on both SS and DS nanostructured surfaces. Thus the use of black Si in the fabrication of high-efficiency Si solar cells is very promising.

The numerical calculation shows that n-type polished side and black Si side of c-Si wafer had high volume lifetime and minority carrier lifetime, indicating a high purity of material volume and surface. However, the surface lifetime was less than the volume lifetime of minority carriers. So the measured experimentally effective lifetime of minority carriers was determined by the surface lifetime. The minority carrier lifetime in the black Si wafer was compared with a volume one. The surface lifetime reduced three times faster in the n-type polished and black Si due to high volume and surface lifetime. An experimental lifetime of minority carriers for cones was in good correlation with calculations of the effective lifetime of photo carriers taking into account the volume n- and p-type SRV. The same lifetime one could obtain for pyramids at lower sizes in comparison with cones.

It was observed that textures with higher surface area obtain higher doping concentration. The black Si was observed with the highest doping level in comparison to plain and KOH pyramidal textures doped at the same temperatures. The KOH and plain were comparable in sheet resistance, but the KOH was more doped, having a lower resistance. Also, the experiments were compared with the theory and gave a general linear behavior when plotted on a semilog plot versus the inverse of the temperature. However, the theory that the doping was inversely proportional to the square root of time remains inconclusive, because of too few data points. While this data seems to stay consistent, it is a well-known thing that it was hard to get the same level of sheet resistance, of different wafers, of different batches. It is also important to remember that the error bars here were a representation of the sheet resistance measurements and not the actual variation for multiple samples. Variation from sample to sample could be much larger than these error bars. However, these results can be used as a rough guideline for estimating the sheet resistance for future projects with doping of these nanostructures.

Chapter 5

Outlook and Guideline for Future Work

"Words do not, cannot mean all that they stand for, yet they are all we have to describe experience."

Roald Hoffmann, from the talk at Noble Prize Award Ceremony, 1981

In Chapter, the final key points are presented regarding the experimental results, including the experiments with TiO$_2$-Si heterojunction diode and passivation and light trapping nanostructures with focus on RIE black Si light trapping and passivation optimization. In addition, brief overview of experimental work on NiO-Si heterojunction, ALD AZO and fabrication of TiO$_2$-Si-NiO heterojunction solar cells with carrier selective contacts and textured surfaces are also given. These additional section on NiO, AZO and TiO$_2$-Si-NiO solar cell fabrication are not represented as separate chapter due to a need for more detailed analysis of obtained results.

5.1 Outline on the main results

The key target of this work was to investigate the potential of SHJ solar cells with metal oxide selective contacts. Such contacts can revolutionize the photovoltaic industry, reduce the budget and improve performance for higher efficiencies. The key finding from this project resulted in several publications and are summarized in Chapter 3, 4, and in this Chapter as an outline of conducted experiments and attempts.

In **Chapter 3**, the comprehensive experiments, simulation, design, and optimization of TiO$_2$-Si structures with and without SiO$_2$ and Al$_2$O$_3$ interlayers for applications in heterojunction Si solar cells were presented. The TiO$_2$-Si structure for passivation and carrier-selective properties have been studied. The results suggest that TiO$_2$ and interlayer growth condition, surface passivation, TiO$_2$-Si energy band alignment, and the quality of interfaces play a major role in determining the performance of heterojunction devices. Consequently, the following key factors, which improved the performance during fabrication of TiO$_2$-Si passivating carrier-selective contacts, were determined as following:

ALD temperature affected the passivation and diode properties of the TiO$_2$-Si devices. Low-temperature-grown TiO$_2$ films possessed much higher passivation quality owing to the continuous amorphous film. At higher temperatures, the TiO$_2$ films formed preferentially in the anatase phase with increased roughness. At 80 °C, the V_{OC} had low value equal to 275 mV. V_{OC} values increased either with the higher ALD growth temperature at 100-150 °C or with annealing at around 200 °C. Above 250 °C, the growth or annealing processes

had a detrimental effect on passivation and diode properties. This effect was caused by the modification of the TiO_2 surface morphology, anatase crystal grain formation, and change in stoichiometry in TiO_2 films.

Therefore, it is suggested in this work growing TiO_2 films at low temperature (80 °C) and further annealing at 200-250 °C for 10 min in order to obtain carrier selective and passivation properties. These conditions allow transforming amorphous film to the anatase phase. Such treatment allows improving the lifetime even further and increasing V_{OC} without degradation of TiO_2 film quality.

Interlayers such as SiO_2 and Al_2O_3 markedly improve passivation quality by the factor 3-10. Note that Al_2O_3 interlayers show a significant enhancement of passivation properties. However, the nature of this phenomenon has not yet been investigated. Simulation predicts that TiO_2 with the high carrier density is a favored candidate. Despite the increase in carrier lifetime for TiO_2 with interlayers (SiO_2 or Al_2O_3), the $J - V$ performance has not improved for the metallized test structure used in this work. In contrast, mild degradation is observed for the case of the TiO_2 film with low carrier density when compared with that without interlayers.

In **Chapter 4** discussed the optical and light trapping properties of black Si nanostructures fabricated with one-step mask-less RIE. The black Si optimization led to the development of highly efficient nanostructuring recipe. The RIE black Si recipe guarantees to obtain low damage black Si surfaces with low SRV (below 10 cm/sec). The RIE black Si method was compared with the KOH-etched standard procedure and MACE black Si process in terms of fabrication process, optical reflectance, recombination properties and possibility to dope in standard high temperature furnaces. RIE black Si surface defect density is comparable to KOH and plain polished surface. As a passivation layer Al_2O_3 was used. Al_2O_3 is well-known in PV industry as one the best passivation layer on silicon with surface recombination velocity reaching close to 4 cm/sec. One of the intention in this project was to optimize RIE black Si for doping process. Therefore, the results of doping of RIE black Si experiment and investigated its properties were presented. However, our experimental results confirmed that black Si tended to have over-doped regions due to inhomogeneous dopant distribution on a rough surface analyzed with sheet resistance measurements and simulation. Due to fatal breakdown of SIMS setup that allows to measure doping profile and complexity of such measurements on nanostructured surfaces with wide ion beam, further investigation is required and currently in progress.

5.2 Concepts in progress

In this section, the experiments results overview that required additional analysis and testing are presented. Most of experiments and devices presented in this section were fabricated and characterized, however were not sufficient to present as separate chapters and required additional analysis and optimization.

5.2.1 NiO as p-Type Carrier Selective Contact on Si

One of the most promising and important concept tested during this project was development of hole selective contacts based on NiO-Si heterojunction.
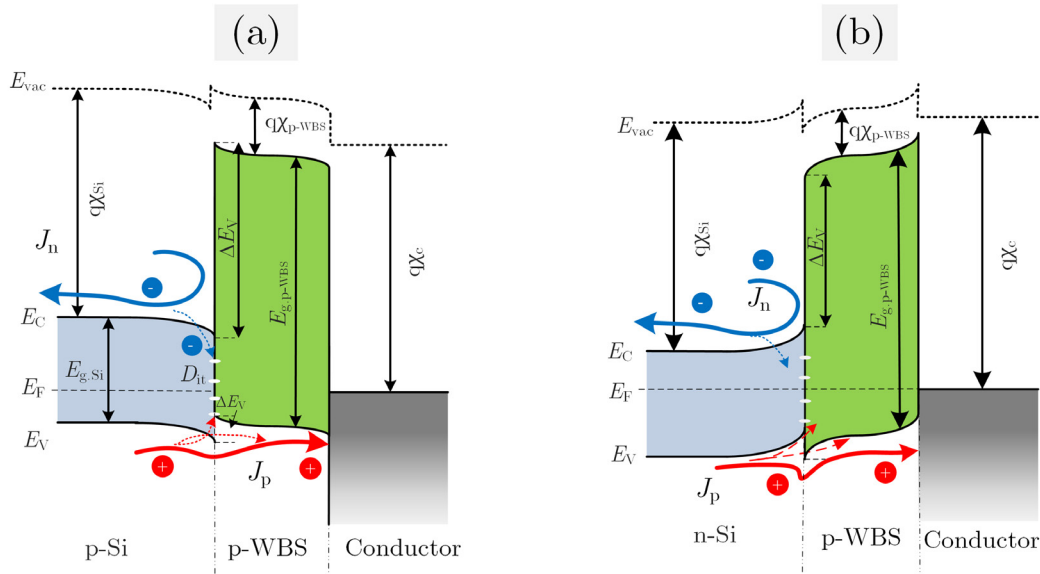
FIGURE 5.1: Anderson energy band diagram of NiO-Si heterojunction: (a) n-p structure, (b) n-n structure

Nickel (II) oxide or NiO has recently gained attention as the potential carrier selective contact in solar cells. The recent report on application NiO as a CSC proved its potential for application in silicon solar cells as well as in organic solar cell [161, 220–224]. NiO is the optically transparent, high work function (>5 eV) wide energy band gap (E_g=3.6 eV) with low electron affinity semiconductor material, excellent valence band alignment to silicon, and high conduction band offset (ΔE_c=2.6 eV) (see Tab. 5.2 and Fig. 5.1). Also, NiO is chemically stable and has one stable crystal phase [225]. As a result, NiO acts as a transparent hole conducting contact (HCC) for SHJ solar cells [161]. There are different deposition techniques exist that could guarantee high quality of NiO films. Among them, RF and DC sputtering from NiO target [226, 227] and oxidation of Ni particles in oxygen plasma [228], electron beam deposition from NiO target [229], and ALD growth of NiO [222], etc. Each of these techniques can be operated at low temperatures giving additional advantage over the high-temperature process. These techniques have their benefits and disadvantages.

In the context of this project, RF sputtering from a Ni target in Ar and Oxygen ambient, RF sputtering from a NiO target and ALD NiO using Ni(acac)$_2$ (nickel acetylacetonate) with O$_3$ synthesized films were deposited to form a NiO-Si heterojunction in order to investigate NiO passivation properties, isotypical and anisotypical heterojunction properties. The experiments of NiO and c-Si heterojunction development with electron blocking properties were conducted with the focus to investigate the back surface field carrier selective contact, rectifying carrier selective contact and passivation properties of NiO films in NiO-Si heterojunction.

All the techniques allowed depositing NiO films to form NiO-Si(p) structures. However, there was detected a huge difference between RF sputtering techniques and ALD. RF sputtering processes are well known to cause surface damage due to energetic ions. On the other hand, ALD process uses atomic scale surface reaction and allows very precisely and damage-free deposition of NiO. The quantitative analysis of the deposition methods was made based on the effective lifetime measurements with the MDP lifetime measurement method and setup of the samples deposited with all three techniques and presented in Fig. 5.2
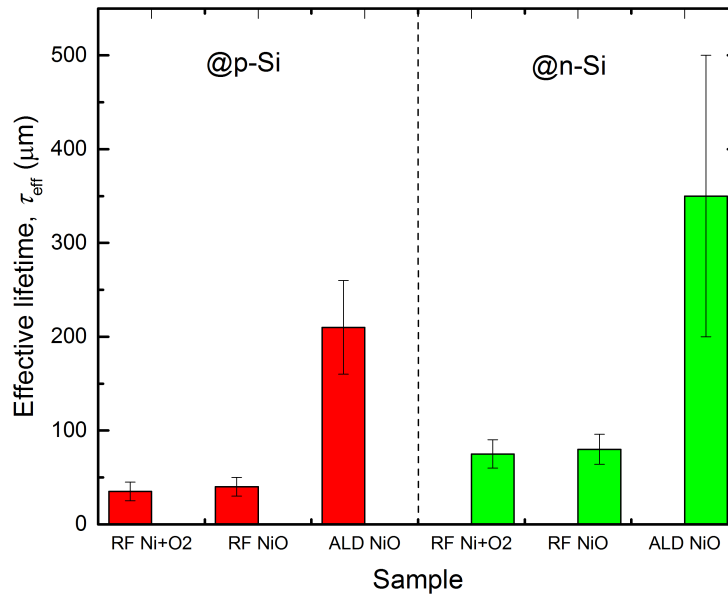
FIGURE 5.2: Effective carrier lifetime of RF sputtered NiO films from Ni target oxidized in plasma, RF sputtering from NiO target and ALD grown NiO measured with microwave detected photoconductivity (MDP) lifetime mapping method at the 10^{15} cm^{-3} injection level

Electrical properties (I-V illuminated and dark conditions) on all the films altered a lot for all three deposition techniques and in most cases were uneven with S-shape varied behavior. Isotypical NiO-pSi heterojunction showed close to ohmic behavior. However, further optimization is still required. Therefore, they were not included here and are required more detailed analysis to understand the behavior of NiO-Si heterojunction and effect on device performance, including valence band alignment of NiO and Si, oxygen vacancies in NiO, defect states at the heterointerface and Fermi level pinning in regards of NiO to metal contact.

5.2.2   Top Contact Carrier Collecting Layers

In order to support the concept of carrier selective contacts based on transition metal oxides in silicon solar cell fabrication, a top transparent conductive layer should be implemented. In silicon solar cells and generally in all solar cells, the power conversion efficiency is limited by many fundamental losses. One of the principal causes of such losses is incomplete absorption of solar spectrum, shading and series resistance losses [100, 202]. Metal interconnects in a solar cell are excellent conductors with low resistive losses; however, due to the shadowing effect, the shape of metal interconnected requires optimization [230]. Such optimization leads to the adverse effect on series resistance and power conversion efficiency. Therefore, transparent conductive oxides (TCOs) or graphene film can provide 100 % covering of the top contact could solve the problem. TCOs also possess low resistivity ($\rho \approx 10^{-4}$ Ωcm), and high transparency ($T > 85$ %) in the limited visible and near ultraviolet part of the solar spectrum and is thus transparent to only the limited spectral range [231]. Most conventional TCOs are indium tin oxide (ITO) [232], fluorine doped tin oxide (FTO), ZnO:Al

(AZO) [233], and ZnO:Ga (GZO) [234] have had the dominant shares in optoelectronic devices including solar cells for several decades. TCOs are still limited by optical transparency and parasitic absorption and series resistance, as well as high cost for depleted materials such as ITO. Graphene and other ultra-thin metallic films [235], and grids could be used as an alternative for top contact in solar cells. A monolayer of graphene absorbs only 2.3 % of visible light and is theoretically as low as 30 $\Omega/\square$ [236]. TCO films such as AZO could be deposited with a variety of deposition methods. These methods include RF magnetron sputtering [237], chemical vapor deposition [238], pulse laser deposition [239–241], and ALD [242–245]. However, the series resistance of synthesized graphene usually exceeds several hundred $\Omega/\square$, and on the corrugated surface its behavior is not well studied. The corresponding graph of sheet resistance versus transmittance of different top contact materials is shown in Fig. 5.3.
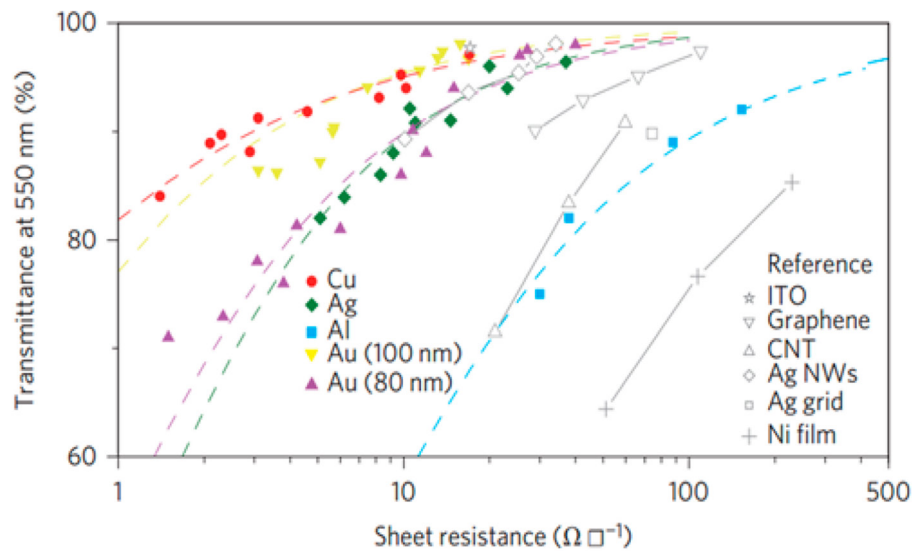
FIGURE 5.3: Sheet resistance versus optical transmission (at 550 nm) for ITO, graphene, CNT, Ag NWs, Ag grid, Ni, Cu, Au, Ag, and Al [246]

In this context, there were attempts to introduce graphene as a transparent conductor on top of the black Si roughened surfaces in this project. However, the attempts did not provide any significant results, since graphene was found to be suspended on top of the corrugated surface and displayed severe adhesion problem to such surfaces. Second, all the methods for graphene transfer allowed to transfer only damaged flakes of graphene. Therefore, it was decided to test TCO films based on aluminum zinc oxide (AZO) material as a top contact transparent conductive layer. RF sputtering process for AZO was first tested; however, due to the highly sensitive ultra-thin TiO_2 film and induced damaged by the sputtering process, it decided to focus on ALD AZO process. The low resistive AZO (below 10 $m\Omega\cdot$cm) films grown at 150 to 250 °C with excellent film quality were developed. However, this process was developed after the main batch of the solar cell had been fabricated, and, therefore, the process was not implemented in the fabrication process flow. However, additional analysis of AZO effect on TiO_2-Si and NiO-Si heterojunctions should be conducted in order to investigate diode properties, contact resistance, optical losses in the layer and devices.

In heterojunction solar cell, a conducting metal contact to each carrier selective layer plays an important role. Islam et al. [224] simulated on the TiO_2-Si-NiO heterostructure solar cell with pinning materials with different workfunctions. Different workfunctions do not affect J_{SC} and V_{OC}, but the slope of $I-V$ curve decreases if the workfunction is too large for the

layer on top of NiO or too small for the layer on top of TiO_2 as shown in Fig. 5.4. Overall, such effect results in the reduction of fill factor and power conversion efficiency.
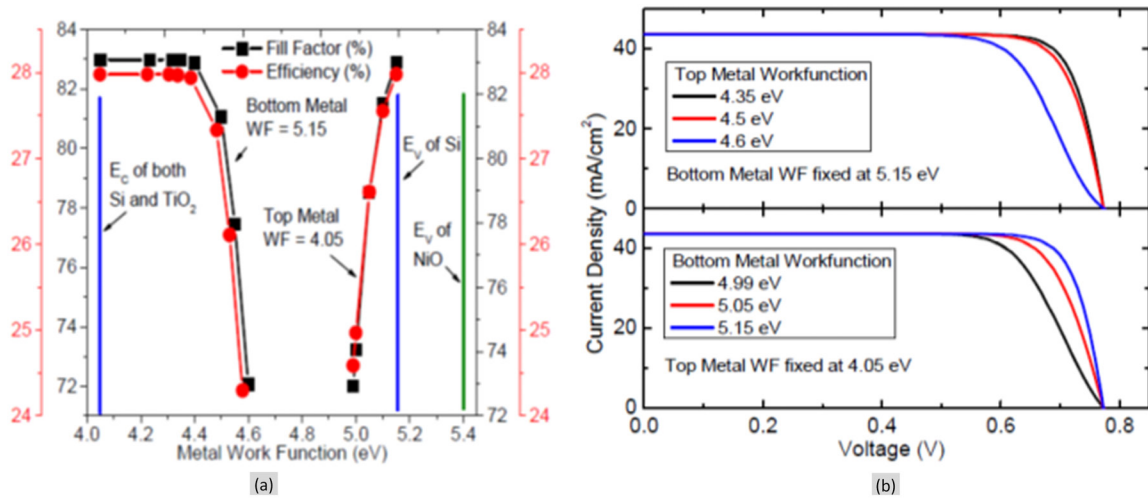

FIGURE 5.4: (a) Effect of metal workfunction on the fill factor (FF) and efficiency of the TiO_2/Si/NiO solar cell and (b) current-voltage characteristic of the TiO_2/Si/NiO solar cell for different metal workfunctions [224]

Based on the analysis the best fit of conductor material workfunction on top TiO_2 CSCs could be evaluated based on Fermi level pinning in the range of 4.0-4.6 eV, particularly Ti, Al, Ta, Zr, In and TCO AZO. For NiO CSC: Ni, C, graphene, Cu, Ir are conductors with workfunction in the range of 4.9-5.2 eV. Therefore, Ti ultra-thin 5 nm layer was implemented on top of TiO_2 films before Al finger deposition. NiO was tested as back side field layer in TiO_2-Si-NiO cell. On top of NiO, Ni ultra-thin 5 nm layer was deposited before Al contact deposition. Important to note that AZO is a material with an excellent fit with TiO_2 coating, while graphene is with NiO. The corresponding material workfunction is shown in Tab. 5.1.

5.2.3 Nanotextured Si solar cell with electron conductive TiO_2 contact and hole conductive NiO contact

State of the art in Si photovoltaic is interdigitated back contact Si solar cell with amorphous silicon carrier selective contacts and record efficiency 26.7 % [11]. Amorphous silicon (a-Si:H) solar cells technology provides the best passivation of silicon interfaces, low temperature processing and high scalability to industrial production [41–43]. Although a-Si:H and SiO_2 -based carrier selective contacts have shown remarkable performance, these technologies have some fundamental challenges related to thermal stability and parasitic photon absorption in a-Si:H films, a complicated deposition process and toxicity, and quite high production costs. Therefore, there is an interest in developing high-quality CSCs that can be easily deposited, at low cost and with minimal use of hazardous materials [44].

One of the most promising material groups for carrier selective contacts is transition metal oxides (TMOs). TMOs were first used in organic and perovskite solar cells [46]. These CSCs have shown potential as alternative CSCs in silicon photovoltaics [47] due to the low cost of processing steps involved. For each group of carrier selective contacts, there is a wide selection of materials available. As a hole-selective CSC's molybdenum oxide (MoO_x) [48–55], nickel oxide (NiO_x) [56–60], vanadium oxide (VO_x) and tungsten oxides (WO_x) [47] have been investigated as replacements for a-Si:H p-type layer in silicon solar cells with

TABLE 5.1: Workfunction of conductive coatings (metal and TCO films) as a carrier collector

Material	Φ, eV	References
4.0-4.6 eV (suitable for contact with TiO_2)		
Cd	4.08	
Cr	4.5	[247],
In	4.09	[248],
Mn	4.1	[249]
Nb	4.02-4.36	
Sn	4.42	
Ta	4.15-4.25	
Ti	4.33	
V	4.3	
Zr	4.05	
AZO	3.7-4.4	[250]
4.9-5.2 eV (suitable for contact with NiO)		
Cu	4.94-5.1	[247],
Ge	5.0	[248],
Ir	5.00	[249]
Ni	5.04-5.35	
Rh	4.98	
Te	4.95	
ITO	4.4-4.9	[251]

a record efficiency of 22.5 % [48]. For the n-type electron selective CSC, TiO_2 is the most promising materials in SHJ solar cells [50–61] and was also tested in this work. TiO_2 has a 3.2 eV band gap energy. TiO_2 as a hole-blocking layer in silicon solar cells is intensively investigated. A single heterojunction silicon solar cell with a TiO_2 backside hole blocking layer achieved an efficiency of 21.6 % [61].

A huge advantage of metal oxides is a possibility to deposit theses materials with ALD and provide highly conformal films on any surface morphology, free of pinholes and with excellent passivation properties. In few words, it becomes possible to fabricate solar cells using ALD or other low process temperature techniques and decrease levelized cost [62, 63]. In combination with advanced light trapping texturing such as RIE for black silicon nanostructures, heterojunction Si solar cells with CSC can be a strong competitor to a-Si:H heterojunction technology. The main advantages are mostly based on a deposit of these materials with ALD technique that also leads to low toxicity and a low deposition temperature of the process and in principle possibility to deposit all functional thin films in one ALD process line at atmospheric pressure (i.e. Spatial atmospheric ALD). Such benefits can simplify the process flow, reduce production cost within production line and thermal budget. Based on this, an advanced Si solar cell device concept was suggested in this work and tested.

The Si solar cell device concept with TiO_2 and NiO carrier selective contacts was previously suggested and simulated by Islam et al. [224]. Islam et al. suggested to use TiO_2 and NiO films as carrier selective contacts on Si and predicted possibility to obtain power conversion efficiency above 27 % that is close to Shockley-Queisser limit [29]. This concept has a potential to become a highly efficiency solar cells that could realize Swanson prediction possible [252]. Swanson predicted that highly efficient solar cell with high short circuit current,

open circuit voltage and above 25 % power conversion efficiency could be realized with efficient selective contacts, one for electron blocking and another for hole blocking. In this context, TiO_2 and NiO are almost perfect candidates. There materials have almost perfect energy band alignment in conduction band (for TiO_2) and valence band (for NiO) and huge valence band barrier for holes at the TiO_2-Si interface and conduction band barrier for electrons at the NiO-Si interface as shown in Fig. 5.5 and accordingly to Tab. 5.2. TiO_2-Si and Si-NiO heterojunctions have either with p- or n-type equivalent to Si doping and therefore n-p, n-n and p-p and n-p heterojunctions. Corresponding properties of these materials are presented in Tab. 5.2 [161]. These two thin films in conjunction have the same role as the p-n–junction in the conventional solar cell. The barrier from each CSCs should result in a current flow.

TABLE 5.2: Physical parameters of Si, TiO_2 (anatase), NiO and a-Si semiconductor materials [161, 253]

Parameters	Si	TiO$_2$ (anatase)	NiO	a-Si
Energy bandgap, E_g, eV	1.12	3.26	3.36	1.4-1.9
Electron affinity, χ, eV	4.01	4.1	1.8	3.8
Net donor doping, $N_D - N_A$	10^{18}		10^{18}	10^{18}
Net acceptor doping, $N_A - N_D$	10^{18}	10^{18}		10^{18}
Lattice constant, a, (Å)	5.431	$a_0=b_0=3.785$ $c_0=9.514$	$a_0=4.1758$ $c_0=5.213$	NA
Dielectric constant, ε	12	86	11.75	11.8
Electron mobility, μ_e, (cm^2/(Vs))	1350	0.1	0.1	1
Hole mobility, μ_h, (cm^2/(Vs))	480	0.1	0.1	0.01
Effective density of states (conduction band), N_C, (cm^{-3})	2.8×10^{19}	7.93×10^{20}	8.87×10^{18}	4.5×10^{21}
Effective density of states (valence band), N_V, (cm^{-3})	1.04×10^{19}	1.79×10^{19}	7.57×10^{18}	6.4×10^{21}

Based on the presented solar cell concept with carrier selective TiO_2-Si and Si-NiO heterojunctions contacts, an advanced architecture on nanostructured Si solar cell was suggested and presented in Fig. 5.6. Figure 5.7 shows the simplified process flow in order to fabricate the cell. More details process flow is attached as Appendix C. In order to increase the short circuit current, light trapping texturing was employed for silicon wafers as a step (1). Texturing techniques and optimization process are presented in details in Chapter 4 and consisted of three set of wafer: polished, KOH textured and RIE black Si textured. KOH textured samples were processed for 50 min in 2 % KOH, 7 % IPA (HO_2 solution) at 70 °C and RIE black Si with etching time - 14 min; pressure 38 mTorr; O_2 100 sccm; SF_6 70 sccm; power coil 3000 W; power platen 10 W, chiller temperature, -20 °C; etch rate - 98 nm/min. The second (2) step consists of ALD deposition of Al_2O_3 layer in order to suppress minority carrier recombination at the interface. ALD Al_2O_3 process was conducted with TMA and H_2O precursors as described in Chapter 4 at 200 °C with 380 cycles, which resulted to 32 nm thick layer.

After deposition, Al_2O_3 films were annealed in N_2 ambient at 400 °C for 30 min. The third (3) step was UV photolithography in order to prepare opening on the backside of the wafer prior to NiO carrier selective film deposition (see Appendix C). Forth step was NiO deposition with RF sputtering from Ni target in Ar and O_2 ambient leading to Ni oxidation in
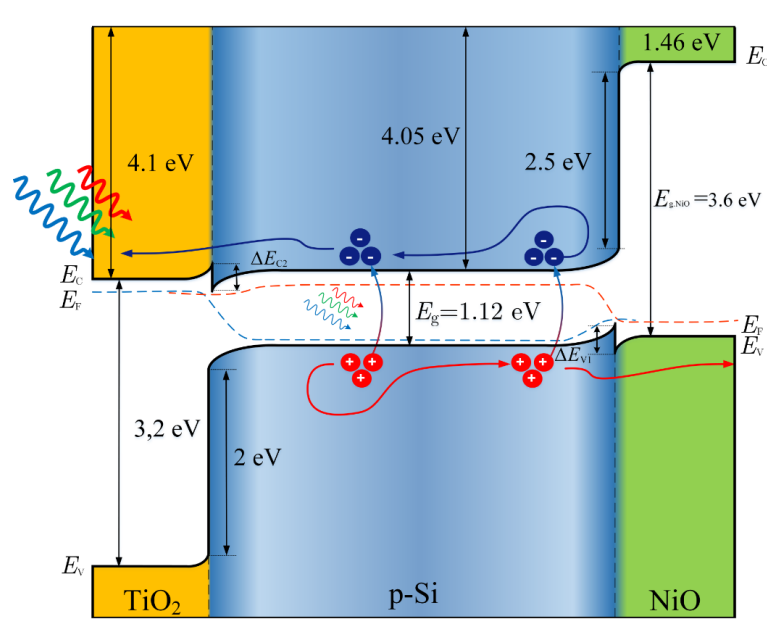
FIGURE 5.5: Energy band diagram of proposed TiO$_2$-Si-NiO solar cell
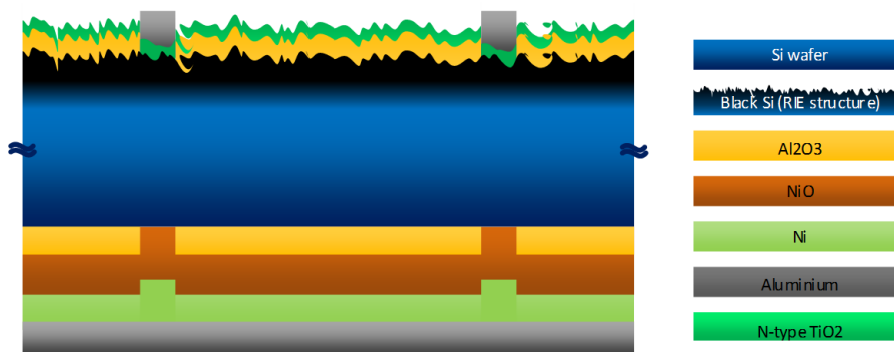
FIGURE 5.6: Structure of proposed TiO$_2$-Si-NiO solar cell with all interlayers
and CSCs

plasma and its deposition on Si wafer. NiO RF sputtering process was conducted at 20 %
Ar/O_2 ratio, power 20 W, pressure 5 mTorr, temperature 20 °C for 3 min and resulted in 15
nm thick NiO film. Fifth step was Ni film electron beam deposition in order to obtain 5 nm
thick film. Ni film was deposited with intention to adjust hole barrier height and Fermi level
depinning [224]. The next step (6), Al with electron beam technique was deposited with a
thickness of 300 nm. The seventh step (7) included UV front side photolithography in order
to prepare opening on the backside of the wafer prior to TiO$_2$ film growth. The eighth step
(8) was ALD TiO$_2$ growth at 80 °C with 110 cycles leading to 5 nm thick film. Post deposition
annealing at 200 °C for 10 min was applied in order to improve TiO$_2$ properties. Next and
the last step (9) was Ti film 5 nm thick deposition, in order to adjust hole barrier height and
Fermi level depinning [224], following with 300 nm Al film deposition with electron beam
technique.

Figure 5.8 shows KOH textured and black Si textured fabricated solar cell with metal oxide
carrier selective contacts concept.

Characterization of the cell performance was evaluated under a sun simulator. The current
density -voltage (j-V) experimental results in dark and under one sun illumination (AM1.5G)
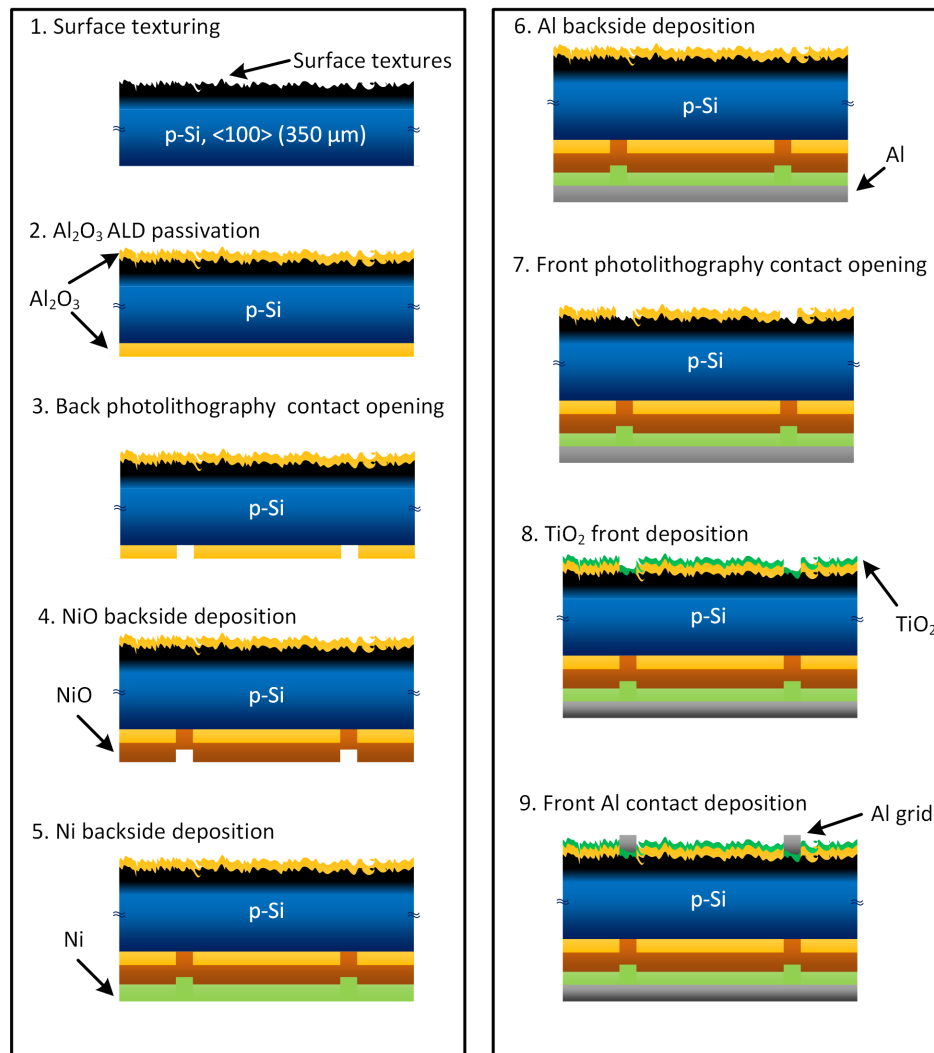
FIGURE 5.7: Process flow of proposed TiO_2-Si-NiO solar cell with all interlayers and CSCs
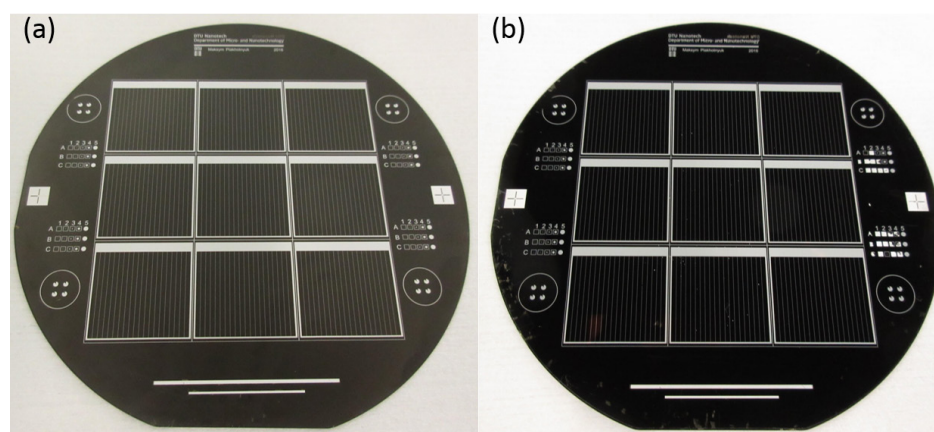
FIGURE 5.8: Photoimages of fabricated solar cells: (a) KOH-textured solar cell and (b) black Si RIE textured solar cell

for all cells obtained from each of the fabricated devices. However, only one selected illuminated J-V curves for each type of cells (polished, KOH textured and black Si) are shown
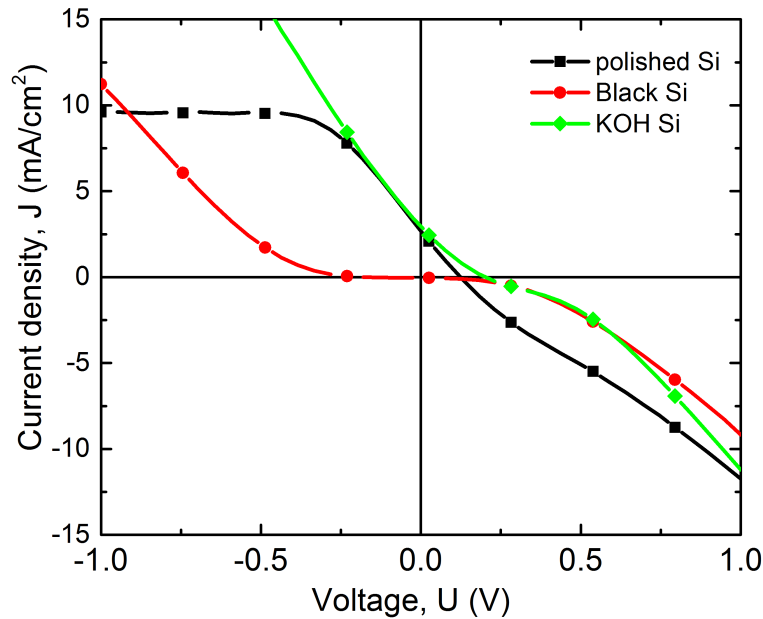
FIGURE 5.9: J-V characteristic of fabricated solar cells on a polished, KOH-textured and black Si RIE textured substrate

in Fig. 5.9 since the other characteristic expressed similar behaviour. It is obvious from Fig. 5.9 that solar cell devices suffer from severe issues. Analysis of lifetime evolution during fabrication of solar cell batch led to conclusion that the causes of lifetime degradation is possible Al_2O_3 damage during photolithography steps, electron beam metal deposition and/or TMA precursor poor quality. The S-type varied J-V behaviour of the devices could be due to surface interface recombination difference, excessive defects in Al_2O_3 layer, defects in TiO_2 layer due to electron beam deposited particles, ALD $TiCl_4$ precursor impurity, defects in NiO layer due to RF sputtering induced damage on Si and oxygen vacancies effect on NiO properties. In order to understand in details the causes, more comprehensive analysis is required. Detailed analysis including simulation of devices and comparison with experimental device characterization, SEM and TEM study of metal oxides coating of textured surfaces, external quantum efficiency in order to understand the carrier extraction issues, surface recombination analysis to understand losses at the interfaces, UPS and XPS study of heterojunctions in order to understand composition of deposited materials, oxygen vacancies and band alignment at the interfaces.

5.3 Future work

Metal oxide carrier selective contacts have an enormous potential for solar cells as a potentially cheap and reliable technology to advance the field. The goal of this thesis was to identify the issue, challenges, and possible solutions. First – improvement of interface passivation, second – reliable device architecture, and third – testing and development of alternative materials as carrier selective passivating contacts. Alternative methods of surface passivation can be based on TiO_2 and Al_2O_3 material and their ALD deposited stacks. Section 3.2 briefly discussed the possibility of using tunnelling oxides as an enhancement to the

interface passivation. The well-tested architecture could be simulated and tested with new materials like CSCs. The concept of such based HIT architecture is presented in Fig. 5.10, by replacing conventional CSC with metal oxides (TiO_2 or NiO, etc.). Application of new materials based on perfect fit with silicon either conduction or valence band can guarantee low interface defects, higher efficiency, and low-cost production technology. In Figure 5.11, brief summary of the most interesting and already tested metal oxide materials such as CSC and TCOs are shown.
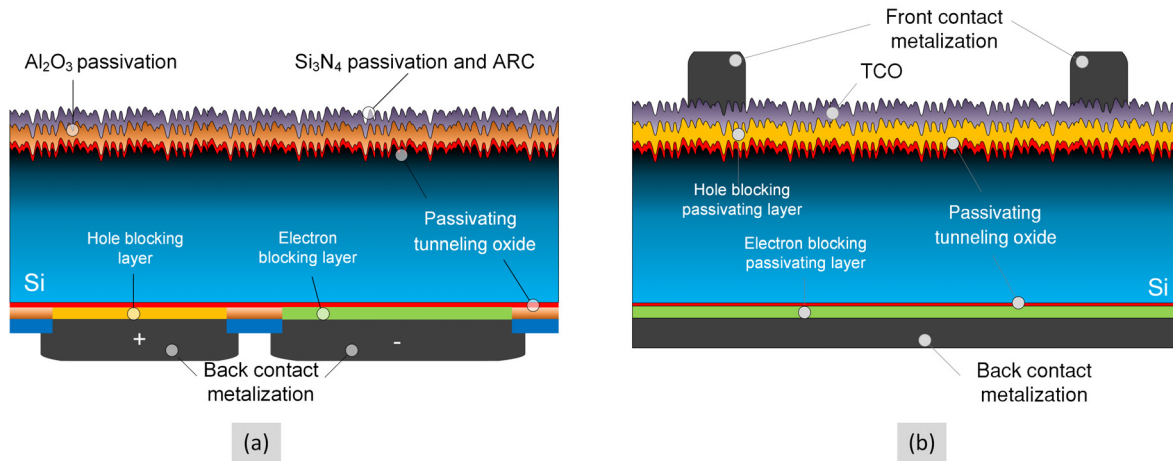
FIGURE 5.10: Illustrations of IBC (a) front contact (b) SHJ solar cell with carrier selective transition metal oxides contacts and nanostructured (black Si) front surface absorber

Electron conductive materials (TiO_2, ZnO, Ta_2O_5) [50–61], transparent conductive oxides (AZO, ITO, IZO etc.)[232–234], hole conductive materials (NiO, MoO_3, CuAlOx, V_2O_5, WO_3 etc.) [48–55], [56–60], [47] and tunneling passivation oxides (SiO_2, Al_2O_3) are already in good match with silicon (Fig. 5.11) to be tested in a heterojunction concept (Fig. 5.12). This work was called to explore some of the concepts. However, there are numerous opportunities that could be explored further with the materials mentioned above. Another interesting concept is to test such carrier selective contacts with perovskite absorbers or in tandem with Si heterojunction solar cells.

5.4 ALD grown CSCs, passivation layers, ARC and TCO and industrial potential

Furthermore, the above mentioned materials (TiO_2, ZnO, Ta_2O_5, AZO, ITO, IZO, NiO, MoO_3, CuAlOx, V_2O_5, WO_3, SiO_2, Al_2O_3) become even more interesting if all of them are deposited with ALD techniques [254], which provides excellent quality of the films without any surface damage and even possibility for stack deposition; consequently, more efficient passivation of interfaces and tuning of material properties. During this PhD project, ALD has shown as the most reliable thin film deposition technique, that allowed to deposit highly conformal films on any simple and complex surface morphology, guarantee excellent surface passivation with different materials and precisely control film thickness. It is one of the most interesting topics for future work: application of ALD for deposition of carrier selective and passivating materials in solar cell fabrication. Moreover, ALD has already gained some industrial interest, and there are several companies that manufacture industrial scale ALD equipment (Beneq, SoLayTec, Oxford Instruments, ALD NanoSolutions, Cambridge
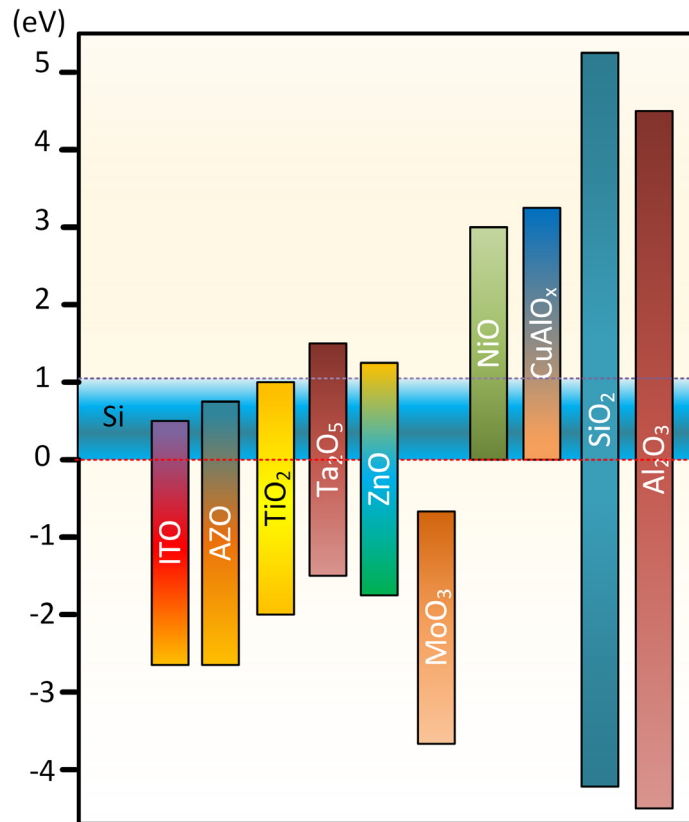
FIGURE 5.11: Energy band gap of materials that have potential as a carrier selective contacts in silicon solar cells
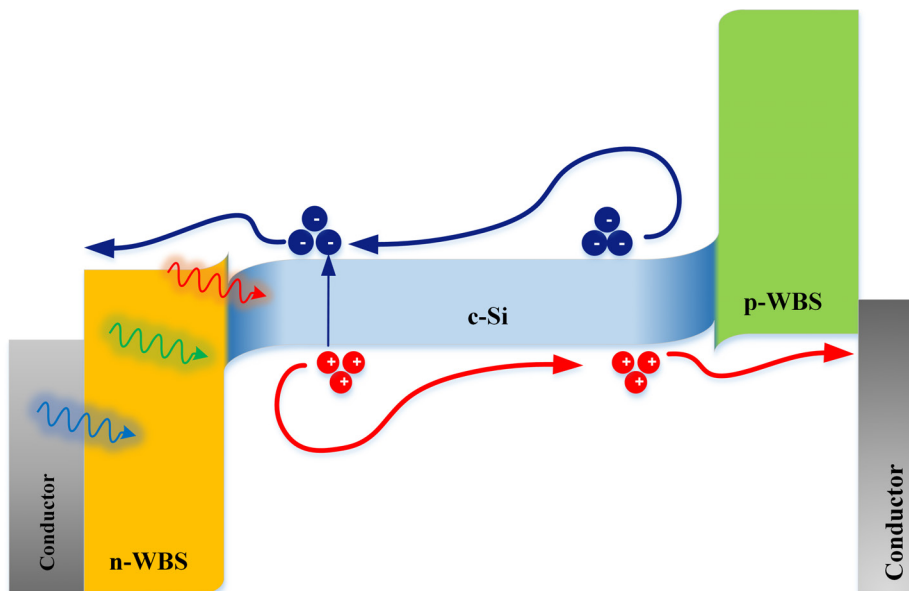
FIGURE 5.12: Energy band diagram of heterojunction silicon solar cells with wide bandgap transition metal oxide carrier selective contacts

NanoTech, Encapsulix, Picosun etc.) focused for PV applications. Such equipment can replace almost all high-temperature processing equipment in the solar cell production line (Fig. 5.13). Consequently, industrial ALD process development for PV industry acquired a

new interesting turn and opportunities to explore. Now the time to show a proof of concept devices with ALD deposited layers in solar cell.
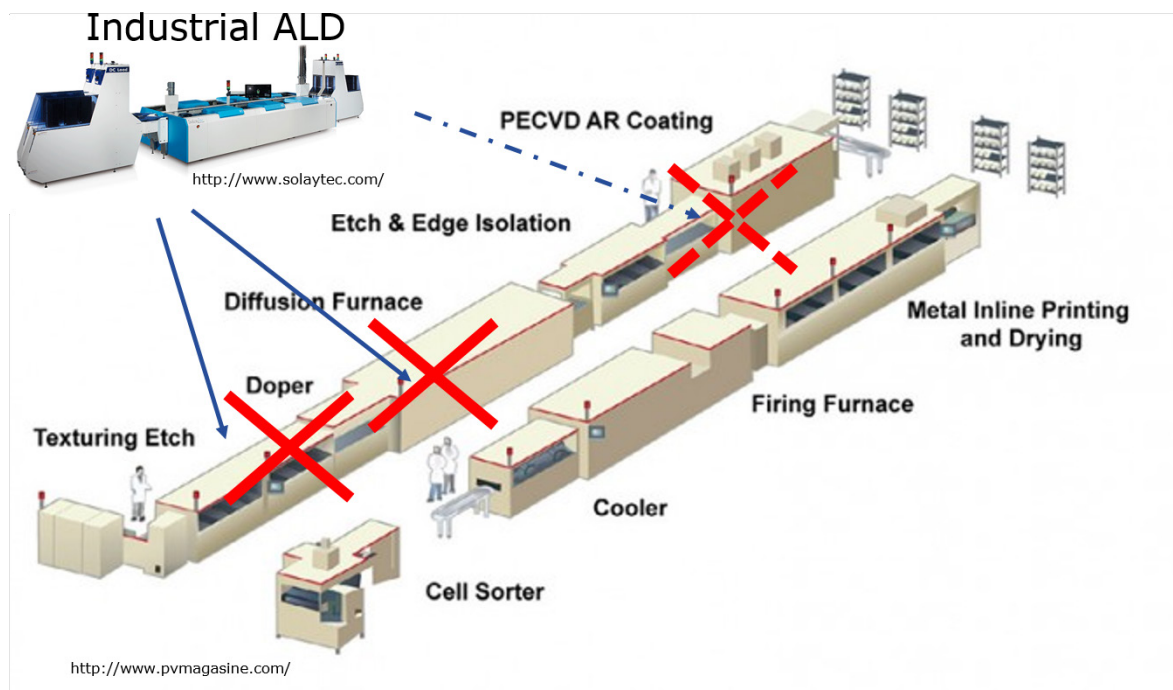
FIGURE 5.13: ALD industrial equipment as an alternative to the conventional high-temperature process production line. Note: red cross indicates the equipment which could be replaced with ALD

In addition, the newest concepts in ALD development, such as spacial atmospheric ALD, combine the advantage of temporal ALD, excellent control of film composition, conformality and uniformity at atmospheric pressure and at low temperatures with a deposition rate approaching 100 nm per min. In this sense, ALD start to compete with other well established thin film deposition techniques particularly in PV industry and not only. No doubt, ALD is the future technology for precise thin film growth and worth to explore!

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Appendix A

B.Sc. and M.Sc. Supervised Students Theses

- Jesper Mark Fly Hansen and Jesper Bodilsen. "Fabrication, Optimization and Characterization of Titania/Silicon Heterojunction Solar Cells", Bachelor Thesis, Technical University of Denmark, 2014

- Marco De Paolis. "Design and Fabrication of an Interdigitated Back Contact Silicon Heterojunction Solar Cell with Poly-Silicon Carrier Selective Contacts", Master Thesis, Sapienza Universita Di Roma and Technical University of Denmark, 2015

- Ermis Kanakakis. "Simulations and Experiments on Carrier Selective Contacts for Junction-less Photovoltaic Cells", Master Project, Technical University of Denmark, 2016

- Alix Dodu. "Doped Nanostructured Silicon Solar Cells with TiO_2 Electron Selective Contacts", Master Project, UPMC Sorbonne University and Technical University of Denmark, 2016

- Frederik Villebro. "Heterojunction Silicon Solar Cells", Bachelor Thesis, Technical University of Denmark, 2016

- Emil Astrup Wrisberg and Anders Lyngbye Pedersen. "Black Silicon Nanostructures for PV Application and Selective Carrier Contacts Solar Cells", Bachelor Project, Technical University of Denmark, 2016

Appendix B

Publications and Approbation

Author's Publications

Published

- Plakhotnyuk M.M., Schüler N., Shkodin E., Vijayan R.A., Masilamani S., Varadhara-japerumal M., Crovetto A., Hansen O. (2017). Surface passivation and carrier selectivity of the thermal-atomic-layer-deposited TiO_2 on crystalline silicon. *Japanese Journal of Applied Physics*, V.56, 8S2, pages 08MB18 [118]

- Plakhotnyuk M.M., Davidsen R. S., Schmidt M. S., Malureanu R., Stamate E., Hansen O. (2016). Lifetime of Nano-Structured Black Silicon for Photovoltaic Applications. *Proceedings of the 32nd European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC)*, pp. 764-767 [86]

- Plakhotnyuk M.M., Gaudig M., Davidsen R. S., Lindhard J.M., Hirsh J., Lausch D., Stenbæk M.S., Stamate E., Hansen O. (2017). Low surface damage dry etched black silicon. *Journal of Applied Physics*, 122(14), pp.143101, 2017 [170]

- V.F. Onyshchenko, L.A. Karachevtseva, O.O. Lytvynenko, M.M. Plakhotnyuk, O.J. Stronska (2017). Effective lifetime of minority carriers in black silicon nano-textured by cones and pyramids. *Semiconductor Physics, Quantum Electronics and Optoelectronics*, 20(3), pp.325, 2017 [87]

Under preparation

- Plakhotnyuk M.M., Schüler N.,Iandolo B., Hansen O. (2017). Effect of ultra-thin Al_2O_3 film on passivation and diode properties in TiO_2/Al_2O_3-Si stack. Under preparation, 2017

- Plakhotnyuk M.M., Bae D., Stamate E., Villebro F., Nilsen O., Bratvold J.E., Hansen O. (2017). Comparative studies of NiO film as a carrier selective contact prepared by RF sputtering and atomic layer deposition. Under preparation, 2017

Conference Contributions

Oral Presentations

- Plakhotnyuk M.M. et al. "Hole Selective NiO Contact for Silicon Solar Cells", European Advanced Material Conference (EAMC), Stockholm, Sweden, 2016

- Plakhotnyuk M. et al. "Enhanced Passivation And Characterization Of Titania Silicon Heterojunction With Tunneling Oxide Interlayers", European Advanced Material Conference (EAMC), Stockholm, Sweden, 2016

- Plakhotnyuk M.M. et al. "Heterojunction Nanostructured Silicon Solar Cells with Metal Oxide Carrier Selective Contacts", (Invited talk, Halle, Germany, 2016)

- Plakhotnyuk M.M. et al. "Discovering Challenges in Fabrication of Nanostructured c-Si Solar Cells with Metal Oxides Carrier Selective Contacts", Sustain-ATV conference, Kgs. Lyngby, Denmark, 2016

- Plakhotnyuk M.M. et al. "Behind the Nature of Titanium Oxide Excellent Surface Passivation and Carrier Selectivity of c-Si", *26th International Photovoltaic Science and Engineering Conference (Asia PVSEC)*, Singapore.

- Plakhotnyuk M.M. et al. "Application of ALD in Photovoltaics", International Training School on Atomic Layer Deposition – "ALD-UKRAINE 2017", Kyiv, Ukraine, 2017

Posters

- Plakhotnyuk, M.M., Shvets, V., Whelan, P. R., Mackenzie, D., Bøggild, P., Hansen, O. (2015). Graphene transfer on highly corrugated black silicon surface. *6th Symposium on Carbon and Related Nanomaterials*, Copenhagen, Denmark. [255]

- Plakhotnyuk, M.M., Hansen, O. (2015). TiO2-Si solar cells with carrier selective contacts and low temperature processing. *DTU Sustain Conference 2015* [E-37] Lyngby: Technical University of Denmark. [256]

- Plakhotnyuk, M.M., Davidsen, R. S., Steckel, A., Dodu, A., Hansen, O. (2016). Phosphorous Doping of Nanostructured Crystalline Silicon. *26th International Photovoltaic Science and Engineering Conference*, Singapore, Singapore. [257]

- Plakhotnyuk M.M., Davidsen R. S., Schmidt M. S., Malureanu R., Stamate E., Hansen O. (2016). Lifetime of Nano-Structured Black Silicon for Photovoltaic Applications. *32nd European Photovoltaic Solar Energy Conference and Exhibition* [86]

As co-author

- Iandolo B., Plakhotnyuk M.M., Gaudig M., Davidsen R. S., Lausch D., Hansen O. (2017). Dry Etch Black Silicon with Low Surface Damage: Effect of Low Capacitively Coupled Plasma Power. *Proceedings to the 33nd European Photovoltaic Solar Energy Conference and Exhibition (33rd EU PVSEC)*, Amsterdam, Netherlands.

- Payne D., Lopez A.C., Zeng Y., Abbott M., McIntosh K., Cruz-Campa J., Davidson R., Plakhotnyuk M.M., Bagnall D. (2017). Rapid Optical Modelling of Plasma Textured

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- Karachevtseva L., Lytvynenko O., Onyshchenko V., Plakhotnyuk M., Stronska E. Effective lifetime of minority carriers in black silicon nano-textured by cones and pyramids (2017). *Abstract at the V International Research and Practice Conference "Nanotechnology and Nanomaterials" NANO-2017*, August, 2017

- Iandolo B., Fiordaliso E.M., Johannsen S.J., Davidsen R. S., Plakhotnyuk M.M., Beleggia M., Kasama T., Hansen O. Accessing nanoscale structural and electrical properties of black silicon for solar cells. *Abstract at the European Material Research Society Meeting (2017 Fall E-MRS Meeting)*, Fall 2017, Warsaw, Poland

Patent Applications

- Plakhotnyuk, M.M., Davidsen, R.S., Hansen O. Heterojunction silicon solar cells with nanostructured surfaces and ALD grown passivation and carrier selective contacts, Submitted in January 2017.

- Plakhotnyuk, M.M., Davidsen, R.S., Hansen O. Interdigitated back contacted heterojunction silicon solar cells with front surface nanostructured surfaces and ALD grown passivation and carrier selective contacts, Submitted in January 2017.

Appendix C

Solar Cell Fabrication Process Flows

C.1 TiO$_2$-Si Heterojunction

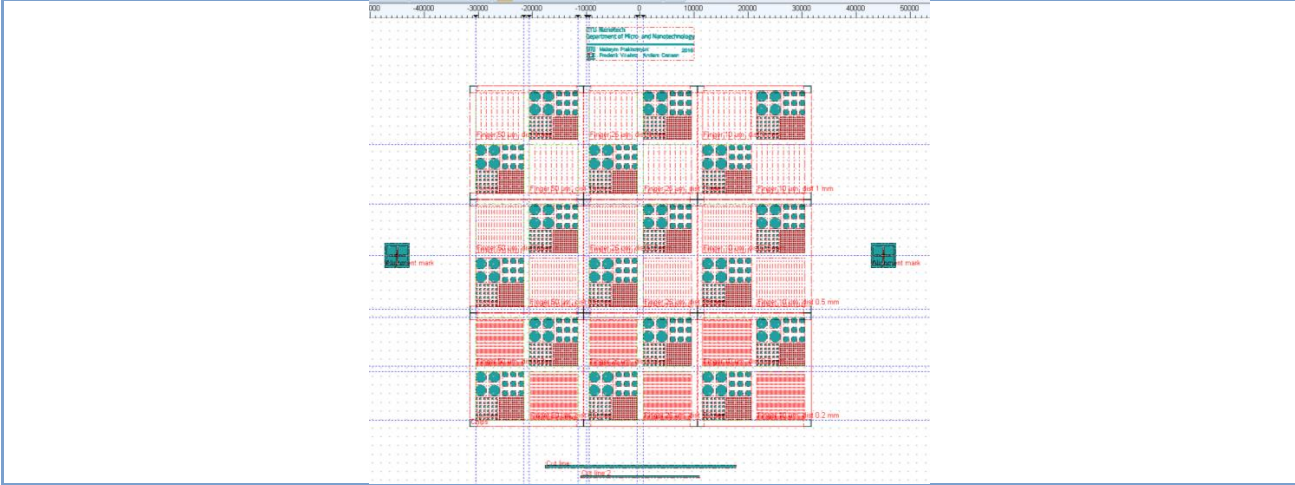| Process flow title			Revision
Al2O3 passivated TiO2 test solar cell			**1.0**
DTU Danchip National Center for Micro- and Nanofabrication			Contact phone
	Labmanager group Microreactors		Date of creation	Date of revision

Objective

- **Investigate small area TiO2-Si diode for photovoltaic properties with Al2O3 passivated surface**
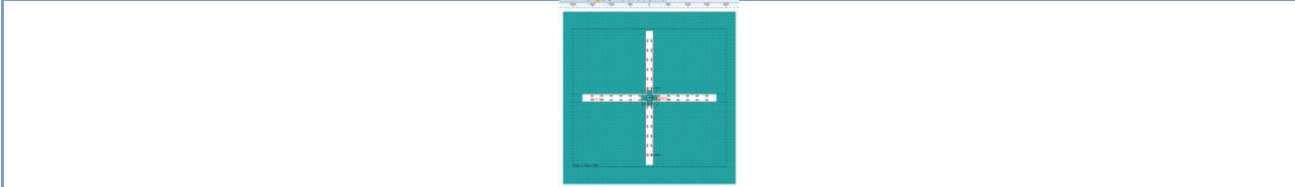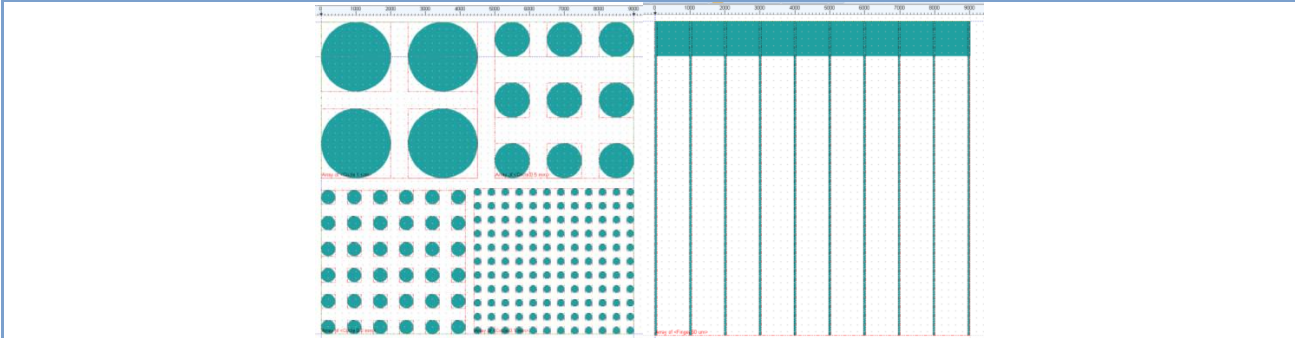
Device cross section

Process flow

Si

Al₂O₃

TiO₂

Al

1

2

3-4

5

6

7

8-9
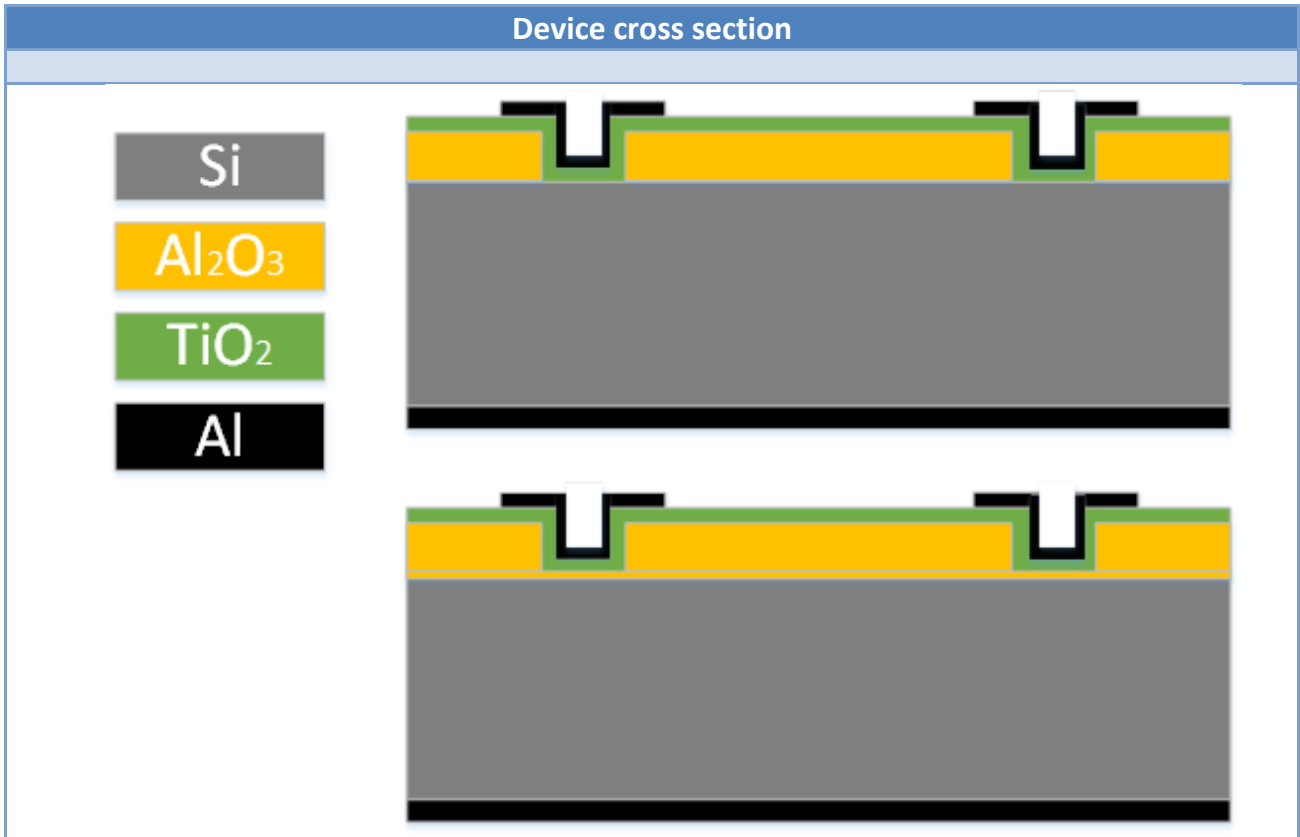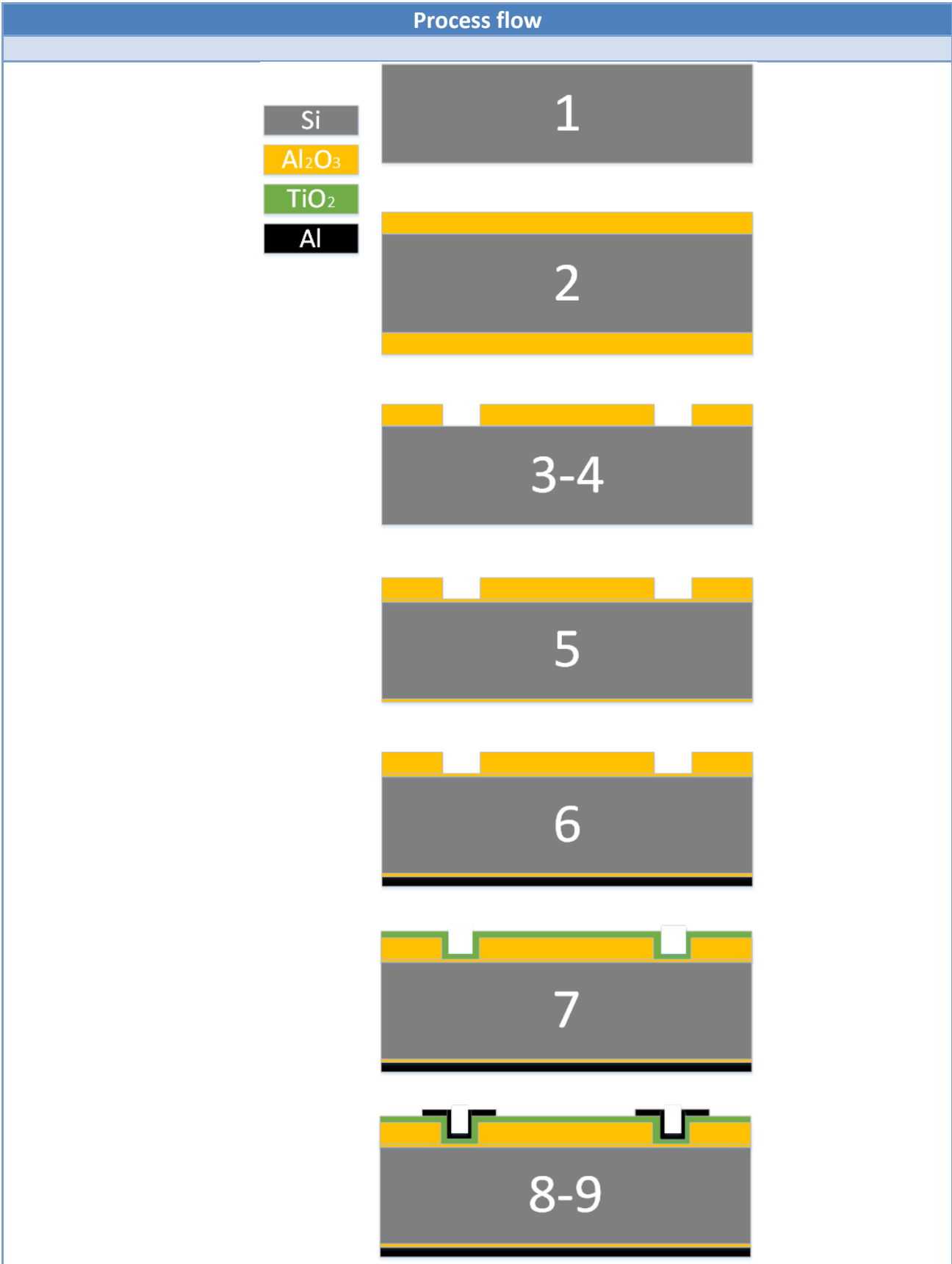
Mask design

Mask 1: General view

Mask 1: Alignment marks

Mask 1: Test structure

Mask 2: General view

Design of Experiment							
Wafer ID	**Top contact**	**Emmiter**	**Interlayers**	**Front passivation**	**Substrate**	**BSF layer**	**Back contact**
WA1.1	Al.300nm/Ti5 nm	TiO2	NA	Al2O3 380 c	pSi	NA	Al.300nm
WA1.2	Al.300nm/Ti5 nm	TiO2	Al2O3 1 c	Al2O3 380 c	pSi	NiO / Ni	Al.300nm
WA1.3	Al.300nm/Ti5 nm	NA	NA	Al2O3 380 c	pSi	NA	Al.300nm
WA1.4	Al.300nm/Ti5 nm	TiO2	NA	Al2O3 380 c	nSi	NA	Al.300nm
WA1.5	Al.300nm/Ti5 nm	TiO2	Al2O3 1 c	Al2O3 380 c	nSi	NiO / Ni	Al.300nm
WA1.6	Al.300nm/Ti5 nm	NA	NA	Al2O3 380 c	nSi	NA	Al.300nm

Substrates									
Substrate	Orient.	Size	Doping/type	Polish	Thickness	Box	Purpose	#	Sample ID
Silicon	<100>	4"	p(Boron)	DSP	350±25µm	OP506	Device wafers	5	WA1.1- WA1.3, D1-D3
Silicon	<100>	4"	n(Phospor)	DSP	350±25µm	ON505	Device wafers	5	WA1.4- WA1.6

Al-TiO2-Si-Al	Al-TiO2-Si-NiO-Al	Al-TiO2-Al2O3-Si-Al	Al-TiO2-Al2O3-Si-NiO-Al	Al-Si-Al
1. BHF 2. ALD Al2O3 30 nm 3. Litho 1 4. BHF Al2O3 5. Back metal 6. ALD TiO2 4-5nm 7. Litho 2 8. Front metal	1.BHF 2.ALD Al2O3 30 nm 3.Litho 1 4.BHF Al2O3 5.NiO on a back 6.Back metal 7.ALD TiO2 4-5nm 8.Litho 2 9.Front metal	1. BHF 2.ALD Al2O3 30 nm 3.Litho 1 4.BHF Al2O3 5.Back metal 6.ALD Al2O3 1c 7.ALD TiO2 4-5nm 8.Litho 2 9.Front metal	1. BHF 2.ALD Al2O3 30 nm 3.Litho 1 4.BHF Al2O3 5.NiO on a back 6.Back metal 7.ALD Al2O3 1c 8.ALD TiO2 4-5nm 9.Litho 2 10. Front metal	1. BHF 2.ALD Al2O3 30 nm 3.Litho 1 4.BHF Al2O3 5.Back metal 6.Litho 2 7.Front metal

Process flow			
Step Heading	Equipment	Procedure	Comments
1 Wafer selection			**Wafer**
1.1 Wafer selection	Wafer Box	Follow standard procedure.	Buy wafers in the Labmanager
1.2 Measure sheet resistivity	Four point probe	Measure resistivity of wafer no. 1-4 Expected 1-20 Ω cm	
2 ALD Al2O3 growth			**All**
2.1 Oxide growth	ALD	200°C 350 cycles Expected thickness = 30 nm	**All**

| 2.2	Annealing	ALD, C1, ATV	30 min annealing at 375-415C	**All**
3	**Lithography #1– 1.5µm standard**			**Test first on 3 dummy wafer**
3.1	Surface treatment	HMDS in new SS spinner	Load all wafers in oven for ~30 min Recipe: program 4	Note time in logbook
3.2	Clean spinner	SSE spinner	Clean spinner nozzle and run the dummy wafers Recipe: 1,5um 4inch_Prox bake (Temp: 95°C, time: 90 sec). Spin coat both sides of the wafer	1-3 dummies dedicated to SS spinner Note time in logbook
3.3	Coat wafers frontside	SSE spinner	Coat the front side of the device wafers 1.5 µm AZ5214e Novolac resist Soft bake on hotplate Recipe: 1,5 4inch_Prox bake (Temp: 95°C, time:90 sec)	Resist thickness not checked Note time in logbook
3.4	Exposure	KS Aligner/MA6 aligner	Hard contact Exposure time: 6.5-7 sec (check logbook) Mask:	Note time in logbook Define exposure time on dummy wafer
3.5	Develop	Developer TMAH UV lithography	Development SP 120 sec and post bake for 60 sec	Note time in logbook
3.6	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
3.7	Inspection: Optical	Optical microscope	Check pattern and alignment marks	**D1-D3** Note in measurement sheet
4	**Al2O3 etching in BHF**			**All**
4.1	BHF	BHF	Prepare separate solution Etching rate: **30 nm/min**	
4.2	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
4.3	Inspection: Optical	Optical microscope	Check pattern and alignment marks	**D1**
4.4	Strip resist	Acetone	First 2-3 min in rough followed by 5 min in fine strip bath with US. Acetone strip in ultrasound bath. Strip with ultrasound for 5 min	
4.5	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
4.6	Inspection: Profile	AFM, Optical Profilometer	Measure step height Target: 30±10 nm	**D1** Note in measurement sheet
5	**ALD Al2O3 growth**			
5.1	Oxide growth	ALD	200°C 1 cycles Expected thickness?	**2n and 2p**
6	**Contact deposition: backside**			
6.1	Al film deposition	Wordentec/ Alcatel	Expected thickness 300 nm	**Register in logbook.**
7	**ALD TiO2 growth**			
7.1	Oxide growth	ALD	80°C 95 cycles Expected thickness 4-5nm	**All**
8	**Lithography#2: 1.5 µm standard – Brightfield, negative: front side openings**			**Can be done in Gamma spinner**
8.1	Surface treatment	HMDS oven	Load all wafers in oven for ~30 min Recipe: program 4	Note time in logbook

8.2	Clean spinner	SSE spinner	Clean spinner nozzle and run the dummy wafers Recipe: 1.5 4inch	1-3 dummies Note time in logbook
8.3	Coat wafers backside	SSE spinner	Coat the backside of the device wafers 1.5 µm AZ5214e Novolac resist Recipe: 1,5 4inch_Prox bake (Temp: 95°C, time:90 sec)	Resist thickness not checked Note in logbook
8.4	Coat wafers frontside	SSE spinner	Coat the front side of the device wafers 1.5 µm AZ5214e Novolac resist Soft bake on hotplate Recipe: 1,5 4inch_Prox bake (Temp: 95°C, time:90 sec)	Resist thickness not checked Note time in logbook
8.5	Exposure	KS Aligner/MA6	Align to alignment marks. Hard contact Exposure time: 6.5-7 sec (check logbook) Mask: **Front Contact**	**Register in logbook.**
8.6	Develop	Developer TMAH UV lithography	Development SP 120 sec and post bake for 60 sec	Note time in logbook
8.7	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
8.8	Inspection: Optical	Optical microscope	Check pattern and alignment	**D1** Note in measurement sheet.
9	**Contact deposition: frontside**			**All**
9.1	Deposition frontside	Alcatel, Wordentech	Metals to deposit: Al / TI - 300/5 nm	Note time in logbook
9.2	Inspection: Optical	Optical microscope	Check for completeness	
9.3	Lift-off	Lift-off bench	Leave wafers in acetone for 2-3 min. Start the US for 10 min. Rotate wafers and start US for another 10 min.	Fill the bench with Acetone until carrier is covered.
9.4	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	

C.2   NiO-Si Heterojunction

Process flow title	Revision
NiO-SiO-Si Process optimization	**1.0**

DTU Danchip National Center for Micro- and Nanofabrication	Contact email makpl@nanotech.dtu.dk	Contact persons Maksym Plakhotnyuk	Contact phone 27575092
	Labmanager group Microreactors	Batch name Feb 2016	Date of creation 3-Jul-16	Date of revision 3-Jul-16

Objective

- **Optimize the NiO deposition process for use in heterojunction solar cell.**

Device cross section

Silicon
Native oxide
NiO
Al
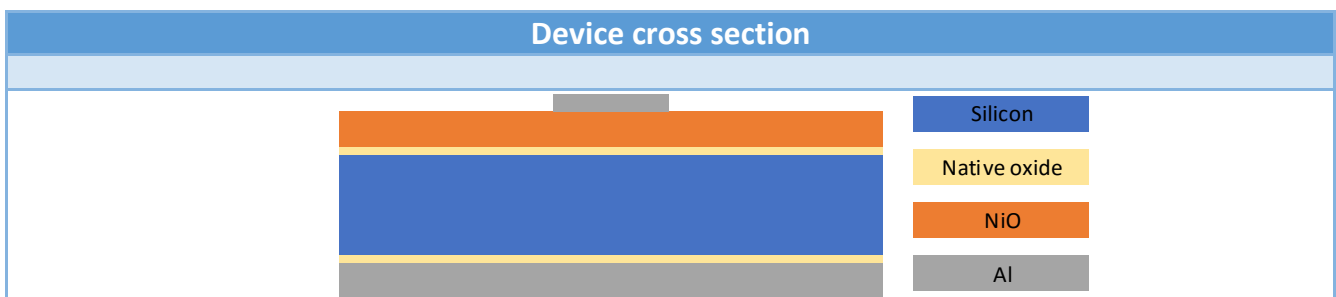
Design of Experiment

Optimization settings

#.#	O2 [%] 1	Power [W] 2	Pressure 3	Temp [C] 3
1	5	100	3	20
2	10	125	4	50
3	15	150	5	75
4	20	175	7	100
5	25	200	10	125
6	30		12.8	150
7	40			175
8	50			200
9	70			

Table 1 Optimization parameters for NiO thin film deposition.

Wafer ID	Type	Thickness	Polished	Number
P.1	P	350 um	DSP	OP506
N.1	N	350 um	DSP	ON505

Table 4 Wafers used for optimization process.

Figures

Figure	Caption	Step	Figure
1	**Wafer selection**	Buy in labmanager, ON505 and OP506.	
2	**Deposit back contact** Alcatel	300 nm of al is deposited.	
3	**Slice into chips** Slicing machine	The wafer is sliced into 2x2cm chips.	
4	**Deposit NiO thin film** Lesker sputtering	NiO is deposited with the desired test parameters.	
5	**Deposit front contact**	15 nm of al is deposited through shadow mask.	

Comments:Click here to enter text.

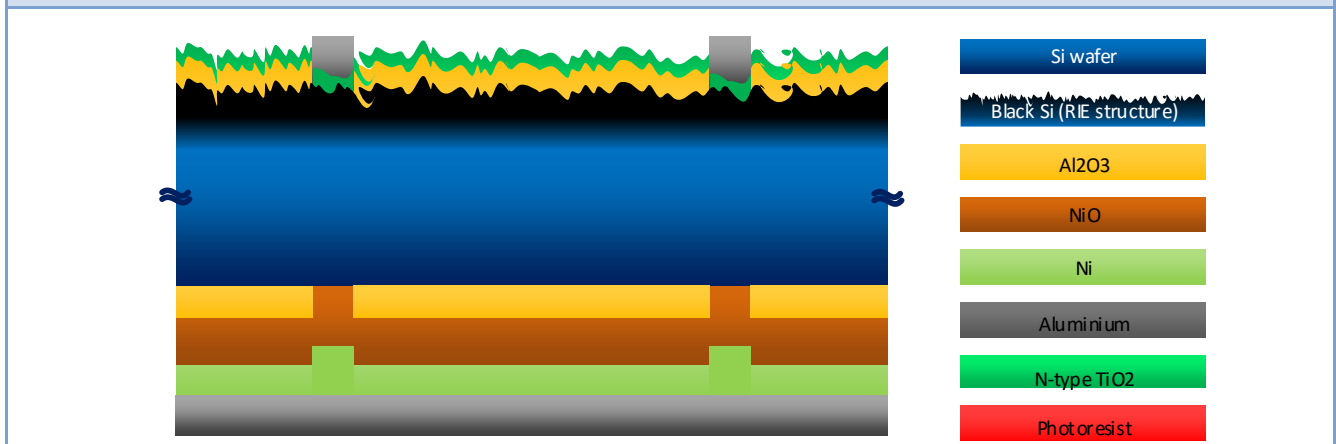| Process flow				
Step Heading	**Equipment**	**Procedure**	**Comments**	**References**
1 Wafer selection			**P.1 and N.1**	
1.1 Wafer selection	Wafer Box	Follow standard procedure. ON 505 and OP506	Buy wafers in the Labmanager	
2 Back contact deposition			**P.1 and N.1**	
2.1 Back contact	Alcatel	Deposit 300 nm of al on the backside		
3 Slice into chips			**P.1 and N.1**	
3.1 Chips	Dedicated slicing room	Slice the wafer into 2x2 chips using the slicing machine.		
4 NiO thin film			**P.1 and N.1**	
4.1 NiO thin film	Lesker sputtering system	Deposit NiO thin film with the desired test parameters available in table 1 on both a P and N-type 2x2 cm chip.	Include a 2x2 piece of glass for transmission measurements.	
5 Front contact deposition				
5.1 Front contact	Alcatel	Deposit 15 nm of al on the front side through a shadow mask to create pattern required for further measurements.	Use the created chip holder and shadow masks.	
6 Characterization - Cleanroom			**P.1 and N.1**	
6.1 Ellipsometry Thickness	Ellipsometer VASE	Check thickness of thin film.		
6.2 Ellipsometry Band gap	Ellipsometer VASE	Check the bandgap.		
6.3 Ellipsometry Transmission		Check the transmission.	**Glass pieces**	
7 Characterization – Outside cleanroom			**P.1 and N.1**	
7.1 Light IV	Room above cleanroom	Check Voc, Jsc, FF, Pout, efficiency.	Let the lamp heat up for 30 min before use.	
7.2 Dark IV	MEMS lab	Check Rs, Rsh, Ideality factor and J0.		
7.3 XPS	X-ray Photoelectron Spectroscopy	Check oxygen vs nickel content.		

C.3 TiO$_2$-Si-NiO Heterojunction Cell
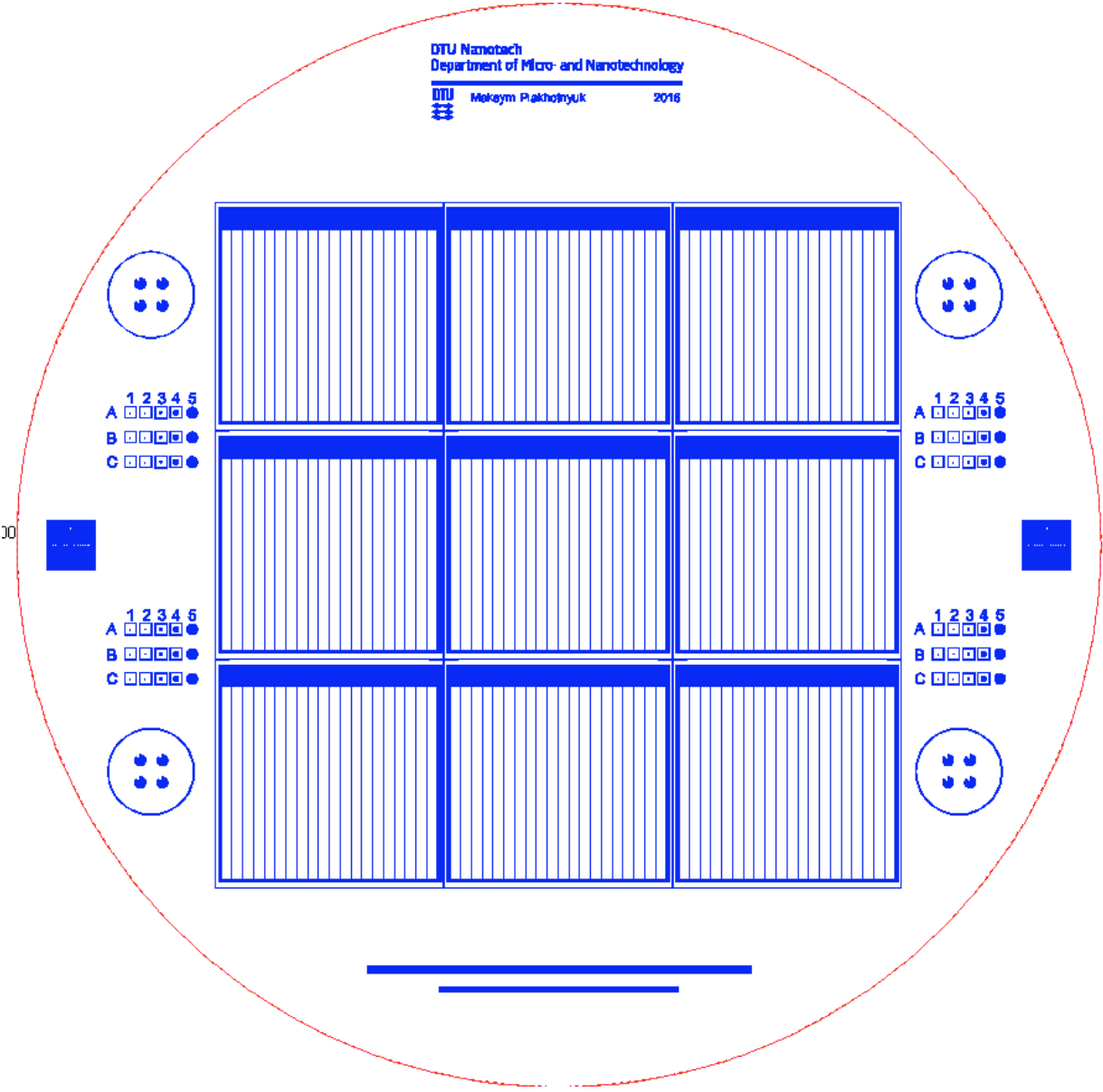
Objective

- **Fabricate crystalline silicon solar cells with double side carrier selective contacts of TiO2 and NiO layers and Al2O3 passivation layer**
- **Investigate effect of double side carrier selective contacts, nanostructuring, aluminum oxide passivation of crystalline Si solar cells**
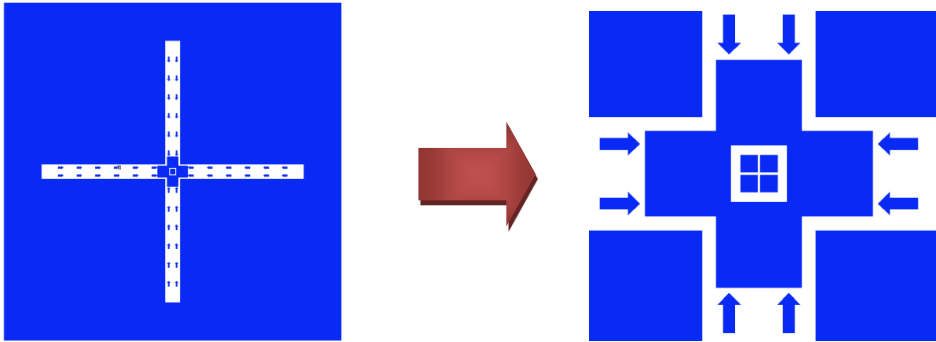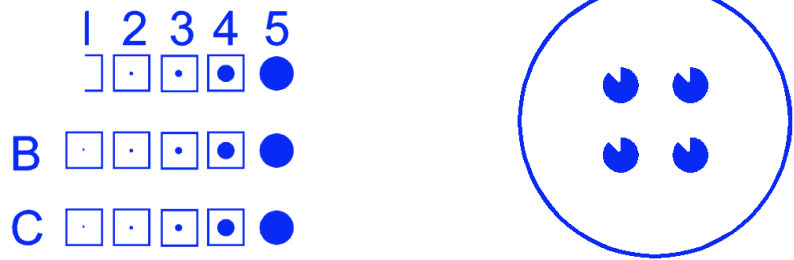
Device cross section

Legend:
- Si wafer
- Black Si (RIE structure)
- Al2O3
- NiO
- Ni
- Aluminium
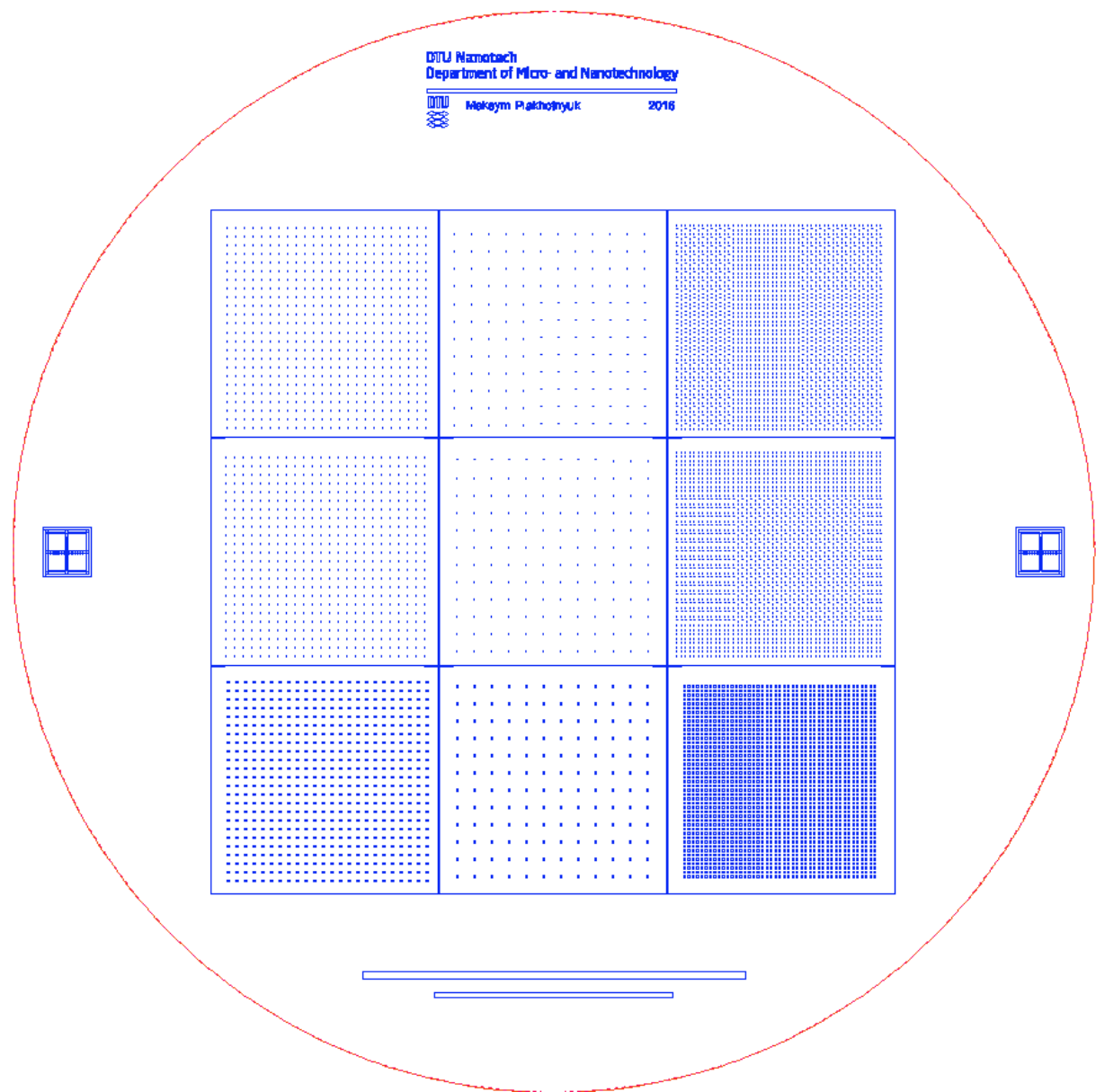- N-type TiO2
- Photoresist

Mask design

Front side

Alignment marks

Test structures

Back side mask

DTU Nanotech
Department of Micro- and Nanotechnology

Maksym Plakhotnyuk   2016

Process flow title	Rev.	Date of revision	Contact email
TiO2-Al2O3-BSi-Al2O3-NiO-Ni Solar cell process	1.0	17-Jun-16	makpl@nanotech.dtu.dk

Design of Experiment
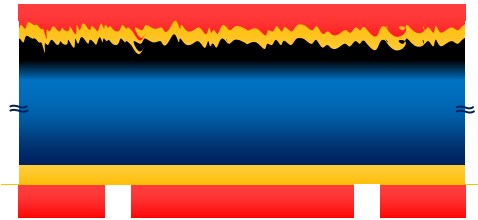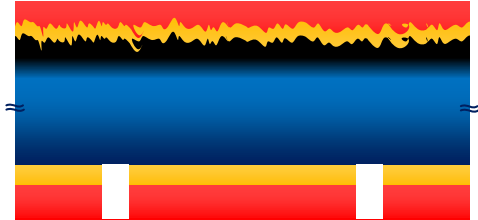
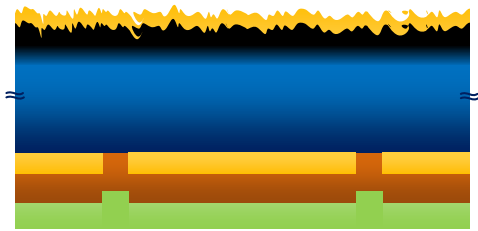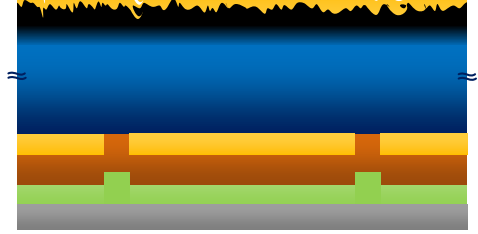| Wafer ID	7. Top contact	6. Emmiter	3. Front passivation	2. ARC	1. Substrate	2. ARC	3. Back passivation	4. BSF layer	5. Back contact
W 7.1	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c		pSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.2	Al.300nm/Ti5 nm	TiO2/Al2O3	Al2O3 380 c		pSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.3	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	pSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.4	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	pSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.5	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	pSi	Black Si	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.6	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c		nSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.7	Al.300nm/Ti5 nm	TiO2/Al2O3	Al2O3 380 c		nSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.8	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	nSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.9	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	nSi		Al2O3 380 c	NiO / Ni	Al.300nm
W 7.10	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	Black Si	nSi	Black Si	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.11	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	KOH	pSi	KOH	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.12	Al.300nm/Ti5 nm	TiO2/Al2O3	Al2O3 380 c	KOH	pSi	KOH	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.13	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	KOH	nSi	KOH	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.14	Al.300nm/Ti5 nm	TiO2/Al2O3	Al2O3 380 c	KOH	nSi	KOH	Al2O3 380 c	NiO / Ni	Al.300nm
W 7.15	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	MACE	pSi		Al2O3 380 c	NiO / Ni	Al.300nm
W7.16	Al.300nm/Ti5 nm	TiO2	Al2O3 380 c	MACE	nSi		Al2O3 380 c	NiO / Ni	Al.300nm
Test wafers									
WT 7.17	Al.15nm/Ti5 nm	TiO2			pSi				Al.300nm
WT 7.18	Al.15nm/Ti5 nm	TiO2			nSi				Al.300nm
WT 7.19	Al.15nm/Ti5 nm				pSi			NiO / Ni	Al.300nm
WT 7.20	Al.15nm/Ti5 nm				nSi			NiO / Ni	Al.300nm
WT 7.21	Al.15nm/Ti5 nm	TiO2/Al2O3			pSi			NiO / Ni	Al.300nm
WT 7.22	Al.15nm/Ti5 nm	TiO2/Al2O3			nSi			NiO / Ni	Al.300nm
WT 7.23	Al.15nm/Ti5 nm	TiO2			pSi			NiO / Ni	Al.300nm
WT 7.24	Al.15nm/Ti5 nm	TiO2			nSi			NiO / Ni	Al.300nm
Total = 22 wafers	Metal deposition = 22 wafer	ALD TiO2 growth =20 wafers	ALD Al2O3 growth & annealing = 16 wafer	Front RIE = 6 wafer	22 Si wafers 11 pSi 11 nSi	Back RIE = 2 wafer		NiO / Ni deposition= 20 wafers	Metal deposition = 22 wafer
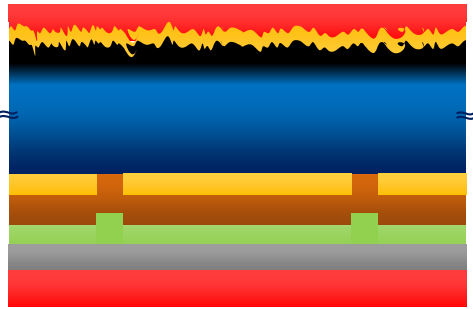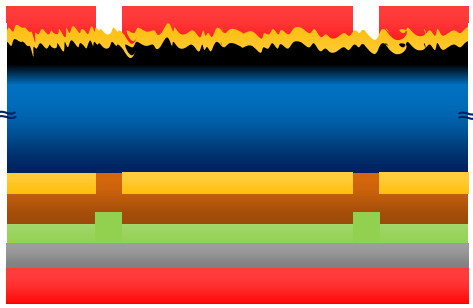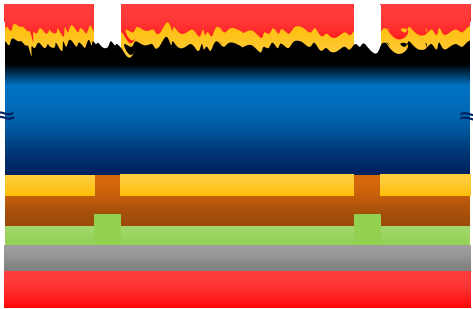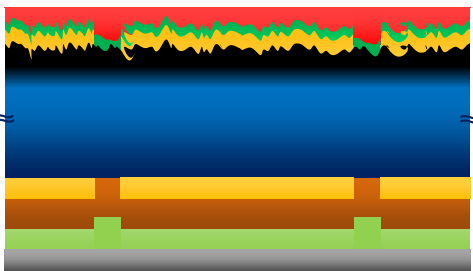
Substrates									
Substrate	Orient.	Size	Doping/type	Polish	Thickness	Box	Purpose	#	Sample ID
Silicon	<100>	4"	p(Boron)	DSP	350±25µm	OP506	Device wafers	5	W1-5
Silicon	<100>	4"	n(Phospor)	DSP	350±25µm	ON505	Device wafers	5	W6-10
Silicon	<100>	4"	p(Boron)	DSP	350±25µm	OP506	Test wafers	5	WT 11, 13, 15, 17, 18
Silicon	<100>	4"	n(Phospor)	DSP	350±25µm	ON505	Test wafers	5	WT 12, 14, 16, 19, 20
Silicon	<100>	4"	p (Boron)	SSP	525±25µm		Danchip test wafers	3	T1-3

Figures

Figure	Caption	Step	Figure
1	**Wafer selection**	1	
2	**After RIE Etch: Black Silicon**	2	
3	**Lithography alignment marks**		
4	**ASE: Shallow trench Pegasus: Process D**		
5	**RCA Clean**		
6	**After ALD Al2O3 growth**	4	
7	**Lithography #1: wafer coating both sides**	5.3	
8			
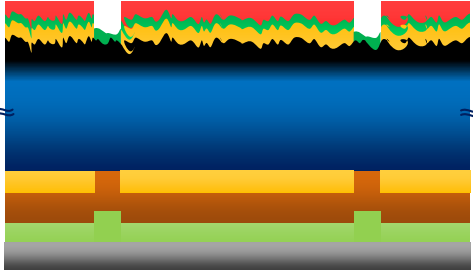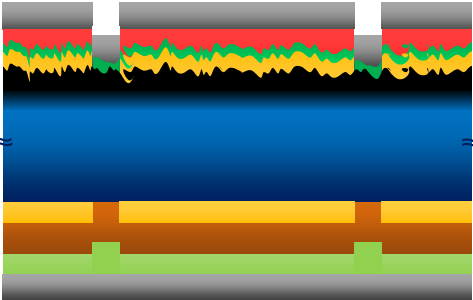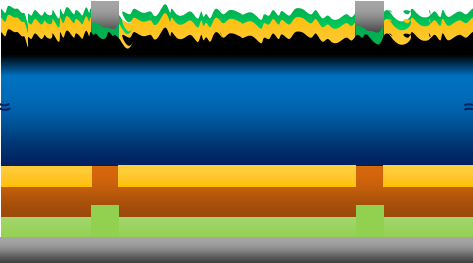
	Lithography #1: develop backside	5.5	
9	**Al2O3 etching in BHF**	6	
10	**After lithography #1**	6.3	
11	**After NiO film growth**	7	
12	**After Ni film growth**	8	
13	**After Al back contact film growth**	8	

14	**Lithography #2: wafer coating both sides**	9.3	
15	**Lithography #2: develop front side**	9.5	
16	**Al2O3 etching in BHF**	10	
17	**ALD TiO2 growth** +ALD Al2O3 1 c interlayer	11	
18	**Lithography #3: frontside wafer coating**	12.3	

19	**Lithography #3: frontside develop**	12.5	
20	**Contact Al deposition: frontside**	13.1	
21	**Lift off**	13.3	

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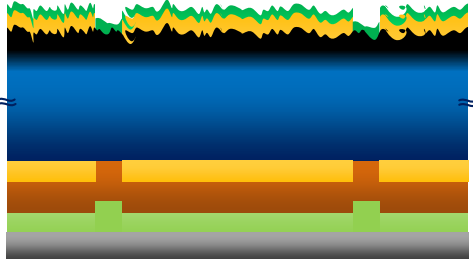| Process flow title	Rev.	Date of revision	Contact email
TiO2-Al2O3-BSi-Al2O3-NiO-Ni Solar cell process	1.0	17-Jun-16	makpl@nanotech.dtu.dk

Process flow			
Step Heading	Equipment	Procedure	Comments
1 Wafer selection			**Wafer W7.1-16, WT7.17-24**
1.1 Wafer selection	Wafer Box	Follow standard procedure.	Buy wafers in the Labmanager
1.2 Measure sheet resistivity	Four point probe	Measure resistivity of wafer no. 1-4 Expected 1-20 Ω cm	**Measure on WT 7.17 and WT 7.18 Register in logbook.**
2 RIE Etch: Black Silicon			
2.1 DRIE	DRIE Pegasus	Recipe: LPP BS, time - 14 min; pressure 38 mtorr; O2 100 sccm; SF6 70 sccm; Power coil 3000 W; Power platen 10 W, Chiller temperature, -20 C; Etch rate, 98 nm/min	**W 7.3-7.5 W 7.8-7.10 Double RIE: W 7.5, W 7.10 Register in logbook.**
2.2 Inspection SEM	SEM & Optical microscope	Check pattern	**W7.3 Register in logbook.**
3 Lithography #0 – Alignment marks			
3.1 Spin coating	Gamma UV	1.5 um MiR 701 on the frontside of the wafer.	**W 7.1-16**
3.2 Exposure	MA6-Aligner	Approximately 13 secs. Cover the main mask with square wafer (8x8 cm) to leave the alignment marks free.	**W 7.1-16**
3.3 Develop	TMAH Developer	Prebake at 110C 60 secs + SP 60 secs.	**W 7.1-16**
3.4 Post bake	Oven 110-250C	150C for 30 min.	**W 7.1-16**
4 Alignment mark etching			
4.1 Etching	ASE Pegasus	ASE: recipe: shallowtr (Shallow trench) in the Danchip ASE folder. Pegasus: Process D.	**W 7.1-16**
5 RCA clean			**W 7.3-5, W 7.8-10**
5.1 RCA clean	RCA bench	Follow standard procedure. RCA1 for 10 min / DI water rinse (3 dumps) 72C in Ammonium hydrooxide and H2O2 Rinse 5 min; HF: 30 sec / DI water rinse (3 dumps) RCA2: 10 min / DI water rinse (3 dumps) 72C in H2SO4 and H2O2 HF: 30 sec / DI water rinse (3 dumps, 5 min) Spindry 3 min	**W 7.3-5 W 7.8-10**
6 ALD Al2O3 growth			**W 7.1-7.16**
6.1 Oxide growth	ALD	200°C 380 cycles Expected thickness = 30 nm	**W 7.1-7.16**
6.2 ALD in situ annealing	ALD	30 min annealing at 370-420C	**W 7.1-7.16**
6.3 Inspection ellipsometer	Ellipsometer VASE	Measure thickness on a test wafer WT 7.1	**W 7.1 Register in logbook.**
6.4 Inspection lifetime	MDP Lifetime measurements	Expected lifetime nSi=10-13ms, pSi=1.5-2 ms	**W 7.1-16 Register in logbook.**

7 Lithography #1– 1.5µm standard

W 7.1-7.16

7.1	Clean spinner	Gamma spinner	Recipe: 1,5um 100mm_AZ MiR 701 with HMDS. Spin coat both sides of the wafer	Note time in logbook
7.2	Coat wafers backside	Gamma spinner	Coat the backside of the device wafers 1.5 µm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	**W 7.1-10, W 7.15-16**
7.3	Coat wafers backside	Gamma spinner	Coat the backside of the device wafers 2 µm AZ MiR 701 resist Recipe: 2 um 100mm_AZ MiR 701 with HMDS	**W 7.11-14**
7.4	Coat wafers frontside	Gamma spinner	Coat the front side of the device wafers 1.5 µm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	Note time in logbook
7.5	Exposure	MA6-aligner	Align to alignment marks. Hard contact Exposure time: 13 sec (check logbook) Mask: **Back Contact**	Note time in logbook
7.6	Develop	Developer TMAH UV lithography	Pre-bake @ 110C for 60 secs, SP 60 secs.	Note time in logbook
7.7	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
7.8	Post bake	110-250C oven	Post bake for 30 min at 150C.	**W 7.1-16**
7.9	Inspection: Optical	Optical microscope	Check pattern and alignment marks	**W 7.1**

8 Al2O3 etching in BHF

W 7.1-7.16

8.1	BHF	BHF	Prepare separate solution Etching rate: 30 nm/min Time: 1-1.1 min	
8.2	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
8.3	Inspection: Optical	Optical microscope	Check pattern and alignment marks	
8.4	Strip resist	Lift-off bench	Lift-off bath for 30 min.	
8.5	Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
8.6	Inspection: Optical	Optical microscope	Check etch pattern	**W 7.1**

9 NiO film growth

9.1	NiO film sputtering	Lesker Sputtering machine	Expected thickness 10-20 nm, Time check O2, 20%, O2, 13 sccm, Ar, 100%, Ar, 43 sccm, Pressure, 5 mTorr, Gun 4, Target - Ni, Power, 150 W, Substrate Temperature 20C	**W 7.1-7.16** **WT 7.19-7.24**
9.2	Inspection: Ellipsometer	Ellipsometer VASE	Measure thickness on a testwafer T1	**WT 7.19** **Register in logbook.**
9.3	Inspection: AFM	AFM	Check film continuity	**WT 7.19** **Register in logbook.**

10 Contact deposition: backside

W 7.1-7.16, WT 7.19-7.24

10.1	Al film deposition	Wordentec	Expected thickness 300 nm	**Register in logbook.**

11 Lithography#2: 1.5 μm standard – Brightfield, negative: front side openings — **W 7.1-7.16**

11.1 Coat wafers backside	Gamma spinner	Coat the backside of the device wafers 1.5 μm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	**W 7.1-10, W 7.15-16**
11.2 Coat wafers backside	Gamma spinner	Coat the backside of the device wafers 2 μm AZ MiR 701 resist Recipe: 2 um 100mm_AZ MiR 701 with HMDS	**W 7.11-14**
11.3 Coat wafers frontside	Gamma spinner	Coat the front side of the device wafers 1.5 μm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	Note in logbook
11.4 Exposure	MA6-aligner	Align to alignment marks. Hard contact Exposure time: 13 sec (check logbook) Mask: **frontside Al2O3 mask**	Note time in logbook
11.5 Develop	Developer TMAH UV lithography	Pre-bake @ 110C for 60 secs, SP 60 secs.	**Register in logbook.**
11.6 Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	Note time in logbook
11.7 Post bake	110-250C oven	Post bake for 30 min at 150C.	**W 7.1-16**
11.8 Inspection: Optical	Optical microscope	Check pattern and alignment marks	**W 7.1** Note in measurement sheet.

12 Al2O3 etching in BHF — **W 7.1-7.16**

12.1 BHF	BHF	Prepare separate solution Etching rate: 30nm/min Time: 1-1.1 min	Investigate etch rate for Al2O3
12.2 Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
12.3 Inspection: Optical	Optical microscope	Check pattern and alignment marks	
12.4 Strip resist	Lift-off bench	Lift-off bath for 30 min.	
12.5 Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
12.6 Inspection: AFM	AFM	Measure step height Target: 30±10 nm	**W 7.1**

13 ALD Al2O3/TiO2 growth — **W 7.1-16, WT 7.17-24**

13.1 Oxide growth	ALD	200°C 1 cycle Al2O3 interlayer	**W 7.2, W 7.7, W 7.12, W 7.14 WT 7.21-22**
13.2 Oxide growth	ALD	80°C 5 nm (110cycles) TiO2 will be deposited on Al back layer	**W 7.1-16 WT 7.17-24**
13.3 Inspection: Ellipsometer	Ellipsometer VASE	Measure thickness on a testwafer T1	**WT 7.17 Register in logbook.**
13.4 Inspection: AFM	AFM	Measure step height, Target: 5 nm	**W 7.1** Note in measurement sheet
		:	

14 Lithography #3 – 2.2µm standard – Brightfield, negative: front side metal grid

W 7.1-7.16

14.1 Coat wafers backside	Gamma spinner	Coat the backside of the device wafers 1.5 µm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	**W 7.1-16**
14.2 Coat wafers frontside	Gamma spinner	Coat the front side of the device wafers 1.5 µm AZ MiR 701 resist Recipe: 1,5um 100mm_AZ MiR 701 with HMDS	**W 7.1-16** Note in logbook
14.3 Exposure	MA6-aligner	Align to alignment marks. Hard contact Exposure time: 13 sec (check logbook) Mask: **Front contact**	Resist thickness not checked Note time in logbook
14.4 Develop	Developer TMAH UV lithography	Pre-bake @ 110C for 60 secs, SP 60 secs.	**Register in logbook.**
14.5 Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
14.6 Inspection: Optical	Optical microscope	Check pattern and alignment marks	**W 7.1** Note in measurement sheet.

15 Contact deposition: frontside

W 7.1-7.10, WT 7.11-7.16

15.1 Deposition frontside	Alcatel, Wordentech	Metals to deposit: Al / TI - 300/5 nm	Note time in logbook
15.2 Inspection: Optical	Optical microscope	Check for completeness	**W 7.1-7.10, WT 7.11-7.16**
15.3 Lift-off	Lift-off bench	Leave wafers in acetone for 2-3 min. Start the US for 10 min. Rotate wafers and start US for another 10 min.	Fill the bench with Acetone until carrier is covered.
15.4 Rinse/dry	Wet bench/ Spin dryer	Rinse in DI water for 5 min (300±30 sec). Spin dry	
15.5 Inspection: Optical	Optical microscope	Check for completeness	**W 7.1-7.16, WT 7.17-7.24**
15.6 Inspection: AFM	AFM	Measure step height, Target:	Note in measurement sheet **W 7.1, W7.3**
15.7 Inspection: SEM	SEM	Check film continuity and cross section images	**W 7.1, W7.3**
15.8 Inspection: lifetime	MDP Lifetime measurements	Expected lifetime nSi=10-13ms, pSi=1.5-2 ms	**W 7.1-16 WT 7.17-24 Register in logbook.**
15.9 **IV measurements**	Light IV		
15.10 **IV measurements**	Dark IV		
15.11 **EQE**	R, EQE, IQE	Spectral Response	

C.4   Matlab Code

C.4.1   Illuminated IV Extraction Code

```matlab
%% Startup
% Clears workspace and closes all figures
clearvars
close all

% Defining constants
size = (0.5)^2*pi;
q = 1.602*10^(-19);
k = 1.38*10^(-23);
T = 293;
LightIntensity = 1000;

% Asking user for data folder
main = uigetdir;
cd(main);
f = dir;

% Preallocates for data
data = cell(length(f)-2,1);

% Getting data
for n = 1:length(f)-2
    data{n} = Light_IV_mean([main,'\' , f(n+2).name]);
end

%% Characteristic parameter extraction
% Preallocating for parameter extraction
l = length(data);
V = cell(1,l);
I = cell(1,l);
J = cell(1,l);
V_fit = cell(1,l);
J_fit = cell(1,l);
J_sc = zeros(1,l);
I_sc = zeros(1,l);
V_oc = zeros(1,l);

for n = 1:l
    % Extracting data
    V{n} = data{n}(:,1);
    I{n} = data{n}(:,2);
    J{n} = I{n}/size;

    % Fitting data
    p = polyfit(V{n},J{n},15);
    V_fit{n} = linspace(min(V{n}),max(V{n}));
```

```matlab
47        J_fit{n} = polyval(p, V_fit{n});
48        fit = @(x) polyval(p,x);
49
50     % Calculating Voc, Isc and Jsc
51     J_sc(n) = fit(0);
52     if J_sc(n) <= 0
53         J_sc(n) = 0;
54     end
55     I_sc(n) = J_sc(n)*size;
56     V_oc(n) = fzero(fit,0.3);
57     if V_oc(n) <= 0
58         V_oc(n) = 0;
59     end
60
61     % Power
62     P{n} = I{n}.*V{n};
63     pp = polyfit(V{n},P{n},15);
64      P_fit{n} = polyval(pp, V_fit{n});
65
66     % Max power
67      if max(P{n})<=0
68         Pmax(n) = 0;
69      else
70          Pmax(n) = max(P{n});
71     end
72
73     % Theoretical max power
74     theorPmax(n) = abs(I_sc(n)*V_oc(n));
75
76     % Fill factor
77     FF(n) = Pmax(n)/theorPmax(n);
78      if ~isfinite(FF(n))
79         FF(n) = 0;
80     end
81
82     % Efficiency
83     eta(n) = (Pmax(n)/(LightIntensity * size))*100;
84     if V_oc(n) == 0
85         eta(n) = 0
86     end
87 end
88
89 %% PLotting preparation
90 % Legends and labels
91 leg = f(3:length(f));
92 k = {leg.name};
93 for n = 1:length(k)
94     k{n} = k{n}(3:end);
95 end
96 le = length(V_oc);
97
```

```matlab
 98
 99  %% Parameter plot
100  fig_para = figure;
101  hold on
102
103  % Voc
104  subplot(2,2,1)
105  p1 = plot(1:l,V_oc,'--*');
106  title('Open circuit voltage - V_{oc}')
107  ylabel('Voltage [V]')
108  p1.Parent.XTick = 1:le;
109  p1.Parent.XTickLabel = k;
110  p1.Parent.XTickLabelRotation = 45;
111  p1.Parent.XLim = [1 le]
112
113  % Isc
114  subplot(2,2,2)
115  p2 = plot(1:l,J_sc*1000,'--*');
116  title('Short circuit current - I_{sc}')
117  ylabel('Current density [mA/cm^2]')
118  p2.Parent.XTick = 1:le;
119  p2.Parent.XTickLabel = k;
120  p2.Parent.XTickLabelRotation = 45;
121  p2.Parent.XLim = [1 le]
122
123  % FF
124  subplot(2,2,3)
125  p3 = plot(1:l,FF,'--*');
126  title('Fill factor - FF')
127  p3.Parent.XTick = 1:le;
128  p3.Parent.XTickLabel = k;
129  p3.Parent.XTickLabelRotation = 45;
130  p3.Parent.XLim = [1 le]
131
132  % Efficiency
133  subplot(2,2,4)
134  p4 = plot(1:l,eta,'--*');
135  title('Efficiency - \eta')
136  ylabel('Percentage [%]')
137  p4.Parent.XTick = 1:le;
138  p4.Parent.XTickLabel = k;
139  p4.Parent.XTickLabelRotation = 45;
140  p4.Parent.XLim = [1 le]
141
142  %% Light IV-curve plotting
143  fig_IV = figure;
144  hold all
145
146  % Defining linetypes
147  linetype = {'-*' '-o' '-+' '-p' '-x' '-s' '-d' '-^' '-h'};
148
```

```matlab
149  % Actual plotting
150  for n = 1:l
151      plot(V{n},J{n}*1000,linetype{n})
152  end
153
154  % Title, labels and legends
155  fig_IV.CurrentAxes.Box = 'on';
156  title('Oxygen ligth IV-curve, p-type')
157  xlabel('Voltage [V]')
158  ylabel('Current [mA/cm^2]')
159  legend(k{:});
160
161  % Creating lines and adjusting axis
162  li1 = line([0 0],[-10 10]);
163  li2 = line([-10 10],[0 0]);
164  axis([-0.5 0.5 -6 3]);
165
166  % Resets working directory
167  cd(main);
```

C.4.2   Dark IV Extraction Code

```matlab
%% Startup
% Clears the workspace and closes all figures.
clc
close all

% Defining constants
q = 1.602*10^(-19);
legends = 1.3806488*10^(-23);
T = 293;

% Size and type of sample is defined
% True = p-type,  False = n-type.
size = ((0.05)^2*pi);
type = true;

%% Acquiring data
% Aks the user for a data folder
main = uigetdir;
cd(main);
f = dir;

% Preallocating
le = length(f)-2;
datapara = ones(4,length(f)-2);
data = cell(le,1);

% Extracts estimated characteristic parameters and mean dark IV
    curves
for n = 1:le
    datapara(:,n) = dark_para([main,'\' , f(n+2).name],type);
end
datapara(datapara <= 0) = 0;
for n = 1:le
    data{n} = mean_data([main,'\' , f(n+2).name]);
end

%% Plotting all of the extracted parameters
% Creates figure for parameters
fig_para = figure;
titles = {'Ideality factor', 'Saturation current', 'Series
    resistance', 'Shunt resistance'};
ylab = {'' 'Current densisty [mA/cm^2]' 'Resistance [\Omega]' '
    Resistance [k\Omega]' };

% Plotting all parameters
for n = 1:length(datapara(:,1));
subplot(2,2,n)
plot(1:length(datapara(1,:)),datapara(n,:),'--*');
title(titles(n));
```

```matlab
47      ylabel(ylab(n))
48  end
49
50  % Getting labels for legends, etc.
51  leg = f(3:length(f));
52  legends = {leg.name};
53  for n = 1:length(legends)
54      legends{n} = legends{n}(3:end);
55  end
56
57  % Changing the labels
58  ax = findobj(fig_para.Children,'-property','XTickLabel');
59
60  for n = 1:length(ax);
61      ax(n).XTick = 1:le;
62      ax(n).XTickLabel = legends;
63      ax(n).XTickLabelRotation = 45;
64      ax(n).XLim = [1 le];
65  end
66
67  %% Creating Dark IV-curve plot.
68  % Figure is created
69  fig_plot = figure;
70  hold on
71
72  % Markers and linetypes is defined
73  markers = {'*' 'o' '+' 'pentagram' 'x' 'square' 'diamond' '^' '
         hexagram'};
74  linetypes = {'-*' '-o' '-+' '-p' '-x' '-s' '-d' '-^' '-h'};
75
76  % Plotting all the curves
77  for n = 1:le
78      fig_plot.CurrentAxes.ColorOrderIndex = n;
79      plot(data{n}(:,1),abs(data{n}(:,2)/size)*1000,'HandleVisibility
         ', 'off')
80      fig_plot.CurrentAxes.ColorOrderIndex = n;
81      plot(data{n}(1:10:end,1),abs(data{n}(1:10:end,2)/size)*1000,'
         Marker',markers{n},'LineStyle','none','HandleVisibility', '
         off')
82      fig_plot.CurrentAxes.ColorOrderIndex = n;
83      plot(data{n}(1,1),abs(data{n}(1,2)/size)*1000,linetypes{n})
84  end
85
86  % Adds title, labels, etc.
87  fig_plot.Children.YScale = 'log';
88  fig_plot.Children.Box = 'on';
89  title('Thickness dark IV-curve, p-type')
90  xlabel('Voltage [V]')
91  ylabel('Current density [mA/cm^2]')
92  legend(legends)
93  axis([-1 1 10^(-4) 10^3])
```

```matlab
94
95  %% Sets the working directory back to default
96  cd(main)

1   function M = dark_para(folder,type)
2   %% Constants
3   q = 1.602*10^(-19);
4   k = 1.3806488*10^(-23);
5   T = 293;
6   V_t = (k*T)/q;
7   size = ((0.05)^2*pi);
8
9   %% Loading the text files
10  cd(folder)
11  txtfiles = dir('*.txt');
12  list = {txtfiles.name};
13
14  %% Extracting the data
15  data = cell(length(list),1);
16  for d = 1:length(list);
17      data{d} = dlmread(list{d},'',11);
18  end
19
20  if type
21      for n = 1:length(data)
22          data{n} = flipud(data{n});
23          data{n}(:,1) = -data{n}(:,1);
24          data{n}(:,2) = -data{n}(:,2);
25      end
26  end
27
28  Rs = zeros(1,length(data));
29  Rsh = zeros(1,length(data));
30  ideality = zeros(2,length(data));
31
32  %% Estimating the shunt resistance
33  % At zero voltage the shunt resistance dominates the device.
34  % The resistance is equivalent to the inverse slope.
35
36  for n = 1:length(data);
37      d = and(data{n}(:,1) >= -0.1, data{n}(:,1) <= 0.1);
38      X = data{n}(d,1);
39      Y = data{n}(d,2);
40      p_rsh = polyfit(X,Y,1);
41      Rsh(n) = (1/abs(p_rsh(2)))/1000;
42  end
43
44
45  %% Ideality factor, Series resistance and I0
46
47  for n = 1:length(data)
```

```matlab
48      % Data for fitting
49      X_orig = data{n}(:,1);
50      Y_orig= real(log((data{n}(:,2))));
51
52      % Creates n_fit
53      int = and(X_orig >= 0.1, X_orig <= 0.2);
54      X = X_orig(int);
55      Y = Y_orig(int);
56      p_n = polyfit(X,Y,1);
57      n_fit = @(V) polyval(p_n,V);
58
59      n_real = (0.1)/(V_t*(n_fit(0.2)-n_fit(0.1)));
60      I0 = (exp(-p_n(1))*1000)/size;
61
62      % Estimates saturation current and ideality factor
63      ideality(1,n) = n_real;
64      ideality(2,n) = I0;
65
66      % Creates rs_fit
67      int = and(X_orig >= 0.8, X_orig <= 1);
68      X = X_orig(int);
69      Y = Y_orig(int);
70      p_rs = polyfit(X,Y,1);
71      rs_fit = @(V) polyval(p_rs,V);
72
73      % Calculates the series resistance
74      I_fitting = rs_fit(0.8);
75      n_v = @(v) I_fitting - n_fit(v);
76      rs_v = @(v) I_fitting - rs_fit(v);
77      dv = fzero(rs_v,0.8) - fzero(n_v,0.6);
78      rs = dv/exp(I_fitting);
79      Rs(n) = rs;
80  end
81
82  %% Output
83  % The rows of the output matrice is as follows: n, I0, Rs, Rsh.
84  extracted = [ideality; Rs; Rsh];
85
86  M = mean(extracted,2);
87  end
```

C.4.3 IV Mean Code

```matlab
function mean_IV = IV_mean(folder)
%% Searches for txt files in the given folder
cd(folder)
txtfiles = dir('*.txt');
list = {txtfiles.name};

%% Extracting the data of each txt file
data = cell(length(list),1);
for d = 1:length(list);
    data{d} = dlmread(list{d},'',11);
end

% Calculates the mean
mean_IV = zeros(size(data{1}));

for n = 1:length(data)
    mean_IV = mean_IV + data{n};
end

% Exports the mean Dark IV curve
mean_IV = mean_IV/length(data);
end
```

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