Transferred-Substrate InP/GaAsSb Heterojunction Bipolar Transistor Technology With fmax ~ 0.53 THz

Weimann, Nils G.; Johansen, Tom Keinicke; Stoppel, Dimitri; Matalla, Matthias; Brahem, Mohamed; Nosaeva, Ksenia; Boppel, Sebastian; Volkmer, Nicole; Ostermay, Ina; Krozer, Viktor

Total number of authors:
12

Published in:
I E E E Transactions on Electron Devices

Link to article, DOI:
10.1109/TED.2018.2854546

Publication date:
2018

Document Version
Peer reviewed version

Transferred-Substrate InP/GaAsSb Heterojunction Bipolar Transistor Technology With $f_{max} \sim 0.53$ THz

Nils G. Weimann, *Member, IEEE*, Tom K. Johansen, *Member, IEEE*, Dimitri Stoppel, Matthias Matalla, Mohamed Brahem, Ksenia Nosaeva, Sebastian Boppel, Nicole Volkmer, Ina Ostermay, Viktor Krozer, *Senior Member, IEEE*, Olivier Ostinelli, and Colombo R. Bolognesi, *Fellow, IEEE*

***Abstract*— We report on the realization of transferred-substrate InP/GaAsSb double heterostructure bipolar transistors in a terahertz monolithic integrated circuit process. Transistors with 0.4-μm-wide single emitters reached unilateral gain cutoff frequencies of around 530 GHz with simultaneous current gain cutoff frequencies above 350 GHz. Extrinsic collector capacitance is effectively reduced in the transfer-substrate process. In combination with the high collector breakdown voltage in the InP/GaAsSb heterobipolar transistor structure of 5 V, this process is amenable to analog power applications at millimeter (mm-wave) and sub-mm-wave frequencies. We demonstrate reliable extraction procedures for unilateral gain and current gain cutoff frequencies.**

***Index Terms*— Gallium arsenide antimonide, heterojunction bipolar transistors, indium phosphide, millimeter-wave (mm-wave) integrated circuits, submillimeter-wave (sub-mm-wave) integrated circuits.**

I. Introduction

THERE has been much recent progress in the realization of millimeter wave (mm-wave) and terahertz transistors, with the indium-based compound semiconductor devices demonstrating the highest cutoff frequencies to date. Both InAs-channel high-electron-mobility transistors (HEMTs) [1] and InP/InGaAs and InP/GaAsSb heterobipolar transistors (HBTs) [2], [3] with f_{max} around 1 THz have been reported. The combination of high electron mobility and high breakdown voltage makes the indium phosphide material system very suitable for RF power applications at sub-mm-wave and terahertz frequencies. High breakdown voltage translates directly into power handling and pulse operation capability. The open-base breakdown voltage BV_{CEO} of the current 90-nm SiGe HBT generation with $f_{max} \sim 700$ GHz amounts to less than 2 V [4] and is expected to shrink further with continued device scaling. In contrast, double heterostructure bipolar transistors (DHBTs) with InP collector exhibit $BV_{CEO} > 4$ V. Owing to the type-II band alignment between GaAsSb and InP, structures with a GaAsSb/InP base–collector junction can forgo the collector bandgap grading needed in InGaAs/InP devices, which is most often realized as a superlattice consisting of InGaAs and InAlAs. In an GaAsSb/InP HBT, the entire collector including the critical region below the base can be made from InP, leading to further improved breakdown characteristics and reduced thermal resistance in the collector by omission of the ternary grading layers.

Suppression of parasitic capacitance becomes ever more important as critical HBT dimensions are scaled to 100 nm and below. In traditional top-down triple-mesa device processing, the collector is processed last, and extrinsic capacitance may only be reduced through lateral undercut processes that are difficult to control. The transfer substrate method has been applied successfully by several research groups to break this scaling barrier (see [5], [6]). In our approach, the active device layers are transferred to a host substrate after the processing of the emitter and base structures is completed [7]. After wafer bonding and InP substrate release, the collector side of the device becomes accessible from the top, allowing for realignment and independent lithographic definition of the collector. This process enables the replacement of extrinsic semiconductor material ($\epsilon_r \sim 12$) by low-k benzocyclobutene (BCB) with $\epsilon_r = 2.65$ in the extrinsic collector region (Fig. 1), verifiable in a focused ion beam cross section shown in [8]. Furthermore, the transferred substrate process flow is amenable to post-CMOS monolithic heterogeneous integration [8], enabling system-on-chip integration of terahertz functionality.

Manuscript received April 19, 2018; revised June 7, 2018; accepted July 4, 2018. This work was supported by Leibniz Gemeinschaft at FBH through SAW Contract InP THz Transistor. The review of this paper was arranged by Editor P. J. Fay. *(Corresponding author: Nils G. Weimann.)*

N. G. Weimann is with the Components for High Frequency Electronics Department (BHE), Faculty of Engineering, University of Duisburg-Essen, 47057 Duisburg, Germany (e-mail: nils.weimann@ieee.org).

T. K. Johansen is with the Electromagnetic Systems Group, Department of Electrical Engineering, Technical University of Denmark, 2800 Kongens Lyngby, Denmark.

D. Stoppel, M. Matalla, M. Brahem, K. Nosaeva, S. Boppel, N. Volkmer, I. Ostermay, and V. Krozer are with the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, 12489 Berlin, Germany.

O. Ostinelli and C. R. Bolognesi are with the Millimeter-Wave Electronics Group, ETH Zürich, 8092 Zürich, Switzerland.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2854546

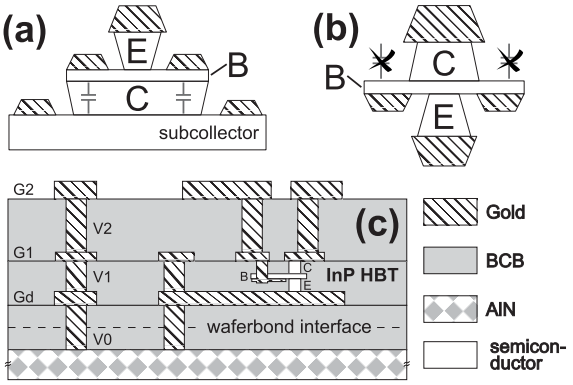


Fig. 1. Schematic of the transferred-substrate HBT process with indicated extrinsic base–collector capacitance. (a) Traditional top-down triple mesa HBT. (b) Transferred substrate InP HBT. (c) Cross section of our THz monolithic integrated circuit stack with interconnect wiring layers Gd, G1, and G2.

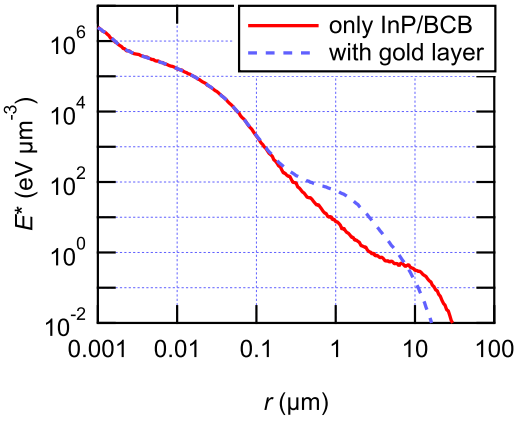


Fig. 2. Comparison of radial PSF with and without gold underground, for 50-keV incident electron energy. The energy density E^* is normalized to one electron.

In this paper, we report on the first realization of a monolithically integrated transferred substrate InP/GaAsSb DHBT process aimed at parasitic capacitance reduction, along with improved deembedding of measured S-parameters, and reliable extraction of the maximum frequency of oscillation $f_{\max}$.

II. Technology

First, the epitaxial structure was grown at ETHZ by metal-organic vapor phase epitaxy in a traditional emitter-up sequence on a 3" diameter semi-insulating ⟨100⟩ InP substrate, similar to the one described in [9]. The emitter consisted of 20-nm $Ga_{0.22}In_{0.78}P$ graded to InP with an n-dopant concentration of 2.5×10^{16} cm^{-3}. The base was 20 nm thick and carbon doped to 8.0×10^{19} cm^{-3}, with a composition graded from $GaAs_{0.41}Sb_{0.59}$ to $GaAs_{0.61}Sb_{0.39}$ at the emitter interface. The InP collector was 125 nm thick and n-doped to 1.3×10^{17} cm^{-3}.

The HBT device and circuit fabrication were done at Ferdinand-Braun-Institut. The three critical layers, emitter, base, and collector, were defined by electron-beam lithography with a 50 keV shaped-beam system (Vistec SB251). The remaining layers were patterned with i-line stepper lithography. First, single-finger and multifinger emitters with widths between 300 and 800 nm and lengths of 6 and 10 μm were defined by e-beam lithography and deposited by electron beam evaporation followed by conventional bilayer polymethyl methacrylate (PMMA) liftoff. The emitter mesa was wet-etched in dilute HCl, stopping on the GaAsSb base. The self-aligned base metal was e-beam evaporated over the emitter structures, again lifted off with a bilayer PMMA mask, and followed by inductively coupled plasma-enhanced chemical vapor deposition SiN_X passivation of the emitter–base diode. The SiN_X passivation layer, deposited at only 80 °C, leads to a significant improvement of device stability as compared to BCB passivation. HBT devices with 0.8×6-μm^2 emitter area were stressed on-wafer at 250-kA/cm^2 current density for 1000 h, resulting in current gain degradation of less than 10%.

Following passivation, the surface is planarized with BCB. A 2.5−μm-thick electroplated gold layer is added, providing the first interconnect layer Gd. Then, the structure is bonded face down on a ceramic AlN carrier substrate in a BCB waferbond process at 250 °C, followed by the wet-chemical release of the InP substrate in hot HCl. The wafer release etch stops on a 200-nm-thick sacrificial InGaAs layer between the InP substrate and the subcollector layer.

Processing continues with the subcollector now being the topmost layer. In contrast to triple-mesa processing, the collector contact can be placed here vertically onto the subcollector layer. The width of the collector is targeted ∼100 nm wider than the emitter to account for current spreading in the structure and marginal collector–emitter misalignment. The electron-beam lithography of the collector layer takes into account ∼140 ppm layout expansion during epilayer transfer in the cooldown cycle of the waferbond process caused mainly by the difference in a thermal expansion coefficient of the InP wafer and the ceramic AlN carrier substrate. The layout is precompensated to take up the bulk of the magnification. The remaining magnification error was corrected on the fly during the exposure by utilizing up to six local registration marks per die, resulting in a placement error of less than ±50 nm. The e-beam exposure is proximity corrected to account for the background changing according to the layout. In areas where the buried gold Gd layer is present, a modified point spread function (PSF) is used to calculate the dose correction (Fig. 2). The high Z-contrast of the gold in the 2.5-μm-thick layer significantly alters the PSF in the critical region around 1 μm. The PSF was simulated using the TRACER software package (GeniSys Inc.). The PSF was then used to calculate the dose assignment for each fractured polygon (Proxecco, Vistec Inc.).

The collector metal was deposited by electron beam evaporation and conventional liftoff, followed by wet chemical etch of the InGaAs subcollector and the InP collector material. The collector etch stops with high selectivity at the GaAsSb–InP interface, leaving only the 20-nm-thick base layer membrane. Following device mesa isolation by BCl_3 reactive ion etch, the structure is planarized with BCB. Contact holes are etched in the BCB layer to connect Gd and the base metal layer. The collector metal is exposed in a planar etchback step, similar to the connection between emitter metal and Gd.

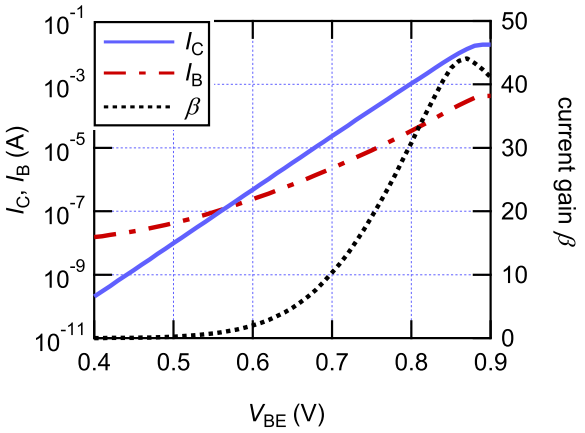


Fig. 3. Gummel plot ($V_{CB} = 0$) and dc current gain β. The collector current compliance was set at 18 mA.

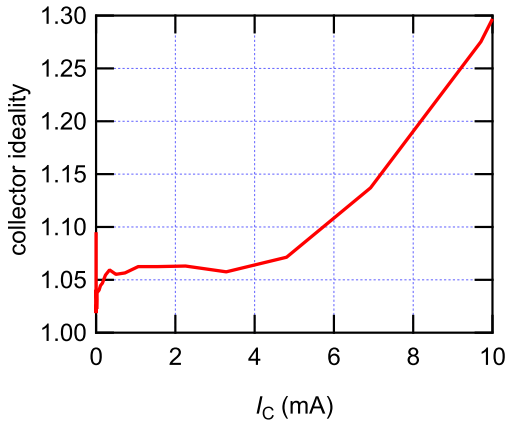


Fig. 4. Collector ideality factor from differentiated Gummel plot.

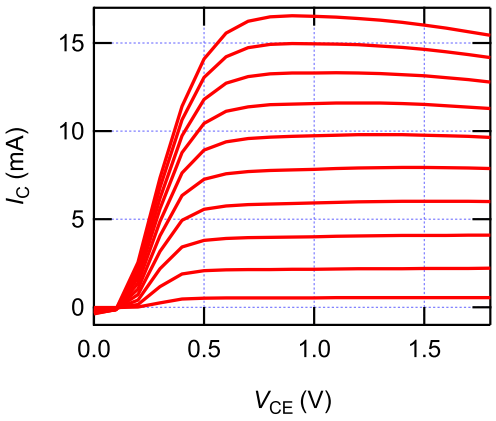


Fig. 5. Transistor output curve of 0.4 × 6 μm^2 emitter area device. The base current was increased from 20 to 380 μA in steps of 40 μA.

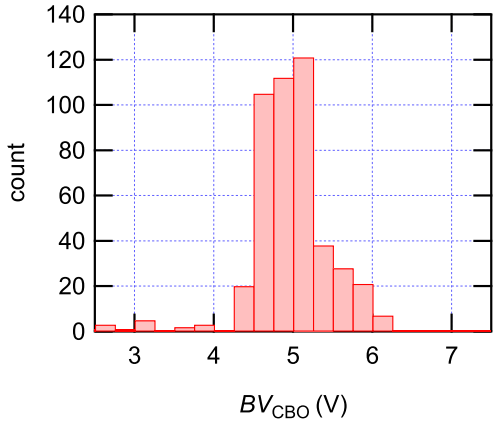


Fig. 6. Breakdown voltage BV_{CBO} distribution (at 1 kA/cm^2 reverse collector current density).

The terahertz monolithic integrated circuit process is completed with 1.5-μm-thick electroplated gold second interconnect metal G1, a further BCB interlayer dielectric, SiN_X thin-film capacitor (0.3 fF/μm^2), NiCr resistor (25 Ω/□), and 4.5-μm-thick electroplated gold final metal G2. The vertical distance amounts to 1 μm between Gd and G1 and 5.1 μm between Gd and G2, respectively. In this layer stack, 10-μm-wide microstrip lines in layer G2 over a ground plane in layer Gd exhibit 50 Ω impedance. A schematic cross section of the technology layers is shown in Fig. 1(c). Via V1 connects layers Gd and G1, and V2 connects G1 and G2, respectively. An additional via V0 is used to thermally connect RF-grounded areas to the AlN substrate.

III. HBT Device Measurements

A. DC Data

The transistors were characterized on-wafer with a standard coplanar probing. DC data were collected with 50 Ω terminated coplanar probe heads. The Gummel plot of a 0.4 × 6 − μm^2 device shows a peak current gain β of more than 40 (see Fig. 3). The collector ideality factor amounts to 1.06 in the low-injection regime (Fig. 4). The transistor output curve in Fig. 5 shows a low turn-ON voltage. The negative output conductance at higher current is indicative of self-heating. We calculated the HBT's thermal impedance to be ∼6 K/mW, higher than in triple-mesa devices of a similar geometry [10], [11]. The thermal implications of removing the InP substrate have been recognized before [6], [12], also when employing an InP/GaAsSb structure [13]: whereas the heat is dissipated cylindrically in the substrate under a triple-mesa device, the only heat extraction path in a transferred-substrate HBT is through the collector and emitter contacts. It can be reduced with additional heat sinking [6], [13], [14].

The breakdown behavior was assessed by measuring the base–collector diode reverse current. The base–collector breakdown voltage of more than 400 transistors was recorded, defining a breakdown at a reverse current of 1kA/cm^2. The distribution of BV_{CBO} is shown in Fig. 6, with a median of 5 V. Short term on-wafer dc stress measurement revealed a stable operation over several days under normal operating conditions (Fig. 7).

B. RF Data

For RF characterization, the transistors were measured on-wafer using a 110-GHz setup consisting of a PNA network vector analyzer (Keysight Inc.) with OML frequency extenders and 100-μm pitch Infinity coplanar probes from Cascade Microtech. The setup was calibrated to the probe tips with the augmented line-reflect-match procedure using an impedance standard substrate (ISS type 104–783) from

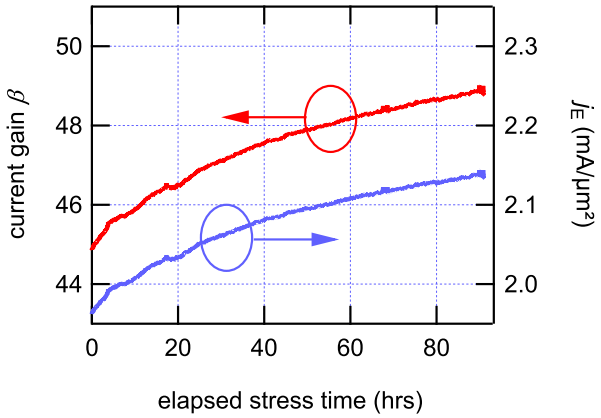


Fig. 7. Current gain β stability at ~200 kA/cm^2 emitter current density, $V_{CE} = 1.8$ V.

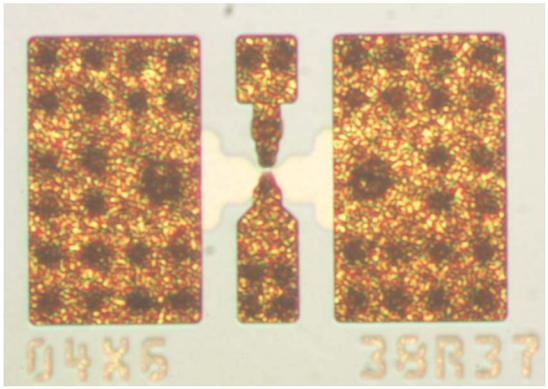


Fig. 8. Micrograph of coplanar waveguide HBT test structure. Base is connected to the top coplanar pad and collector to the bottom. Emitter is grounded.

Cascade Microtech. The bias point for RF extraction was $V_{CE} = 1.3$ V, $I_C = 10.5$ mA.

The low loss in the AlN carrier substrate, along with the elevated ground plane, may result in the propagation of substrate modes. Electromagnetic (EM) energy may be injected at the location of the RF probe pads, where the ground plane is not continuous. The calculation of Mason's unilateral gain U appears to be easily affected by parallel signal propagation in the substrate mode, manifesting itself in the observation of artifacts in the $|U(f)|$-plot, which occur at multiple fractions of the wavelength and make reliable determination of f_{max} from extrapolated values of $|U(f)|$ difficult. Transistors made in our transferred substrate technology connected with microstrip lines display strong aberrations of $|U|$ over frequency. In contrast, clean $|U(f)|$ data could be measured on HBTs connected in a short coplanar test frame (see Fig. 8). In principle, U is invariant with respect to transformations as represented by a reactive embedding network [15], which can be approximated by serial impedances Z_i and parallel admittances Y_i surrounding the device-under-test (DUT).

Proper extraction of intrinsic cutoff frequencies requires deembedding of the external parasitic elements. In general, the serial impedances are measured with the help of a representative SHORT, and the parallel admittances with an OPEN structure. The sequence of deembedding becomes important because of the small internal capacitance of scaled-terahertz devices, being the same magnitude or smaller than the line and pad capacitance of the RF test frame. In particular, the maximum frequency of oscillation f_{max} extrapolated from Mason's gain assumes different values for open-first and short-first deembedding, where the traditional SHORT–OPEN sequence [16] leads to an overestimation of f_{max}, while consecutive OPEN–SHORT deembedding leads to the opposite [3].

For accurate estimation of Mason's unilateral power gain at higher frequencies, a distributed deembedding approach should be employed. A representation as shown in Fig. 9 is often sufficient to model the pad configuration in a typical short coplanar waveguide (CPW) test frame [17]. In this representation, the parallel admittances, Y_i, are distributed between the outer pad structure and the transistor terminals according to a distribution factor α. The lumped-element approximation follows from a truncated Taylor series expansion of the input impedance for an open-circuited uniform transmission line (given as $Z_{in} = Z_0 \coth(\gamma l) \sim Z_0((1/\gamma l) + (1/3)\gamma l)$, where Z_0 is the characteristic impedance, $\gamma = \alpha + j\beta$ is the complex propagation constant, and l is the length of the access line leading from the outer pad to the transistor terminals). According to the lumped-element approximation, a distribution factor of $\alpha = 2/3$ is derived. In practice, however, the tapering of the pad structures and fringing fields off the open-ends, lead to a modification of this distribution factor. The distribution factor can be experimentally determined, e.g., if a pad-only deembedding structure is available along with the standard open and short deembedding structures [17]. Alternatively, the distribution factor can be determined from EM simulation of the deembedding structures. The corrected transistor two-port Y-parameters, Y_{DUT}, follow from

$$Y_{DUT} = \frac{1}{\frac{1}{Y_{MEAS} - \alpha \cdot Y_{OPEN}} - \frac{1}{Y_{SHORT} - \alpha \cdot Y_{OPEN}}} - (1-\alpha) \cdot Y_{OPEN}$$

where Y_{MEAS} denotes the measured two-port Y-parameters for the embedded DUT, Y_{OPEN} denotes the two-port Y-parameters measured on the open structure, and Y_{SHORT} denotes the two-port Y-parameters measured on the short structure [18]. Setting $\alpha = 1$ corresponds to the OPEN–SHORT deembedding technique while $\alpha = 0$ corresponds to the SHORT–OPEN deembedding technique. Here, we use an EM simulation approach to obtain the distribution factor α. Due to the difference in the layout on the base and collector side shown in Fig. 8, we obtain values of 0.6 for the base and 0.54 for the collector. To not overly complicate the extraction procedure, a value of α of 0.6 is chosen for both base and collector in the following.

The curves of $|h_{21}|$ and $|U|$ for different deembedding approaches with $\alpha = 0$, 0.6, and 1 are shown in Fig. 10. The unity-gain frequencies f_T and f_{max} are obtained by extrapolation along a line with a slope of -20 dB/dec between 30 and 90 GHz. The resulting frequencies are summarized in Table I. For the unity-current-gain frequency f_T, the differences between the deembedding methods are marginal, comparable to the uncertainty of the line fit (± 0.8 GHz). The

TABLE I
EXTRACTED UNITY-GAIN FREQUENCIES

	comp.	parameter α			iterative method [3]	
		0.0	0.6	1.0	single pole	−20 dB/dec
f_T (GHz)	no	368	370	371	373	370
	yes	374	372	371	376	373
f_{max} (GHz)	no	541	531	524	540	525
	yes	555	535	524	545	531

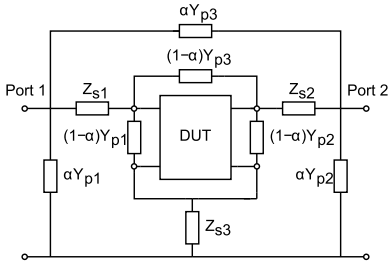


Fig. 9. Deembedding network without compensation.

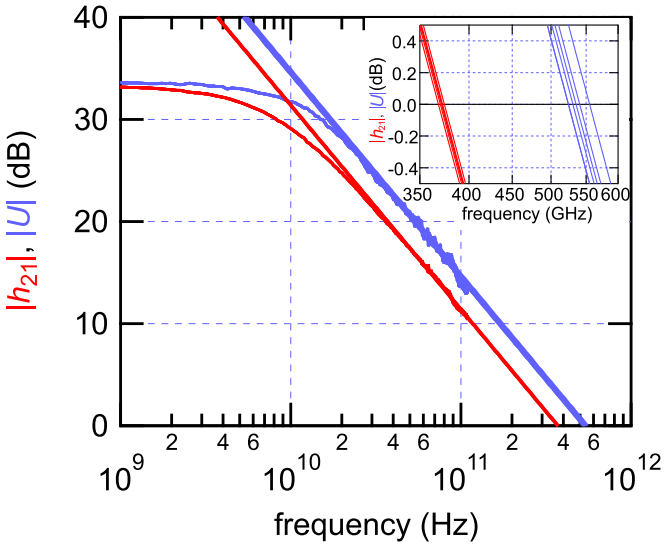


Fig. 10. Overlaid plot of $|h_{21}|$ and $|U|$ with the 2×3 different values of α versus frequency, extrapolated to f_T and f_{max} with −20 dB/dec slope. The insert shows a closeup of extrapolated small signal gain x-axis intercept, the values are given in Table I.

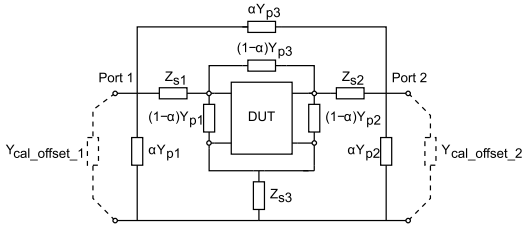


Fig. 11. Deembedding network with compensation.

maximum frequency of oscillation f_{max}, however, shows some dependence on the parameter α.

The probe-tip calibration followed by deembedding using on-wafer fabricated standards may lead to a residual calibration error. The residual calibration error is due to the differences in substrate permittivities and probe-tip-to-line geometry between the off-wafer ISS calibration substrate and the actual measurement wafer [19]. This residual calibration error is expected to be significant for the CPW test structures considered here. This is because the electric field of the coplanar waveguide mode is confined largely to the air–BCB ($\epsilon_r = 2.65$) interface as opposed to the air–alumina ($\epsilon_r = 9.9$) interface on the ISS calibration substrate. The effect of the residual calibration error can electrically be represented as admittances ($Y_{\text{cal\_offset\_1}}$ and $Y_{\text{cal\_offset\_2}}$) shunting the deembedding network at the location of the probe tips, as shown in Fig. 11. The distributed deembedding procedure will be erroneous if this residual calibration error is not compensated.

To correct the residual calibration error, the following two-step approach is proposed. In the first step, an EM simulation of the CPW open structure is performed to extract the expected values of open-structure capacitances. In the second step, the measurements of the embedded DUT, open structure, and short structure are all corrected for the calibration offset. For the EM simulation, an accurate 3-D model of the open structure was created in Ansys HFSS. Parasitic effects associated with the excitation of the on-wafer structure is calibrated out using the $L - 2L$ approach [20]. Comparison with the extracted open-structure capacitances from the measurement wafer allows the calibration offset to be compensated. The employed calibration offset compensation admittances are $Y_{\text{cal\_offset\_1}} = -j2\pi f \times 7$ fF and $Y_{\text{cal\_offset\_2}} = -j2\pi f \times 7.5$ fF, where f is the frequency. The offset capacitances are negative as the probe-tip calibrated measurements performed on-wafer will actually underestimate the open-structure capacitances. An improved calibration offset compensated the deembedding technique can now be formulated

$$Y_{\text{DUT}} = \left[\frac{1}{(Y_{\text{MEAS}} - Y_{\text{CAL\_OFFSET}}) - \alpha(Y_{\text{OPEN}} - Y_{\text{CAL\_OFFSET}})} - \frac{1}{(Y_{\text{SHORT}} - Y_{\text{CAL\_OFFSET}}) - \alpha(Y_{\text{OPEN}} - Y_{\text{CAL\_OFFSET}})}\right]^{-1} - (1-\alpha)(Y_{\text{OPEN}} - Y_{\text{CAL\_OFFSET}})$$

where $Y_{\text{CAL\_OFFSET}}$ is the diagonal matrix containing the compensation admittances $Y_{\text{cal\_offset\_1}}$ and $Y_{\text{cal\_offset\_2}}$. It is interesting to note that the above-mentioned deembedding technique still reduces to the OPEN–SHORT deembedding technique for $\alpha = 1$. The improvement due to compensation is only necessary in the case of distribution of the parallel admittances, Y_i, according to the parameter α.

Table I provides the summary of the extracted unity-gain frequencies, f_T and f_{max} for a $0.4 \times 6 - \mu\text{m}^2$ InP/GaAsSb HBT. As observed, the HBT in the short CPW test frame is relatively robust against the distribution factor regardless of whether the uncompensated or compensated deembedding technique is used. The variation range is from 523 to 546 GHz for the deembedding technique with no calibration offset compensation applied. For the improved calibration offset compensation deembedding technique, the variation range is from 523 to 535 GHz. For a distribution factor of $\alpha = 0.6$,

the calibration offset compensation deembedding technique leads to an extracted $f_{\max} = 535$ GHz.

As shown in Table I, we compare the results obtained from the here presented distributed deembedding to the iterative scheme proposed in [3], which exhibited convergence to the expected $f_{\max}$ value for a transistor embedded in a pad configuration consisting of uniform lossy transmission lines leading into the DUT. The column "single pole" contains the results considering the fit of the data spanning the entire frequency range to a single-pole response. The rightmost column shows the extrapolated cutoff frequencies using a −20-dB/dec fit between 30 and 90 GHz. Although the CPW test layout configuration as shown in Fig. 8 does not well resemble a uniform transmission line, similar values are obtained when applying the iterative deembedding approach following [3]. The distributed deembedding scheme can be expressed as a special case of the iterative algorithm when limiting the number of iterations to $N = 2$, and obtaining the weight α from 3-D EM simulations of the pad and test frame.

Compared to a triple-mesa device with the similar epitaxial structure [21] and $0.3 \times 9.4 - \mu\text{m}^2$ emitter area, which displayed peak f_T and $f_{\max}$ of 365 and 501 GHz at $j_E = 500$ kA/cm^2, the here-reported transferred-substrate device with 30% wider $0.4 \times 6 - \mu\text{m}^2$ emitter exhibited higher gain cutoff frequencies at lower current density.

IV. Conclusion

An InP/GaAsSb transferred-substrate HBT technology was demonstrated, with the potential to further sub-100-nm scalability. HBTs with an emitter area of 0.4×6 μm^2 yielded f_T and $f_{\max}$ of 370 and 535 GHz, respectively, at emitter-current density $j_E = 420$ kA/cm^2. The replacement of microstrip leads with short-coplanar sections resulted in clean unilateral gain data, facilitating reliable extraction of $f_{\max}$. A distributed deembedding method for terahertz HBTs in short coplanar test frames was applied, showing a good agreement with a previously published iterative method. The base–collector breakdown voltage with open emitter was measured to $\text{BV}_{\text{CBO}} = 5$ V, underscoring the RF power capability of InP/GaAsSb HBTs at mm-wave and terahertz frequencies.

Acknowledgment

The authors would like to thank the Process Technology Department, Ferdinand-Braun-Institut (FBH), in particular, S. Hochheim, D. Rentner, and J.-M. Koch, for wafer fabrication, S. Schultz of FBH for many detailed dc and RF on-wafer measurements, as well as W. Quan and A. M. Arabhavi of ETHZ for aid with the iterative deembedding.

References

[1] R. Lai *et al.*, "Sub 50 nm InP HEMT device with $f_{\max}$ greater than 1 THz," in *IEDM Tech. Dig.*, Dec. 2007, pp. 609–611.

[2] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130nm InP DHBTs with f_T >0.52THz and $f_{\max}$ >1.1THz," in *Proc. 69th Annu. Device Res. Conf. (DRC)*, Jun. 2011, pp. 281–282.

[3] C. R. Bolognesi, R. Flückiger, M. Alexandrova, W. Quan, R. Lövblom, and O. Ostinelli, "InP/GaAsSb DHBTs for THz applications and improved extraction of their cutoff frequencies," in *IEDM Tech. Dig.*, Dec. 2016, pp. 29.5.1–29.5.4.

[4] B. Heinemann *et al.*, "SiGe HBT with $f_T/f_{\max}$ of 505 GHz/720 GHz," in *IEDM Tech. Dig.*, Dec. 2016, pp. 3.1.1–3.1.4.

[5] Q. Lee *et al.*, "A >400 GHz $f_{\max}$ transferred-substrate heterojunction bipolar transistor IC technology," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 77–79, Mar. 1998.

[6] D. W. Scott *et al.*, "InP HBT transferred to higher thermal conductivity substrate," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 507–509, Apr. 2012.

[7] T. Kraemer, M. Rudolph, F. J. Schmueckle, J. Wuerfl, and G. Traenkle, "InP DHBT process in transferred-substrate technology with f_t and $f_{\max}$ over 400 GHz," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1897–1903, Sep. 2009.

[8] N. G. Weimann *et al.*, "SciFab—A wafer-level heterointegrated InP DHBT/SiGe BiCMOS foundry process for mm-wave applications," *Phys. Status Solidi A*, vol. 213, no. 4, pp. 909–916, 2016.

[9] R. Flückiger, R. Lövblom, M. Alexandrova, O. Ostinelli, and C. R. Bolognesi, "Type-II InP/GaAsSb double-heterojunction bipolar transistors with $f_{\text{MAX}} > 700$ GHz," *Appl. Phys. Exp.*, vol. 7, no. 3, p. 034105, 2014.

[10] I. Harrison, M. Dahlstrom, S. Krishnan, Z. Griffith, Y. M. Kim, and M. J. W. Rodwell, "Thermal limitations of InP HBTs in 80- and 160-gb ICs," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 529–534, Apr. 2004.

[11] V. E. Houtsma *et al.*, "Self-heating of submicrometer InP-InGaAs DHBTs," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 357–359, Jun. 2004.

[12] K. Nosaeva, N. Weimann, M. Rudolph, W. John, O. Krueger, and W. Heinrich, "Improved thermal management of InP transistors in transferred-substrate technology with diamond heat-spreading layer," *Electron. Lett.*, vol. 51, no. 13, pp. 1010–1012, Jun. 2015.

[13] Y. Shiratori, T. Hoshi, N. Kashio, K. Kurishima, and H. Matsuzaki, "Indium phosphide-based heterojunction bipolar transistors with metal subcollector fabricated using substrate-transfer technique," *NTT Tech. Rev.*, vol. 14, no. 11, pp. 1–6, 2016.

[14] K. Nosaeva *et al.*, "Multifinger indium phosphide double-heterostructure transistor circuit technology with integrated diamond heat sink layer," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1846–1852, May 2016.

[15] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Trans. Microw. Theory Techn.*, vol. 40, no. 5, pp. 864–879, May 1992.

[16] L. F. Tiemeijer and R. J. Havens, "A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 822–829, Mar. 2003.

[17] T. K. Johansen, R. Leblanc, J. Poulain, and V. Delmouly, "Direct extraction of inp/gaassb/inp dhbt equivalent-circuit elements from *S*-parameters measured at cut-off and normal bias conditions," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 115–124, Jan. 2016.

[18] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE Bipolar Circuits Technol. Meeting*, Minneapolis, MN, USA, Sep. 1991, pp. 188–191.

[19] G. Carchon, B. Nauwelaers, W. D. Raedt, D. Schreurs, and S. Vandenberghe, "Characterising differences between measurement and calibration wafer in probe-tip calibrations," *Electron. Lett.*, vol. 35, no. 13, pp. 1087–1088, Jun. 1999.

[20] T. K. Johansen, C. Jiang, D. Hadziabdic, and V. Krozer, "EM simulation accuracy enhancement for broadband modeling of on-wafer passive components," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Oct. 2007, pp. 447–450.

[21] R. Lovblom *et al.*, "InP/GaAsSb DHBTs with 500-GHz maximum oscillation frequency," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 629–631, May 2011.

Nils G. Weimann (S'96–M'99) received the Diploma degree (Hons.) in physics from the University of Stuttgart, Stuttgart, Germany, in 1996, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, USA, in 1999.

Since 2017, he has been the Chair Professor for High Frequency Electronic Components (BHE), Faculty of Engineering, University of Duisburg-Essen, Duisburg, Germany. His current research interests include nanoelectronic and nanooptoelectronic devices based on InP and GaN.

Tom K. Johansen (S'04–M'04) received the M.S. and Ph.D. degrees in electrical engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1999 and 2003, respectively.

In 1999, he joined the Electromagnetic Systems Group, DTU Elektro, Technical University of Denmark, where he is currently an Associate Professor. His current research interests include the modeling of high-frequency solid-state devices and millimeter-wave and sub-millimeter-wave integrated circuit design.

Dimitri Stoppel received the B.Eng. degree in microsystems technology and the M.Eng. degree in systems engineering from the University of Applied Sciences, Berlin, Germany, in 2012 and 2013, respectively. He is currently pursuing the Ph.D. degree with the Ferdinand-Braun-Institut, Berlin, with a focus on process development for InP-DHBT millimeter-wave monolithic integrated circuit processes.

Matthias Matalla received the Diploma degree in physics from Friedrich-Schiller-University Jena, Jena, Germany, in 1984.

From 1988 to 1991, he was a member of the Central Institute of Electron Physics (ZIE), Berlin, Germany. Since 1992, he has been with the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Berlin, Germany, where he is involved in electron beam lithography, mask manufacturing, and optical stepper lithography.

Mohamed Brahem received the B.Sc. and M.Sc. degrees in electronic engineering from the Polytechnic University of Turin, Turin, Italy, in 2012 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Ferdinand-Braun-Institut, Berlin, Germany, and the Technical University of Berlin, Berlin.

From 2014 to 2016, he was a member of the Design for Manufacturing Team, Infineon Technologies Austria, Villach, Austria.

Ksenia Nosaeva received the B.S. and M.S. degrees in electronics engineering from the Tomsk State University of Control Systems and Radio-Electronics, Tomsk, Russia, in 2007 and 2008, respectively, and the Dr.-Ing. degree in electrical engineering from the Berlin University of Technology, Berlin, Germany, in 2016.

She is currently with the Ferdinand-Braun-Institute, Leibniz Institute für Höchstfrequenztechnik, Berlin.

Sebastian Boppel received the Diploma degree in physics from the University of Heidelberg, Heidelberg, Germany, in 2008, and the Ph.D. degree from Goethe University Frankfurt, Frankfurt, Germany, in 2013.

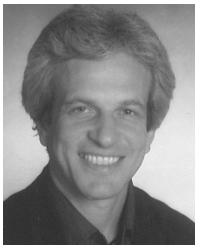
From 2008 to 2016, he was a member of the Ultrafast Spectroscopy and Terahertz Physics Group, Goethe University Frankfurt. He is currently the Head of the InP Devices Laboratory, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Berlin Germany.

Nicole Volkmer received the M.Sc. degree in microsystems technology from the University of Applied Science, Berlin, Germany. She is currently pursuing the Ph.D. degree with the Process Technology and GaN Power Electronics Department, Ferdinand-Braun-Institut, Berlin.

Her current research interests include thin-film technology, especially atomic layer deposition with a focus on aluminum oxide on vertical GaN MIS-FETs, as well as electrical device characterization.

Ina Ostermay received the M.Sc. degree in ceramic, glass, and construction materials from TU Freiberg, Freiberg, Germany, in 2006, and the Ph.D. degree from TU Dresden, Dresden, Germany.

Since 2013, she has been the Group Leader for thin-film deposition at the Ferdinand-Braun-Institut, Berlin, Germany. Her current research interests include the improvement of semiconductor processing including e-beam evaporation, sputtering, ALD, PECVD, and annealing processes.



Viktor Krozer (M'91–SM'03) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Technical University Darmstadt, Darmstadt, Germany, in 1984 and in 1991, respectively.

Since 2012, he has been the Head of the Goethe-Leibniz-Terahertz-Center, Johann Wolfgang Goethe University Frankfurt, Frankfurt, Germany. He is also leading the THz Components and Systems Group at the Ferdinand-Braun-Institut, Berlin, Germany.

Olivier Ostinelli received the M.Sc. and Ph.D. degrees in physics from ETH-Zürich, Zürich, Switzerland, in 2000 and 2006, respectively, with a focus on the development of long-wavelength vertical cavity lasers.

Since 2006, he has been a Senior Scientist with the MWE-Group, ETH-Zürich, where he is involved in epitaxial growth of advanced III–V heterostructure devices by metalorganic vapor phase and molecular beam epitaxy.

Colombo R. Bolognesi (S'84–M'94–SM'03–F'08) received the Ph.D. degree in electrical engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 1993, with a focus on InAs/AlSb HEMTs.

Since 2006, he has been a Professor of millimeter-wave electronics with ETH-Zürich, Zürich, Switzerland, where he leads the InP DHBT and GaInAs- and GaN-based HEMT research.