Advances in Bidirectional DC-DC Converters for Future Energy Systems

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Publication date:
2018

Document Version
Publisher's PDF, also known as Version of record

Technical University of Denmark

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Advances in Bidirectional dc-dc Converters for Future Energy Systems

Ph.D. Dissertation, August 2018

DTU Electrical Engineering
Department of Electrical Engineering

Kevin Tomas Manez

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Release date:	31$^{\text{th}}$ August 2018
Category:	1 (public)
Edition:	First
Comments:	This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree at the Technical University of Denmark.

Preface and Acknowledgment

This thesis is submitted in partial fulfilment of the requirements for obtaining Ph.D. degree at Technical University of Denmark. The research has been carried out at the Electronics group in the Elektro Department from September 2015 to August 2018 under the supervision of associate prof. Zhe Zhang and associate prof. Ziwei Ouyang.

The Ph.D. project entitled "Advances in Bidirectional dc-dc Converter for Future Energy Systems" is founded by the Danish Energy Technology Development and Demonstration Programme (EUDP).

My special thanks and deep appreciation to:

- My supervisors Zhe Zhang and Ziwei Ouyang, who gave me the opportunity to conduct the Ph.D. project. My deepest gratitude to Zhe Zhang, for his support and consistent encouragement that helped me finish this project and the endless talks and discussions.
- Prof. Michael A.E. Andersen, for being there when I needed support, and for valuable discussions and advise.
- To all who guided me through the elaboration of this thesis and helped reviewing it. To Zhe Zhang, Ziwei Ouyang, Martijn Duraij, Yasser Nour, Christian K. Lumby, Ahmed Ammar and Pere Llimos.
- All my colleagues at DTU Elektro for their help, support and constructive discussions, and of course, for the shared funny moments. My special gratitude to Henriette for making our group something more than a working place and for her endless support in any kind of matter; and to Hans-Christian for continuously improving our labs, his hard work and being always ready to give a hand.
- My deepest gratitude to all who made the difference, shared good and special moments, provide of help and advise without any hesitation and have always been there to support each other when we most needed it. To Yasser, Pere, Maria, Alexander, Ahmed, Gabriel and Yudi.
- To my family in Copenhagen. To the ones that left and the ones that still remain. All this would not have been possible without you. To Sepehr, Julio, Marcos, Jose, Martijn, Sergi, Hugo and Mpizos.
- To Maria. Thank you for your endless support in all my decisions, for your encouragement and for always believing in me.
- To my mother, Sussanna, my father, Jaume, and my sister Judith, for the unconditional love and encouragement. You are the pillars of my life, you made me feel proud of myself, you raised me to be the person I am today. I will never be able to thank you enough.
- And last but not least, a special gratitude to Denmark, that offered me the best weather ever recorded during the period I was locked in the office writing this thesis.

Abstract

The contemporary electricity grid is in the midst of a transformation in which decentralization of energy production is playing a key role. Spurred by the environmental concerns of traditional energy sources and the costs reduction of photovoltaic energy and energy storage systems (ESSs), energy decentralization is disrupting traditional models of energy generation. In addition, vehicle-to-grid technology has been presented as an opportunity to optimize the grid utilization. Considering that photovoltaic energy, energy storage systems and electrical vehicles operate in dc, the electricity network is following a trend of moving towards dc distribution in the form of multiple microgrids. Accordingly, technological advances that allow a simplified and flexible interconnection of microgrids with high energy efficiency are key enablers for the electricity grid transformation. In this regards, high efficiency power electronics interconnecting microgrids and integrating energy storage systems, constitute a main pillar for the development of microgrids and reaching high penetration of renewable energy sources.

The state-of-the-art technologies in electrical power conversion are trending towards the utilization of dc solid-state transformers (SST) as interlinking converters between dc grids. Among the different power converter topologies implemented as SSTs, the series-resonant converter (SRC) has been extensively used, thanks to its load regulation characteristics in open-loop together and its soft-switching conditions for wide power ranges.

This Ph.D. dissertation is divided into two parts. In the first part, the investigation of two-port and three-port SRCs in open-loop operation for dc SST applications is carried out and presented. The study focuses on the design considerations of distributed resonant tanks to improve the load regulations characteristics in open-loop operation at a fixed switching frequency and duty cycle. On this subject, the design criteria to operate multi-port SRCs in soft-switching at input and output ports is overviewed. The resonance frequency matching can pose a challenge in multi-port SRCs with distributed resonant tanks. Therefore, a resonance frequency matching process is proposed to address this issue. This methodology allows to remove the resonant inductors and solely use the stray inductances and leakage inductance of the multi-winding transformer as the inductive component of the resonant tank. As a result, the efficiency and power density of the converter can be highly increased. The SRC tends to have large root-square-mean (rms) currents due to the sinusoidal waveform of the resonant currents and the circulating energy required to achieve zero-voltage switching. So the conduction losses are usually high. The minimization of circulating energy by an optimal selection of dead-time and magnetizing inductance is also analysed. In this regard, wide bandgap semiconductors, which are widely known for their benefits in reduced switching loss, have a direct impact on the circulating energies. This introduces additional advantages into the SRC which have also been investigated. Some of these advantages are the reduction of conduction losses and turn-off losses.

In the second part of this PhD dissertation, different power converters configurations to integrate energy storage systems into the dc microgrid are investigated. Each of the converters presented aim to solve different challenges in the integration of ESSs. Firstly, a dual-active-bridge (DAB) derived topology for high voltage gain operation is

illustrated. The proposed topology features voltage and current stresses reduction as well as an additional degree of freedom to improve the DAB controllability. Secondly, a power conversion system which achieves a large reduction of the power processed by the dc-dc converter is presented. This solution focuses on the rearrangement of the dc-dc converter connection with the dc bus and the ESS. With this configuration, the system efficiency and power density can be largely increased, while the fabrication costs can be potentially reduced. Finally, a three port converter to integrate photovoltaic modules and the ESS into the microgrid is proposed. The converter is derived from conventional buck and boost topologies, hence its implementation is simple. High efficiency can be easily achieved since single energy conversion stages are required to transfer power between different ports.

Resumé

Det nuværende elforsyningsnet er under forandring, hvori decentralisering af energiproduktion spiller en væsentlig rolle. Ansporet af bekymringer for miljømæssige konsekvenser ved traditionelle energikilder samt den reducerende prisudvikling på markederne for solcelleenergi og energilagring er decentraliseringen ved at omvælte traditionelle modeller for energiproduktion. Ydermere er køretøj-til-hjem/køretøj-til-elnet teknologi blevet præsenteret som en mulighed for at optimere udnyttelsen af elnettet. Med tanke på at solcelleenergi, energilagringssystemer og elektriske køretøjer opererer ved dc, har elnettets udvikling tendens til at bevæges mod dc distribution i form af flere mikronet. Tilsvarende er den teknologiske udvikling, som muliggør en simple og fleksibel forbindelse mellem mikronet med høj nyttevirkning, i centrum af elnettets transformation. Effektelektronik med høj nyttevirkning ved forbindelse mellem mikronet og integration af energilagringssystemer spiller i den forbindelse en central rolle for udviklingen af mikronet og anvendelsen af vedvarende energikilder.

State-of-the-art teknologier indenfor energiomformning bevæger sig mod anvendelse af dc solid-state transformere (SST) som bindeled mellem dc net. Blandt de forskellige topologier for effektomformere implementeret som SST er serie-resonans omformeren (SRO) blevet ekstensivt anvendt grundet dens belastningsregulerings karakteristika ved åben sløjfe operation samt dens soft-switching betingelser for store effektområder.

Denne ph.d.-afhandling er inddelt i to dele. Den første del omhandler en undersøgelse af to-port og tre-port SROer i åben sløjfe til dc SST-anvendelser. Studiet fokuserer på overvejelser i forbindelse med design af distribuerede resonanstanke for at opnå høj belastningsregulerings karakteristika ved åben sløjfe operation med fast skiftefrekvens og duty cycle. Herunder gennemgås designkriteriet for at operere multi-port SROer i soft-switching ved indgangs- og udgangs-port. Tilpasning af resonansfrekvensen kan være en udfordring i multi-port SROer med distribuerede resonanstanke. Derfor foreslås en metode for tilpasning af resonansfrekvens til at adressere dette problem. Metoden tillader at resonansspolerne udelades til fordel for blot at benytte parasitisk induktans fra ledningsføring samt læk-induktans fra den flervundne transformer som den induktive komponent af resonanstanken. Som resultat heraf kan omformerens nyttevirkning og effekttæthed forøges betydeligt. SROen har normalvis store root-mean-square (rms) strømme grundet den sinusformede kurve på resonansstrømmene og den cirkulerende energi, som er nødvendig for at opnå zero-voltage switching. Derfor er ledetabene sædvanligvis høje. Muligheder for at minimere den cirkulerende energi undersøges ved at analysere optimale valg af dead-time og magnetiseringsinduktans. Herved konstateres det, at Gallium Nitrid (GaN) komponenter, som er velkendt for deres fordelagtigt lave skiftetab, har direkte indflydelse på de cirkulerende energier. Dette introducerer yderligere fordele ved SROen, hvilket også er blevet undersøgt. Disse fordele er blandt andet reduktion af (1) ledetab, (2) magnetiske viklingstab og (3) ESR tab for resonanskondensatoren.

I anden del af denne ph.d.-afhandling undersøges forskellige effektomformer konfigurationer til integration af energilagringssystemer i dc mikronettet. Hver af de præsenterede omformere forsøger at løse forskellige udfordringer ved integrationen af energilagringssystemer. Først illustreres en dual-active-bridge (DAB) afledt topologi til høj

spændingsforstærkning. Den foreslåede topologi har fordel af nedsatte spændings- og strømbelastning foruden en yderligere frihedsgrad til at forbedre DABens kontrollérbarhed. Dernæst præsenteres et system til effektomformning, der opnår stor reduktion af den effekt, som dc-dc omformeren behandler. Denne løsning fokuserer på en omordning af dc-dc omformerens forbindelse med dc-busen og energilagringssystemet. Med denne konfiguration kan systemets nyttevirkning og effekttæthed forøges væsentligt, mens fabrikationsomkostninger potentielt kan reduceres. Endeligt foreslås en tre-port omformer til at integrere solcellemoduler og energilagringssystemer i mikronettet. Omformeren er afledt fra konventionelle buck og boost topologier, hvorfor dens implementering er simpel. Høj nyttevirkning kan nemt opnås, eftersom enkeltstående energiomformningstrin er nødvendige to at flytte effekt mellem de forskellige porte.

Contents

Preface and Acknowledgement i

Abstract i

Resumé iv

List of Figures x

List of Tables xiii

1 Introduction 1

1.1 Background . . . 1
1.2 Project objectives . . . 2
1.3 Dissertation scope . . . 2
1.4 Thesis structure . . . 3

2 State-of-the-art 5

2.1 Future energy systems . . . 5
2.1.1 Energy storage systems . . . 7
2.2 Dc-dc power converters for the future energy systems . . . 9
2.2.1 Power converters for dc SST applications . . . 12
2.2.2 Power converters for ESSs . . . 14

3 Series Resonant Converter Dc Transformer 17

3.1 System description . . . 17
3.2 Operating principle of the SRC dc transformer . . . 20
3.2.1 SRC operating regions . . . 20
3.2.2 Steady-state operation . . . 22
3.3 Design considerations of the SRC dc transformer . . . 23
3.3.1 Zero-Voltage Switching . . . 23
3.3.2 Inductive operation . . . 24
3.3.3 Inherited load regulation characteristics . . . 27
3.3.4 Resonance frequency matching . . . 29

3.4 Design optimization for high efficiency operation . . . 33
3.4.1 Dead-time contribution to losses . . . 34
3.4.2 SRC performance improvements with GaN FETs . . . 36
3.4.3 Transformer design . . . 37
3.4.4 Resonant capacitors . . . 42
3.4.5 Efficiency analysis . . . 42
3.5 Experimental prototypes . . . 43
3.5.1 Prototypes summary . . . 44

4 Advances in Power Electronics for Energy Storage Systems 49

4.1 Partially Paralleled Dual Active Bridge Converter with Dual Phase-Shift Control . . . 49
4.1.1 Topology and operating principle . . . 50
4.1.2 Design considerations . . . 54
4.1.3 Experimental prototype . . . 55
4.2 Series-connected power conversion system . . . 56
4.2.1 System analysis . . . 56
4.2.2 Design considerations . . . 59
4.2.3 Dynamic power conversion system for SOEC/SOFC . . . 61
4.2.4 Series connected PCS with DAB converter for high voltage gain 61
4.2.5 Series connected PCS with an isolated boost dc-dc converter . . 62
4.3 Three-port dc-dc converter for PV-Battery systems with direct energy storage . . . 64
4.3.1 System analysis . . . 64
4.3.2 Topology and operating principle . . . 65
4.3.3 Modularity by interleaving . . . 67

5 Conclusion 69

6 Future work 73

6.1 Project proposals for the SRC dc Transformer . . . 73
6.2 Project proposals for the Partially Paralleled DAB . . . 73

Bibliography 75

Appendix 83

A List of Publications **83**

B Unregulated Series Resonant Converter for Interlinking DC Nanogrids **85**

C Multi-port Isolated LLC Resonant Converter for Distributed Energy Generation with Energy Storage **95**

D Design and Experimental Validations of a Bidirectional Three-Port Series-Resonant Solid-State Transformer **105**

E Three-Port Series-Resonant Converter DC Transformer with Integrated Magnetics for High Efficiency Operation **137**

F Dual Active Bridge DC-DC Converter with Extended Operation Range **147**

G High Voltage Gain Dual Active Bridge Converter with an Extended Operation Range for Renewable Energy Systems **179**

H Series-Connected Power Conversion System **187**

I High Efficiency Power Converter for a Doubly-fed SOEC/SOFC Systems **219**

J High efficiency non-isolated three port DC-DC converter for PV-battery systems **229**

List of Figures

1.1 Thesis outline. 4

2.1 Building block of ac microgrid system. 6

2.2 Building block of dc microgrid system. 6

2.3 Building block of multiple dc microgrid system. 7

2.4 Building block of dc solid-state transformer enabled dc microgrid. 8

2.5 Discharge curve of a lithium-ion battery. Datsheet:[1]. 9

2.6 Typical current-voltage characteristics of a SOEC/SOFC single cell. . . 10

2.7 High voltage gain and multiple ports integration through high frequency transformer. 10

2.8 Topology of the series resonant converter. 12

2.9 Topology of the dual active bridge. 12

2.10 Common dc gain characteristics for the DAB and SRC in terms of typical control parameter, i.e. phase angle for the DAB and switching frequency for the SRC, for different output power. 13

3.1 Structure of Chapter 3. 18

3.2 Series Resonant Converter for dc SST applications. 19

3.3 Dc gain curves of a resonant tank versus normalized frequency ω_n. . . . 21

3.4 Typical resonant current waveforms at the input side bridge i_{ri} and output side bridge i_{ro} when operating within the inductive region above the resonance frequency $\omega_n > 1$, at the resonance frequency $\omega_n = 1$ and below the resonance frequency $\omega_n < 1$ 21

3.5 Steady-state waveforms of the SRC when operating slightly below the resonance frequency. 23

3.6 Experimental results of ZVS operation for different output power. . . . 25

3.7 Dc gain characteristics of an arbitrary resonant tank when $m = m_{min}$. . 26

3.8 Resonant tank components size $L_{ri,max}$ and C_{ri} for $m = m_{min}$ versus t_d and ω_r. 27

3.9 Voltage limits of a microgrid with three dc buses. 28

3.10 Gain limitations of the SRC. The figure illustrates the SRC dc gain in terms of ω_n for different loads. The converter switching frequency is marked with f_s. The gain limitations according to the design specifications are $H_{i-o,min}$, $H_{i-o,max}$, $H_{o-i,min}$ and $H_{o-i,max}$, where i and o refers to the port number. 28

3.11 Dc gain characteristics vs inductance ratio m for different ω_n. 29

3.12 Experimental results of the steady-state dc gain of a 3P-SRC for a resonant tank with $m = 20$. 30

3.13 Experimental results of the steady-state dc gain of a 3P-SRC for a resonant tank with $m = 80$. 30

3.14 Voltage regulation with power fluctuations of the 3P-SRC. Port 3(V_3) is regulated at 400 V, while ports 1 (V_1) and 2 (V_2) are the unregulated ports. Inputs: Port 1 and 2; Output: Port 3. 31

3.15 Resonance frequency matching methodology. (a) Measurement set-up for Port-1: the gain after the resonant capacitor is measured with a Bode analyser. (b) Equivalent circuit of the measurement set-up, where $L_{r1,eq}$ is the overall resonant inductance seen from Port-1. (c) Measured bode plot and equivalent resonance frequency due to C_{r1} and $L_{r,eq1}$. . . 32

3.16 Voltage gain measurement before compensation with all the resonant tank components. 33

3.17 Voltage gain measurement and equivalent resonance frequency from each port. 33

3.18 Voltage gain measurement and resonance frequency after compensation with all the resonant tank components. 34

3.19 Theoretical per-unit rms currents versus dead-time under different load conditions, where the rms current base value is the dc port current I. . 35

3.20 Semiconductors' losses proportional to the power output in percentage versus t_d for different output power. 36

3.21 Theoretical per-unit rms currents in function of dead-time, where the rms current base value is the dc port current I. 38

3.22 Conduction losses in function of dead-time. 39

3.23 Switching losses in function of dead-time. 39

3.24 Total semiconductors losses in function of dead-time. 39

3.25 Simplified flowchart of the algorithm used to design the optimized transformer. 40

3.26 Theoretical efficiency of 3P-SRC in terms of resonance frequency and resonant components size. Efficiency is calculated for dual-output mode with equal power sharing among ports. 43

3.27 Design flowchart when using integrated resonant inductors. 44

4.1 Topology of the proposed P^{2}DAB converter. 50

4.2 Switching patterns of HB-LV1 ($S_1 - S_4$), HB-LV2 ($S_{1_2} - S_{4_2}$) and HB-HV ($Q_1 - Q_4$), ac inductor current i_{Lac} and voltage v_{Lac}. 51

4.3 Transferred power in terms of φ and φ_p, where the the base unit is $nV_1V_2/4f_sL_{ac}$. 52

4.4 Transferred power in terms of $\Delta\varphi$ for $\varphi_p = 0$ and $\varphi_p = 0.2$. 52

4.5 Experimental waveforms of the reflected LVs voltage $n(v_{1,1} + v_{1,2})$, voltage v_2 and ac inductor current i_{Lac} with different phase shift angles φ_p and φ. 53

4.6 Average input current $I_{in1,avg}$ and $I_{in2,avg}$ in terms of phase shift angle φ and φ_p. 55

4.7 Ac voltage and current on the LVs of the P^{2}DAB converter. 55

4.8 Experimental waveforms of voltage v_1, voltage v_{12}, current i_1 and current i_2. 56

4.9 Picture of the P^{2}DAB converter prototype. 57

4.10 Efficiency curves of the P^{2}DAB converter prototype. 57

4.11 Block diagram of a grid connected power conversion system for energy storage. 58

4.12 Efficiency and power density improvements with the series connection power conversion system. 59

4.13 Electrical characteristics of RFCs. 60

4.14 Dc-dc converter voltage and power rating in function of ESS power. . . 60

4.15 Overall system efficiency for different η_{dc-dc} 60

4.16 Dc-dc converter specification for ESS with different voltage ratings of the ESS. The legend shows the open-circuit voltage of different ESS configurations. 61

4.17 Efficiency measurements of the dynamic conversion system in SOFC and SOEC mode. 62

4.18 Schematic of the S-PCS with a DAB converter. 62

4.19 Picture of the test site. 63

4.20 I-V characteristics of the SOEC/SOFC tested. 63

4.21 Experimental waveforms of the series-connected DAB - RFC system. . . 64

4.22 Power flow of the three-port dc-dc converter for a PV-Battery system. . 65

4.23 Schematic of the three-port dc-dc converter. 66

4.24 Equivalent circuits for all operating modes. 66

4.25 Schematic of the two stages interleaved three-port dc-dc converter. . . . 67

4.26 Picture of the three port dc-dc converter prototype. 68

4.27 Picture of the coupled inductors. 68

6.1 A high voltage gain DAB converter with multiple partially paralleled LV bridges. 74

List of Tables

2.1 Review of Solid State Transformers. 13

2.2 Review of bidirectional dc-dc converters for ESSs. 16

3.1 Specifications for the TP-SRC 34

3.2 Specifications of the Silicon devices used in the analysis. 35

3.3 Specifications of the GaN devices used in the analysis. 37

3.4 Transformer specifications 42

4.1 Specifications for the P^2DAB converter. 55

4.2 Specifications for Lithium-ion batteries. 58

4.3 Specifications for the three-port dc-dc converter. 65

1

Introduction

1.1 Background

We live in a world that runs on electricity. The flow of electrons shapes our daily lives in everything we produce and everything we do. Alternating current (ac) powers our grid, street-lights and freezers, while direct current (dc) supplies our everyday devices such as phones, laptops and and cars. Ac and dc have cooperated for decades, but now the world needs more power than ever before [2, 3] and with smaller environmental impact. In a *"more dc world"*, we will be able to connect more efficiently renewable energy sources (RES) in extremely remote locations, wherever the wind is blowing, water flowing or sun is shinning [4, 5]. We will be able to capture the energy of the sun and transfer it from Sahara to Scandinavia or anywhere in between [5]. Electrical vehicles can be pulled up to any corner street and charge up as fast as it takes to have a coffee break [6]. Extremely energy consumers data centres will be capable to store and serve billions of web pages using less resources and space [7, 8]. Buildings and homes will be have the capacity to feed dc power directly and efficiently to the devices that run on dc power like appliances, computers and lightening [9–11]. Moving towards a distribution system with higher grade of dc where each kilowatt counts, we could live in a more efficient and reliable world while limiting the environmental impact.

In the last two decades, the integration of RES into our society has experienced an extraordinary development which is constantly progressing [2, 3]. Spurred by the costs decrease in photovoltaic (PV) panels and the high feed-in tariff, the decentralization of energy production has been advancing together with the development of RES. Besides the economic benefits for costumers and the environmental impact, distributed energy systems will grant the deferral of capital investment to maintain and upgrade grids to support load growth [5, 12]. As RES increase, the need for distributed storage will become essential. Without energy storage systems (ESS), when the production of electricity from RES exceeds the demand, negative pricing might occur and energy would be lost. ESSs adds flexibility to the system by balancing the energy production and the demand and thus, making a more effective use of the energy and preventing disruptive economics [12]. Moreover, through energy storage, additional services can be added to enhance the distribution system reliability and flexibility such as, frequency regulation, voltage support or backup power [13].

Thanks to the benefits of dc distribution and the tremendous increase of RESs and ESSs, future energy systems in residential applications are envisioned to evolve into multiple dc and ac microgrids [10, 11, 14–16]. Power electronics are a key component to fuel the potential of this evolution. In fact, power converters are used to interconnect

all the units that compose the electrical distribution grid, such as PV panels, batteries and loads. In addition, in dc distribution systems, power converters play the role of the core transformer in conventional ac distribution systems, wherein they operate as power conditioning and as power routers among the multiple dc grids. The research areas in power electronics which will reinforce the electricity grid transformation range from improvements in interoperability of systems, manufacturability, reliability, modularity and scalability, reduction of costs and high efficiency power converters [5, 12, 17, 18]

1.2 Project objectives

High efficiency power electronics are a driving force for the disruption of dc distribution and empower the high penetration of RES and ESSs. Therefore, the aim of this project is to identify current limitations and challenges within power conversion in dc distribution and ESSs and to envision the opportunities that this challenges bring to the development of alternative high efficiency power conversion systems. Accordingly, the main objectives and/or contributions of this PhD project are summarized below:

- To identify the trends of power electronics for residential dc distribution and/or microgrids.
- To investigate the utilization of unregulated solid-state transformers as power routers between microgrids.
- To demonstrate high efficiency bidirectional dc-dc converters to interconnct multiple dc grids. The aim is to achieve dc-dc conversion efficiency of 99 % over wide power ranges.
- To identify the challenges for high efficiency power converters in energy storage applications.
- To investigate and propose alternative solutions for high efficiency power converters in energy storage applications. The aim is to achieve dc-dc conversion above 98 % in high voltage gain and wide voltage range operation.

1.3 Dissertation scope

This dissertation summarizes and presents a more complete overview of the results achieved throughout the Ph.D. project entitled *Advances in Bidirectional dc-dc Converter for Future Energy Systems* which has been carried out from September 2015 until August 2018. The research carried out during this Ph.D. project has been presented or submitted in the form of peer review conference and journal papers as well as patent applications. These publications and patent applications constitute an essential part of this dissertation and hence, are included in the Appendices. In addition, App.A presents the list of publications, where joint publications, which has not been included in the Appendices, are also listed.

1.4 Thesis structure

The structure and content of the PhD dissertation are illustrated with Fig.1.1.

Chapter 1: Covers the background and motivation of this PhD project, describes the scope of the thesis and the project objectives and gives an overview of the content of the thesis.

Chapter 2: Describes the state-of-the art in microgrids and ESSs, and the review of high efficiency dc-dc converters for these applications.

Chapter 3: Presents the series-resonant converter in open-loop operation as a solid-state transformer to interconnect dc distribution systems. The design considerations for the specific application and design improvements for high efficiency operation are investigated.

Chapter 4: Presents three different solutions aiming to overcome different challenges of the energy storage systems.

Chapter 5: Summarizes the research and results obtained, conclude on the work presented in this thesis and describes the future work.

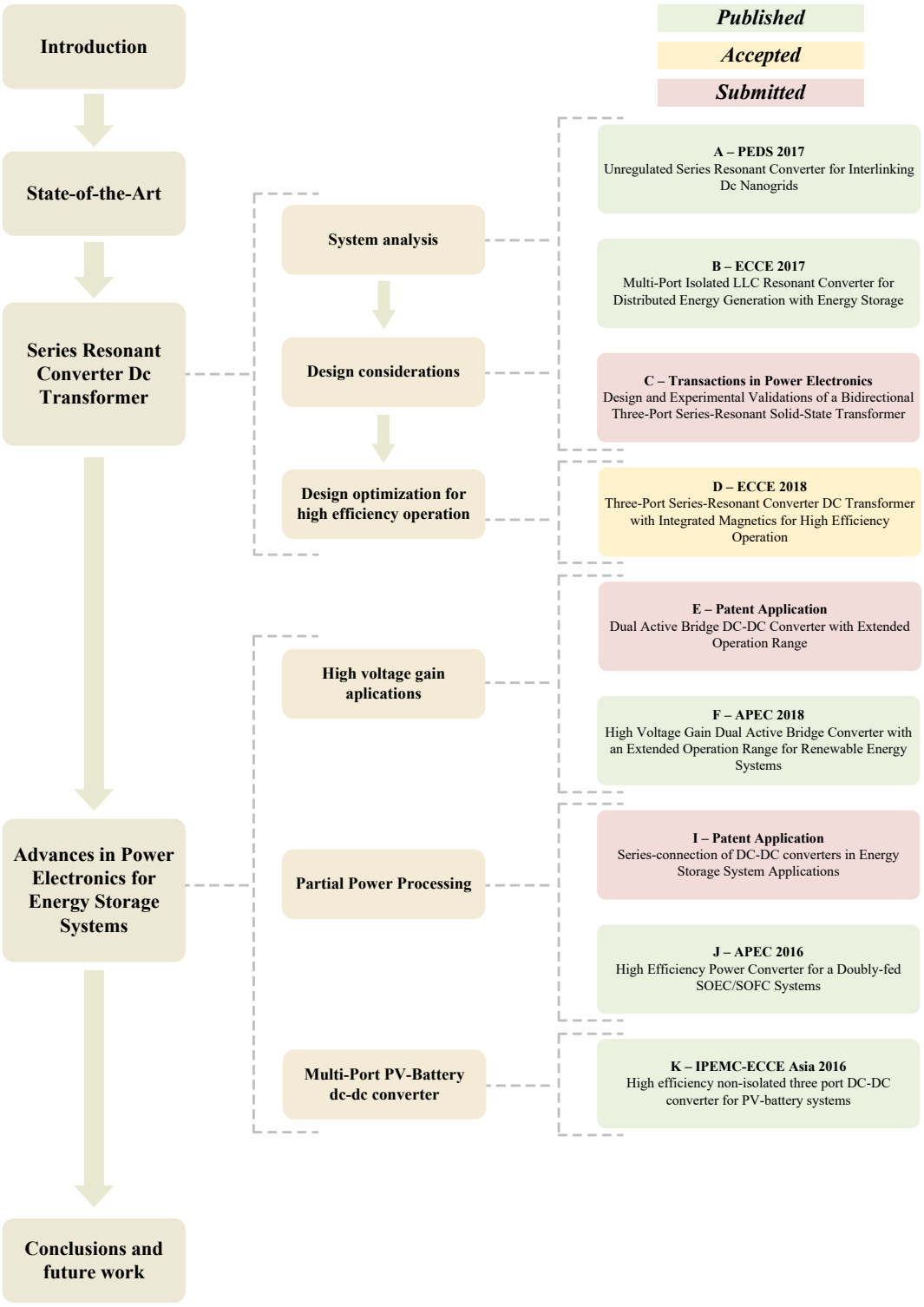


Figure 1.1: Thesis outline.

2

State-of-the-art

2.1 Future energy systems

In the recent years our society has been immersed in environmental issues of centralized traditional energy sources. In addition, the ageing of current distributions system and the growing demand of electrical energy have stressed this concerns. Even though the promising recent developments in energy decentralizations by means of renewable energy sources (RES) [2, 3], the increasing penetration of distributed energy sources into the traditional ac grid can cause additional problems such as voltage and frequency unstability [19, 20]. In order to solve these problems concepts such as "Microgrids" and "Smart grids" for the future distribution systems have been proposed. The microgrid concept was originally proposed in 2002 [21] and its operating principle was based on the principle of aggregating multiple micro-sources and loads into a single entity which can be interpreted as a single dispatch-able consumer and producer from the power systems perspective [13]. Nowadays, most of the microgrids are based on the traditional ac grid system as shown with Fig.2.1. However, large number of the units forming the microgrid generate dc voltages, e.g. photovoltaic (PV) panels, energy storage systems (ESSs) or electric vehicles (EV). These units require of dc-dc and dc-ac power converters to transfer or absorb power from the ac grid. These multiple power conversion stages increase the total energy consumption as well as reduces its reliability [10, 17]. More recently, microgrids systems based on a dc grid, as shown in Fig.2.2, have been proposed. Compared to the traditional ac grid, the dc grid can bring many advantages as (1) fewer power converters are required resulting in higher efficiency, higher power density and lower costs [7, 10, 22], (2) easier system integration, since issues related to the reactive power or grid synchronization are eliminated [8, 10] , (3) higher efficiency in the power transmission, since there is no skin effect and ac losses [23] and (4) grid connected loads such as computers or lightning systems can be directly powered by the dc system [8, 14]. During the last decade, research on microgrids architectures has been established as a research topic by itself where the key features are control flexibility, robustness and reliability [13].

Conventionally,a microgrid structure with direct connection of the ESS to the dc bus has been the most popular. Direct connection of battery stacks to the dc bus results in very high system robustness due to the high capacitance of the ESS and the dynamic stability. On the other hand, the uncontollable voltage of the dc bus, which mostly depends of the battery state-of-charge, makes this system poorly flexible [13]. Interconnecting ESSs through power converters, allows an active regulation of the dc bus voltage and thus, flexibility of the system is largely increased [13, 22]. From this struc-

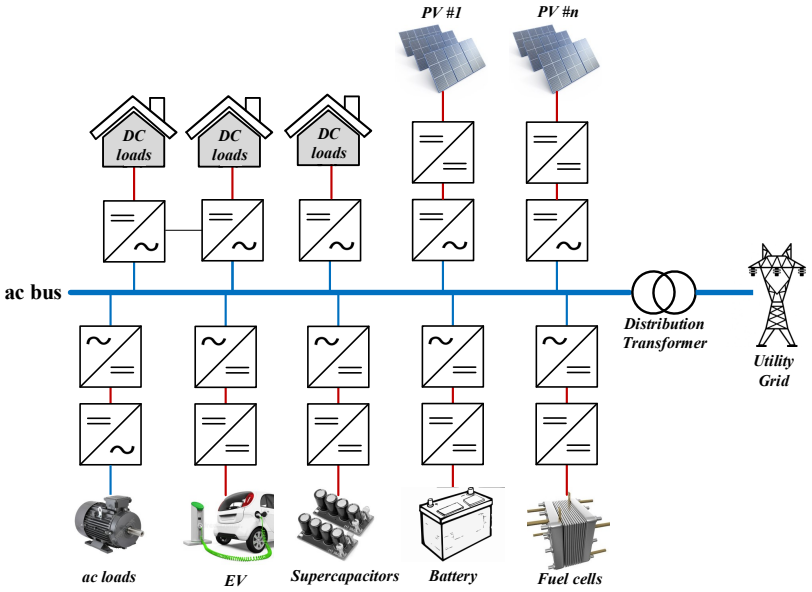


Figure 2.1: Building block of ac microgrid system.

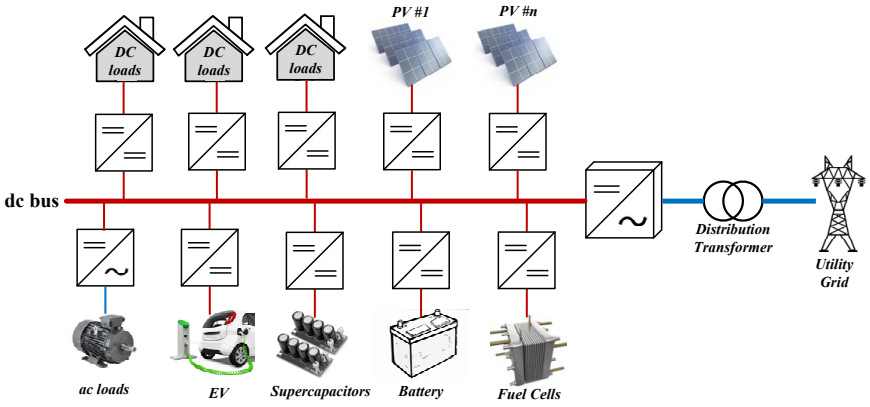


Figure 2.2: Building block of dc microgrid system.

ture, multiple other architectures have been studied in the literature [8, 10, 13, 14, 24]. As isllustrated with Fig.2.3, microgrids in future energy saving buildings is envisioned to have multiple dc grids at different voltage levels for powering high voltage loads such as heating, ventilation or kitchen loads and low voltage loads such as computers or light-emitting diodes [8, 10, 14]. Although many efforts have been carried out to reach a consensus for standards on dc grids [25–30], the standardization is still one of the biggest barriers for the incursion of microgrids into the power system.

The smart grid and microgrid scenario with high penetration of RES is going to be further enhanced by ensuring a production, distribution and use of the energy as efficient as possible. In that terms, power electronics are being seriously considered as one of the key technologies that will empower the future energy systems at all levels of the electrical system. Using highly efficient power electronics in power generation, power transmission, power distribution and at end-user applications, can pave the way to the smart grid [12, 18, 31–33].

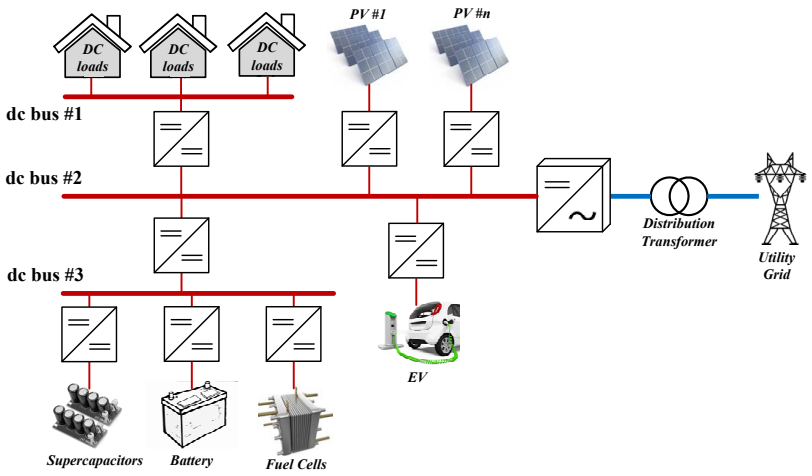


Figure 2.3: Building block of multiple dc microgrid system.

On this subject, during the last decade, a new power converter named solid-state transformer (SST) has caught much attention and been extensively studied for the distribution system [24]. Initially, the SST was proposed as a dc-dc converter with a high-frequency transformer to replace the utility grid line frequency transformer [24, 34]. Recently, the idea of a dc SST has also been proposed as an energy router in multi-bus dc microgrids as shown in Fig.2.4 [24, 35, 36]. Therefore, only single-stage conversion is needed to transfer power between the different dc grids.

In dc microgrid systems such as the one illustrated in Fig.2.4, the key components forming the dc cluster are summarized below:

- Renewable energy sources RES (PVs) and interfacing dc-dc converters.
- Energy storage systems ESSs (e.g. batteries and fuel cells).
- Interlinking converters (dc SSTs).
- Storage interfacing converters (bidirectional dc-dc converters).

2.1.1 Energy storage systems

Another key element to enhance the smart grids irruption into the electrical grid is the integration of stationary storage systems. The uncontrollable and inherent characteristics of RES introduce additional issues with system stability, reliability and power quality [19, 20, 37]. ESSs provide an effective way of balancing power supply and consumption, in order to decouple energy generation from demand [31]. Moreover, ESSs can be used to address power quality issues and improve the system flexibility by providing ancillary services to the grid [38–41]. This makes the ESS indispensable in order to efficiently and reliably deliver sustainable, economic and secure electricity supply in the future distribution systems [38–41].

The main ESS for grid applications are summarized in[42, 43]:

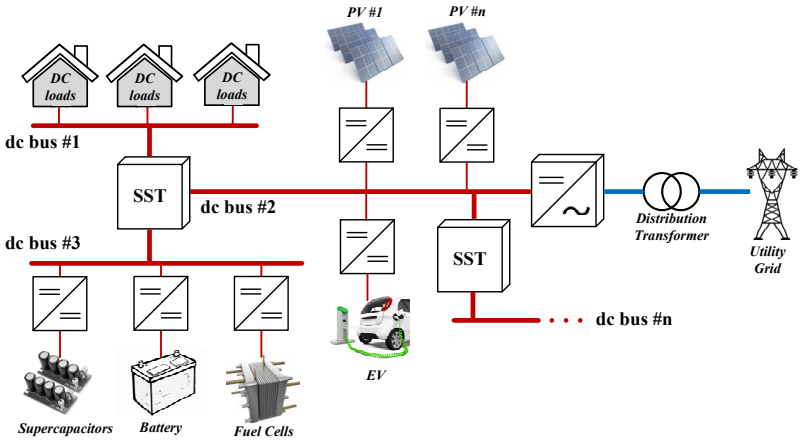


Figure 2.4: Building block of dc solid-state transformer enabled dc microgrid.

- Batteries
- Regenerative fuel cells
- Pumped-hydro
- Flywheels
- Thermoelectric
- Super-capacitors

The selection of the ESS depends on the application and factors such as power and energy ratings, response time, weight and size and operating temperature [43, 44]. Reviews of ESSs for grid applications with RES can be found in [37, 43]. In residential applications, batteries are the most widely used ESS, where high energy-to-weight ratios are required [43]. On the other hand, regenerative fuel cells (RFC) represent an attractive alternative due to their high energy density and lower environmental disposal concerns [44, 45].

Batteries :

Batteries can be found in many types depending on its chemistry [46]. In residential and EV applications most of the ESSs are lead-acid or lithium-ion based battery systems. Typical nominal voltages of a single cell battery range between 1.2 V to 3.8 V [44, 46] depending on the chemistry. Therefore, battery suppliers provide battery packs with multiple number of cells stacked in series to achieve higher operating voltages and energy storage capacity. Typical nominal voltages of battery packs can be found in the low voltage range 12 V-50 V [47] to higher voltage ranges 350 V-550 V [48–50] depending on the application.

Although the electrical characteristics of batteries might differ with the technology used, typical discharge curves are similar to the one illustrated with Fig.2.5. The battery capacity or state-of-charge (SOC) determines the terminal voltage, which is usually flat and located around the nominal voltage V_{nom}. The nominal voltage is also dependent on other factors such as temperature or cycle-life. Typically, batteries are charged and discharged at a constant current until reaching the depth of discharge

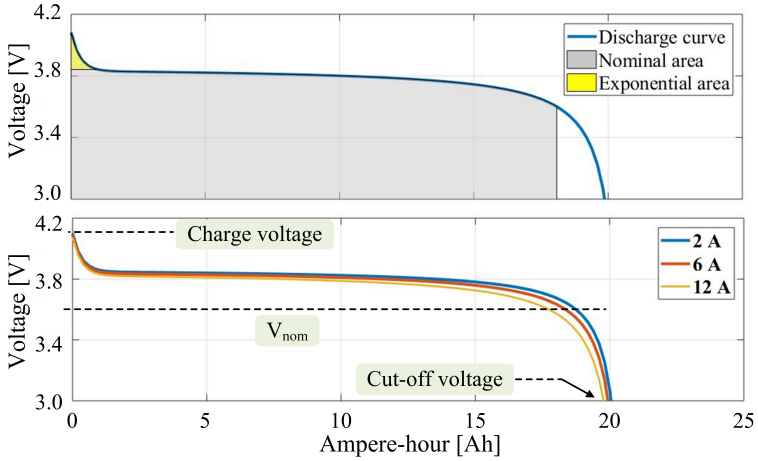


Figure 2.5: Discharge curve of a lithium-ion battery. Datsheet:[1].

limits. When approaching the SOC superior and inferior limits, i.e. charge voltage and cut-off voltage respectively, constant voltage is applied to avoid any hazardous conditions such as battery overcharging or going beyond the cut-off voltage and charge voltage[38, 51]. Therefore, power converters in battery applications should operate in wide voltage ranges where its optimised operation should be around the battery nominal voltage.

Regenerative fuel cells :

Fuel cells are another kind of electrochemical device that uses a chemical reaction to produce electricity directly from the fuel. Typical example of a fuel cell technology is the hydrogen-based solid oxide. These types of fuel cells have been proved to have bidirectional capabilities, also recalled as Solid oxide electrolyzed cells /fuel cells (SOEC-SOFC) or regenerative fuel cells (RFC) [45].

Electrical characteristics of RFC are dependent on a number of factors such as operating temperature, fuel composition or fuel pressure. Nevertheless, typical current-voltage characteristics of a single cell can be represented as illustrated with Fig.2.6. Although the mechanical processes of SOEC and SOFC are founded on the same basis, due to variation in the internal resistance and the current direction, the operating voltage in SOFC mode (discharging mode) is lower than in SOEC mode (charging mode) [52, 53]. In addition, in some cases tests demonstrated that power capability in SOEC mode is larger than in SOFC mode. Higher voltage ranges and power ranges are also achieved by stacking RFC in series.

Differently from the batteries, where normal operation is around the nominal voltage, RFCs nominal operation can range from maximum to minimum voltage. This requires of power electronic interfaces capable of operating in wide voltage ranges at the highest efficiency possible.

2.2 Dc-dc power converters for the future energy systems

Current activity towards high efficiency power electronics is mainly driven by three research areas, (I) converter topologies and system architectures, (II) control techniques

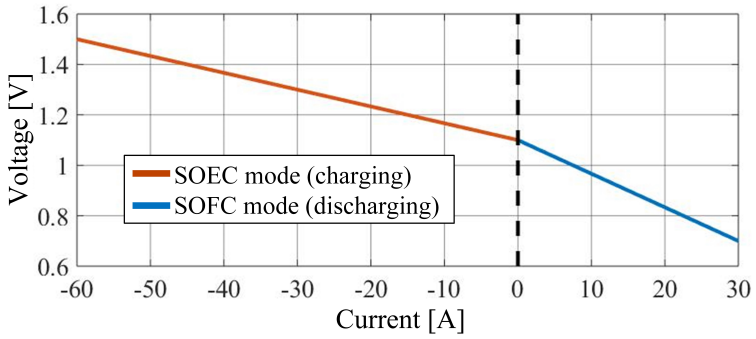
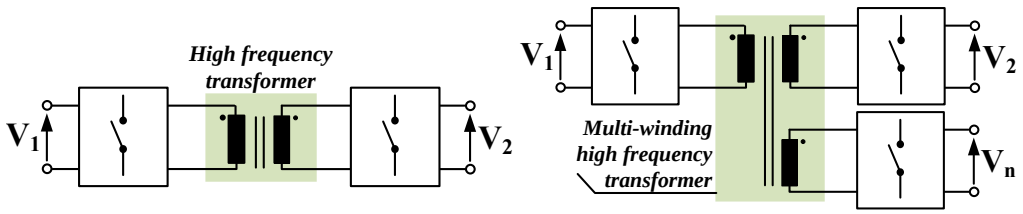


Figure 2.6: Typical current-voltage characteristics of a SOEC/SOFC single cell.



(a) Two ports configuration. **(b)** Three ports configuration.

Figure 2.7: High voltage gain and multiple ports integration through high frequency transformer.

and (III) wide bandgap semiconductor devices.

From the topological viewpoint, research in bidirectional isolated dc-dc converters have gained increased attention during the past years. Due to the nature of each system, large different voltage levels have to be accommodated by the power converters. This has stimulated the interest on isolated power converters, even when galvanic isolation is not a requirement. The magnetic element, besides due to its conventional advantages regarding reliability, reduced noise and electromagnetic interference (EMI), it is also used to achieve certain dc gain ranges. In addition, the magnetic link from the high frequency transformer also eases the interconnection of multiple dc buses. As illustrated in Fig.2.7, multiple active switching bridges can be coupled to a multi-winding transformer, while the switching signals from each bridge can be used to regulate the voltage at each port and the power flow. In that way, the number of power conversion stages can be reduced, which can result in potential improvements in terms of efficiency and power density.

Conventional bidirectional isolated dc-dc converters are composed by at least one energy storage element, a capacitor, an inductor or a combination of two, and a bidirectional switching bridge connected at each of the transformer. Voltage and power flow is regulated at a constant switching frequency with pulse-width modulation (PWM). Authors in [54, 55] presented a review of conventional step-up/-down bidirectional isolated dc-dc converters. In the recent years, conventional isolated dc-dc converters have evolved into more complex topologies with the objective of increasing the system efficiency among other features, such as power density and reliability. In this aspect, soft-switching topologies have become popular in the academia as well as the industry. In soft-switching converters, the voltage or current during the semiconductors' switch-

ing transitions are zero. In that way, the energy related to the switching is zero and thus, the switching losses are highly reduced. Thanks to the lower switching losses, dc-dc converters can operate at higher switching frequency, which allows the implementation of high efficiency and high power density converters. Moreover, as a result of a reduction in the dv/dt and di/dt at switch turn-on and turn-off, soft-switching converters can potentially reduce the EMI [56, 57].

Soft-switching operation of a semiconductor device can be broadly classified into zero-current switching (ZCS) and zero-voltage switching (ZVS). In ZCS operation, the current flowing through the semiconductor is reduced to zero before the voltage across it increases. Contrarily, in ZVS operation, the voltage across the switching devices is brought to zero before the current increases. Different soft-switching techniques and converter topologies to achieve ZVS and ZCS operation have been studied in the literature [56] such as the resonant switching transitions by means of auxiliary circuits, ZVS through discontinuous conduction mode and the resonant and quasi-resonant power converters.

The traditional power converter topologies for soft-switching operation are the so-called resonant power converters. Resonant conversion in power electronics was firstly proposed in 1970 by F.C. Schwarz [58]. Resonant converters are composed by a switching bridge generating a voltage pulse which excites a resonant tank, creating a sinusoidal current at the primary side circuit. This sinusoidal current is transferred and scaled to the secondary side bridge and filtered by the output capacitance. Due to the sinusoidal current, the switches at the input and output bridges can operate with soft-switching. The resonant tank contains L-C networks which resonance frequency is tuned to match the fundamental component of the excitation voltage, i.e. the switching frequency. The dc voltage and current magnitudes can be regulated by changing the switching frequency closer or further from the resonance frequency. A multitude of resonant tank networks can be utilized to achieve different dc gain and resonant conversion characteristics [59]. From all the isolated resonant power converter topologies, one of the most popular is the series-resonant converter (SRC) or LLC converter. The SRC is composed by a series L-C network connected in series to the high-frequency transformer. The circuit schematic of a full-bridge SRC is shown in Fig.2.8. The SRC features ZVS at the input side switches and ZCS at the output side switches. At the same time, turn-off at the input side switches is carried out at low current, which leads to even lower switching losses. In addition, soft-switching operation and the current at turn-off is not load-dependent, but voltage dependent. This makes the SRC topology very attractive for applications with constant dc voltages, such as microgrid applications. On the other hand, in the SRC, ZVS is achieved with the magnetizing current of the transformer. This additional circulating current added up to the sinusoidal shape of the resonant current, results in larger rms currents and hence, higher conduction losses.

Beside the SRC, one of the most promising and studied soft-switched converter topologies in the past years is the dual-active-bridge (DAB) converter. The DAB was firstly proposed in 1991 by De Doncker [60]. The DAB converter topology is shown in Fig.2.9. Two full-bridges are interconnected with a high frequency transformer that provides both galvanic isolation and energy storage in its leakage inductance. Larger energy storage is achieved utilizing external ac inductors in series with the transformer. The two full-bridges typically operate at a fixed switching frequency and 50 % duty cycle, and the phase shift angle between the two bridges is used to control the magnitude and direction of power flow. Unlike other isolated dc-dc converter topologies, the DAB

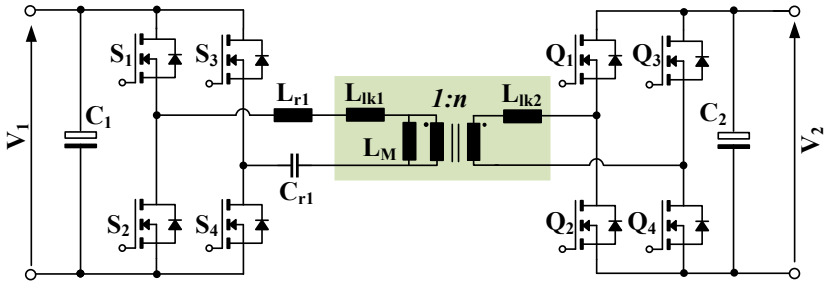


Figure 2.8: Topology of the series resonant converter.

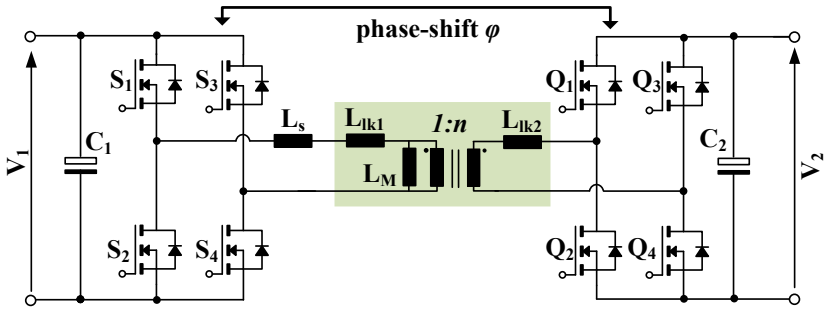


Figure 2.9: Topology of the dual active bridge.

has a symmetrical configuration, which enables bidirectional power flow with identical dc gain characteristics. By means of phase-shift modulation (PSM), the transformer current waveform becomes trapezoidal and delayed from the primary side transformer voltage. In that way, the energy stored in the transformer leakage inductance and the ac inductor after the primary side turn-off event is reused to achieve ZVS. Because of the trapezoidal shape of the transformer current and the reduced circulating current, the DAB bridge typically features reduced rms currents compared to the SRC [61]. On the other hand, turn-off commutation is carried out at larger current, which leads to increased switching losses [61]. Moreover, the transformer current is load dependent and thus, ZVS is lost under light load conditions [61]. The DAB bridge has been extensively studied since it was firstly proposed and multiple modulation strategies and topological variations have been addressed to improve its soft-switching characteristics and reduce the switching loss [62–72].

2.2.1 Power converters for dc SST applications

For all the aforementioned reasons, the DAB and SRC are the most popular power converter topologies used in dc SST applications to interconnect dc buses. In App.D a review of SSTs based on the DAB and SRC has been performed and Table 2.1 presents the review summary.

The DAB, in contrast to the SRC, allows the integration of multiple active bridge coupled with a multi-winding transformer, wherein the phase-shift angle between each bridge can be used to control the power flow and regulate the voltage across each

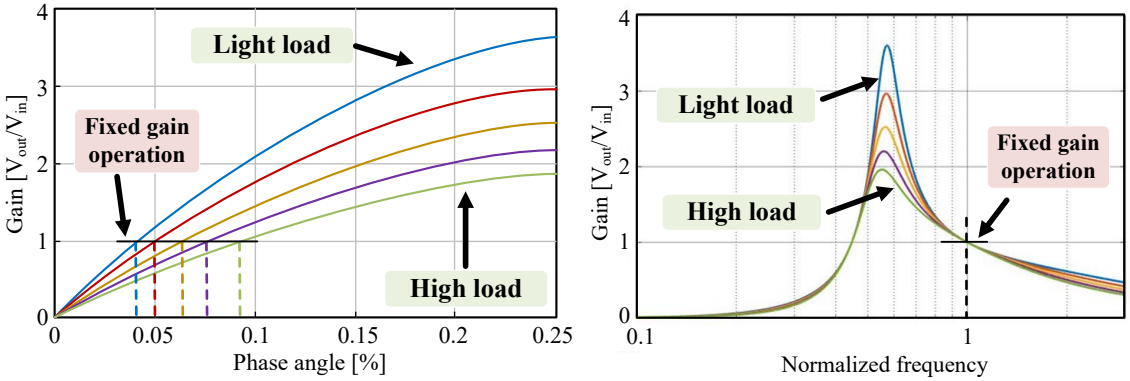
Table 2.1: Review of Solid State Transformers.

	DAB-based topologies				SRC-based topologies		
Study	[73]	[74]	[75]	[36]	[76]	[77]	[78]
Year	2014	2018	2008	2013	2013	2016	2018
Power Flow	⇒	⇒	⇔	⇔	⇔	⇒	⇔
No. ports (n)	2	2	3	4	2	2	2
Control	PSM	PSM	PSM	PSM	PFM + PWM	Open-loop	Open-loop
Voltage rating	3.6 kV;	343 V,	300 V;	48 V; 48 V;	380 V;	700 V;	760 V;
(V_1; ...; V_n)	200 V	120 V	42 V; 14 V	48 V; 48 V	380 V	600 V	380 V
Power rating	9 kW	800 W	1.5 kW	240 W	5 kW	10 kW	6 kW
Sw. frequency	3.6 kHz	20 kHz	100 kHz	20 kHz	55 kHz-70 kHz	20 kHz	100 kHz
Max. efficiency	92 %	96.3 %	91.7 %	-	97.8 %	98.61 %	97.8 %

port. This makes the DAB an interesting topology for multi-port applications where voltage regulation at each port has to be carried out by the dc SST. On the other hand, the SRC presents inherited load regulation characteristics when operating at the resonance region, which makes it suitable for open-loop operation. Fig.2.10 shows the dc gain characteristics of the DAB and SRC for different output power in function of the control parameter, where for the DAB is the phase shift angle φ and for the SRC is the normalized frequency. It can be observed that for the DAB the control parameter has to be actively regulated to maintain the same voltage gain under power fluctuations. Otherwise, the SRC can operate at a fixed switching frequency and fixed unity gain under power fluctuations. The SRC operating at the unity gain region is also known as dc transformer. In applications with constant dc bus voltages, such as microgrid and smart grid applications, the SRC dc transformer presents additional advantages into the system: (1) avoids the necessity of control loops, reducing the complexity of the control circuitry and software, (2) less number of sensors are required, (3) soft-switching operation under all operating conditions and (4) allows an optimal and simplified design for high efficiency and power density.

During the past couple of years, the SRC dc transformer has gained an increasing attention due to its advantages in dc SST applications [34, 69, 77–86]. Studies carried about the SRC dc transformer cover issues such as topology derivations to improve the performance of the converter [81, 82], reliability [77], high frequency operation with wide bandgap devices [86] or components design for high efficiency and power density [84, 87]. However, the design methodology of the open-loop SRC differs from the conventional closed-loop SRC. Design considerations such as maximum power transfer for soft-switching operation, load regulation to fulfil the design requirements or accurate selection of the resonant tank components and dead-time for reduced circulating energy were not fully covered in the literature by the start of this project.

Moreover, for applications where multi-port dc SSTs are required to interconnect multiple dc buses, SRCs with three or more ports can be used. The three-port SRC (3P-SRC) was first proposed by [88]. The circuit topology presented in [88] operates at a fixed switching frequency with a centralized PSM scheme to regulate voltage and power flow. However, investigations about multi-port SRC dc transformer and its de-



(a) Dual-Active Bridge Converter. **(b)** Series Resonant Converter.

Figure 2.10: Common dc gain characteristics for the DAB and SRC in terms of typical control parameter, i.e. phase angle for the DAB and switching frequency for the SRC, for different output power.

sign considerations have not been reported yet. In chapter 3 all the literature gaps regarding design considerations for the two-port and three-port SRC are covered and verified with experimental prototypes.

2.2.2 Power converters for ESSs

Research challenges in power electronics for ESSs integration lay on the high efficiency operation with high voltage gain and in some cases, coupled with wide voltage ranges, as in RFC applications. In non-isolated topologies, the basic approach to achieve high voltage gain is the utilization of cascaded dc-dc converters. In high-power applications, where efficiency is a concern, it is often beneficial to use magnetic coupling to achieve higher voltage gain ratios. Interleaved configurations are also used in high current applications to reduce current stress on semiconductor devices and decrease the size of passive components. However, electrical isolation is often required in grid-connected applications where reliable power transfer with low noise and EMI are needed.

The DAB and SRC topologies are also popular isolated dc-dc converter topologies in ESS applications. However, in wide voltage range applications, their efficiency performance degradates [89]. It has been studied that, in some cases, their losses can be even higher than in traditional bidirectional isolated topologies [90]. Table 2.2 shows a review of bidirectional dc-dc converters for wide voltage range applications based on the SRC, the DAB converter and the boost full-bridge and half bridge converter.

The SRC, for instance, has to operate in wide frequency ranges to regulate wide voltage ranges. This increases the complexity of the magnetics design as well as the converter loses. In [91] the efficiency of the SRC is analysed under different output voltages. In this study, the efficiency of the SRC drops almost a 1.5 % when the operating voltage is 29 % below the optimal output voltage. Different approaches are proposed in the literature to improve the efficiency performance of the SRC in wide voltage range applications. In [76, 92–96] optimised design methodologies for the resonant tank components to achieve high efficiency operation are presented. Nowadays, first harmonic approximation (FHA) is the most used and simplest way to design the SRC. How-

ever, in wide voltage range applications the operating frequency is usually far from the resonance frequency which makes the FHA inaccurate. To solve this issue, authors in [97, 98] utilize numerical non-linear programming techniques to design the SRC for high efficiency operation. Studies in [91, 99] propose a variable dc bus voltage, which is regulated by the grid-tied inverter, to reduce the gain requirements for the SRC and thus, reduce the frequency range. Other researchers [76, 100] proposed fixed switching frequency operation in conjunction to PWM or PSM, in order to maintain soft-switching operation for larger operating ranges at the expense of increased circulating currents.

Regarding the DAB, in wide voltage range applications, the voltage unmatch between low voltage side and high voltage side causes that the isosceles trapezoid current waveform becomes a scalene trapezoid waveform. Consequently, the current at the turn-off event and the rms current increase. Which leads to higher switching losses and conduction losses. Targeting towards turn-off current reduction and ZVS extension, advanced modulation strategies were studied and adopted in the DAB. For instance, double or triple PSM, variable frequency modulation and PWM control [63, 64, 66–68, 101]. Various techniques to reduce the conduction losses at the low voltage side have also been proposed. The well-know method is to parallel semiconductor devices or converter modules [69–72]. However, parallel switching devices increases parasitic inductances and creates temperature imbalances among paralleled switches, complicating the circuit layout. In addition, thick copper or parallel structure must be applied to transformer windings resulting in high manufacturing cost and high interwinding capacitance. Furthermore, paralleling converter modules need additional efforts to eliminate circulating currents between units. Besides the current sharing at the low voltage side, methodologies to reduce the voltage stress at the high voltage side have also been proposed, such as the series connection of semiconductors and switching bridges [73, 74, 102].

Table 2.2: Review of bidirectional dc-dc converters for ESSs.

Study	Year	Topology	Switches	Power	Sw. frequency	V_1	V_2	Efficiency 1	Efficiency 2	Power density
[103]	2012	DAB	Si	6 kW	40 kHz	288 V	24 V - 48 V	96.4 % @ 36 V	94.5 % @ 24 V	Not given
[104]	2012	DAB	IGBT	6 kW	20 kHz	355 V	50 V - 59 V	96.9 % @ 59 V	93 % @ 55 V	Not given
[105]	2017	DAB	GaN	1 kW	100 kHz	400 V	11 V - 13 V	98.3 % @ 12 V	Not given	1.83 W cm^{-3}
[106]	2017	DAB	SiC	5 kW	48 kHz	750 V	100 V - 700 V	98.5 % @ 600 V	92.5 % @ 100 V	1.8 W cm^{-3}
[107]	2017	SRC	Si	3.3 kW	150 kHz - 350 kHz	400 V	180 V - 430 V	98.1 % @ 320 V	95.6 % @ 180 V	Not given
[107]	2017	SRC	GaN	3.3 kW	150 kHz - 350 kHz	400 V	180 V - 430 V	97.4 % @ 320 V	94.8 % @ 180 V	Not given
[108]	2017	SRC	Si + SiC	300 W	110 kHz - 1 kHz	380 V	28 V - 32 V	97.6 % @ 30 V	96.7 % @ 32 V	Not given
[109]	2018	SRC	Si + SiC	5 kW	40 kHz - 160 kHz	400 V	42 V - 58 V	97.1 % @ 50 V	95 % @ 42 V	1.09 W cm^{-3}
[110]	2017	Boost Half-B.	Si	1 kW	100 kHz	400 V	30 V - 60 V	91 % @ 30 V	89 % @ 60 V	Not given
[111]	2013	Boost Full-B.	Si + SiC	6 kW	40 kHz	800 V	30 V - 80 V	97.8 % @ 80 V	96 % @ 30 V	Not given

3

Series Resonant Converter Dc Transformer

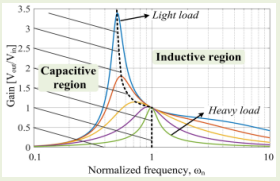
In this chapter, the work presented in Appendices B, C, D and E is summarized. The main objectives of this study are to analyse the design considerations and efficiency optimization of the Series-Resonant Converter (SRC) dc transformer, i.e. open-loop operation with unity gain at the resonance frequency. Accordingly, the chapter is organized as shown in Fig.3.1. First, an overview of the system is presented. Then, the fundamentals of typical dc gain characteristics and steady-state waveforms of the SRC are given. This explanation will serve as a baseline for the design considerations subsequently explained. The design considerations for open-loop operation consist of (1) minimum circulating current to achieve ZVS, (2) operation within the inductive region of the resonant tank under all operating conditions, (3) limit the resonant tank gain to fulfil the load regulation requirements and (4) tuning the distributed resonant tanks at the same resonance frequency. Afterwards, the SRC efficiency is analyzed and optimizations methods are proposed. To do so, firstly the components' losses are detailed. Then, the impact of the switching frequency and dead-time to the losses is analyzed. The losses reduction at the different components of the SRC achievable with the utilizations of GaN devices is also investigated. Finally, a design methodology in accordance with the design considerations and the efficiency optimization is proposed. A summary of the developed prototypes is presented at the end.

3.1 System description

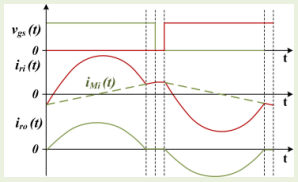
The SRC is intended to operate as a dc SST which main functionalities are to (I) provide isolation between the converter ports , (II) set the voltage of the unregulated dc buses and (III) support soft-switching in order to reduce the system losses. The SRC has inherent load regulation characteristics when switching at the vicinity of the resonance frequency, which means that the voltage gain between ports remain constant from no load to 100 % load. Due to the load regulation characteristics, the SRC has an intrinsic voltage balancing tendency among ports and thus, it can be interpreted as a gain module between the different dc buses. Therefore, only one of the ports has to be line regulated, while the other dc buses are effectively clamped by the transformer turns ratio and the resonant tank gain. Consequently, it is feasible to operate the SRC in open-loop at a fixed switching frequency and duty cycle.

3.1) System description

3.2) Operating principle

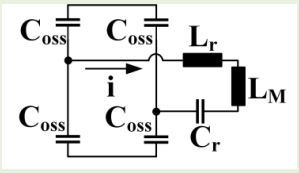


Dc gain

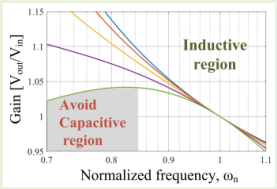


Steady-state

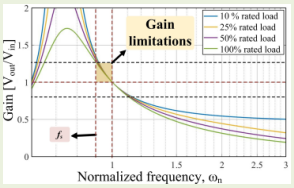
3.3) Design considerations for open-loop operation



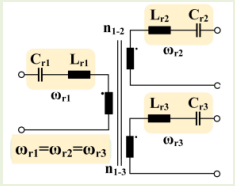
Zero-Voltage Switching



Inductive region operation

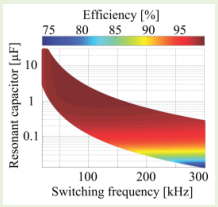


Load regulation requirements

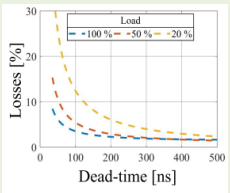


Resonance frequency matching

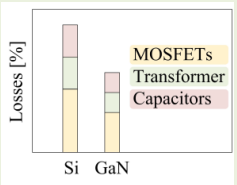
3.4) Design optimization for high efficiency operation



Switching frequency selection



Dead-time contribution to loss

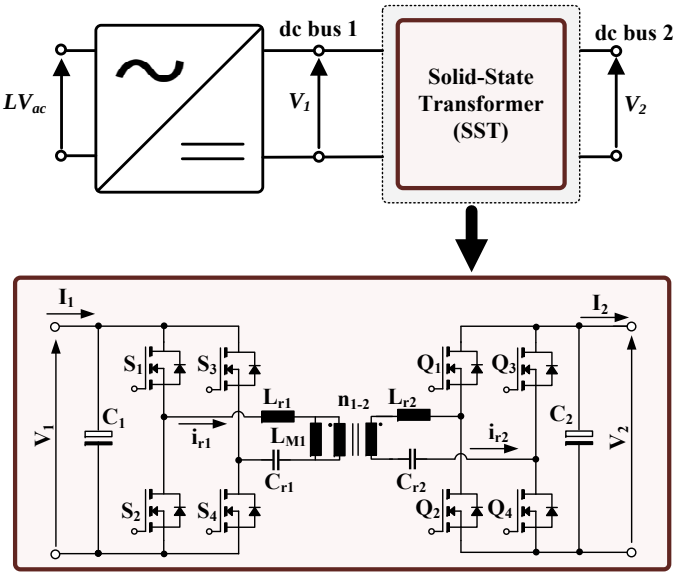


Performance improvements with GaN

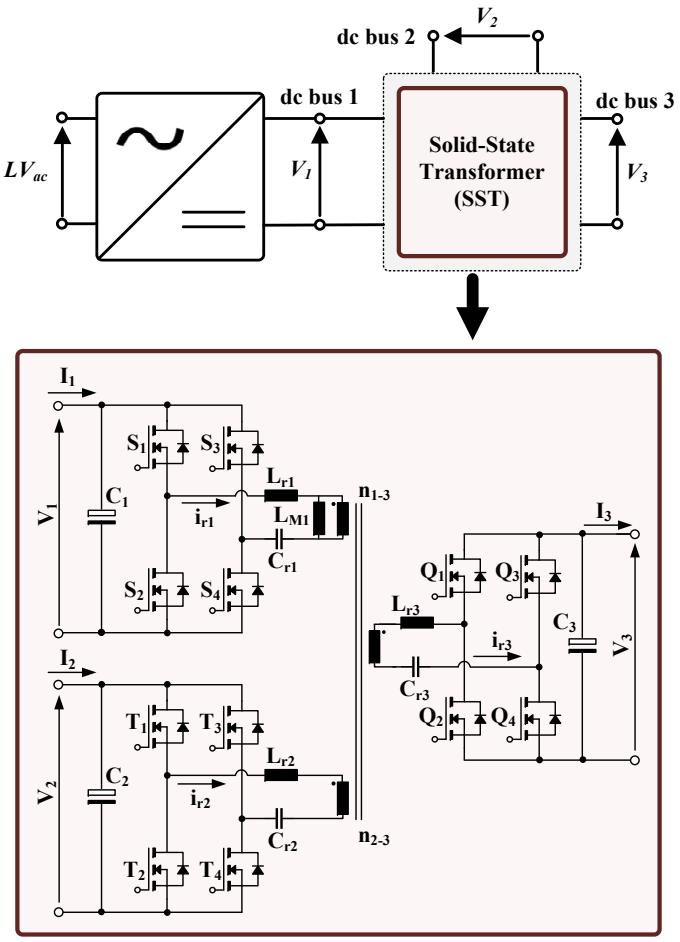
3.5) Prototyping process

- Design flowchart
- Prototypes summary

Figure 3.1: Structure of Chapter 3.



(a) Two port series resonant converter (2P-SRC).



(b) Three port series resonant converter (3P-SRC).

Figure 3.2: Series Resonant Converter for dc SST applications.

Figures 3.2a and 3.2b show a two-port SRC (2P-SRC) and three-port SRC (3P-SRC) connected to the ac grid through the dc bus V_1 and an inverter. The SRC ports are interconnected by a high frequency transformer. Each port consists of a full-bridge with four power devices and a dc capacitor. Because of the lack of active regulation, a certain gain symmetry is required regardless the power flow direction. Therefore, a distributed resonant tank among the converter ports is used. The resonant tank is constituted by the resonant inductors L_r and the resonant capacitors C_r. The resonant inductors are formed by the leakage inductance of the transformer, the parasitic inductances and, if required, by external inductors.

3.2 Operating principle of the SRC dc transformer

3.2.1 SRC operating regions

Typical dc gain characteristics of the SRC and its operating regions are illustrated in Fig.3.3 in terms of the normalized frequency ω_n. The normalized frequency is defined by (3.1). The operating regions are divided in inductive impedance and capacitive impedance. The boundaries between the regions are determined by the peak of the gain curve at any load condition. The impedance of the resonant tank can also be identified from the slope of the dc gain curves, wherein a negative gain slope results in an inductive impedance. Operation with an inductive impedance is desired, since the current flowing through the input bridges is lagging the voltage, which causes ZVS of the input side MOSFETs.

$$\omega_n = \frac{2\pi f_s}{\omega_r} \tag{3.1}$$

where f_s refers to the switching frequency in Hz and ω_r refers to the resonance frequency in rad/s.

At the resonance frequency, i.e. $\omega_n = 1$, the dc gain curves of the resonant tank converge at the unity gain, which means that the input-to-output voltage gain remains constant regardless the output power. This demonstrates the inherited load regulation characteristics of the SRC.

The circuit configurations in Fig.3.2, contain a resonant tank distributed among the different ports. The benefit of utilizing a distributed resonant tanks is that the impedance behaviour has a certain symmetry regardless the power flow direction. In the conventional SRC with a single resonant tank, the impedance differs with the power flow direction and thus, the dc gain is not symmetrical [112].

When operating at the inductive region of the SRC, ZVS can be achieved. Moreover, depending on the oeprating point, different soft-switching conditions can be achieved as well. Figure 3.4 shows the resonant tank currents when operating within the inductive region above, below and at the resonance frequency. It can be observed that the best conditions occur at the resonance frequency due to the (1) ZVS and low turn-off current at input ports, (2) ZCS at output ports and (3) lower rms currents [77].

According to the previous discussion, the optimal switching frequency is at $\omega_n = 1$. However, due to factors such as parasitic components, tolerances in the resonant components and temperature variations, the resonance frequency can be subject to varia-

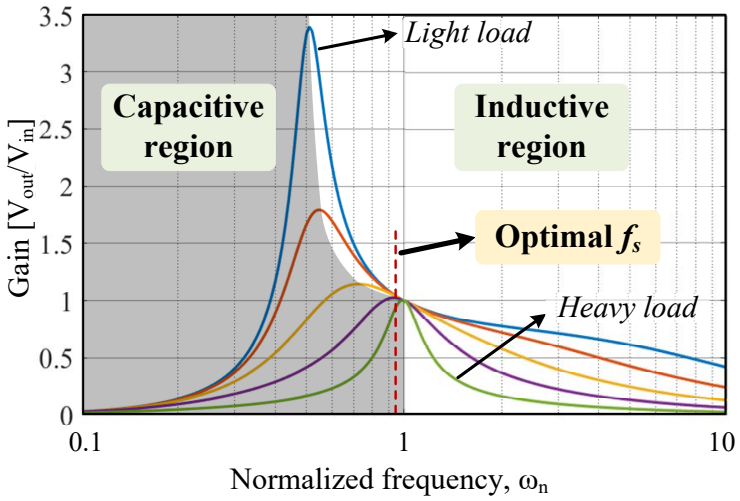


Figure 3.3: Dc gain curves of a resonant tank versus normalized frequency ω_n.

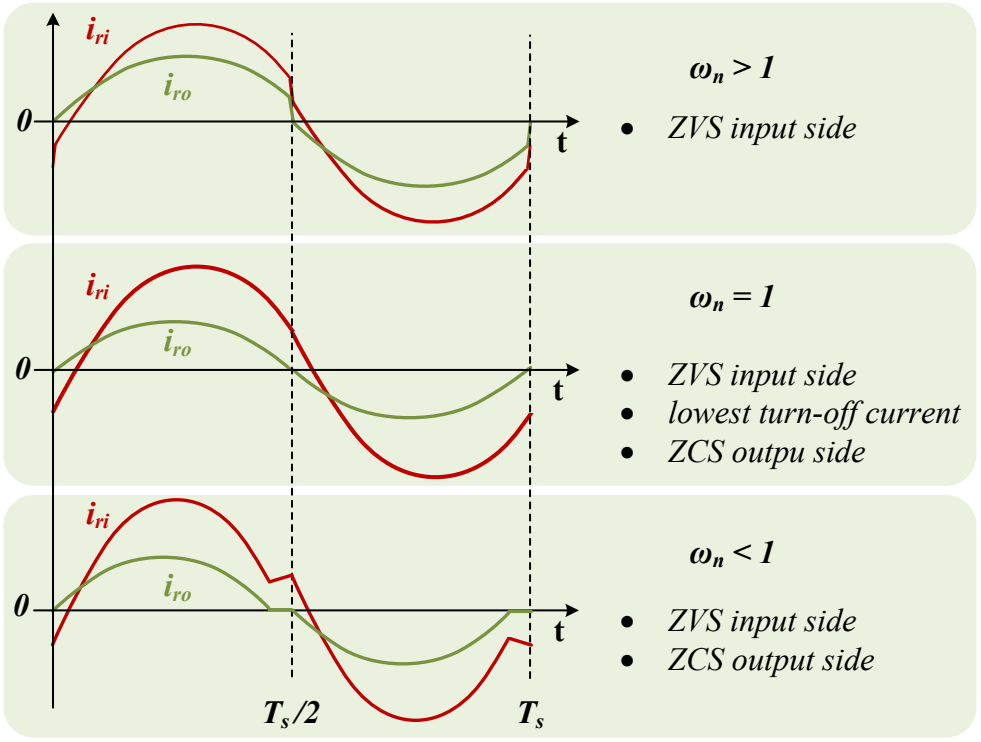


Figure 3.4: Typical resonant current waveforms at the input side bridge i_{ri} and output side bridge i_{ro} when operating within the inductive region above the resonance frequency $\omega_n > 1$, at the resonance frequency $\omega_n = 1$ and below the resonance frequency $\omega_n < 1$.

tions. Therefore, according to Fig.3.4 the selected switching frequency is located below but close to the resonance frequency. The design choice is selected at $\omega_n = 0.96$, which has been obtained empirically through experimental tests.

3.2.2 Steady-state operation

The steady-state waveforms of the SRC with $\omega_n < 1$ are shown in Fig.3.5. A detailed time-domain analysis of the SRC can be found in App.D. Note that the main converter waveforms do not differ with the number of ports or the operation mode. Therefore, as an illustrative example, the following explanation is given for 2P-SRC from Fig.3.2a. Half-switching period is divided in three sub-intervals:

- Stage 1 $[t_0 < t < t_1]$:
  Pair of switches at the input side are driven high and the resonant tank is excited with a positive voltage. The resonance begins and power is transferred to the rectifying stage. The voltage across the magnetizing inductance is clamped to the input voltage and thus, the current increases linearly [1].
- Stage 2 $[t_1 < t < t_2]$:
  Half the resonance period ends. The resonant current at the input side equals the magnetizing current. There is no power transferred to the output ports and thus, the resonant current at the output side become zero. The magnetizing inductance is still clamped by the input voltage, so the magnetizing currents keeps increasing.
- Stage 3 $[t_2 < t < t_3]$:
  The pair of switches at the input side turn-off and the dead-time interval begins. The semiconductors' output capacitances at the input side bridge are charged/discharged with the magnetizing current.

The resonant current at the input port $i_{ri}(t)$ is given by the sum of the resonant currents at the output ports $i_{ro}(t)$ and the magnetizing current $i_{Mi}(t)$ as shown in (3.2). The peak magnetizing current I_{Mi}, and the input and output rms currents $I_{ri,rms}$, $I_{ro,rms}$ derived in App.D are given by (3.3) - (3.5).

$$i_{ri}(t) = i_{Mi}(t) + n_{i-o} i_{ro}(t) \tag{3.2}$$

$$I_{Mi} = \frac{1}{4} \frac{n_{i-o} V_o (T_s - 2t_d)}{L_{Mi}} \tag{3.3}$$

$$I_{ri,rms} = n_{i-o}^2 V_o \frac{\sqrt{2}}{8} \sqrt{\frac{(T_s - 2t_d)^2 (T_s + 2t_d)}{T_s L_{Mi}^2} + \frac{T_s 4\pi^2 P_i^2}{(T_s - 2t_d) n_{i-o}^4 V_o^4}} \tag{3.4}$$

$$I_{ro,rms} = \frac{\sqrt{2}}{4} V_o \sqrt{\frac{n_{i-o}^4}{L_{Mi}^2} \frac{(T_s - 2t_d)^3}{T_s} \frac{5\pi^2 - 48}{12\pi^2} + \pi^2 \frac{T_s}{T_s - 2t_d} \frac{P_o^2}{V_o^4}} \tag{3.5}$$

[1] The voltage across the magnetizing inductance has an ac component at the resonance frequency due to the ac voltage across the output capacitors. Therefore, the current increase quasi-linearly. For the proposed design methodology the ac voltage across the capacitors is relatively low and thus, it can be neglected to simplify the analysis. More information can be found in App.D.

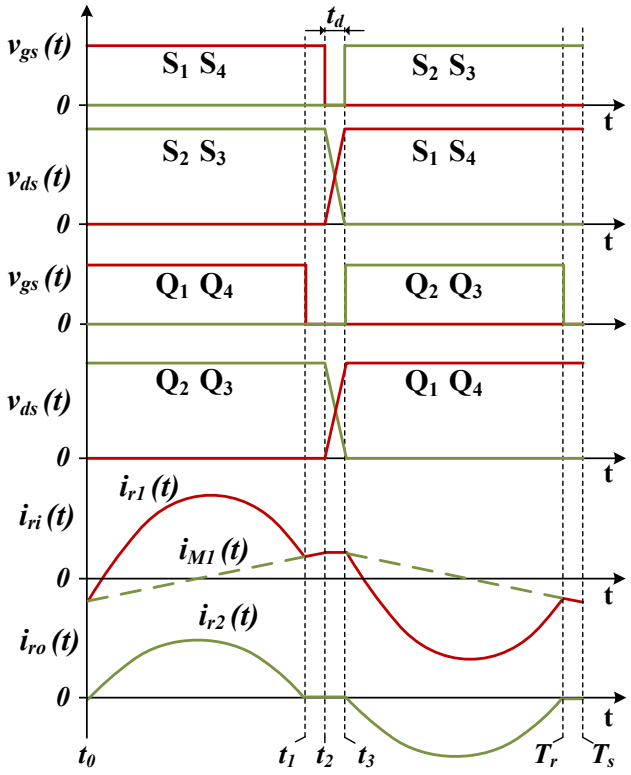


Figure 3.5: Steady-state waveforms of the SRC when operating slightly below the resonance frequency.

where P_i and P_o refer to the power transferred by input and output ports respectively, T_s is the switching period, t_d the dead-time, L_{Mi} the magnetizing inductance referred to the input port, V_o the dc voltage at the output port and n_{i-o} the transformer turns ratio from input to output port.

Synchronous rectification can be used to reduce the conduction losses of the semiconductors at the output side. Because of the fixed switching frequency operation, the duty cycle at the output ports can be pre-set according to the resonance frequency, so no feedback loop is required. As shown in Fig.3.5, the output side switches are turned-on at t_0, at the same time that the input side switches. The turn-off event occurs at t_1, when half resonance period ends and the resonant current at the output side becomes zero.

3.3 Design considerations of the SRC dc transformer

3.3.1 Zero-Voltage Switching

To fulfil ZVS requirements, the magnetizing current I_{Mi} has to be large enough at the beginning of the dead-time interval to charge and discharge the MOSFETs' output capacitances C_{oss}. From (3.3) it can be observed that, differently from the resonant currents, I_{Mi} is not load-dependent. However, it depends on the dc voltage, which is

a design requirement, and the magnetizing inductance, switching frequency and dead-time, which are design choices. Because of the constant voltage and fixed switching frequency operation of the SRC, the design methodology to achieve ZVS is simplified. According to [113], the maximum magnetizing inductance to achieve soft-switching can be calculated by (3.6). Note that in bidirectional and multi-port topologies the maximum magnetizing inductance has to be calculated for the worst case scenario as carried out in App.E.

$$L_{M,max} = \frac{\pi t_d}{4 C_{oss} \omega_r} \tag{3.6}$$

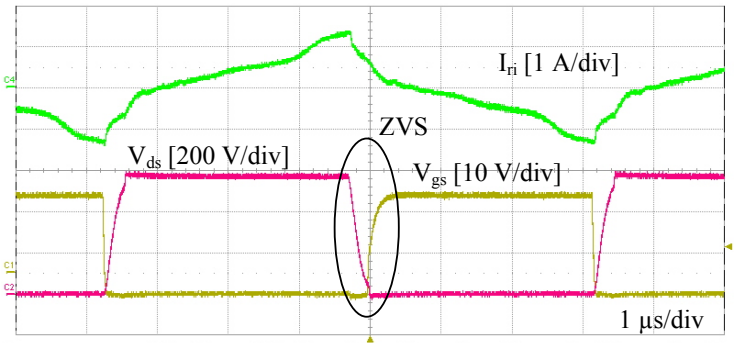
Fig.3.6 shows ZVS operation under different loads obtained from a laboratory prototype of a 3P-SRC rated at 1 kW. More detailed specifications and experimental results can be found in App.E. Results depicted in Fig.3.6 verify that ZVS is achieved with a fixed t_d from light load to 100 % load and thus, ZVS operation is not load dependent.

3.3.2 Inductive operation

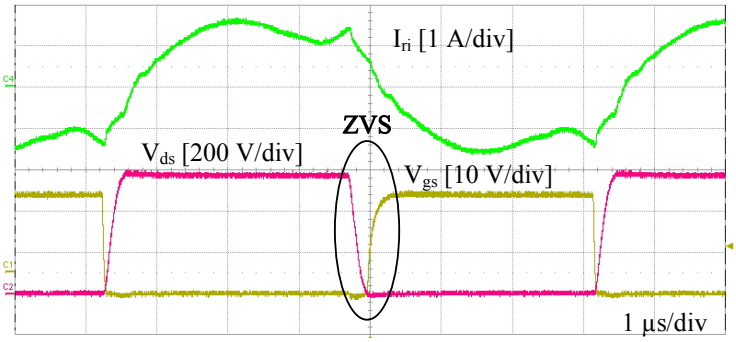
By analysing the dc gain characteristics of the SRC illustrated in Fig.3.3, it can be observed that the output power influences the dc gain behaviour. When the power increases, the dc gain slope below the resonance frequency decreases and the peak gain moves towards the resonance frequency. If the output power further increases, the resonant tank can become underdamped, so the slope of the gain at the switching frequency would become positive. Consequently, the resonant tank would operate within the capacitive region. Therefore, for a given resonance frequency and maximum power rating, the resonant tank parameters have to be selected in order to ensure operation within the inductive region under any operating condition.

In Appendices B and D, the dc transfer functions for the 2P-SRC and 3P-SRC have been derived from the respective ac equivalent circuits[2]. As can be observed, the dc transfer functions of the resonant tanks do not give an intuitive sense to choose the resonant tank parameters. Some authors [76, 96] use the derivative of the dc gain at the switching frequency to calculate the gain slope and find the boundaries between capacitive and inductive region. However, this methodology is a complex algebraic process when utilizing distributed resonant tanks. Authors in [94], using a graphical tool with bode plots, derived a criterion to select the resonant tank parameters of the conventional SRC with a single resonant tank. In App. D, this criterion has been extended for multi-port SRC with distributed resonant tanks. If the resonant tank is designed symmetrically, which means that the ratio of magnetizing inductance to resonant inductance m is equal in all ports, the criterion in (3.7) can be used. In (3.7), m_{min} refers to the minimum inductance ratio that allows operation within the inductive region at maximum output power. For designs with asymmetrical resonant tanks, the criterion in (3.9) can be applied and verified at each side of the transformer independently. Asymmetrical resonant tanks are utilized when the stray inductances are the only inductive resonant component as in App.E.

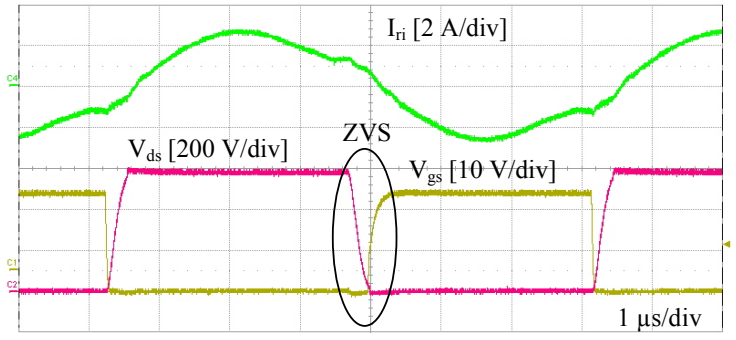
[2] App.B dc transfer functions for the 2P-SRC equations (12)-(19) and App.D dc transfer functions for the 3P-SRC equations (22)-(29) .



(a) 10 % load.



(b) 60 % load.



(c) 100 % load.

Figure 3.6: Experimental results of ZVS operation for different output power.

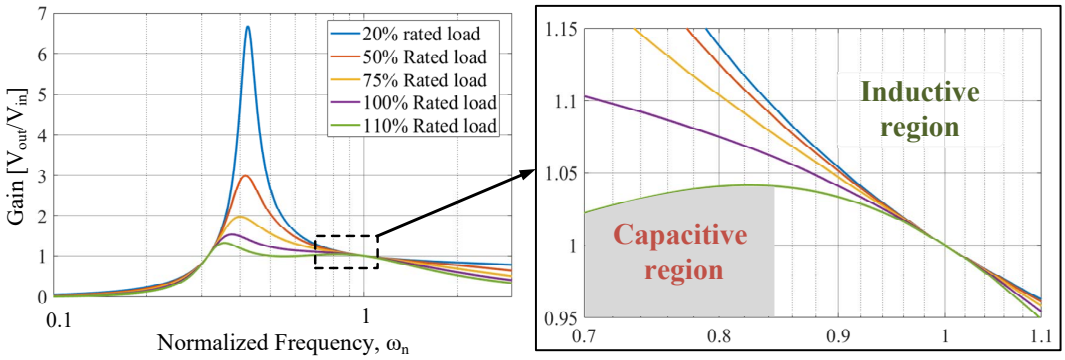


Figure 3.7: Dc gain characteristics of an arbitrary resonant tank when $m = m_{min}$.

$$m_{min} = \frac{p}{p-1}\left(\frac{\omega_r L_{Mi}}{R_{ACi,min}}\right)^2 \quad \text{if } m = \frac{L_{M1}}{L_{r1}} = \frac{L_{M2}}{L_{r2}} = ... = \frac{L_{Mp}}{L_{rp}} \tag{3.7}$$

$$m_{min} = \frac{L_{Mi}}{L_{ri,max}} \tag{3.8}$$

where p refers to the number of ports, i to the reference port number, $R_{ACi,min}$ the minimum equivalent ac load seen from port i (3.10) and $L_{ri,max}$ the maximum resonant inductance seen from port i.

$$L_{ri,eq,max} = \frac{R^2_{ACi,min}}{\omega_r^2 L_{Mi}} \quad \text{if } m \neq \frac{L_{M1}}{L_{r1}} \neq \frac{L_{M2}}{L_{r2}} \neq ... \neq \frac{L_{Mp}}{L_{rp}} \tag{3.9}$$

where $L_{ri,eq,max}$ refers to the maximum overall equivalent stray inductance seen from port i.

$$R_{ACi,min} = \frac{8V_i^2}{\pi^2 P_{max}} \tag{3.10}$$

where P_{max} refers to the maximum output power and V_i refers to the dc bus voltage at port i.

Fig.3.7 shows the dc gain characteristics for an arbitrary deign of a 3P-SRC with an inductance ratio of $m = m_{min}$. The dc gain curves have been plotted using the dc gain transfer functions from App.D. It can be observed that slope of the gain shifts from negative to positive when the load rises above the maximum load. Therefore, with the conditions given in (3.7) or (3.9), the boundaries between capacitive and inductive region can be well approximated.

In App.E the impact of the dead-time and resonance frequency to the resonant components are analyzed. For given converter specifications and semiconductors' C_{oss}, the resonant components are calculated for m_{min} in function of t_d and ω_r according to (3.6) and (3.7). Results are depicted in Fig.3.8. The y-axis shows the maximum inductance that allows operation within the inductive region and the x-axis the corresponding resonance capacitor. According to the results, increasing t_d and/or ω_r reduces the size of

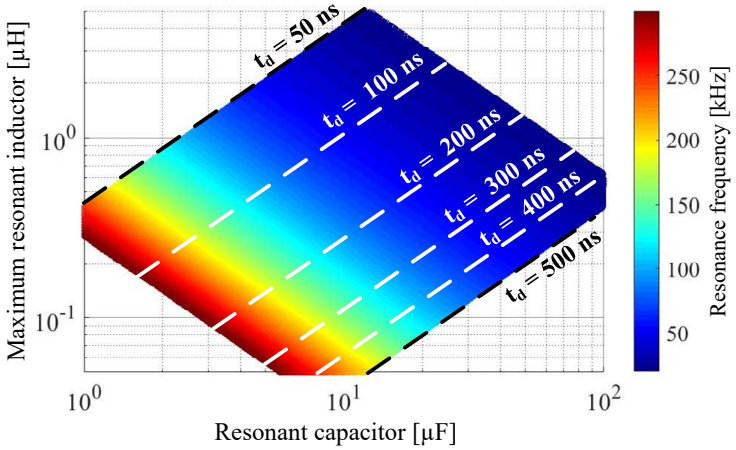


Figure 3.8: Resonant tank components size $L_{ri,max}$ and C_{ri} for $m = m_{min}$ versus t_d and ω_r.

the resonant tank components. However, large t_d and/or ω_r might cause the maximum resonance inductance to drop below the leakage inductance of the transformer and PCB parasitic inductances. Therefore, t_d and ω_r are limited by the series inductance between the input and output bridges of the resonant tank.

3.3.3 Inherited load regulation characteristics

In dc microgrids systems, the voltage at one of the ports can be actively regulated with the grid-connected inverter or in lack of grid connection, as in islanding operation mode, can be maintained with the ESS. At the same time, the dc SST accommodates the voltage of the other dc ports. Even though the active regulation, in practice, the dc buses voltage might have variations due to power fluctuations between the different units of the microgrid system. For instance, in a three-port dc SST, the voltage variation at each dc bus can be defined as ΔV_1, ΔV_2 and ΔV_3, and the nominal voltages as $V_{1,nom}$, $V_{2,nom}$ and $V_{3,nom}$. Then, the voltage limits of the dc buses are given by (3.11)-(3.13) as illustrated with Fig.3.9.

$$V_1 \in V_{1,nom} \pm \Delta V_1 \tag{3.11}$$

$$V_2 \in V_{2,nom} \pm \Delta V_2 \tag{3.12}$$

$$V_3 \in V_{3,nom} \pm \Delta V_3 \tag{3.13}$$

Accordingly, the SRC dc transformer has to guarantee that the unregulated dc buses do not exceed these voltage limitations. Therefore, the converter has to be designed to meet the gain requirements according to the specifications as illustrated with Fig.3.10. Since the switching frequency is selected below the resonance frequency, the minimum gain requirement will be always fulfilled. The maximum gain limits can be calculated by (3.14).

$$H_{i-o,max} = \frac{V_o}{V_i} = \frac{1}{n_{i-o}} \frac{V_o + \Delta V_o}{V_i - \Delta V_i} \tag{3.14}$$

where i refers to the input port and o refers to the output port.

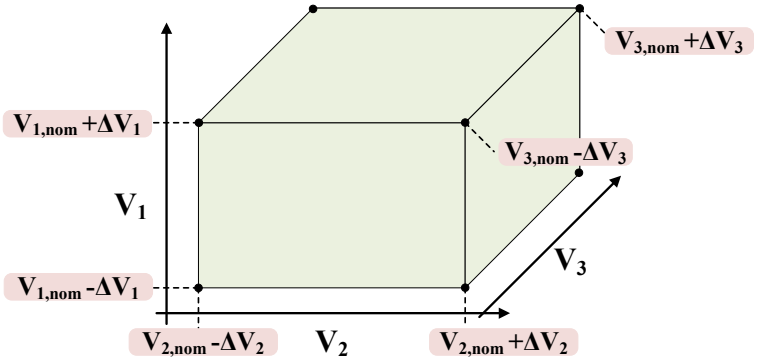


Figure 3.9: Voltage limits of a microgrid with three dc buses.

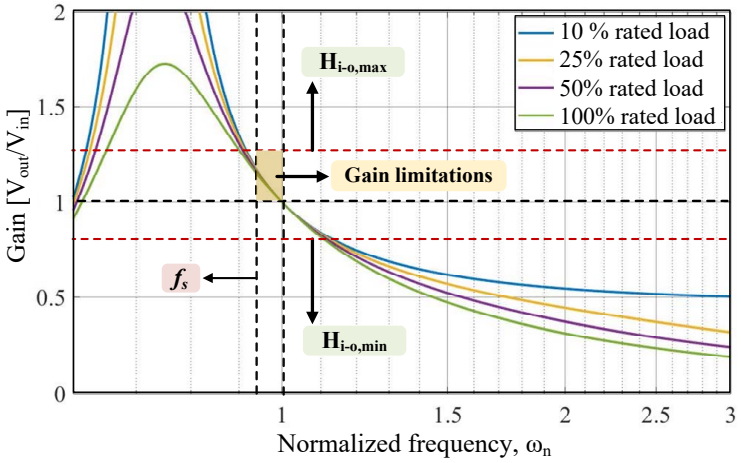


Figure 3.10: Gain limitations of the SRC. The figure illustrates the SRC dc gain in terms of ω_n for different loads. The converter switching frequency is marked with f_s. The gain limitations according to the design specifications are $H_{i-o,min}$, $H_{i-o,max}$, $H_{o-i,min}$ and $H_{o-i,max}$, where i and o refers to the port number.

The largest voltage gain is found at no load conditions. Hence, to fulfil the dc gain limitations, the criterion given by (3.15) must be accomplished. The resonant tank design can then be verified with the dc gain transfer functions of the SRC [3].

$$H_{i-o,max} \geq H_{i-o}(R_{ac,max}) \tag{3.15}$$

As explained in App.D, the inductance ratio m can be used to adjust the slope of the dc gain. Larger inductance ratios lead to flatter dc gain characteristics, while lower inductance ratios lead to steeper dc gain slopes. Fig.3.11 shows the dc gain characteristics in terms of m for different ω_n. It can be observed that larger m is preferred to improve the inherited load regulation characteristics of the SRC and hence, fulfil the gain limitations. As studied in App.D, the selection of the inductance ratio m is also subject to a trade-off between the resonant capacitor size and the voltage stress at the resonance capacitors.

Highest m is achieved when the resonant inductance is solely formed by the stray

[3]The dc gain transfer functions for the 2P-SRC can be found in App.B (equations (12)-(19)), and for the 3P-SRC in App.D (equations (22)-(29)).

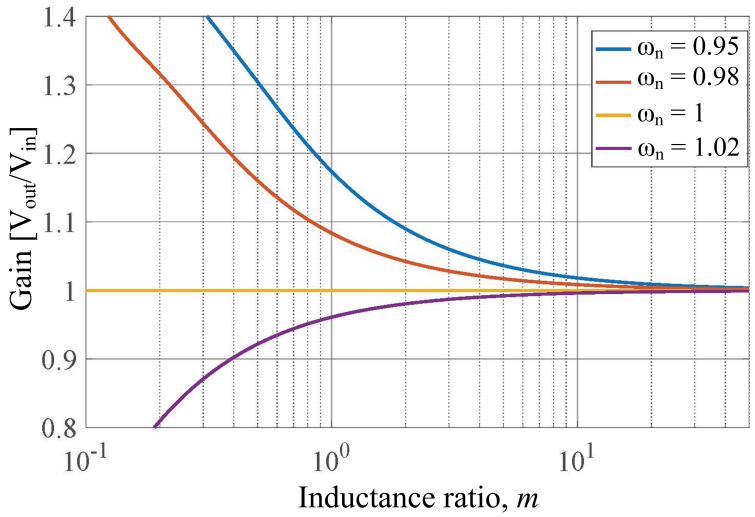


Figure 3.11: Dc gain characteristics vs inductance ratio m for different ω_n.

inductances of the converter. Avoiding the utilization of external resonant inductors is also beneficial in terms of power density and efficiency. On the other hand, the distributed resonant tank becomes more asymmetrical, so the criterion in (3.15) should be verified under all operating modes. When using a symmetrical resonant tank, gain symmetry among ports is achieved and therefore $H_{12} = H_{21}$, which simplifies the design procedure.

In App.D, a 3P-SRC was implemented and tested with two different resonant tanks with $m = 20$ and $m = 80$. Experimental tests were carried out by measuring the voltage across each port with a constant voltage across V_3 while sweeping the output power from no load to full load. Note that the power supplies were used in constant current mode during the experimental tests. Figures 3.13 show the voltage gain obtained in dual-output, dual-input and single-input single output operation modes for each resonant tank.

Figure 3.14 shows the load regulation characteristics under operating modes transitions and power fluctuations from the 3P-SRC experimental prototype in C. It can be observed that the unregulated dc ports V_1 and V_2 remain constant when power transitions occur.

3.3.4 Resonance frequency matching

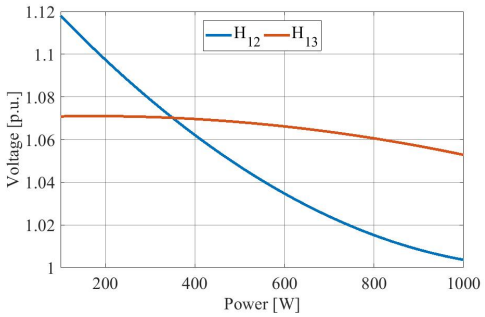
The experimental process to tune the resonance frequency of the distributed resonant tank is explained below.

Firstly, the theoretical values of the resonant capacitors at each port are calculated with (3.16) to resonate the same frequency.

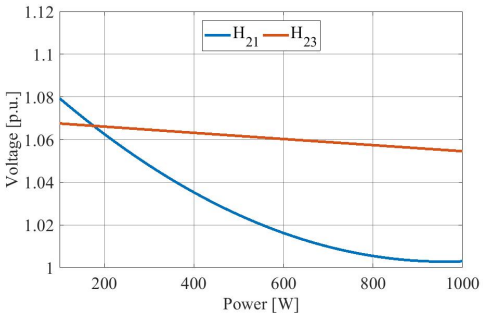
$$C_{ri} = \frac{1}{\omega_r^2 L_{ri}} \tag{3.16}$$

where $i = 1, 2, 3$

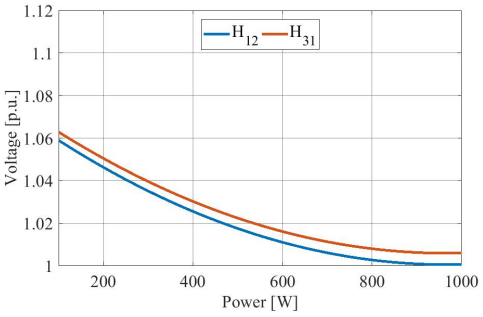
Once the resonant capacitors are mounted on the PCB, the resonance frequency is re-



(a) Dual-Output.

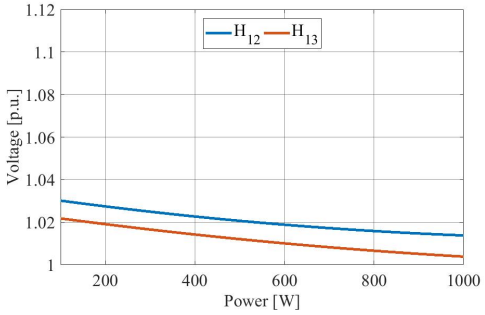


(b) Single-input single-output.

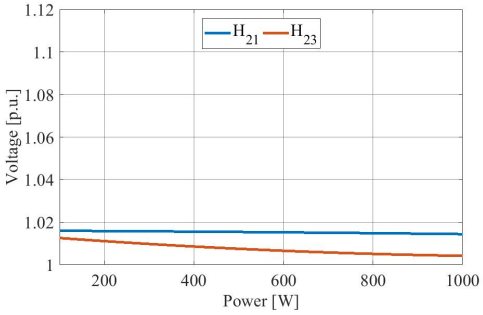


(c) Dual-input.

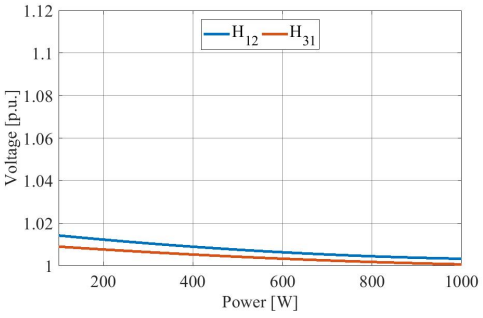
Figure 3.12: Experimental results of the steady-state dc gain of a 3P-SRC for a resonant tank with $m = 20$.



(a) $m = 80$ Dual-Output.

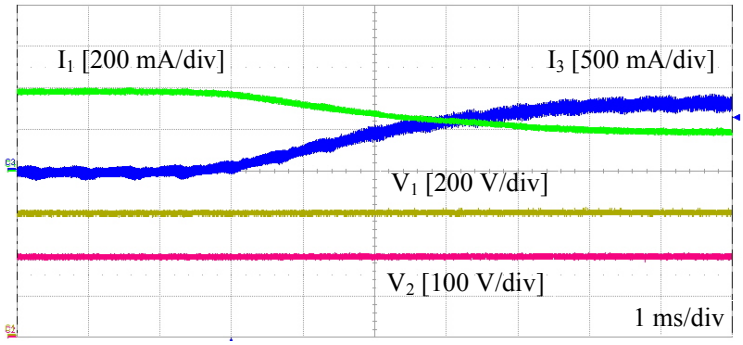


(b) $m = 80$ Single-input single-output.

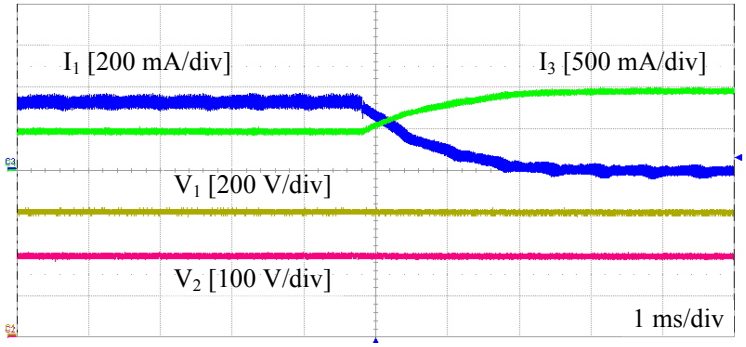


(c) $m = 80$ Dual-input.

Figure 3.13: Experimental results of the steady-state dc gain of a 3P-SRC for a resonant tank with $m = 80$.



(a) Transition from single-input single-output to dual input.



(b) Transition from dual input to single-input single-output.

Figure 3.14: Voltage regulation with power fluctuations of the 3P-SRC. Port 3(V_3) is regulated at 400 V, while ports 1 (V_1) and 2 (V_2) are the unregulated ports. Inputs: Port 1 and 2; Output: Port 3.

tuned to compensate for the parasitic inductances. As shown in Fig.3.15a, the gain across a resonant capacitor is measured while short-circuiting the resonant capacitors at the other ports. Then, an equivalent resonance frequency $f_{r,eq1}$ is found from the bode plot as shown in Fig.3.15c. In that way, f_{req1} is only due to the resonant capacitor C_{r1} and the overall resonance inductance $L_{r1,eq}$, as shown in Fig.3.15b. $L_{r1,eq}$ is then calculated by (3.17). The measurement is repeated for the other two ports to calculate the $L_{r2,eq}$ and $L_{r3,eq}$. Then, the resonance inductances L_{r1}, L_{r2} and L_{r3} can be calculated by solving the system given in (3.18). Finally, the resonant capacitors are recalculated to match the desired resonance frequency using (3.16).

$$\begin{cases} L_{r1,eq} = \frac{1}{(2\pi f_{r,eq1})^2 C_{r1}} \\ L_{r2,eq} = \frac{1}{(2\pi f_{r,eq2})^2 C_{r2}} \\ L_{r3,eq} = \frac{1}{(2\pi f_{r,eq3})^2 C_{r3}} \end{cases} \tag{3.17}$$

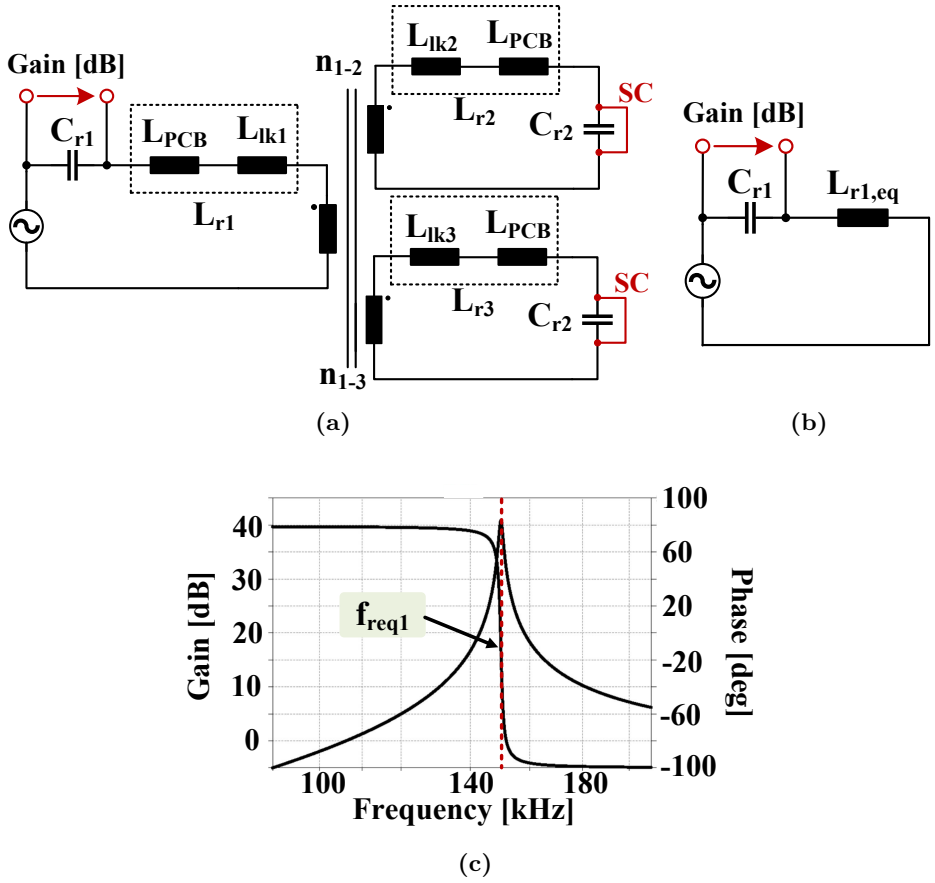


Figure 3.15: Resonance frequency matching methodology. (a) Measurement set-up for Port-1: the gain after the resonant capacitor is measured with a Bode analyser. (b) Equivalent circuit of the measurement set-up, where $L_{r1,eq}$ is the overall resonant inductance seen from Port-1. (c) Measured bode plot and equivalent resonance frequency due to C_{r1} and $L_{r,eq1}$.

$$\begin{cases} L_{r1,eq} = L_{r1} + \left(\frac{1}{n_{12}^2 L_{r2}} + \frac{1}{n_{13}^2 L_{r3}}\right)^{-1} \\ L_{r2,eq} = L_{r2} + \left(\frac{n_{12}^2}{L_{r1}} + \frac{1}{n_{23}^2 L_{r3}}\right)^{-1} \\ L_{r3,eq} = L_{r3} + \left(\frac{n_{13}^2}{L_{r1}} + \frac{n_{23}^2}{L_{r2}}\right)^{-1} \end{cases} \tag{3.18}$$

In App.E the resonance frequency matching methodology has been presented and verified on a 3P-SRC experimental prototype. The presented 3P-SRC converter uses the parasitic inductances and the leakage inductance of the transformer as the only inductive resonant component. Fig.3.16 shows the voltage gain measured across one of the resonant capacitors with all the resonant tank components included. It can be observed that, before the compensation, multiple resonance frequencies appear due to the resonance frequency mismatching. Fig.3.17 shows the equivalent resonance frequencies measured at each side of the resonant tank with the methodology illustrated

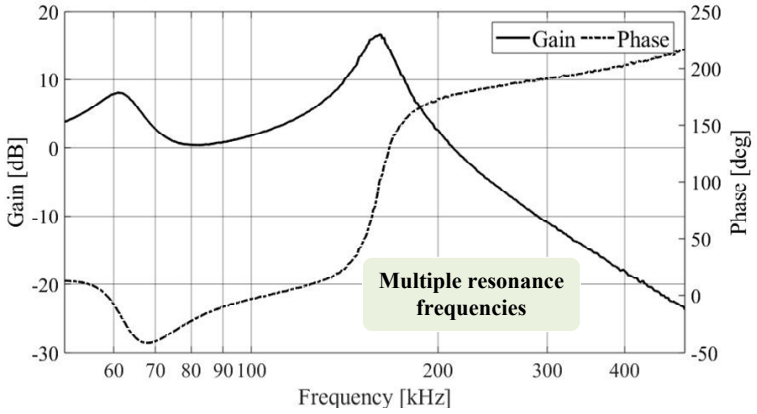
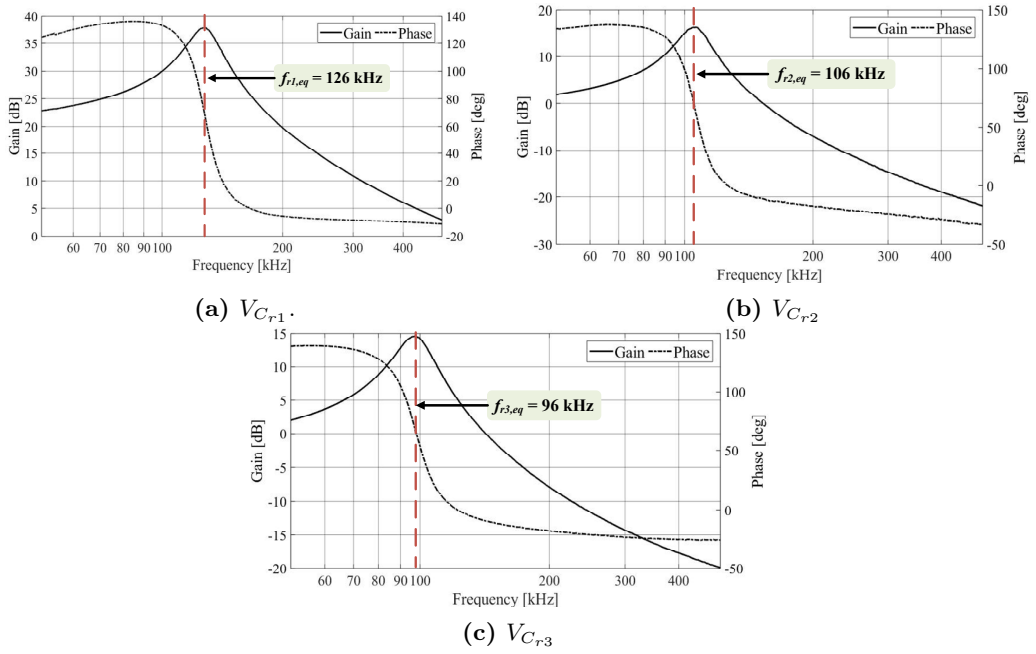


Figure 3.16: Voltage gain measurement before compensation with all the resonant tank components.



(a) V_{Cr1}. **(b)** V_{Cr2}

(c) V_{Cr3}

Figure 3.17: Voltage gain measurement and equivalent resonance frequency from each port.

in Fig.3.15, which evidences the mismatch in the resonance frequency. After performing the resonance frequency matching at 150 kHz, the voltage gain including all the resonant components was performed. Results are shown in Fig.3.18.

3.4 Design optimization for high efficiency operation

This section summarizes the approach used to the design and select the components of the SRC for high efficiency operation. The calculations and results presented throughout this section are based on the specifications given in Table 3.1.

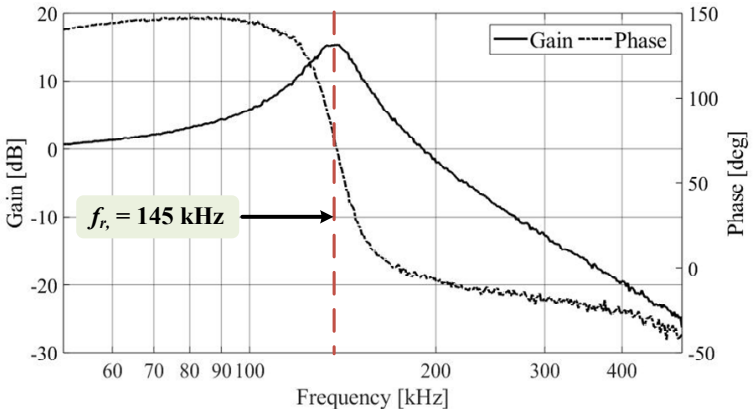


Figure 3.18: Voltage gain measurement and resonance frequency after compensation with all the resonant tank components.

Table 3.1: Specifications for the TP-SRC

Parameter	Value
Maximum power P_{max}	1.5 kW
Port-1 voltage V_1	80 V
Port-2 voltage V_2	400 V
Port-3 voltage V_3	600 V
Turns ratio n_{1-3}	1/7.5
Turns ratio n_{2-3}	1/1.5
Switc. frequency f_s	149 kHz

3.4.1 Dead-time contribution to losses

Resonant converters generally incur into high rms currents due to the sinusoidal shape of the resonant currents along with the circulating currents flowing through input ports. Therefore, while the switching losses are relatively low, resonant converters suffer from high conduction losses. As will be analysed below, the dead-time has a direct impact to the rms currents.

ZVS is achieved by selecting a magnetizing inductance L_{Mi} and dead-time t_d that provides enough circulating energy during the free-wheeling period to charge and discharge the MOSFETs' C_{oss} as given by (3.6). From (3.6) it can be observed that for the selected semiconductors, there are multiple combinations of L_{Mi} and t_d which can ensure ZVS.

The effect of the selected L_M-t_d combination to the rms currents and converter losses is analyzed for the specifications given in Table 3.1 and the Silicon based MOSFETs given in Table 3.2. The energy related C_{oss} is extracted from the manufacturer's datasheet and is used to calculate $L_{M,max}$ from (3.6) for 35 ns $\leq t_d \leq$ 500 ns. Then, the rms currents are calculated by (3.4) and transferred to the per-unit system with the input dc current as the base value. Fig.3.19 depicts the results obtained for 100 %, 50 % and 20 % load. It can be observed that small t_d implies smaller L_{Mi}, which results in larger magnetizing current and hence larger rms currents. At the same time, larger t_d causes

Table 3.2: Specifications of the Silicon devices used in the analysis.

Port	Switches	Reference	V, $R_{ds,on}$
Port-1	$S_1 - S_4$	AUIRFS4410	100 V 9.5 mΩ
Port-2	$T_1 - T_4$	IPW65R070C6	650 V 63 mΩ
Port-3	$Q_1 - Q_4$	IPW65R150CFDA	650 V 130 mΩ

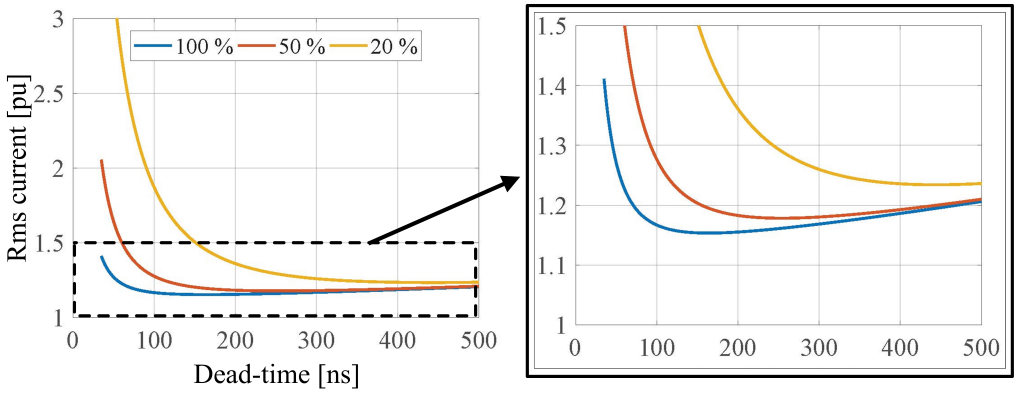


Figure 3.19: Theoretical per-unit rms currents versus dead-time under different load conditions, where the rms current base value is the dc port current I.

a reduction of the effective duty cycle, and thus larger rms currents are required to transfer the same power from input side to output side.

According to the design methodology presented in section 3.3, the converter operates under ZVS for the entire power range. Therefore, the input side turn-on losses can be neglected. However, at the turn-off event, the current hardly commutates with a current equal to the peak magnetizing current I_{Mi}. Then, turn-off losses P_{off} of a full bridge can be calculated with (3.19) as [114]. The conduction losses for the input side switches $P_{cond,in}$ are calculated with (3.20). When using synchronous rectification, conduction losses at the output side bridges $P_{cond,out}$ can be similarly calculated as given by (3.21).

$$P_{off} = 2V_i I_{Mi} t_{off} f_s \tag{3.19}$$

$$P_{cond,in} = 2R_{ds,on} I^2_{ri,rms} \tag{3.20}$$

$$P_{cond,out} = 2R_{ds,on} I^2_{ro,rms} \tag{3.21}$$

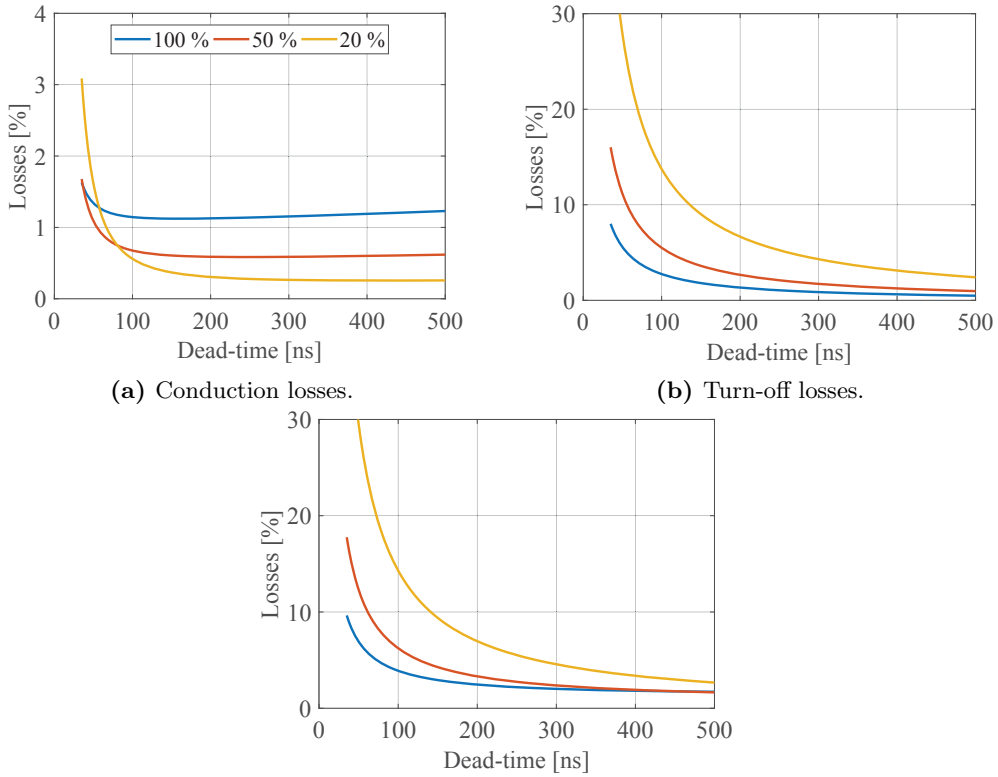
where

i: 1,2,3.

o: 1,2,3.

t_{off}: Semiconductors' turn-off time.

$R_{ds,on}$: Semiconductors' drain-source on resistance.



(a) Conduction losses.

(b) Turn-off losses.

(c) Total losses.

Figure 3.20: Semiconductors' losses proportional to the power output in percentage versus t_d for different output power.

I_{Mi}: Peak magnetizing current given by (3.3).

$I_{ri,rms}$: Input bridge rms current given by 3.4.

$I_{ro,rms}$: Output bridge rms current given by (3.5).

The conduction losses, turn-off losses and total MOSFETs' losses are shown in Fig.3.20. Results depict the proportional losses to the power output in percentage. As t_d increases, MOSFETs' losses decrease due to the the reduction of both the rms currents and peak magnetizing current. Solely considering the conduction losses, the optimal t_d would lay between 100 ns to 200 ns, because the rms current increase with large t_d has a negative impact on the conduction losses. On the other hand, turn-off losses of the Si MOSFETs predominate over the total losses. Therefore, for this example design, t_d should be selected above 400 ns to reduce the overall semiconductors' losses.

3.4.2 SRC performance improvements with GaN FETs

The improved figure of merits of GaN FETs, which implies a reduction of the on-resistance, input capacitance and output capacitance, brings potential advantages over traditional Si-based FETs. Research on the multiple advantages that GaN FETs can bring into power electronics has been one of the main focuses of academia and industry for the last decade. One of the main benefits of GaN devices are the reduced switching losses due to the low C_{oss} and negligible reverse recovery losses (Q_{rr}). Even with the soft-switching characteristics of the SRC, the utilization of GaN devices can still bring

Table 3.3: Specifications of the GaN devices used in the analysis.

Port	Switches	Reference	V, $R_{ds,on}$
Port-1	$S_1 - S_4$	GS61008	100 V 9.5 mΩ
Port-2	$T_1 - T_4$	GS66508	650 V 63 mΩ
Port-3	$Q_1 - Q_4$	GS66504	650 V 130 mΩ

additional advantages. In hard-switched power converter topologies the $R_{ds,on}$ and C_{oss} often results in a compromise between conduction losses and switching losses. However, in the SRC lower C_{oss} means less circulating energy required to achieve ZVS hence, smaller rms currents. Therefore, the C_{oss} has indirect contribution to the conduction loss.

GaN devices from Table 3.3 have been compared to the Si devices from Table 3.2. Fig.3.21 shows the rms resonant currents at input and output side ports in terms of dead-time for different operating power. It can be observed that, besides a reduction of the rms currents, the dependence of dead-time towards rms currents variations is also attenuated. In other words, with GaN devices the selection of dead-time has less impact on the converter rms currents, which simplifies the design process. Fig.3.22 illustrates the conduction losses of Si and Gan devices. From Fig.3.22 it can be inferred that the utilization of GaN FETs result in reduced conduction losses at lower dead-times compared to the Si MOSFETs. In addtion, the reduced C_{oss} of GaN FETs also allows a reduction of the turn-off losses as shown in Fig.3.23. The total semiconductors losses are shown in Fig.3.24.

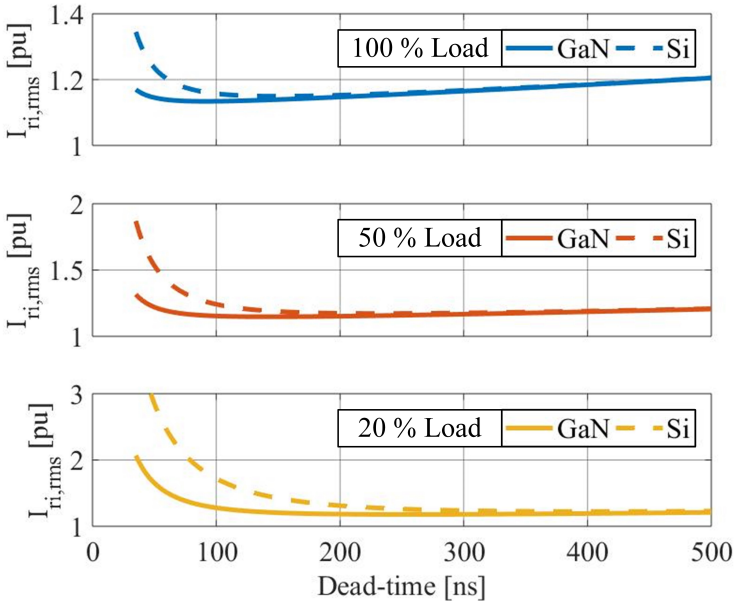
3.4.3 Transformer design

The design of the transformer has also been addressed in App.E.

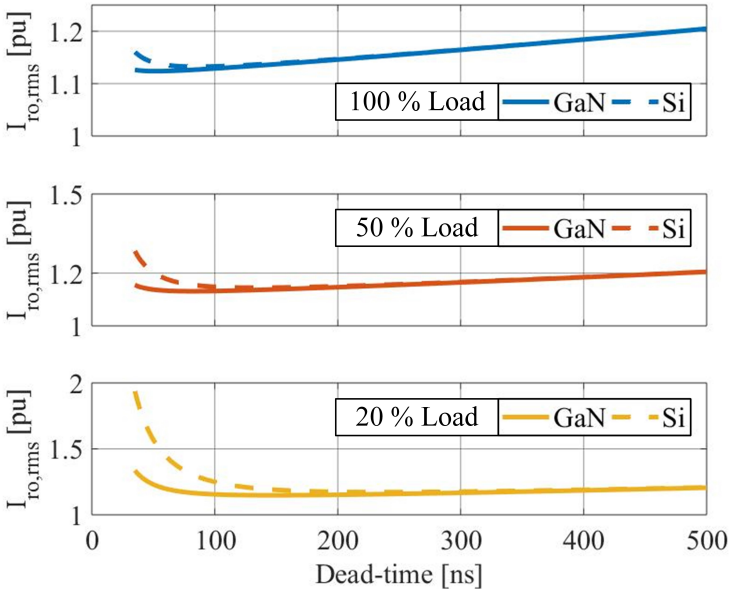
In order to optimize the transformer losses, a computer-aided design was implemented. The algorithm flowchart is shown in Fig. 3.25. A database with suitable core sizes was created, which includes three different core sizes fabricated with N87 material: (I) ETD 49/25/16, (II) ETD 54/28/19 and (III) ETD 59/31/22.

The algorithm starts by selecting the smallest core size and entering into a loop where the peak flux density B_{max} is swept from 50 mT to 300 mT. The wire gauge is selected at the skin depth δ to reduce the skin effect as given by (3.22) , and the number of strands is selected for a current density of 5 A cm^{-2}. The number of turns is calculated with (3.23) for B_{max} at the transformer side with maximum flux linkage. Note that the maximum flux linkage occurs at the high voltage side V_3. Then, the implementation viability is verified by comparing the available window area and the required area by the design. If the design is successful, the transformer losses are calculated. Otherwise B_{max} is increased and the transformer is redesigned. When B_{max} reaches 300 mT a larger core is selected.

$$\delta = \frac{7.5}{\sqrt{f_s}}(cm) \tag{3.22}$$



(a) Input side.



(b) Output side.

Figure 3.21: Theoretical per-unit rms currents in function of dead-time, where the rms current base value is the dc port current I.

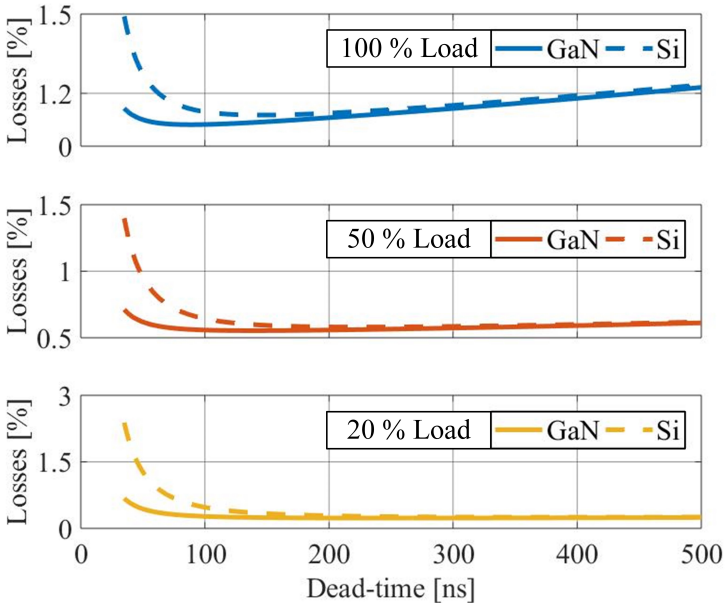
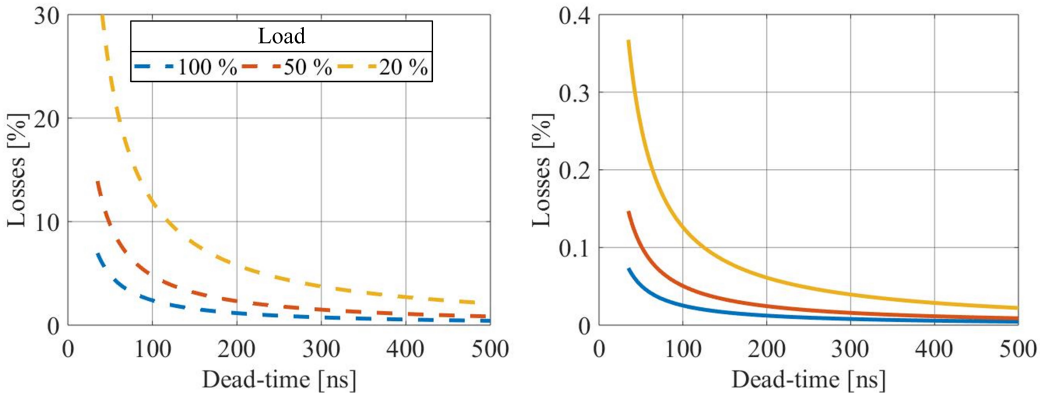
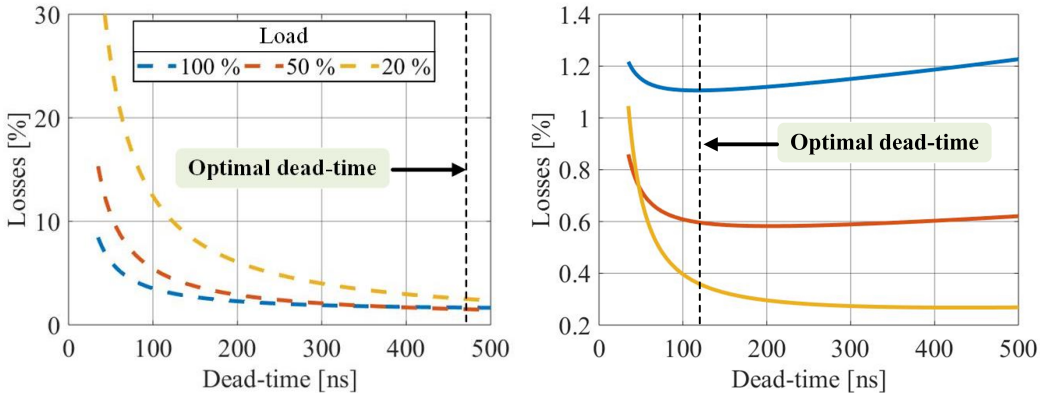


Figure 3.22: Conduction losses in function of dead-time.



(a) Si MOSFETs. **(b)** GaN FETs.

Figure 3.23: Switching losses in function of dead-time.



(a) Si MOSFETs. **(b)** GaN FETs.

Figure 3.24: Total semiconductors losses in function of dead-time.

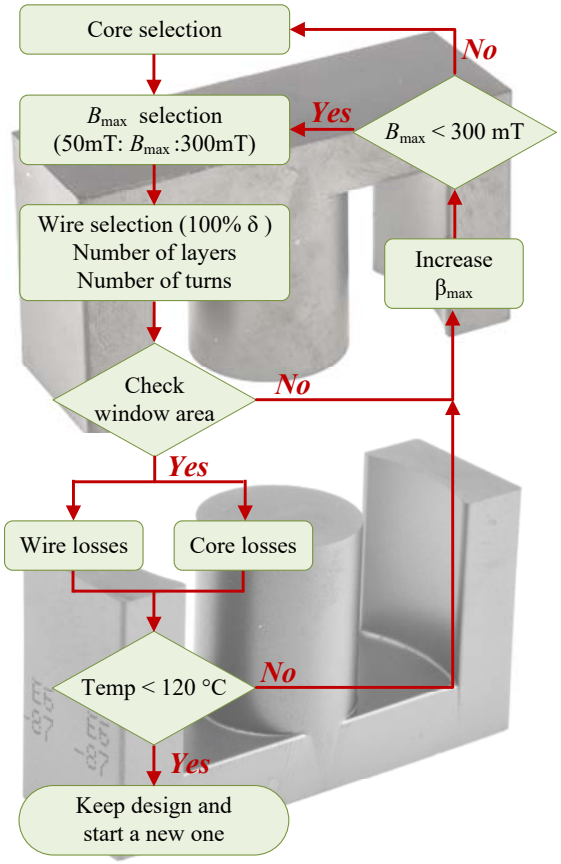


Figure 3.25: Simplified flowchart of the algorithm used to design the optimized transformer.

$$N_3 = \frac{V_3}{4 f_s A_c B_{max}} \tag{3.23}$$

where

N_3: Number of turns at Port-3.

A_c: Cross-sectional area of the transformer core.

η_0: Permeability of free space $\eta_0 = 4\pi \cdot 10^{-7} Hm^{-1}$.

To calculate the copper losses, first the dc winding resistance is calculated by (3.24) and Dowell's equations are used to estimate the ac resistance (3.25). An interleaved arrangement of the windings is assumed in the calculations. Then, the copper losses for a multi-winding transformer can be calculated by (3.26), where the rms current at each winding is calculated with (3.4) or (3.5) whether the port behaves as an input or an output. Core losses can be estimated using the Steinmetz equation given by (3.27). The overall losses are calculated with (3.28).

$$R_{dc,n} = \frac{\rho_{cu} N_n MLT}{A_{AWG}} \tag{3.24}$$

$$\frac{R_{ac,n}}{R_{dc,n}} = \frac{\Delta}{2}\left[\frac{\sinh\Delta + \sin\Delta}{\cosh\Delta - \cos\Delta} + (2m-1)^2\frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta}\right] \tag{3.25}$$

$$P_{Tr,w} = \sum_{n=1}^{p} R_{ac,n} I_{rn,rms}^2 \tag{3.26}$$

$$P_{Tr,c} = \kappa f_s^{\alpha} B_{max}^{\beta} \tag{3.27}$$

$$P_{Tr} = P_{Tr,w} + P_{Tr,c} \tag{3.28}$$

where

MLT: Core mean-length-turn.

ρ_{cu}: Resistivity of the copper. $\rho_{cu} = 1.72 \times 10^{-8}\Omega m$ @ 20 °C.

N_n: Number of turns at transformer port n.

A_{AWG}: Wire cross-sectional area.

$R_{dc,n}$: Dc resistance at transformer port n.

$R_{ac,n}$: Ac resistance at transformer port n.

Δ: h/δ.

h: Conductor height.

m: Number of layers. $m = 1$ for interleaved multilayer windings.

$I_{rn,rms}$: Rms current at port n.

K, α, β: Core material parameters provided by the manufacturer. For N87 material $K = 3.73 \cdot 10^{-7}$, $\alpha = 2.1$ and $\beta = 2.48$.

Finally, operation under safe temperature range is verified with 3.29 assuming natural convection cooling. The maximum temperature allowed is set to 120 °C. If the condition is fulfilled, the design is saved and a new one starts. The design that results in lowest losses is chosen for implementation.

$$P_{TR} \leqslant \frac{T_{max} - T_{amb}}{Tr_c} \tag{3.29}$$

where T_{max} is the maximum safe-operating temperature of the transformer core, T_{amb} is the ambient temperature and Tr_c the core thermal resistance given by the manufacturer.

The resulting transformer specifications are given in Table 3.4. Litz wire with 20 strands of AWG26 wire was used. For the low voltage side 6 paralleled layers of the same wire were utilized. An interleaved winding structure was performed to reduce the ac resistance.

Table 3.4: Transformer specifications

Core	No. of turns	Wire	R_{dc}
ETD	$N_1 = 5$	120 x AWG26	2 mΩ
59/31/22	$N_2 = 25$	20 x AWG26	38 mΩ
	$N_3 = 37$	20 x AWG26	65 mΩ

3.4.4 Resonant capacitors

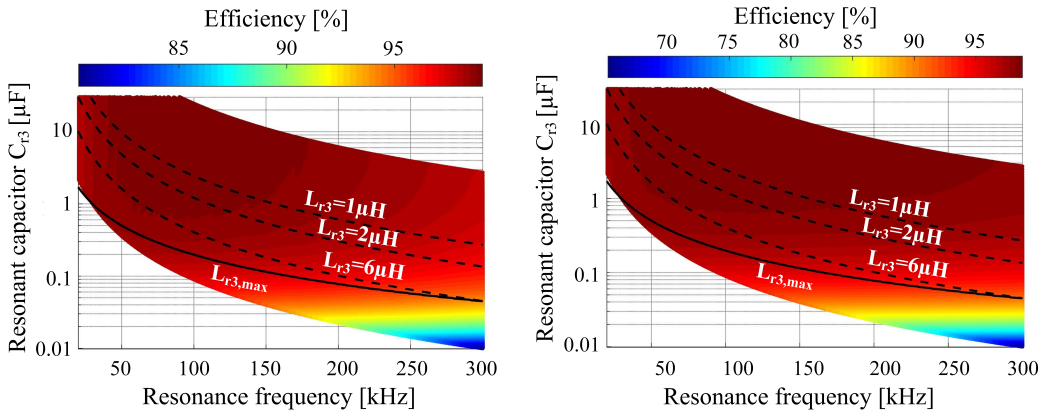
To reduce the losses at the resonant capacitors Polyphenylene Sulfide (PPS) and Polypropylene (PP) film capacitors were used. This capacitors feature low dissipation factor and low dependency of the electrical parameters to temperature and frequency. Losses at the resonant capacitors are due to the equivalent series resistance (ESR) as given by (3.30), where the rms current at each winding is calculated with (3.4) or (3.5) whether the port behaves as an input or an output. The ESR is given by the switching frequency, the capacitance and the dissipation factor $\tan\delta$ from the manufacturer's datasheet as shown in (3.31).

$$P_{C_r} = \sum_{n=1}^{p} ESR_n I_{rn,rms}^2 \tag{3.30}$$

$$ESR = \frac{\tan\delta}{2\pi f_s C_r} \tag{3.31}$$

3.4.5 Efficiency analysis

In App.E theoretical efficiency of a TP-SRC for the specifications given in Table 3.1 is analysed in terms of the resonance frequency and resonant tank components size. Fig.3.26 shows the theoretical efficiencies obtained.



(a) 50 % load

(b) 100 % load

Figure 3.26: Theoretical efficiency of 3P-SRC in terms of resonance frequency and resonant components size. Efficiency is calculated for dual-output mode with equal power sharing among ports.

3.5 Experimental prototypes

The design methodology for the SRC dc transformer with integrated resonant inductors is depicted with the flowchart in Fig.3.27. The design steps are summarized below:

1. The semiconductors are selected according to the converter specifications and to other requirements if apply, such as costs.
2. The switching frequency is selected for the highest efficiency if it is not given by the specifications. Other factors, such as power density and EMI, may also be taken into account.
3. The optimal combination of dead-time and magnetizing inductance for reduced losses is computed.
4. The transformer is designed and implemented, with design efforts to reduce the leakage inductance.
5. The leakage inductance of the transformer is measured and if possible, the PCB parasitic inductances of the transformer can also be measured for a more accurate measurement of the resonance inductance.
6. The minimum inductance ratio allowed to achieve ZVS at the maximum power transfer is calculated and verified with (3.9).
   (a) If the condition is not fulfilled, the switching frequency is decreased. If it is not allowed due to the converter specifications, the dead-time should be decreased. When using GaN devices, there is more flexibility on the dead-time, since it has less impact on the rms currents.
7. Verify that the load regulation characteristics of the converter fulfil the gain requirements. Since the resonant tank is asymmetric, i.e. different inductance ratios at each port, the criterion has to be verified for all operating modes and power flow directions.

(a) If the condition is not fulfilled, the leakage inductance of the transformer and inductance parasitics have to be reduced.

8. The theoretical resonant capacitors are calculated and assembled.

9. The resonance frequency matching is carried out and the switching frequency is adjusted accordingly.

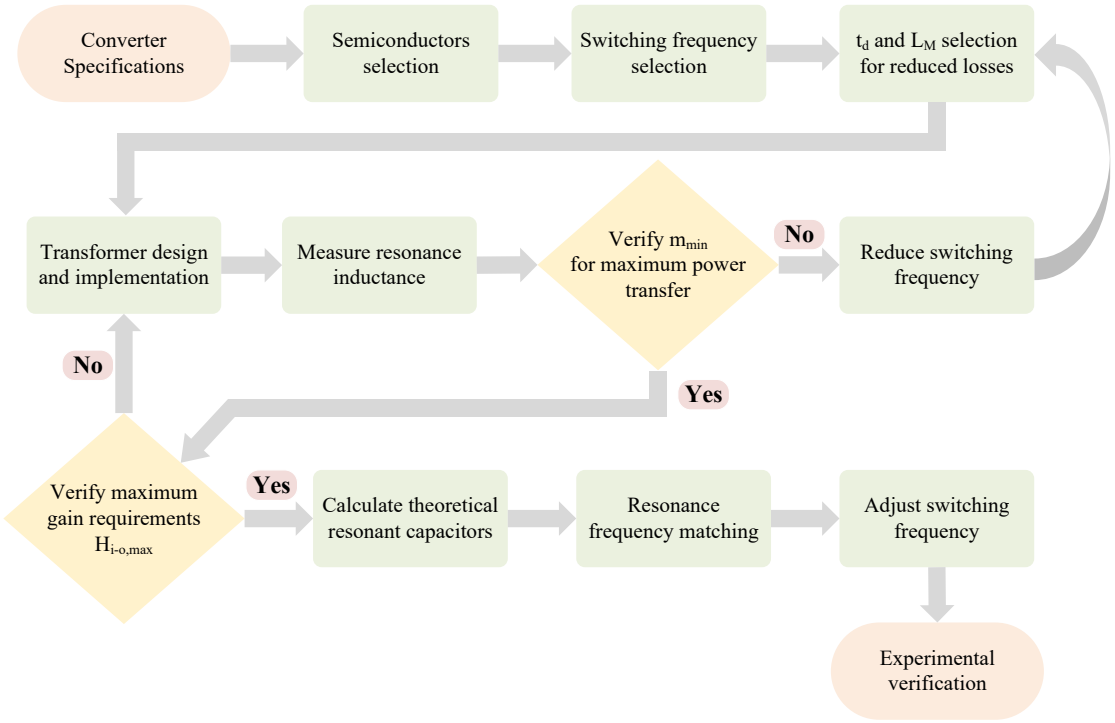


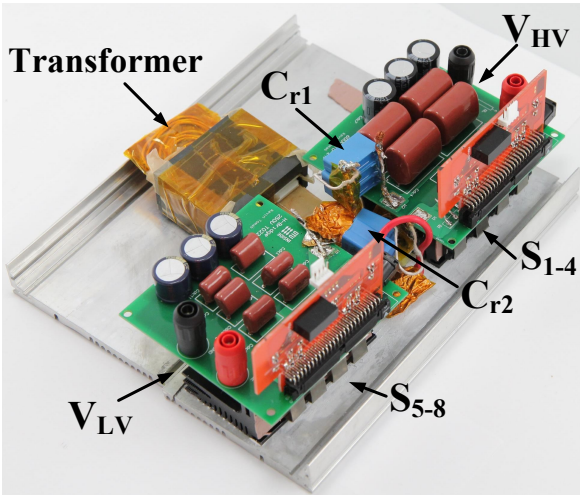
Figure 3.27: Design flowchart when using integrated resonant inductors.

3.5.1 Prototypes summary

Below a summary of the prototypes developed during this PhD project is given. The process involved in the design and development of these prototypes have provided the knowledge and expertise to build-up the design considerations and design optimizations described in this chapter. Therefore, it should be expected that the prototypes below have not been designed with the optimised methodology described in this chapter.

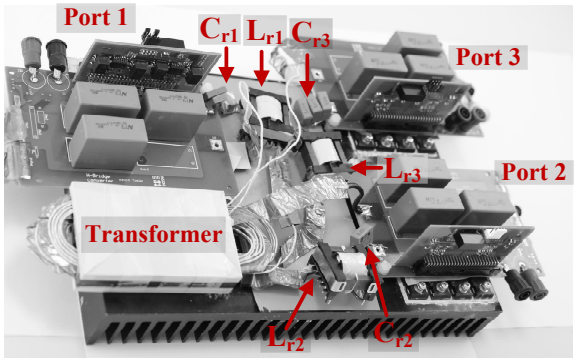
Two-port Series Resonant Converter

Specifications		
Voltage port 1	V_{LV}	48 V
Voltage port 2	V_{MV}	400 V
Maximum power	P_{max}	1 kW
Switching frequency	f_s	148 kHz
Features		
Semiconductors	Port 1 (V_{LV})	IPW65R420CFD (650 V,490 mΩ)
Silicon	Port 1 (V_{HV})	IPP034N08N5 (80 V,3.4 mΩ)
Synchronous rectification	Yes	
Resonant inductors	Integrated	
Efficiency	20 % load	89.3 %..93.1 %
	50 % load	94.1 %..96.7 %
	100 % load	94.1 %..97.1 %
	Maximum	97.14 %
Picture of the prototype		



Three-Port Series Resonant Converter Ver.1

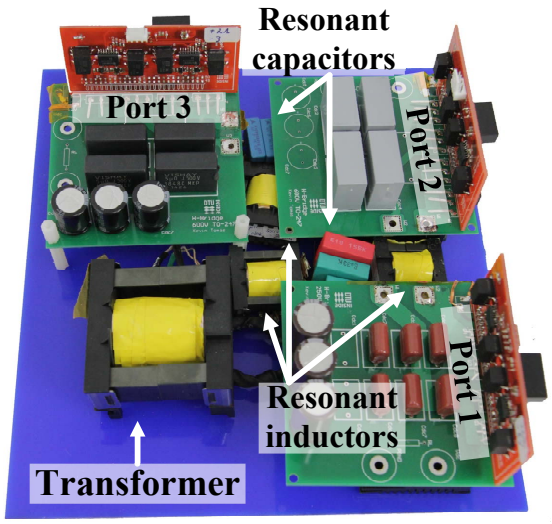
Specifications		
Voltage port 1	V_{LV}	200 V
Voltage port 2	V_{MV}	400 V
Voltage port 3	V_{HV}	600 V
Maximum power	P_{max}	1 kW
Switching frequency	f_s	145 kHz
Features		
Semiconductors	Port 1 (V_{LV})	
	Port 2 (V_{MV})	
	Port 3 (V_{HV})	
Synchronous rectification	No	
Resonant inductors	External	
Efficiency	20 % load	88.5 %..91 %
	50 % load	94 %..95 %
	100 % load	94 %..95.9 %
	Maximum	95.9 %
Picture of the prototype		



Three-Port Series Resonant Converter Ver.2

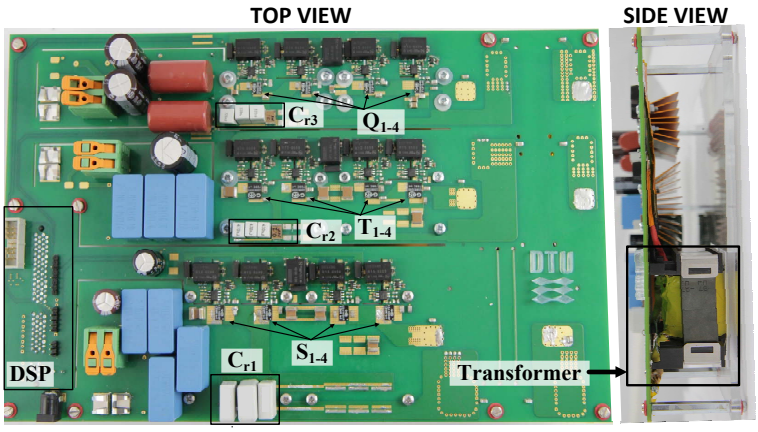
Specifications		
Voltage port 1	V_{LV}	100 V
Voltage port 2	V_{MV}	400 V
Voltage port 3	V_{HV}	600 V
Maximum power	P_{max}	1 kW
Switching frequency	f_s	144 kHz
Features		
Semiconductors	Port 1 (V_{LV})	IPP114N12 (120 V,11.4 mΩ)
Si (V_{LV})	Port 2 (V_{MV})	SCT3120AL (650 V,120 mΩ)
SiC (V_{MV}, V_{HV})	Port 3 (V_{HV})	SCT3120AL (650 V,120 mΩ)
Synchronous rectification	Yes	
Resonant inductors	External	
Efficiency	20 % load	88.5 %..90.0 %
	50 % load	94.7 %..96.3 %
	100 % load	96.5 %..98.0 %
	Maximum	98.0 %

Picture of the prototype



Three-Port Series Resonant Converter Ver.3

Specifications		
Voltage port 1	V_{LV}	80 V
Voltage port 2	V_{MV}	400 V
Voltage port 3	V_{HV}	600 V
Maximum power	P_{max}	1.5 kW
Switching frequency	f_s	149 kHz
Features		
Semiconductors	Port 1 (V_{LV})	GS61008P (100 V,9.5 mΩ)
GaN	Port 2 (V_{MV})	GS66506T (650 V,63 mΩ)
	Port 3 (V_{HV})	GS66504B (650 V,130 mΩ)
Synchronous rectification	Yes	
Resonant inductors	Integrated	
Efficiency	20 % load	88.8 %
	50 % load	98.7 %
	100 % load	98.1 %
	Maximum	98.8 %
Picture of the prototype		



4

Advances in Power Electronics for Energy Storage Systems

The uncontrollable inherent characteristics of distributed energy sources (DES) makes the ESSs indispensable elements for the future distribution grid. ESSs are essential to coordinate DES in smart grids, aiming to achieve an effective way of balancing supply and demand in order to efficiently deliver sustainable, economic and secure electricity supply. To fully exploit the benefits of ESSs in the smart grid environment, high efficiency power electronics play a key role in the integration of energy storage into the microgrids.

As discussed in section 2.1.1, due to the electrical characteristics of ESS, high voltage gain and wide voltage range power conversion systems (PCS) are required to interconnect the ESS to the common dc bus. In this chapter, three different PCS featuring different characteristics with the common goal of high efficiency power conversion are presented. The contributions of this chapter are summarized below:

1. Partially paralleled DAB with dual phase shift control: A DAB derived topology, wherein high voltage gain and improved controllability is achieved. Appendices F and G.
2. Series-connected PCS: A PCS architecture suitable for wide voltage range ESS, wherein high efficiency is obtained by a rearrangement of the conventional connection between input and output of the PCS. Appendices H and I.
3. Three-port converter with direct energy storage: A simple multiple port converter derived from the buck and boost topologies suitable for household PV systems with local energy storage, wherein energy transfer between each unit is performed in a single power conversion stage. App. J.

4.1 Partially Paralleled Dual Active Bridge Converter with Dual Phase-Shift Control

In accordance with an essential principle of connecting the circuit parts which need to carry high current in parallel and connecting the circuit parts which need block high voltage in series, a DAB-derived topology, so-called Partially Paralleled Dual Active Bridge (P^2DAB) converter is presented. The main characteristics of the P^2DAB are summarized below:

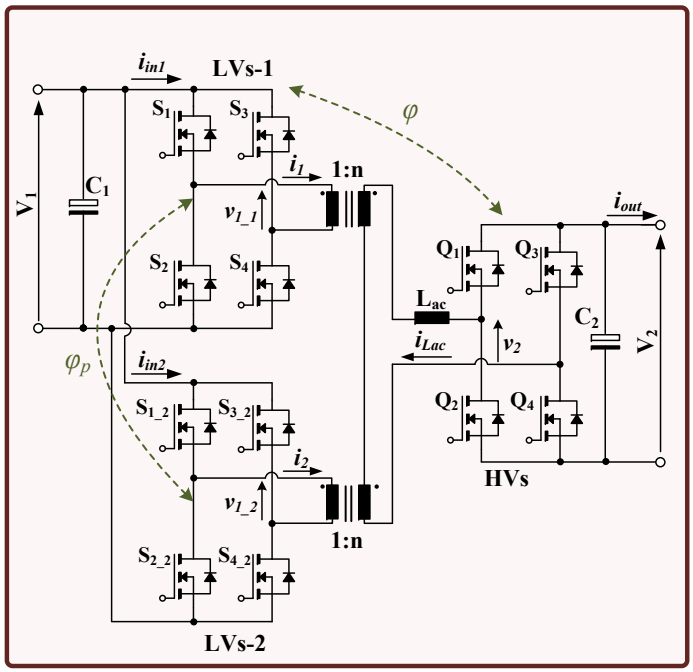


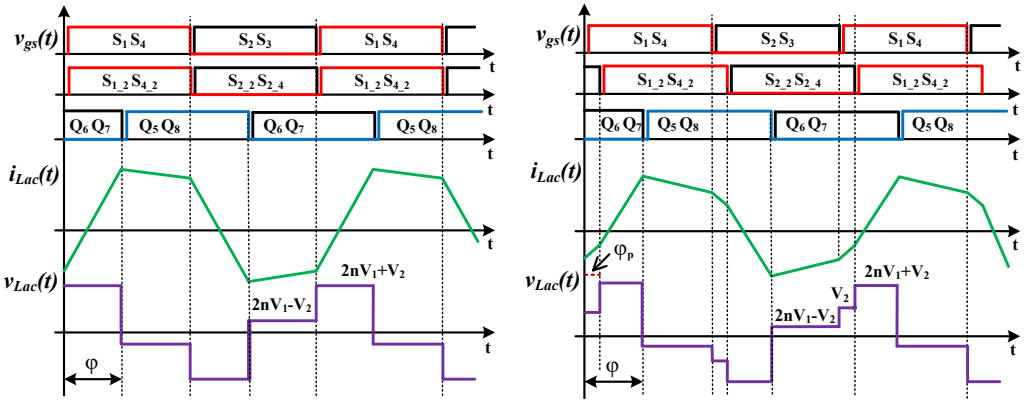
Figure 4.1: Topology of the proposed P^{2}DAB converter.

- The series connection of the transformer windings on high voltage side (HVs), reduces the voltage stress of the transformer and the required number of turns, hence easing the design for high voltage gain conversion.
- Ac current balancing between the parallel full-bridges is inherently ensured by the series connection of the transformers windings.
- Phase shift regulation between the paralleled full bridges on low voltage side (LVs), adds an additional degree of freedom to control power, hence the P^{2}DAB operating range is extended.

4.1.1 Topology and operating principle

The topology of the proposed converter is shown in Fig.4.1. The P^{2}DAB comprises a low voltage side (LVs) with V_1 and a high voltage side (HVs) V_2, two dc capacitors C_1 and C_2 connected to V_1 and V_2 respectively and two high frequency transformers with turns ratio n. The high voltage side V_2 is connected to a single high voltage active bridge and to the transformers, wherein the transformers windings are connected in series. Two active low voltage bridges are connected in parallel to the low voltage side V_1. Each low voltage bridge is connected to a transformer winding.

Due to the series connection of the HVs transformer windings, the reflected currents at the LVs are equal as given by (4.1). The series-to-parallel configuration of the transformer windings splits the ac high-current loops into two smaller ac current loops, where each of them only has half ni_{Lac}. At the same time, compared to the conventional DAB high frequency transformer, the voltage stress of the HVs transformer windings is also halved. Decrease of voltage stress allows a reduced number of turns and the



(a) $\varphi_p = 0$ and $0 < \varphi < 0.25$. **(b)** $0 < \varphi_p < \varphi$ and $\varphi < 0.25$.

Figure 4.2: Switching patterns of HB-LV1 ($S_1 - S_4$), HB-LV2 ($S_{1_2} - S_{4_2}$) and HB-HV ($Q_1 - Q_4$), ac inductor current i_{Lac} and voltage v_{Lac}.

decrease of the current stress allows a reduced copper thickness. This simplifies the transformer design and might potentially reduce the manufacturing costs.

$$i_1 = i_2 = n i_{Lac} \tag{4.1}$$

Besides the conventional control methodology of the DAB, where a phase-shift φ is applied between the LVs and the HVs bridges, a phase-shift φ_p between the two paralleled bridges can also be implemented. In that manner, φ_p gives an additional control freedom to regulate the output power or voltage. Fig.4.2 illustrates the switching patterns and the ac inductor voltage and current waveforms. The steady-state waveforms for $\varphi_p = 0$ are shown in Fig.4.2a and for $0 < \varphi_p < \varphi$ are shown in Fig.4.2b.

From Fig.4.2 the inductor current can be calculated as a function of φ and φ_p and, by applying the mean-value theorem to the ac inductor, the power transfer equation given by (4.2) can be calculated. The phase-shift angle is limited to be smaller than $\pi/2$, i.e. $max(\varphi, \varphi_p) \leq 0.25$. More details on the derivation of the power transfer equation can be found in Appendices F and G.

$$P = \begin{cases} \frac{2nV_1V_2}{f_s L_{ac}} \varphi \left(1 - 2\varphi + 2\varphi - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi}\right) & \text{for} \quad 0 < \varphi_p < \varphi \\ \frac{4nV_1V_2}{f_s L_{ac}} \left(\varphi - \frac{\varphi_p}{2}\right)\left(\frac{1}{2} - \varphi_p\right) & \text{for} \quad \varphi < \varphi_p < 0.25 \end{cases} \tag{4.2}$$

where the phase-shift angles φ and φ_p are represented as a percentage of the switching period T_s, f_s refers to the switching frequency and L_{ac} is the sum of the external inductance and the transformer leakage inductance seen from the HVs.

Moreover, if $\varphi_p = 0$, the power equation without additional phase-shift between LVs bridges is expressed by (4.3).

$$P(\varphi_p = 0) = \frac{2nV_1V_2}{f_s L_{ac}} \varphi(1 - 2\varphi) \tag{4.3}$$

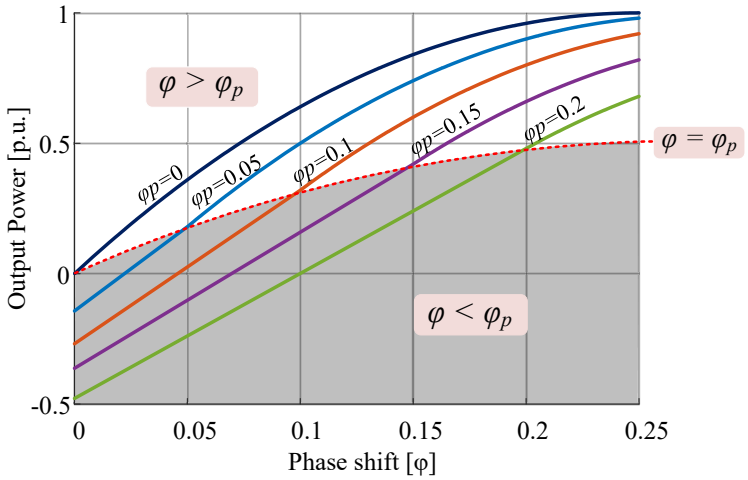


Figure 4.3: Transferred power in terms of φ and φ_p, where the the base unit is $nV_1V_2/4f_sL_{ac}$.

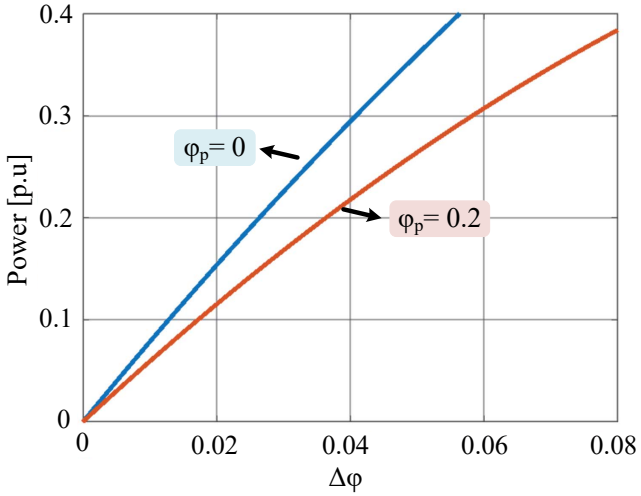
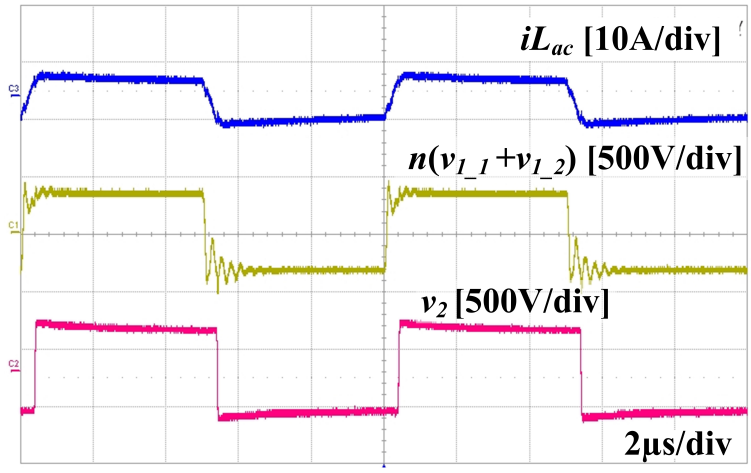


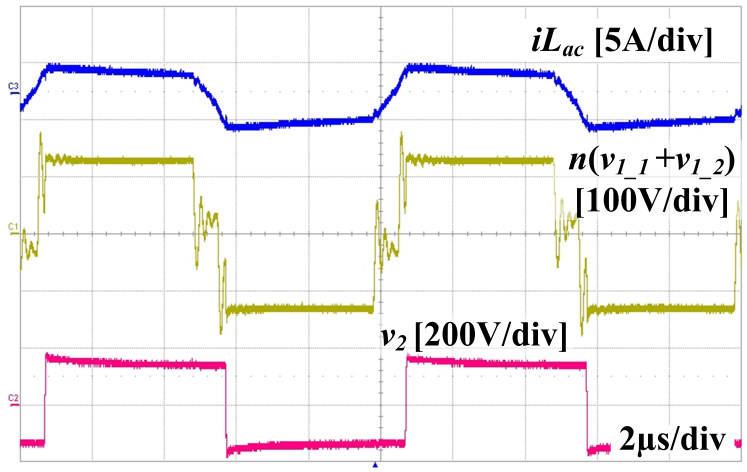
Figure 4.4: Transferred power in terms of $\Delta\varphi$ for $\varphi_p = 0$ and $\varphi_p = 0.2$.

Figure 4.3 shows the transferred power in terms of φ and φ_p in per-unit, where the base power is $nV_1V_2/4f_sL_{ac}$. It can be observed that for the same transferred power there are multiple combinations of φ and φ_p. As shown in Fig.4.4, with an increasing φ_p, the slope of transferred power versus the variation of φ ($\Delta\varphi$) is decreased. In that manner the controllability of the DAB topology can be improved. Specially under light load conditions, where, for $\varphi_p = 0$, small variations of φ may incur into large variations of transferred power.

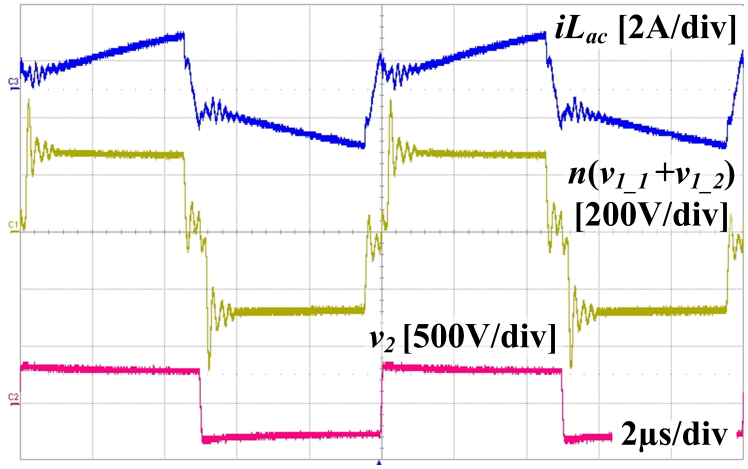
Figure 4.5 shows the experimental waveforms from a 1 kW rated power P^{2}DAB prototype under different phase shift angles combinations. The results presented match with the theoretical analysis. When $\varphi_p \neq 0$, the voltage across the series connected high-voltage windings becomes a three-level waveform that changes the current waveforms accordingly.



(a) $\varphi_p = 0$, $\varphi = 0.034$ and $n(v_{1,1} + v_{1,2}) = v_2$.



(b) $\varphi_p = 0.06$, $\varphi = 0.08$ and $n(v_{1,1} > v_{1,2}) = v_2$.



(c) $\varphi_p = 0.04$, $\varphi = 0.05$ and $n(v_{1,1} < v_{1,2}) = v_2$.

Figure 4.5: Experimental waveforms of the reflected LVs voltage $n(v_{1,1}+v_{1,2})$, voltage v_2 and ac inductor current i_{Lac} with different phase shift angles φ_p and φ.

4.1.2 Design considerations

Because of the series winding connection on the HVs, the rms currents is the same in the LVs windings and semiconductors. On the other hand, adding φ_p creates an unbalance between the real power transferred by each LVs bridge. For instance, when $0 < \varphi_p < \varphi$, the average input current to the LVs bridges current can be calculated by (4.4) and (4.5).

$$I_{in1,avg} = \frac{n^2 V_1}{f_s L_{ac}} [2M(1-2\varphi) + \varphi_p(2\varphi_p - 1)] \tag{4.4}$$

$$I_{in2,avg} = \frac{n^2 V_1}{f_s L_{ac}} [2M(\varphi - \varphi_p)(1-2\varphi+2\varphi_p) + \varphi_p(1-2\varphi_p)] \tag{4.5}$$

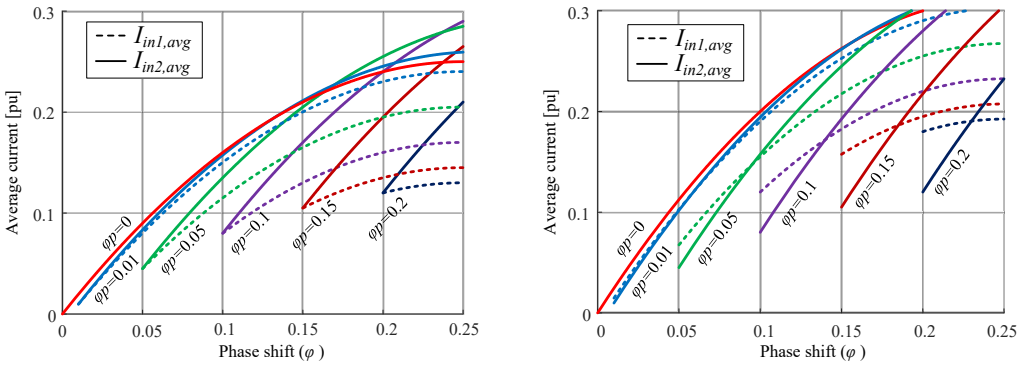
where

$$M = \frac{V_2}{2nV_1} \tag{4.6}$$

Fig.4.6 shows the LVs average currents $I_{in1,avg}$ and $I_{in2,avg}$ in per-unit, where the base value is n^2V_1/f_sL_{ac}, in terms of φ and φ_p. It can be observed that the average current of the LVs bridges, so as their input real power, diverse from each other due to φ_p. For instance, high-frequency ac current and voltage waveforms for $0 < \varphi_p < \varphi$ on the LVs are presented in Fig.4.7. As highlighted by the shaded areas in Fig.4.7, the reactive power can be found when the instantaneous ac voltage and current have opposite polarity. With this illustrative example it can be observed that real power in the lagging LVs bridge is increased while the reactive power in the leading bridge is increase and thus, the unbalance of the average current between paralleled bridges.

It can also be observed that the turn-off event at the lagging bridge HB-LV2 occurs at lower current than the leading bridge HB-LV1. Therefore, the switches S_{1_2}-S_{4_2} will have lower turn-off losses than the switches S_1-S_4. On the other hand, in order to successfully charge and discharge the semiconductors' output capacitance and thus, achieve ZVS, the currents at the turn-off event must be large enough. Therefore, the lagging bridge HB-LV2 has a narrower ZVS range, since its turn-off current is lower than the current of the leading bridge HB-LV1. This is consistent with the analysis above, since HB-LV2 has less reactive power.

Figure 4.8 shows the experimental waveforms of the low-voltage side ac voltages and ac currents when $\varphi_p = 0$ and $\varphi_p \neq 0$. It can be observed that, the ac currents at the paralleled bridges are always the same regardless the phase-shift angles hence, the rms currents are also the same and (4.1) applies. Moreover, by regulating the phase-shift φ_p, the delayed bridge has less reactive component, as highlighted with the dashed line, which explains the unbalance of average input current among paralleled bridges. Finally, it can also be observed that the delayed bridge has a lower turn-off current, which leads to lower switching losses.



(a) $M = 1$ **(b)** $M \neq 1$

Figure 4.6: Average input current $I_{in1,avg}$ and $I_{in2,avg}$ in terms of phase shift angle φ and φ_p.

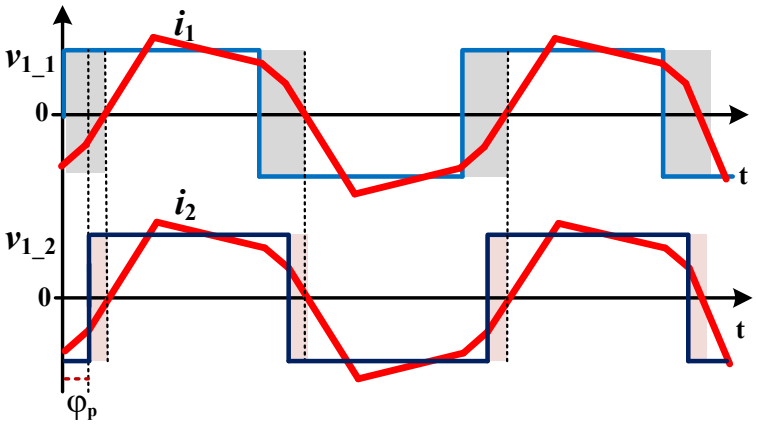


Figure 4.7: Ac voltage and current on the LVs of the P^{2}DAB converter.

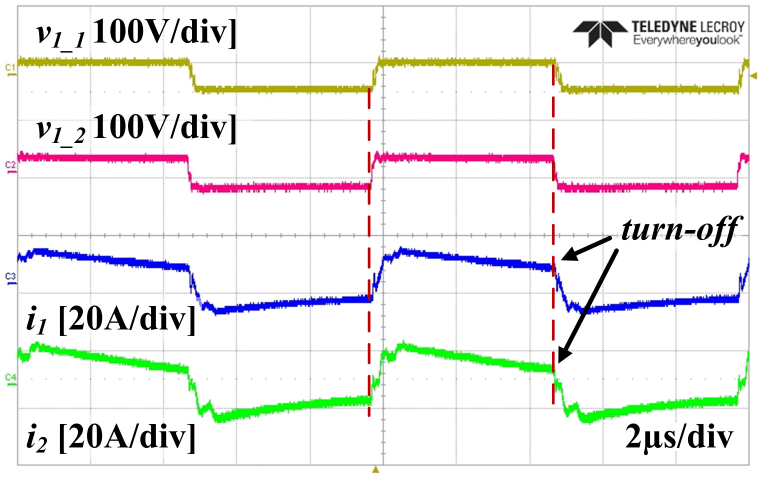
4.1.3 Experimental prototype

An experimental prototype based on the specifications given in Table 4.1 was implemented. More details about the prototype design and implementation can be found in [115]. A picture of the prototype is given in Fig.4.9.

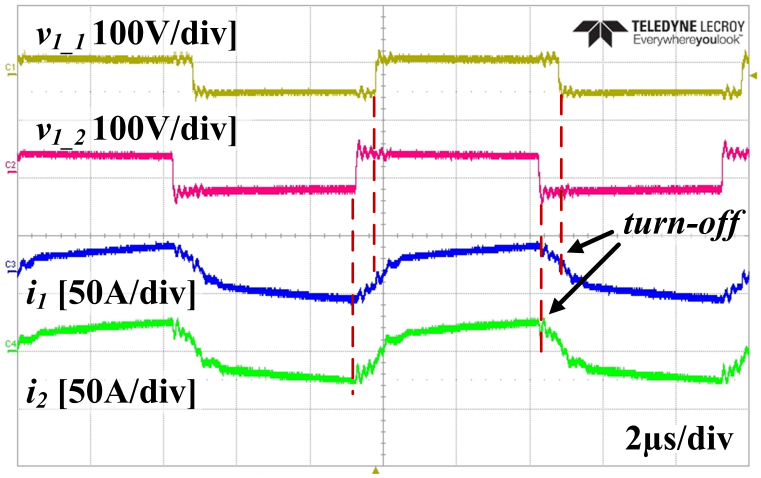
Table 4.1: Specifications for the P^{2}DAB converter.

Parameter	Value
LVs voltage V_1	48 V
HVs voltage V_2	400 V
Maximum output power	1.7 kW
Switching frequency	100 kHz

In Fig.4.15 a first set of experimental efficiency results is depicted. It can be observed that at light loads, the efficiency can be improved by increasing the phase-shift between paralleled bridges φ_p. *This project is currently under development.*



(a) $\varphi_p = 0$, $\varphi_p < \varphi$



(b) $\varphi_p \neq 0$, $\varphi_p < \varphi$

Figure 4.8: Experimental waveforms of voltage v_1, voltage v_{12}, current i_1 and current i_2.

4.2 Series-connected power conversion system

In this section a power conversion system for ESS is proposed. In this case, differently from the other studies presented in this thesis, power electronics improvements are achieved by rearranging the ESS system connection with the dc-dc converter and the dc bus.

4.2.1 System analysis

The conventional way of interconnecting ESS to the dc bus is shown in Fig.4.11a, where a positive and a negative terminal of a bidirectional dc-dc converter are connected to the ESS while the other positive and negative terminals of the dc-dc converter are connected to the regulated dc bus. According to Ohm's law, with the conventional power conversion system, the dc-dc converter must be rated, at least, at the maximum operating power of the ESS. The proposed power conversion system is based on the idea of connecting the ESS in series to the dc-dc converter and the dc bus hence, the

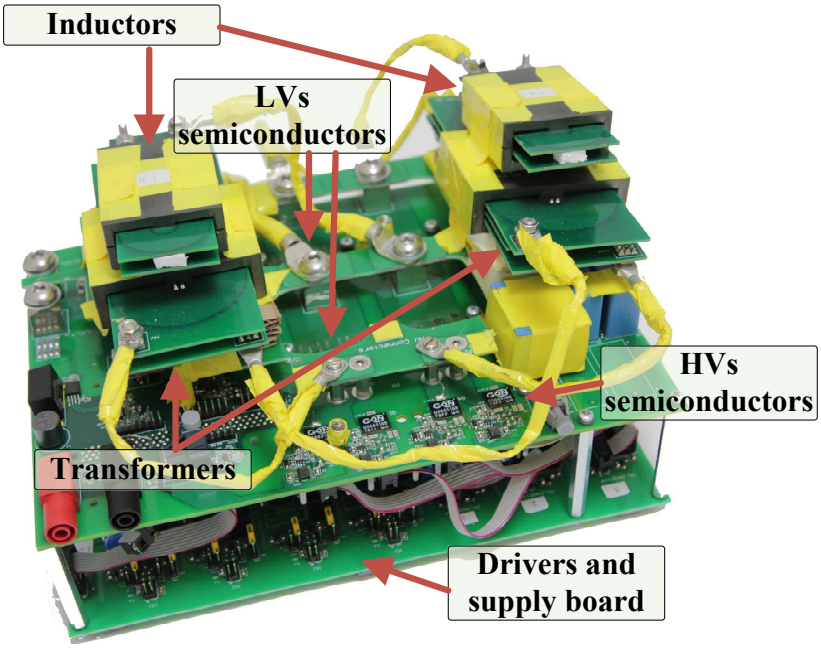


Figure 4.9: Picture of the P^{2}DAB converter prototype.

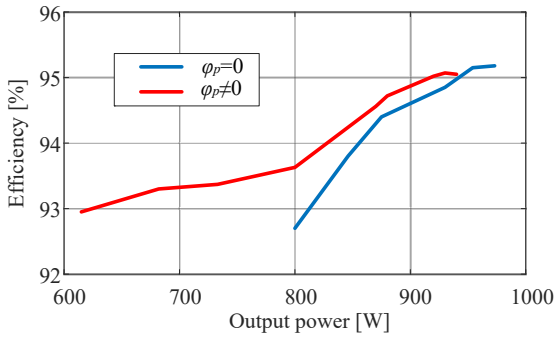
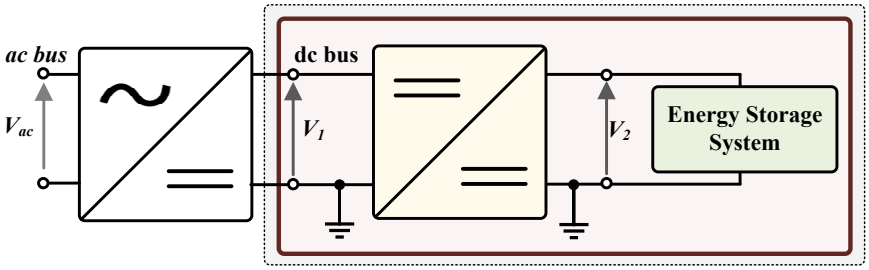


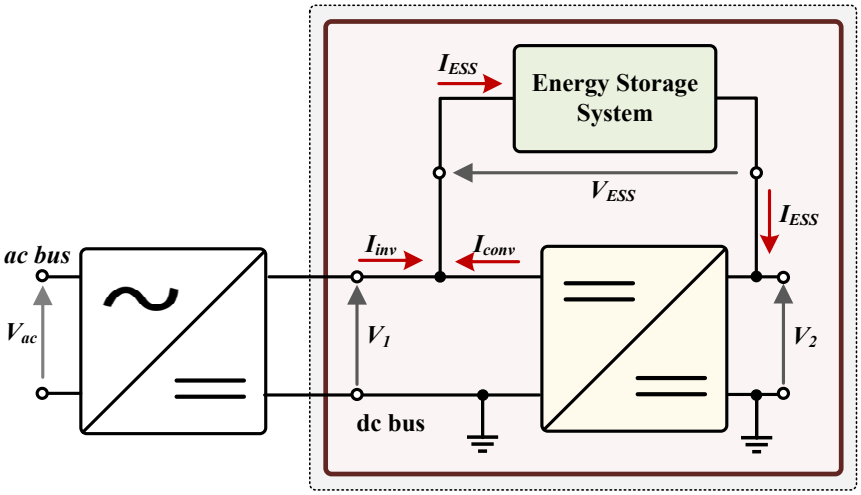
Figure 4.10: Efficiency curves of the P^{2}DAB converter prototype.

name series-connected power conversion system (S-PCS). Fig.4.11 shows the S-PCS. The ESS is connected between the positive terminals of the dc-dc converter, while the dc-bus V_1 is connected to a positive terminal and the reference of the dc-dc converter. In that manner and in accordance to Fig.4.11, the voltage V_2 is set by the differential voltage between the dc bus and the energy storage system ($V_1 - V_{ESS}$), hence, the dc-dc converter only processes the differential power between the dc bus and the ESS.

As an illustrative example, the lithium-ion based ESS with the specifications given in Table 4.2 is interconnected to a dc bus with $V_1 = 400\,\text{V}$. As discussed in section 2, maximum operating power occurs around the nominal voltage V_{nom} at maximum charge/discharge current. Therefore, the maximum power rating of the dc-dc converter can be calculated by (4.7). As observed in Fig.4.12, with the proposed power conversion architecture a reduction of nearly 80 % of the dc-dc converter power rating is achieved for the same ESS. Furthermore, if a dc-dc converter with a 95 % efficiency is utilized, the total system efficiency can be improved by nearly a 4 %.



(a) Conventional cascaded-connected dc-dc converter.



(b) Series-connected dc-dc converter.

Figure 4.11: Block diagram of a grid connected power conversion system for energy storage.

Table 4.2: Specifications for Lithium-ion batteries.

Parameter	Value
Nominal voltage (V_{nom})	330 V
Maximum charge voltage	380 V
Discharge cut-off voltage	270 V
Standard charge/discharge current	4 A
Rapid charge/discharge current	10 A

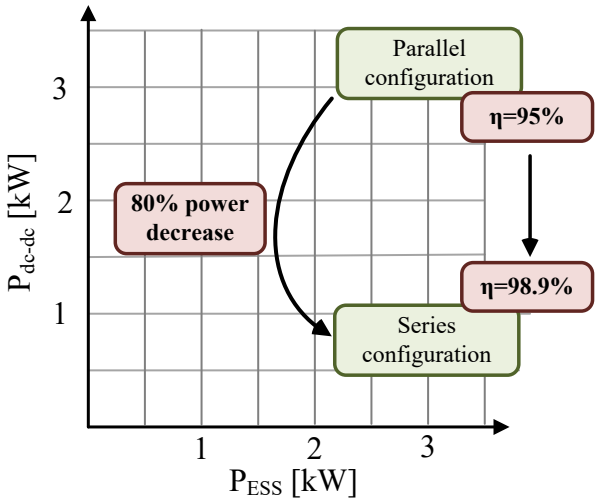


Figure 4.12: Efficiency and power density improvements with the series connection power conversion system.

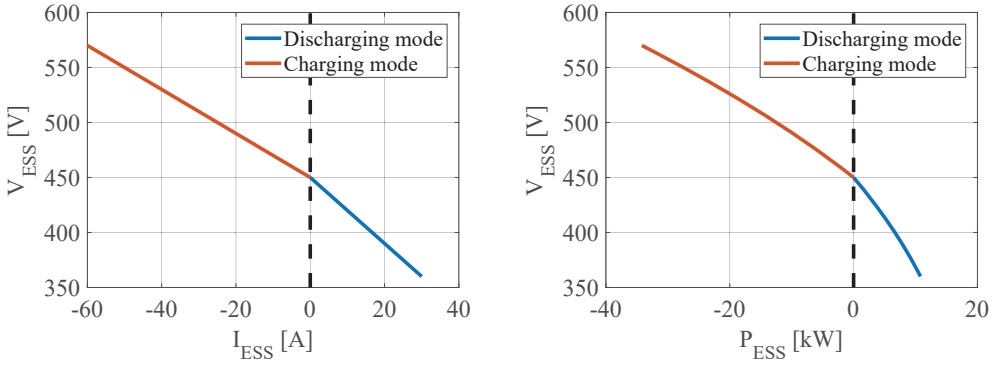
$$P_{dc-dc} = (V_1 - V_{nom})I_{ESS} \tag{4.7}$$

4.2.2 Design considerations

Typical operating conditions of lithium-ion and lead-acid batteries are around their nominal voltage regardless the current magnitude and direction. On the other hand, as discussed in section 2.1.1, other ESS such as Regenerative Fuel Cells (RFC) can operate in wide voltage ranges [116], App.I. Fig.4.13 shows the current-voltage and power-voltage characteristics of high voltage RFC stacks. FIt can be observed that the voltage is strongly dependent to the current and operating mode, where maximum voltage in discharging mode is 540 V and in charging mode is 360 V.

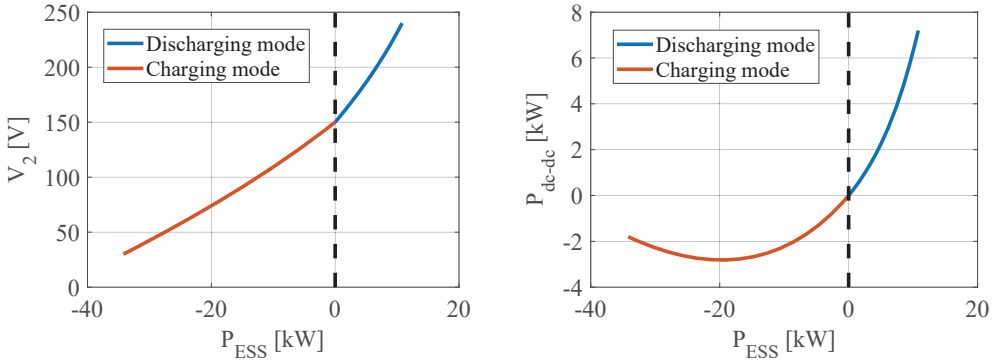
Considering a system with a dc bus voltage $V_1 = 600\,\text{V}$, the voltage V_2 and power processed by the dc-dc converter P_{dc-dc} are calculated and plotted in Fig.4.14. As can be observed from Fig.4.14b, a reduction of the dc-dc converter power rating is still possible, but in a more limited grade due to the RFC wide voltage range operation.

The overall system efficiency η_{system} is analyzed in Fig.4.15, where η_{system} has been calculated for different efficiencies of the dc-dc converter η_{dc-dc}. It can be inferred that with the S-PCS the impact of the dc-dc converter efficiency to the system efficiency is minimized since, for instance, with an efficiency as low as $\eta_{dc-dc} = 92\,\%$ the system efficiency remains between 95 % to 99.5 %. On the other hand, the wide voltage range characteristics of RFCs can dramatically affect the overall system efficiency. Fig.4.16 shows the differential voltage and power processed by the dc-dc converter for different number of RFCs stacks. It can be observed that when V_{ESS} decreases, the differential voltage V_2 increases and thus, the power processed by the dc-dc converter increases above P_{ESS}. Consequently, the system efficiency η_{system} can drop below η_{dc-dc}. Therefore, for an optimal operation of the S-PCS in efficiency terms, V_{ESS} should be close and below to V_1.



(a) Current-Voltage **(b)** Power-Voltage

Figure 4.13: Electrical characteristics of RFCs.



(a) $V_2 = V_1 - V_{ESS}$ **(b)** $P_{dc-dc} = V_2 I_{ESS}$

Figure 4.14: Dc-dc converter voltage and power rating in function of ESS power.

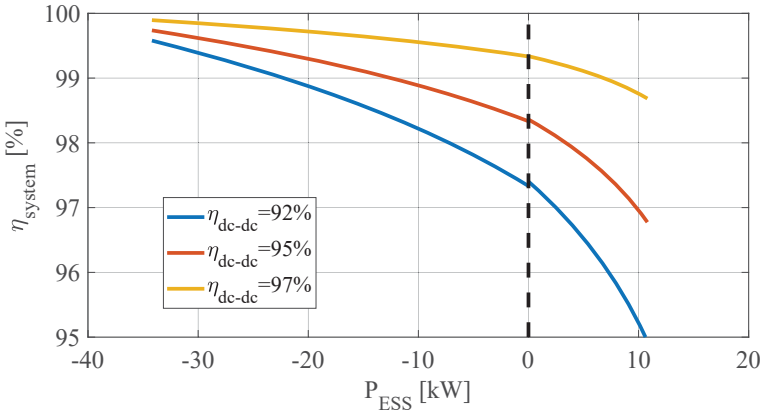
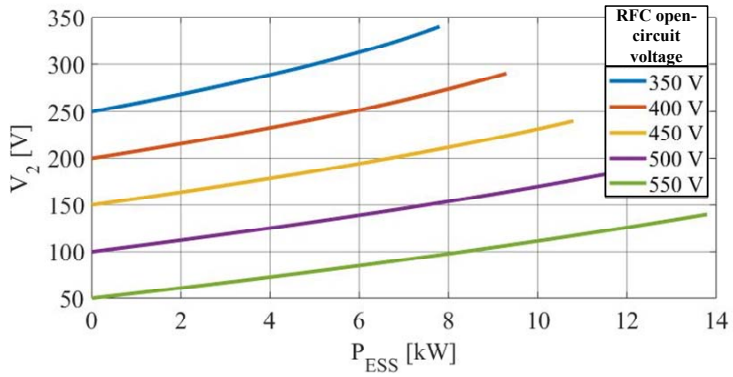
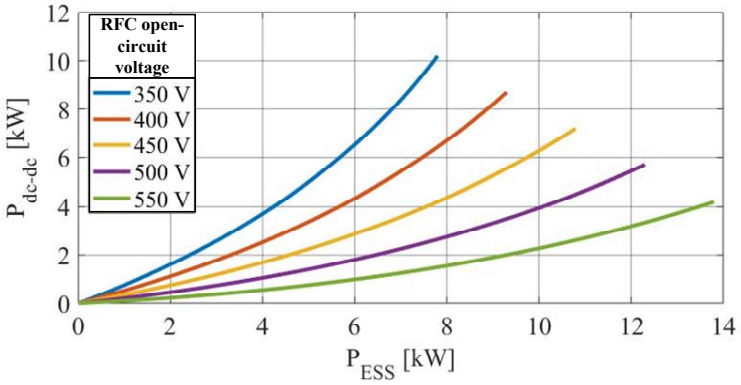


Figure 4.15: Overall system efficiency for different η_{dc-dc} .



(a) Differential voltage V_2



(b) Dc-dc converter power

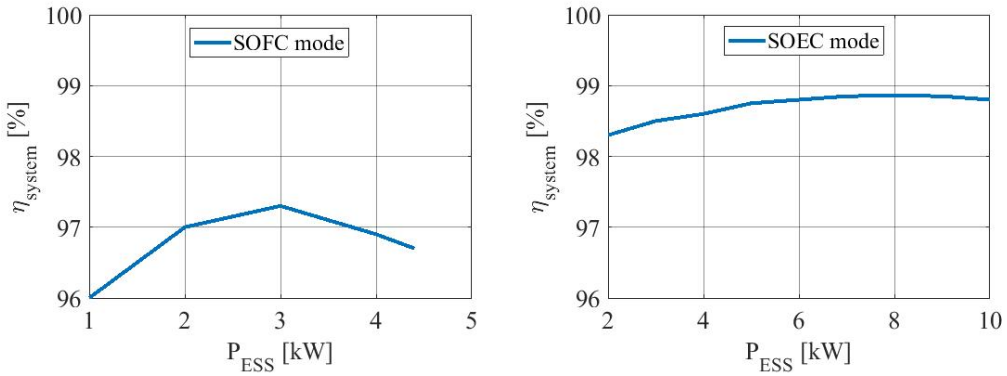
Figure 4.16: Dc-dc converter specification for ESS with different voltage ratings of the ESS. The legend shows the open-circuit voltage of different ESS configurations.

4.2.3 Dynamic power conversion system for SOEC/SOFC

To overcome the drawbacks due to the wide voltage range of RFC systems, in App.I, a dynamic power conversion system was presented. This power conversion system comprises two single pole double throw relays which connect the solid oxide cells in parallel to the dc-dc converter in SOFC mode (charging mode) and in series in SOEC mode (discharging). In this application, the ESS and dc bus were connected at the same port of the dc-dc converter while the other port was utilized to supply auxiliary energy systems. Then, with the utilization of the series-parallel configuration a more symmetrical power-voltage characteristics for the dc-dc converter were achieved. Fig.4.17 shows the system efficiency in SOFC mode (parallel configuration) and SOEC mode (series configuration). More information can be found in App.I.

4.2.4 Series connected PCS with DAB converter for high voltage gain

In applications where a high voltage gain from V_1 to V_2 is required, magnetically coupled topologies might be required. In this case, the transformer is not used for galvanic isolation, but to achieve high voltage gain conversion. A DAB converter was used to verify the operation of the S-PCS with a low voltage RFC system as illustrated in Fig.4.18. Fig.4.19 shows a picture of the test site. The RFC from the test site featured



(a) Charging mode **(b)** Discharging mode

Figure 4.17: Efficiency measurements of the dynamic conversion system in SOFC and SOEC mode.

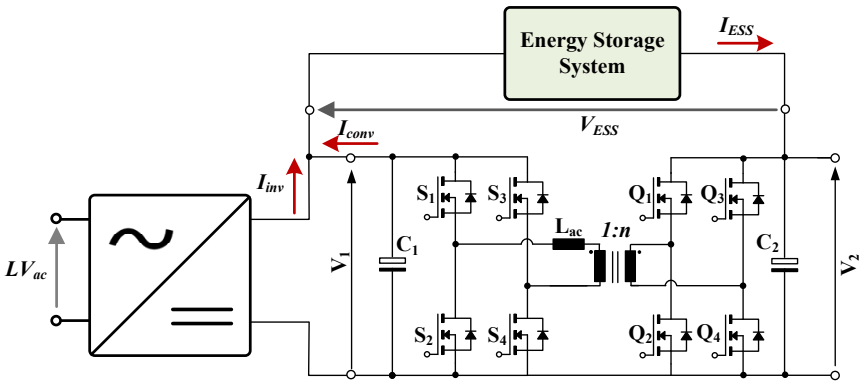


Figure 4.18: Schematic of the S-PCS with a DAB converter.

the I-V characteristics shown in Fig.4.20.

The DAB was designed to operate in close-loop with constant charge/discharge current control. Because of the low voltage characteristics of the available RFC, the dc bus was scaled down to 22 V according to the design considerations previously discussed. Fig.4.21 shows the experimental verification in charging and discharging operation modes. Fig.4.21 illustrates the differential voltage V_2, the RFC voltage V_{ESS} and the current I_{ESS}. Tests were carried at light load, therefore the voltage V_{ESS} is close to the open circuit voltage of the RFC. In each test the current reference of the DAB was driven from 1.5 A to 3 A and viceversa.

4.2.5 Series connected PCS with an isolated boost dc-dc converter

To demonstrate the power rating reduction of the dc-dc converter through the series connected PCS, a project aside of this Ph.D. project was initiated at the Department of Electrical Engineering. The work is summarized in [117].

Authors in [117], developed an isolated boost dc-dc converter based on Silicon MOSFETs rated at 733 W with input voltage 2 V-23 V and output voltage 50 V-53 V. The converter was used to supply Alkaline Electrolyser Cells rated at 3456 W. A reduction

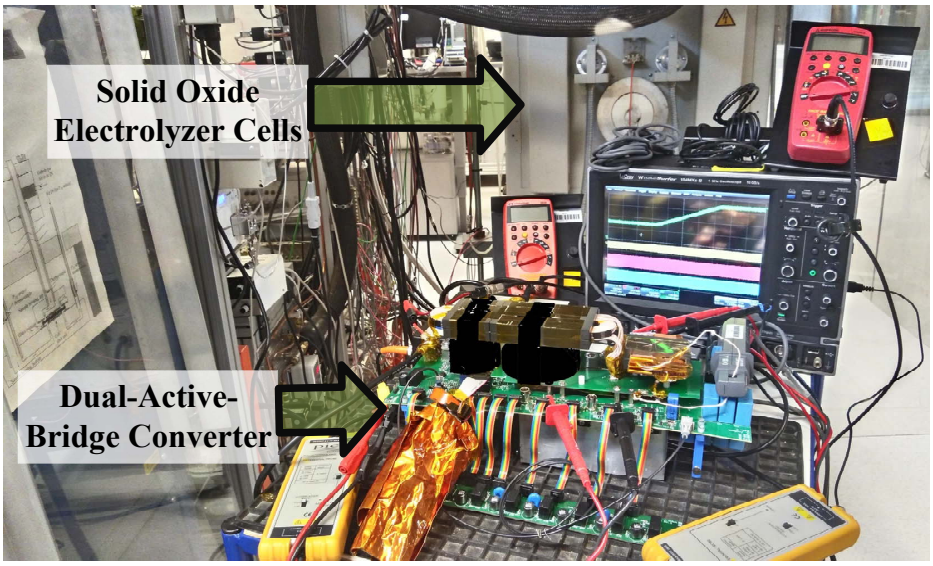


Figure 4.19: Picture of the test site.

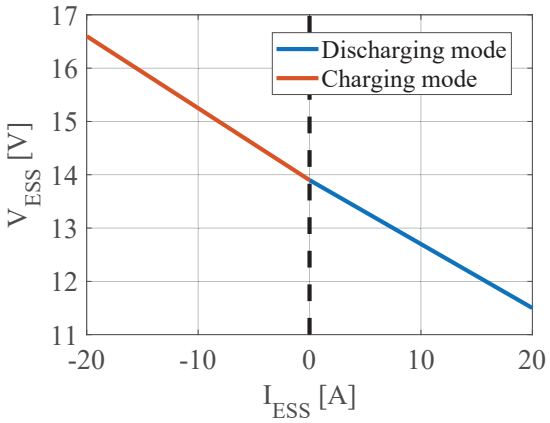
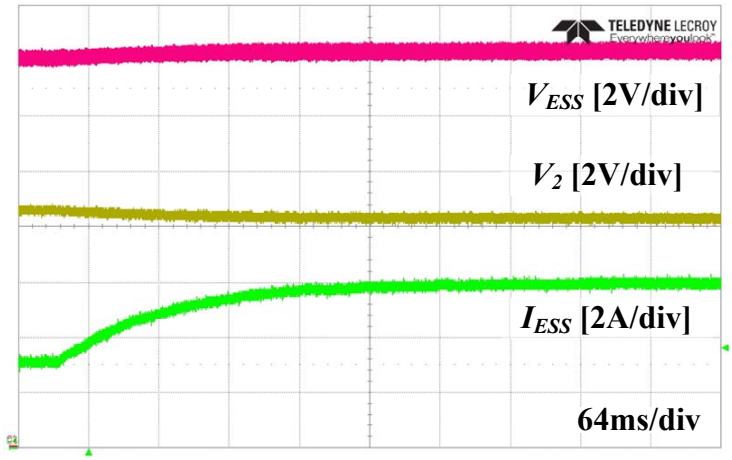
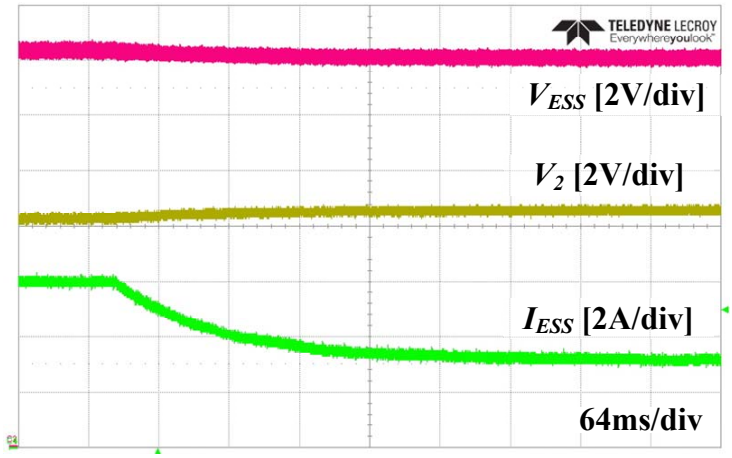


Figure 4.20: I-V characteristics of the SOEC/SOFC tested.

of nearly 80 % of the required power of the dc-dc converter was achieved, leading to an overall power density of 3.52 W cm^{-3}.



(a) Electrolyzer mode (Discharging)



(b) Fuel cell mode (Charging)

Figure 4.21: Experimental waveforms of the series-connected DAB - RFC system.

4.3 Three-port dc-dc converter for PV-Battery systems with direct energy storage

In this section a non-isolated three-port dc-dc converter topology to interconnect PV panels, an ESS and the dc bus is presented. With the proposed topology single power conversion is performed between each port, so high efficiencies can be achieved.

4.3.1 System analysis

Different power flows can take place depending on the available power from the PV panels and the power demand from the dc bus as illustrated in Fig.4.22. System specifications are given in Table 4.3.

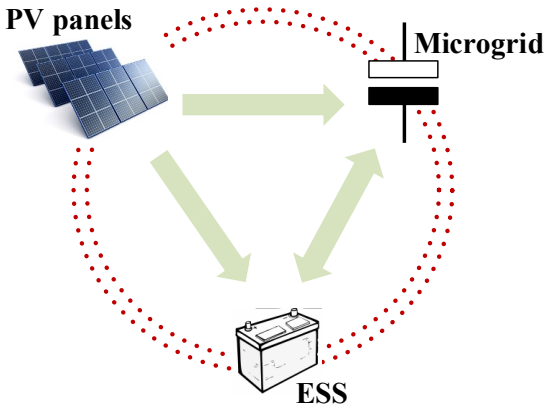


Figure 4.22: Power flow of the three-port dc-dc converter for a PV-Battery system.

Table 4.3: Specifications for the three-port dc-dc converter.

Parameter	Value
PV voltage range V_{PV}	200 V-500 V
Battery nominal voltage V_{ESS}	150 V
Dc bus voltage V_{bus}	600 V
Maximum output power (dc bus)	4 kW
Maximum PV power	4 kW
Maximum battery charge/discharge power	2.4 kW
Switching frequency	20 kHz

4.3.2 Topology and operating principle

The proposed converter is directly derived from common and well-known buck and boost topologies. In applications where high voltage gain is not required, buck and boost topologies typically feature high efficiency operation with reduced costs, due to the low number of components count. Moreover, simplicity of the topology and their well reported modelling equations, eases the design of the power control stage as well as the control system.

The schematic of the TPC dc-dc converter is presented in Fig.4.23. The converter is composed by four insulated gate bipolar transistors (IGBTs) Q_1, Q_2, Q_3 and Q_4 and three diodes D_1, D_2 and D_3. IGBTs with integrated free-wheeling diodes can be used for $Q_3 - D_2$ and $Q_4 - D_3$ to reduce costs and increase the power density. On the other hand, to improve the converter efficiency, utilization of external fast recovery or silicon carbide diodes is recommended. Only two inductors are required, L_1 for energy transfer from PV panels to the dc bus and L_2 for battery charge and discharge operation.

The equivalent circuits for each operating mode are summarized with Fig.4.24.

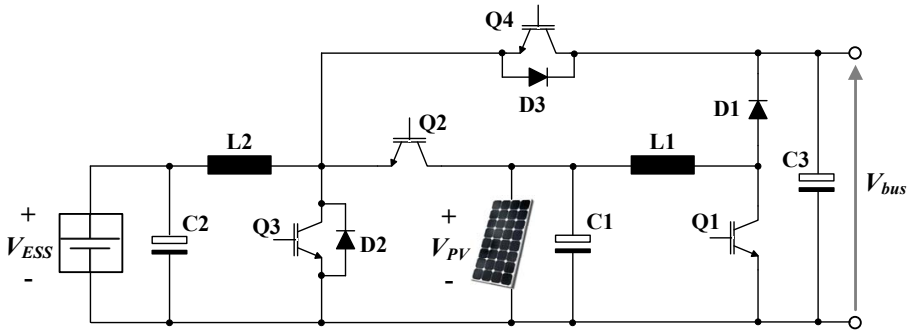
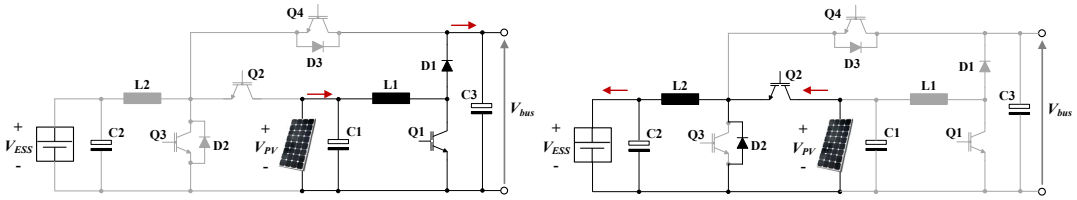
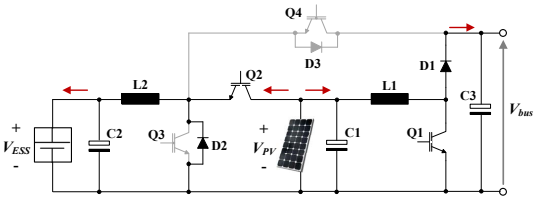


Figure 4.23: Schematic of the three-port dc-dc converter.

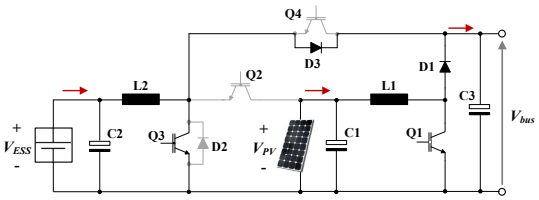


(a) PV to dc bus

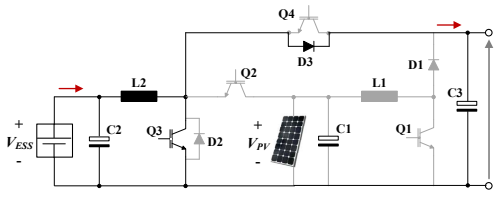
(b) PV to battery



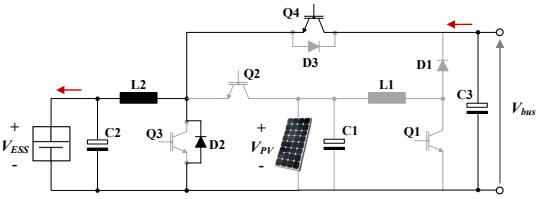
(c) PV to battery and dc bus



(d) PV and battery to dc bus



(e) Battery to dc bus



(f) Dc bus to battery

Figure 4.24: Equivalent circuits for all operating modes.

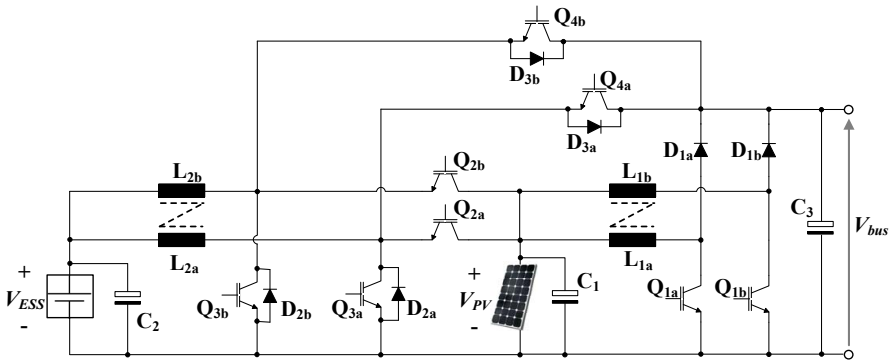


Figure 4.25: Schematic of the two stages interleaved three-port dc-dc converter.

4.3.3 Modularity by interleaving

In high-power high-current applications the conventional buck and boost converter often results in a poor efficiency performance, since the power is processed by only two power devices in hard-switching operation. Interleaving of converters is a common practice to increase the power rating and reduce the passive components' size. Moreover, other benefits can be obtained such as (1) ac current and voltage reduction, (2) reduced EMI, (3) improved efficiency by phase-shedding and (4) increased power density by the utilization of coupled magnetics. Because of the simplicity of the proposed TPC, power modularity by means of interleaving has a straight forward implementation as shown in Fig.4.25.

A two stages interleaved prototype was implemented. A picture of the prototype is given in Fig.4.26. The two stages TPC operates under the specifications given in Table 4.3. The coupled inductor is shown in Fig.4.27 were used. Due to the low switching frequency operation, the inductors were built with flat copper to reduce the dc resistance of the windings. Semiconductors D_1, D_2 and D_3 were implemented with SiC diodes to further increase the efficiency. Maximum efficiency reported was 98.7 % in PV to ESS operation mode at 500 V - 1.2 kW. More details on experimental results and efficiency measurements can be found in App.J.

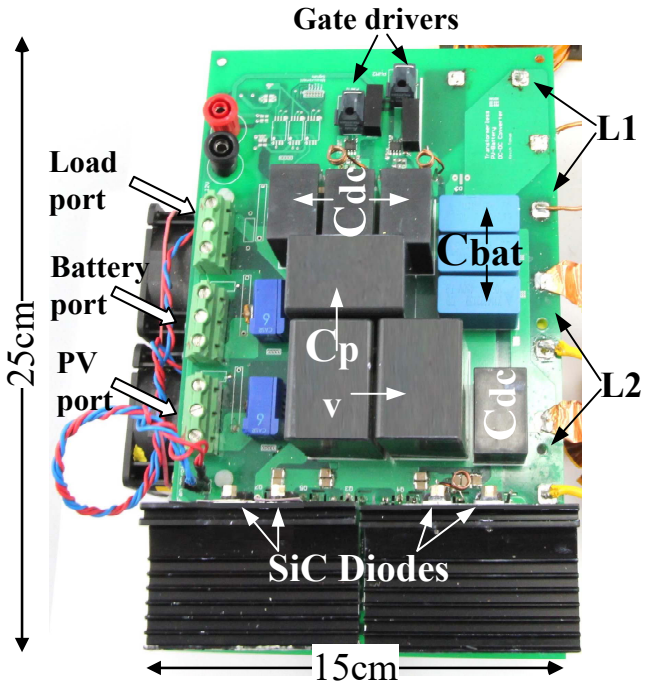


Figure 4.26: Picture of the three port dc-dc converter prototype.

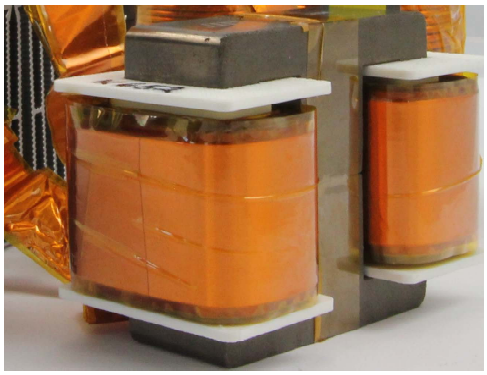


Figure 4.27: Picture of the coupled inductors.

5

Conclusion

The Ph.D. project documented in this thesis has been focused on bidirectional dc-dc power converters for the future electricity grid. The investigation carried out and presented has been divided in two major areas. Each topic has been independently covered in Chapters 3 and 4.

Chapter 2 presents the state-of-the-art and future trends on dc microgrids and the associated power converter technologies. A review of high efficiency bidirectional dc-dc converters for dc SST applications is given, wherein is concluded that the SRC is the most appropriate topology. Then, research challenges on power converters for ESSs in microgrid applications are discussed. Chapter 2 concludes with a review of bidirectional dc-dc converters for ESSs.

In Chapter 3, the multi-port SRC based dc SST has been presented as a solution to interconnect multiple dc systems. The SRC results in an interesting solution thanks to its advantages in terms of soft-switching, high efficiency and power density. In addition, the SRC offers a well-regulated output voltage for wide load ranges when operating at the resonance frequency. The inherited cross and load regulation characteristics of the SRC makes this topology suitable for open-loop operation in applications with constant dc voltages. Open-loop operation brings additional advantages into the system such as simplicity of control system and reduced number of sensors. In this regard, potential improvements in efficiency and power density, in addition to cost reductions, can be achieved. On the other hand, design considerations of a high efficiency multiport SRC in open-loop operation for dc SST applications differs from the conventional two-port SRC topology with frequency modulation.

The major design challenges are:

- to guarantee operation within the inductive region of the resonant tank in all operating modes and under any load condition,
- to support soft-switching operation under any load condition,
- to maintain the unregulated dc ports within certain voltage tolerances according to the design specifications,
- to ensure that the distributed resonant tanks are tuned at the same resonance frequency,
- and to minimize the high rms currents that typically features the SRC.

In accordance to the design challenges, a design methodology to select the resonant tank components, switching frequency and dead-time has been presented. This methodology requires different tools that have been provided along with the thesis. Some of this tools are the rms current equations considering the dead-time, the dc gain transfer functions for the two-port and three-port SRCs, the resonance frequency matching methodology and ZVS criteria. The design methodology has been evolving throughout the implementation of four experimental prototypes with different specifications and characteristics.

The results from this study are summarized as follows:

- The SRC can achieve high cross and load regulation characteristics using resonant tanks with high inductance ratios.
- Using symmetric resonant tanks simplify the design of multiport SRC due to the gain symmetry.
- The resonance frequency of the distributed resonant tanks can be tuned with the external capacitors by means of frequency matching methodology proposed.
- Resonant inductances can be integrated into the converter stray inductances. So, external resonant inductors can be avoided. This highly increases the efficiency and power density and has the potential of reducing fabrication costs. On the other hand, the distributed resonant tank becomes asymmetric, which requires of additional design efforts to fulfil the design specifications.
- With an accurate selection of the dead-time, the circulating current can be decreased leading to reduced conduction and turn-off losses. However, if the dead-time is not properly selected, the efficiency can be highly reduced, specially at light loads.
- High conversion efficiency is achieved by following the proposed design process. From a Si-based 2P-SRC 400 V/48 V prototype rated at 1 kW, a peak efficiency of 97.1 % has been obtained, while the efficiency curve remains above 95 % from 30 % to 100 % load.
- GaN devices can be used to decrease rms currents, leading to a reduction of conduction losses. In addition, when using GaN devices, the negative effect of an inadequate selection of the dead-time has a lower impact on the circulating currents, which eases the design procedure.
- High efficiency improvements are obtained with GaN and integrated resonant inductors that surpass the current state-of-the-art. Recorded peak efficiency in a 3P-SRC 600 V/400 V/80 V prototype rated at 1.5 kW is 98.8 %. Moreover, the converter efficiency remains higher than 98 % with 30 % load and above.

In Chapter 4, different power converter configurations to integrate ESS into the microgrid have been presented. The design of high efficiency power converters for ESS, such as batteries and regenerative fuel cells, is particularly challenging due to the high voltage gain and wide operating conditions. On this subject, the research contributions are summarized below:

- A DAB-derived topology, named partially paralleled DAB (P^2DAB), is proposed for high voltage gain applications. The P^2DAB topology features:
  - Reduced voltage stress at the high voltage side transformer windings and reduced high current stress at the low voltage side switching bridges.
  - Intrinsic rms current balancing among paralleled bridges at the low voltage side.
  - Improved controllability by additional phase-shift between paralleled bridges.
- A power conversion system, wherein the ESS is connected in series with a bidirectional dc-dc converter and a dc bus is proposed. By means of the series connection, the power processed by the dc-dc converter is highly reduced. Accordingly, the series-connected power conversion system features:
  - A reduction of 80 % of the required power of the dc-dc converter can be achieved, to drive an ESS with the same power rating.
  - Simplified design for high efficiency operation in wide voltage range applications. Thanks to the operating power reduction, the efficiency of the converter has a lower impact to the overall system efficiency. Through a theoretical analysis it has been concluded that, utilizing a dc-dc converter with an efficiency of 92 %, the overall system efficiency remains between 95 % to 99.5 % for an ESS with a voltage range of 360 V-570 V.
  - An interleaved boost dc-dc converter rated at 3.6 kW with an efficiency range of 93.2 %-96.9 % was used to drive Solid-Oxide Electrolyser Cells rated at 10 kW. The overall system efficiency reported, remained within a range of 98.35 %-98.85 %.
  - High power densities can also be achieved due to the reduced power rating of the dc-dc converter compared to the overall system power rating. An isolated boost dc-dc converter based on Silicon devices rated at 733 W for an input voltage of 50 V and output voltage of 2 V-20 V was built to drive a Solid-Oxide Electrolyser Cell rated at 3456 W. A power density of 3.52 W cm^{-3} was obtained.
  - Efficiency and power density results obtained with the series-connected PCS shows an improvement over the current state-of-the-art summarized in section 2.2.2.
- A three-port dc-dc converter to integrate photovoltaic modules and ESS into the mircorgrid is proposed and summarized:
  - The converter is derived from the well-know buck and boost topologies, which leads to a simple design and implementation.
  - Single conversion stages are required from each port, which leads to reduced losses. A 1.2 kW prototype was implemented with a peak efficiency of 98.7 %.
  - Modularity with improved performance can be achieved by interleaving.

6

Future work

6.1 Project proposals for the SRC dc Transformer

Robust design accounting resonant parameters variation

As mentioned at the beginning of Chapter 3, the resonance frequency is subject to changes due to factors such as components' tolerances and temperature variations. A switching frequency at $\omega_n = 0.95$ was defined as a design choice to ensure soft-switching operation of input and output ports. This optimal operating point was established empirically through experimental tests. A theoretical robust analysis that accounts for the resonant components' variations is proposed, in order to automatize and optimize the selection of the switching frequency.

Reliability assessment to select the resonant capacitors

The SRC achieve higher cross and load regulation characteristics with resonant tanks with higher inductance ratio. Ideally, the inductance ratio has no upper limit, if the stray inductances of the converter and the transformer leakage inductances are not considered. On the other hand, it has been seen that, the inductance ratio also results in a trade-off between resonant capacitor size and capacitor voltage. Assuming that the voltage gain specifications are fulfilled, one design approach is to select the inductance ratio that reduces both capacitor size and voltage stress.

Another design approach is to perform a reliability assessment of the resonant capacitors, to select the inductance ratio. The study performed in [118] could be used as a baseline of the study.

6.2 Project proposals for the Partially Paralleled DAB

Active thermal management

The proposed P2DAB converter has two degrees of freedom, the phase shift angle between low voltage side and high voltage side φ, and the phase shift angle between the low voltage side paralleled bridges φ_p. By controlling the phase angle between paralleled bridges φ_p, the real power processed by each paralleled cell can be regulated. This additional control of freedom can also be used to carry out an active thermal control of the paralleled low voltage side bridges. Active thermal management can bring advantages in terms of reliability and efficiency [69].

Control design

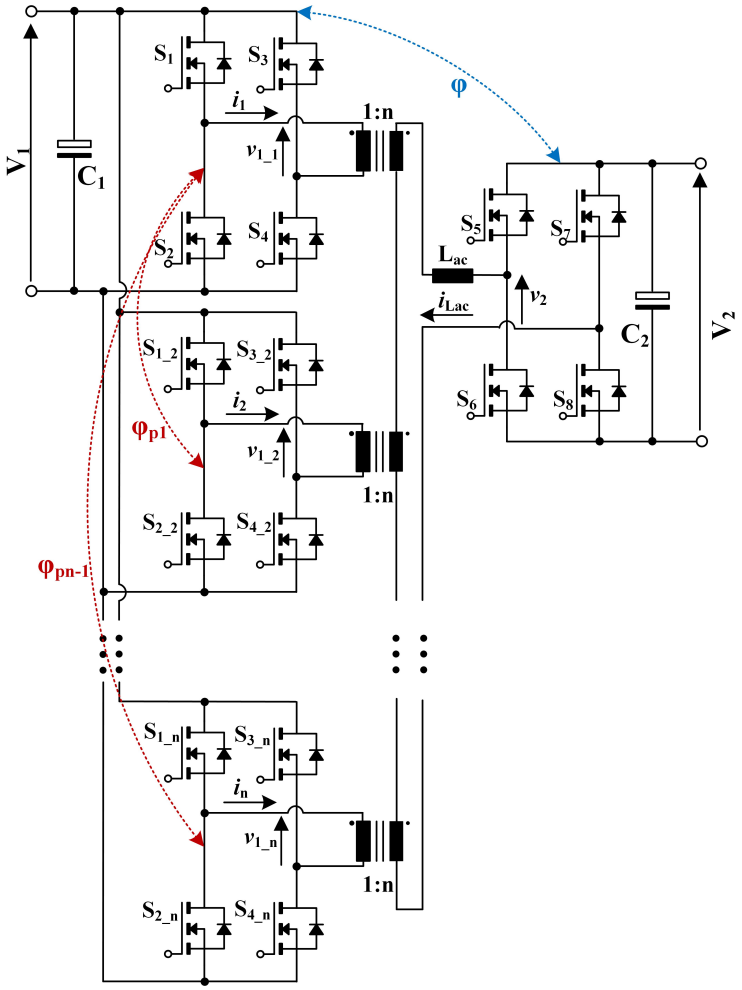


Figure 6.1: A high voltage gain DAB converter with multiple partially paralleled LV bridges.

In order to implement the controller of the P2DAB, first the mathematical model of the P2DAB should be derived. Then, an appropriate controller that provides stability to the system should be studied. Since this is a single-input single-output converter with two control variables, there are multiple combinations of φ and φ_p that lead to the same input-to-output gain. Therefore, an additional controlled parameter can be added to the system, e.g. efficiency optimization or semiconductors temperature.

Topology extension

The proposed P2DAB converter can be extended and implemented to other DAB derived topologies, such as the dual half bridge (DHB) and multi-phase active bridge converters (MHB). Furthermore, the winding connection arrangement can be extended further with multiple transformers and LVs bridges to increase the current rating as well as to obtain high voltage gain. Fig.6.1 shows an example with p paralleled branches. Accordingly, the number of additional phase shift angles φ_p is $p-1$.

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List of Publications

The overview of publications accomplished during the PhD study are given below.

1. **Kevin Tomas Manez**, Alexander Anthon and Zhe Zhang, "High Efficiency Power Converter for a Doubly-fed SOEC / SOFC System" in *IEEE Applied Power Electronics Conference and Exposition (APEC 2016)*, March 2016, pp. 1235-1242.
2. **Kevin Tomas Manez**, Alexander Anthon and Zhe Zhang, "High efficiency non-isolated three port DC-DC converter for PV-battery systems" in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia 2016)*, May 2016, pp. 1806-1812.
3. **Kevin Tomas Manez**, Zhe Zhang and Ziwei Ouyang, "Multi-port isolated LLC resonant converter for distributed energy generation with energy storage" in *IEEE Energy Conversion Congress and Exposition (ECCE 2017)*, September 2017, pp. 2219-2226.
4. **Kevin Tomas Manez**, Zhe Zhang and Ziwei Ouyang, "Unregulated series resonant converter for interlinking DC nanogrids" in *IEEE Power Electronics and Drive Systems (PEDS 2017)*, December 2017, pp. 647-654.
5. Peter Iwer Hoed Karstensen, **Kevin Tomas Manez** and Zhe Zhang, "Control of a Three-Port DC-DC Converter for Grid Connected PV-Battery Applications" in *3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG 2018)*, February 2018.
6. Yudi Xiao, Zhe Zhang, Xingkui Mao, **Kevin Tomas Manez** and Michael A.E Andersen, "Power plateau and anti-power phenomenon of dual active bridge converter with phase-shift modulation" in *IEEE Energy Conversion Congress and Exposition (ECCE 2018)*, March 2018, pp. 1871-1875.
7. Zhe Zhang, **Kevin Tomas Manez**, Yudi Xiao and Michael A.E Andersen, "High voltage gain dual active bridge converter with an extended operation range for renewable energy systems" in *IEEE Energy Conversion Congress and Exposition (ECCE 2018)*, March 2018, pp. 1865-1870.
8. **Kevin Tomas Manez** and Zhe Zhang, "Three-Port Series-Resonant Converter DC Transformer with Integrated Magnetics for High Efficiency Operation" in *IEEE Energy Conversion Congress and Exposition (ECCE 2018)*, September 2018.
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Unregulated Series Resonant Converter for Interlinking DC Nanogrids

In IEEE PEDS, Honolulu, December 12-15, 2017.

IEEE PEDS 2017, Honolulu, USA
12 – 15 December 2017

Unregulated Series Resonant Converter for Interlinking DC Nanogrids

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***Abstract*—DC nanogrids have become a subject of interest in recent years due to the increase of renewable energy sources with energy storage systems. Hybrid AC/DC systems with different DC buses are an interesting solution to efficiently supply different AC and DC loads. In this paper, a high efficiency bidirectional converter to interlink a $400\,\mathrm{V}$ DC bus with a $48\,\mathrm{V}$ DC bus is presented. The proposed converter is based on a LLC resonant converter operating as a DC transformer at a fixed frequency and duty cycle without any complex control strategy. A clear and simplified design procedure for high efficiency operation and optimal self-load regulation is presented. To verify the converter operation, a $1\,\mathrm{kW}$ prototype has been implemented, featuring on maximum efficiency of $96.7\,\%$ and a self-regulated output voltage with $3\,\%$ of maximum offset from the nominal voltage.**

I. Introduction

To date, AC electrical systems have been dominant in power systems. However, due to the increase of distributed generation systems based on renewable energy sources, there is an increasing interest towards DC nanogrids [1], [2]. DC nanogrids appear as an effective and efficient solution to integrate several types of renewable energy sources, energy storage systems and household DC loads. Currently there are no standard voltage levels defined for DC home systems. However, some studies [1] endorse the utilization of a high voltage (HV) DC bus of $400\,\mathrm{V}$ together with a low voltage (LV) DC bus of $48\,\mathrm{V}$. The $400\,\mathrm{V}$ DC bus complies with the AC grid line-to-line voltage standards and is compatible with AC appliances. The $48\,\mathrm{V}$ DC bus can interconnect within the residential area photovoltaic (PV) modules, energy storage systems and DC loads such as electronic devices and LED lighting.

As shown in Fig.1, interconnection of both DC buses is performed with interlinking power converters which require certain features, besides high efficiency and power density which are always the present key design features in power converters, for instance, bidirectional operation, to control the power direction going in and out of the nanogrid; isolation between HV and LV DC buses without utilizing low frequency transformers [1]; a system of simple construction and low maintenance [1].

Typical hard-switched isolated converters result in significant switching losses and therefore a limited efficiency. When decreasing the switching frequency switching losses decrease, but dimension of passive components increase. For that reason, an interest towards soft-switching topologies which result in a

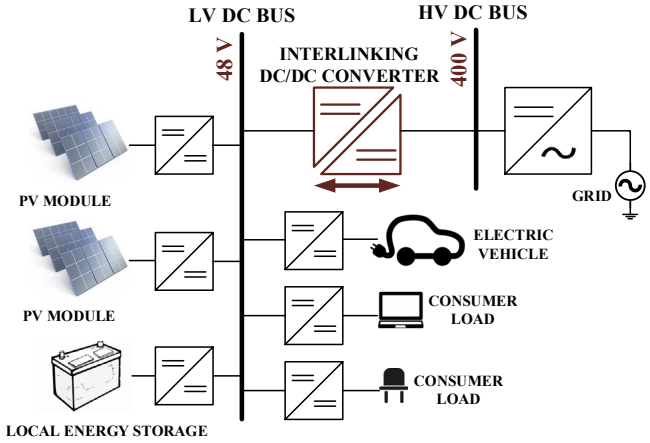

Fig. 1: DC nanogrid in future DC homes

significant reduction of switching losses has increased. Resonant converters represent an interesting solution for improved efficiency due to their inherent soft-switching characteristics.

Among the family of resonant converters, an increased interest towards the LLC resonant converters has arisen during the last years, due to their advantages [3]–[5]: (1) Zero Voltage Switching (ZVS) from light to full load range; (2) low turn-off current for the input side switches; (3) Zero Current Switching (ZCS) for the output side switches. The LLC converter is also an attractive topology for implementing unregulated DC-DC converter modules, due to its inherent load regulation characteristics when operating with a switching frequency close to the resonant frequency [4]. Furthermore, as will be analysed later in this paper, the utilization of an external resonant inductor can be avoided, using solely the leakage inductance of the transformer, which contributes to an improved efficiency and power density. In addition, highest efficiency of LLC converters is obtained when switching at the resonance frequency. Therefore, high efficiency and high power density can be accomplished. Even though the unregulated LLC converter has been addressed in a few publications [6]–[8], a clear and optimal design procedure for bidirectional operation with a distributed resonant tank has not been addressed yet.

In this paper, it is presented a bidirectional unregulated LLC converter, operating as a DC Transformer at $148\,\mathrm{kHz}$

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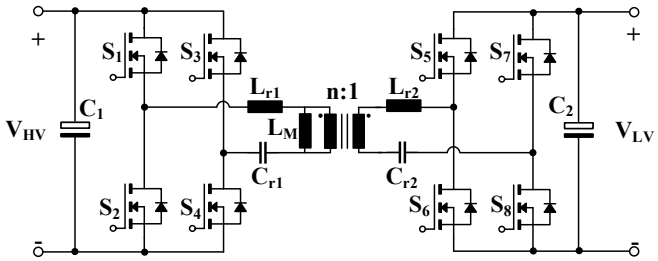


Fig. 2: Topology of the bidirectional LLC converter.

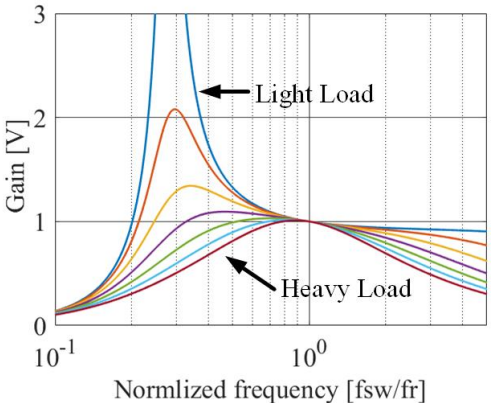


Fig. 3: Typical gain curves of a LLC resonant tank for different loads.

switching frequency and 1 kW maximum power to link the 400 V and 48 V DC buses for the future smart DC homes. A clear and simplified design procedure for optimal operation is proposed and verified with simulation and experimental results. The design methodology is optimised to reduce the input and output voltage variation from their nominal values and to assure soft-switching conditions for the entire power load with a minimum magnetizing transformer current.

II. Circuit configuration and operation principle

The proposed topology is shown in Fig.2. The power converter is based on a LLC converter with H-bridge cells. The high voltage side (HVs) refers to the 400 V DC bus and the low voltage side (LVs) refers to the 48 V DC bus. In hybrid AC/DC grids, generally, the grid-tied inverter regulates the high voltage at the HVs, as explained in [1]. Therefore the voltage on the HVs of the interlinking converter is assumed constant at 400 V in the design procedure.

As proposed in [10] and [11], because of the bidirectional power flow, the LLC resonant tank is distributed on the primary and secondary side of the transformer. In [10], the LLC converter with a distributed resonant tank is named as CLLC converter. The CLLC converter allows ZVS of primary switches and ZCS of output rectifier for the entire power load regardless the power flow direction. In addition, a symmetrical gain of the resonant tank can be achieved if the primary and secondary side resonant networks are symmetrically designed [11]. In Fig.2 the transformer is modelled with a turns ratio $n : 1$ and a magnetizing inductance L_m referred to the HVs. The resonant inductors are L_{r1} on the HVs and L_{r2} on the LVs. The resonant inductors can by composed by an external inductor in series with the leakage inductance of the transformer or only by the leakage inductance. The resonant capacitors are modelled as C_{r1} on the HVs and C_{r2} on the LVs.

One of the key aspects of the LLC transformer is that when switching at the vicinity of the series resonant frequency, the LLC resonant tank features a high inherent load regulation due to the small output impedance as verified in [4]. In Fig.3 the gain of a LLC resonant tank in terms of normalized frequency for different power levels is shown. The normalized frequency is calculated in (1). As can be seen from Fig.3, when operating at f_n, the gain of the resonant tank is kept constant to unity from light load to rated power.

As proposed in [9], the interlinking converter is intended to operate as a dc transformer. Due to the inherent load regulation characteristics of the LLC tank, the converter can operate with a fixed duty cycle of 50 % and a switching frequency for $f_n = 1$. Then, the transformer turns ratio can be selected to obtain the desired voltage gain n as shown in (2). The switches at the input port are actively switched while the output port switches are driven with a continuous low gate signal, and thus using the body diodes as a passive rectifier.

As explained in [8], the LLC converter outperforms when switching at $f_n = 1$, since ZVS of primary side switches and ZCS of the secondary side rectifiers can be ensured while the circulating current is minimized. However, in practice is not possible to keep the switching frequency at $f_n = 1$ without using any kind of close loop control, as proposed in [8], due to, for instance, parasitic components, tolerances of passive and active components, ageing and delays in the switching signals. Therefore, the optimal operating point is chosen below the resonance frequency at $0.97 < f_n < 0.99$, which still allows ZVS while keeping a low circulating current and gives some safety margin to avoid operation above the resonance frequency and thus, ensuring ZCS operation.

$$f_n = \frac{f_{sw}}{f_r} \qquad \omega_n = \frac{\omega}{\omega_r} \tag{1}$$

$$n = \frac{V_{HV}}{V_{LV}} \tag{2}$$

A. DC Gain analysis

When operating with a switching frequency of $f_n = 1$, the first harmonic approximation (FHA) can be used to derive the transfer function of the CLLC resonant tank. Fig.4 shows the AC equivalent circuit using the FHA when the LVs operates as a load. The output equivalent load, derived in [3], is modelled with R_{ac} and can be calculated in (3).

$$R_{ac} = \frac{8}{\pi^2}\frac{V_{LV}^2}{P_{out}} \qquad R'_{ac} = n^2 R_{ac} \tag{3}$$

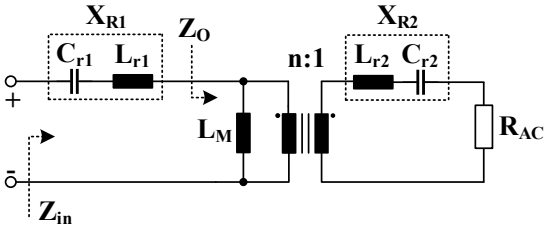


Fig. 4: AC equivalent circuit.

where P_{out} refers to the the output power and R'_{ac} refers to the equivalent ac load referred to the HVs.

The transfer function of the resonant tank can be derived from (4).

$$H_{CLLC}(j\omega) = \frac{Z_o(j\omega)}{Z_{in}(j\omega)} \frac{R'_{ac}}{X'_{R2}(j\omega) + R'_{ac}} \tag{4}$$

where $X'_{R2}(j\omega)$ refers to the reactance of the LVs resonant tank referred to the HVs, $Z_{in}(j\omega)$ and $Z_o(j\omega)$ refer to the input and output impedances of the resonant network.

$Z_{in}(j\omega)$ and $Z_o(j\omega)$ can be calculated with (5) and (6).

$$Z_{in}(j\omega) = X_{R1}(j\omega) + Z_o(j\omega) \tag{5}$$

$$Z_o(j\omega) = \left[X_{L_M}(j\omega)^{-1} + \left(X'_{R2}(j\omega) + R'_{ac} \right)^{-1} \right]^{-1} \tag{6}$$

The reactances are defined as shown in (7), (8) and (9).

$$X_{L_M}(j\omega) = j\omega L_M \tag{7}$$

$$X_{R1}(j\omega) = jZ_{r1} \left(\omega_n - \frac{1}{\omega_n} \right) \tag{8}$$

$$X'_{R2}(j\omega) = jZ'_{r2} \left(\omega_n - \frac{1}{\omega_n} \right) \tag{9}$$

where Z_{r1} refers to the characteristic impedance of the resonant tank at the HVs and Z'_{r2} refers to the characteristic impedance of the resonant tank at the LVs referred to the HVs. Z_{r1} and Z'_{r2} can be calculated with (10) and (11).

$$Z_{r1} = \sqrt{\frac{L_{r1}}{C_{r1}}} \tag{10}$$

$$Z'_{r2} = n^2 \sqrt{\frac{L_{r2}}{C_{r2}}} \tag{11}$$

Combining equations (4) to (9) the transfer function of the CLLC resonant tank is obtained and by finding the modulus the dc gain can be calculated as shown in (12).

$$|H_{CLLC}| = \frac{1}{\sqrt{Re^2 + Im^2}} \tag{12}$$

$$Re = \frac{1}{k_1} - \frac{1}{k_1 \omega_n^2} + 1 \tag{13}$$

$$Im = \frac{Z_{r1} + Z'_{r2}}{R'_{ac}} \left(\omega_n - \frac{1}{\omega_n} \right) + \frac{Z'_{r2}}{R'_{ac}} \frac{(\omega_n^4 - 1)(\omega_n^2 - 1)}{k_1 w_n^4} \tag{14}$$

where k_1 is the inductance ratio between the magnetizing inductor L_m and the HVs resonant inductor L_{r1} defined as shown in (15).

$$k_1 = \frac{L_m}{L_{r1}} \tag{15}$$

In order to obtain a symmetrical gain of the resonant tank regardless the power flow direction and magnitude, the characteristic impedances Z_{r1} and Z_{r2} have to match when referred to the same port, as shown in (16).

$$Z_{r1} = Z'_{r2} \tag{16}$$

Then, an equivalent characteristic impedance seen from the HVs can be defined (17).

$$Z_{req} = Z_{r1} + Z'_{r2} \tag{17}$$

Taking (16) and (17) into account, the expression in (12) can be further simplified to (18).

$$Im = \frac{Z_{req}}{R'_{ac}} \left(\left(\omega_n - \frac{1}{\omega_n} \right) + \frac{1}{2k_1} \frac{(\omega_n^4 - 1)(\omega_n^2 - 1)}{w_n^4} \right) \tag{18}$$

And the converter dc gain, assuming a duty cycle of $50\,\%$ and neglecting the dead time, is presented in (19).

$$H = \frac{V_{LV}}{V_{HV}} = \frac{1}{n} |H_{CLLC}| \tag{19}$$

B. ZVS condition

ZVS operation of the switches at the input port require enough current during the dead-time t_d to charge and discharge the MOSFETs output capacitance C_{oss}. During the dead-time interval, there is no power transfer from the input to the output port and the current flowing through the input port is solely circulating current. The circulating current is set by the magnetizing inductance of the transformer as given in (20).

$$I_m = \frac{V_{LV}}{4nL_m f_{sw}} \tag{20}$$

When switching at the resonance frequency $f_n = 1$, the maximum magnetizing inductance to successfully charge/discharge the MOSFETs C_{oss} can be calculated in (21) as verified in [12].

$$L_{m,max} = \frac{t_d}{8C_{coss} f_r} \tag{21}$$

From (21) it can be observed that for a given C_{oss} there are multiple combinations of L_m and t_d which result in successful ZVS operation. Larger t_d results in a larger magnetizing inductance and thus, lower circulating current (20). On the other hand, an increase of t_d can result in additional drawbacks. An increase of t_d reduces the effective duty cycle, meaning that

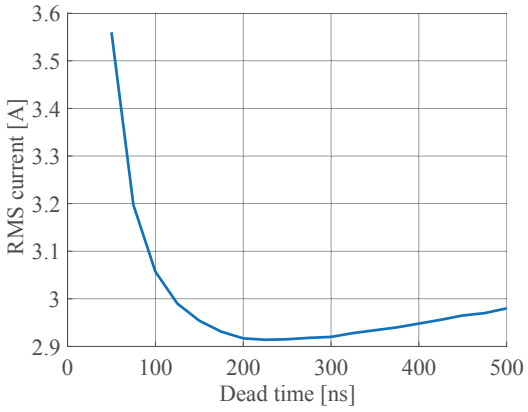


Fig. 5: Current through the HVs of the transformer versus dead time with optimal L_m for $C_{oss} = 230\,\mathrm{nF}$ at rated output power $P_{out} = 1\,\mathrm{kW}$.

the interval of time for energy transfer is smaller. Therefore, the resonant current has to increase to compensate for the duty cycle loss, which in turn causes an increase of the rms current. In addition, considering the voltage drop across the body diodes of the MOSFETs (approximately $0.9\,\mathrm{V}$ for Silicon devices and larger than $2\,\mathrm{V}$ for Silicon Carbide and Gallium Nitride devices), a longer dead time can result in higher losses during the freewheeling interval.

To quantitatively analyze the effect of the dead time, the optimal L_m for different t_d and a given C_{oss} have been calculated from (21). Then, with SPICE simulations the rms current flowing through the primary side of the transformer has been measured. Fig.5 shows the dead-time versus rms current for different combinations of L_m and t_d. It can be observed that the lowest rms current is comprised between $150\,\mathrm{ns}$-$300\,\mathrm{ns}$, and above $300\,\mathrm{ns}$ the rms current starts rising again.

C. Resonant components selection

Selection of the resonant inductors L_{r1}, L_{r2} and capacitors C_{r1} and C_{r2}, require of special attention as they will also affect the soft-switching conditions and the load regulation characteristics of the converter.

In order to ensure ZVS of the primary side switches, the resonant tank has to operate with an inductive impedance as explained in [5]. Referring to Fig.3, it can be observed that with an increasing output power the resonant tank gain decreases and the gain peak value moves towards the resonant frequency. When the slope of the gain curve becomes positive and the gain drops below unity at the switching frequency, the resonant tank impedance becomes capacitive and hence, ZVS switching operation is hindered. This results in a limitation on the power range due to the operation with fixed switching frequency. The analytical determination of the operation boundaries between capacitive and inductive impedance has already been addressed in many publications. In this paper,

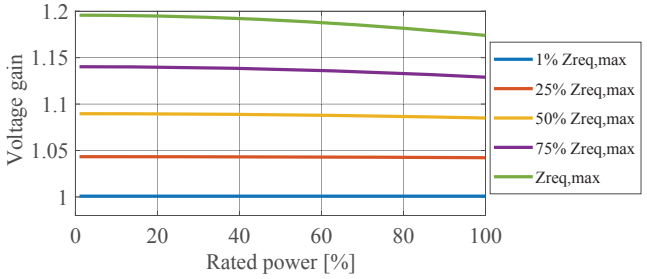


Fig. 6: CLLC resonant tank gain for different Z_{req}, a fixed L_m and $f_n = 0.97$.

the criterion derived in [5] has been utilized, which limits the output load to the inequality shown in (22).

$$R_{ac} \geq \sqrt{\frac{L_m}{C_r}} \tag{22}$$

In [9], condition (22) has been recombined and generalized for resonant converters with more than one resonant tank as shown in (23).

$$Z_{req} \leq \frac{R_{ac,min}^2}{\omega_r L_m} \tag{23}$$

where $R_{ac,min}$ is the equivalent load at the converter rated power.

Once the maximum equivalent characteristic impedance of the resonant tank is obtained, the voltage gain of the CLLC resonant tank can be analyzed by analyzed using (12) for different power ratings and the required magnetizing inductance calculated with (21). Fig.6 shows the voltage gain of the resonant tank for different values of Z_{req} below the maximum allowed in terms of rated power. As can be observed, the lowest possible characteristic impedance gives the best load regulation characteristics of the resonant tank.

Since the resonance frequency is a fixed design parameter, the characteristic impedance will define the resonant capacitor as shown in (24).

$$C_{r1} = \frac{2}{Z_{req}\omega r} \qquad C_{r2} = \frac{2n^2}{Z_{req}\omega r} \tag{24}$$

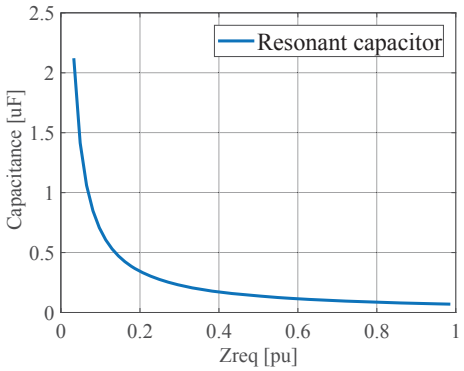
The rms voltage across the capacitor can be calculated with (25).

$$V_{cr1,rms} = \frac{I_{peak} Z_{req}}{2\sqrt{2} f_n} \tag{25}$$

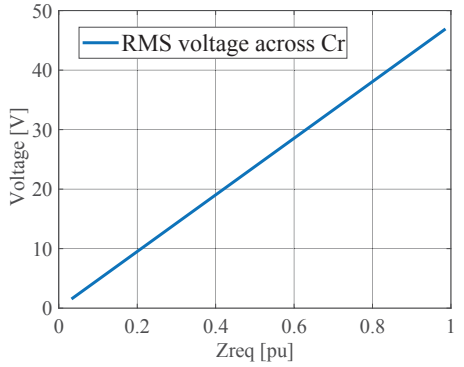
I_{peak} refers to the peak current of the resonant current flowing through the HVs, and can be approximated with (26 according to [12].

$$I_{peak} = \sqrt{\left(\frac{4V_{HV}}{\pi R'_{ac}}\right)^2 + \left(\frac{2V_{HV}}{\pi^2 f_r L_m}\right)^2} \tag{26}$$

Fig.7a and 7b show the capacitor required and the rms voltage across the capacitor for different Z_{req} in per unit,



(a)



(b)

Fig. 7: Required resonant capacitor at the HVs (a) and RMS voltage (b) in terms of the equivalent characteristic impedance in pu, where $Z_{req}[pu] = Z_{req}/Z_{reqmax}$.

being the base value the maximum allowed Z_{req}. The lower the characteristic impedance of the resonant tank, higher is the capacitor required but lower the rms voltage across it. Therefore, a low characteristic impedance will also reduce the voltage stress of the resonant capacitors. The minimum characteristic impedance is achieved when using the leakage inductance of the transformer as the resonant inductor. Then, the external resonant inductors can be avoided, reducing in that way the converter losses and increasing power density.

III. Experimental Results

A 1 kW prototype, shown in Fig.8, was realized to verify the operation of the proposed topology. The converter specifications are given in Table I and the design parameters are given in Table II. The switches used on the HVs are IPW65R420CFD (650 V, 0.49 Ω) and on the secondary side IPP034N08N5 (80 V, 3.4 mΩ).

A planar E64/10/50 core was used to built the transformer with a gap of 20 µm to obtain the required magnetizing inductance L_m. By measuring the transformer with an impedance analyzer, the leakage inductance was extracted. Then, the theoretical values for the resonant capacitors C_{r1} and C_{r2} were calculated for the desired resonance frequency and the minimum characteristic impedance of the resonant tank with

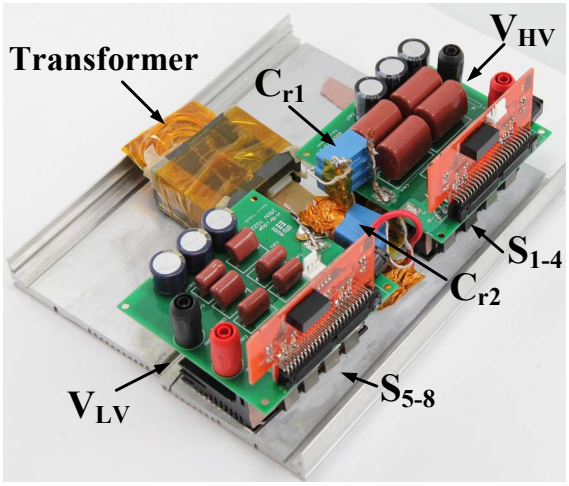


Fig. 8: Picture of the converter prototype.

TABLE I: Specifications

Parameter	Value
V_{HV}	400 V
V_{LV}	48 V
P_{max}	1 kW
f_{sw}	148 kHz

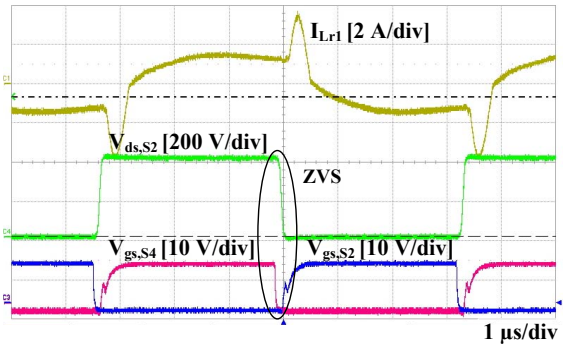
TABLE II: Design parameters and components

Parameter	Value
n	8.3
t_{dead}	175 ns
S_{1-4}	IPW65R420CFD
S_{5-8}	IPP034N08N5
L_m	440 µH
L_{r1}	5.6 µH
L_{r2}	81 nH
C_{r1}	13.8 µF
C_{r2}	200 nF

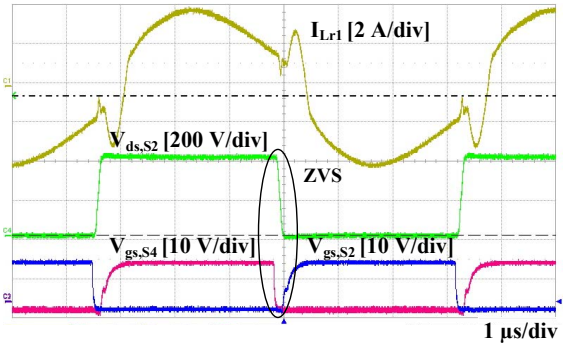
(24). However, due to the low inductance at the LVs, the parasitic inductances from the PCB traces and the MOSFET leads slightly reduced the resonance frequency of the LVs. By operating the converter at maximum load and observing the current waveforms, the resonant capacitors were adjusted to obtain a resonance frequency of 150 kHz.

A. Steady-state waveforms

The steady-state experimental waveforms under operation from HVs to LVs are shown in Fig.9 and 10. Fig.9 shows HVs waveforms at 10 % and 100 % rated power. In all cases the switches operate in ZVS, since it does not depend on the load, but on the circulating current. From Fig.9 it can also be observed the effect of the reverse recovery current of the body diode. Even though the MOSFET S_2 successfully achieves ZVS (and presumably also S_3), the reverse recovery current might still flow through the body diode of S_1 and S_4, which might introduce additional conduction losses. Therefore, for an optimal operation, MOSFETs with low reverse recovery energy body diodes should be selected. In Fig.10 the output



(a) 10 % rated load



(b) 100 % rated load

Fig. 9: HVs waveforms when power transfer occurs from HVs to LVs.

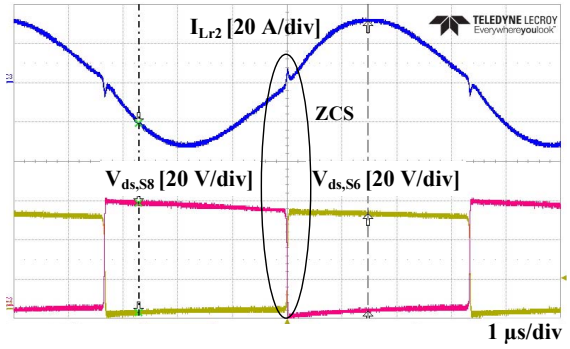
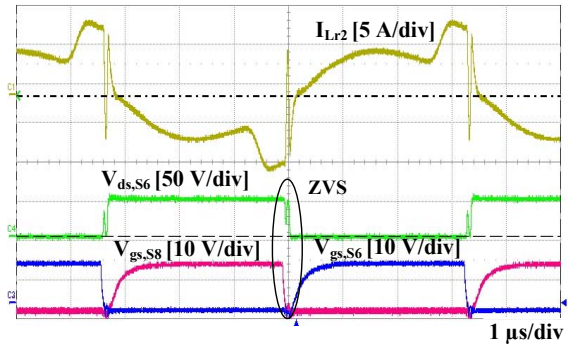


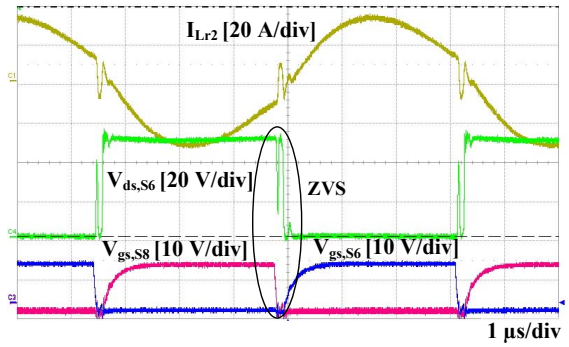
Fig. 10: LVs waveforms when power transfer occurs from HVs to LVs at 100 % rated load.

waveforms at 100 % rated power are shown. It can be observed that at full load both low side switches on the LVs can achieve ZCS.

In Fig.11 and 12 the steady state waveforms when operating from LVs to HVs are shown. In Fig.11 the ZVS operation of the LVs switches at 10 % and 100 % rated power is demonstrated. Similarly, in Fig.12 the ZCS on the LVs switches is verified. However, in this operation another phenomenon is observed. On the HVs, during the the dead time interval, the output capacitance of the MOSFETs resonate with the leakage inductance of the transformer, causing severe oscillations on



(a) 10 % rated load



(b) 100 % rated load

Fig. 11: LVs waveforms when power transfer occurs from LVs to HVs.

the current waveform. This is illustrated in Fig.12, when the current waveform approaches to zero and the drain-to-source voltage of S_2 drops to zero, the resonance begins and high frequency oscillations appear on the current waveform. This oscillations are then reflected to the LVs of the transformer, as can be seen in Fig.11. Since the amplitude of this oscillations is larger than the circulating current on the LVs, the current through the transformer changes direction during the resonance, as can be observed in Fig.11. For that reason, it can be seen in Fig.11 that $V_{ds,S6}$ starts decreasing after S_8 is turned-off, but increases again due to the change of the I_{Lr2} current direction. ZVS is still achieved, since when $V_{gs,S6}$ starts rising, S_6 is already on. However, this effect might incur in additional losses at the switches.

B. Load regulation

To evaluate the self-load regulation characteristics of the converter, the prototype was tested under both operating modes by fixing the voltage at the HVs. In the operation mode from HVs to LVs, the converter was supplied by a voltage source of 400 V and a resistive load on the LVs was used to adjust the power rating. In the operation mode from LVs to HVs an electronic load operating in constant voltage mode at 400 V was connected to the HVs and a voltage supply in constant current mode was connected to the LVs. Then, the current of the voltage supply was adjusted to control the power rating.

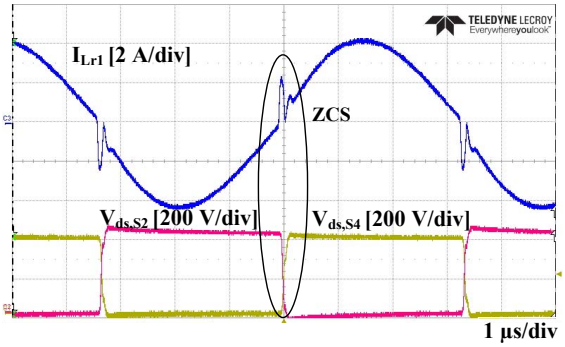


Fig. 12: HVs waveforms when power transfer occurs from LVs to HVs at 100 % rated load.

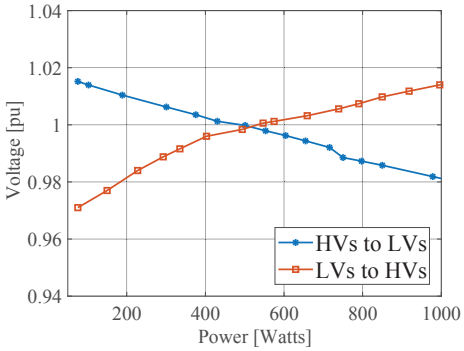


Fig. 13: Voltage regulation results.

The voltage at the LVs was measured and the results are shown in Fig.13. It can be observed that the load regulation characteristics of the converter are outstanding. The highest variation found is 3 % from the nominal value at 75 W.

C. *Efficiency*

Efficiency results are shown in Fig.14. A maximum efficiency of 96.7 % was found when the power flows from LVs to HVs at 700 W. The efficiency at light load was low, which is a common drawback of all resonant converters, due to the large circulating current set by the voltage and the transformer magnetizing inductance, instead of the output power. On the other hand, the efficiency curve remains flat and high for most of the power operating range. The efficiency when the power is transferred from LVs to HVs was almost 2 % higher than when power is transferred from HVs to LVs. This is due to the forward voltage drop of the body diode, since the output bridges operate as a passive rectifier by using the body diodes of the MOSFETs. Even though the switches selected for each bridge have different characteristics, the body diodes forward voltage show a similar behaviour. Therefore, since the LVs handles larger average current than the HVs, the conduction losses became more severe. To highly improve the efficiency, fast recovery diodes with low voltage drop could be mounted in parallel with the LVs switches.

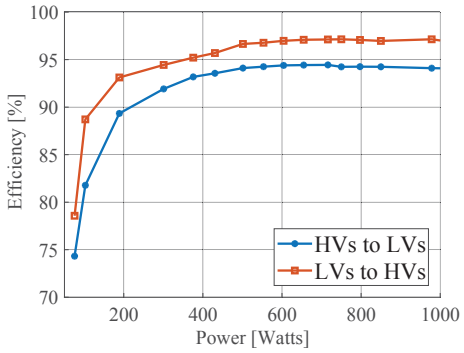


Fig. 14: Efficiency results.

IV. Conclusion

In this paper, a bidirectional series resonant converter with a CLLC resonant network for interlinking DC nanogrids has been presented. The proposed converter operates as an unregulated DC transformer with a fixed switching frequency nearby the resonance frequency and a fixed duty cycle of 50 %. The converter has been designed to interlink the 400 V DC grid with a 48 V LV DC grid for household applications, even though it can also be applied to other DC bus voltage levels, such as 12 V DC bus. The design methodology has been proposed and it has been concluded that for an optimal self-load regulation of the converter, the characteristic impedance of the resonant tank should be minimized. Therefore, to achieve the minimum characteristic impedance, the CLLC resonant network was implemented using the leakage inductance of the transformer together with external capacitors. The resonant tanks at each side of the transformer were selected to match the same resonance frequency. Furthermore, by designing the CLLC tank for the lowest characteristic impedance, the voltage stress across the resonant capacitor was also minimized.

The interlinking converter operation was tested with a 1 kW prototype. From the experimental results, soft-switching operation from light load to heavy load was verified. However, it was observed that MOSFETs selection is crucial for an optimal operation of the converter. High reverse recovery energy of the MOSFETs' body diode and a high MOSFETs' output capacitance can hinder soft-switching. By measuring the voltage variation at the LVs port while fixing the HVs port voltage, the self-load regulation characteristics of the converter was analyzed. Results showed a maximum voltage variation of 3 % from the nominal value when sweeping the output power until the rated power of the converter. Finally, a maximum efficiency of 96.7 % was reported when power transfer occurs from LVs to HVs.

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Multi-port Isolated LLC Resonant Converter for Distributed Energy Generation with Energy Storage

In IEEE ECCE, Cincinnati, October 1-5, 2017.

Multi-Port Isolated LLC Resonant Converter for Distributed Energy Generation with Energy Storage

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***Abstract*—Distributed energy generation systems with energy storage and microgrids have attracted increasing research interest in recent years. Therefore, multi-ports dc-dc converters have gained more interest. However, when integrating into multiple port converters, the power flow control and ports regulation increase in complexity. In this paper, an isolated multi-port bidirectional converter based on an LLC converter is presented. The converter operates as a dc transformer at a fixed switching frequency and duty cycle without any control loop. The resonant tanks are designed to ensure soft-switching for the whole power range and minimize the voltage variation of the unregulated ports. In order to verify the converter operation, a $1\,\mathrm{kW}$ prototype with a $600\,\mathrm{V}$ maximum voltage has been implemented.**

I. Introduction

The future of the electricity grid is moving towards distributed energy generation systems (DGS) and microgrids. The large increase of distributed energy sources, mostly household photovoltaic (PV) systems, has allowed the small consumer to also become an electricity producer. However, the continuously growing number of small decentralized energy sources results in additional drawbacks for the grid quality due to the discontinuity of renewable energy sources. Utilization of local energy storage (LES) systems can support the electricity grid by balancing the energy production and demand. Distributed energy generation systems with LES in microgrid systems comprise a combination of different sources and loads. A typical example of such combinations can include a DGS, such as independent PV arrays; an energy storage system, such as standalone batteries and electrical vehicles; and the household load together with the electricity grid, which can operate as a source or a load.

Multi-port power converters are usually a solution to integrate multiple energy sources and loads providing the advantages of low components count, high power density and high efficiency. However, the complexity of these systems is high in terms of control and regulation of the power flow direction and magnitude. Furthermore, this complexity increases when considering the additional control features required for some sources and loads, such as maximum power point tracking (MPPT) for PV panels or charging and discharging power of batteries. Therefore, in such systems, flexibility and simplicity of multiple sources and loads interconnection should be considered a key design parameter.

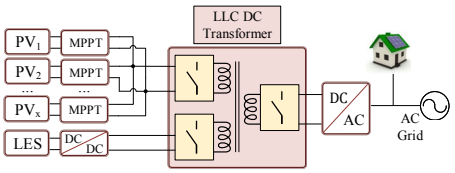

Fig. 1. Multi-port DC Transformer.

For systems with galvanic isolation an increased interest towards resonant converters has arisen, due to their advantages in reduced switching losses for wide power ranges. Resonant converters are composed by a switching bridge generating a voltage pulse which excites a resonant tank, creating a sinusoidal current at the primary side circuit. This sinusoidal current is transferred and scaled to the secondary side rectifier bridge and filtered by the output capacitance. Therefore, due to the sinusoidal current, the switches may achieve Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS).

Up to date, investigations related to soft-switched multi-port power converters to integrate DGS with energy storage and grid-connected inverters can be found. Authors in [1] and [2] presented three-port converters (TPC) derived from the Dual-Active Bridge (DAB), where each port is controlled throughout phase-shift modulation and duty cycle control is employed to extend the ZVS operating range. In [3] authors proposed a four-port quad-active-bridge (QAB) also derived from the DAB, where each port is controled with phase-shift modulation. However, the DAB topology present some limitations on soft-switching operation for the entire power range. In this regard, the LLC resonant converter presents some advantages since it allows soft-switching operation from light-load to heavy load. Authors in [4] and [5] presented an isolated TPC with two LLC resonant tanks. Phase-shift between each port is used to control power flow while soft-switching operation is obtained in all switches for wide power ranges. Authors in [6] and [7] proposed different topologies derived from the LLC converter, where up to two renewable energy sources and an energy storage system are connected to the same port while the load remains at the secondary side. Such topologies allow ZVS as well as a reduced components count.

All the solutions cited above present some drawbacks in

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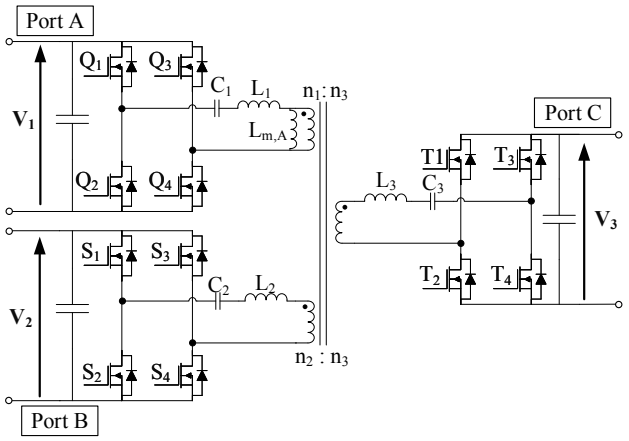


Fig. 2. Topology of the multi-port LLC converter.

terms of modularity, since they do not allow the interconnection of more sources and loads with independent control. Authors in [8] proposed the utilization of a TPC LLC converter as a dc transformer which generates three dc buses at different voltage levels to accommodate sources and loads with different voltage ratings. Experimental results from [8] demonstrate that due to the inherent cross and load regulation of the LLC converter, the voltage variation at each port is relatively small for the entire power range. This allows the operation of the system in open-loop at a fixed switching frequency and duty cycle.

This paper proposes the utilization of a TPC operating as a dc transformer with a distributed LLC resonant tank to interconnect PV arrays with independent MPPT, an energy storage system and a grid connected inverter for household applications. As shown in Fig.1, the proposed topology eases modularity and simplicity of interconnection, since multiple sources can be connected to a single port without interfering with the operation of the dc transformer. In this paper the operating principle of the LLC as a dc transformer is analysed. A design methodology which aims to reduce the voltage variation across each port and ensure soft-switching operation in all switches for the whole power range is given.

II. Topology and operating principle

The proposed converter is shown in Fig.2. The power converter is based on a LLC topology with H-bridge cells. The converter is utilized to provide isolation between ports and setting the voltage gain from port to port. The converter is operated in open-loop at a fixed switching frequency and at $50\,\%$ duty cycle. Ports that are operating as sources are actively switched, while ports operating as load are turned off and the body diodes are used as a passive rectifier bridge. Since the bi-directionality of the converter requires certain symmetry, the resonant network is distributed among the three ports. Each resonant tank is composed by a capacitor C_r and an inductor L_r, which is the sum of an external inductor and the transformer leakage inductance.

For the proposed converter, port A is used as a unidirectional port for PV panels. Each PV string can have independent MPPT by using external dc/dc converters. Port B is a bidirectional port used for local energy storage which can be composed, for example, by a combination of batteries and supercapacitors. Each energy storage system can be independently regulated using external dc/dc converters. Using external dc-dc converters to control each source or energy storage element not only allows a simplified and decoupled control system, but also allows an optimized design for each unit and modularity (i.e. more units can be added to each port without interfering with the system performance). Finally, port C is a bidirectional port connected to the DC bus and the grid-tied inverter.

The grid-tied inverter regulates the DC bus to a suitable voltage level, usually $400\,\mathrm{V}$, therefore the voltage across port C V_3 can be considered constant. Then, due to the inherent cross and load regulation characteristics of the converter [8], the voltage across the other two ports can be self-cross and load regulated using the transformer turns ratio and the dc gain characteristics of the resonant tank.

Treating all ports as identical, three operation modes can be distinguished:

1) Single-input single-output (SISO): In this mode one of the ports is operating as a source and port B or C as a load. The remaining port is not operating. The input port is actively switched with $50\,\%$ duty cycle while the switches of the output port are turned off, therefore the output bridge operates as a passive rectifier.

2) Single-input dual-output (SIDO): In this mode the PV port (i.e. port A) operates as source and the other two ports as loads. The PV port is actively switched with $50\,\%$ duty cycle and the output ports are switched off.

3) Dual-input single-output (DISO): In this mode Port A and one of the other two ports operate as a source, while the remaining port operates as a load. The switching cells of the input ports are actively switched with $50\,\%$ duty cycle and the output bridge acts a passive rectifier. In this operation mode a special attention in the design has to be made. The switches gate signals have to be synchronized, otherwise a phase-shift might be introduced between the input ports, modifying the converter operating principle.

A. LLC converter operating principle

In Fig.3 the AC equivalent circuit for the resonant tank in SIDO operation is shown. The input voltage of a resonant tank $v_{r1}(t)$, is a square waveform at the switching frequency w_{sw} changing from $-V_1$ to V_1 due to the full-bridge topology. When operating in the vicinity of the resonance frequency, the output voltage and current of a resonant network can be well approximated using the First Harmonic Approximation (FHA) from the Fourier series as shown in (1) and (2).

$$v_{ri}(t) = \frac{4V_i}{\pi} \cdot sin(w_{sw}t - \phi_v) \tag{1}$$

$$i_{ri}(t) = \frac{\pi Ir_i}{2} \cdot sin(w_{sw}t - \phi_i) \tag{2}$$

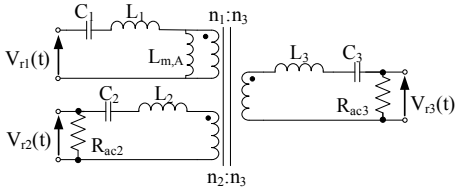


Fig. 3. AC equivalent circuit in SIDO operation.

Where $i = 2, 3$, V_i refers to the amplitude of output square wave voltage, i_{ri} refers to the fundamental component of the current at the output resonant tanks and Ir_i refers to the rms value.

Since $v_{ri}(t)$ and $i_{ri}(t)$ are in phase $\phi_v = \phi_i$, the equivalent dc load R_{ac} of the resonant network can be modelled as the ratio of instantaneous voltage and current, given by (6).

$$R_{ac} = \frac{8R_L}{\pi^2} \tag{3}$$

Where R_L is the load at the output ports.

The resonance frequency of a resonant tank composed by C_r and L_r is given in (4).

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{4}$$

Typical voltage gain curves of the resonant in terms of normalized frequency ($\omega_n = \omega_{sw}/\omega_r$) are shown in Fig.4. When the converter operates with an inductive impedance (i.e. negative gain slope at the switching frequency) [9], the current flowing through the resonant tank lags the voltage which allows ZVS turn on of the switches at the input ports. In addition, when the converter operates at $w_n \leqslant 1$, the sinusoidal output current becomes zero before the switching occurs. This allows ZCS turn off of the output rectifiers. Note that for lower switching frequency with respect to the resonance frequency, the circulating current at the input bridges increases.

As can be seen in Fig.4, when the output power increases the dc characteristic changes and the resonant tank impedance might become capacitive, being the gain slope positive at the switching frequency and thus, ZVS would be hindered. Therefore, the resonant tank has to be carefully designed in order to have an inductive impedance for the entire power load.

B. Resonant tank design considerations

In practice, the conventional LLC converter is designed to have line and load regulation throughout frequency modulation. To perform these regulations, the resonant tank should satisfy certain gain requirements given by the converter power load and voltage ratings. However, the design approach of a multi-port LLC converter operating as a dc transformer with self-cross and load regulation, differs from the conventional approach.

In this design approach the gain of the resonant tank is chosen to be close to the unity gain for the entire power range,

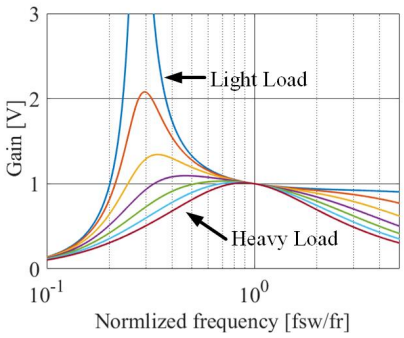


Fig. 4. Typical DC gain of a LLC resonant tank for different power ratings or Q factors.

since it is and the transformer turns ratio is selected to match the required voltage gain, as shown in (5), to obtain the desired ports voltage. Referring to Fig.4, one can observe that the unity gain of the resonant tank is found at the vicinity of the resonance frequency. Therefore, in order to ensure soft-switching operation and keep a low circulating current, the switching frequency is chosen below but close to the resonance frequency.

$$\frac{V_1}{V_2} = n_{1:2} \qquad \frac{V_1}{V_3} = n_{1:3} \tag{5}$$

Design of the resonant components such as L_i, C_i and L_m should consider maximum power load, voltage gain variation, circulating energy in the resonant tanks and soft-switching conditions. The selection of the resonant components are important for power conversion efficiency and improving the self-cross and load regulation. Inductance ratio k and quality factor Q are key design parameters of the LLC converter, since they will determine the dc gain characteristics and available power range.

The quality factor Q is determined by the resonant tank characteristic impedance Z_r and the power load as shown in (6). Q has an impact on the gain characteristics and available power range. With an increasing Q factor, dc voltage gain decreases and the gain peak value moves towards the resonant frequency. However, if the Q factor is too high, the dc gain can be decreased lower than the unity gain and the gain slope before the resonance frequency becomes positive. Then, the input impedance of the resonant tank becomes capacitive below resonance, which hinders soft-switching operation. On the other hand, if the Q factor is too low, the low characteristic impedance of the resonant tank will affect the converter efficiency due to the increased circulating current. To exemplify the effect of Q, Fig.4 shows dc gain of a resonant tank for different Q factors.

$$Q = \frac{Z_r}{R_{ac}} \tag{6}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} = \omega_r L_r = \frac{1}{\omega_r C_r} \tag{7}$$

Therefore, for a fixed switching frequency, there is a maximum quality factor Q_{max} which has to be determined to properly size the resonant tank and thus, fulfil the load requirements. Determining Q_{max} has been already addressed in many publications, in this design the k-Q criterion derived in [9] has been considered. According to the k-Q analysis, the condition given in (8) has to be fulfilled in order to ensure the operation in the inductive region.

$$R_{ac} \geqslant \sqrt{\frac{L_m}{C_{eq}}} \tag{8}$$

Where C_{eq} is the equivalent capacitance of the resonant capacitors distributed among the three different ports (i.e. C_1, C_2 and C_3).

Combining (8) with (7) the maximum equivalent characteristic impedance of the resonant tank $Z_{req,max}$ is given by (9).

$$Z_{req,max} = \frac{R_{ac,min}^2}{\omega_r L_m} \tag{9}$$

Where $R_{ac,min}$ is the equivalent load at the rated power of the converter.

Combining (9) with (7), the maximum equivalent inductance of the resonant network $L_{r,max}$ can be calculated as shown in (10).

$$L_{r,max} = \frac{R_{ac,min}^2}{\omega_r^2 L_m} \tag{10}$$

For the proposed three port LLC converter, the equivalent inductance seen from port A $L_{eq,A}$ is calculated as shown in (11).

$$L_{eq,A} = L_1 + \left(\frac{1}{n_{1:2}^2 L_2} + \frac{1}{n_{1:3}^2 L_3}\right)^{-1} \tag{11}$$

Then, from (8), the resonant tank design has to ensure (12).

$$L_{r,max} \geqslant L_{eq,A} \tag{12}$$

The other design parameter is the inductance ratio k. The inductance ratio k affects the load regulation and soft-switching conditions [9]. If k is high, the voltage gain in the vicinity of the resonance frequency is very close to the unity gain and the gain variation for different loads will be small [9]. Conversely, with low k ratios, the converter will have a poor self-cross and load regulation characteristic and the ports voltage will significantly change from their rated values. For a LLC converter with a distributed resonant tank, the k ratio is given by (13).

$$k = \frac{L_{m,A}}{L_{eq,A}} \tag{13}$$

C. Magnetizing inductance selection

To ensure ZVS of the switches at the input ports, the output capacitances of the MOSFETs have to be fully charged or discharged during the dead-time period. Therefore a minimum magnetizing current given by (14), is required [10].

$$I_m > \frac{2C_{oss}V}{t_d} \tag{14}$$

Assuming that the resonant tank operates at the unity gain, the maximum magnetizing inductance L_m required to achieve ZVS can be calculated with (15) according to [10].

$$L_m \leqslant \frac{t_d}{8C_{oss}f_{sw}} \tag{15}$$

D. Transformer design considerations

The leakage inductances of the transformer form part of the distributed resonant tank, affecting the performance of the converter. The resonance frequency of the resonant tank including the leakage inductance is shown in (16). The leakage inductance of a transformer depends on the coupling factor, which at the same time depends on the winding geometry. Depending on the operation mode in which the converter is operating (i.e. SISO, DISO or SISO) and the active or inactive ports, the coupling factor changes and thereby, also the transformer leakage inductance.

$$\omega_{r,lk} = \frac{1}{\sqrt{(L_r + L_{lk})C_r}} \tag{16}$$

According to (16), with an increasing leakage inductance, the resonance frequency of the resonance tank decreases. Therefore, if the leakage inductance is not taken into account, the converter might enter into the operation above the resonance frequency due to the fixed switching frequency. As a consequence, ZCS operation at the output rectifiers might be lost. For a given transformer, the worst-case leakage inductance or coupling factor has to be used to set the switching frequency to at least $\omega_{r,lk}$.

III. Design example

Fig.5 shows the flowchart to design the resonant network and selecting the appropriate switching frequency. Below a design example is given to illustrate the design procedure. Table I shows the specifications of the converter and table II shows the selected parameters.

To match the gain requirements the turns ratio chosen according to (5) is $n_{1-2} = 1.5$ and $n_{1-2} = 3$. For the output capacitance C_{oss} of the selected MOSFETS and a dead-time of $200\,\mathrm{ns}$, the magnetizing inductance $L_{m,A}$ is set to $560\,\mu\mathrm{H}$. Then, according to (10), the maximum equivalent resonant tank inductance referred to port A $L_{rA,max}$ which allows ZVS is found to be $170\,\mu\mathrm{H}$. The inductance ratio k is set to 6, which results in a L_{rA} lower than $L_{rA,max}$. Then, the resonant inductors L_2 and L_3 are set to $28\,\mu\mathrm{H}$ and $7\,\mu\mathrm{H}$ respectively. According to (11), the resonant inductor L_1 is calculated resulting in $62\,\mu\mathrm{H}$. Finally, the resonant capacitors of each port

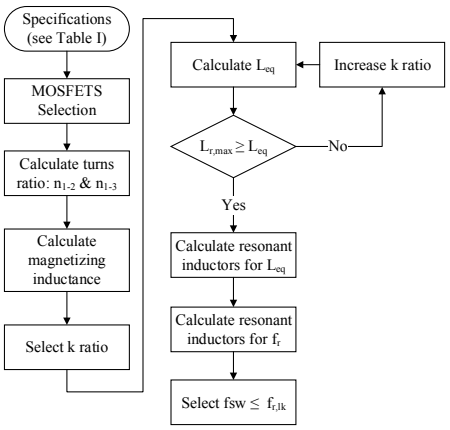


Fig. 5. Optimal design flowchart.

TABLE I
SPECIFICATIONS

Parameter	V_1	V_2	V_3	P_{max}	f_r
Value	600 V	200 V	400 V	1 kW	150 kHz

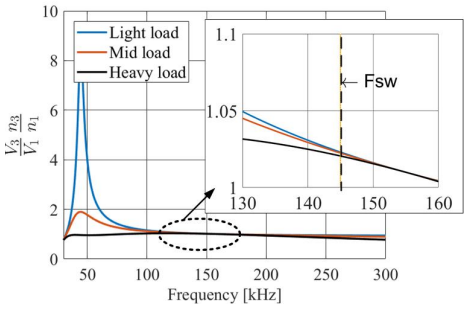
TABLE II
DESIGN PARAMETERS

Parameter	n_{1-2}	n_{1-3}	t_{dead}	C_{oss}	$L_{m,A}$
Value	3	1.5	200 ns	300 pF	560 µH
Parameter	L_1	L_2	L_3	$L_{lk1,max}$	C_1
Value	62 µH	28 µH	7 µH	2 µH	18 nF
Parameter	C_2	C_3	$f_{r,lk}$	f_{sw}	
Value	40 pF	160 pF	147 kHz	145 kHz	

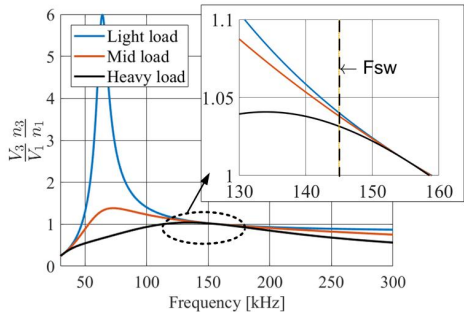
are calculated using (4) for the resonance frequency given in table I.

The transformer leakage inductance is measured under all operation modes (i.e. SISO, SIDO and DISO) using an impedance analyzer. The largest leakage inductance occurs between windings of port A and port C when port B is left opened ($L_{lk,13}$), being 2 µH. This results in a resonant frequency of approximately 147 kHz according to (16). Then, the switching frequency is set to 145 kHz to allow some margin.

In order to illustrate the effect of the inductance ratio on the converter load regulation characteristics a second design with $k = 3$ have been performed following the procedure aforementioned. Then, with the resulting parameters, the ac equivalent circuit of the converter as shown in Fig.3 has been analyzed with AC simulations using SPICE software. Fig.6 shows the dc gain obtained for both designs at heavy load, mid load and light load. In order to solely visualize the gain of the distributed resonant tank, the dc gain obtained is multiplied by the transformer turns ratio. According to the results obtained, the total voltage variation from light load to heavy load for $k = 3$ is 1.1% while with $k = 6$ is 0.03%. Therefore, with a high k ratio the load regulation characteristic of the converter is improved.



(a) k=6



(b) k=3

Fig. 6. DC gain of the distributed resonant tank for different inductance ratios.

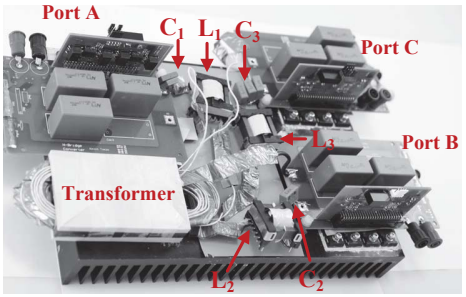


Fig. 7. Prototype of the multi-port LLC converter.

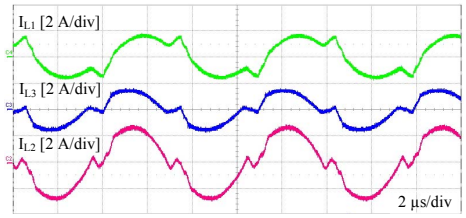
IV. EXPERIMENTAL RESULTS

The operation of the proposed converter is analysed on a prototype with the specifications given in Table I and the parameters given in Table II. Fig.7 shows a picture of the prototype.

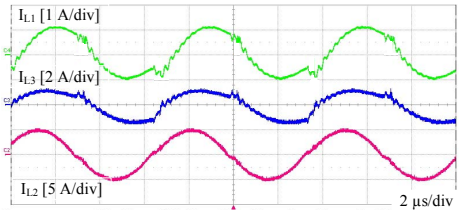
The converter has been tested under the three operation modes as follows:

1) SIDO: Port A operating as a source while ports B and C operate as loads. Voltage across port C (i.e. grid-side port) is kept constant at 400 V.

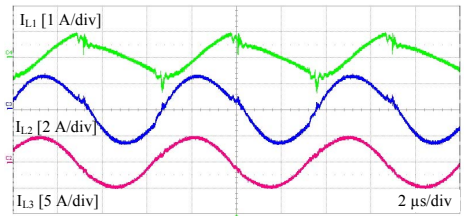
2) DISO: Ports A and C operate as source while port B operates as a load. Port C is supplied by a voltage source at a constant voltage of 400 V and port A is supplied by a voltage source in constant current operation. The output current of the voltage source is manually modified to achieve different power sharing among the input ports.



(a) SIDO

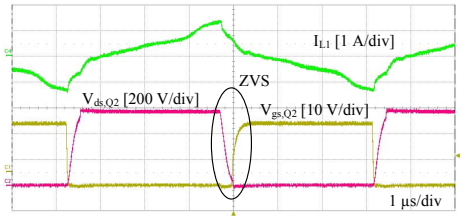


(b) DISO

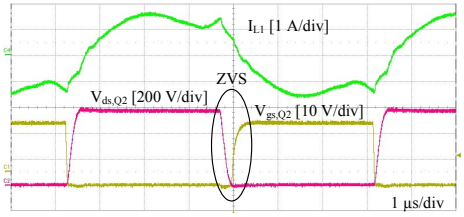


(c) SISO (Port A off)

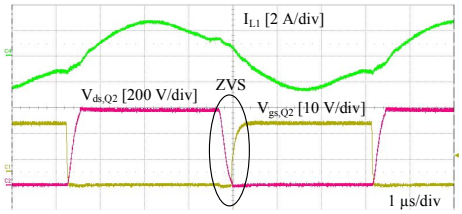
Fig. 8. Tranformer currents at 65 % rated load on different operation modes.



(a) 10 % Load



(b) 65 % Load



(c) 100 % Load

Fig. 9. ZVS waveforms of Port A under SIDO operation mode at different rated loads.

3) SISO: Port C operates as a source, port B as a load and port A remains unloaded. Port C is supplied with a voltage source at constant voltage.

A. Steady-state waveforms

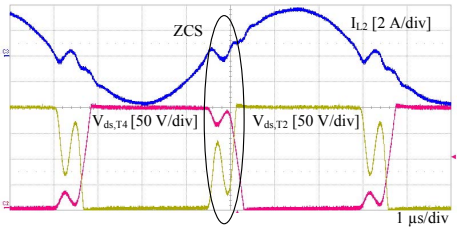
Fig.8 shows the experimental waveforms of the prototype at 65 % rated load under all operation modes. The figure illustrates the current flowing through the resonant tanks. In Fig. 8a and 8b the currents at the input and output ports are nearly sinusoidal due to the operation near the resonant frequency determined by the resonant tanks. Therefore, the resonant frequency of the distributed resonant tanks have a good match. In Fig.8c, the current through the resonant tank of port A I_{L1} looks like a triangular wave because the port is unloaded, being the only load the capacitor across V_1. The current I_{L1} is then, the magnetizing current.

Fig.9 illustrates the ZVS operation under SIDO at different power levels. This refers to the worst-case condition for ZVS operation, since port A has the larger voltage rating and the lowest circulating current. Referring to (14), one can see that to achieve ZVS operation for a given MOSFET, larger voltages and lower currents will hinder ZVS operation. Fig.9 illustrates the current flowing through the resonant tank, the drain-source voltage and the gate-source voltage of Q_2 at 10 %, 65 % and 100 % rated load. The waveforms show that in all conditions ZVS is achieved, which is not dependent on the load.

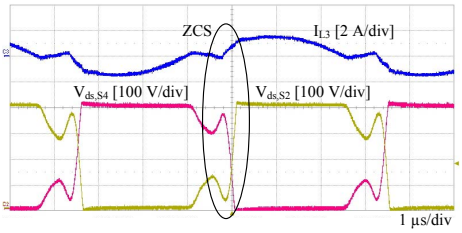
Fig.10 and 11 show the waveforms of the output bridge in SIDO and DISO operation modes at different power levels to verify the ZCS operation. Fig.10a shows the resonant tank current of port B, the drain-source voltage and gate-source voltage of S_4 while Fig.10b shows the resonant tank current of port C, the drain-source voltage and gate-source voltage of T_4. The converter is operating in SIDO mode at 65 % rated load, which is equally shared among the output ports. At medium-low power rating ZCS turn-off is successfully achieved, while the turn-on is performed at lower current due to the sinusoidal shape of the current. A high frequency ringing can be observed during the dead-time due to the resonance between the parasitic capacitances and the resonant inductor in series with the leakage inductance. Fig.11 shows the ZCS operation of port B at DISO operation at 40 % and 100 % load. This refers to the worst-case scenario to achieve ZCS, as it is the higher current port, and therefore the sinusoidal current requires of larger time to reach zero. ZCS switching, differently from ZVS, depends on the load conditions. At full load condition, shown in Fig.11b, all switches turn off with ZCS.

B. Dynamics

In order to observe the dynamics of the system, transitions between SISO and DISO operation have been analyzed by enabling and disabling port A during DISO operation. Fig.

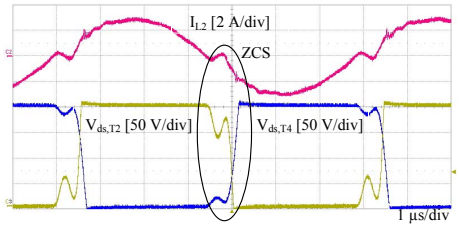


(a) Port B

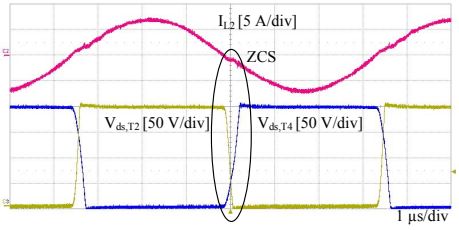


(b) Port C

Fig. 10. ZCS waveforms under SIDO operation at 65 % rated load with equal load sharing among output ports.



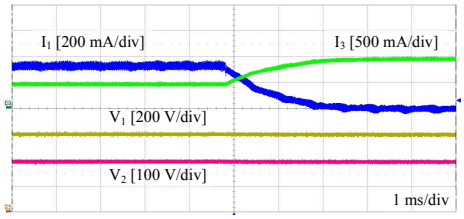
(a) 40 % rated load



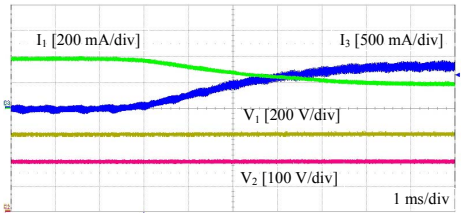
(b) Rated load

Fig. 11. Port B ZCS waveforms under DISO operation.

12a shows the transition from DISO and SISO when port A is switched off and Fig.12b shows the transition from SISO to DISO when port A is switched on. Port C operates as an input while port B as an output. Fig. 12 illustrates the currents flowing through the input of ports A (I_1) and C (I_3), and the voltage across ports A (V_1) and B (V_2). As shown in Fig.12a, when port A is shut down, I_1 gradually decreases to zero and and I_3 increases with the same rate. Voltages across the self-regulated ports V_1 and V_2 are stable during the power transition. Switching on dynamics does not differ from the switching off.



(a) DISO to SISO disconnecting Port A



(b) SISO to DISO disconnecting Port A

Fig. 12. Operation modes transition.

C. Self-cross and load regulation

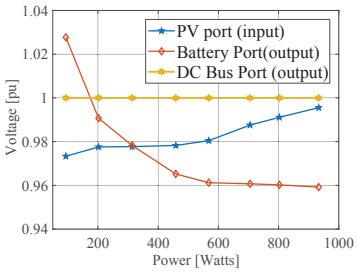
The steady state voltage regulation performance of the transformer is illustrated in Fig.13a, 13b and 13c for SIDO, DISO and SISO operation modes respectively. Fig.13 shows the voltage in p.u. values, being the base voltage the rated voltage at each port. From light load to full load, the maximum voltage variation across port A is found to be 2.5 %. The worst-case steady state regulation for port A is observed in SIDO operation, where port A is the only sourcing port. The maximum voltage variation across port B occurs in SISO operation being 5.6 %, which coincides with the worst-case scenario. In SISO, the output impedance of the converter is higher compared to the other operation modes [8], and therefore a worst steady state voltage regulation is expected.

D. Efficiency

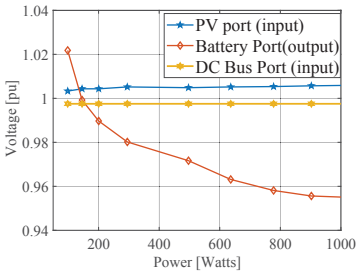
Efficiency results for all operation modes are shown in Fig.14. To obtain consistent efficiency measurements, in dual-output and dual-input modes, the power sharing between output loads and input sources respectively has been kept nearly constant at a 50 % share.

Highest efficiency is found at medium to full load in DISO operation mode, reaching a peak efficiency of 95.9 % at full load. SISO operation mode shows the worst efficiency because port A does not participate in the active power transfer, but it does in the circulating power as can be seen in Fig.8c. Therefore, even though the unloaded port does not carry active power, conduction losses at the switches and losses in the resonant tank are still present up to some extent.

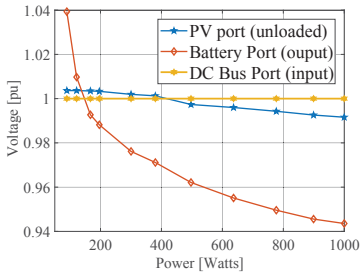
As previously mentioned, switches of the output ports are used as a passive rectifier by using the MOSFET body diodes. The switches selected for this prototype are SiC MOSFETS, which have a high voltage drop across the body diode during reverse conduction (it can be found to be approximately 2 V). This leads to increased conduction losses at the output ports. In order to highly increase the efficiency, Si MOSFETS with



(a) SIDO. Output ports with equal power sharing



(b) DISO. Inputs ports with equal power sharing



(c) SISO.

Fig. 13. Steady-state voltage regulation.

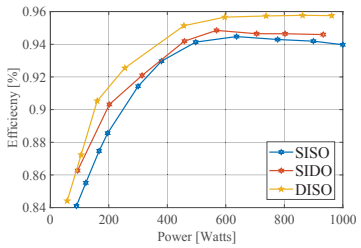


Fig. 14. Efficiency measurements.

a low voltage drop in reverse conduction might be selected or Schottky diodes in parallel with the MOSFETS can be used.

V. Conclusion

In this paper an isolated TPC LLC converter operating as a dc transformer has been presented. The converter aims to simplify the integration of multiple PV arrays with independent MPPT together with an energy storage system and a grid-connected inverter. The converter operates with open-loop, at a fixed switching frequency and duty cycle. Due to the benefits of the LLC converter in terms of self-cross and load regulation, when the voltage across one of the ports is fixed, as the DC bus connected to the grid-tied inverter, the voltage across the other ports can be adjusted with the transformer turns ratio. Due to the operation at a fixed switching frequency, ZVS at the input ports and ZCS at the output ports can be easily obtained for the entire power range. A detailed design procedure has been presented in order to ensure soft-switching operation and improve the cross and load regulation characteristics. The proposed solution has been verified on a $1\,\mathrm{kW}$ prototype. Results show that, due to the voltage regulation characteristics of the converter, voltage variation across each port can be kept relatively low. Soft-switching operation is obtained under all operating conditions and thus, achieving efficiencies up to $95.9\,\%$. Efficiency could be further improved by selecting MOSFET with low voltage drop in reverse conduction mode, in order to reduce the losses when acting as a passive rectifier.

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D

Design and Experimental Validations of a Bidirectional Three-Port Series-Resonant Solid-State Transformer

Submitted for IEEE Transactions on Power Electronics, June, 2018

Design and Experimental Validation of a Bidirectional Three-Port Series-Resonant Solid-State Transformer

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Abstract

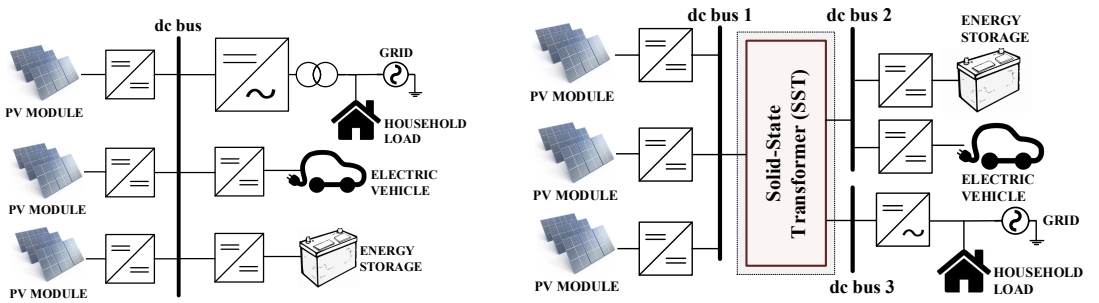
This paper proposes a three-port solid-state transformer (SST) to facilitate the integration of distributed renewable energy systems (RES) and energy storage systems (ESS) to the electrical grid. The SST consists of a three-port series-resonant converter (TP-SRC) coupled with a multi-winding transformer and a symmetrical resonant tank distributed among the three ports. Due to the inherited load regulation characteristics of the SRC, the converter operates in open-loop at a fixed switching frequency and duty cycle. The utilization of the TP-SRC as SST facilitates the interconnection of systems which require high voltage gain and enhance the flexibility and the level of integration. This paper focuses on the hardware design and experimental verification of the TP-SRC to operate in open-loop as a SST. A design methodology to successfully operate multi-port SRCs in open-loop is given. This design guarantees soft-switching operation and fixed dc gain voltage for the entire power range. In addition, a time-domain analysis is carried out to derive the root-square-mean (rms) equation of the currents at the input and output sides of the transformer taking into account the dead-time. An optimal selection of a fixed dead-time and the transformer's magnetizing inductance is performed to reduce the rms currents and thus, reduce the conduction losses. The TP-SRC is experimentally verified on a $1\,\mathrm{kW}$ prototype with $600\,\mathrm{V}/400\,\mathrm{V}/100\,\mathrm{V}$ dc ports with a maximum efficiency of $98\,\%$.

I. Introduction

Due to the increase of distributed renewable energy sources (RES), such as solar photovoltaic (PV), the development of electric vehicles (EV) and the existence of household dc loads, the electricity network is showing a tendency of moving towards hybrid ac and dc distribution. The unpredictable and uncontrollable characteristics of RES require the integration of energy storage systems (EES) which enhances the importance of dc distribution. Interconnecting all these devices with a common dc bus through active power converters, as shown in Fig.1a, has become an attractive option due to its multiple benefits when compared to the interconnection through the ac distribution system. Some of these benefits are the reduced number of conversion stages which introduces additional system power losses, and a simplifyed control system since in the dc bus there are no reactive components or issues related to the grid synchronization [1]–[3]. On the other hand, due to the nature of each system, large different

voltage levels have to be accommodated by the active power converters. For instance, to transfer power from the dc bus to the ac grid requires a voltage level within the range 380 V - 800 V depending on the number of phases; PV voltage ratings can range from low voltage levels, such as 15 V to 30 V, if sub-module integrated converters are used [4], [5], to high voltage levels, such as 800 V-1500 V, if series arrangements of PV modules are used; and ESS can also be found with very wide nominal voltage ranges depending on the technology used and the battery cells arrangement, parallel arrangement of battery voltage cells have typical nominal voltages from 12 V to 48 V [6], [7], while plug-in electric vehicles batteries or series arrangement of battery cells can reach voltage levels from 300 V to 600 V [8], [9].

During the past years numerous publications have proposed magnetically coupled multi-port power converters as a solution to interconnect with high efficiency and lower components count RES with ESS [10], [11], [13]. However, for systems where an unlimited number of RES and ESS has to be considered, these solutions are infeasible due to the lack of control variables, which are necessary to perform the different control mechanisms required by each device, e.g maximum power point tracking (MPPT) in PV systems or charge/discharge power control in ESS.



(a) with common dc bus.

(b) with multiple dc buses isolated with a solid-state transformer (SST).

Fig. 1: dc distribution system in household PV systems with energy storage.

State-of-the-art in electrical power delivery shows a tendency towards the implementation of solid-state transformers (SST) for applications such as traction, ac and dc distribution systems and microgrids [14]–[16]. SST are generally composed by two switching cells coupled with a medium- to high-frequency transformer to achieve a voltage transformation. In that way, the bulky low frequency transformer which provides isolation between the ac grid and the grid-tie inverter can be removed. In addition, with the utilization of front- and load-end active power converters, the different sources and loads integrating the system can be independently controlled [14]. The SST principle can be extended to multi-port SSTs for grid connected systems with multiple RES and ESS, as shown in Fig.1b, in order to provide solutions to the system complexities regarding high voltage gain and interconnection of multiple RES and ESS. The magnetic link between ports at the SST allows the generation of multiple dc bus to accommodate the different voltage levels with potentially high efficiency. Furthermore, the SST can provide voltage regulation and power balancing among ports, therefore each RES and ESS can be independently controlled by the front-end active converters.

Several SST topologies have been proposed in the past years for different applications. Amongst all the studies the dual-active-bridge (DAB) and the series-resonant converter (SRC) are the most popular due to their advantages of soft-switching, high power density and high efficiency [15]. The SRC has inherited load regulation characteristics when operating at the resonance region, which allows operation in open-loop, for that reason it is also named as dc transformer [15]. In contrast, the DAB requires closed-loop control, where the most commonly used is the phase-shift modulation (PSM), to regulate the voltage and the power flow.

Table I presents a summary of past studies on SST based on the DAB and SRC converter topologies. In [17] a unidirectional three-stage DAB converter in a series-input parallel-output configuration is proposed. The converter input is connected to the ac grid with an active rectifier and scales down the voltage at its output to a $200\,\mathrm{V}$ dc bus for household dc grid applications. In addition, a grid-tie inverter is connected to the dc bus for sending surplus power from the dc distribution to the ac grid. Experimental results on a $9\,\mathrm{kW}$ prototype results in a maximum efficiency of $92\,\%$. In [18] another series-input series-output multilevel DAB converter is presented. The converter is implemented as a current source with an input inductor and a switched capacitor at the input of each module, which aims at improving the soft-switching operation and the current ripple performance. In addition silicon-carbide (SiC) semiconductors are utilized to further reduce the losses. Maximum efficiency reported on a $800\,\mathrm{W}$ prototype is $96.3\,\%$. Authors in [19] propose a three-port bidirectional converter derived from the DAB with a single three-winding transformer. A dual-PSM is implemented to manage the power flow while pulse-width modulation (PWM) is utilized to reduce the system losses. Reported efficiency on a $1.5\,\mathrm{kW}$ prototype with a switching frequency of $100\,\mathrm{kHz}$ is $91.7\,\%$. In [20] the DAB is extended to a fully four-port quad-active-bridge (QAB) converter, which provides isolation between PV modules, the ESS and two dc buses to interconnect the grid-tie inverter and the dc loads. Power and voltage regulation is carried out by means of PSM between the four active bridges. Authors in [21] present a bidirectional full-bridge SRC to interconnect dc distribution systems. The SRC is implemented with a symmetrical distributed resonant tank, or symmetrical CLLC resonant tank, to achieve bidirectional power transmittion. Power flow and voltage magnitude are controlled by pulse-frequency modulation (PFM) while PWM is implemented to improve the poor controllability issues at light load conditions, which is a common drawback of the SRC. The topology in [21] is tested on a $5\,\mathrm{kW}$ prototype with a 1:1 transformer turns ratio, to interconnect two $380\,\mathrm{V}$ dc buses, which performs at a maximum efficiency of $97.8\,\%$. Authors in [22] proposed a unidirectional SiC-based SRC with a resonant tank at the primary side of the transformer. The proposed converter operates in open-loop, slightly below the resonance frequency to achieve high load regulation characteristics. An optimal design of the transformer and selection of semiconductors for high efficiency operation is presented in [22]. The topology is verified on a $10\,\mathrm{kW}$ prototype with a switching frequency of $20\,\mathrm{kHz}$ and a peak efficiency of $98.61\,\%$. Finally, in [23] a bidirectional CLLC SRC in open-loop operation is presented. The paper presents an analysis of the best design practices to achieve high load regulation characteristics. Authors in [23] compare through experimental verifications the efficiency of an asymmetrical CLLC SRC with PSM to a symmetrical CLLC in open-loop operation. Results show a maximum efficiency of $96.5\,\%$ in the first case while the efficiency increases up to $97.8\,\%$ when utilizing the open-loop methodology.

As studied in [19], [20], with the DAB, multiple active bridges can be coupled with a multi-winding transformer

TABLE I: Review of Solid State Transformers.

	DAB-based topologies				SRC-based topologies			
Study	[17]	[18]	[19]	[20]	[21]	[22]	[23]	This study
Year	2014	2018	2008	2013	2013	2016	2018	2018
Power Flow	$\Rightarrow$	$\Rightarrow$	$\Leftrightarrow$	$\Leftrightarrow$	$\Leftrightarrow$	$\Rightarrow$	$\Leftrightarrow$	$\Leftrightarrow$
No. ports (n)	2	2	3	4	2	2	2	3
Control	PSM	PSM	PSM	PSM	PFM + PWM	Open-loop	Open-loop	Open-loop
Application	ac and dc distribution	dc distribution	-	Grid integration of RES and ESS	dc distribution	dc distribution	ac and dc distribution	Grid integration of RES and ESS
Voltage rating ($V_1; ...; V_n$)	3.6 kV; 200 V	343 V, 120 V	300 V; 42 V; 14 V	48 V; 48 V; 48 V; 48 V	380 V; 380 V	700 V; 600 V	760 V; 380 V	600 V; 400 V; 100 V
Power rating	9 kW	800 W	1.5 kW	240 W	5 kW	10 kW	6 kW	1 kW
Sw. frequency	3.6 kHz	20 kHz	100 kHz	20 kHz	55 kHz-70 kHz	20 kHz	100 kHz	145 kHz
Max. efficiency	92 %	96.3 %	91.7 %	-	97.8 %	98.61 %	97.8 %	98 %

while PSM among each bridge can be utilized to control the power flow and regulate the voltage across each port. Therefore, the DAB results in an interesting topology for multi-port applications where line regulation has to be carried out by the SST. In contrast, in multi-port applications where solely load regulation is required, in other words, the dc voltage at each port is fixed, the SRC operating in open-loop results a more appropriate topology. As can be observed in Table I, the SRC operating at the vicinity of the resonance frequency outperforms in efficiency the DAB-based topologies. In addition, open-loop operation with a fixed switching frequency and duty cycle results in other benefits: (1) soft-switching operation under all operating conditions at input and output ports, (2) allows an optimal and simplified design of the magnetic components to achieve higher efficiency and power density, (3) avoids the necessity of control loops, reducing the complexity of the control circuitry from the hardware and software point of view and (4) reduction of the number of sensors. All the aforementioned benefits converge into potential improvements related to increase of efficiency, increase of power density and costs reduction.

The bidirectional TP-SRC was first proposed in [24]. The circuit topology presented in [24] has an assymterical resonant tank distributed among two out of the three ports. The converter operates at a fixed switching frequency with a centralized PSM scheme to regulate the voltage and power flow. The paper in [24], presents a time-domain analysis of the TP-SRC with PSM and verifies the theoretical analysis on a $500\,\mathrm{W}$ prototype rated at $200\,\mathrm{V}$, $50\,\mathrm{V}$ and $36\,\mathrm{V}$. An average efficiency of $91\,\%$ was reported.

Differently from [24], this paper presents a SST based on a three-port bidirectional series-resonant converter (TP-SRC) capable to interconnect, for instance, multiple RES, such as PV modules, ESS and the grid-tie inverter, as shown in Fig.1b. The TP-SRC operates in open-loop at a fixed switching frequency and duty cycle. The SRC converter generally incurs high circulating currents, which in turn causes high conduction losses. This can be exacerbated in multi-port configurations, where the circulating currents also flow through the inactive ports. In this paper a time-domain analysis of the TP-SRC is performed to accurately derive the rms currents of the resonant tank including the dead-time. In that manner, an optimal selection of the resonant components and dead-time can be

performed to reduce the rms currents and thus, reduce the conduction losses. To successfully operate in open-loop, the resonant tank impedance has to be properly selected. This has been addressed in previous publications for the two port SRC, however there are no verified design equations in the literature that covers the TP-SRC. In this paper, a design procedure to successfully operate the TP-SRC in open-loop is proposed, which is also generalised for multi-port SRC, i.e. three or more ports. In addition, because of the open-loop and bidirectionality, a gain symmetry among ports is necessary. Therefore, the design approach also covers the symmetrical gain operation. Load regulation characteristics of the SRC strongly depend on the resonant tank parameters which can be affected by factors such as temperature, components' tolerances and parasitic inductances and capacitances. The dc gain transfer functions of the TP-SRC are derived to discuss a design that can achieve high load regulation characteristics. Finally, the analysis and design approach of the TP-SRC is experimentally verified with a $1\,\mathrm{kW}$ converter prototype to interconnect three dc buses: (1) a low voltage (LV) dc bus of $100\,\mathrm{V}$, (2) a medium voltage (MV) dc bus of $400\,\mathrm{V}$ and a high voltage (HV) dc bus of $600\,\mathrm{V}$.

This paper is organized as follows. In Section II, the system that integrates the RES, ESS and the electrical grid with a SST based on the TP-SRC is presented. The required control algorithms and the TP-SRC operation are also discussed. In Section III, the TP-SRC circuit configuration and switching behaviour are analysed in detail. The main rms equations are derived from the time-domain analysis and the dc gain transfer functions are obtained from the first harmonic approximation. The design methodology is given in Section IV and the experimental verification is presented in Section V. Finally, the conclusions are given in Section VI.

II. Topology and operating principle of the grid-connected RES with ESS

The schematic of the proposed grid-connected RES with ESS is presented in Fig.2. The system contains the TP-SRC operating as a dc transformer, which has three isolated ports with constant dc voltages V_1, V_2, V_3 and bidirectional power flow capability. The household electrical grid is integrated into the system throughout a grid-tie inverter connected to V_3. The grid-tie inverter regulates the dc bus voltage V_3 to a sufficient voltage level and performs the grid synchronization control. The TP-SRC fixes V_1 and V_2 to a constant dc voltage level. The RES, such as PV panels, are integrated into the system throughout independent active front-end power converters connected between each RES and the dc bus V_1 which can perform the MPPT to each PV module independently, or any other control algorithm required by the RES. Similarly, the ESS, such as standalone batteries or EVs, can be interconnected with bidirectional active front-end power converters placed between each ESS and the dc bus V_2 which can control the charge/discharge power of each EES independently according to its needs and the energy management system requirements. Since the voltages V_1 and V_2 are constant and fixed by the dc transformer TP-SRC, a decoupled control methodology can be implemented to the front-end power converters that can enhance the functionality of the overall system, e.g. reactive power compensation and system integration and modularity.

The study presented in this paper is focused on the hardware design considerations of the TP-SRC, which operation principle is subsequently explained in more detail. The TP-SRC consists of three ports connected by a high-frequency transformer. Each port consists of a full-bridge with four power MOSFETs ($S_1 \sim S_4$, $T_1 \sim T_4$ and $Q_1 \sim Q_4$), a distributed resonant tank composed by the resonant inductors (L_{r1}, L_{r2} and L_{r3}), which are the sum

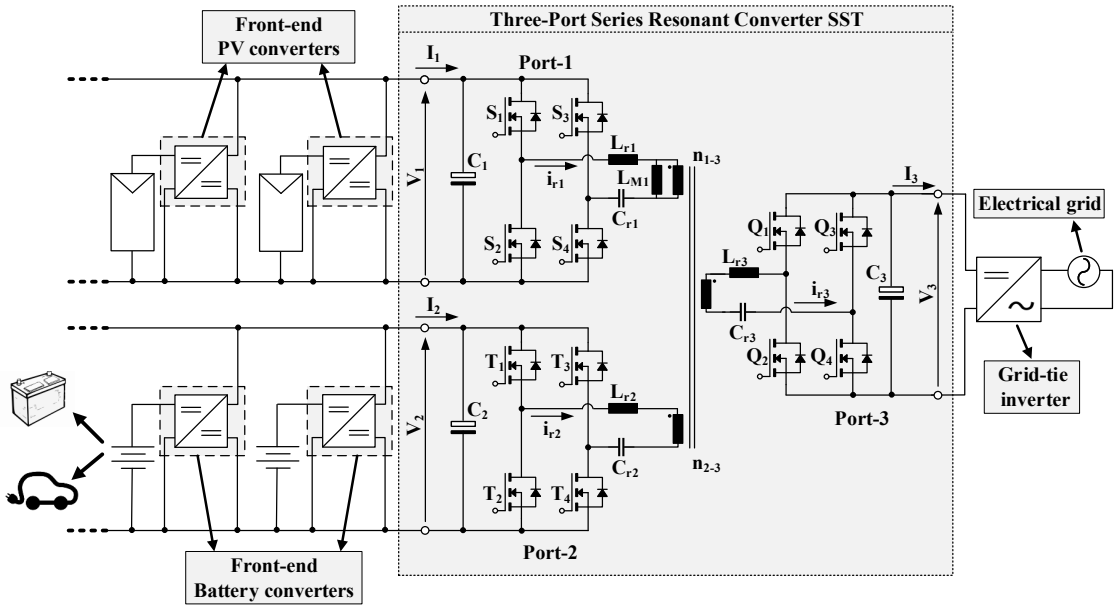


Fig. 2: Schematic of the proposed renewable energy system with energy storage with the open-loop three-port series resonant converter solid-state transformer. The grid-tie inverter carries out the dc bus voltage control and grid synchronization algorithm; the front-end PV converters carry out the MPPT algorithm at each PV panel; the front-end battery converters control the charge/discharge power of each ESS.

of the leakage inductance of the transformer and the external inductor, and the resonant capacitors (C_{r1}, C_{r2} and C_{r3}). The high frequency transformer is modelled with the magnetizing inductance L_{M1} referred to Port-1 and the turns ratio n_{1-3} from Port-1 to Port-3 and n_{2-3} from Port-2 to Port-3.

The TP-SRC is intended to operate as a SST which main functionalities are to (1) provide isolation among all ports, (2) adapt the voltage between Port-1, Port-2 and Port-3 and (3) support soft-switching in order to reduce the system losses. When switching at the vicinity of the resonance frequency, the TP-SRC has inherent cross- and load-regulation characteristics. In other words, the voltage gain of the converter remains constant from no load to full load. Due to the load-regulation characteristics, the TP-SRC has an intrinsic power balancing tendency among ports. Therefore, the TP-SRC solely behaves as a gain module or dc transformer between the three dc buses V_1, V_2 and V_3. Then, with a dedicated design methodology of the resonant tank, which will be addressed in section IV, only one of the dc bus ports has to be line regulated while the other two dc bus voltages are effectively clamped by the transformer turns ratio and the resonant tank gain, regardless magnitude and direction of the power flow. Therefore an open-loop mode of operation can be implemented.

Open-loop operation means that the TP-SRC operates at a fixed switching frequency ω and duty cycle D. Switching frequency is selected to be in the region below and in the vicinity of the resonance frequency, which is defined by the resonant inductors and capacitors. In that manner, turn-on ZVS for the MOSFETs at the input ports is ensured over the entire load range, while the turn-off event is performed at a low current defined by the

magnetizing current. In addition, MOSFETs at the output side operate with ZCS.

Input ports are actively switched with a 50% duty cycle and MOSFETs 1, 3 and 2, 4 are driven with complementary gate signals with a dead-time t_d. Synchronous rectification is used in the output MOSFETs to reduce the conduction losses. Because of the fixed switching frequency and duty cycle operation, the duty cycle at the output ports can be predefined according to the resonance frequency ω_r and no feedback loop is required to carry out the synchronous rectification.

The different operation modes of the TP-SRC are shown in Fig.3. Considering the nature of each port, i.e. RES, ESS and grid integration, the proposed converter can operate in different operating modes: in dual-input mode (DI) when the load demand is higher than the available power from the RES, i.e. Mode A, or when the energy generation is high and grid power has to be levelled down, i.e. Mode B; in dual-output mode (DO) when power generation is higher than the load power demand and the energy storage element is used to balance power production and power demand, i.e. Mode C; and in single-input single-output mode (SISO) when power flows from one of the ports to the ESS or the grid, i.e. Mode D - Mode G.

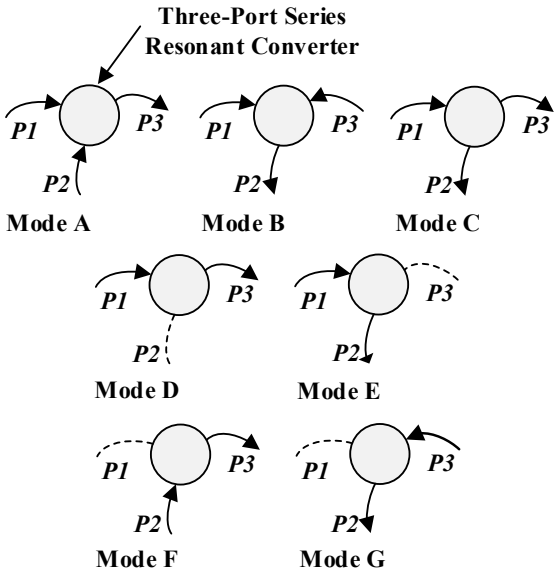


Fig. 3: Operation modes of the TP-SRC according to the power flow direction, where $P1$, $P2$ and $P3$ refer to the power transferred from or to Port-1, Port-2 and Port-3 respectively.

III. TP-SRC ANALYSIS

In this section the TP-SRC circuit is analysed. First an overview of the operating regions of the SRC converter to justify the selected operating point in the frequency domain of the open-loop TP-SRC. Subsequently a time-domain analysis is carried out to derive the rms equations of the currents flowing through the resonant tank. Finally, the dc gain transfer functions for all operating modes are derived from the First-Harmonic-Approximation (FHA).

A. SRC operating region

Fig.4a shows the ac equivalent circuit of a conventional single-input single-output SRC from which the dc gain curves can be derived. Fig.4b shows the dc gain curves in terms of normalized frequency ω_n from light load to heavy load for a $1:1$ transformer turns ratio. ω_n is given by (1).

$$\omega_n = \frac{\omega}{\omega_r} \tag{1}$$

where ω_r refers to the resonance frequency.

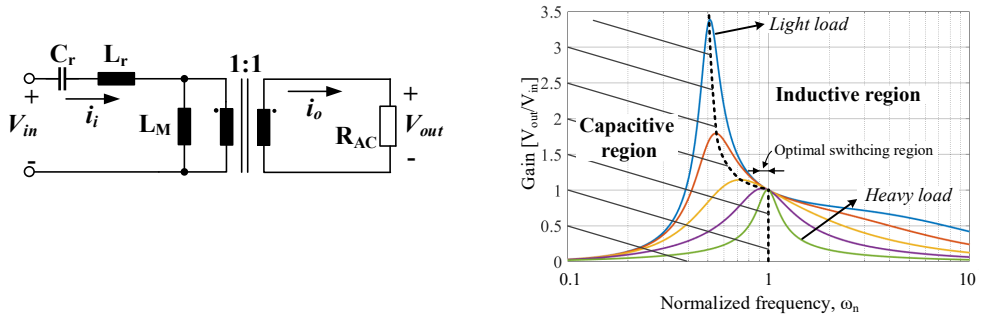
The ac equivalent load of the resonant tank R_{ac} is derived from the FHA of the output voltage and currents. Where the rms value of the fundamental components of the voltage $V_{ro,rms}$ and current $I_{ro,rms}$ at the ac equivalent load are defined with (2) and (3). Then, R_{ac} is calculated with (4).

$$V_{ro,rms} = \frac{2\sqrt{2}}{\pi} V_{out} \tag{2}$$

$$I_{ro,rms} = \frac{\pi}{2\sqrt{2}} i_o \tag{3}$$

$$R_{ac} = \frac{V_{ro,rms}}{I_{ro,rms}} = \frac{8V_{out}^2}{\pi^2 P} \tag{4}$$

where V_{out} is the voltage and and i_o the current at R_{ac} and P the power dissipated in R_{ac}.



(a) ac equivalent circuit.

(b) dc gain curves.

Fig. 4: Conventional single-input single-output SRC.

As can be seen in Fig.4b, the operating regions of the resonant tank can be divided in inductive and capacitive. The boundaries between the regions is determined by the peak of the gain curve at any load condition. Operation within the inductive region is preferred, since the resonant tank operates with an inductive impedance, i.e. a negative gain slope at the switching frequency. In this region the current is leading the voltage, which causes zero voltage switching (ZVS) of the MOSFETs at the input side.

At the vicinity of the resonance frequency $\omega_n = 1$, dc curves for any load converge at the unity gain. This means that the SRC has inherited load regulation characteristics, so it behaves as a gain block with voltage gain defined by the transformer turns ratio.

It has to be noted that, for an increasing output power the dc characteristic changes and the resonant tank impedance might become capacitive, i.e. a positive gain slope, in the vicinity of the resonant frequency and thus, hindering ZVS. This operating condition has to be avoided and will be addressed in section IV.

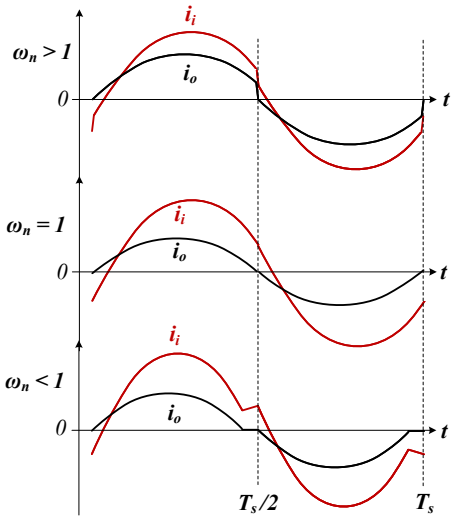


Fig. 5: Typical transformer current waveforms within the inductive region.

Fig.5 shows the resonant tank currents at the input side i_i and output side i_o of the transformer (Fig.4a) operating within the inductive region for $\omega_n > 1$, $\omega_n = 1$ and $\omega_n < 1$. When operating at $\omega_n = 1$, the resonance half cycle ends at the half switching cycle, when the resonance current at the input side i_i reaches the magnetizing current and the resonance current at the output side i_o reaches zero. Therefore, the output side semiconductors operate with zero current switching (ZCS) and power delivery from input side to output side is performed during the entire switching period if the dead-time is neglected. When operating at $\omega_n < 1$ within the inductive region, the resonance half cycle ends before the end of the half switching period when i_i reaches the magnetizing current and i_o becomes zero. At this time free-wheeling operation starts, during which only circulating current flows through the input bridge. Therefore, at $\omega_n < 1$ ZCS operation of semiconductors at the output bridge is maintained but there are additional conduction losses due to the free-wheeling period during which no power is transferred to the output side. When operating at $\omega_n > 1$, the switching half cycle ends before the resonance half cycle, so i_o does not reach zero before the commutation and thus, ZCS operation of the semiconductors at the output bridge is hindered.

According to the previous analysis, the optimal operating point in terms of efficiency is at $\omega_n = 1$, where conduction losses are minimized while ZCS operation is maintained. However, operation at $\omega_n = 1$ is not a realistic design choice in an open-loop TP-SRC, since the resonance frequency can variate due to the parasitic components, the tolerances of the resonant tank components, the operating temperature, etc. Then, the optimal operating point is selected at the vicinity but below the resonance frequency, where ZVS and ZCS is maintained while the circulating currents can still be low.

B. Operation and time-domain analysis

A time-domain analysis is carried out to extract the rms equations of the current flowing through the transformer. As an illustrative example, the analysis is performed from the DI operating mode. However, neither the operating principle nor the resulting rms equations differ with different operating modes. The steady-state waveforms and the equivalent circuit of operation in DI for a half switching period when $\omega_n < 1$ are shown in Figs. 6 and 7. For the theoretical analysis it is assumed that the converter is under steady-state operation, the capacitors C_1, C_2 and C_3 are and the MOSFETs' output capacitances are large enough to hinder any high frequency resonance.

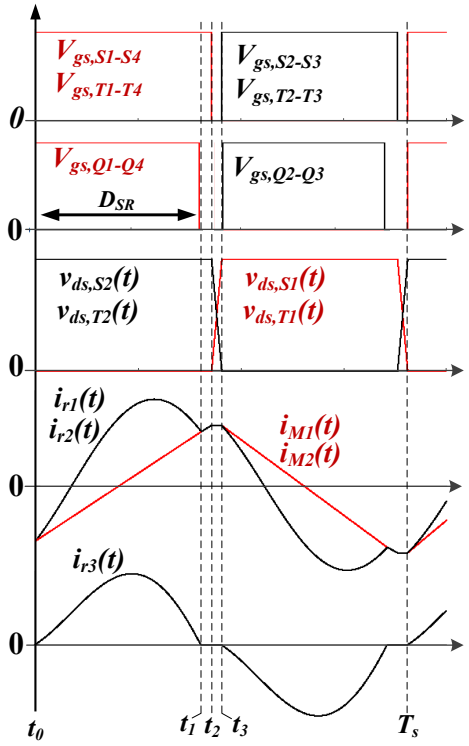
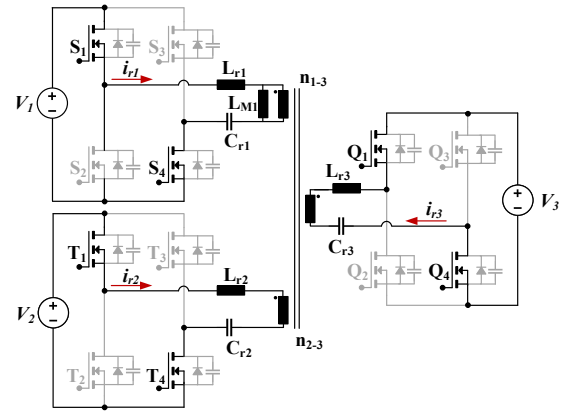


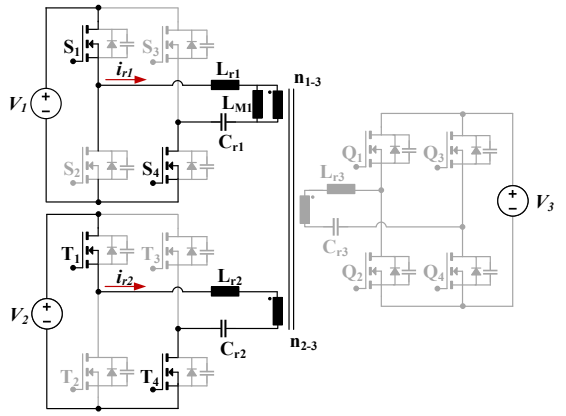
Fig. 6: Steady-state waveforms of the proposed converter operating in DI mode. V_{gs} and V_{ds} refer to the gate-source voltage of the selected switches. Switches $S1-S4$ correspond to Port-1, $T1-T4$ to Port-2 and $Q1-Q4$ to Port-3. Currents $i_{r1}(t)$ and $i_{r2}(t)$ refer to the input resonant currents of Port-1 and Port-2 respectively. Currents $i_{M1}(t)$ and $i_{M2}(t)$ refer to the magnetizing currents of Port-1 and Port-2 respectively. Current $i_{r3}(t)$ refers to the output resonant current of Port-3. In DO and SISO mode the waveforms at the output or inactive bridges correspond to the same waveforms as in Port-3 in this figure. In SISO the current flowing through the resonant tank of the inactive port is almost negligible.

Stage 1 $[t_0 < t < t_1]$:

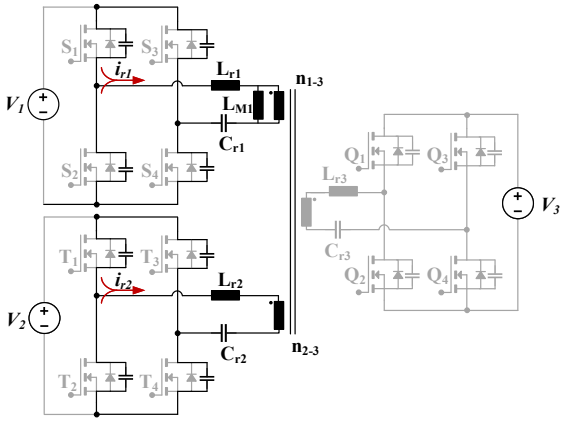
At t_0 the gate signals of S_1,S_4 and T_1,T_4 are driven high and the resonance between the resonant components $L_{r1}-C_{r1}$ and $L_{r2}-C_{r2}$ begins. Power is transferred to the output rectifying stage through the transformer. At this time the gate signals of Q_1 and Q_4 are driven high so the current through the output side switches flows through



(a)



(b)



(c)

Fig. 7: Equivalent circuits for a half switching period in DI mode for $\omega_n < 1$: (a) Stage 1, (b) Stage 2 and (c) Stage 3. V_1 refers to the voltage across Port-1, V_2 refers to the voltage across Port-2 and V_3 refers to the voltage across Port-3. In DO and SISO mode the output bridges or inactive bridges have the same operation as Port-3 in this figure.

the MOSFET instead of the body diode. The resonant currents at the input sides i_{r1}, i_{r2} change direction from negative to positive since the resonant tanks are excited with a positive voltage V_1 and V_2. At t_0 the magnetizing current equals to the resonance current. The voltage across the magnetizing inductance is the reflected output voltage $n_{1-3}V_3$ plus the ac voltage $v_{ac}(t)$ due to the resonant capacitor at the output port C_{r3}. The resonant current at the input ports $i_{ri}(t)$ and the magnetizing current i_{Mi} can be expressed with the general form given in (5) and (6). Similarly, the initial magnetizing current $i_{Mi}(t_0)$ can be approximated with the general form given in (7).

$$i_{ri}(t) = i_{ri}(t_0)\cos\omega_r t + \frac{V_i - n_{i-o}V_o - v_{ac}(t)}{Z_{ri}}\sin\omega_r t \quad \text{for } t_0 < t < t_1 \tag{5}$$

$$i_{Mi} = i_{Mi}(t_0) + \frac{1}{L_{M_i}}\left[n_{i-o}V_o t + v_{ac}(t)\right] \quad \text{for } t_0 < t < t_1 \tag{6}$$

$$i_{Mi}(t_0) = i_{ri}(t_0) = \frac{1}{4}\frac{n_{i-o}V_o(T_s - 2t_d)}{L_{Mi}} \tag{7}$$

where $i, o = 1, 2, 3$ and $i \neq o$

Stage 2 $[t_1 < t < t_2]$:

At t_1 half resonance cycle $T_r/2$ ends and currents i_{r_1}, i_{r_2} equal the magnetizing currents i_{M_1}, i_{M_2}. During this stage there is no power transferred to the output bridge and therefore, the current through the transformer at the output side i_{r_3} becomes zero. The input side switches S_1,S_4 and T_1,T_4 are still on, clamping the voltage at the resonant networks at V_1 and V_2, which forces the magnetizing currents to increase until the end of this stage. The gradient of the magnetizing current can be calculated with the voltage across the inductance at the input resonant tank as shown in the general form with (8).

$$i_{ri}(t) = i_{Mi}(t) = i_{ri}(t_1) + \frac{V_i - v_{cr_i}(t)}{L_{Mi} + L_{ri}} \quad \text{for } t_1 < t < t_2 \tag{8}$$

where $i = 1, 2, 3$, $o = 2, 3$ and $i \neq o$

For a proper operation of the open-loop synchronous rectification, the gate signals of Q_1 Q_4 have to be turned off before t_1, otherwise circulating current at the input side would be forced to circulate through the output side as well, and soft-switching operation would be hindered. Accordingly, the maximum duty cycle of the output switches is given by (9) while the maximum dead-time of the input switches is given by (10).

$$D_o = \frac{T_r}{2T_s} \tag{9}$$

$$t_{d,max} = T_s(0.5 - D_o) \tag{10}$$

Stage 3 $[t_2 < t < t_3]$:

This is the dead-time stage. At t_2 switches S_1,S_4 and T_1,T_4 are driven low. The circulating current flowing through the input bridges charge the output capacitances of S_2,S_3 and T_2,T_3, and discharge the output capacitances of S_1,S_4

and T_1,T_4. The voltage across the input of the resonant tanks softly changes polarity during stage 3. Assuming that the charging and discharging of the output capacitances is performed during the whole dead-time interval then, the average voltage at the input of the resonant tank is zero. Considering a loss-less model of the power converter, the circulating current during the dead-time interval remains constant (11). At t_3 the resonant tanks are excited with $-V_1$ and $-V_2$ and another half resonance cycle begins.

$$i_{ri}(t) = -i_{ri}(t_0) \quad \text{for } t_1 < t < t_2 \tag{11}$$

where $i = 1, 2, 3$, $o = 2, 3$ and $i \neq o$

RMS currents derivation:

Assuming that the converter operates at the resonance frequency or very close to it, the input resonant current during a half switching period considering the dead-time interval can be expressed by (12).

$$i_{ri}(t) = \begin{cases} \sqrt{2} I_{ri,rms,\omega_r} \sin(\omega_r t + \phi) & \text{for } 0 < t < T_s/2 - t_d \\ -I_{ri}(t_0) & \text{for } (T_s/2 - t_d) < t < T_s/2 \end{cases} \tag{12}$$

where I_{ri,rms,ω_r} is the rms value of the sinusoidal current at the resonance frequency and ϕ is the phase angle.

The power transfer from the transformer input side to the transformer output side is carried out during stage 1. Therefore, the output resonant current is the difference between the resonant current and the magnetizing current. In addition, the output current is the average value of the transformer current at the output side as shown in (13). The phase angle ϕ can be calculated with (14). Notice that the ac voltage due to the resonant capacitor at the output side $v_{ac}(t)$ has been neglected. As explained later in section III, for the proposed design the ac voltage across the resonant capacitor is low compared to the voltage across the transformer and it can therefore be neglected to simplify the analysis.

$$I_o = \frac{1}{T_s/2} \int_0^{\frac{T_s}{2} - td} \left(\sqrt{2} I_{ri,rms,\omega_r} \sin(\omega_r t + \phi) + i_{Mi}(t_0) - \frac{V_o}{L_{Mi}} t \right) dt = \frac{V_o^2}{P_i} \tag{13}$$

$$\phi = -\arcsin\left(\frac{\sqrt{2}}{8} \frac{V_o (T_s - 2t_d)}{L_{Mi} I_{ri,rms,\omega_r}} \right) \tag{14}$$

where P_i refers to the power transferred by port i and $i = 1, 2, 3$.

From (13) and (14), the rms value of the sinusoidal current at the resonance frequency flowing through the input side transformer can be obtained (15).

$$I_{ri,rms,\omega_r} = \frac{\sqrt{2}}{8} \frac{n V_o}{L_{Mi}} \sqrt{\frac{4\pi^2 L_{mi}^2 P_i^2}{n^4 V_o^4} \frac{T_s^2}{(T_s - 2t_d)^2} + (T_s - 2t_d)^2} \tag{15}$$

Using (7), (12) and (15) the rms current flowing through the input side of the transformer considering dead-time when $\omega_n = 1$ is calculated as follows:

$$I_{ri,rms}^2 = \frac{1}{T_s/2} \left(\int_0^{\frac{T_s}{2} - t_d} i_{ri}(t)^2 dt + \int_{\frac{T_s}{2} - t_d}^{T_s/2} i_{ri}^2(t) dt \right) \tag{16}$$

Which results in (17).

$$I_{ri,rms} = n_{i-o}^2 V_o \frac{\sqrt{2}}{8} \sqrt{\frac{(T_s - 2td)^2 (T_s + 2t_d)}{T_s L_{Mi}^2} + \frac{T_s 4\pi^2 P_i^2}{(T_s - 2t_d) n_{i-o}^4 V_o^4}} \tag{17}$$

where $i = 1, 2, 3$, $o = 2, 3$ and $i \neq o$

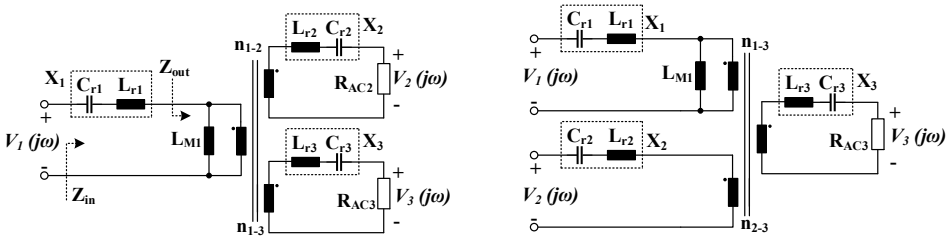
The rms current at the at the output side of the transformer can be expressed with (18).

$$I_{ro,rms} = \frac{\sqrt{2}}{4} V_o \sqrt{\frac{n_{i-o}^4}{L_{Mi}^2} \frac{(T_s - 2t_d)^3}{T_s} \frac{5\pi^2 - 48}{12\pi^2} + \pi^2 \frac{T_s}{T_s - 2t_d} \frac{P_o^2}{V_o^4}} \tag{18}$$

where P_o refers to the power at the output port.

C. Gain analysis using FHA

The DC gain analysis of the resonance network is performed by means of the FHA, where the fundamental component of the resonant tank voltage and current are considered. In Fig.8 the ac equivalent circuits of the resonant tank in DO and DI operation modes are shown.



(a) DO operation mode

(b) DI operation mode

Fig. 8: ac equivalent circuit of the TP-SRC for different operating modes.

In DO operation the dc transfer function can be derived from (19).

$$H_{oi}(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{n_{i-o}} \frac{Z_{out}(j\omega)}{Z_{in}(j\omega)} \frac{R_{aco}}{X_o(j\omega) + R_{aco}} \tag{19}$$

where $i, o = 1, 2, 3$ and $i \neq o$

The input impedance $Z_{in}(j\omega)$ and output impedance $Z_{out}(j\omega)$ of the resonant tank are calculated with (20) and (21) respectively.

$$Z_{in}(j\omega) = X_i(j\omega) + Z_{out}(j\omega) \tag{20}$$

$$Z_{out}(j\omega) = \left[X_{L_M i}(j\omega)^{-1} + n_{i-o}^{-1} \left(X_o(j\omega) + R_{aco} \right)^{-1} + n_{i-k}^{-1} \left(X_k(j\omega) + R_{ack} \right)^{-1} \right]^{-1} \tag{21}$$

where $i, o, k = 1, 2, 3$, $i \neq o \neq k$ and $i \neq k$

Combining equations (19) to (21) the dc transfer function can be obtained and by finding the modulus the dc gain can be calculated. Due to the symmetric design of the distributed resonant tank, the characteristic impedance

of the resonant components at each port are identical being $Z_{ri} = n_{i-j} Z_{rj} = n_{i-k} Z_{rk}$, if the parasitic components are neglected. Then, the dc transfer function can be simplified as shown in (22).

$$||H_{oi}(j\omega)_{DO}|| = \frac{1}{n_{i-j}} \sqrt{\frac{F^2(\omega) Q_{Lk}^2 n_{i-k}^{-4} + 1}{\left(1 + \frac{F(\omega)}{\omega_n m} - F(\omega)^2 \frac{Q_{Lk} Q_{Lo}}{n_{i-k}^2 n_{i-o}^2} \left(3 + \frac{F(\omega)}{\omega_n m}\right)\right)^2 + F(\omega)^2 \left(\frac{Q_{Lk}}{n_{i-k}} + \frac{Q_{Lo}}{n_{i-o}}\right)^2 \left(\frac{F(\omega)}{\omega_n m} + 2\right)^2}} \tag{22}$$

where $i, j, o = 1, 2, 3 \quad i \neq o \neq k \quad i \neq k$; Q_{Lo} and Q_{Lk} refer to the loaded quality factors in (23) and (24), m is the inductance ratio between the magnetizing inductor and the resonant inductor as shown in (26) and $F(\omega)$ is the expression given by (27).

$$Q_{Lo} = \frac{Z_{ri}}{R_{aco}} \tag{23}$$

$$Q_{Lk} = \frac{Z_{ri}}{R_{ack}} \tag{24}$$

$$Z_{ri} = \sqrt{\frac{L_{ri}}{C_{ri}}} \tag{25}$$

$$m = \frac{L_{M1}}{L_{r1}} = \frac{L_{M1}}{n_{1-2}^2 L_{r2}} = \frac{L_{M1}}{n_{1-3}^2 L_{r3}} \tag{26}$$

$$F(\omega) = \omega_n - \frac{1}{\omega_n} \tag{27}$$

It should be noted that the gain analysis in SISO mode can be carried out from (22), by equating to infinity the ac resistance of the unloaded port.

The transfer function in DI operation mode is derived by means of superposition and is expressed as function of $V_i(j\omega)$ and $V_k(j\omega)$ as shown in (28). Similarly as before, assuming a symmetrical design of the resonant tank, the dc transfer function can be expressed as shown in (29).

$$V_o = ||H_{oi}(j\omega)_{DI}||V_i + ||H_{ok}(j\omega)_{DI}||V_k \tag{28}$$

$$||H_{oi}(j\omega)_{DI}|| = \frac{1}{n_{i-o}} \frac{1}{\sqrt{\frac{F^2(\omega) Q_{Lo}^2}{n_{i-o}^4} \left(\frac{F(\omega)}{m\omega_n} + 3\right)^2 + \left(\frac{F(\omega)}{m\omega_n} + 2\right)^2}} \tag{29}$$

where $i, o, k = 1, 2, 3 \quad i \neq o \neq k \quad i \neq k$

IV. Design methodology

In this section the design methodology of the resonant tank components is addressed. The conventional SRC is generally designed to carry out line and load regulation throughout frequency modulation. To successfully perform this regulation, the components of the resonant tank, i.e. L_r, C_r and L_M, are chosen to meet certain voltage gain range and power range requirements. However, the design approach for an open-loop TP-SRC with high inherited cross and load regulation characteristics differs from the conventional approach. The resonant tank is designed to meet the following three main requirements:

- Minimum circulating energy that provides ZVS operation.
- Operate with an inductive impedance at any operating condition.
- Resonant tank with a constant and symmetrical dc gain at any operating condition.

A. Magnetizing inductance selection

To ensure ZVS operation of the switches at the input ports, the circulating current during the dead-time, i.e. stage 3 in Fig.7c, must be large enough to charge and discharge the output capacitances of the MOSFETs. The magnetizing current at the beginning of the dead-time can be calculated with (7). The ZVS analysis proposed and verified in [30], defines the required current I_{zvs} to charge and discharge the MOSFETs output capacitances with (30).

$$I_{zvs} > \frac{2C_{oss}V_{ds}}{t_d} \tag{30}$$

where C_{oss} is the output capacitance of the MOSFET and V_{ds} the drain-source voltage.

For a resonant tank with a high inductance ratio where $V_i \approx n_{io}V_o$ and a normalized frequency of $\omega_n \approx 1$, the maximum magnetizing inductance that can provide ZVS can be calculated with (31).

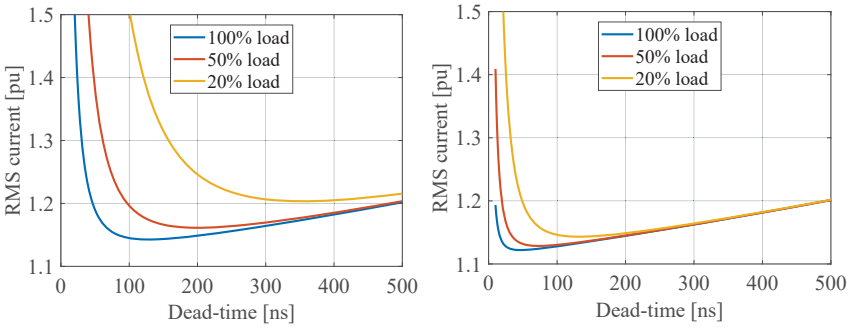
$$L_M \leq \frac{2\pi t_d}{8C_{oss}\omega_r} \tag{31}$$

From (31) it can be observed that for a given C_{oss} there are multiple combinations of L_M and t_d which can provide ZVS operation. From (17), (18) and (31) the rms value of the resonant currents for different combinations of L_M and t_d can be calculated. Fig.9 shows the rms current in per-unit versus dead-time for a given C_{oss}, where the base value is the port dc current. Generally, larger L_M leads to lower current and thus, is desired to reduce conduction losses. However, larger L_M also requires larger t_d, which causes a reduction of the effective duty cycle and as a consequence, larger rms currents are required to transfer the same amount of power. For this reason, Fig.9 results in a U shape plot, where the optimal dead-time lays at the corner of the line. So, with a careful selection of L_M and t_d for given design specifications, the rms currents can be highly reduced without incurring in additional design efforts.

B. Operation with an inductive impedance

One of the key design parameters of the resonant tank is the loaded quality factor Q_L, which is defined as the ratio between energy stored and energy loss. In practice, Q_L is calculated as the ratio between the characteristic impedance of the reactances L_r, C_r and the output load R_{ac} as given in (23) and (24).

Referring to Fig.4b, Q_L has a great impact on the dc gain characteristics and available power range. With an increasing Q_L, i.e. increasing output power, the dc gain decreases while the peak gain value moves towards the resonance frequency at $\omega_n = 1$. If Q_L is too high the resonant tank might become underdamped, so the slope of the gain curve at the switching frequency may become positive. Consequently, the impedance of the resonant network would shift from inductive to capacitive and the gain at $\omega_n = 1$ would fall below unity, and soft-switching would



(a) Input side

(b) Output side

Fig. 9: RMS current through the resonant tank in per-unit versus dead-time for $C_{oss} = 100\,\mathrm{nF}$. The rms current is converted to the per-unit system with the dc current at the selected port I_n as the base value and is calculated with $I_{rn,rms}/I_n$.

be hindered. Therefore, for a given resonance frequency ω_r and a maximum power load determined by $R_{ac,min}$, there is a maximum quality factor $Q_{L,max}$ that allows operation with an inductive impedance.

Determining $Q_{L,max}$ has already been addressed in different publications, which generally is derived from the first derivative of the gain curve with respect to the switching frequency. However, due to the high complexity of the dc transfer functions of the TP-SRC, the solution will require multiple algebraic manipulations and assumptions. In [31], the condition in (32) has been derived from a graphical tool analysis.

$$R_{AC,min} \geqslant \sqrt{\frac{L_M}{C_{eq}}} \tag{32}$$

where C_{eq} refers to the equivalent capacitance of the resonant tank.

The resonant tank capacitance is given by (33)

$$C_{eq} = \frac{1}{\omega_r L_{eq}} \tag{33}$$

L_{eq} is the equivalent inductance of the resonant tank and is calculated with (34) when referred to port i. For a symmetric design of the distributed resonant tank, i.e. $Z_{ri} = n_{i-o} Z_{ro} = n_{i-o} Z_{ro}$, (34) can also be expressed in terms of L_{Mi} as shown in (35). Finally, using (35) the condition in (32) can be rewritten as shown in (36).

$$L_{eq,i} = L_{ri} + \left(\frac{1}{n_{i-o}^2 L_{ro}} + \frac{1}{n_{i-k}^2 L_{rk}} \right) \tag{34}$$

$$L_{eq,i} = \frac{3}{2} \frac{L_{Mi}}{m} \tag{35}$$

$$m \geqslant \frac{3}{2} \left(\frac{\omega_r L_{Mi}}{R_{ACi,min}} \right)^2 \tag{36}$$

where $i = 1, 2, 3$

Equation (36) is extended for multi-port SRC architectures in (37).

$$m \geqslant \frac{p}{p-1}\left(\frac{\omega_r L_{Mi}}{R_{ACi,min}}\right)^2 \tag{37}$$

where p refers to the number of ports.

An example design is given to illustrate the dc gain characteristics of the resonant tank according to the previous constraints. A resonant tank has been designed for arbitrary design specifications and the minimum inductance ratio allowed by (36) has been selected. Fig.11-12 show the dc gain characteristics in DI and DO operation modes for different power levels and power sharing obtained from (22) and (29). It can be observed that the gain slope is negative under all operating conditions, which means that the resonant tank impedance is within the inductive region. The most restrictive scenario occurs in Fig.12b, when full power is supplied in SISO mode. It can observed that the gain slope starts shifting from negative to positive when the power slightly rises above the rated power.

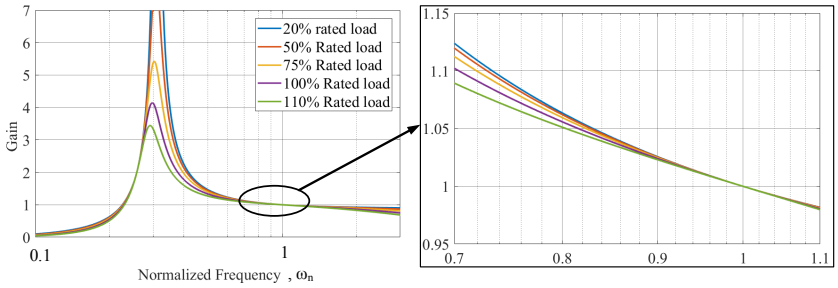


Fig. 10: dc gain characteristics in DI mode with equal power sharing.

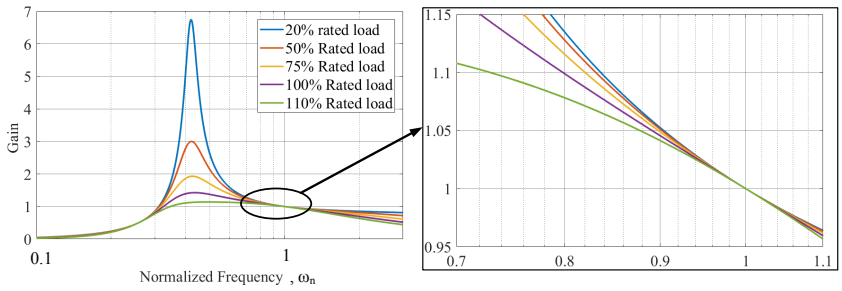
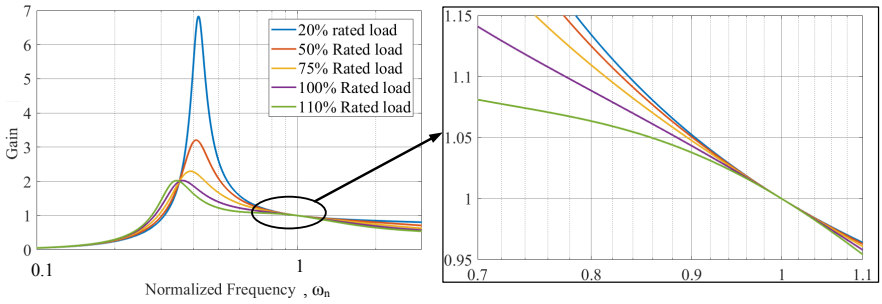


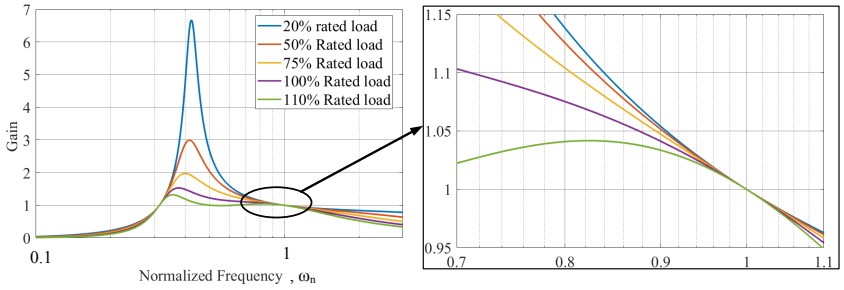
Fig. 11: dc gain characteristics in DO mode with equal power sharing.

C. Series resonant inductor selection

Because of the open-loop operation, it is important to ensure a symmetrical dc gain of the resonant tank. This is achieved by equally distributing the resonant tank among the three ports of the converter with an equal characteristic impedance, i.e. $Z_{r1} = n_{1-3} Z_{r2} = n_{1-3} Z_{r3}$. According to that, the distributed resonant inductors can be calculated with (26).



(a) Unloaded port.



(b) 100 % loaded port.

Fig. 12: dc gain characteristics in DO mode with unequal power sharing.

The inductance ratio m, and thus the selected resonant inductors, can be used to adjust the slope of the dc gain. High inductance ratios lead to flat dc gain characteristics, while low inductance ratios lead to steep dc gain slopes. For the open-loop TP-SRC, a constant dc gain at the unity is preferred, so the voltage gain can be adjusted with the transformer turns ratio as given in (38).

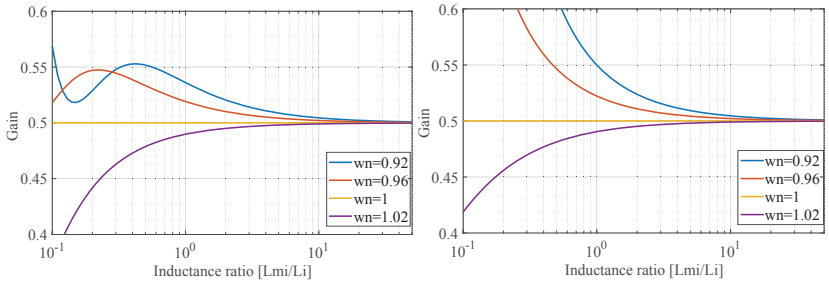
$$n_{1-3} = \frac{V_1}{V_3} \qquad n_{2-3} = \frac{V_2}{V_3} \tag{38}$$

From the dc transfer functions in (22) and (29) the effect the inductance ratio over the dc gain characteristics can be analysed. Fig.13-15 show the inductance ratio m versus dc gain under different operating conditions and switching frequencies. It can be observed that for this specific example, which do not apply to any design specifications, with $m > 10$ high cross and load regulation characteristics of the TP-SRC are obtained, since the dc gain of the resonant tank remains almost constant at the unity gain for any load condition.

D. Series resonant capacitor

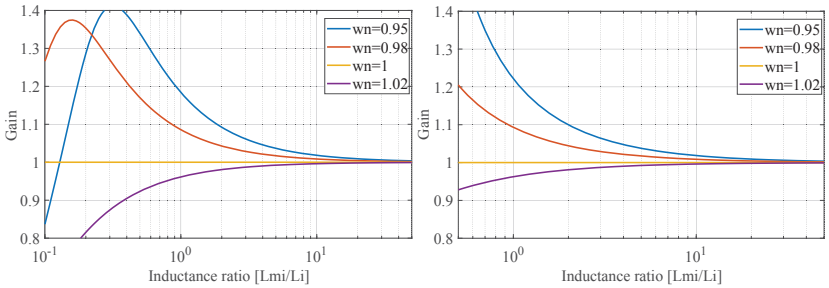
The series resonant capacitors C_r are chosen to match the resonant frequencies of the distributed resonant tank according to (39).

$$\omega_r = \frac{1}{\sqrt{L_{r1}C_{r1}}} = \frac{1}{\sqrt{L_{r2}C_{r2}}} = \frac{1}{\sqrt{L_{r3}C_{r3}}} \tag{39}$$



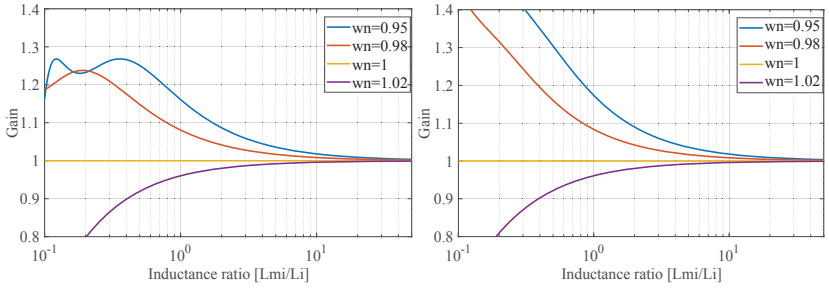
(a) At rated load. (b) At 5 % rated load.

Fig. 13: dc gain characteristics vs inductance ratio m in DI mode with equal power sharing.



(a) At rated load. (b) Unloaded.

Fig. 14: dc gain characteristics vs inductance ratio m in DO mode with equal power sharing.



(a) Loaded port. (b) Unloaded port.

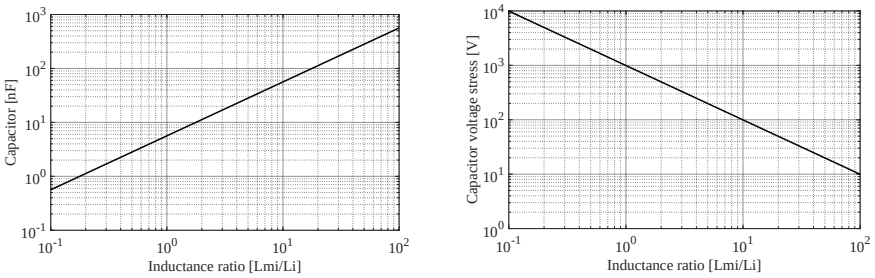
Fig. 15: dc gain characteristics vs inductance ratio m in DO mode with unequal power sharing.

For a given resonance frequency ω_r and a magnetizing inductance that fulfils ZVS conditions, the inductance ratio will also determine the resonance capacitors as shown in (40) obtained from (26) and (39).

$$C_{ri} = \frac{m}{\omega_r^2 L_{Mi}} \tag{40}$$

The voltage stress of a capacitor can be calculated with (41).

$$v_{c,pk} = \sqrt{2} I_{rms} X_c \tag{41}$$



(a) Capacitor value.

(b) Voltage stress.

Fig. 16: Resonant capacitor parameters.

where I_{rms} refers to the rms current flowing through the capacitor and X_c refers to the capacitor reactance.

Then, using (40) for $\omega_n = 1$, (41) can be rewritten as shown with (42) to approximate the voltage of the resonant capacitors.

$$v_{c,pk} \approx \sqrt{2} I_{ri,rms,\omega_r} \frac{\omega_r L_M}{m} \tag{42}$$

where I_{ri,rms,ω_r} is given in (15).

To illustrate the effect of m, in Fig.16 the required resonant capacitor and voltage stress have been calculated for the same conditions as the previous example case. For an increasing inductance ratio, the voltage stress on the capacitor dramatically decreases, being below $50\,\mathrm{V}$ for $m > 20$ with an input voltage of $400\,\mathrm{V}$. Which means that high inductance ratios will also reduce the voltage stress of the resonant capacitors. On the other hand, capacitor size increases with larger m. Therefore, there is a trade-off between voltage stress across the capacitor and capacitor size when selecting m.

V. Prototype and Experimental results

The TP-SRC SST has been validated on a $1\,\mathrm{kW}$ experimental prototype with the specifications given in Table II. A picture of the experimental prototype is shown in Fig.17. The MOSFETs selected for low voltage side (LVs) with V_{LV} are IPP114N12 ($120\,\mathrm{V}$ $11.4\,\mathrm{m\Omega}$) and for medium voltage side (MVs) with V_{MV} and high voltage side (HVs) with V_{HV} are SCT3120AL ($650\,\mathrm{V}$ $120\,\mathrm{m\Omega}$). A dead-time t_d of $275\,\mathrm{ns}$ and a magnetizing inductance of $1.1\,\mathrm{mH}$ referred to HVs have been selected, after analysing the rms of the resonant current at different load conditions for different combinations of L_M and t_d. An ETD49/25/16 core has been used to built the transformer with an air gap of $10\,\mu\mathrm{m}$ to obtain the desired magnetizing inductance. By measuring the transformer with an impedance analyzer, the leakage inductance has been extracted, resulting in $1\,\mu\mathrm{H}$ seen from the HVs. The minimum inductance ratio to fulfil ZVS at any load condition is $m_{min} = 18$, nevertheless and inductance ratio of $m = 85$ has been chosen since gives the best trade-off between load regulation together with voltage stress across the capacitors and resonant capacitors size. The resonant components have been selected to match the preferred resonance frequency $f_r = 150\,\mathrm{kHz}$, where f_r is given by (43). The resonant inductors have been built using ETD 29/16/10 cores. Finally, the resonance frequency has been measured accounting components' tolerances and parasitics. The final resonance

TABLE II: Specifications

Parameter	$V_1 = V_{LV}$	$V_2 = V_{HV}$	$V_3 = V_{MV}$	P_{max}	f_r
Value	100 V	600 V	400 V	1 kW	150 kHz

TABLE III: Design parameters

Parameter	n_{1-2}	n_{1-3}	t_{dead}	C_{oss}	L_{M1}
Value	1/6	1/4	275 ns	200 pF	30.5 µH
Parameter	L_{r1}	L_{r2}	L_{r3}	L_{Lk2}	C_1
Value	380 nH	13.8 µH	6.1 µH	1 µH	2.7 µF
Parameter	C_2	C_3	$f_{r,min}$	f_{sw}	
Value	77 nF	173 nF	146 kHz	144 kHz	

frequency measured is $f_r = 146\,\text{kHz}$ and therefore, the switching frequency is set to $f_{sw} = 144\,\text{kHz}$, where f_{sw} is given by (44). All the design parameters are summarized in Table III.

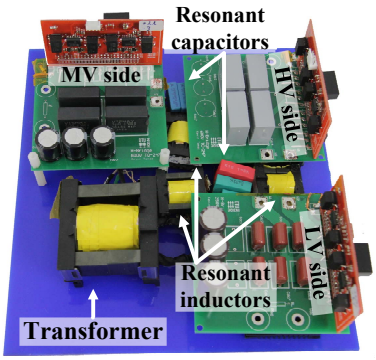
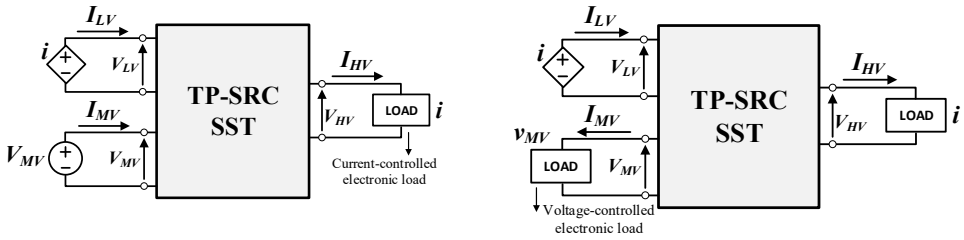


Fig. 17: Experimental prototype.

$$f_r = 2\pi\omega_r \tag{43}$$

$$f_{sw} = 2\pi\omega \tag{44}$$

The experimental verification has been carried out with two different testing platforms for DI mode and DO mode. The diagram of the experimental set-up is shown in Fig.18. The LVs is an input port and is supplied with a current-controlled voltage supply. The HVs is an output port and is connected to a current-controlled electronic load. The MVs is a bidirectional port which in DI is connected to a power supply with fixed voltage $V_{MV} = 400\,\text{V}$ and in DO mode is connected to a voltage-controlled electronic load. Tests in SISO mode are carried out by setting the current of one current-controlled port to zero. In that way the MVs port is regulated to a fix dc bus voltage while the voltage at the LVs and MVs is clamped by the TP-SRC.

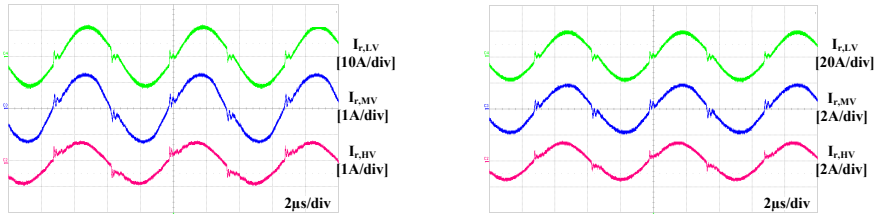


(a) DI mode (b) DO mode

Fig. 18: Simplified diagram of the testing platform

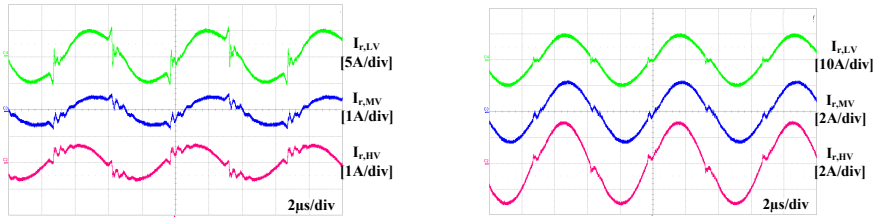
A. Steady-state operation

Figures 19 and 25 show the resonant currents flowing through each transformer winding in DO and DI operation mode at $50\,\%$ load and at rated load. It can be observed that all currents are nearly sinusoidal regardless the operation mode and the load. Therefore, the resonant converter is always operating in the vicinity of the resonance frequency at $\omega_n \approx 1$. In Fig.21, the current waveforms at no load operation are shown, where the magnetizing currents can be observed.



(a) $50\,\%$ rated load. (b) $100\,\%$ rated load.

Fig. 19: Waveforms of the resonant currents in DO mode. Input: LVs; Output: HVs and MVs.



(a) $50\,\%$ rated load. (b) $100\,\%$ loaded port.

Fig. 20: Waveforms of the resonant currents in DI mode. Input: LVs and MVs; Output: HVs.

Figures 22 and 23 show the ZVS operation at LVs (PV port) and HVs (grid-side port) at $50\,\%$ load and at rated load. Fig.22 and 23 illustrate the transformer current, MOSFET's drain-source voltage V_{DS} and MOSFETs' gate to source voltage V_{GS}.

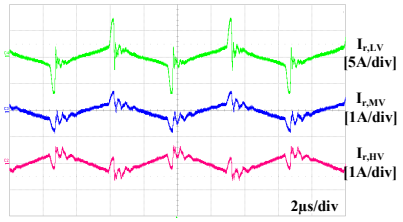
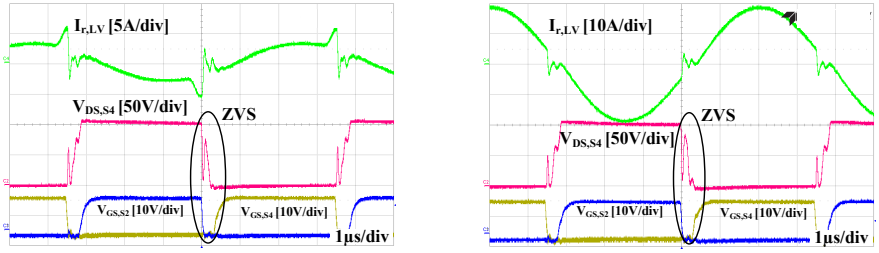


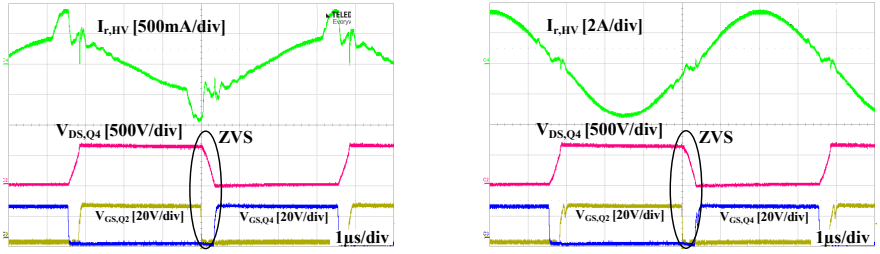
Fig. 21: No load operation.

In Fig.22 high frequency oscillations appear around the current zero crossings after the turn-off event. These high frequency oscillations at approximately $4\,\mathrm{MHz}$ are caused by the resonance between the MOSFETs' output capacitances C_{oss} of the output bridges and the resonant inductor. These capacitors will participate in the resonance whenever the resonance current equals to the magnetizing current. When the LVs operates as an input (Fig.22), the amplitude of the reflected high frequency oscillations force the current to change direction during the free-wheeling period. For that reason, oscillations appear at the drain-source voltage, evidenced in $V_{DS,S4}$ from Fig.22.



(a) 10 % rated load. (b) 100 % rated load.

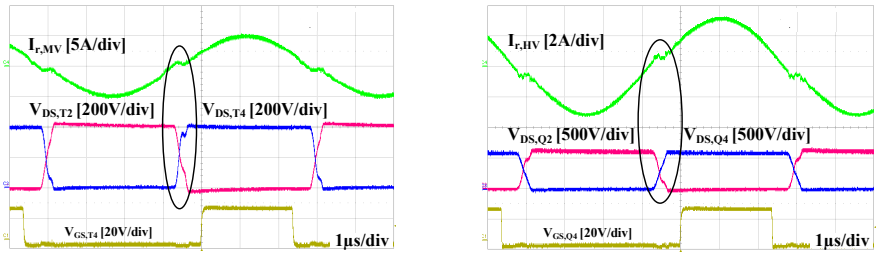
Fig. 22: ZVS operation at LVs.



(a) 5 % rated load. (b) 100 % rated load.

Fig. 23: ZVS operation at HVs.

Fig. 24 shows MVs (battery port) and HVs (grid-side port) when operating as output ports at rated load. Fig. 24 illustrates transformer currents, MOSFETs' drain-source voltage V_{DS} of complementary switches and gate to source voltage V_{GS}.

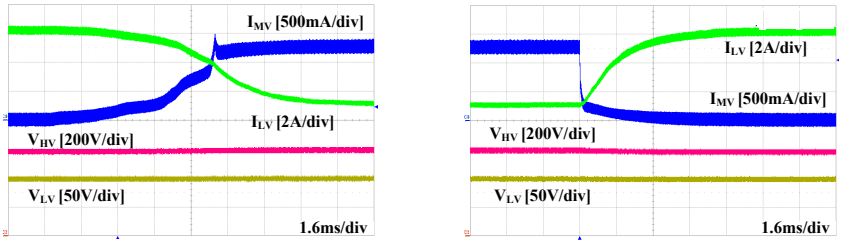


(a) MVs. (b) HVs.

Fig. 24: Soft-commutation operation of output ports at $100\,\%$ rated load.

B. Dynamics

Dynamic tests have been carried out to verify the voltage stability of the unregulated ports HVs and LVs during changes of power magnitude and operation mode. Fig.25 shows a transition from SISO to DI and vice-versa. Fig.25 illustrates currents flowing through the input ports I_{LV} and I_{MV},voltage at LVs input V_{LV} and voltage at HVs output V_{HV}, while the voltage at MVs V_{MV} is constant at $400\,\mathrm{V}$. The transition test performed consists of changing the current reference of the current-controlled power supply at the LVs while keeping the same output power. In Fig.25a shows that the LVs supplies $600\,\mathrm{W}$ to HVs while MVs does not transfer any power. Then, the current referenced of the LVs is decreased from $6\,\mathrm{A}$ to $1.75\,\mathrm{A}$, so current starts flowing from the MVs to the HVs to compensate the loss of power. It can be observed that the unregulated voltage at the unregulated dc buses V_{LV} and V_{HV} remain always constant. Fig.25b shows the transient from DI to SISO, which shows the same results.



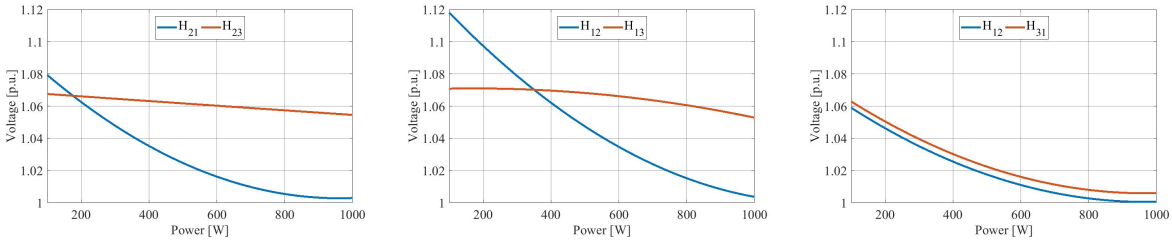
(a) SISO to DI. (b) DI to SISO.

Fig. 25: Operation mode transition SISO-DI. Input: LVs and MVs; Ouput: HVs.

C. Cross and -load regulation characteristics

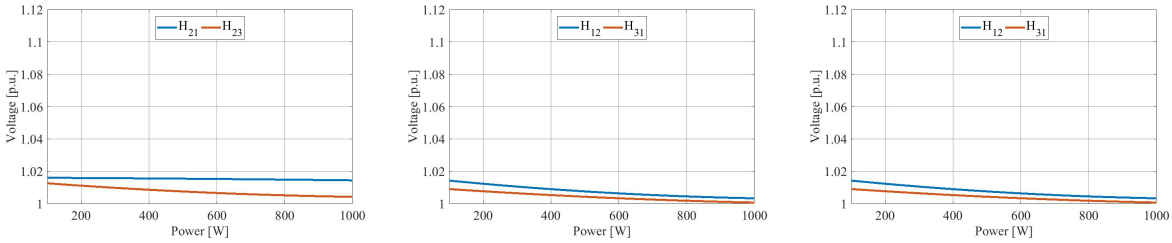
To verify and contrast the design optimization of the open-loop TP-SRC a second resonant tank with a lower inductance ratio was implemented and tested with the converter prototype. Experimental verification has been carried out by measuring the voltage across each port while sweeping the output power from no load to full load. Fig.26 shows the results obtained in SISO, DO and DI operation modes with the lowest inductance ratio of $m = 20$ and Fig.27 shows the final design with the highest inductance ratio of $m = 80$, notice that the y-axis scales are different

and the voltage magnitude is given in per-unit system. For $m = 20$ the largest voltage variation is $8.6\,\%$ in DO operation in Fig.26b. In contrast, for $m = 80$ the largest voltage variation is $1.6\,\%$ also in DO mode.



(a) SISO (b) DO (c) DI

Fig. 26: Experimental results of the steady-stage load regulation with $m = 20$.



(a) SISO (b) DO (c) DI

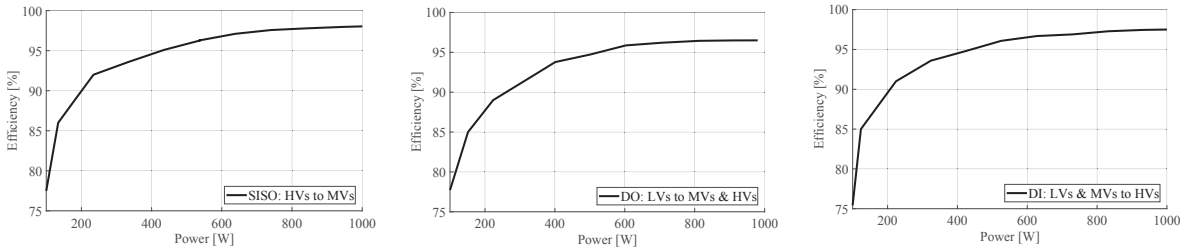
Fig. 27: Experimental results of the steady-stage load regulation with $m = 80$.

D. Efficiency

Efficiency results are shown in Fig.28. To obtain consistent efficiency measurements the power has been kept equally shared in DI and DO among input and output ports respectively. Similar results are obtained for the different operation modes. A maximum efficiency of $98\,\%$ has been found at rated load, while at $20\,\%$ load a maximum efficiency of $90\,\%$ has been reported. Considering the state of the art in resonant converters, the light load efficiency can be considered high, since usually these kind of converters incur in high losses at light load. This increase in efficiency is given due to an optimal selection of the circulating current at a fixed switching frequency which provides ZVS. In addition, utilization of synchronous rectification at the output ports incurs in reduced conduction losses at heavy load, so high efficiencies can also be reported at the high end of the power range.

VI. Conclusions

In this paper a three-port series resonant converter (TP-SRC) operating in open loop with a fixed duty cycle and switching frequency have been proposed. The TP-SRC aims to simplify the interconnection of multiple RES, ESS and the grid in household applications, even though it can be implemented in any solid-state transformer



(a) SISO (b) DO (c) DI

Fig. 28: Efficiency measurement.

applications. The TP-SRC has three dc buses where two of them are not controlled and kept constant because of the inherited cross and load regulation characteristics of TP-SRC. The proposed system also aims in improving the system modularity achieve a high level of RES and ESS integration. Open-loop operation highly simplifies the control system design from the hardware and software point of view, and therefore it can also potentially reduce the costs. Open-loop operation also allows an optimal design of the TP-SRC to achieve high efficiency, since zero voltage switching (ZVS) at the input ports and soft-commutation at the output ports can always be achieved. In this paper, the rms current of the resonant tank considering the dead-time has been derived. This allows an optimal selection of the dead-time and the transformer magnetizing inductance which can provide ZVS with the lowest circulating current and thus, with reduced conduction losses and turn-off. Synchronous rectification at a fixed duty cycle of the output side switches is implemented, therefore conduction losses in the output ports are also reduced. A design methodology to select the minimum inductance ratio that allows operation within the inductive region of the resonant tank has been proposed and verified for all operation modes. To analyze the dc gain performance under different operating conditions and design approaches, the dc transfer functions for DI and DO operation of the TP-SRC have been derived. Finally, a design approach to improve the inherited cross and load regulation characteristics of the converter and reduce the voltage stress of the resonant capacitors has been proposed. The proposed solution has been verified on a $1\,\mathrm{kW}$ converter prototype. Results show that soft-switching operation is obtained in all operating modes from light load to heavy load. Results obtained from the voltage regulation characteristics show a maximum voltage span of $1.6\,\%$ over the dc voltage, which verified the optimal design of the open-loop TP-SRC. Finally, a maximum efficiency of $98\,\%$ have been reported at rated load while at $20\,\%$ load the efficiency is around $90\,\%$.

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Three-Port Series-Resonant Converter DC Transformer with Integrated Magnetics for High Efficiency Operation

In IEEE ECCE, Portland, September 23-27, 2018.

Three-Port Series-Resonant Converter DC Transformer with Integrated Magnetics for High Efficiency Operation

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***Abstract*—The series-resonant converter has become a very attractive topology for solid-state transformers due to its fixed voltage gain and soft-switching conditions when operating at the resonance frequency. This paper presents an open-loop three-port series-resonant converter (TP-SRC) capable of interconnecting three dc microgrids. High efficiency power electronics is a key enabler for the future dc distribution systems. In this paper, efficiency optimization and rms current reduction of the TP-SRC is achieved by a detailed analysis of the resonance frequency and dead-time selection. The analysis is supported by a losses modelling of the main components of the converter. In addition, Gallium Nitride (GaN) MOSFETs are used to reduce semiconductors' losses. Furthermore, the resonance inductance of the distributed resonant tank has been integrated into the leakage inductance of the transformer and the PCB parasitic inductances. In order to ensure a fixed resonance frequency, an experimental resonance frequency matching methodology for the resonant tank has been presented. Experimental results were obtained for a $1.4\,\mathrm{kW}$ featuring a peak efficiency of $98.8\,\%$.**

I. Introduction

State-of-the-art in electrical power conversion shows a tendency towards the utilization of Solid-State transformers (SST) as interlinking converters between dc grids [1]. Technological advances in SST that enhance the system scalability and dc grids flexibility in combination with improvements in energy conversion efficiency, are key enablers to motivate the penetration of SST into dc distribution systems. Among the different power converter topologies implemented as SST , the Series-Resonant converter (SRC) has been extensively used [2–5] because of its load regulation characteristics in open-loop together with its soft-switching conditions for wide power ranges. Many optimization methods focusing on the efficiency improvement of the SRC have been discussed in the literature. Authors in [6] proposed a computer aided algorithm with the calculated efficiency as the objective function. The loss model was carried out for a LLC SRC with phase-shifted modulation and results were verified on a $300\,\mathrm{W}$ $400\,\mathrm{V}$ prototype with a peak efficiency of $97.07\,\%$. In [7] an efficiency analysis for a two port open-loop SRC was presented. The efficiency was optimized by utilizaing silicon-carbide MOSFETs and a detailed design procedure based on an accurate losses modelling, where the losses were analysed for a fixed resonance frequency of $20\,\mathrm{kHz}$. The losses model was verified on a $10\,\mathrm{kW}$ SRC with a peak efficiency of $98.61\,\%$. In [8] losses optimization were performed for a current-fed SRC based on $15\,\mathrm{kV}$ SiC MOSFETs. A fixed dead-time strategy was adopted, incurring in partial soft-switching conditions, so the converter design parameter was carried out based on a trade-off between conduction losses and switching losses. Reported efficiency on a $12\,\mathrm{kW}$ prototype was $97.8\,\%$.

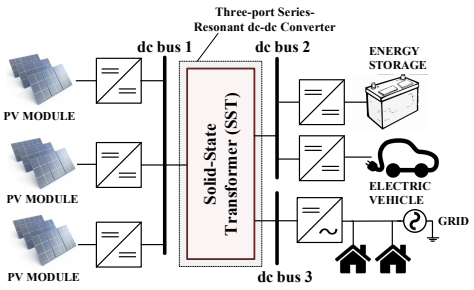


Fig. 1. Example of application for the Three-Port Series-Resonant Converter operating as a Solid-State Transformer to interconnect multiple dc grids.

In this paper, an efficiency optimization for a Three-Port Series-Resonant converter (TP-SRC) with a distributed resonant tank is presented. The TP-SRC aims at interconnecting three dc-bus, which are utilized to integrate RES, LES and the ac grid. The system architecture diagram is presented in Fig.1. The TP-SRC operates in open-loop at the sub-resonance region, at a fixed switching frequency and duty cycle. The design methodology of the TP-SRC is based on the design equations proposed in [4], [5], where the resonant tank parameters are selected to ensure soft-switching under all operation conditions. On the other hand, the SRC generally incurs into high root-square-mean (rms) currents due to the sinusoidal shape of the resonant current together with the magnetizing current flowing through the inputs ports. Therefore, while the switching losses are almost negligible, the SRC suffers from higher conduction losses. The design procedure given in [4], [5] have two degrees of freedom which are the switching frequency and dead-time. The effect of these two parameters into the converter rms currents and losses is analyzed in this paper. To further improve the efficiency, Gallium-Nitride (GaN) MOSFETs with very low on-state resistance are used, decreasing dramatically the conduction losses. Furthermore,

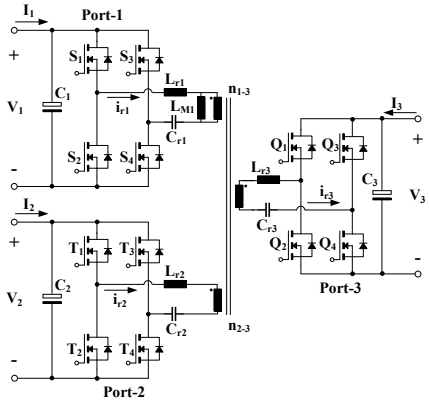


Fig. 2. Topology of the Three-Port Series Resonant Converter.

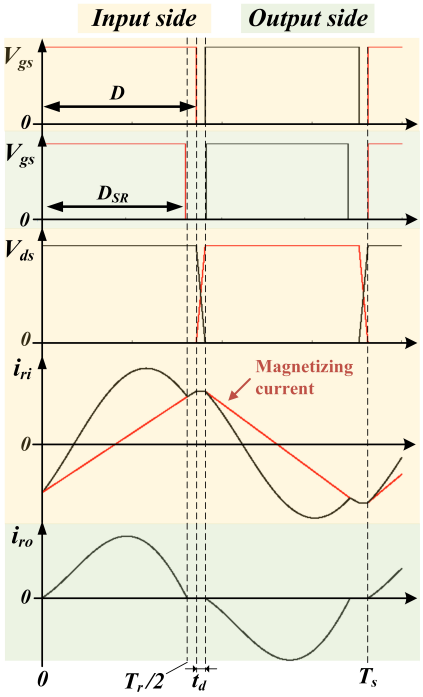


Fig. 3. Main waveforms of the Three-Port Series Resonant Converter.

the leakage inductance of the resonant tank is solely implemented by the leakage inductance of the transformer and the PCB parasitics. In that way, external resonant inductors are avoided and the converter losses are further minimized. Since the resonant inductance is solely composed by the leakage inductance of the transformer and the parasitic inductances, the resonance frequency matching of the distributed resonant tank becomes challenging. An experimental methodology for tuning the resonant tanks at each side of the transformer at the same resonance frequency id also presented in this study.

This paper is organized as follows: section II describes the operation principle of the TP-SRC, where the main design equations are provided. In section III the extended rms equations of the resonant currents are given and the losses analysis methodology in all components is presented. In section IV, the influence of the dead-time and switching frequency to the rms currents and the efficiency is analyzed. In section V, the resonance frequency matching methodology is explained. Section VI presents the implementation procedure and the experimental results on a $1.4\,\mathrm{kW}$ prototype, where a peak efficiency of $98.8\,\%$ is demonstrated.

II. Three-Port Series-Resonant Converter

The circuit diagram of the bidirectional TP-SRC is shown in Fig.2 and Fig.3 illustrates the main waveforms of the converter. The SRC achieves the highest efficiency when the switching frequency is equal or slightly below the resonance frequency [7], which is given by the resonant inductors L_r and resonant capacitors C_r. At this operation region the MOSFETs at the input bridges operate with zero-voltage switching (ZVS) at the turn-on, while the turn-off is carried out at low current and the MOSFETs at the output bridges operate with zero-current switching (ZCS). An additional advantage is that the SRC has a fixed input-to-output voltage gain when is operating at the vicinity of the resonance frequency. Due to the fixed voltage gain and soft-switching conditions, open-loop operation of the TP-SRC results in a very attractive solution for applications where only load regulation is required and the dc bus voltages are constant.

The TP-SRC operates at a fixed switching frequency f_{sw} and MOSFETs at input ports are actively switched with a $50\,\%$ duty cycle with a dead-time. Synchronous rectification is used in the output ports to reduce conduction losses. In order to prevent hindering soft-switching, synchronous rectification is implemented at the switching frequency and with an on-time equal to half the resonant period.

The design of the resonant tank is based on the methodology proposed in [5], where the main requirements are (I) to provide the minimum energy to charge/discharge the MOSFTETs' output capacitance C_{oss} and (II) to operate with an inductive impedance of the resonant tank under any load condition. The first conditions is fullfiled by selecting a magnetizing inductance L_{M1} that provides enough peak current during the dead-time to charge and discharge the MOSFETs' C_{oss}. According to [5], to ensure ZVS the magnetizing inductance L_{M1} should be lower than the maximum magnetizing inductance $L_{M1,max}$ given by (1). Then, the magnetizing inductance is chosen according to (2) to ensure that ZVS will be achieve in all ports. As explained by the authors in [5], the minimum inductance ratio to ensure operation with an inductive impedance, and thereby achieve ZVS under all operating conditions, can be calculated with (3), and therefore the condition in (4) has to be fulfilled. Finally, the resonant capacitors are chosen with (5).

Utilizing the design equations (1)-(5) and the design specifications from Table I, the resonant tank parameters can be calculated. As can be observed, the design procedure contains two main degrees of freedom, which are the resonance fre-

TABLE I
SPECIFICATIONS FOR THE TP-SRC

Parameter	Value
Maximum power P_{max}	1.4 kW
Port-1 voltage $V_1 = V_{LV}$	80 V
Port-2 voltage $V_2 = V_{MV}$	400 V
Port-3 voltage $V_3 = V_{HV}$	600 V
Turns ratio n_{1-3}	1/7.5
Turns ratio n_{2-3}	1/1.5

quency and the dead-time. These parameters will be selected in order to achieve the highest efficiency.

$$\begin{aligned} L_{M1,max,S} &= \frac{t_d}{8C_{oss,_S} f_{sw}} \\ L_{M1,max,T} &= n_{1-2}^2 \frac{t_d}{8C_{oss,_T} f_{sw}} \\ L_{M1,max,Q} &= n_{1-3}^2 \frac{t_d}{8C_{oss,_Q} f_{sw}} \end{aligned} \tag{1}$$

$$L_{M1} = min\{L_{M1,S}, L_{M1,T}, L_{M1,Q}\} \tag{2}$$

$$k_{min} = \frac{3}{2}\left(\frac{\pi^2 \omega_r L_{M1} P_{max}}{8V_1^2}\right)^2 \tag{3}$$

$$k_{min} \leqslant \frac{L_{M1}}{L_{r1}} \quad k_{min} \leqslant \frac{L_{M1}}{n_{1-2}^2 L_{r2}} \quad k_{min} \leqslant \frac{L_{M1}}{n_{1-3}^2 L_{r3}} \tag{4}$$

$$C_{r1} = \frac{1}{\omega_r^2 L_{r1}} \quad C_{r2} = \frac{1}{\omega_r^2 L_{r2}} C_{r3} = \frac{1}{\omega_r^2 L_{r3}} \tag{5}$$

where

$C_{oss,_S}$: Output capacitances of MOSFETs S_1-S_1.
$C_{oss,_T}$: Output capacitances of MOSFETs T_1-T_4.
$C_{oss,_Q}$: Output capacitances of MOSFETs Q_1-Q_4.
f_{sw}: Switching frequency.
f_r: Resonance frequency.
ω_r: angular resonance frequency given by $\omega_r = 2\pi f_r$.
n_{1-2}: Turns ratio from Port-1 to Port-2 given by n_{1-3}/n_{2-3}.
k_{min}: Minimum inductance ratio.
P_{max}: Maximum rated power.

III. LOSSES ANALYSIS METHODOLOGY

In order to analyse the effect of the switching frequency and dead-time to the converter efficiency, a careful analysis of the losses in the main components of the TP-SRC is computed for the given specifications. To support the losses analysis the equations to calculate the rms currents flowing through the resonant tanks are given by (6) and (7) and the magnetizing current at the beginning of the dead-time is given by (8).

$$\begin{aligned} I_{ri,rms} = n_{i-o}^2 V_o \frac{\sqrt{2}}{8} \sqrt{\frac{(T_{sw} - 2t_d)^2 (T_{sw} + 2t_d)}{T_{sw} L_{Mi}^2}} \\ + \sqrt{\frac{T_{sw} 4\pi^2 P_i^2}{(T_{sw} - 2t_d) n_{i-o}^4 V_o^4}} \end{aligned} \tag{6}$$

TABLE II
SPECIFICATIONS OF THE MOSFETS USED IN THE DESIGN

Port	Switches	Reference	V, I
Port-1	$S_1 - S_4$	GS61008P	100 V 90 A
Port-2	$T_1 - T_4$	GS66506T	650 V 22.5 A
Port-3	$Q_1 - Q_4$	GS66504B	650 V 15 A

$$\begin{aligned} I_{ro,rms} = \frac{\sqrt{2}}{4} V_o \sqrt{\frac{n_{i-o}^4}{L_{Mi}^2} \frac{(T_{sw} - 2t_d)^3}{T_{sw}} \frac{5\pi^2 - 48}{12\pi^2}} \\ + \sqrt{\pi^2 \frac{T_{sw}}{T_{sw} - 2t_d} \frac{P_o^2}{V_o^4}} \end{aligned} \tag{7}$$

$$I_M = \frac{1}{4} \frac{V_1 (T_s - 2t_d)}{L_{M1}} \tag{8}$$

where i refers to the input port, o to the output port, t_d to the dead-time, T_{sw} to the switching period $1/f_{sw}$ and L_{Mi} to the magnetizing inductance referred to the input port.

A. Semiconductors losses

In order to achieve highest efficiency performance of the semiconductors, GaN MOSFETs are selected. GaN transistors are characterized by low on resistance $R_{ds,on}$ and low output capacitance C_{oss}. The combination of low energy losses with ZVS results in very low switching losses. In reverse conduction, GaN MOSFETs have larger voltage drop across the body diode than Silicon MOSFETs. But when using synchronous rectification, the current flows through the MOSFET channel, and therefore the losses in reverse conduction are given by the $R_{ds,on}$. The MOSFETs selected are given in Table II.

The main losses of a MOSFET are divided in conduction losses and switching losses. The conduction losses for the input side MOSFETs $P_{cond,in}$ can be calculated with (9), where $I_{ri,rms}$ is calculated with (6). As the converter operates under ZVS on the input side, turn-on losses can be neglected. However, at the turn-off event, the current flowing through the MOSFETs channel hardly commutates to the body diodes of the complementary switches incurring in turn-off losses $P_{off,in}$. The turn-off losses when switching at the vicinity of the resonance frequency can be calculated with (10) [9], where I_M is the magnetizing current at the turn-off event.

Synchronous rectification is used at the output side MOSFETs. Because of the fixed switching frequency and fixed duty cycle operation, the output MOSFETs turn-on and turn-off events can be adjusted to avoid current circulation through the body diode by fixing the on-time below half the resonance period. Therefore, the conduction losses of a MOSFET at the output side $P_{cond,out}$ can be calculated with (11). As the converter operates in the vicinity of the resonance frequency ZCS on the output side is always achieved, and thus, the switching losses can be neglected.

$$P_{cond,in} = \frac{R_{ds,on} I_{ri,rms}^2}{2} \tag{9}$$

$$P_{off,in} = \frac{1}{6}\left(V_{ds} I_M - C_{oss}\frac{V_{ds}}{t_{off}}\right) t_{off} f_s \tag{10}$$

$$P_{cond,out} = \frac{R_{ds,on} I^2_{ro,rms}}{2} \tag{11}$$

B. Transformer losses

The transformer design has been carried out to optimize its losses through the design methodology explained below. The design procedure have two degrees of freedom, which are the core size and the flux density. The cores considered for the design are (I) ETD 49/25/16, (II) ETD 54/28/19 and (III) ETD 59/31/22. The transformer has been designed through a loop where the peak flux density β_{max} has been swept from $50\,\mathrm{mT}$ to $300\,\mathrm{mT}$. To reduce the complexity of the comparative analysis single wire gauge has been considered and an interleaved arrangement of the transformer windings is assumed. The wire gauge is selected at the skin depth δ as given by (12) to reduce the skin effect, and the number of strands is calculated to meet the power requirements. Then, the number of turns is calculated for the flux density selected. Based on the design specifications, the maximum flux linkage occurs at Port-3, where $V_3 = 600\,\mathrm{V}$ and thus, the number of turns is calculated according to (13). To adjust the inductance of the transformer to the desired magnetizing inductance, given by (2), the air-gap length is calculated with (14). Subsequently the implementation viability is verified by comparing the window area of the core with the required area by the design. If the design is successful the winding and core losses are calculated, otherwise the peak flux density is increased and the transformer is redesigned. When the peak density reaches the maximum, a larger core size is chosen.

$$\delta = \frac{7.5}{\sqrt{f_{sw}}}(cm) \tag{12}$$

$$N_3 = \frac{V_3}{4 f_{sw} A_c \beta_{max}} \tag{13}$$

$$l_g = \frac{\eta_0 N_3^2 A_c}{n_{1-3}^2 L_{M1}} \tag{14}$$

where

N_3: Number of turns of the transformer at Port-3.
A_c: Cross-sectional area of the transformer core.
η_0: Permeability of free space $\eta_0 = 4\pi \cdot 10^{-7} Hm^{-1}$.

The dc winding resistance is calculated with (15) and Dowell's equations [10] are used to estimate the ac resistance (16). The copper loss of the transformer can be calculated with (17), where the rms currents at the transformer windings are calculated with (6) or (7) whether the port behaves as an input or an output. Finally, the core losses are estimated using Steinmetz equation (18).

$$R_{dc} = \frac{\rho_{cu} N_{tr} MLT}{A_{AWG}} \tag{15}$$

$$\frac{R_{ac}}{R_{dc}} = \frac{\Delta}{2}\left[\frac{\sinh\Delta + \sin\Delta}{\cosh\Delta - \cos\Delta} + (2m-1)^2 \frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta}\right] \tag{16}$$

$$P_{TR,W} = R_{ac1} I^2_{r1,rms} + R_{ac2} I^2_{r2,rms} + R_{ac3} I^2_{r3,rms} \tag{17}$$

$$P_{TR,C} = K f_{sw}^{\alpha} \beta_c^{\beta} \tag{18}$$

Δ: h/δ.
h: Conductor height
m: Number of layers. $m = 1$ for interleaved multilayer windings.
ρ_{cu}: Resistivity of the copper. $\rho_{cu} = 1.72 \times 10^{-8} \Omega m$ @ $20\,^{\circ}\mathrm{C}$.
MLT: Core mean-length-turn.
A_{AWG}: Wire cross-sectional area.
K, α, β: Core material parameters provided by the manufacturer. For N87 material $K = 3.73 \cdot 10^{-7}$, $\alpha = 2.1$ and $\beta = 2.48$.

The total transformer losses are calculated with (19) and to ensure transformer operation under a safe temperature range, the condition in (20) should be satisfied.

$$P_{TR} = P_{TR,W} + P_{TR,C} \tag{19}$$

$$P_{TR} \leqslant \frac{T_{max} - T_{amb}}{T r_c} \tag{20}$$

where T_{max} is the maximum safe-operating temperature of the transformer core, T_{amb} is the ambient temperature and $T r_c$ the core thermal resistance given by the manufacturer.

C. Resonant capacitor

The losses at the capacitor are due to the equivalent series resistance (ESR) which is given by the resonance frequency, the capacitance and the dissipation factor $\tan\delta$ as shown in (21). To optimize the losses at the resonance capacitor, Polyphenylene sulfide (PPS) and Polypropylene (PP) film capacitors have been utilized due to their low dissipation factor. In addition, the temperature and frequency dependence of the electrical parameters in PP and PPS film capacitors are also low compared to their counterparts. To have a more accurate estimation of the losses at the resonant capacitor, a database containing a linearised function of $\tan\delta$ in terms of frequency for different capacitors have been included in the calculation. Once the ESR has been estimated, the losses at the resonant capacitors are calculated with (22), where the rms currents are calculated with (6) or (7) whether the port behaves as input or output.

$$ESR = \frac{\tan\delta}{2\pi f_r C_r} \tag{21}$$

$$P_{C_r} = ESR_1 I^2_{r1,rms} + ESR_2 I^2_{r2,rms} + ESR_3 I^2_{r3,rms} \tag{22}$$

IV. RMS CURRENTS AND EFFICIENCY ANALYSIS

A. Switching frequency analysis

By following the design procedure given in Section II, with equations (1)-(4) soft-switching conditions are always achieved and thus, MOSFETs' turn-on losses are almost negligible. This indicates that potentially higher switching frequency is achievable. The rms currents in terms of switching frequency have been calculated for different dead-times using (1)-(8). Results are depicted in Fig.4. The rms currents are given in per-unit, where the base unit is the dc current at the input or output port. The base relationships at the input port are not the same for different power levels due to the magnetizing current, which is not load-dependent. Conversely, at the output side the per-unit rms current do not differ for different power levels. It can be observed that for a fixed t_d, increasing the switching frequency can lead to an increase of the rms current, and thus, the MOSFETs' conduction losses can increase accordingly.

On the other hand, increasing the switching frequency allows the use of smaller passive components, including the resonant tank parameters. The maximum resonant inductance allowed to operate the TP-SRC with an inductive impedance and the corresponding resonance capacitance have been calculated using (1)-(5) for different t_d and f_{sw}. Results are given in Fig.5. As expected, by increasing the switching frequency the maximum resonant inductance L_r decreases. This can increase the design complexity of the converter, since the maximum L_r allowed by the design might drop down below the total series inductance, which is mainly composed by the leakage inductance of the transformer together with the parasitic inductances of the PCB. Consequently, the resonant converter would fall into the capacitive operating region and soft-switching would be hindered [4], [5].

B. Dead-time analysis

For a given switching frequency the rms currents have been calculated with different combinations of t_d and L_M at different power levels using (1)- (8). Results obtained are given in Fig. 9. Small t_d implies smaller L_M which results in larger circulating current hence larger conduction losses. At the same time, large t_d causes a reduction of the effective duty cycle, and thus larger rms currents are required to transfer the same power from input side to output side.

For different power levels the optimal combination of t_d and $L_M 1$ that gives the lowest rms currents differs, and therefore the optimal design for the entire power range can not be accomplished. For a design where the rms current should be minimized for all load conditions, a normal distribution of the optimal t_d for each power level can be utilized as illustrated in Fig.7.

C. Efficiency analysis

First, the overall efficiency of the TP-SRC has been calculated in terms of switching frequency and resonant components size. The efficiency calculation has been carried out following the losses analysis depicted in Section II. At this stage, the

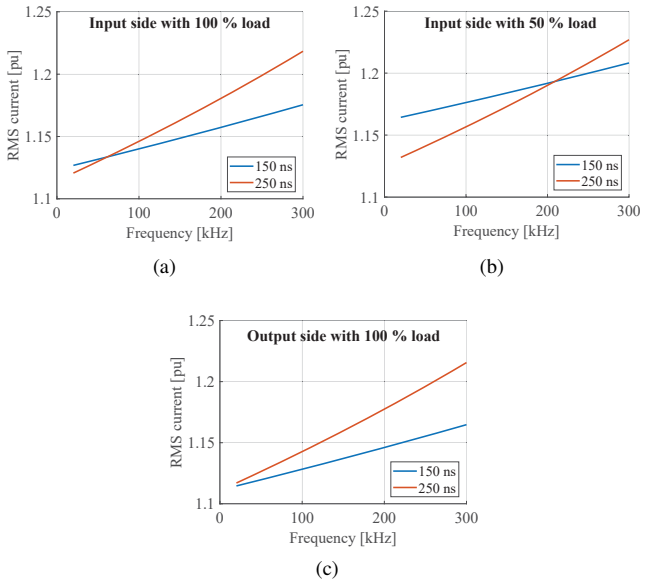


Fig. 4. Resonant rms current in per-unit at input and output side in terms of frequency with fixed dead-time and different power transfer. The rms current is converted to the per-unit system with the dc current at the input or output port I as the base value and is calculated with $Ir, rms(pu) = Ir, rms/I$. The per-unit rms current at the input side is load-dependent due to the magnetizing current, which is not load-dependent.

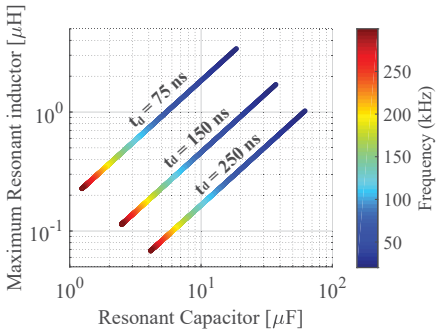


Fig. 5. Resonant tank components at the LV side $L_{r,HV}$ and $C_{r,HV}$ for different switching frequencies f_{sw} and dead-times t_d. For each switching frequency and dead-time the result gives the maximum resonant inductance allowed according to (3).

resonant inductance is an unknown parameter, since it is composed by the leakage inductance of the transformer and the parasitic inductances of the PCB. For that reason, the resonant inductor parameter has been swept from a minimum to maximum value of $L_{r,HV} = 100\,\text{nH}..30\,\mu\text{H}$ in the computational algorithm. The efficiency has been calculated for the lowest conduction losses by selecting the dead-time that results in the lowest rms current for each switching frequency. Results obtained are given in Fig.10. Taking into account the results obtained for $50\,\%$ load and rated load, a potential switching frequency between $100\,\text{kHz}$ to $150\,\text{kHz}$ would give the highest efficiency with the smallest resonant capacitor.

As previously discussed, the optimal combination of t_d

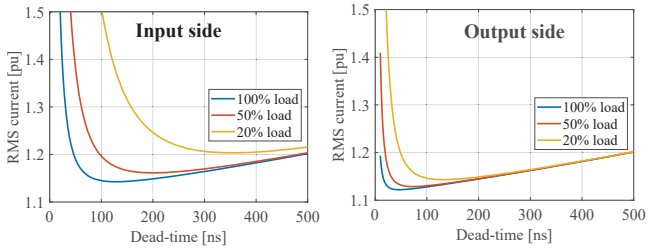


Fig. 6. Resonant rms current in per-unit at input and output side in terms of dead-time with a $f_{sw} = 150\,\text{kHz}$ and different power transfer. The rms current is converted to the per-unit system with the dc current at the input or output port I as the base value and is calculated with $Ir, rms(pu) = Ir, rms/I$. The per-unit rms current at the input side is load-dependent due to the magnetizing current, which is not load-dependent.

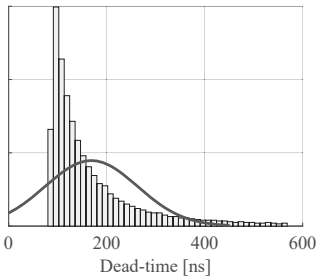


Fig. 7. Normal distribution of the optimal dead-time for each power level.

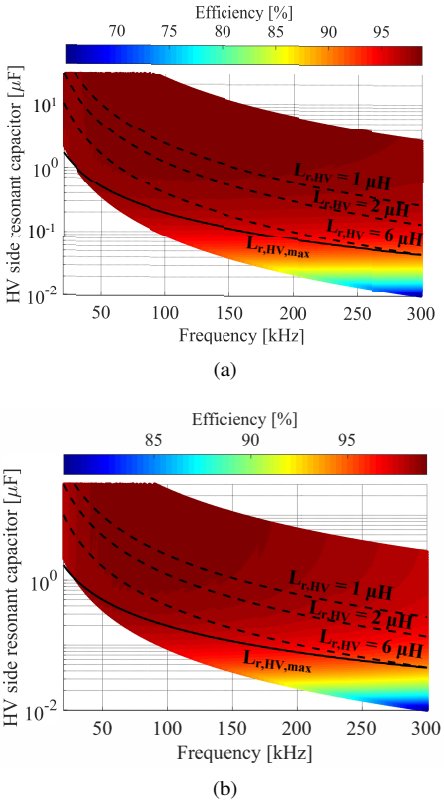


Fig. 8. Analysis of the TP-SRC efficiency in terms of switching frequency and resonant components size. Efficiency is calculated for dual-output mode with LV side as input at maximum output power with equal power sharing among ports. The dead-time has been selected to achieve the lowest rms current in each efficiency measurement.

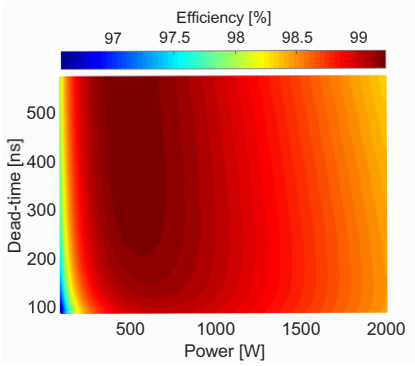


Fig. 9. Analysis of the TP-SRC efficiency in terms of t_d and power level. Efficiency is calculated for dual-output mode with LV side as input at $f_{sw} = 150\,\text{kHz}$ with $L_{r,HV} = 1.5\,\mu\text{H}$.

and L_M that incurs in the smallest rms current changes for different power levels. For that reason, the effect of t_d to the overall efficiency is also analysed. Fig.9 shows the theoretical efficiency in terms of t_d and input power for a given switching frequency.

V. Resonance Frequency Matching

The TP-SRC presented in this paper utilizes the leakage inductance of the transformer and the PCB parasitic inductances as the inductive component of the resonant tank. Consequently, the total resonant inductance seen from each port is unpredictable, which complicates the resonance frequency matching. The TP-SRC can still operate at a fixed switching frequency, even if the resonant frequency at each port is not the same. However, in some operating modes, the resonance frequency would be further away from the switching frequency and thus, the converter would not be operating at its optimal operating region from the efficiency point of view. The process implemented to carry out the resonance frequency matching is described below.

From the transformer leakage inductance, the theoretical values of the resonant capacitors at each port are calculated with (5) for the selected resonance frequency. Once the resonant capacitors are mounted on the PCB, the resonance frequency has to be retuned to compensate for the parasitic inductances. Firstly, the resonance frequency at one side of the transformer is found by short-circuiting the resonant capacitors at the other two sides and measuring the voltage gain after the resonance capacitor, as shown in Fig.10a. In that way, the resonance frequency obtained f_{req1} from the gain measured is only due to the capacitor at the input side and the overall resonance inductance of the resonant tank L_{eq1} as shown in Fig.10b. Then, from $f_{r,eq1}$ and C_{r1}, the equivalent resonance inductance L_{eq1} can be calculated as given in (23). The measurement is repeated for the other two ports to calculate the equivalent inductances L_{eq2} and L_{eq3}. Subsequently, the

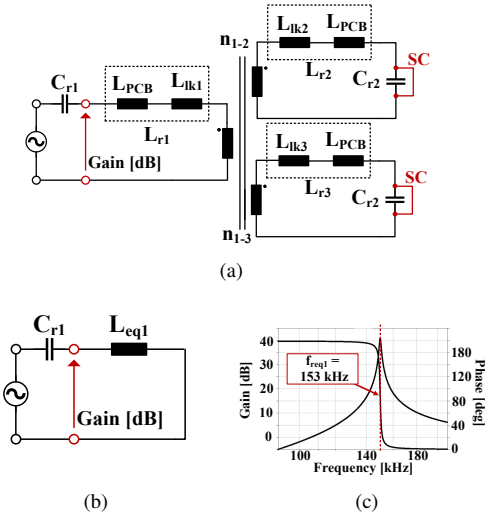


Fig. 10. Resonance frequency matching methodology. (a) Measurement set-up for Port-1: the gain after the resonant capacitor is measured with a Bode analyser. (b) Equivalent circuit of the measurement set-up, where L_{eq1} is the overall resonant inductance seen from Port-1. (c) Measured bode plot and equivalent resonance frequency due to C_{r1} and L_{eq1}.

resonance inductances L_{r1}, L_{r2} and L_{r3} can be calculated by solving the system given in (24). Finally, the resonant capacitors are recalculated to match the desired resonance frequency using (5).

$$L_{eq1} = \frac{1}{(2\pi f_{r,eq1})^2 C_{r1}} \quad L_{eq2} = \frac{1}{(2\pi f_{r,eq2})^2 C_{r2}} \quad L_{eq3} = \frac{1}{(2\pi f_{r,eq3})^2 C_{r3}} \tag{23}$$

$$\begin{aligned} L_{eq1} &= L_{r1} + \left(\frac{1}{n_{12}^2 L_{r2}} + \frac{1}{n_{13}^2 L_{r3}}\right)^{-1} \\ L_{eq2} &= L_{r2} + \left(\frac{n_{12}^2}{L_{r1}} + \frac{1}{n_{23}^2 L_{r3}}\right)^{-1} \\ L_{eq1} &= L_{r1} + \left(\frac{n_{13}^2}{L_{r1}} + \frac{n_{23}^2}{L_{r2}}\right)^{-1} \end{aligned} \tag{24}$$

VI. Implementation of the Converter Prototype and Experimental Results

The TP-SRC prototype was designed for the specifications given in Table I with the GaN MOSFETs specified in Table II. A picture of the prototype is shown in Fig.11. According to the efficiency analysis, the ideal resonance frequency was selected at 140 kHz and the three-winding transformer was constructed following the design analysis presented in section II.B for the selected frequency. The transformer was evaluated with an impedance analyser and the main parameters were extracted. The physical implementation of the transformer and the measured parameters are given in Table III. The resonant capacitors were calculated with the resonance frequency matching methodology given in section V. The resonant tank parameters are given in Table IV. The switching frequency

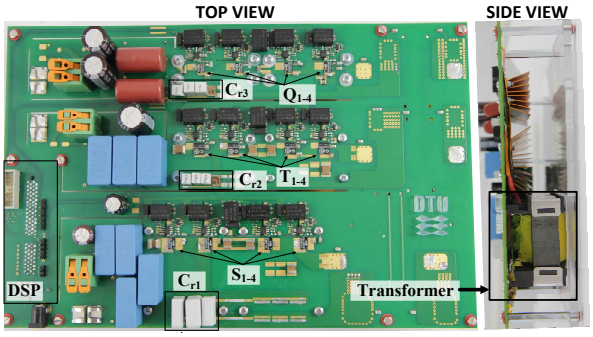


Fig. 11. Picture of the prototype.

TABLE III
Transformer Specifications

Core	No. of turns	Wire	R_{dc}	L_M
ETD	$N_1 = 6$	120 x AWG26	2 mΩ	32.9 µH
59/31/22	$N_2 = 26$	20 x AWG26	38 mΩ	817 µH
	$N_3 = 39$	20 x AWG26	65 mΩ	1.88 mH

was selected at 133 kHz, which is 7 kHz below the resonance frequency, in order to add some safety margin and ensure soft-switching operation. The dead-time utilized was 220 ns, which gives a high efficiency performance for the entire power range according to the analysis carried out in Section V.

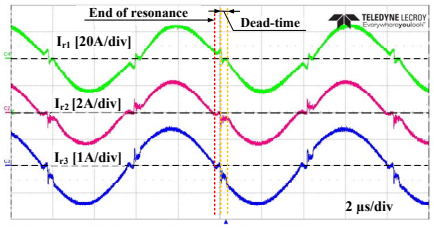
A. Experimental results

The experimental results were obtained with the converter operating in stead-state in dual-output mode with Port-1 ($V_1 = 80$ V) as the input port. The main waveforms obtained are shown in Fig.12. In Fig.12a the resonant currents at the input side (I_{r1}) and output side (I_{r2} and I_{r3}) are presented. It can be observed that the resonance cycle ends before the switching event, where the input side switches turn-off and the dead-time interval begins. The output side currents I_{r2} and I_{r3} become zero before the turn-off event, and therefore the MOSFETs at the output sides operate in ZCS. Fig.12b shows the drain-source voltage and gate source voltage on the MOSFET S_4 at the input side and the resonant current I_{r1}. In Fig.12b ZVS operation and turn-off event with low current I_M can be verified.

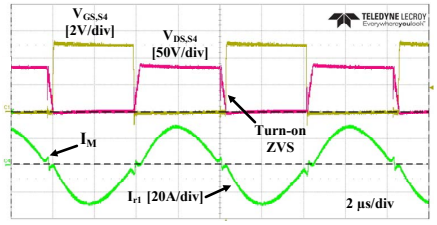
The efficiency curve in function of the output power is shown in Fig.13, while the theoretical losses distribution is presented in Fig.14. The efficiency was measured in dual-output operation with an equal power sharing among output ports. A peak efficiency of 98.8 % was measured at 800 W, while at rated load an efficiency of 98.15 % was measured. From the losses distribution given in Fig.14, it can be observed

TABLE IV
Resonant Tank Parameters

C_{r1}	C_{r2}	C_{r3}	L_{r1}	L_{r2}	L_{r3}
8 µF	1.88 µF	910 nF	161.5 nH	687.4 nH	1.42 µH



(a)



(b)

Fig. 12. Experimental results obtained in steady-state at 1.2 kW in dual-output mode with Port-1 ($V_1 = 80$ V) operating as input. (a) Tank circuit currents, (b) Tank current at input side, drain-source voltage and gate-source voltage of MOSFET S_4.

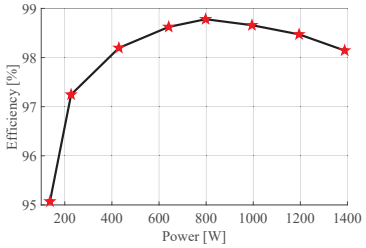


Fig. 13. Efficiency results in dual-output mode with Port-1 ($V_1 = 80$ V) operating as input.

that the MOSFETs at the input side are responsible of 65 % of the total losses, while the MOSFETs at both output sides are responsible for only 5 % of the losses. Such a large difference between the losses at the input side and the output side is due to the relatively large on-resistance of the MOSFETs at Port-1 compared to the other two MOSFETs. In order to decrease the conduction losses at Port-1, GaN MOSFETs with larger current rating should be selected.

VII. Conclusion

The multi port series resonant converter in open-loop operation is a promising topology to be used as a dc-dc statge of SST to interconnect multiple dc grids. In dc distribution systems for distributed energy sources, high efficiency power electronics are highly desired. In this paper, the losses analysis of the main components of TP-SRC has been presented. Then, the effect of the dead-time and resonance frequency to the rms currents and converter losses have been analysed and discussed. To further improve the converter efficiency, GaN MOSFETs with very low output capacitance and on-resistance were used. The resonance inductances of the resonant tank

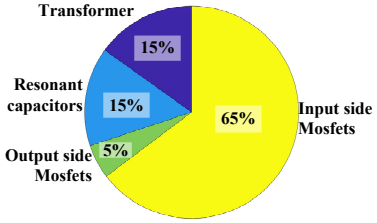


Fig. 14. Losses distribution on the main components of the converter at 1.4 kW.

were integrated into the leakage inductance of the transformer and the PCB parasitic inductances. Because of the fixed switching frequency operation, a resonance frequency matching among the resonant tanks at each side of the transformer is required to operate the TP-SRC at its efficiency-wise optimal operating region. Therefore, a resonance frequency matching methodology was also presented in this paper. Finally, experimental results were provided for a 1.4 kW prototype. The proposed TP-SRC obtained a peak efficiency of 98.8 %.

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Dual Active Bridge DC-DC Converter with Extended Operation Range

Patent application submitted to Europe Patent office, January, 2018.

Dual active bridge DC-DC converter with extended operation range

The present disclosure relates to a dual active bridge DC-DC converter with an extended operation range and to a method for controlling a dual active bridge DC-DC converter to achieve an extended operation range.

Background of invention

Bidirectional DC-DC converters provide the capability of effectively and flexibly regulating reversible DC power flows, making them suitable for use in applications such as renewable energy systems, electrical vehicles and DC microgrids. One bidirectional DC-DC topology which has gained popularity is the dual active bridge (DAB) converter.

The efficiency of DAB converters suffer from large root mean square (RMS) current caused by voltage mismatch between the low voltage side (LVs) and high voltage side (HVs) and phase-shift control introducing reactive power. When voltage amplitudes of the two sides of the transformer of the dual active bridge converter do not match, the difference causes RMS current. A greater mismatch increases the RMS current.

Various techniques for high current applications have been proposed. One method is to use parallel semiconductor devices or converter modular units. However, paralleling switches complicates circuit layout and increases parasitic inductance. Moreover, thicker copper or a parallel structure must be applied to transformer windings resulting in high manufacturing cost and high interwinding capacitance especially for print circuit board (PCB) windings. Paralleling converter modular units also need an additional control scheme to eliminate circulating current between units.

Summary of invention

In the present disclosure a new dual active bridge (DAB) converter is proposed. The problem of large root mean square (RMS) current because of voltage mismatch between the low voltage side (LVs) and high voltage side (HVs) typically become even more severe for high voltage gain high power applications. The proposed DAB converter may therefore be particularly useful for high-power high-voltage-gain applications. The disclosure relates to a partially paralleled DAB configuration, in which AC current balancing between parallel full-bridges is ensured by series connected transformer windings on the high voltage side of the DAB. The present disclosure

therefore relates to a partially paralleled dual active bridge converter, wherein a low-voltage (LV) side parallel and high-voltage (HV) side series topology is configured to achieve high voltage gain while reducing current stress over switching devices and transformer windings on the low voltage high current side of the DAB converter. The configuration is based on an idea of connecting the circuit parts which need to carry high current in parallel and connecting the circuit parts which need to block high voltage in series. Moreover, by regulating the phase shift between the paralleled low voltage active bridge circuits on the low voltage side, the DAB converter may extend the operating range of the DAB converter in terms of output power, which is described in further detail below.

A first embodiment of the present invention therefore relates to a dual active bridge DC-DC converter comprising:

- a low voltage port;
- a high voltage port;
- a set of *n* transformers, each transformer comprising a primary and a secondary winding magnetically coupled to each other;
- a single active high voltage bridge circuit connected between the high voltage port and the set of *n* transformers, wherein the *n* transformers are arranged to operate in series;
- *n* active low voltage active bridge circuits connected in parallel between the set of n transformers and the low voltage port, wherein the *n* transformers are arranged to operate in parallel;
- a control unit configured to control:
    - a first phase-shift angle between one of the *n* active low voltage active bridge circuits and the single active high voltage bridge circuit; and
    - a second phase-shift angle between the *n* active low voltage active bridge circuits, thereby extending an operation range of the dual active bridge DC-DC converter;

wherein *n* is a positive integer number larger than or equal to 2.

Fig. 1 shows an example of such an embodiment. In this embodiment the single active high voltage bridge is a high voltage H-bridge comprising four controllable switches, and the parallel low voltage active bridge circuits are low voltage H-bridges, each low voltage H bridge comprising four controllable switches.

The control unit may control the second shift angle between the parallel low voltage active bridge circuits to modify the power equations of the circuit and thereby extend the operation range of the circuit in terms of power. This means that the control unit may also be operable to adjust the second phase shift angle, and/or use a number of different configurations with different second phase shift angles in order to get a number of different power output curves. By exploiting the different second phase angle configurations, the operation range may be further extended. The presently disclosed dual active bridge DC-DC converter can thus be said to introduce an additional degree of freedom to control output power or voltage.

The first phase shift angle φ may be represented as a percentage of the switching period of the dual active bridge DC-DC converter. The second phase-shift angle φ_p may then be a value between 0 and φ ($0<\varphi_p<\varphi$).

The present disclosure further relates to a method for controlling a dual active bridge DC-DC converter having *n* transformers; a single active high voltage bridge circuit, such as a high voltage H-bridge, connected to a high voltage port, and *n* active low voltage active bridge circuits, such as low voltage H-bridge circuits, connected in parallel to a low voltage port, the method comprising the steps of:

- applying a first pulse width modulated drive signal to the single active high voltage bridge circuit;
- applying a second pulse width modulated drive signal to a first active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the second pulse width modulated drive signal having a first phase-shift angle in relation to the first pulse width modulated drive signal;
- applying a third pulse width modulated drive signal to a second active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the third pulse width modulated drive signal having a second phase-shift angle in relation to the first pulse width modulated drive signal, wherein the second phase-shift angle is less than the first phase-shift angle;

The method may be carried out using any embodiment of the presently disclosed dual active bridge DC-DC converter.

These and other aspects of the invention are set forth in the following detailed description if the invention.

Description of drawings

Fig. 1 shows an example of the presently disclosed dual active bridge DC-DC converter having a single active high voltage bridge circuit and two low voltage active bridge circuits connected in parallel connected to the same low voltage port.

Fig. 2 and 3 show different phase shift modulations for the dual active bridge DC-DC converter.

Fig. 4 shows transferred power as a function of φ at different $\varphi_{p.}$

Fig. 5 (A and B) show average current as a function of φ at different $\varphi_{p.}$

Fig. 6 shows an example of the presently disclosed dual active bridge DC-DC converter having a single active high voltage bridge circuit and more than two low voltage active bridge circuits connected in parallel connected to the same low voltage port

Fig. 7 shows experimental voltage and current waveform comparisons for voltage ($v_{1\_1}+v_{1\_2}$) (Ch1), voltage v_2 (Ch2) and current i_{LAC} (Ch3) with (a) $\varphi_p=0$, (b) $0<\varphi_p<\varphi$ and (c) $\varphi<\varphi_p$ for one embodiment of the presently disclosed dual active bridge DC-DC converter.

Fig. 8 shows experimental voltage and current waveform comparisons for voltage v_{1_1} (Ch1), voltage v_{1_2} (Ch2), current i_1 (Ch3) and current i_2 (Ch4) with (a) $\varphi_p=0$, (b) $0<\varphi_p<\varphi$, and (c) $\varphi_p>\varphi$ for the implementation of fig. 1.The currents i_1 and i_2 are the same regardless the phase-shift angles.

Detailed description of the invention

The present disclosure relates to a dual active bridge DC-DC converter comprising a low voltage port; a high voltage port; one high voltage bridge circuit; a plurality of parallel low voltage active bridge circuits, wherein a plurality of transformers, arranged to operate in series, connect the high voltage bridge circuit with the plurality of parallel low voltage active bridge circuits. Preferably, the dual active bridge DC-DC converter comprises a control unit for controlling phase-shift angles between the high voltage bridge circuit and the plurality of parallel low voltage active bridge circuits, and phase-shift angles between the parallel low voltage active bridge circuits. By regulating the phase shift between the paralleled low voltage active bridge circuits on the low voltage

side, the DAB converter may extend the operating range of the DAB converter in terms of output power. Each transformer may comprise a primary and a secondary winding magnetically coupled to each other by means of for example a transformer core of high magnetic permeability. Preferably, the plurality of transformers are arranged to operate in series, as shown in for example fig. 1, wherein each of the parallel low voltage active bridge circuits are connected to one transformer, and wherein the transformers are connected in series on the high voltage side. Preferably, the control unit is configured to control a first phase-shift angle between one of the *n* active low voltage active bridge circuits, for example a selected reference low voltage active bridge circuit, and the single active high voltage bridge circuit. Fig. 2 shows an example of a first phase-shift angle between a first low voltage active bridge circuit (S1, S2, S3, S4) and the high voltage bridge circuit (S5, S6, S7, S8) based on the topology of fig. 1. In addition to the first phase-shift angle, there is preferably at least one second phase-shift angle internally between the active low voltage active bridge circuits. Fig. 2 shows an example of such a second phase-shift angle between two active low voltage active bridge circuits, (S1, S2, S3, S4), (S1_2, S2_2, S3_2, S4_2) respectively. If the first phase-shift angle is not the same as the second phase-shift angle, the operation range of the dual active bridge DC-DC converter can be extended. Preferably, when using the presently disclosed dual active bridge DC-DC converter, the total current between the low voltage port and the n transformers is split between the *n* active low voltage active bridge circuits.

The single active high voltage bridge circuit may be a high voltage H-bridge comprising four controllable switches, for example S5, S6, S7, S8. The active low voltage active bridge circuits may be low voltage H-bridges, each low voltage H bridge comprising four controllable switches, for example S1, S2, S3, S4 and S1_2, S2_2, S3_2, S4_ 2 and so forth. Examples of H-bridges are shown in fig. 1. Generally, H-bridge refers to a structure derived from a typical graphical representation of an integrated circuit that enables a voltage to be applied across a load in opposite directions. An H-bridge is typically built with four switches as shown in for example fig. 1. When the switches S1 and S4 are closed, and S2 and S3 are open, a positive voltage is applied between the node between S1-2 and the node between S3-4. By opening the S1 and S4 switches and closing the S2 and S3 switches, this voltage is reversed.

The dual active bridge DC-DC converter, in particular the H-bridges of the converter, may operate for example with a switching frequency between 1 kHz and 1 MHz,

preferably between 10 kHz and 500 kHz, more preferably between 50 kHz and 200 kHz. The switching frequency in this regard may refer to the switching of the S1-S8, S1_2-S4_2 as illustrated in fig. 3.

The dual active bridge DC-DC converter may be configured to operate on low voltage (V_1) on the low voltage port that is lower than 100V, preferably lower than 50V, more preferable lower than 40V, even more preferably lower than 25V, most preferably lower than 10V. A high voltage (V_2) on the high voltage port may be for example higher than 100V, preferably higher than 150V, more preferable higher than 200V, even more preferably higher than 300V.

Operation and phase-shift angle management

As stated, the partial parallel configuration may split the high-current loops into two smaller loops with half the total input current, thereby reducing conduction and switching losses.

The basic converter operating waveforms under single phase-shift modulation (first phase-shift angle only) are presented in fig. 2. The converter's steady-state power equation can be derived from:

$$P = \frac{2nV_1V_2}{f_S L_{AC}}\varphi(1-2\varphi)$$

where the phase shift φ is represented as a percentage of the switching period T_s, f_s is the switching frequency and L_{ac} is the sum of the external inductance and the transformer leakage inductance seen from the high-voltage side.

The four controllable switches of each high voltage H-bridge and/or the low voltage H-bridge may form two pairs of switches, wherein the control unit is configured to open and close the two pairs of switches in mutually exclusive configurations, as described. The first phase-shift angle may represent a first shift in time, preferably a predetermined shift in time, between switching of pairs of switches of the high voltage H-bridge and pairs of switches of a first low voltage H-bridge. The first phase-shift angle can be said to determine the shape of the current and voltage on the high voltage side (i_{LAC}, v_{LAC}). An example is shown in fig. 2.

In addition to the first phase-shift angle, the present disclosure proposes a second phase-shift angle between the low voltage active bridge circuits. The second phase-shift angle may represent a second shift in time, preferably a predetermined second shift in time, between switching of corresponding pairs of switches a first low voltage H-bridge and a second low voltage H-bridge. An example of such a second phase-shift angle is shown in fig. 3, wherein the phase-shift angle between the first low voltage H-bridge and the second low voltage H-bridge is different than the phase-shift angle between the first low voltage H-bridge and the high voltage H-bridge.

Regulating the phase shift between the two paralleled active bridges gives an additional degree of freedom to control output power or voltage. Fig. 3 shows an example of a switching pattern and the typical AC inductor current and voltage waveforms when the second phase shift φ_p is inserted. In one embodiment the second phase-shift angle is less than the first phase-shift angle. This may be represented by $0<\varphi_p<\varphi$.

Based on the waveforms in the example of fig. 3, I_1, I_2 and I_3 can be calculated accordingly in.

$$I_1 = \frac{(4\varphi - 2\varphi_p - 1)2nV_1 + V_2)}{4f_S L_{ac}}$$

$$I_2 = \frac{(1 - 2\varphi_p)2nV_1 + (4\varphi - 1)V_2)}{4f_S L_{ac}}$$

$$I_3 = \frac{(1 - 2\varphi_p)2nV_1 + (4\varphi - 4\varphi_p - 1)V_2)}{4f_S L_{ac}}$$

By using the mean-value theorem, the power equation for dual active bridge DC-DC converter with φ and φ_p as the control parameters is expressed can be expressed as:

$$P = \frac{2nV_1V_2}{f_S L_{ac}}\varphi(1 - 2\varphi + 2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi} \qquad (0<\varphi_p \leq \varphi)$$

In comparison with the single phase-shift modulation it has an additional term

$$2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi}$$

Similarly, the power equation for $\varphi < \varphi_p < 0.25$ is can be expressed as:

$$P = \frac{4nV_1V_2}{f_S L_{ac}}(\varphi - \frac{\varphi_p}{2})(\frac{1}{2} - \varphi_p) \qquad (0 < \varphi_p \leq 0.25)$$

Therefore, in one embodiment of the presently disclosed dual active bridge DC-DC converter, the generated power of the converter is expressed as:

$$P = \frac{2nV_1V_2}{f_S L_{ac}}\varphi(1 - 2\varphi + 2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi}$$

wherein V_1 is the input voltage, V_2 is the output voltage, f_s is the switching frequency, L_{AC} is the sum of external inductance, φ is the first phase-shift angle, and φ_p is the second phase-shift angle.

Examples of the power as a function of φ and φ_p are shown and compared against single phase-shift modulation ($\varphi = \varphi_p$) in fig. 4. In one embodiment of the presently disclosed dual active bridge DC-DC converter, the control unit is configured to control the second phase-shift angle dynamically to regulate a generated power of the dual active bridge DC-DC converter to optimize the transferred power. Moreover, the control of the second phase-shift may be based on a relation between an input voltage on the low voltage port and an output voltage on the output voltage port. The control unit may be configured to control the second phase-shift angle to regulate an output voltage and/or power and/or current, such as a steady-state power, of the dual active bridge DC-DC converter.

By regulating the second phase-shift angle (φ_p) an unequal power distribution, and/or an unequal current distribution between the parallel low voltage active bridge circuits can be achieved. When $0 < \varphi_p < \varphi$, the average input currents I_{in1_avg} and I_{in2_avg} in the parallel low voltage active bridge circuits can be calculated as follows:

$$I_{in1\_avg} = \frac{n^2V_1}{f_S L_{ac}}[2m\varphi(1 - 2\varphi) + \varphi_p(2\varphi_p - 1)]$$

$$I_{in2\_avg} = \frac{n^2 V_1}{f_S L_{ac}} [2m(\varphi - \varphi_p)(1 - 2\varphi + 2\varphi_p) + \varphi_p(1 - 2\varphi_p)]$$

where

$$m = \frac{V_2}{2nV_1}$$

It follows that the current distribution between the two paralleled bridges depends on the phase-shift angles φ and φ_p and m. Fig. 5 shows the ratios of the average currents I_{in1_avg} and I_{in2_avg} against $n^2 \cdot V_1/f_s/L_{ac}$ as a function of φ. The dashed line and solid line represent I_{in1_avg} and I_{in2_avg} respectively. Fig. 5A shows the average current as a function of φ at different φ_p when $m = 1$ and 5B shows the same when $m \neq 1$.

Despite the possible unequal distribution of current, the series winding connection of the transformers may constrain the RMS currents to be equal in all the semiconductor switches on the low voltage side.

$$I_{S1\sim S4\_rms} = I_{S1\_2\sim S4\_2\_rms}$$

Topology details

Fig. 1 shows an example of the presently disclosed dual active bridge DC-DC converter having a single active high voltage bridge circuit and two low voltage active bridge circuits connected in parallel connected to the same low voltage port.

Preferably the plurality of active low voltage active bridge circuits is connected to the same low voltage port. The active high voltage bridge circuit may comprise four controllable semiconductor switches (S5, S6, S7, and S8) in an H-bridge configuration, wherein a first output of the plurality transformers is connected to a node between S5 and S6, and wherein a second output of the plurality of transformers is connected to a node between S7 and S8. An inductor may be placed between the first output of the plurality transformers and the node between S5 and S6. The outputs of S5 and S7 of the high voltage H-bridge are preferably connected to a first high voltage terminal of the high voltage port. Similarly, the outputs of S6 and S8 may be connected to a second high voltage terminal of the high voltage port.

On the low voltage side, the first low voltage H-bridge may comprise four controllable semiconductor switches S1, S2, S3, and S4 in an H-bridge configuration. In this

configuration a node between S1 and S2 may be connected to one side of the primary winding (i.e. the low voltage side of the transformer) of a first transformer. A node between S3 and S4 may be connected to another side of the primary winding of the first transformer. The inputs of S1 and S3 may be connected to a first low voltage terminal of the low voltage port, and the inputs of S2 and S4 connected to a second low voltage terminal of the low voltage port. This configuration results in that the first transformer is connected to the low voltage port through the first active low voltage active bridge circuits.

In one embodiment of the presently disclosed dual active bridge DC-DC converter, the second low voltage active bridge circuit is a second low voltage H-bridge which comprises four controllable semiconductor switches S1_2, S2_2, S3_2, and S4_4 in an H-bridge configuration. A node between S1_2 and S2_2 may be connected to one side of the primary winding (i.e. the low voltage side of the transformer) of a second transformer, and a node between S3_2 and S4_2 to connected to the other side of the primary winding of the second transformer. The inputs of S1_2 and S3_2 may be connected to a first low voltage terminal of the low voltage port, and the inputs of S2_2 and S4_2 connected to a second low voltage terminal of the low voltage port. This configuration results in that the second transformer is connected to the low voltage port through the second active low voltage active bridge circuits.

The first and second active low voltage active bridge circuits may thereby be seen as parallel, whereas the secondary windings of the transformers are serially connected, wherein the ends of the chain formed by the secondary windings are connected to the connection nodes of the high voltage active bridge circuits.

The presently disclosed concept of a partially paralleled dual active bridge converter can be extended to a higher number of parallel transformers and low voltage active bridge circuits. In one embodiment the dual active bridge DC-DC converter therefore comprises:

- a set of *n* transformers, each transformer comprising a primary and a secondary winding magnetically coupled to each other;
- a single active high voltage bridge circuit connected between the high voltage port and the set of *n* transformers, wherein the *n* transformers are arranged to operate in series;

- *n* active low voltage active bridge circuits connected in parallel between the set of n transformers and the low voltage port, wherein the *n* transformers are arranged to operate in parallel;

wherein *n* is a positive integer number larger than or equal to 3, or larger than 4, or larger than 5. The controllable number of shift angles between the first active low voltage active bridge circuits and the second/third/fourth (etc.) active low voltage active bridge circuits may therefore be *n*-1. The extended number of parallel active low voltage active bridge circuits is shown in fig. 6.

Method for controlling a dual active bridge DC-DC converter

The present disclosure further relates to a method for controlling a dual active bridge DC-DC converter. The dual active bridge DC-DC converter may be any embodiment of the presently disclosed dual active bridge DC-DC converter. Preferably the DAB DC converter has *n* transformers; a single active high voltage bridge circuit, such as a high voltage H-bridge, connected to a high voltage port, and *n* active low voltage active bridge circuits, such as low voltage H-bridge circuits, connected in parallel to a low voltage port.

In a first embodiment the method for controlling a dual active bridge DC-DC converter comprises the steps of:

- applying a first pulse width modulated drive signal to the single active high voltage bridge circuit;
- applying a second pulse width modulated drive signal to a first active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the second pulse width modulated drive signal having a first phase-shift angle in relation to the first pulse width modulated drive signal;
- applying a third pulse width modulated drive signal to a second active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the third pulse width modulated drive signal having a second phase-shift angle in relation to the first pulse width modulated drive signal, wherein the second phase-shift angle is less than the first phase-shift angle.

The first phase shift angle may be represented by φ as a percentage of the switching period T_s. The second phase-shift angle may be represented by $\varphi_{p..}$ The first phase

shift angle and the second phase-shift angle may have the relationship ($0<\varphi_p\leq\varphi$). As can be seen from for example fig. 3, the inventors have realized that a partially parallel implementation combined with individual control of the parallel low voltage active bridge circuits can be used to shape and balance power and/or current differently, which may be particularly useful and high voltage and/or high power applications. The opearting range of the dual active bridge DC-DC converter may be extended by applying different second phase angles. The second phase angle may be controlled dynamically.

In one embodiment the second phase-shift angle is chosen for distributing power over the *n* active low voltage active bridge circuits, optionally for distributing the power unequally over the *n* active low voltage active bridge circuits. One way of selecting the second phase shift angle is based on an input and output voltage relation of the dual active bridge DC-DC converter. This may also involve the step of adapting the combined effect of the first phase-shift angle and the second phase-shift angle to regulate a load power of the dual active bridge DC-DC converter.

As described above, the single active high voltage bridge circuit may comprise a high voltage H-bridge and each active low voltage active bridge circuit may comprise a low voltage H-bridge circuit. The four controllable switches of each high voltage H-bridge and/or the low voltage H-bridge may form two pairs of switches. The first and second pulse width modulated drive signals may therefore, accordingly, be switching signals for the pairs of switches of H-bridge circuits.

Detailed description of drawings

The invention will in the following be described in greater detail with reference to the accompanying drawings. The drawings are exemplary and are intended to illustrate some of the features of the presently disclosed dual active bridge DC-DC converter and method for controlling a dual active bridge DC-DC converter, and are not to be construed as limiting to the presently disclosed invention.

Fig. 1 shows an example of the presently disclosed dual active bridge DC-DC converter (1) having a single active high voltage bridge circuit (9) and two low voltage active bridge circuits (10, 11) connected in parallel connected to the same low voltage port V_1 (2) having a positive terminal (+) (5) and a negative terminal (-) (6). The single active high voltage bridge circuit (9) is connected to a high voltage port V_2 (3) having a

positive terminal (+) (7) and a negative terminal (-) (8). In this example there are two parallel low voltage active bridge circuits (10, 11) and two transformers (4). A control unit (13) controls the phase angles between the low voltage and high voltage side and between the two low voltage active bridge circuits (10, 11). The low voltage port V_1 (2) has a capacitor C_1 (2) and the high voltage port V_2 (3) has a capacitor C_2 (3). In the example of fig. 1, the high voltage bridge circuits (9, 10, 11) are implemented as H-bridges, each H-bridge having four controllable switches, (S1, S2, S3, S4), (S1_2, S2_2, S3_2, S4_2) respectively.

Fig. 3 shows an example of a configuration, wherein a first phase-shift angle has been introduced between one of the low voltage active bridge circuits and the high voltage active bridge circuit (φ, shift between S1/S4 and S5/S8, then between S2/S3 and S6/S7 etc.). In addition to the first phase-shift angle φ there is a second phase-shift angle φ_p between the low voltage active bridge circuits (φ_p, shift between S1/S4 and S1_2/S4_2, then between S2/S3 and S2_2/S2_4 etc.). The additional phase-shift has, as can be seen in the figure, an impact on the current (i_{LAC}) and voltage (v_{LAC}) of the dual active bridge DC-DC converter.

Fig. 6 shows an example of the presently disclosed dual active bridge DC-DC converter having a single active high voltage bridge circuit (9) and more than two low voltage active bridge circuits (10, 11A, 11B) connected in parallel connected to the same low voltage port. The n transformers are connected in series. The extension of the concept into further parallel low voltage active bridge circuits allows for combinations of addition internal phase-shift angles between the low voltage active bridge circuits. In the example of fig. 6 two such phase-shift angles (φ_{p1} and φ_{pn-1}) are shown.

Fig. 7-8 show experimental voltage and current waveform comparisons for voltage ($v_{1\_1}+v_{1\_2}$) (Ch1), voltage v_2 (Ch2) and current i_{LAC} (Ch3) with (a) $\varphi_p=0$, (b) $0<\varphi_p<\varphi$ and (c) $\varphi<\varphi_p$ for one embodiment of the presently disclosed dual active bridge DC-DC converter. In fig. 7 (a) $\varphi=0.034$ and $\varphi_p=0$, (b) $\varphi=0.08$ and $\varphi_p=0.06$, and (c) $\varphi=0.04$ and $\varphi_p=0.05$. When $\varphi_p\neq 0$, the voltage across the series connected high-voltage windings, i.e. $n\cdot(v_{1\_1}+v_{1\_2})$ becomes a three-level waveform consisting of $\pm 2nV_1$ and 0, which changes the current waveforms accordingly. Fig. 8 illustrates the effect of φ_p on the low voltage side. Fig. 8 shows experimental voltage and current waveform comparisons for voltage v_{1_1} (Ch1), voltage v_{1_2} (Ch2), current i_1 (Ch3) and current i_2 (Ch4) with (a)

φ_p=0, (b) 0<φ_p<φ, and (c) φ_p>φ for the implementation of fig. 1.The currents i_1 and i_2 are the same regardless the phase-shift angles. Moreover, as can be seen, L_{ac} causes the AC current to lag behind the AC voltage, which introduces reactive power and leads to extra conduction losses. The larger the phase shift, the higher the loss. However, in this scenario, regulating φ_p is able to delay the AC voltage v_{1_1}, so that the effective phase-shift angle between v_{1_1} and i_1 is reduced, as highlighted in Fig. 8 (b) and (c) with the dashed lines, and the reactive power decreases. This also explains why the input currents i_{in1} and i_{in2} have different average values.

Further details of the invention

1. A dual active bridge DC-DC converter comprising:
    - a low voltage port;
    - a high voltage port;
    - a set of *n* transformers, each transformer comprising a primary and a secondary winding magnetically coupled to each other;
    - a single active high voltage bridge circuit connected between the high voltage port and the set of *n* transformers, wherein the *n* transformers are arranged to operate in series;
    - *n* active low voltage active bridge circuits connected in parallel between the set of n transformers and the low voltage port, wherein the *n* transformers are arranged to operate in parallel;
    - a control unit configured to control:
        - a first phase-shift angle between one of the *n* active low voltage active bridge circuits and the single active high voltage bridge circuit; and
        - a second phase-shift angle between the *n* active low voltage active bridge circuits, thereby extending an operation range of the dual active bridge DC-DC converter;

    wherein *n* is a positive integer number larger than or equal to 2.

2. The dual active bridge DC-DC converter according to any of the preceding items, wherein the single active high voltage bridge circuit is a high voltage H-bridge comprising four controllable switches, and wherein the *n* active low voltage active bridge circuits are low voltage H-bridges, each low voltage H bridge comprising four controllable switches.

3. The dual active bridge DC-DC converter according to item 2, wherein the four controllable switches of each high voltage H-bridge and/or the low voltage H-bridge form two pairs of switches, and wherein the control unit is configured to open and close the two pairs of switches in mutually exclusive configurations.

4. The dual active bridge DC-DC converter according to item 3, wherein the first phase-shift angle represents a first predetermined shift in time between switching of pairs of switches of the high voltage H-bridge and pairs of switches of a first low voltage H-bridge.

5. The dual active bridge DC-DC converter according to any of the preceding items, wherein the second phase-shift angle represents a second predetermined shift in time between switching of corresponding pairs of switches a first low voltage H-bridge and a second low voltage H-bridge.

6. The dual active bridge DC-DC converter according to any of items 2-5, wherein the H-bridges are switched with a switching frequency between 1 kHz and 1 MHz, preferably between 10 kHz and 500 kHz, more preferably between 50 kHz and 200 kHz.

7. The dual active bridge DC-DC converter according to any of the preceding items, wherein the second phase-shift angle is less than the first phase-shift angle.

8. The dual active bridge DC-DC converter according to any of the preceding items, wherein the control unit is configured to control the second phase-shift based on a relation between an input voltage on the low voltage port and an output voltage on the output voltage port.

9. The dual active bridge DC-DC converter according to any of the preceding items, said converter being adapted to operate on a low voltage on the low voltage port, said low voltage lower than 100V, preferably lower than 50V, more preferable lower than 40V, even more preferably lower than 25V, most preferably lower than 10V.

10. The dual active bridge DC-DC converter according to any of the preceding items, said converter being adapted to operate on a high voltage on the high voltage port, said high voltage higher than 100V, preferably higher than 150V, more preferable higher than 200V, even more preferably higher than 300V.

11. The dual active bridge DC-DC converter according to any of the preceding items, wherein the control unit is configured to control the second phase-shift angle dynamically to regulate a generated power of the dual active bridge DC-DC converter.

12. The dual active bridge DC-DC converter according to item 11, wherein the generated power of the converter is expressed as $P = \frac{2nV_1V_2}{f_s L_{ac}} \varphi \left(1 - 2\varphi + 2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p{}^2}{\varphi} \right)$, wherein V_1 is the input voltage, V_2 is the output voltage, f_s is the switching frequency, L_{AC} is the sum of external inductance, φ is the first phase-shift angle, and φ_p is the second phase-shift angle.

13. The dual active bridge DC-DC converter according to any of the preceding items, wherein the control unit is configured to control the second phase-shift angle to regulate an output voltage and/or power, such as a steady-state power, of the dual active bridge DC-DC converter.

14. The dual active bridge DC-DC converter according to any of the preceding items, wherein the *n* active low voltage active bridge circuits are connected to the same low voltage port.

15. The dual active bridge DC-DC converter according to any of the preceding items, wherein the active high voltage bridge circuit comprises four controllable semiconductor switches S5, S6, S7, and S8 in an H-bridge configuration, wherein a first output of the *n* transformers is connected to a node between S5 and S6, and wherein a second output of the *n* transformers is connected to a node between S7 and S8.

16. The dual active bridge DC-DC converter according to item 15, wherein outputs of S5 and S7 are connected to a first high voltage terminal of the high voltage port, and wherein outputs of S6 and S8 are connected to a second high voltage terminal of the high voltage port.

17. The dual active bridge DC-DC converter according to any of the preceding items, wherein a first low voltage H-bridge comprises four controllable semiconductor switches S1, S2, S3, and S4 in an H-bridge configuration, wherein a node between S1 and S2 is connected to one side of the primary winding of a first transformer, and a node between S3 and S4 is connected to another side of the primary winding of the first transformer.

18. The dual active bridge DC-DC converter according to item 17, wherein inputs of S1 and S3 are connected to a first low voltage terminal of the low voltage port, and wherein inputs of S2 and S4 are connected to a second low voltage terminal of the low voltage port.

19. The dual active bridge DC-DC converter according to any of the preceding items, wherein a second low voltage H-bridge comprises four controllable semiconductor switches S1_2, S2_2, S3_2, and S4_4 in an H-bridge configuration, wherein a node between S1_2 and S2_2 is connected to one side of the primary winding of a second transformer, and a node between S3_2 and S4_2 is connected to another side of the primary winding of the second transformer.

20. The dual active bridge DC-DC converter according to item 19, wherein inputs of S1_2 and S3_2 are connected to the first low voltage terminal of the low voltage port, and wherein inputs of S2_2 and S4_2 are connected to the second low voltage terminal of the low voltage port.

21. The dual active bridge DC-DC converter according to any of the preceding items, wherein a total current between the low voltage port and the n transformers is split between the *n* active low voltage active bridge circuits.

22. A method for controlling a dual active bridge DC-DC converter having *n* transformers; a single active high voltage bridge circuit, such as a high voltage

H-bridge, connected to a high voltage port, and *n* active low voltage active bridge circuits, such as low voltage H-bridge circuits, connected in parallel to a low voltage port, the method comprising the steps of:

- applying a first pulse width modulated drive signal to the single active high voltage bridge circuit;
- applying a second pulse width modulated drive signal to a first active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the second pulse width modulated drive signal having a first phase-shift angle in relation to the first pulse width modulated drive signal;
- applying a third pulse width modulated drive signal to a second active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the third pulse width modulated drive signal having a second phase-shift angle in relation to the first pulse width modulated drive signal, wherein the second phase-shift angle is less than the first phase-shift angle.

23. The method for controlling a dual active bridge DC-DC converter according to item 22, wherein the second phase-shift angle is chosen for distributing power over the *n* active low voltage active bridge circuits, optionally distributing the power unequally over the *n* active low voltage active bridge circuits.

24. The method for controlling a dual active bridge DC-DC converter according to any of items 22-23, wherein the second phase-shift angle is chosen based on an input and output voltage relation of the dual active bridge DC-DC converter.

25. The method for controlling a dual active bridge DC-DC converter according to any of items 22-24, further comprising the step of adjusting the first phase-shift angle and the second phase-shift angle to regulate a load power of the dual active bridge DC-DC converter.

26. The method for controlling a dual active bridge DC-DC converter according to any of items 22-25, wherein the first and second pulse width modulated drive signals are switching signals for pairs of switches of H-bridge circuits.

27. The method for controlling a dual active bridge DC-DC converter according to any of items 22-26, wherein the dual active bridge DC-DC converter is the converter of any of items 1-21.

28. The method for controlling a dual active bridge DC-DC converter according to any of items 22-27, further comprising the step of providing the dual active bridge DC-DC converter of any of items 1-21.

Claims

1. A dual active bridge DC-DC converter comprising:
    - a low voltage port;
    - a high voltage port;
    - a set of *n* transformers, each transformer comprising a primary and a secondary winding magnetically coupled to each other;
    - a single active high voltage bridge circuit connected between the high voltage port and the set of *n* transformers, wherein the *n* transformers are arranged to operate in series;
    - *n* active low voltage active bridge circuits connected in parallel between the set of n transformers and the low voltage port, wherein the *n* transformers are arranged to operate in parallel;
    - a control unit configured to control:
        - a first phase-shift angle between one of the *n* active low voltage active bridge circuits and the single active high voltage bridge circuit; and
        - a second phase-shift angle between the *n* active low voltage active bridge circuits, thereby extending an operation range of the dual active bridge DC-DC converter;

    wherein *n* is a positive integer number larger than or equal to 2.

2. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the single active high voltage bridge circuit is a high voltage H-bridge comprising four controllable switches, and wherein the *n* active low voltage active bridge circuits are low voltage H-bridges, each low voltage H bridge comprising four controllable switches.

3. The dual active bridge DC-DC converter according to claim 2, wherein the four controllable switches of each high voltage H-bridge and/or the low voltage H-bridge form two pairs of switches, and wherein the control unit is configured to open and close the two pairs of switches in mutually exclusive configurations.

4. The dual active bridge DC-DC converter according to claim 3, wherein the first phase-shift angle represents a first predetermined shift in time between switching of pairs of switches of the high voltage H-bridge and pairs of switches

of a first low voltage H-bridge and the second phase-shift angle represents a second predetermined shift in time between switching of corresponding pairs of switches a first low voltage H-bridge and a second low voltage H-bridge.

5. The dual active bridge DC-DC converter according to any of claims 2-4, wherein the H-bridges are switched with a switching frequency between 1 kHz and 1 MHz, preferably between 10 kHz and 500 kHz, more preferably between 50 kHz and 200 kHz.

6. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the second phase-shift angle is less than the first phase-shift angle.

7. The dual active bridge DC-DC converter according to any of the preceding claims, said converter being adapted to operate on a low voltage on the low voltage port, said low voltage lower than 100V, preferably lower than 50V, more preferable lower than 40V, even more preferably lower than 25V, most preferably lower than 10V.

8. The dual active bridge DC-DC converter according to any of the preceding claims, said converter being adapted to operate on a high voltage on the high voltage port, said high voltage higher than 100V, preferably higher than 150V, more preferable higher than 200V, even more preferably higher than 300V.

9. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the control unit is configured to control the second phase-shift angle dynamically to regulate a generated power of the dual active bridge DC-DC converter.

10. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the control unit is configured to control the second phase-shift angle to regulate an output voltage and/or power, such as a steady-state power, of the dual active bridge DC-DC converter.

11. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the *n* active low voltage active bridge circuits are connected to the same low voltage port.

12. The dual active bridge DC-DC converter according to any of the preceding claims, wherein the active high voltage bridge circuit comprises four controllable semiconductor switches S5, S6, S7, and S8 in an H-bridge configuration, wherein a first output of the *n* transformers is connected to a node between S5 and S6, and wherein a second output of the *n* transformers is connected to a node between S7 and S8, and wherein a first low voltage H-bridge comprises four controllable semiconductor switches S1, S2, S3, and S4 in an H-bridge configuration, wherein a node between S1 and S2 is connected to one side of the primary winding of a first transformer, and a node between S3 and S4 is connected to another side of the primary winding of the first transformer, and wherein a second low voltage H-bridge comprises four controllable semiconductor switches S1_2, S2_2, S3_2, and S4_4 in an H-bridge configuration, wherein a node between S1_2 and S2_2 is connected to one side of the primary winding of a second transformer, and a node between S3_2 and S4_2 is connected to another side of the primary winding of the second transformer.

13. The dual active bridge DC-DC converter according to any of the preceding claims, wherein a total current between the low voltage port and the n transformers is split between the *n* active low voltage active bridge circuits.

14. A method for controlling a dual active bridge DC-DC converter having *n* transformers; a single active high voltage bridge circuit, such as a high voltage H-bridge, connected to a high voltage port, and *n* active low voltage active bridge circuits, such as low voltage H-bridge circuits, connected in parallel to a low voltage port, the method comprising the steps of:
    - applying a first pulse width modulated drive signal to the single active high voltage bridge circuit;
    - applying a second pulse width modulated drive signal to a first active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the second pulse width modulated drive signal having a first

phase-shift angle in relation to the first pulse width modulated drive signal;

- applying a third pulse width modulated drive signal to a second active low voltage active bridge circuit of the *n* active low voltage active bridge circuits, the third pulse width modulated drive signal having a second phase-shift angle in relation to the first pulse width modulated drive signal, wherein the second phase-shift angle is less than the first phase-shift angle.

15. The method for controlling a dual active bridge DC-DC converter according to claim 14, wherein the dual active bridge DC-DC converter is the converter of any of claims 1-13.

Abstract

The present disclosure relates to a dual active bridge DC-DC converter comprising a low voltage port; a high voltage port; a set of *n* transformers, each transformer comprising a primary and a secondary winding magnetically coupled to each other; a single active high voltage bridge circuit connected between the high voltage port and the set of *n* transformers, wherein the *n* transformers are arranged to operate in series; *n* active low voltage active bridge circuits connected in parallel between the set of n transformers and the low voltage port, wherein the *n* transformers are arranged to operate in parallel; a control unit configured to control: a first phase-shift angle between one of the *n* active low voltage active bridge circuits and the single active high voltage bridge circuit; and a second phase-shift angle between the *n* active low voltage active bridge circuits, thereby extending an operation range of the dual active bridge DC-DC converter; wherein *n* is a positive integer number larger than or equal to 2.

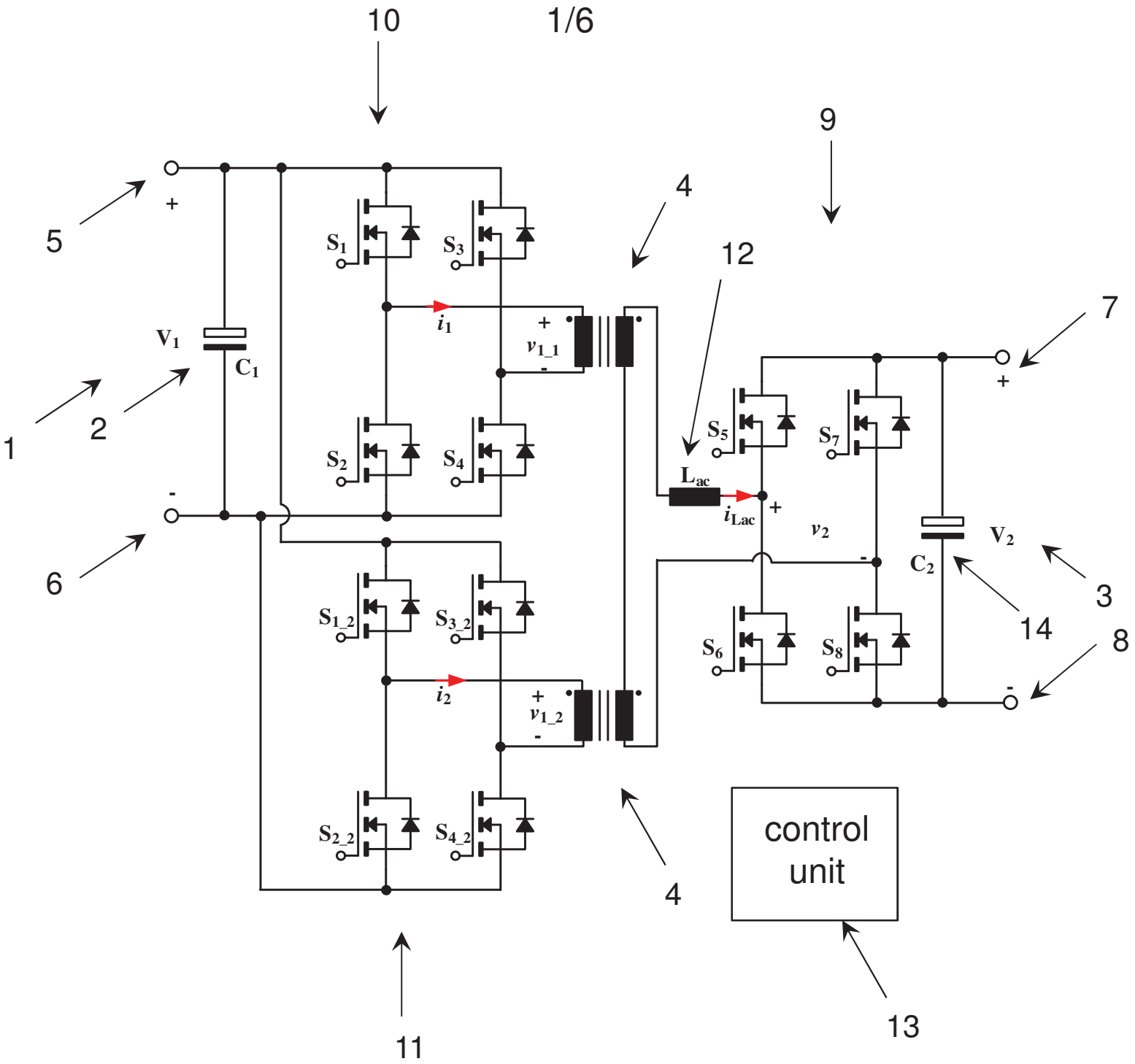
10
9
5
4
12
7
1
2
6
3
14
8
11
4
13
+
-
V_1
C_1
S_1
S_3
S_2
S_4
i_1
v_{1_1}
S_{1_2}
S_{3_2}
S_{2_2}
S_{4_2}
i_2
v_{1_2}
L_{ac}
i_{Lac}
S_5
S_7
S_6
S_8
v_2
V_2
C_2
control unit

FIG. 1

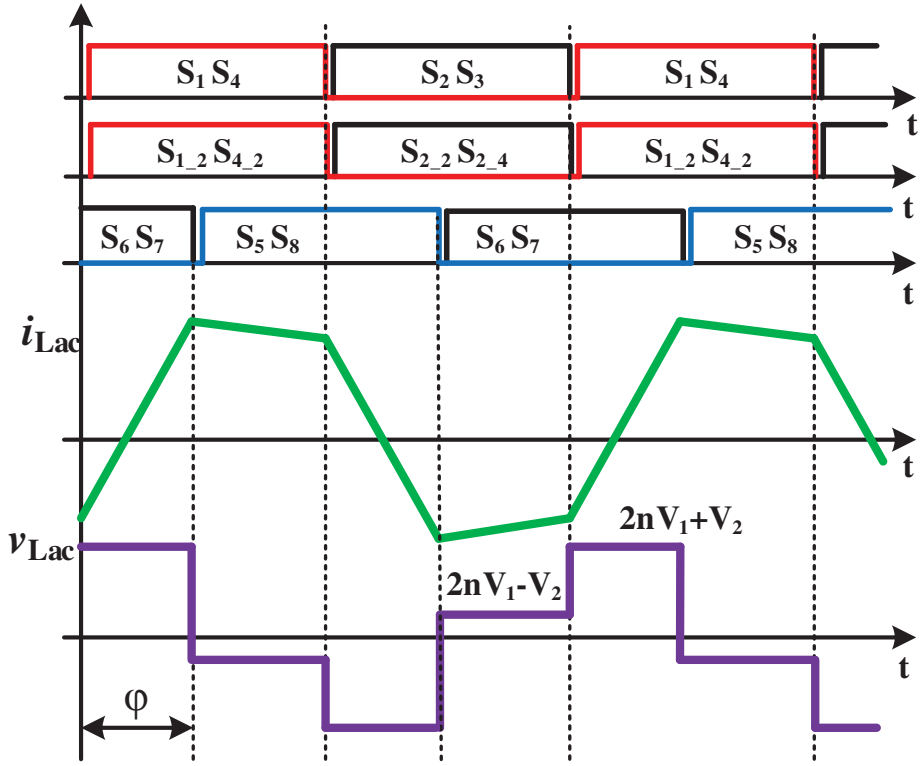
S1 S4
S2 S3
S1 S4
t
S1_2 S4_2
S2_2 S2_4
S1_2 S4_2
t
S6 S7
S5 S8
S6 S7
S5 S8
t
iLac
t
2nV1+V2
vLac
2nV1-V2
t
φ

FIG. 2

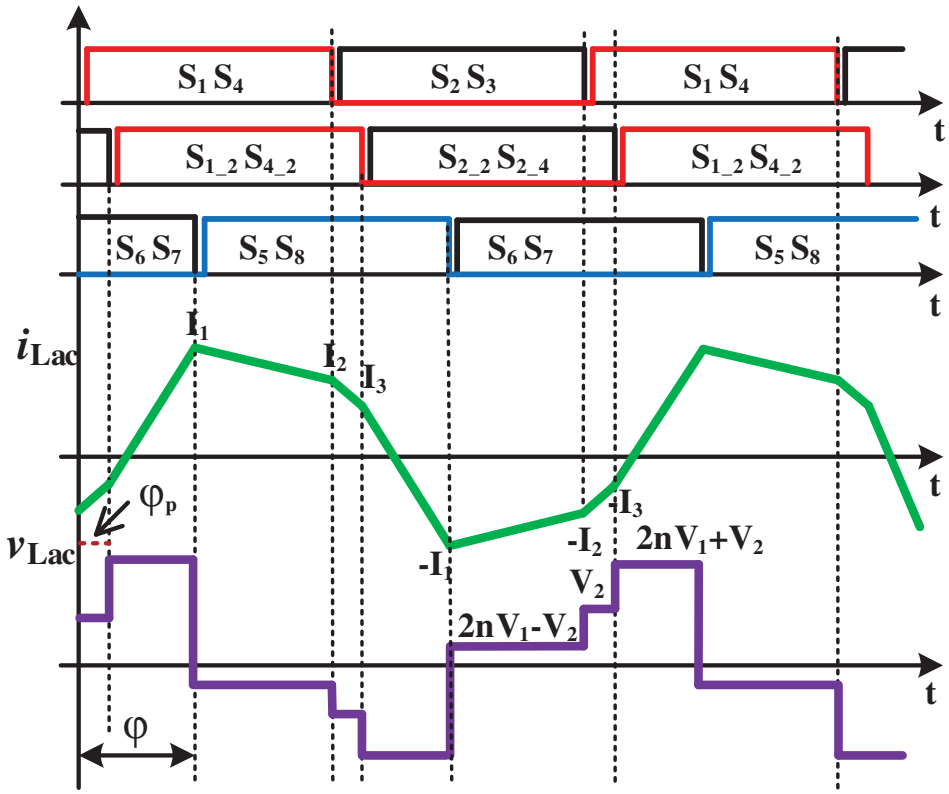
S1 S4
S2 S3
S1 S4
t
S1_2 S4_2
S2_2 S2_4
S1_2 S4_2
t
S6 S7
S5 S8
S6 S7
S5 S8
t
iLac
I1
I2
I3
t
φp
-I3
vLac
-I2
2nV1+V2
-I1
V2
2nV1-V2
t
φ

FIG. 3

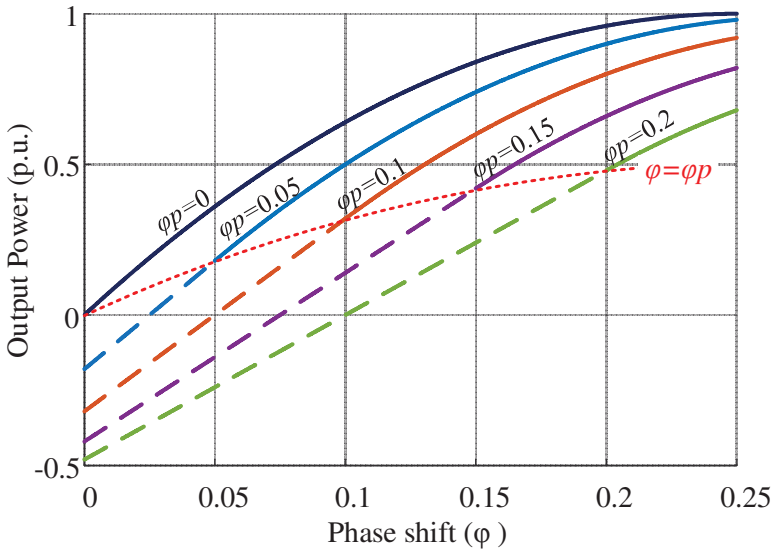

FIG. 4

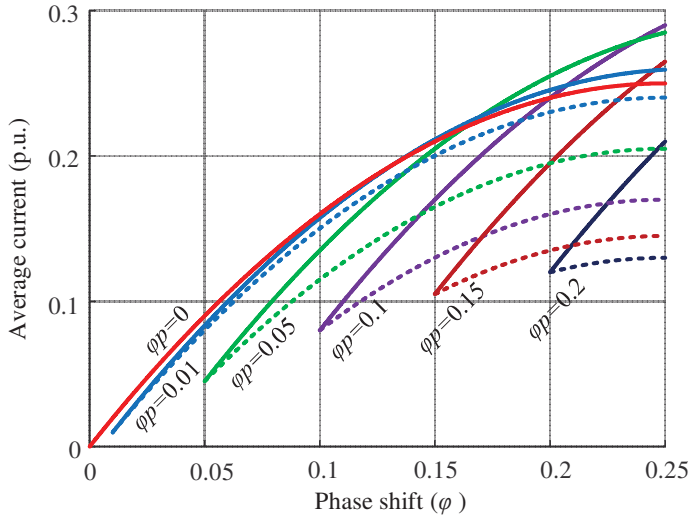

FIG. 5A

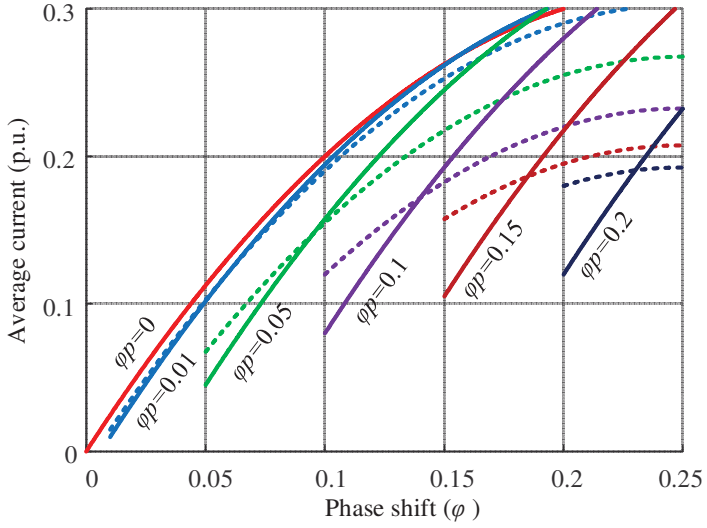

FIG. 5B

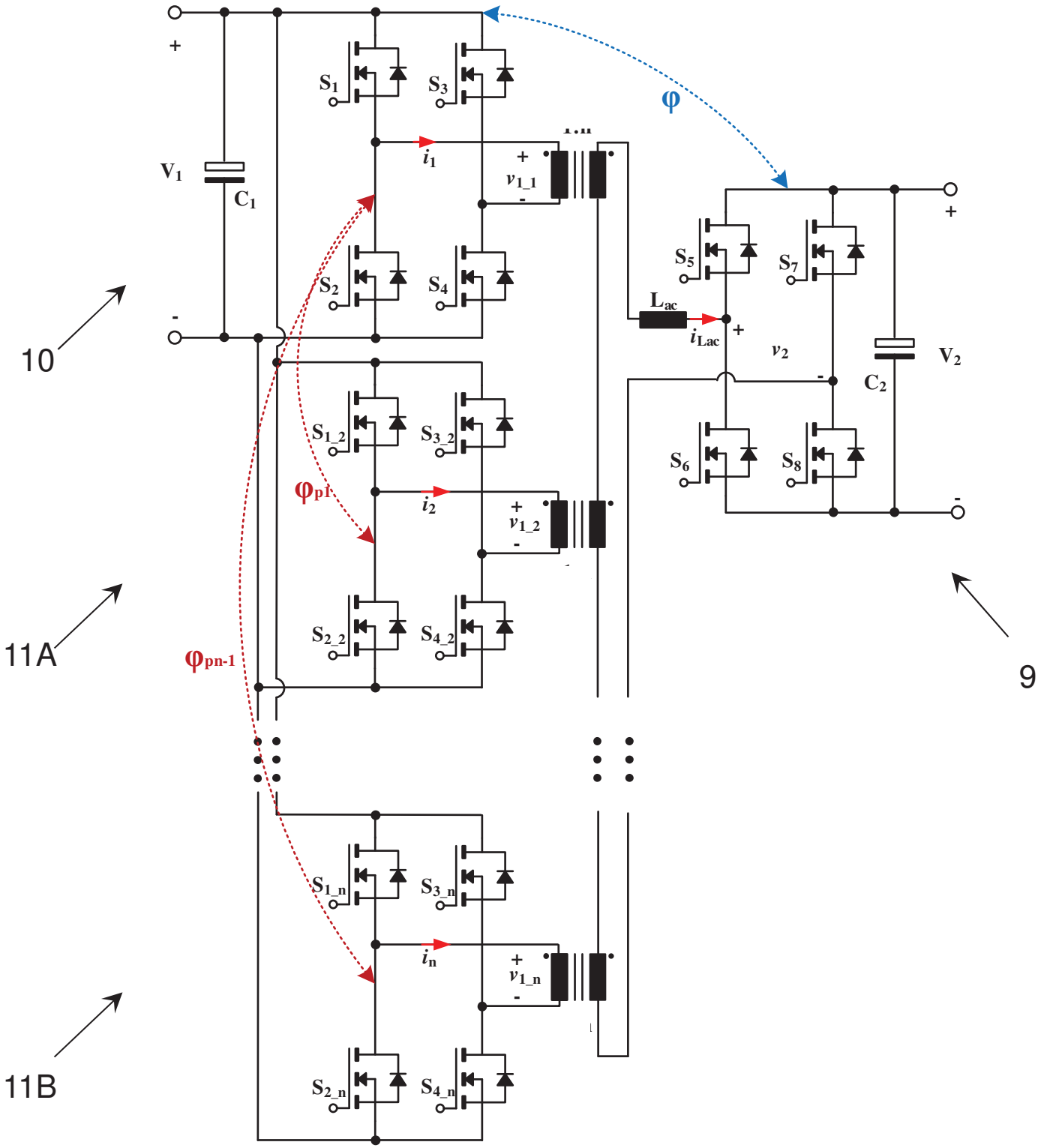
10
11A
11B
9
φ
φpi
φpn-1
V1
C1
S1
S3
S2
S4
i1
v1_1
S1_2
S3_2
S2_2
S4_2
i2
v1_2
S1_n
S3_n
S2_n
S4_n
in
v1_n
Lac
iLac
S5
S7
S6
S8
v2
C2
V2

FIG. 6

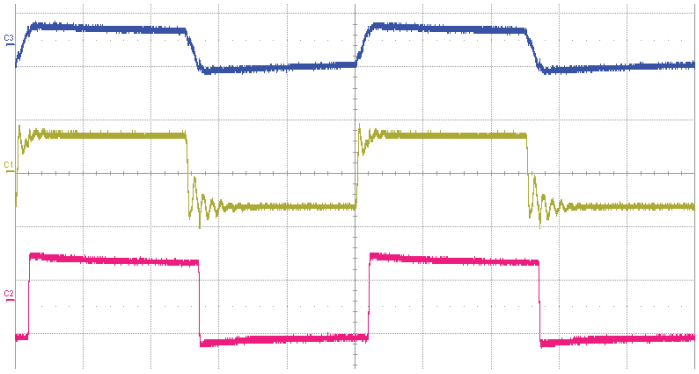

FIG. 7A

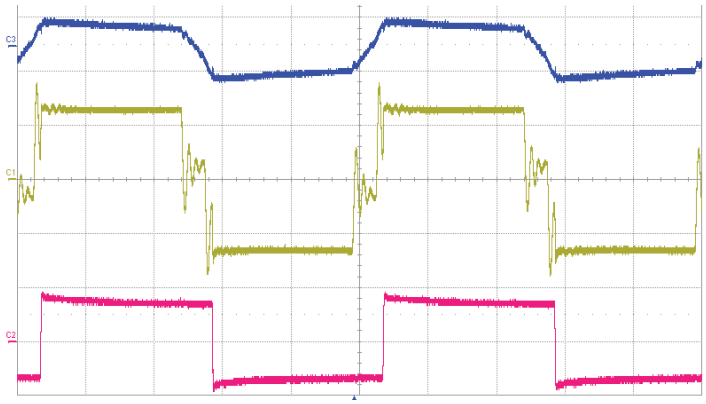

FIG. 7B

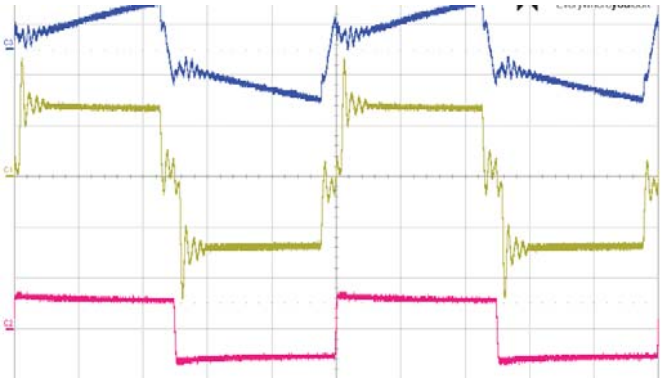

FIG. 7C

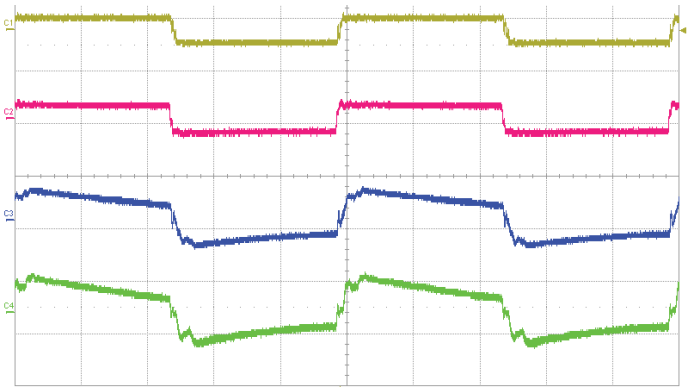

FIG. 8A

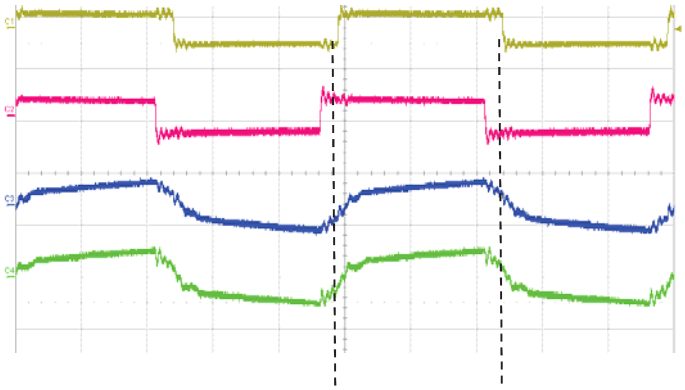

FIG. 8B

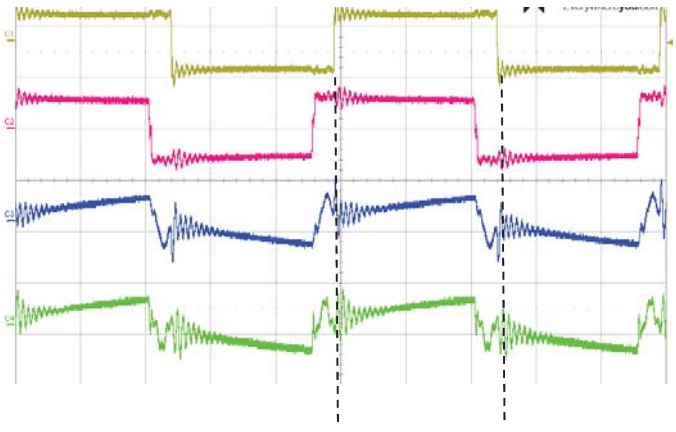

FIG. 8C

G

High Voltage Gain Dual Active Bridge Converter with an Extended Operation Range for Renewable Energy Systems

In IEEE APEC, San Antonio, March 4-8, 2018.

High Voltage Gain Dual Active Bridge Converter with an Extended Operation Range for Renewable Energy Systems

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***Abstract*—Developing bidirectional dc-dc converters has become a critical research topic and gains more and more attention in recent years due to the extensive applications of smart grids with energy storages, hybrid and electrical vehicles and dc microgrids. In this paper, a Partial Parallel Dual Active Bridge (P^2DAB) converter, i.e. low-voltage (LV) side parallel and high-voltage (HV) side series, is proposed to achieve high voltage gain and low current stress over switching devices and transformer windings. Given the unmodified P^2DAB power stage, by regulating the phase-shift angle between the paralleled active bridges, the power equations and voltage gain are then modified, and therefore the operation range can be extended effectively. The operating principles of the proposed converter and its power characteristics under various operation modes are studied, and the design constraints are discussed. Finally, a laboratory prototype is constructed and tested. Both simulation and experimental results have verified the proposed topology's operation and design.**

***Keywords*—Bidirectional; converter; DAB; dc-dc; high voltage gain; soft-switching.**

I. INTRODUCTION

Bidirectional dc-dc converters provide the capability of effectively and flexibly regulating reversible dc power flows, making them an essential solution in applications such as renewable energy systems, electrical vehicles and dc microgrids [1]-[5]. Several bidirectional dc-dc topologies, as well as their derivations, exist but given the galvanic isolation requirement, the two most established converters are the dual active bridge (DAB) and the isolated boost/buck converter [6], [7]. This paper focuses on the DAB converter, which has been implemented in a wide range of applications including renewable energy conversion, smart transformers, and transportation electrification, due to its unique features such as symmetrical configuration and zero voltage switching (ZVS). However, there are still some fundamental issues existing, for instance, the DAB converter's efficiency suffers from large root mean square (rms) current because of 1) voltage unmatch between low voltage side (LVs) and high voltage side (HVs) and 2) phase-shift control introducing reactive power, and it becomes even severe for high-power applications. Various techniques for high current applications have been proposed. The well-known method is directly parallel semiconductor devices or converter modular units [8]-[11]. Paralleling switches complicates circuit layout and increases parasitic inductance. Moreover, thicker copper or a parallel structure must be applied to transformer windings resulting in high manufacturing cost and high interwinding capacitance, especially for print circuit board (PCB) windings. On the other hand, paralleling converter modular units need additional control scheme to eliminate circulating current between units. Besides paralleling, other methods are targeted towards reactive current reduction and ZVS region extension by using more advanced modulation strategies for instance double- or triple-phase-shift modulations and variable frequency modulations [12]-[14].

In this paper, based on an idea of connecting the circuit parts, which need to carry high current, in parallel and connecting the circuit parts, which need to block high voltage, in series, a new DAB converter configuration, so-called Partial Parallel Dual Active Bridge (P^2DAB) converter is proposed for high-power applications. The ac current balancing between the parallel full-bridges is inherently ensured by the winding series connection on the HVs. Moreover, compared with the traditional DAB converter, regulating the phase-shift angle between the paralleled active bridges gives an additional degree of freedom for power control, and thereby extends the P^2DAB converter's operating range.

II. PROPOSED P^2DAB CONVERTER

The proposed topology is presented in Fig. 1. The converter is derived from a DAB topology with parallel high-current parts. Two transformers operated in parallel on the LVs and in series on the HVs. Due to series connection of the HVs windings, the currents i_1 and i_2 are forced to be the same and can be expressed as,

$$i_1 = i_1 = n \cdot i_{ac} \tag{1}$$

where i_{ac} and n represent the HVs winding current and the transformer turns ratio, respectively, as denoted in Fig. 1.

A single common active full bridge is connected to the high-voltage port V_2. This partial parallel configuration splits the high-current loops into two smaller loops with half the total

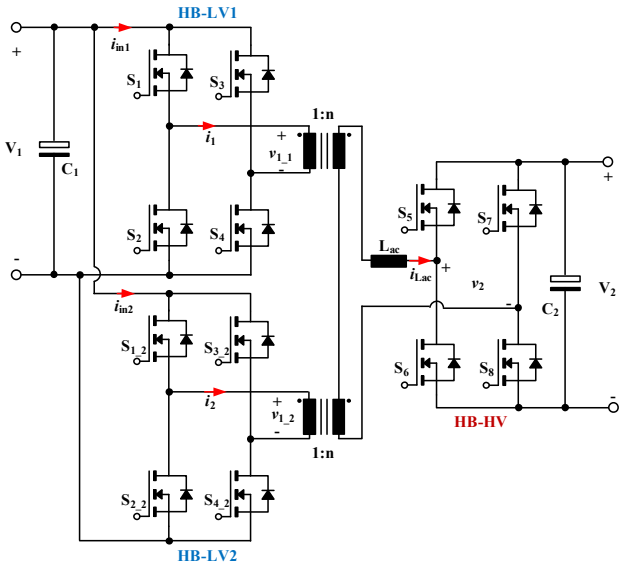


Fig. 1. Topology of the proposed P²DAB.

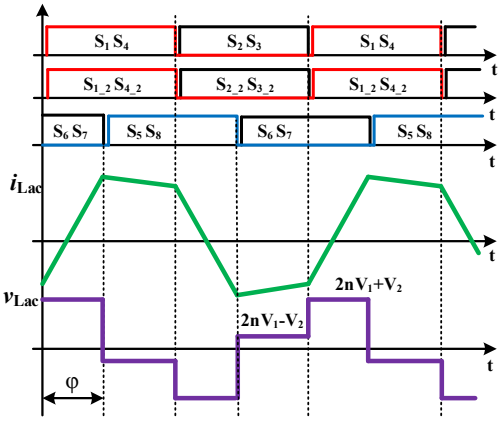


Fig. 2. Basic single phase-shift modulation.

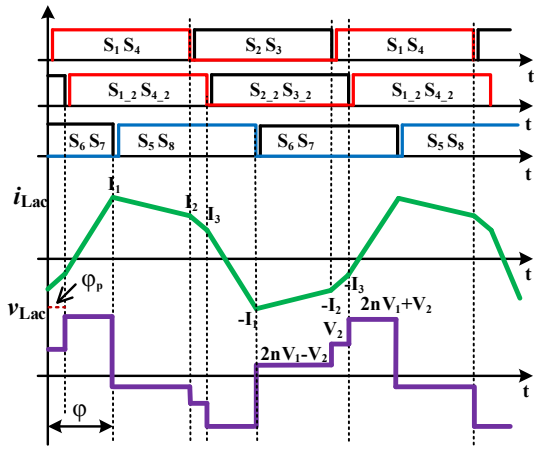


Fig. 3. Phase-shift control of the paralleled active bridges.

input current, and thereby reduces conduction and switching losses. Due to only high-current parts duplicated, cost can be reduced accordingly. The basic converter operating waveforms under single phase-shift modulation are presented in Fig. 2, and the converter's steady-state power equation can be derived from (2).

$$P = \frac{2nV_1V_2}{f_s L_{ac}}\varphi(1-2\varphi) \tag{2}$$

where the phase shift φ is represented as a percentage of the switching period T_s, f_s is the switching frequency and L_{ac} is the sum of the external inductance and the transformer leakage inductance seen from the HVs.

If a fixed load Z_L is connected to V_2 port, the P²DAB converter's voltage gain can be expressed by (3). As it can be observed, it is twice as much as that of conventional DAB converters.

$$G(\varphi) = \frac{V_2}{V_1} = 2n\frac{Z_L}{f_s L_{ac}}\varphi(1-2\varphi). \tag{3}$$

This partial parallel principle can also be applied to other DAB derived topologies, such as single active bridge (SAB), dual half bridge (DHB) and dual three- or multi-phase bridge (DTB or DMB) converters for high-current applications.

III. Operating Range Extension

A. Additional Phase-shift and Effects

Regulating the phase shift between the two paralleled active bridges, i.e. HB-LV1 and HB-LV2 gives an additional degree of freedom to control output power or voltage. Fig. 3 shows the switching pattern and the typical ac inductor current and voltage waveforms when the additional phase shift φ_p is inserted and $0<\varphi_p<\varphi$. Based on the waveforms in Fig. 3, I_1, I_2 and I_3 can be calculated accordingly in (4)-(6). By using the mean-value theorem, the power equation for P²DAB with φ and φ_p as the control parameters is expressed in (7).

$$I_1 = \frac{(4\varphi - 2\varphi_p - 1)\cdot 2nV_1 + V_2}{4f_s L_{ac}}. \tag{4}$$

$$I_2 = \frac{(1-2\varphi_p)\cdot 2nV_1 + (4\varphi - 1)\cdot V_2}{4f_s L_{ac}}. \tag{5}$$

$$I_3 = \frac{(1-2\varphi_p)\cdot 2nV_1 + (4\varphi - 4\varphi_p - 1)\cdot V_2}{4f_s L_{ac}}. \tag{6}$$

$$P = \frac{2nV_1V_2}{f_s L_{ac}}\varphi\left(1 - 2\varphi + 2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi}\right) \quad (0<\varphi_p\le\varphi). \tag{7}$$

Equation (7), in comparison to (2), has an additional term i.e. $2\varphi_p - \frac{\varphi_p}{2\varphi} - \frac{\varphi_p^2}{\varphi}$ which is always negative when $0<\varphi\le 0.25$ (the phase-shift angle is limited to be smaller than $\pi/2$).

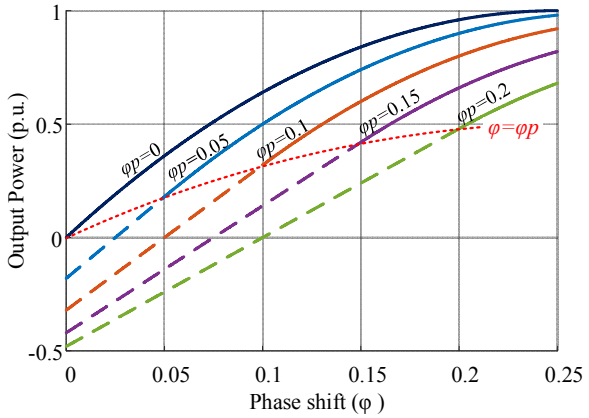


Fig. 4. Power as a function of φ at different φ_p.

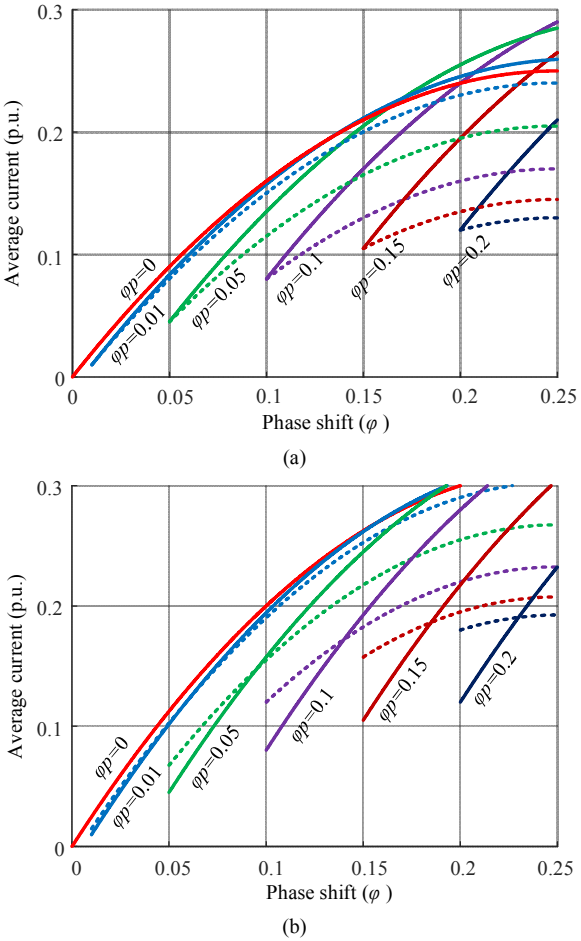


Fig. 5. Average input current as a function of φ_p at different φ. (a) m=1, and (b) $m\neq1$.

Similarly, the power equation for $\varphi<\varphi_p<0.25$ is expressed by (8).

$$P=\frac{4nV_1V_2}{f_sL_{ac}}\left(\varphi-\frac{\varphi_p}{2}\right)\left(\frac{1}{2}-\varphi_p\right)\quad(\varphi<\varphi_p\leq0.25). \tag{8}$$

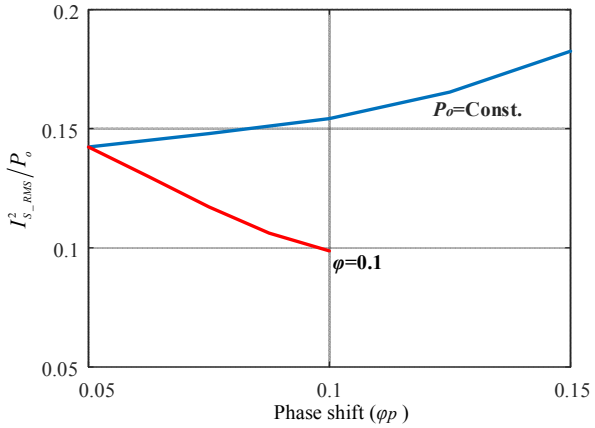


Fig. 6. Variation of rms currents as a function of $\varphi_p<\varphi$.

Therefore, the power as a function of φ and φ_p can be plotted in Fig. 4, where the base power is $nV_1V_2/4f_sL_{ac}$.

B. Design Considerations

It is found that regulating φ_p results in an unequal power distribution between the paralleled active bridges. When $0<\varphi_p<\varphi$, the average input currents I_{in1_avg} and I_{in2_avg} can be calculated by (9) and (10).

$$I_{in1\_avg}=\frac{n^2V_1}{f_sL_{ac}}\left[2m\varphi(1-2\varphi)+\varphi_p(2\varphi_p-1)\right] \tag{9}$$

$$I_{in2\_avg}=\frac{n^2V_1}{f_sL_{ac}}\left[2m(\varphi-\varphi_p)(1-2\varphi+2\varphi_p)+\varphi_p(1-2\varphi_p)\right] \tag{10}$$

where

$$m=\frac{V_2}{2nV_1}. \tag{11}$$

From (9)-(11), it can be seen that the current distribution between the two paralleled bridges depends on the phase-shift angles φ and φ_p and m. When φ_p=0,

$$I_{in1\_avg}=I_{in2\_avg}=\frac{n^2V_1}{f_sL_{ac}}2m\varphi(1-2\varphi)=\frac{nV_2}{f_sL_{ac}}\varphi(1-2\varphi). \tag{12}$$

Fig. 5 shows the ratios of the average currents I_{in1_avg} and I_{in2_avg} against $n^2\cdot V_1/f_s/L_{ac}$ as a function of φ. The dashed line and solid line represent I_{in1_avg} and I_{in2_avg} respectively. When m=1, I_{in1_avg} and I_{in2_avg} always intersect at $\varphi=\varphi_p$. In fact, the introduced φ_p varies the effective phase-shift angle between ac current and voltage, which results in the different input currents. The active bridge in which the ac current and voltage have smaller phase delay will carry more real power and accordingly has larger average input current.

On the other hand, the series winding connection constrains the rms currents to be equal in all the semiconductor switches on the LVs.

$$I_{S1\sim S4\_rms}=I_{S1\_2\sim S4\_2\_rms}. \tag{13}$$

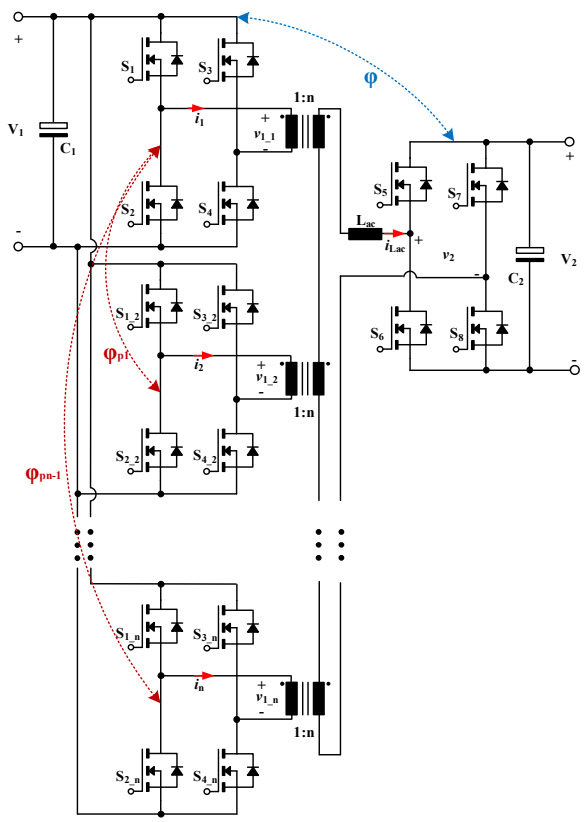


Fig. 7. A high voltage gain DAB converter with multiple partially paralleled LV bridges.

In Fig. 6, $I_{S\_RMS}^2/P_o$ as a function of φ_p is plotted. To keep the output power constant as the blue line illustrated, φ must be increased when increasing φ_p, which leads to higher reactive power as well as a higher rms current. But if φ is fixed, the red line shows that increasing φ_p causes output power reduction, but at the same time, $I_{S\_RMS}^2$ decreases even further so that lowers conduction loss.

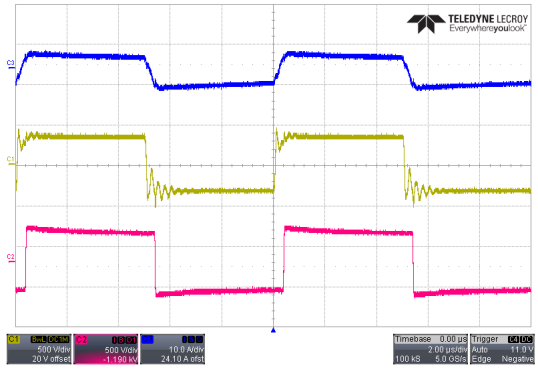
For switching losses, S_{1_2}~S_{4_2} have lower turn-off losses than S_1~S_4, since they are turned off at I_3 which is smaller than I_2 at which S_1~S_4 are switched off, as shown in Fig. 3. However, I_2 and I_3 must be positive in order to discharge the MOSFET's output capacitance and achieve ZVS during turn on. The larger the current, the easier the ZVS is achieved.

C. Topological Extension

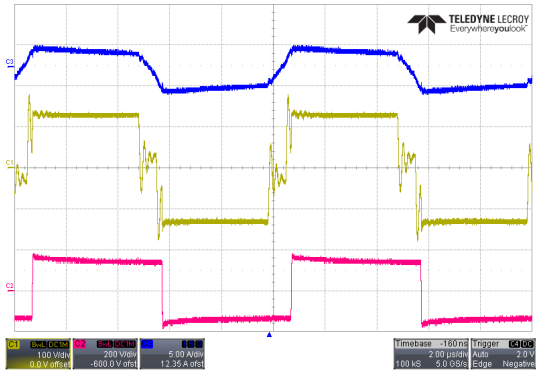
This partial parallel idea can be extended further and be applied to a DAB converter with multiple transformers in order to carry large current as well as obtain high voltage gain. An example is given in Fig. 6, where the number of branches is n, and accordingly the number of additional and controllable phase-shift angles is n-1.

IV. Experimental Results

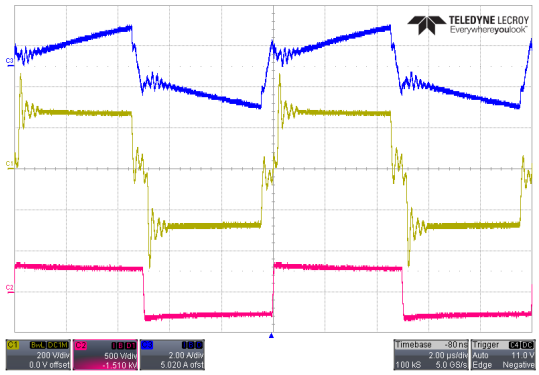
The proposed P^{2}DAB converter has been simulated, built and tested to validate the theoretical analysis. The prototype parameters are listed in Table I.



(a)



(b)

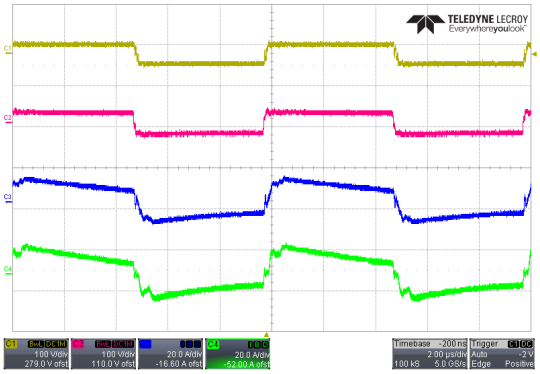


(c)

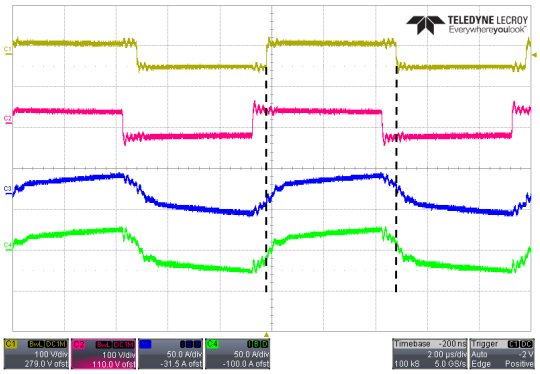
Fig. 8. Experimental waveforms of voltage $n\cdot(v_{1\_1}+v_{1\_2})$ (Ch1), voltage v_2 (Ch2) and current i_{Lac} (Ch3): (a) φ=0.034 and φ_p=0, (b) φ=0.08 and φ_p=0.06, and (c) φ=0.04 and φ_p=0.05. (Time: 2μs/div)

TABLE I. Prototype Parameters

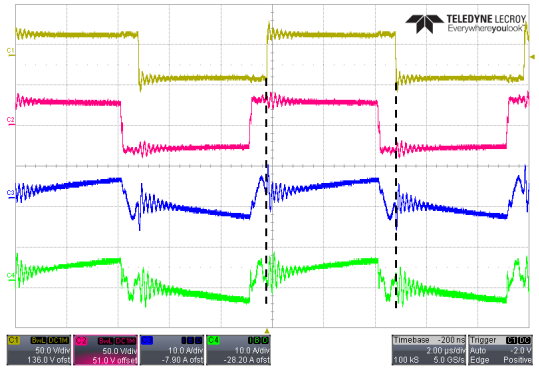
Parameters	Values
V_1 and V_2	50 V and 400 V
Maximum output power, P_{O_max}	1 kW
Transfromers, $Tr1$ and $Tr2$	4:16, 3C90
Inductor, L_{ac}	30 μH
Switching frequency, f_s	100 kHz
Digital controller	TMS320F28335



(a)



(b)



(c)

Fig. 9. Experimental waveforms of voltage v_{1_1} (Ch1), voltage v_{1_2} (Ch2), current i_1 (Ch3) and current i_2 (Ch4): (a) φ_p=0, (b) φ_p<φ, and (c) φ_p>φ (Time: 2μs/div)

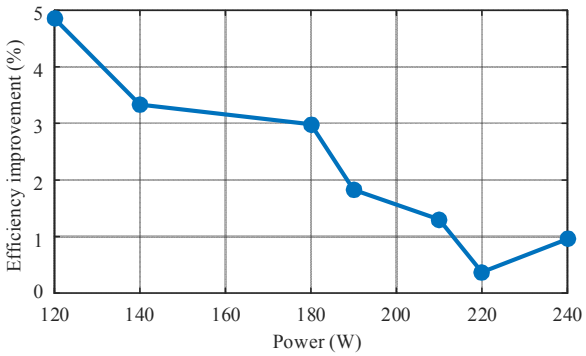


Fig. 10. Measured efficiency improvement at low power.

In Fig. 8, the experimental waveforms with φ_p=0, φ_p<φ and φ_p>φ are presented respectively and the measured results can match the theoretical analysis well. When φ_p≠0, the voltage across the series connected high-voltage windings, i.e. $n\cdot(v_{1\_1}+v_{1\_2})$ becomes a three-level waveform consisting of $\pm 2nV_1$ and 0, which changes the current waveforms accordingly.

The low-voltage side waveforms are given in Fig. 9 to show the effect of φ_p. The currents i_1 and i_2 are always the same regardless the phase-shift angles. Moreover, as it can be observed, L_{ac} makes the ac current lagging behind the ac voltage, which introduces reactive power and leads to extra conduction losses. The larger the phase shift, the higher the loss is. However, regulating φ_p is able to delay the ac voltage v_{1_1}, so that the effective phase-shift angle between v_{1_1} and i_1 is reduced, as highlighted in Fig. 9 (b) and (c) with the dashed lines, and the reactive power decreases. It also explains the reason why the input currents i_{in1} and i_{in2} have different average values.

According to the principles explained above, at the same input and output voltages, using both φ and φ_p to regulate power can improve the converter efficiency at light loads in comparison to the single phase-shift modulation. The measured efficiency improvement is presented in Fig. 10.

V. Conclusion

A new way to extend power level of DAB converters for high-power high-gain applications is proposed and presented in this paper. Partially paralleling allows efficient operation due to small ac loops, reduced current switching losses and fewer high-voltage power devices. Regulating the phase shift between the paralleled active bridges can not only improve the power controllability but also reduce the high-frequency reactive power and, therefore, is more power efficient than the traditional DAB converters with a single phase-shift control.

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H

Series-Connected Power Conversion System

Patent application submitted to Europe Patent office, August, 2018.

A DC-DC CONVERTER ASSEMBLY

The present invention relates to a DC-DC converter assembly which comprises a DC-DC converter. A converter load is electrically connected between a positive input and a positive output of the DC-DC converter such that a DC input voltage source of the assembly supplies power directly to the converter load without passing through the DC-DC converter.

BACKGROUND OF THE INVENTION

Active and passive components of existing high power DC-DC converters are subjected to large voltage and current stresses and large heat dissipation caused by the flow of power through the converter and into the converter load. This reduces reliability and lifetime of high power DC-DC converters and requires costly active and passive components that can withstand the high currents and/or voltages.

Hence, it is desirable to reduce the current stress and/or voltage stress of active and passive components of DC-DC converters of DC-DC converter assemblies for a given or nominal load power.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a DC-DC converter assembly which comprises a DC-DC converter. The DC-DC converter is configured to convert a DC input voltage into a DC output and comprises:

- a positive input and a negative input for receipt of the DC input voltage from a DC input voltage source,
- a positive output and a negative output for supply of the DC output voltage to a converter load,
- a voltage regulation loop and/or a current regulation loop configured to adjust the DC output voltage or DC output current in accordance with a target DC voltage or a DC target current, respectively; and wherein the converter load is electrically connected between the positive input and the positive output of the DC-DC converter such that the DC input voltage source supplies power directly to the converter load without passing through the DC-DC converter.

By connecting the converter load of the converter assembly between the positive input and the positive output of the DC-DC converter, the DC input voltage source may supply the majority of the power in the converter load, for example more than 50 %, or more than 66 %, or even the substantially entire load power, directly to the converter load. This feature markedly reduces the amount of power that is converted by, i.e. flowing through, the DC-DC converter for a given or target power delivery. The ratio between the power supplied directly to the converter load by the DC input voltage source and the power flowing through the DC-DC converter can be controlled or adjusted by selecting a value of the DC output voltage for a given DC input voltage. A step-down ratio or step-up of the DC-DC converter corresponds to the ratio between the DC output voltage and the DC input voltage depending where the converter load and DC input voltage source is connected. The predetermined step-down ratio or step-up of the DC-DC converter can also be expressed as a corresponding voltage gain as discussed below by numerical examples with reference to under the appended drawings.

For mains connected applications, the DC input voltage may lie between 320 V and 800 V for example higher than 565 V. The DC output voltage may be smaller than one-fifth or one-tenth of the DC input voltage. The load power may be larger than 10 kW or larger than 50 kW.

Various types of DC-DC converters may be utilised in the present DC-DC converter assembly for example a high voltage gain DC-DC converter. The DC-DC converter may comprise a resonant converter topology or a non-resonant or hard-switched converter topology. The DC-DC converter may comprise one transformer or several separate transformers coupled in-between a primary side circuit and a secondary side circuit of the DC-DC converter to support a relatively high voltage gain of the DC-DC converter.

The DC-DC converter may comprise a resonant converter as mentioned above. The resonant converter may comprise a resonant network, e.g. an LC based circuit or resonator as discussed below, connected to an input driver or an output driver of the power converter. The input driver may therefore be configured to operate in so-called ZVS or ZCS mode to decrease power dissipation of one or more controllable

semiconductor switches of the input driver. The input driver may comprise well-known driver topologies such as a half-bridge driver or an H-bridge driver. The input driver may comprise a plurality of appropriately arranged semiconductor switches such as IGBT switches or MOSFET switches to form well-known driver topologies.

The output voltage regulation loop ensures that the DC output voltage tracks the DC target voltage and the output current regulation loop likewise ensures the DC output current tracks the DC target current. The output voltage regulation loop ensures that the voltage drop across the converter load is relatively constant and well-defined as the difference between the DC input voltage and the DC output voltage. The output voltage or current regulation loop may include various known control mechanism such as pulse width modulation (PWM), phase shift modulation (PSM) or frequency modulation (FM) of a drive signal applied to an input driver or output driver of the DC-DC converter.

One embodiment of the DC-DC converter comprises an isolated or non-isolated Dual-Active-Bridge (DAB) converter since the latter topologies possess a number of beneficial properties in applications where a high voltage ratio between DC input voltage and DC output voltage is required. A high DC input voltage may for example be stepped down to a much smaller DC output voltage. Generally, a step-down ratio or step-up ratio may be at least 2, or more preferably at least 10, such as between 20 and 40. This corresponds to a voltage gain between the DC input voltage and DC output voltage from 0.5 down to 0.025. High input voltages are typically present in grid connected applications of the DC-DC converter assembly where the DC input voltage is derived from a grid connected DC input voltage source, for example through a single-phase or three-phase AC-DC converter, and this high input voltage must be stepped-down to a much lower output voltage level. The lower output voltage level may be one tenth or less of the input voltage. The DAB converter possesses numerous beneficial properties for high voltage and power applications due to its inherent zero voltage switching (ZVS) characteristics, simplified transformer design and high voltage gain as discussed below in additional detail with reference to the appended drawings. One embodiment of the Dual Active Bridge converter comprises:

- a first set of *n* transformers comprising respective input windings and respective output windings magnetically coupled to each other through respective magnetically permeable cores; said input windings being connected in series,
- a first resonant network connected in series with the series connected input windings or a first set of *n* resonant networks connected in series with respective ones of the output windings,
- a first set of *n* rectification circuits connected to respective ones of the output windings of the first set of *n* transformers to supply a first set of *n* rectified transformer voltages and currents to a first set of *n* rectification nodes,
a summing node configured to combine the first set of *n* rectified transformer voltages and currents to generate the DC output voltage;
- *n* being a positive integer number larger than or equal to 2 - for example between 2 and 6.

The individual transformers of the first set of *n* transformers are preferably nominally identical to facilitate equal voltage division between the input windings of individual transformers and facilitate equal current sharing between the output windings of the *n* transformers and other secondary side circuitry like the *n* rectification circuits. The first set of *n* transformers may comprise between 2 and 6 individual transformers.

Certain embodiments of the Dual Active Bridge converter comprises:
- a current balancing transformer comprising *n* transformer windings connected between respective ones of the first set of *n* rectification nodes and the summing node to force current balancing between individual windings of the first set of output winding. The *n* transformer windings of the current balancing transformer are preferably wound around a common magnetically permeable core to provide strong magnetic coupling between the *n* transformer windings. The *n* transformer windings of the current balancing transformer are preferably wound around a shared leg structure of the common magnetically permeable core to conduct equal amounts of magnetic flux through each transformer winding. Alternatively, the *n* transformer windings of the current balancing transformer may be implemented as *n* magnetically coupled inductors. The skilled person will appreciate that the current balancing transformer provides numerous benefits to DC-DC converters which comprises a plurality, such as two, three, four or more, parallelly coupled secondary side circuits. These bene-

fits include elimination, or at least a significant reduction, of output current mismatches caused by practically occurring mismatches between electrical components and/or drive voltage waveform mismatches between the primary side circuits and secondary side circuits. The elimination of the output current mismatches allows parallel connection of numerous secondary side circuits and series connection of numerous input side circuits without inducing significant current imbalances between the individual secondary side circuits. Furthermore, each secondary side circuit and each primary side circuit can be rated at a much lower power rating compared to a single high-power secondary or primary side circuit. Hence, enabling utilization of relatively low cost active and passive components such as MOSFET and IGBT transistors. The thermal stress on the active and passive components is also reduced and leads to significant increase the life time expectancy of the Dual Active Bridge DC-DC converters.

The DC output voltage, and hence also load power, of the Dual Active Bridge converter may be controlled in an efficient manner by adjusting a phase difference between the respective control signals or drive signals of the active rectification circuit and the input driver. In this embodiment, the output voltage or output current regulation loop may comprise: a DC target voltage or a DC target current,

- a first input driver for generating a first pulse width modulated drive signal at a first phase angle and applying the first pulse width modulated drive signal to the series connected input windings of the first set of *n* transformers;
- a first active rectification circuit configured to generate a second pulse width modulated drive signal at a second phase angle and apply the second pulse width modulated drive signal to respective control terminals of a plurality of controllable semiconductor switches of each rectification circuit of the first set of *n* rectification circuits; wherein the output voltage or output current regulation loop is configured to adaptively adjusting a phase difference between the first phase angle and the second phase angle to reach a desired DC output voltage, or a desired DC output current, of the dual active bridge DC-DC converter.

The skilled person will appreciate that some embodiments of the DC-DC converter may be unidirectional supporting only transfer of power/energy from the DC input voltage source to the converter load. Such unidirectional DC-DC converters may

comprise one or more passive rectification circuit(s) on the secondary side. Alternative embodiments of the DC-DC converter may be bi-directional supporting the transfer of power/energy from the DC input voltage source to the converter load and vice versa. The reverse transfer of power from the converter load to the DC input voltage source may be enabled by active rectification circuits on the secondary side of the DC-DC converter and a control mechanism as discussed in additional detail below with reference to the appended drawings. Hence, according to certain embodiments of the DC-DC converter assembly, power may be transferred from the converter load directly to the DC input voltage source without passing through the DC-DC converter when operating in reverse mode. The skilled person will understand that the roles of the converter load and the DC input voltage source may be dynamically interchanged as needed during operation if the DC-DC converter supports bidirectional operation.

In grid-connected applications of the DC-DC converter assembly at least one of the converter load and the DC input voltage source may comprise an inverter, aka DC-AC converter, as discussed in additional detail below with reference to the appended drawings. The converter load may comprise a rechargeable battery pack and the DC input voltage source may comprise an inverter connectable to a single phase mains grid or a three phase mains grid. In this manner, the DC-DC converter assembly may charge the rechargeable battery pack through the mains voltage or alternatively, the DC-DC converter assembly may energize, drive or stabilize the mains grid using stored power/energy from the rechargeable battery pack.

Alternative embodiments of the DC-DC converter assembly, without grid connection, may operate without the inverter as part of the converter load or the DC input voltage source. The inverter may be eliminated where both the converter load and the DC input voltage source are native DC sources. For example, the DC input voltage may comprise photovoltaic cell(s) and/or batteries and the converter load may comprise solid oxide fuel cells to produce hydrogen.

Certain DAB DC-DC converter embodiments may comprise a poly-phase DAB DC-DC converter as disclosed in the applicant’s co-pending European application EP 16200247.1.

A second aspect of the invention relates to a method of supplying power to a converter load by a DC-DC converter, comprising:

- connecting a first terminal of the converter load to a positive input of the DC-DC converter,
- connecting a second terminal of the converter load to a positive output of the DC-DC converter,
- connecting a DC input voltage source to the positive input,
- adjusting a DC output voltage or a DC output current at the positive output of the DC-DC converter in accordance with a target DC voltage or target DC current, respectively.

The target DC voltage may be less than one-fifth, or even less than one-tenth, of the DC input voltage such that the DC input voltage source supplies a majority of the load power directly to the converter load compared to the power flowing through the DC-DC converter. The DC input voltage source may for example supply more than 75 % of the load power, or more than 90 % of the load power such as substantially 100 % of the load power as discussed in the numerical examples below.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

FIG. 1 is a schematic diagram of an exemplary DC-DC converter assembly in accordance with a first embodiment of the invention,

FIG. 2 is a schematic diagram of a DC-DC converter assembly in accordance with a second embodiment of the invention,

FIG. 3 is a schematic diagram of a DC-DC converter assembly in accordance with a third embodiment of the invention,

FIG. 4 is a schematic diagram of a DC-DC converter assembly in accordance with a fourth embodiment of the invention,

FIG. 5 is a schematic diagram of a DC-DC converter assembly in accordance with a fifth embodiment of the invention,

FIG. 6 shows schematic diagram of a DC-DC converter assembly based on a single-phase dual active bridge (DAB) DC-DC converter in accordance with a sixth embodiment of the invention; and

FIG. 7 is a circuit diagram of various exemplary resonant networks for use in DC-DC converters of the present DC-DC converter assemblies.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following, various exemplary embodiments of the present DC-DC converter assembly are described with reference to the appended drawings. The skilled person will understand that the accompanying drawings are schematic and simplified for clarity and therefore merely show details which are essential to the understanding of the invention, while other details have been left out. Like reference numerals refer to like elements or components throughout. Like elements or components will therefore not necessarily be described in detail with respect to each figure. It will further be appreciated that certain actions and/or steps may be described or depicted in a particular order of occurrence while those skilled in the art will understand that such specificity with respect to sequence is not actually required.

FIG. 1 shows a schematic diagram of an exemplary DC-DC converter assembly 100 in accordance with a first embodiment of the invention. The DC-DC converter assembly 100 comprises a DC-DC converter 101 which converts a first fraction of a load power of the converter load 110 (Load/Source), while a DC input voltage source or current source 120 (Source/Load) supplies a second fraction of the load power directly to the converter load 110 without passing through the DC-DC converter 101. The direct supply of load power to the converter load 110 is achieved because the converter load 110 is connected between a positive input 103 and positive output 108 of the DC-DC converter 101 - for example via an electrical wire or conductor 112. This load connection arrangement connects the converter load 110 in series with the DC-DC converter 101 instead of the traditional parallel output connection of the converter load. In some embodiments of the DC-DC converter assembly 100, the second fraction of the load power may be markedly larger than the first fraction - for example at least 3, 5 or 10 times larger depending on design details, voltage specifications of the converter load and DC input source and performance requirement of the DC-DC converter assembly 100. The reduced power de-

livery of the DC-DC converter 101 leads to a considerable reduction in size and costs of the DAB DC-DC converter 101 at any given load power in combination with increased reliability, since voltage stress and heat dissipation of active and passive components of the DC-DC core 102 are reduced. The overall energy/power efficiency of the DC-DC converter assembly 100 also increases because the DC-DC converter 102 converts less power which reduces power losses within the converter 102.

The DC input voltage source 120 is connected between a positive input 103 and negative input 104 of the DC-DC converter 101. The negative input 104 may for example be connected to a ground potential of the DC converter assembly 100 and a negative output 107 also connected to the ground potential.

The DC-DC converter 101 additionally comprises a voltage or current regulation loop 111a, 111b, 111c configured to adjust the DC output voltage at the output terminal 122 in accordance with a target DC voltage or equivalent adjusting a DC output current flowing through the output terminal 122 in accordance with a target DC current. The voltage or current regulation loop 111a, 111b, 111c may comprise a feedback mechanism. The regulation mechanism of the voltage or current regulation loop may comprise a modulation strategy such a PWM, PSM or FM of a drive signal applied to an input driver and/or an output driver of the DC-DC converter 101 as discussed in additional detail below. The skilled person will appreciate that some embodiments of the DC-DC converter 101 may be unidirectional where power only can be transferred from the source 120 to the load 110. Such unidirectional DC-DC converters may comprise a passive rectification circuit on the secondary side. Alternative embodiments of the DC-DC converter 101 may be bi-directional enabling power transfer from the source 120 to the load 110 and vice versa depending on a suitable control mechanism applied to an active rectification circuit on the secondary side. In the latter embodiments, the skilled person will understand that the role of the DC input voltage source 120 and the converter load 110 may be interchanged when the DC-DC converter 101 operates in reverse mode and hence the DC input voltage source 120 is also indicated as Load while the converter load 110 is also indicated as Source.

The DC output voltage, as set by the voltage or current regulation loop, may be significant smaller than the DC input voltage supplied by the DC input source 120 at the positive and negative inputs of the DC-DC converter 101. This feature ensures that the majority of the load power is supplied by the DC input source 120 as illustrated by the quantitative example below.

An exemplary embodiment of the DC-DC converter assembly 100 may be designed using the following constraints and target performance:

DC input voltage = Vs= 565 V – corresponding to a three-phase rectified mains voltage.
Iload = 100 A.
Pload = 54 kW.

Vload = Pload/Iload = 540 V.
Vout = Vs-Vload = 565 V - 540 V = 25 V.
Iout = Iload, due to the series connection of the load and the output of the DC-DC converter.

Using the above design and performance targets for the DC-DC converter assembly 100 and for simplicity assuming 100 % efficiency of the DC-DC converter eff=100/100 reveals that:

Converter power at Vout terminals = P1= 25 V * 100 A = 2.5 kW.
Converter power at Vin terminals = P2 = P1*eff = 2.5 kW *1 = 2.5 kW
Iin = P2 / Vs = 4.4248 A
Is = Iload – Iin = 95.5752 A
Ps = Vs * Is = 54 kW

Consequently, in the above scenario the DC input voltage source supplies 100 % of the 54 kW of load power directly to the converter load 110, i.e. without passing through the DC-DC converter. Furthermore, the DC-DC converter 101 converts 2.5 kW of circulating power flowing through the DC-DC converter 101.

Assuming an efficiency of the DC-DC converter 95% eff=95/100 reveals using the same target specifications as above reveals that:
Converter power at Vout terminals = P1= 25 V * 100 A = 2.5 kW.
Converter power at Vin terminals = P2 = P1*eff = 2.5 kW * 0.95 = 2.375 kW
The DC-DC converter losses = P1 – P2 = 2.5 kW – 2.375 kW = 125 W
Iin = P2 / Vs = 4.2035 A
Is = Iload – Iin = 95.7965 A
Ps = Vs * Is = 54.125 kW

Accordingly, the efficiency of the DC-DC converter assembly Passembly:
Passembly =100*(Pload / Ps) =100*(54 kW / 54.125 kW) = 99.77%

Consequently, the DC input voltage source supplies 54.125 kW of power of which 54 kW is the power supplied directly to the converter load 110 and an additional fraction of power related to the DC-DC converter 101 losses of 125 W. This leads to a total efficiency of the DC-DC converter assembly of 99.77%.

The skilled person will understand that the voltage regulation loop 111a, 111b, 111c may be adapted to set a higher DC output voltage of the converter 101 than the above-specified 25 V or an even smaller DC output voltage of the converter 101. Hence, a smaller fraction or an even larger fraction of the load power may be converted by, or supplied through, the DC-DC converter 101. The lower the DC output voltage will lead to a lower circulating power converted by the DC-DC converter. However, the lower DC output voltage will generally lead to a larger voltage gain of the DC-DC converter 101 which may present practical problems for passive components, like transformers, of the DC-DC converter 101.

However, a large voltage gain can be accommodated in an advantageous manner by utilizing a DC-DC converter topology which comprises a plurality of transformers with their primary side windings connected in series to the DC input voltage. The series connected primary side windings lead to a smaller voltage drop across each primary winding and a reduced requirement to the voltage gain between the primary winding and secondary winding of each transformer. The DC-DC converter may for example comprise a Dual-Active-Bridge (DAB) converter since the latter converter

topology possesses a number of beneficial properties when exploited in the present DC-DC converter 101 where a high input voltage often arises from a grid connected input source. This high voltage must be transformed down to a much lower output voltage level e.g. one tenth or less of the input voltage. The (DAB) converter possesses numerous beneficial properties for high power applications due to its inherent zero voltage switching (ZVS) characteristics, simplified transformer design and high voltage gain [1], [2], [3]. The DAB converter is preferably configured with parallel connected secondary side circuits (i.e. low voltage side) while the primary side circuits (i.e. high voltage side) are series connected to achieve a high voltage gain or step-down ratio as discussed below in additional detail with reference to FIG. 6.

FIG. 2 shows a schematic diagram of a DC-DC converter assembly 200 in accordance with a second embodiment of the invention. The DC-DC converter assembly 100 comprises a DC-DC converter 201 which may be identical to any of the previously discussed exemplary DC-DC converters. The present DC-DC converter 201 may be unidirectional and transfer power from a DC input voltage source which comprises a two-phase or three-phase grid-connected inverter 222, 220. The load 210 may comprise an energy storage unit such as a rechargeable battery stack or package comprising a plurality of series connected rechargeable battery cells or a fuel cell etc.

FIG. 3 shows a schematic diagram of a DC-DC converter assembly 300 in accordance with a third embodiment of the invention. The DC-DC converter assembly 300 comprises a DC-DC converter 301 which may be identical to any of the previously discussed exemplary DC-DC converters. The present DC-DC converter 301 may be unidirectional and transfer power from a DC input voltage source 320 which comprises an energy storage unit such as a rechargeable battery stack or package comprising a plurality of series connected rechargeable battery cells or a fuel cell etc. The load 310 may comprise a grid-connected inverter 310. In this manner, the grid acts as a converter load and the energy storage unit may deliver power/energy to the grid for example for grid stabilization purposes or deliver power/energy to AC loads such as dishwashers or washing machines.

FIG. 4 shows a schematic diagram of a DC-DC converter assembly 400 in accordance with a fourth embodiment of the invention. The DC-DC converter assembly 400 comprises a DC-DC converter 401 which may be identical to any of the previously discussed exemplary DC-DC converters. The present DC-DC converter 401 may be bi-directional and in a reverse mode of operation transfer power from a load connected DC source 410 to a two-phase or three-phase grid-connected inverter 420. The load connected DC source 410 may comprise an energy storage unit such as a rechargeable battery stack or package comprising a plurality of series connected rechargeable battery cells or a fuel cell etc.

FIG. 5 shows a schematic diagram of a DC-DC converter assembly 500 in accordance with a fifth embodiment of the invention. The DC-DC converter assembly 500 comprises a DC-DC converter 501 which may be identical to any of the previously discussed exemplary DC-DC converters. The present DC-DC converter 501 may be adapted for bidirectional operation and, in a reverse mode of operation, transfer power from grid-connected inverter 510, which is connected to the load terminals of the converter, to a DC source 520. The load connected DC source 520 may comprise an energy storage unit such as a rechargeable battery stack or package 525 comprising a plurality of series connected rechargeable battery cells or a fuel cell etc. Hence, the roles of the load and source have been interchanged comparted to the DC-DC converter assembly 400 discussed above.

FIG. 6 shows a schematic electrical diagram of an exemplary embodiment of the previously discussed DAB embodiment of the DC-DC converter 101. The depicted DAB converter 602 may be viewed as a single-phase embodiment of a range of DAB converter topologies that additional comprises poly-phase embodiments as those discussed in the applicant's co-pending European application EP 16200247.1. The DAB converter 602 comprises a positive input 603 for receipt of a DC input voltage produced by a DC input voltage or current source 620. The skilled person will understand that a DC input voltage source 620 may comprise an inverter, i.e. AC-DC converter, supplying a rectified mains voltage from a single phase mains voltage or a three-phase mains voltage. Hence, the DC input voltage may lie between 380 V and 565 V in grid connected embodiments of the DC-DC converter

assembly. The converter load/source is electrically connected between an output node or terminal 630 of the DAB converter 602 and the positive input 603 receiving the DC input voltage leading to the previously discussed benefits on the performance and reliability of the present DC-DC converter assembly because the load power is supplied directly by the DC input voltage or current source 620 without passing through the DAB DC-DC converter 602. Consequently, the DAB DC-DC converter 602 merely converts a certain fraction of the load power, and this fraction may be markedly smaller than the load power, which leads to a considerable reduction in size and costs of the DAB DC-DC converter 602 and increased reliability since voltage stress and heat dissipation in active and passive components are reduced.

The DAB DC-DC converter 602 may as illustrated comprise an H-bridge input driver comprising four controllable semiconductor switches SP1, SP2, SP3 and SP4 generating a first pulse width modulated drive signal (not shown) at a first phase angle φ1. The skilled person will understand that the first pulse width modulated drive signal may be generated by a voltage or current regulation loop (not shown) configured to generate or supply an appropriate drive signal to respective control terminals (not shown) of the four controllable semiconductor switches SP1, SP2, SP3 and SP4 of the H-bridge input driver. Each of the four controllable semiconductor switches SP1, SP2, SP3 and SP4 may for example comprise a MOSFET or an IGBT with a gate terminal acting as control terminal. The control terminals are utilised to control state switching of the MOSFET or an IGBT devices between a conducting state (on-state) and a non-conducting state (off-state). The DAB DC-DC converter 620 comprises a set of transformers where each transformer preferably is configured to deliver a substantial voltage gain between voltages of the primary side winding and secondary side winding of the transformer. The present embodiment of the DAB DC-DC converter 620 utilizes merely two separate transformers T1-1 and T1-2, but the skilled person will understand that alternatively embodiments may comprise one or more additional transformers having their primary winding(s) connected in series with the primary side windings of T1-1 and T1-2, and the secondary side winding(s) connected to a separate rectification circuit such that all rectification circuits are coupled in parallel to a common DC output voltage node 613.

The input/primary winding and output/secondary winding of each of the first and second transformers T1-1 and T1-2 are magnetically coupled to each other through respective magnetically permeable cores e.g. an E-core or toroidal core. The winding ratio of each of the first and second transformers T1-1 and T1-2 may vary depending on factors like the DC input voltage, number of transformers and a desired DC output voltage, or voltage range, of the converter 602. In some embodiments, a winding ratio between 4 and 20 such as about 9 has proven useful. The first and second transformers T1-1 and T1-2 are preferably nominally identical to facilitate equal voltage division between the respective input windings of first and second transformers and facilitate equal current sharing between the output windings and other secondary side circuitry. The first pulse width modulated drive signal generated by the H-bridge input driver is applied to the series connected input windings of first and second transformers T1-1 and T1-2 either through a resonant network 635, as illustrated in the present embodiment, or directly (without intermediate electric components like inductors and capacitors, to the series connected input windings. In the latter embodiment, the resonant network 635 is moved from the primary side of each transformer to the secondary side of the converter 602, more specifically to each of the output windings of the first and second transformers T1-1 and T1-2 on the secondary side of the DAB DC-DC converter 602. In the latter case, appropriately modified first and second resonant networks (not shown) are connected in series with respective ones of the output windings of the first and second transformers T1-1 and T1-2 by taken into account the impedance transformation caused by the winding ratios of the first and second transformers T1-1 and T1-2 and the number of parallelly connected output windings.

Three exemplary embodiments of the resonant network 635 are schematically illustrated on FIG. 7. The resonant network 635 may comprise a single series connected inductor L_{AC} connected in series with the series connected input windings of first and second transformers T1-1 and T1-2 or a series connected combination of an inductor L_{AC} and capacitor C_{AC}. The resonant network 635 may alternative comprise a pair of series connected inductors L_{AC1}, L_{AC2} and with a midpoint between these connected to a first terminal of a capacitor C_{AC} where the series connected inductors are inserted in series with input windings of the first and second transformers T1-1 and T1-2 and the other end of C_{AC} is connected to an ac ground potential.

The duty cycle of the first pulse width modulated drive signal may be 50 % and the first phase angle is an arbitrary value which is used to define respective phase shifts to additional pulse width modulated drive signal(s) and certain pulse width modulated rectification signals as discussed in additional detail below. The first pulse width modulated drive signal may have a frequency between 1 kHz and 1 MHz depending on numerous performance requirements of a specific design of the present DAB DC-DC converter 602 such as a desired maximum power output, properties of the first and second transformers and properties of the resonant network 635 or networks.

The DAB DC-DC converter 602 additionally comprises a set of rectification circuits comprising first and second active rectification circuits 607, 609 in the present embodiment but may comprise one or more additional active rectification circuits in other embodiments as mentioned above. The first and second active rectification circuits 607, 609 are connected to respective ones of the output windings of the first and second transformers T1-1 and T1-2 to supply respective rectified transformer voltages to first and second rectification nodes 607, 609 of the converter. Each of the first and second active rectification circuits comprises a full-wave rectifier in the present embodiment. The first active rectification circuit 632 comprises four controllable semiconductor switches, i.e. SS5, SS6, SS7 and SS8, connected to respective ends of the first output winding for receipt of the ac voltage induced in the first output winding. The second active rectification circuit 640 likewise comprises four controllable semiconductor switches, i.e. SS9, SS10, SS11 and SS12, connected to respective ends of the second output winding (of transformer T1-2) for receipt of the ac voltage induced in the second output winding. Each of the controllable semiconductor switches SS5, SS6, SS7, SS8, SS9, SS10, SS11 and SS12 of these rectification circuits may for example comprise a MOSFET or an IGBT with a gate terminal. The latter terminals are utilised to control state switching of the MOSFET or an IGBT devices between a conducting state (on-state) and a non-conducting state (off-state).

Hence, the term “active” in “active rectification circuit” means that the latter is based on controllable semiconductor switches, e.g. transistors, where the switching time

instant can be controlled via the respective control terminals of the switches by an appropriately timed control signal as opposed to a passive rectification circuit based on diodes. The latter control signal may in particular comprise a second pulse width modulated drive signal (not shown) that is off-set with a fixed or adjustable phase angle relative to the first pulse width modulated drive signal driving the input windings. The phase difference between the first and second pulse width modulated drive signals may be used to control load power to a converter load 610 connected to a DC output terminal or node 630 of the converter 602. Hence, this method of adjusting the load power supplied to the converter load 610 by the DC-DC converter 602 preferably comprising:

- applying the first pulse width modulated drive signal at a first phase angle to the series connected input windings of the first set of transformers,
- applying the second pulse width modulated drive signal at a second phase angle to respective control terminals of a plurality of controllable semiconductor switches of each rectifier of the first set of rectifiers,
- adaptively adjusting a phase difference between the first phase angle and the second phase angle to reach a desired DC output voltage of the dual active bridge DC-DC converter. The skilled person will understand that the adaptive adjustment of the phase difference may be carried out by a suitable voltage or current regulation loop sensing the instantaneous DC output voltage and comparing the latter with a certain DC reference/set-point voltage indicating a desired DC output voltage of the DC-DC converter 602.

The DAB DC-DC converter 602 may comprise an optional current balancing transformer 625 which comprises first and second transformer windings wound around a common magnetically permeable core (not shown). The number of turns of the first transformer winding is preferably identical to the number of turns of the second transformer winding in the present embodiment which comprises an even number of parallel secondary side circuits, i.e. two parallel secondary side circuits. One end of each of the first and second transformer windings of the current balancing transformer 625 is interconnected to form a common DC output voltage node 613 while the opposite ends of the first and second transformer windings are connected to respective ones of the first and second rectification nodes 632, 640. Hence, each transformer winding is connected between a rectification nodes and the common DC

output voltage node 613 and thereby forces current balancing between the output/secondary windings of the first and second transformers T1-1 and T1-2. The current balancing effect on currents flowing through first and second active rectification circuits 607, 609 and their associated output winding can be understood by noting the transformer 625 exhibits a high impedance against differential components of the first and second output currents *i1 and i2* and a low impedance in respect of common mode current components of the first and second output currents *i1* and *i2*. Construction details of the current balancing transformer 625 are discussed in detail in the applicant's co-pending application EP 16200247.1. The skilled person will appreciate that the current balancing transformer 625 provides numerous benefits to DAB DC-DC converter topologies comprising a plurality of parallelly coupled secondary side circuits. These benefits include the elimination, or at least a significant reduction, of output current mismatches, such as i1 and i2 discussed above, caused by practically occurring mismatches between electrical components and/or drive voltage waveform mismatches between the primary side circuits and secondary side circuits. The elimination of the output current mismatches allows numerous secondary side circuits to be coupled in parallel and numerous input side circuits coupled in series as discussed above, without inducing significant current imbalances between the individual secondary side circuits. The skilled person will appreciate that the series connection of the respective input windings of the set of transformers, e.g. the first and second transformers T1-1 and T1-2, provides numerous benefits to DAB DC-DC converter topologies comprising a plurality of series connected primary side circuits to achieve a high voltage gain in a grid-connected power converter. The transformer for each of the stages can be realized with a lower turns ratio for the input and output windings thereby significantly easing the transformer design process and enabling a modular design approach of simplified transformers.

The skilled person will appreciate that the controllable semiconductor switches SS5, SS6, SS7 SS8, SS9, SS10, SS11 and SS12 of first active rectification circuit 607 and the second active rectification circuit 609 may be replaced by diodes in alternative embodiments of the DAB DC-DC converter 602. Such a variant of the DAB DC-DC converter 602 is merely capable of supporting unidirectional power flow from the DC input voltage or energy source 620 to the converter load 610.

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+

CLAIMS

1. A DC-DC converter assembly comprising:
a DC-DC converter configured to convert a DC input voltage into a DC output voltage at a predetermined step-down ratio or step-up ratio, comprising:
- a positive input and a negative input for receipt of the DC input voltage from a DC input voltage source,
- a positive output and a negative output for supply of the DC output voltage to a converter load,
- a voltage regulation loop and/or a current regulation loop configured to adjust the DC output voltage or DC output current in accordance with a target DC voltage or a DC target current, respectively; and
wherein the converter load is electrically connected between the positive input and the positive output of the DC-DC converter such that the DC input voltage source supplies power directly to the converter load without passing through the DC-DC converter.

2. A DC-DC converter assembly according to claim 1, wherein the predetermined step-down ratio is at least 2, or more preferably at least 10, such as between 20 and 40 or the predetermined step-up ratio is at least 2, or more preferably at least 10, such as between 20 and 40.

3. A DC-DC converter assembly according to claim 1 or 2, wherein the DC-DC converter comprises a resonant network connected to an input driver of the power converter.

4. A DC-DC converter assembly according to claim 3, wherein the DC-DC converter comprises a Dual Active Bridge (DAB) converter.

5. A DC-DC converter assembly according to claim 4, wherein the Dual Active Bridge (DAB) converter comprises:
- a first set of *n* transformers comprising respective input windings and respective output windings magnetically coupled to each other through respective magnetically permeable cores; said input windings being connected in series,

- a first resonant network connected in series with the series connected input windings or a first set of *n* resonant networks connected in series with respective ones of the output windings,
- a first set of *n* rectification circuits connected to respective ones of the output windings of the first set of *n* transformers to supply a first set of *n* rectified transformer voltages and currents to a first set of *n* rectification nodes,
a summing node configured to combine the first set of *n* rectified transformer voltages and currents to generate the DC output voltage;
- *n* being a positive integer number larger than or equal to 2.

6. A DC-DC converter assembly according to claim 5, wherein the Dual Active Bridge (DAB) converter additionally comprises:
- a current balancing transformer comprising *n* transformer windings connected between respective ones of the first set of *n* rectification nodes and the summing node to force current balancing between individual windings of the first set of output windings.

7. A DC-DC converter assembly according to claim 5 or 6, wherein the first set of *n* transformers of the Dual Active Bridge (DAB) converter comprises of the between 2 and 6 individual transformers.

8. A DC-DC converter assembly according to any of claims 5 - 7, wherein the output voltage or output current regulation loop comprises:
- a first input driver for generating a first pulse width modulated drive signal at a first phase angle and applying the first pulse width modulated drive signal to the series connected input windings of the first set of *n* transformers;
- a first active rectification circuit configured to generate a second pulse width modulated drive signal at a second phase angle and apply the second pulse width modulated drive signal to respective control terminals of a plurality of controllable semiconductor switches of each rectification circuit of the first set of *n* rectification circuits; wherein the output voltage or output current regulation loop is configured to adaptively adjusting a phase difference between the first phase angle and the second phase angle to reach a desired DC output voltage or a desired DC output current of the dual active bridge DC-DC converter.

9. A DC-DC converter assembly according to any of the preceding claims, wherein at least one of the converter load and the DC input voltage source comprises an inverter, aka DC-AC converter.

10. A DC-DC converter assembly according to any of the preceding claims, wherein the DC-DC converter is configured for bidirectional operation to additionally transfer power from the converter load directly to the DC input voltage source without passing through the DC-DC converter.

11. A DC-DC converter assembly according to claim 10, wherein the converter load comprises a rechargeable battery pack and the DC input voltage source comprises an inverter, aka DC-AC converter, connectable to a single phase mains grid or a three phase mains grid.

12. A method of supplying power to a converter load by a DC-DC converter, comprising:
- connecting a first terminal of the converter load to a positive input of the DC-DC converter,
- connecting a second terminal of the converter load to a positive output of the DC-DC converter,
- connecting a DC input voltage source to the positive input,
- adjusting a DC output voltage or a DC output current at the positive output of the DC-DC converter in accordance with a target DC voltage or target DC current, respectively.

13. A method of supplying power to a converter load by a DC-DC converter according to a claim 12, wherein the target DC voltage is less than one-fifth of the DC input voltage such that the DC input voltage source supplies power directly to the converter load without passing through the DC-DC converter.

ABSTRACT

The present invention relates to a DC-DC converter assembly which comprises a DC-DC converter. A converter load is electrically connected between a positive input and a positive output of the DC-DC converter such that a DC input voltage source of the assembly supplies load power directly to the converter load without passing through the DC-DC converter.

(FIG. 1 to be published)

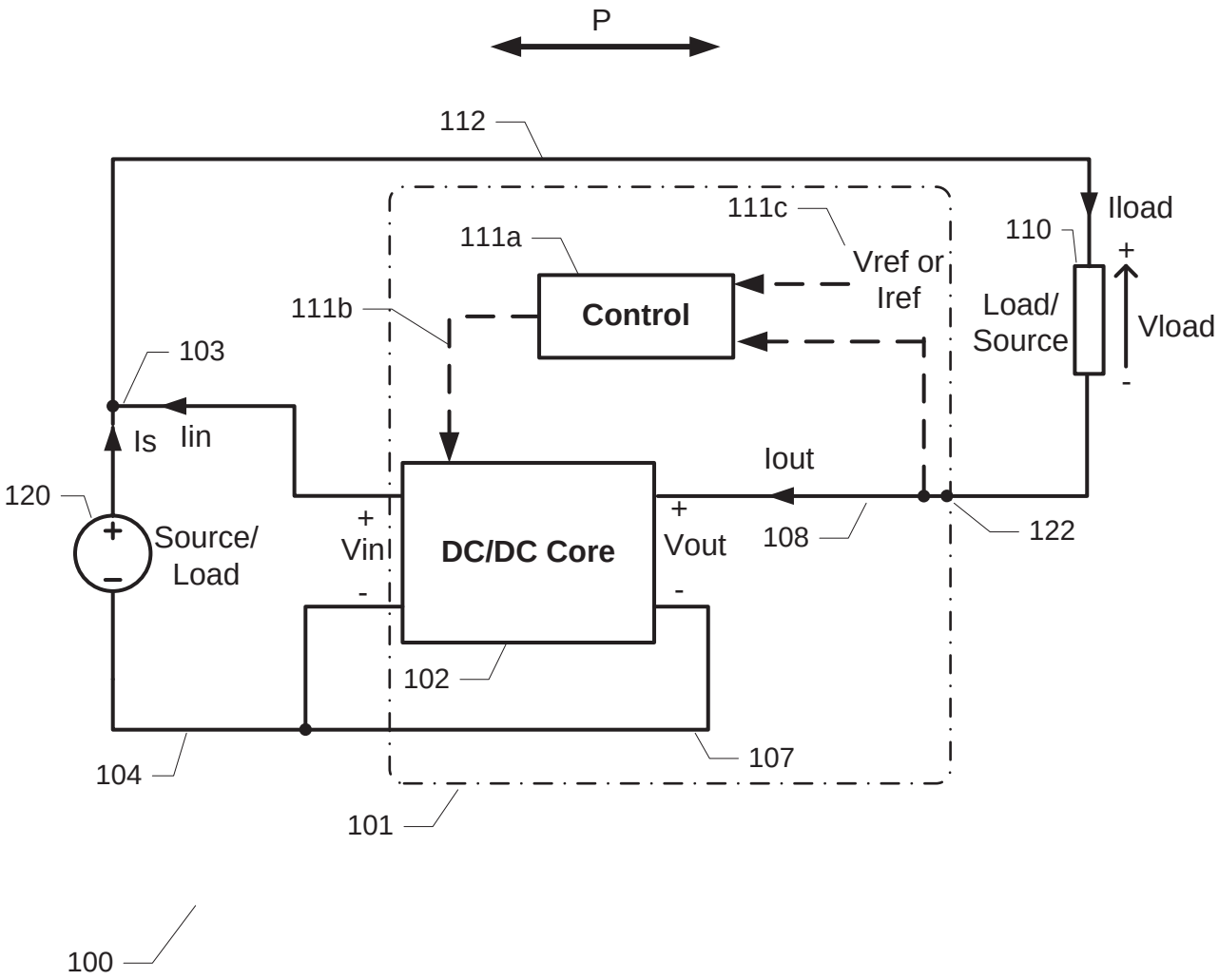
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FIG. 1

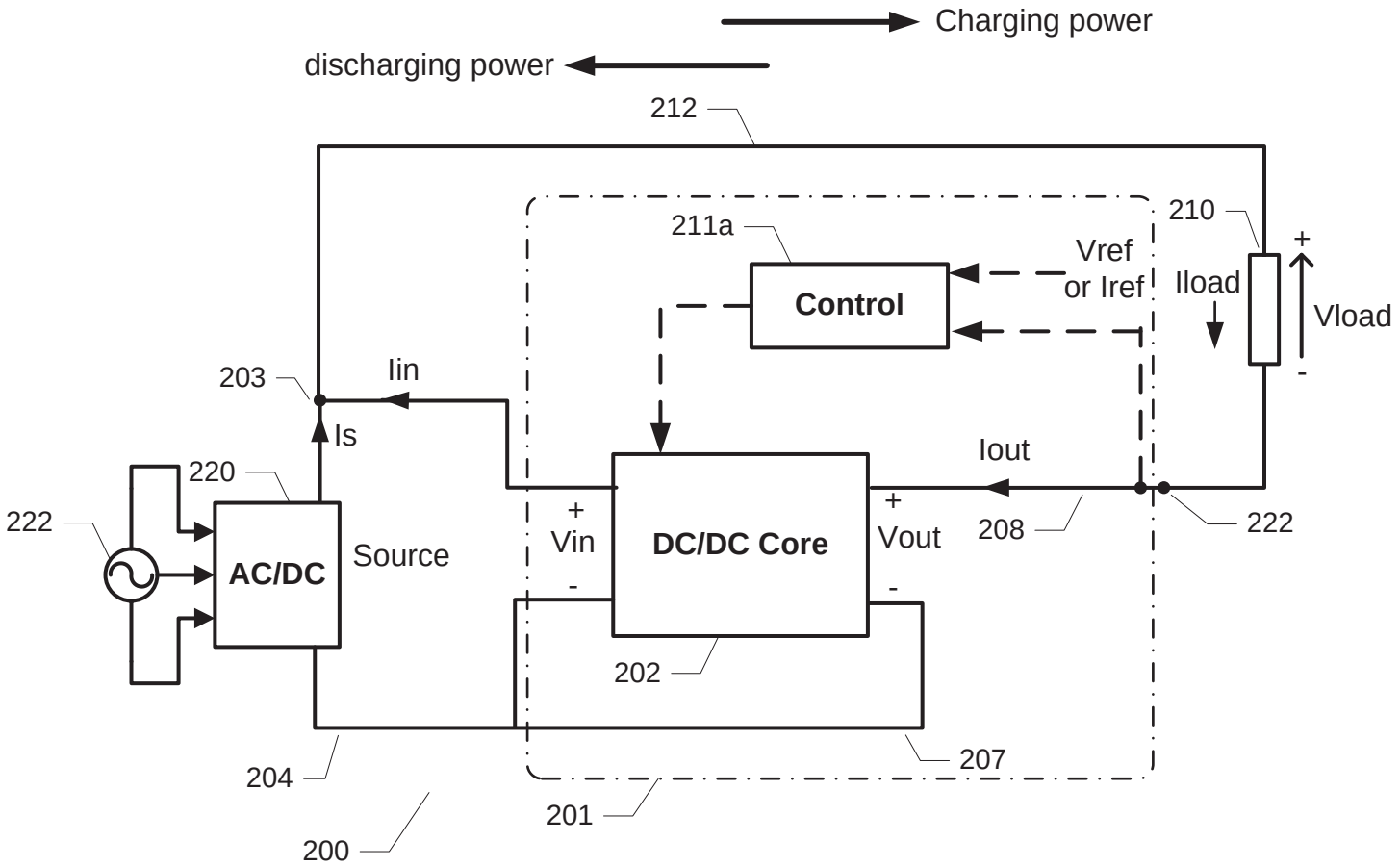
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FIG. 2

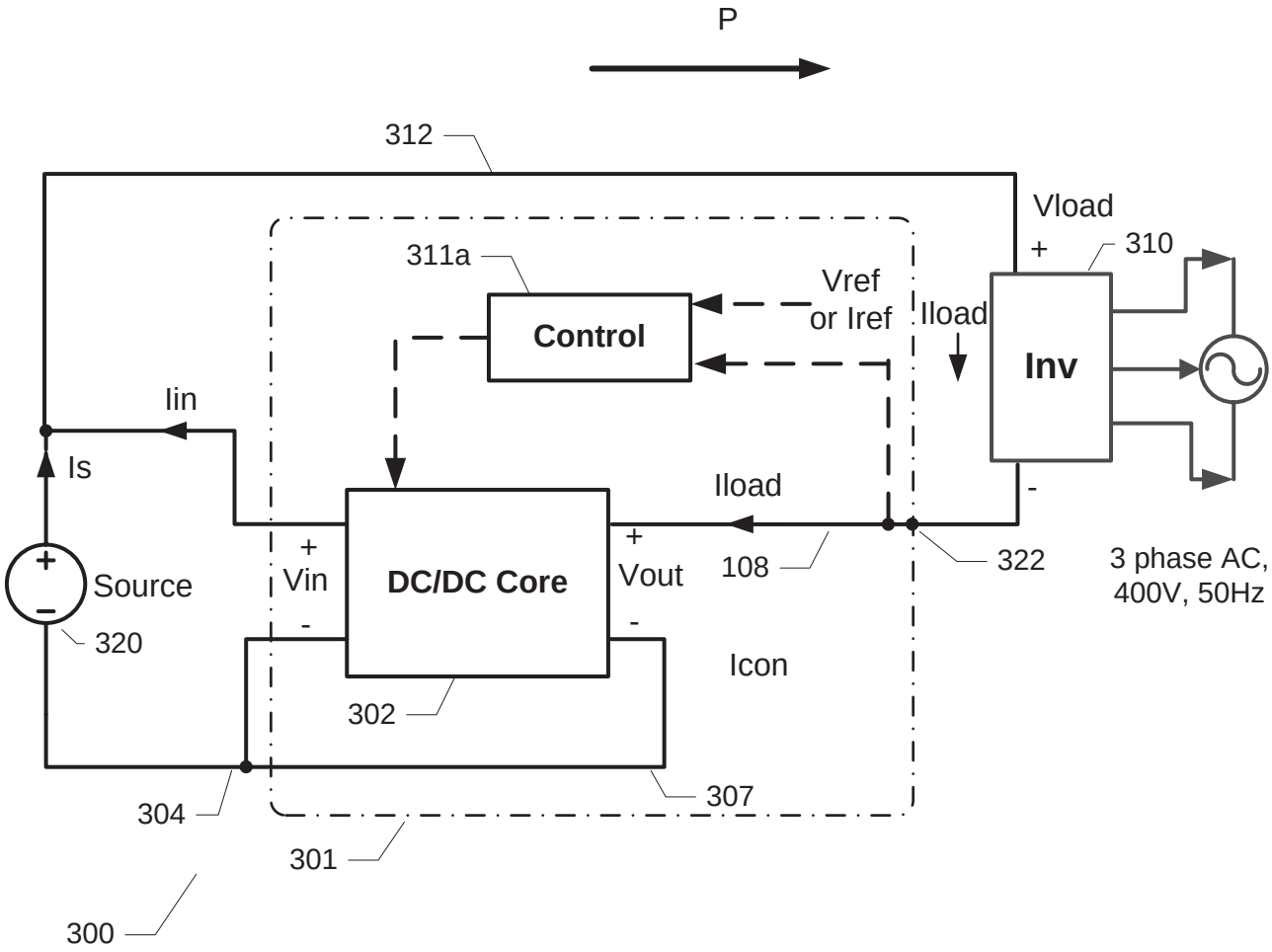
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FIG. 3

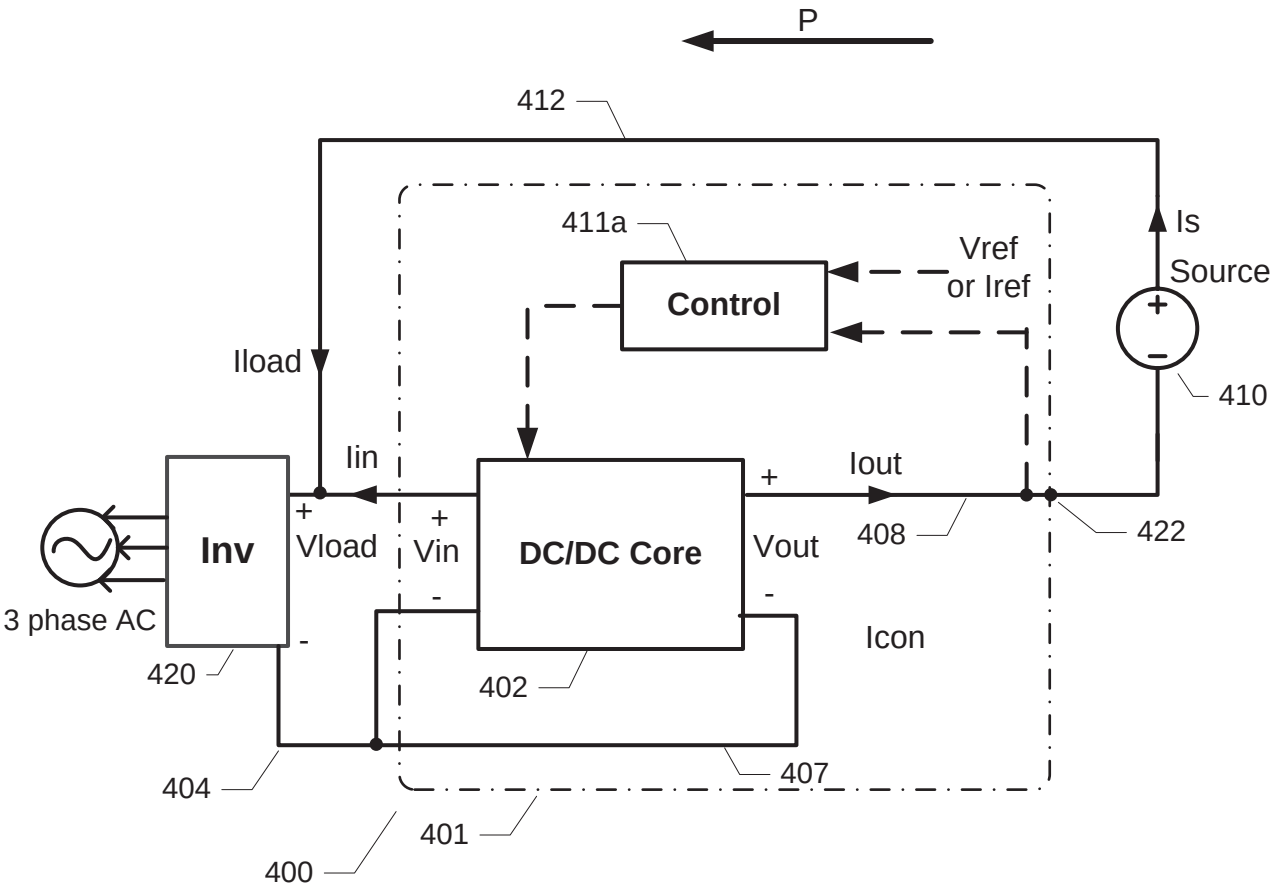
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FIG. 4

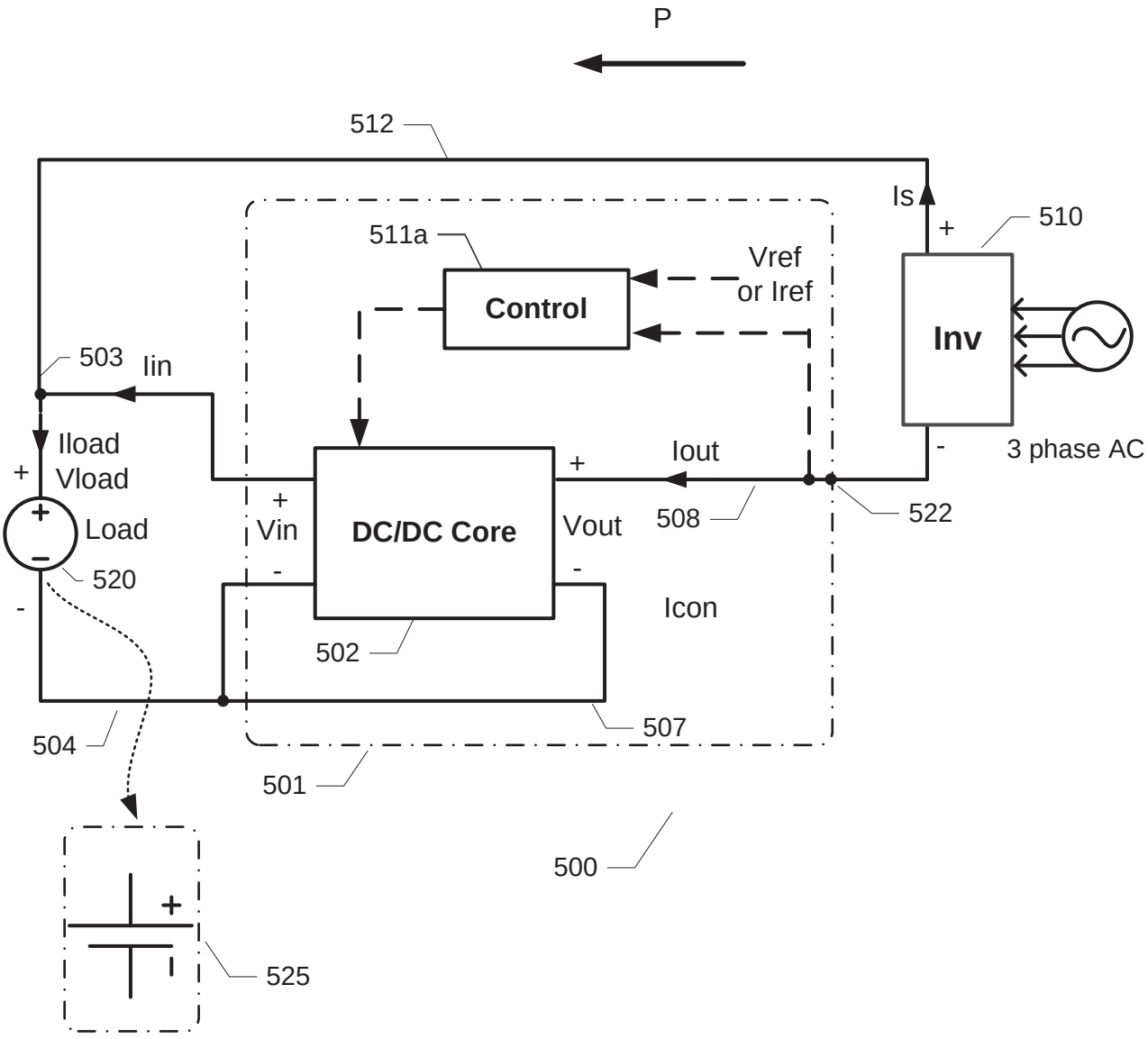
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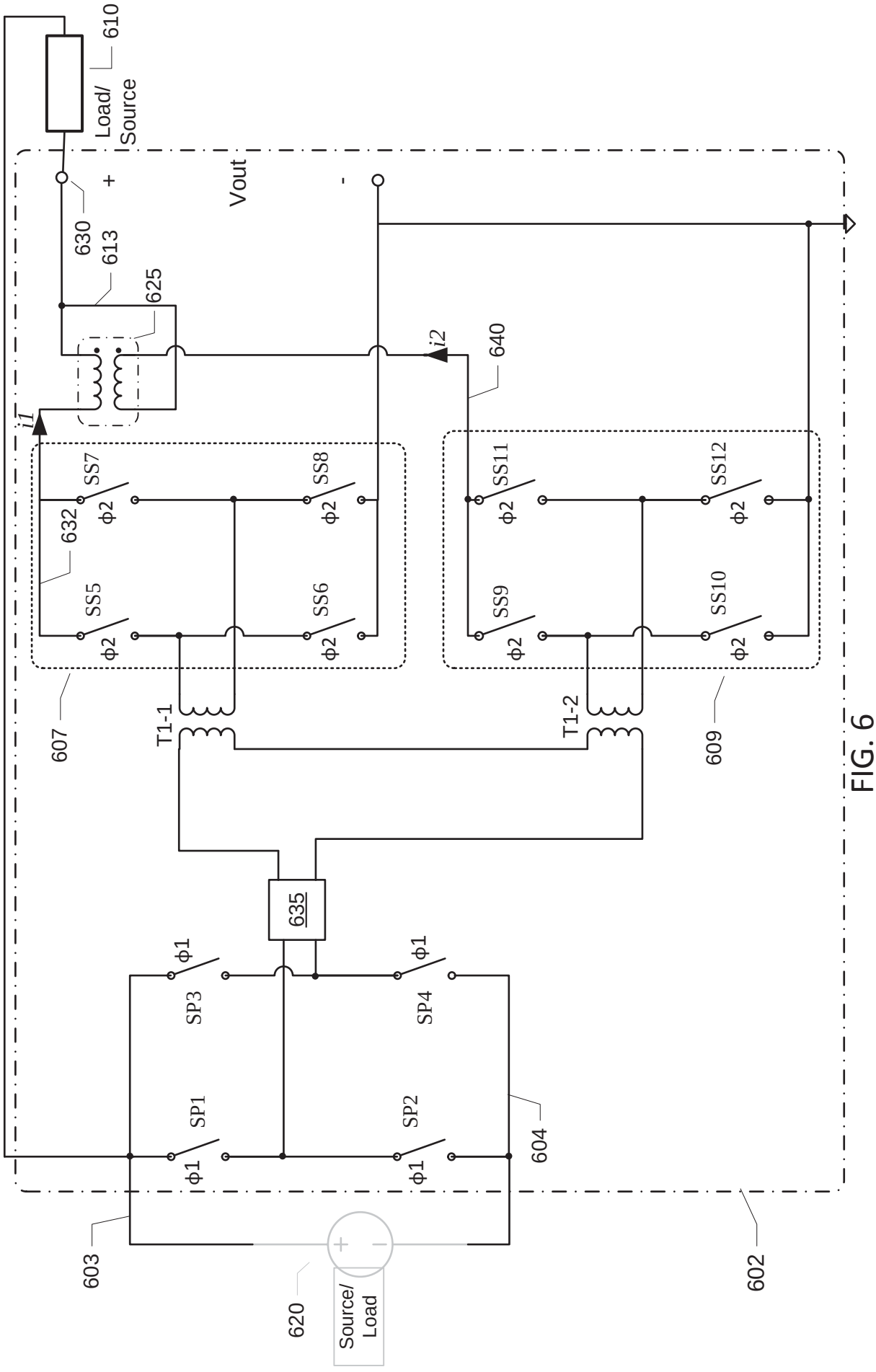
FIG. 5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613
625
Vout
+
-
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i2
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SS8
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SS11
SS12
SS9
SS10
ϕ2
607
609
T1-1
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635
ϕ1
SP3
SP4
SP1
SP2
604
603
620
Source/
Load
602

FIG. 6

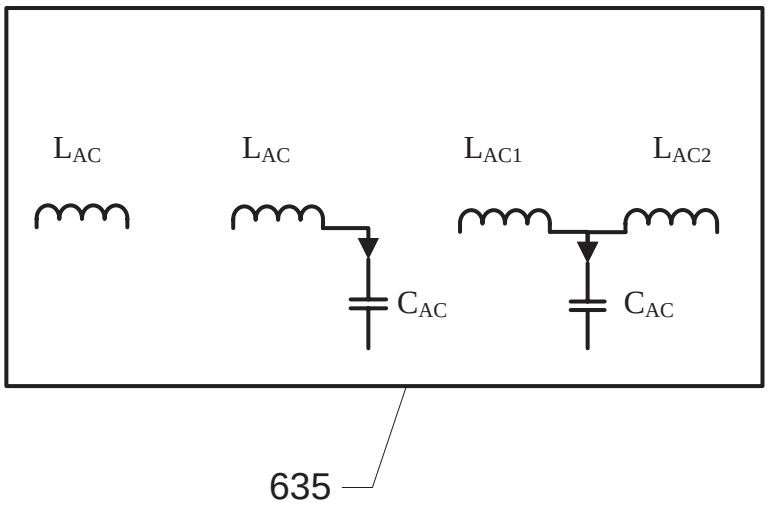

FIG. 7

High Efficiency Power Converter for a Doubly-fed SOEC/SOFC Systems

In IEEE APEC, Long Beach, March 20-24, 2016.

High Efficiency Power Converter for a Doubly-fed SOEC/SOFC System

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***Abstract*—Regenerative fuel cells (RFC) have become an attractive technology for energy storage systems due to their high energy density and lower end-of-life disposal concerns. However, high efficiency design of power conditioning unit (PCU) for RFC becomes challenging due to their asymmetrical current-power characteristics that are dependent on the operation mode (energy storage / energy supply). This paper proposes a new PCU architecture for grid-tie RFC with which the RFC's asymmetrical characteristic becomes less critical and thus a much more symmetrical power rating of the dc-dc converter for both operating modes is possible. This paper discusses the design considerations for this novel PCU, and verifies its operation principle with Matlab/Simulink simulations. Experimental results on a tailored dc-dc converter confirm the design simplifications for high efficiency operation along the entire power operating range of the RFC as well as the utilization of the same control strategy design for the two RFC operating modes.**

Keywords*—Bidirectional fuel cells, power conditioning, Interleaved boost converter, renewable energies, grid tie

I. Introduction

Over the last years renewable energies have experienced a strong development to become alternatives for conventional energy resources, among others due to the global awareness on limited fossil fuel resources and a widespread sensibility towards the environmental impacts. However, large scale integration of renewable energy sources present an important drawback because of their highly irregular and mostly unpredictable production [1], which causes high dynamics on the grid infrastructure and thus, electrical grid reliability is lowered. Large scale energy storage systems are therefore a potential solution to improve grid system reliability and stability when supplied by renewable energy sources [2]. With the utilization of information technologies to the grid system, consumers' behavior can become much more predictable, and therefore contribute to a better load regulation and an increased grid reliability [1]. The combination of renewable energy sources including energy storage systems and information technology systems can establish an equilibrium between energy production and demand, because surplus energy from renewable energy sources can be stored for later use to support the grid demands when necessary [3].

Regenerative or bidirectional fuel cells (RFC) could be an attractive technology for such large scale energy storage systems by means of hydrogen storage. Their particular benefits over traditional batteries are their high energy density of the fuel and their lower environmental disposal concerns [4]. In [5] an energy storage system based on RFC which couples the electricity grid with the natural gas grid is presented showing the potential of RFC for large scale energy storage.

Grid-tie energy storage systems based on RFC require power converter units to couple the grid with the RFC, to accommodate voltage levels and to regulate the system power flow. For traditional grid-tie fuel cell systems (not RFC), high efficiency PCU ranging from $96.8\,\%$ to $98\,\%$ have been demonstrated [6]. However, RFCs present a very asymmetrical current-power characteristic depending on the operating mode (i.e. energy storage or energy supply), leading to wide power rating spans with which the power conditioning unit (PCU) has to operate at high efficiency.

Different approaches to improve system performance and efficiency have been addressed. For instance, it has been verified in [7] that the efficiency of bidirectional dc-dc converters for grid-tie RFC systems can be greatly improved with the utilization of wide bandgap semiconductors such as SiC MOSFETs. Another way towards increasing efficiency is to reduce the switching energies of power devices in the RFC bidirectional dc-dc converters by means of soft switching as shown in [8]. Research on magnetics optimization based on planar magnetics can further increase both efficiency and power density [9]. Other investigations aim to compensate the slow dynamics of RFC by the inclusion of auxiliary sources. For instance, in [10] a dc-dc converter for FCs with an additional battery-based energy storage and a bidirectional dc-dc converter has proven to successfully support rapid load demand, and in [16] a grid-tie multiple port converter for fuel cells with super-capacitors as an auxiliary source has been proven to clearly increase the dynamic response compared to systems without auxiliary energy storage element.

Research performed to date is based on traditional PCU architectures for energy storage systems, as the one shown in Fig. 3. However, they are limited to the power rating symmetry characteristic of the PCU itself. Power symmetry implies that the power rating of the system is equal regardless the power flow direction. Considering the asymmetrical and wide power range of RFC, the design of high efficiency PCU for the entire operating area becomes very challenging. Furthermore, due to the power asymmetry of RFC, cooling effort for the PCU can be oversized depending on the operation mode, which greatly challenges high power density design. Due to the aforementioned drawbacks with the RFC systems, this paper presents a novel PCU architecture aiming for a much more symmetrical power rating of the dc-dc converter in both

978-1-4673-9550-2/16/$31.00 ©2016 IEEE

operation modes in order to simplify the high efficiency converter design. Design considerations are discussed, principle operation modes verified by simulations and experimentally confirmed on a 5 kW interleaved boost converter

II. Bidirectional SOEC/SOFC technology

Solid oxide electrolyzer cells/fuel cells (SOEC/-SOFC) are a kind of fuel cell technology which uses hydrogen as a fuel and takes advantage of the released energy during the reaction of hydrogen and oxygen to produce electricity. It has been proven that solid oxide cells (SOCs) have the capability to operate in bidirectional mode [11], also referred as regenerative mode. When hydrogen is used a fuel, reaction of hydrogen and oxygen is produced and an amount of energy is released generating electricity when connected to a load (SOFC operation). On the other hand, when current is forced to flow through the SOCs the electrolysis of water is produced and hydrogen is generated (SOEC operation).

Design and system specifications of a grid-tie power conditioning units for SOEC/SOFC systems are defined according to the current-voltage (I-V) characteristics of the SOEC/SOFC system, which is set by the number of stacked cells. However, I-V characteristics of SOEC/SOFC are highly dependent on operating temperature, fuel, pressure and degradation as explained in [12], [13]. This dependency must be considered in mature prototyping stages for long-term operation, specially the degradation ratio since it can strongly degrade the operating voltage ratings [12], [13]. The I-V characteristic for a single SOEC/SOFC provided by SOCs manufacturers is shown in Fig. 1, which will be the starting point of the PCU design.

As shown in the I-V curve from Fig. 1, SOCs operate at very low voltage and high currents, and for that reason it is necessary to stack many cells in series. Due to the immaturity of SOEC/SOFC technology, currently there are still mechanical limitations to obtain high power SOEC/SOFC systems, among others due to the maximum number of stackable cells, current density limitations, operating temperature, etc. Currently, the maximum current capability in SOEC mode is up to 60 A and up to 30 A in SOFC mode.

For the proposed system design in this work, fours stacks in series with 75 cells per stack has been chosen in agreement with SOCs manufacturers. Fig. 2a shows the I-V characteristics and Fig. 2b shows the current-power (I-P) characteristics for the SOEC/SOFC stacks system, which has been extrapolated from the I-V curve of a single cell Fig. 1. From the I-P curve in Fig. 2b, it can be seen that the power rating in SOFC mode is lower than in SOEC mode, which is due to the variation of the internal resistance and current direction [11]. This results in a very asymmetrical I-P characteristic, which leads to a wide operating power range for the PCU and thus, high efficiency design for the whole power range becomes challenging.

III. Grid-tie power conditioning unit for SOEC/SOFC systems

A. Traditional PCU architecture for SOEC/SOFC systems

Several power conditioning topologies can be used to realize SOEC/SOFC systems, and may differ depending on the particular application, system requirements and stacks structure

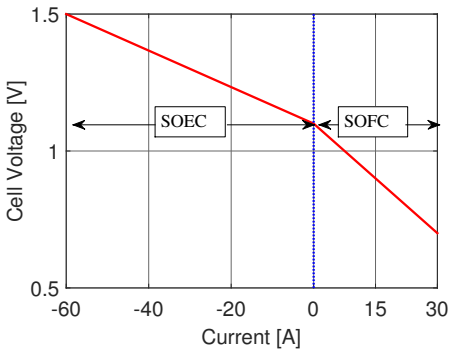
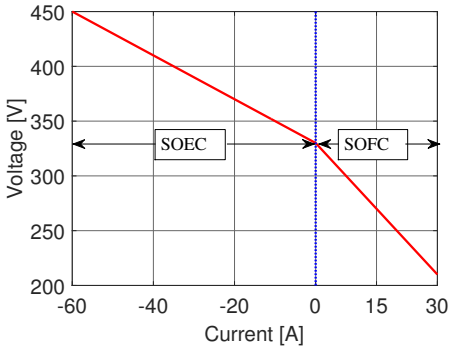
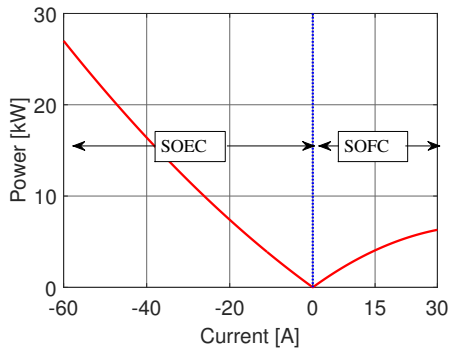


Fig. 1. Current-voltage characteristics of a single Solid Oxide Electrolyzer/Fuel Cell



(a) Current-voltage characteristics.



(b) Current-power characteristics.

Fig. 2. SOEC/SOFC stacks composed by 4 stacks in series with 75 cells/stack

[14]. However, the simplified architecture from Fig. 3 can be defined as a basis. System configuration is based on the parallel connection of an ac-dc converter, a dc-dc converter and the SOEC/SOFC stacks. Bidirectional power flow of the power converter units is required to allow the RFCs to operate in both modes. In particular, power flows from the grid to the SOCs when operating in SOEC mode (energy storage) and from the SOCs to the grid when operating in SOFC mode (energy generation). The dc-dc converter regulates the SOCs power flow and sets the required voltage level for the dc-link of the inverter.

TABLE I. TRADITIONAL PCU ARCHITECTURE: SOEC/SOFC AND DC-DC CONVERTER SPECIFICATIONS

Specification	SOEC	SOFC	dc-dc converter
Voltage [V]	330 - 450	210 - 330	210 - 450
Current [A]	0 - 60	0 - 30	0 - 60
Power rating [W]	27000	6300	27000
Power flow	from the grid	to the grid	bidirectional

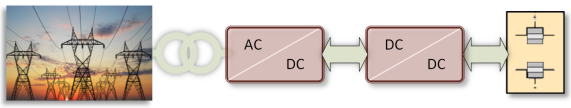


Fig. 3. Traditional PCU architecture for SOEC/SOFC systems.

According to the SOEC/SOFC stacks characteristics from Fig. 2, the system specifications for the dc-dc converter and the SOEC/SOFC stacks using the traditional PCU architecture are specified in Table I. With the traditional architecture from Fig. 3, a 27 kW power rated dc-dc converter would be required to cover the whole power range in both operation modes. This clearly leads to an oversized dc-dc power converter when operating in SOFC mode, which only requires a 6.3 kW rated system. Therefore, a different PCU architecture that counteracts the SOEC/SOFC power asymmetry would greatly simplify the converter design.

B. Novel doubly-fed SOEC/SOFC system

The novel PCU architecture presented in this work aims to achieve a much more symmetrical power operating range of dc-dc converter. The architecture is based on a dynamic PCU which connection varies according to the operation mode by the utilization of two single pole double through (SPDT) relays as subsequently explained. The proposed PCU architecture for both operation modes is shown in Fig. 4.

Under **SOFC mode**, shown in Fig. 4a, SOC stacks are connected in parallel to the dc-dc converter, which is the same scenario as with the traditional PCU architecture. Power is transferred from the SOCs to the output of the dc-dc converter P_{out} through the dc-dc converter. Therefore the power rating of the dc-dc converter P_{conv} is equal to the power generated by the SOFCs P_{sofc}, and the dc-dc converter electrical characteristics are defined as in equations 1, 2 and 3.

$$V_{conv(sofc)} = V_{sofc} \tag{1}$$

$$I_{conv(sofc)} = I_{sofc} \tag{2}$$

$$P_{conv(sofc)} = P_{soc} = V_{sofc} \cdot I_{sofc} \tag{3}$$

Under **SOEC mode**, shown in Fig. 4b, SOC stacks are connected in series with the dc-dc converter, and these two are then connected in parallel with the ac-dc converter. Energy required for the electrolysis of water and hydrogen generation is supplied from the grid through the ac-dc converter. For this operating mode the power rating of the dc-dc converter P_{conv} is the power difference between the output power of the dc-ac converter P_{inv} and the power consumed by the SOECs P_{soec}. The electrical characteristics of the dc-dc converter are expressed with equations 4, 5 and 6. From these equations, it can be inferred that in this scenario the power rating of the dc-dc converter will be reduced compared to the traditional PCU architecture. This is illustrated in the following design example.

$$V_{conv(soec)} = V_{inv} - V_{soec} \tag{4}$$

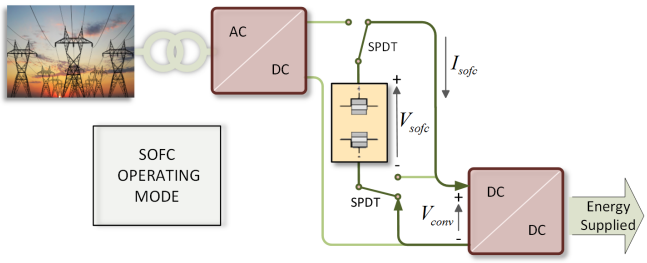
$$I_{conv,(soec)} = -I_{soec} \tag{5}$$

$$P_{conv(soec)} = P_{inv} - P_{soec} = V_{conv(soec)} \cdot I_{soec} \tag{6}$$

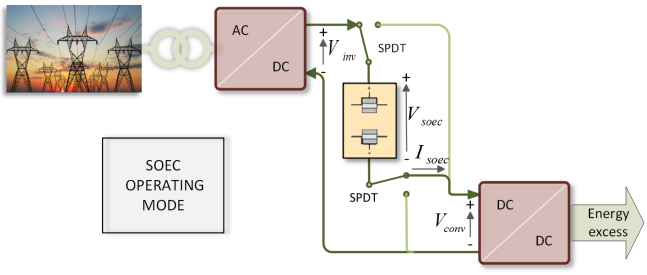
A 3-phase grid with $V_{line} = 230\,\text{V}$ is considered. Then the voltage at the output of the ac-dc converter is calculated with equation 7 as shown in [15].

$$V_{inv} = \sqrt{2} \cdot \sqrt{3} \cdot V_{line} \approx 560\,\text{V} \tag{7}$$

According to the SOEC/SOFC stacks characteristics from Fig. 2, system specifications for the dc-dc converter and the SOEC/SOFC stacks using the proposed PCU architecture can be redefined using equations 1-6 and with the specifications from Table II. Calculations show that using a dc-dc converter rated at 6.6 kW, a 27 kW-SOEC/6.3 kW-SOFC system can be realized using the proposed PCU architecture. In other words, in SOFC mode the dc-dc converter maximum power is $P_{conv(sofc)} = 6.3\,\text{kW}$ while in SOEC mode maximum power is $P_{conv(soec)} = 6.3\,\text{kW}$, resulting not only in a much more symmetrical dc-dc converter I-P characteristic, but also clearly a four times lower rated power system and thus a reduced cooling effort.



(a) SOFC mode

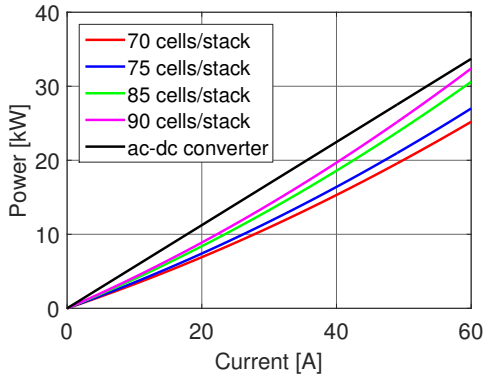


(b) SOEC mode

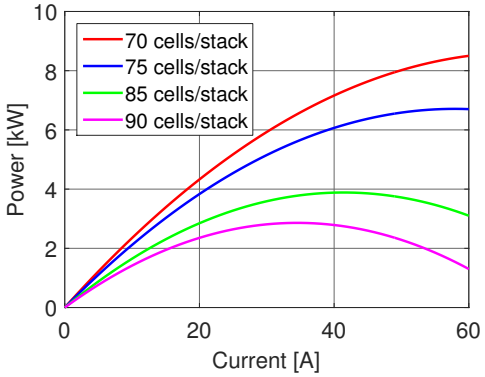
Fig. 4. Novel doubly-fed power conditioning architecture for SOEC/SOFC.

TABLE II. NOVEL PCU ARCHITECTURE: SOEC/SOFC AND DC-DC CONVERTER SPECIFICATIONS

Specification	SOEC	SOFC	dc-dc converter
Voltage [V]	330 - 450	210 - 330	110 - 330
Current [A]	0 - 60	0 - 30	0 - 60
Power rating [W]	27000	6300	6600
Power flow	from the grid	to the grid	unidirectional



(a) SOEC/SOFC and ac-dc converter

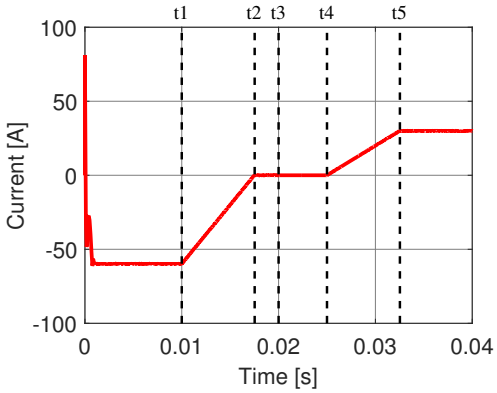


(b) dc-dc converter

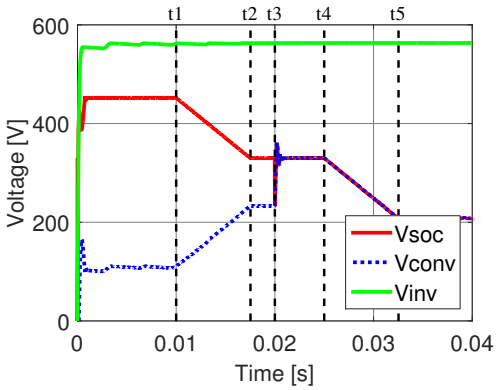
Fig. 5. Current-power characteristics for different number of cells per stack with four stacks in series.

The proposed system is subsequently analyzed when operating under SOEC mode with different number of SOEC/SOFC cells by calculating the dc-dc converter specifications as previously shown. Fig. 5a shows the I-P characteristics of the SOEC/SOFC stacks and Fig. 5b shows the I-P characteristics for the dc-dc converter. Fig. 5 shows that by increasing the number of cells the power consumed by the SOEC stacks increases. Since the voltage across the SOEC stacks moves towards the inverter voltage with an increasing number of cells, the voltage at the input of the dc-dc converter decreases. This causes a significant reduction of the power rating of the dc-dc converter.

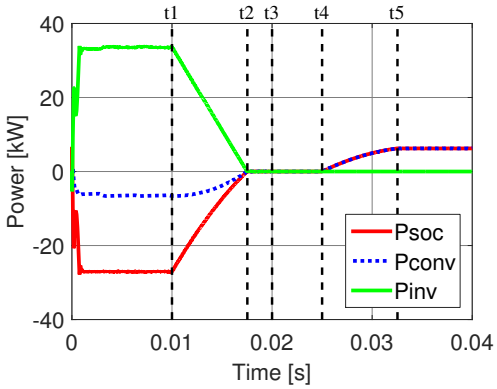
In order to describe the circuit operation in more detail, simulations of the entire PCU including a closed-loop SOEC/SOFC current control have been performed with a full bridge rectifier connected to the 3-phase grid and a boost dc-dc converter. Two ideal SPDT relays are used to switch from one operating mode to another, which occurs at very low frequencies because the operating mode is related to the grid power excess and power demand rather than conventional PWM mode of the dc-dc converter itself. Simulations are performed according to the specifications from Table II. Fig. 6a shows the current through the SOEC/SOFC system I_{conv}, whereas Fig. 6b shows the inverter voltage V_{inv}, the voltage across the SOEC/SOFC stacks V_{soec} / V_{sofc} and the input voltage of the dc-dc converter V_{conv}. Fig. 6c shows the inverter



(a) Current through the SOEC/SOFC stacks ((+) for SOEC and (-) for SOFC)



(b) Voltage at the rectifier output, SOCs and input of dc-dc converter



(c) Power at the rectifier output, SOCs and dc-dc converter input

Fig. 6. Simulation results

power P_{inv}, the power of the SOEC/SOFC stacks P_{soec} / P_{sofc} and the power of the dc-dc converter P_{conv}.

Step 1 (before t_1): System is in steady state, operating in SOEC mode, as depicted in Fig. 4b. Current reference is regulated to the maximum SOEC current capability $I_{soec,max} = -60$ A. The input voltage of the dc-dc converter V_{conv} is the difference between inverter voltage and SOEC stacks voltage as expressed by equation 4, and thus P_{conv} corresponds to

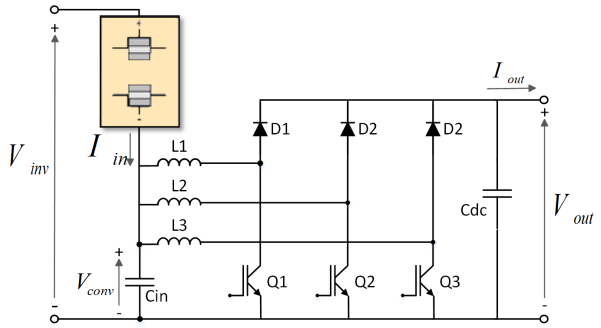


Fig. 7. Three stages interleaved boost converter schematic operating in SOEC mode.

$P_{inv} - P_{soec}$ (Eq. 6). Note that P_{soec} is negative in Fig. 6c, because SOCs are consuming power.

Step 2 ($t_1 - t_2$): Before switching the operating mode, current reference decreases to zero with a certain slope to prevent any over-voltages on the SOEC/SOFC stacks. At the end of this period, voltage across the SOEC/SOFC stacks reaches the open-circuit voltage.

Step 3 (t_3): The SPDT relays are switched, and the system connection is changed to SOFC mode as shown in Fig. 4a. A step variation of V_{conv} occurs since the input voltage condition changes from Eq. 4 to Eq. 1.

Step 4 ($t_3 - t_4$): Due to the V_{conv} step variation, voltage oscillations occur across SOEC/SOFC stacks and V_{conv}. A short period of time with zero current is held to stabilize the system.

Step 5 ($t_4 - t_5$): Current reference is driven with a certain slope to the maximum SOFC current capability $I_{sofc,max} = 30$ A.

Step 6 ($t_5 - end$): Systems is in steady state, operating in SOFC mode, where V_{conv}= V_{sofc} and P_{conv}=P_{sofc}, as expressed with Eq. 1 and Eq. 3, respectively.

IV. DC-DC Converter

The main focus of this paper is the verification of the feasibility of the proposed PCU, for that reason a tailored dc-dc converter with a closed-loop control has been implemented for the defined SOEC/SOFC system in table II.

A. Power stage

A three-stages Interleaved Boost Converter (IBC) is used in this work as shown in Fig. 7 to test the proposed PCU architecture. The IBC topology is a widely accepted topology for fuel cell power conditioning systems due to its benefits [17]-[20]. SOCs lifetime can be dramatically reduced with large ripple current [21], thus by means of interleaving the inductor currents, the input current ripple amplitude can be reduced [20], thus greatly improving the lifespan of SOCs. Moreover, the output voltage frequency is also increased, therefore reducing the voltage ripple and allowing a reduction of dc-link capacitors [20].

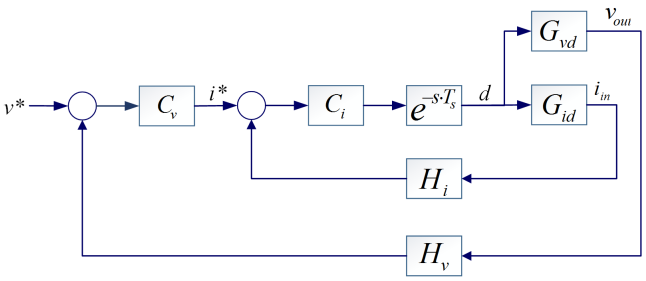


Fig. 8. Block diagram of the double-loop control strategy.

Converter's component details are given in Table III. Output voltage is set to 600 V in order to reach a proper dc-link voltage level to feed energy to the grid and the switching frequency is 25 kHz.

TABLE III. Converter's component details

Inductors $L_1 - L_3$	1 mH KoolMμ core
DC-Link cap. (I) C_{DC}	20 µF/800 V Film Cap.: 2 in parallel
DC-Link cap. (II) C_{DC}	12 nF/800 V Film Cap.: 3 in parallel
Input cap. C_{in}	50 µF/800 V Film Cap.
IGBTs $Q_1 - Q_3$	IKW25N120H3 1200 V/25 A
Diodes $D_1 - D_3$	IDH08S120 1200 V/7.5 A

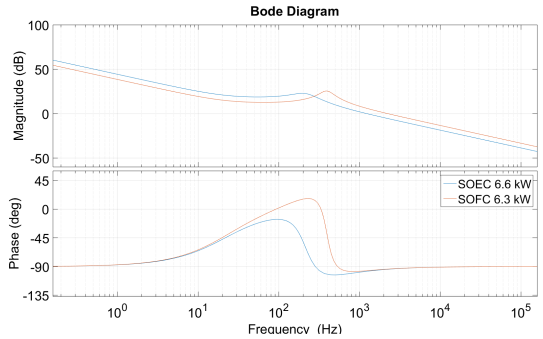
B. Closed-loop control strategy

A DSP-based closed-loop control system has been implemented. It is intended to design and apply the established control loop strategy for both operating modes (SOEC and SOFC) by considering the input-output I-V characteristics of the dc-dc converter in the design process.

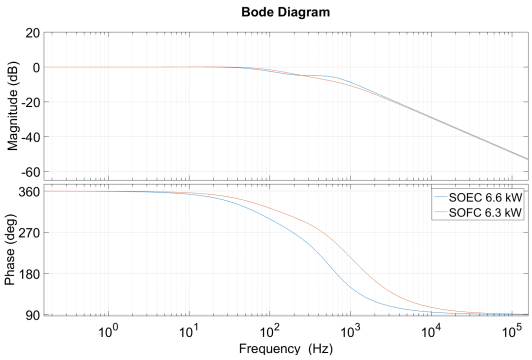
The closed-loop control strategy is designed in order to reach and keep the 600 V output voltage and to keep the input power of the dc-dc converter inside the allowed limits of the SOC stacks.

The classical double-loop control strategy represented in Fig. 8 is applied [22], where G_{id} refers to the duty cycle-to-input current transfer function and G_{vd} refers to the duty cycle-to-output voltage transfer function. This controller requires the measurement of two variables, i.e. the dc output voltage and current at the input of the converter, which are filtered by second-order filters from the measurement circuits, H_i and H_v, such that the high frequency components are properly attenuated. Classical proportional-integral (PI) controllers C_v and C_i are used for voltage and current compensation. In addition, a soft start-up procedure has been integrated to the control system, so during the converter turn-on voltage overshoots are avoided. The soft start-up consists of a reference signal v_{ref} with a certain slope from 0 to the desired reference.

Referring to the double-loop control, the fast inner loop is used to regulate the average input current using the controller C_i. The output voltage is regulated with the slower outer loop with the controller C_v. To obtain the closed-loop system stability, the inner loop bandwidth has to be larger than the outer loop [22]. Due to the slow dynamics of the SOCs the



(a) Current loop gain.



(b) Closed-loop response

Fig. 9. Control system Bode Plots

outer loop bandwidth has to be kept small and the inner current loop needs to assure reaching the faster transient response of the dc-dc converter.

State-space average model for the IBC is developed as performed in [23], [24], to thereafter calculate the system transfer functions shown in Eq. 8 and Eq. 9.

$$G_{id} = \left.\frac{\tilde{i}_{in}(s)}{\tilde{d}(s)}\right|_{\tilde{v}_{conv}(s)=0} = \frac{V_{conv}}{R \cdot D'^2} \cdot \frac{1 + s\frac{1}{R \cdot C_{dc}}}{1 + s\frac{L}{R \cdot D'^2} + s^2 \frac{L \cdot C_{dc}}{D'}} \tag{8}$$

$$G_{vd} = \left.\frac{\tilde{v}_c(s)}{\tilde{d}(s)}\right|_{\tilde{v}_{conv}(s)=0} = \frac{V_{conv}}{D'} \cdot \frac{1 - s\frac{L}{R \cdot D'^2}}{1 + s\frac{L}{R \cdot D'^2} + s^2 \frac{L \cdot C_{dc}}{D'}} \tag{9}$$

Where $D' = 1 - D$, $R = V_{out}/I_{out}$ and $L = L_1 = L_2 = L_3$.

PI controller for inner current loop is designed for full load condition obtaining the bode diagram shown in Fig. 9a. The loop is closed at the cross-over frequency $f_c = 1.25\,\text{kHz}$ with a phase margin of $83°$ for the SOEC mode at full load and at $f_c = 2.26\,\text{kHz}$ with a phase margin of $86°$ for the SOFC mode on full load condition. Once the stability of the inner current loop is obtained, the outer voltage loop controller is calculated for full load condition and the closed-loop response shown in Fig. 9b is obtained.

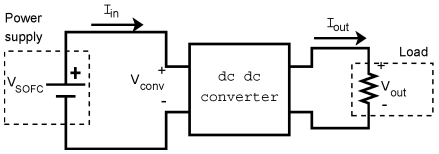
V. Experimental Results

Experimental tests have been carried out independently for each operating mode. Tests under SOFC mode have been executed simply using a laboratory power supply at the dc-dc converter input and an output resistive load emulating the power demand from the dc-link side. Tests under SOEC mode have been carried out using a dc source to supply the ac-dc converter output voltage and an electronic load in fixed voltage mode with a dynamic resistance emulating the SOEC stacks power consumption. Fig. 10 shows the diagrams representing the experimental set-up.

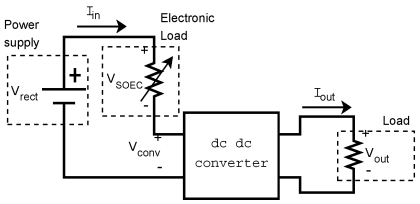
Interleaved inductor currents and input current waveforms are shown in Fig. 11. From these results it is verified that the input current ripple is greatly reduced with the interleaving technique, therefore demonstrating an attractive topology for RFC systems.

A. *Efficiency measurements*

Efficiencies of the dc-dc converter are measured by using a power analyser PPA5530 from N4L. The efficiencies have been measured under SOEC and SOFC operating modes independently according to dc-dc converter I-P and I-V characteristics derived from the SOEC/SOFC stacks characteristics from Fig. 2. The results are shown in Fig. 12, clearly demonstrating that since the dc-dc converter can be rated for a similar power level in both operation modes, high efficiencies in both modes are possible. Note that efficiency curves are close to each other resulting in similar thermal stress for both modes which can simplify the heat sink design.



(a) SOFC tests



(b) SOEC tests

Fig. 10. Experimental set-up

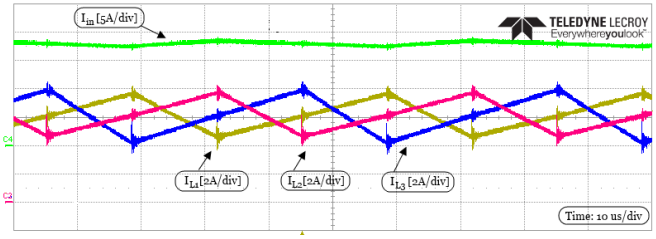
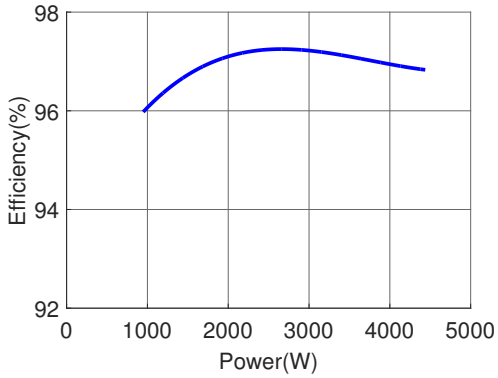
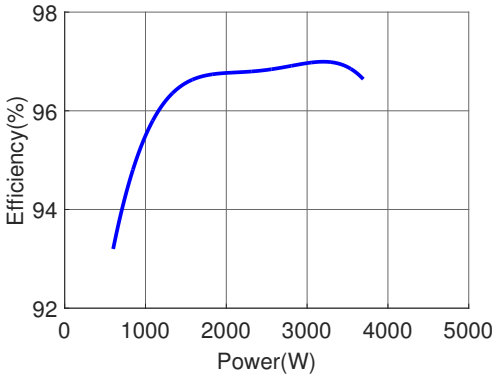


Fig. 11. Experimental results: 3 stages IBC inductors current (I_{L1},I_{L2} and I_{L3} and input current I_{in}.



(a) SOFC mode



(b) SOEC mode

Fig. 12. Experimental and theoretical efficiency curves

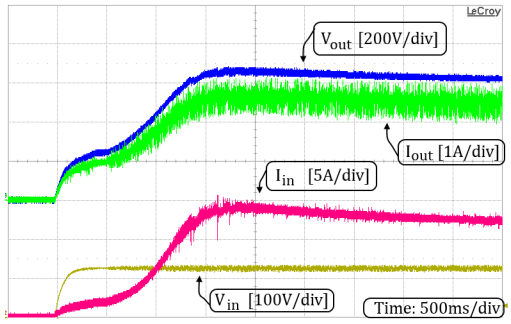


Fig. 13. Soft start-up test

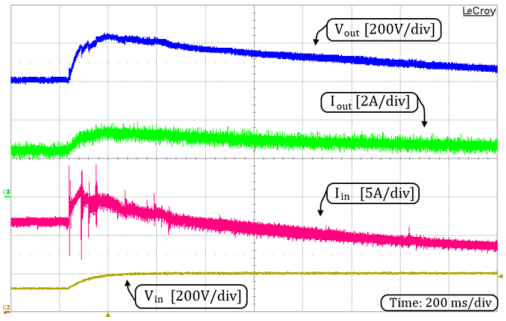


Fig. 15. SOFC voltage 80 V step-up

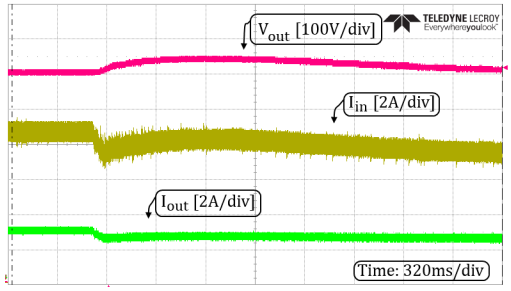


Fig. 14. 10% load step-up

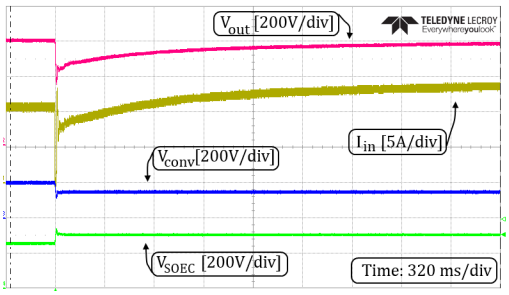


Fig. 16. SOEC voltage 50 V step-up

B. *Closed-loop tests*

To verify the proposed PCU including its control design is suitable for both operating modes, closed-loop measurements are performed.

Fig. 13 shows the main converter waveforms during the system turn-on when a step from 0-120 V occurs at the input voltage. Steady-state condition is reached in approximately 4 s, with a very smooth output voltage response having a small overshoot of 20 V. Fig. 14 shows the system response for an output load step of 10 % of the rated load, where the output voltage and input current have no oscillations and a small undershoot is appreciated. Fig. 15 shows the system response for SOFC voltage (V_{in}) 80 V step-up, where the inner current loop suffers oscillations but the outer voltage loop has negligible oscillations and in 2 s steady-state is reached. Fig. 16 shows the system response for SOEC voltage 50 V step-up. Notice that the inverter voltage has been limited to 450 V to protect the voltage supply from over rated current. Similarly as with the previous test, few oscillations in the current are present at the step time, but the output voltage has a smooth response without noticeable oscillations, and reaching a steady-state condition within 2.2 s. As explained throughout the system operation principle and simulations, the inverter voltage is shared across the SOEC and the dc-dc converter, leading to a reduced power rating of the dc-dc converter.

VI. Conclusion

This paper has presented the design considerations for a novel PCU for grid-tie SOEC/SOFC system. A 6.7 kW dc-dc converter has been implemented which aims to be able to regulate 27 kW-SOEC/6.3 kW-SOFC stacks, with efficiencies of up to 97 % in SOEC mode and 97.3 % in SOFC mode. Furthermore, it has been verified that the power rating reduction of the dc-dc converter in SOEC mode leads to a more symmetrical I-P characteristic of dc-dc converter which eases the design for a high efficiency converter, leading to similar efficiency curves for both operation modes of the SOEC/SOFC system. This not only results in similar losses in both modes, but can also be beneficial in terms of simplified heat sink design of the dc-dc converter power stage. Closed-loop experimental tests show that with a dual-loop control strategy, system robustness in terms of steady-state and transient performance is reliable under both operating modes SOEC and SOFC at the same time. Thus, the proposed PCU architecture can be a very attractive alternative for high efficiency RFC systems.

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High efficiency non-isolated three port DC-DC converter for PV-battery systems

In IEEE IPEMC-ECCE Asia, Hefei, May 22-26, 2016.

High Efficiency Non-isolated Three Port DC-DC Converter for PV-Battery Systems

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***Abstract*—This paper presents a nonisolated Three Port Converter (TPC) with a unidirectional port for photovoltaic (PV) panels and a bidirectional port for energy storage. With the proposed topology single power conversion is performed between each port, so high efficiencies are obtained. A theoretical analysis is carried out to analyze all operating modes and design considerations with the main equations are given. A 4kW laboratory prototype is developed and tested under all operating conditions. Results obtained feature on efficiencies higher than 97% for all operating modes and all power levels from light load to full load.**

Keywords—Energy storage, multiport converter, boost, buck, interleaved converter.

I. INTRODUCTION

Renewable energy generation has been gaining increasing interest in the last two decades of which photovoltaic (PV) generation is one of the most significant with a total global capacity of 177GW in 2014 [1]. However, the continuously growing number of decentralized energy sources negatively affects the quality of the grid voltage [2, 3]. In particular, the influence of distributed energy production has caused the power quality to deteriorate. In some areas the quality impaired so much such that the PV-inverter disconnects from the grid, due to the power quality being outside the range of the inverter setting resulting in disability to feed power to the grid [2, 3]. However, the deterioration in grid quality is not the only reason that the PV-plant work less reliable. Typically the electricity customers can experience a very high grid voltage in their electrical installations due to high injection of power from PV-plants to the grid [2, 3].

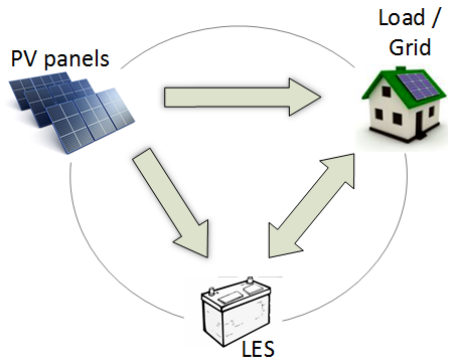

Fig 1. Power flow for a PV system with LES and grid support.

A local energy storage (LES) system can supply and buffer energy and thereby support the power quality of the electricity grid [3, 4, 5]. If the energy that severely deteriorates the power quality, instead of being feed directly to the electricity grid with full power is send in a smaller degree to the grid and in larger degree to the local energy storage system this resolves the problems with high power over a low timeframe. Later in the day when the production from the PV-plant is lower, power from the LES can be fed to the consumer, thereby equalizing the power to the grid over the day, and hence reducing the impact on the power quality. On the other hand, when distributed energy sources produce such amount of energy that the grid cannot support, local energy storage can support the grid by storing the surplus energy from other resources [3, 4, 5]. According to this description, power systems for grid-connected PV systems with LES need to operate with multiple power flows as shown in Fig 1.

Therefore, during the last decade an interest on research about three port dc-dc converters (TPC) capable of interfacing PVs to DC bus with energy storage systems has arisen. Previous work has demonstrated the advantages of TPC over single-input-single-output (SISO) topologies such as high efficiency, high power density, reduction of conversion stages and centralized control system and energy management system [6, 7, 8]. TPC topologies can be classified into three main categories: non-isolated, partially isolated, where two ports have a common ground, and isolated topologies.

Isolated and partially isolated TPC are generally derived from three basic cells [9]: half bridge, boost-half bridge and full bridge. Isolated topologies do not require a dc common bus, but rather use a magnetic coupling through a high-frequency transformer [9]. On the other hand, partially isolated topologies might require a common dc bus as well as magnetic coupling [9]. Besides providing isolation, these topologies have the advantages of wide voltage ranges [10, 11], zero-current and zero-voltage switching [12, 13] and simplicity to increment the number of ports [14, 15].

Non-isolated topologies are mostly derived from common step-down and step-up converters such as buck and boost dc-dc converters. The main advantages of non-isolated TPC compared to isolated and partially isolated topologies are their

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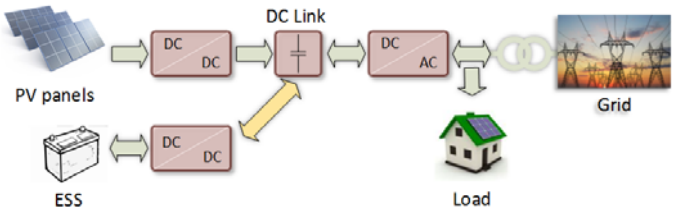


Fig 2. Block diagram of the traditional grid-connected PV plant with energy storage system (ESS) or LES.

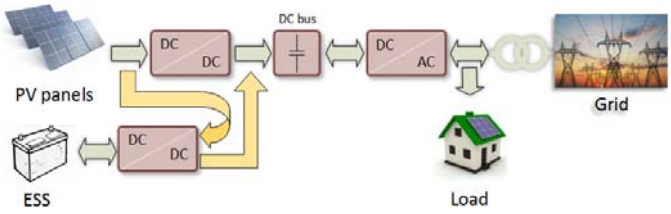


Fig 3. Block diagram of the proposed grid-connected PV plant with energy storage system (ESS) or LES.

high efficiency and high power density. Generally, these topologies are most commonly found to be two independent converters with a common DC bus as shown in Fig. 2 [16, 17]. This results in a lower efficiency when transferring energy from PV panels to the LES due to energy has to be converted at least two times.

Where previous work generally reports efficiency improvements in power conversion units by utilizing new kind of switching devices made of Silicon Carbide [18, 19, 20] or proposing optimized design procedures for the given topology [21, 22], this work follows a more direct approach by reducing the number of conversion stages while keeping its simplicity. This is done by adapting well-known buck and boost topologies capable of operating with all the power flows within one power conversion stage as shown in Fig.3. The objectives of this paper are to explain the different operation modes and design of the converter together with experimental results of the converter focusing on steady-state analysis and efficiency analysis under all operation modes.

II. PROPOSED TOPOLOGY

The proposed converter topology is illustrated in Fig 4. This converter can interface three different ports, i.e. battery, PV panels and the load. It allows operation as a single-input-single-output (SISO), dual-input-single-output (DISO) and single-input-dual-output (SIDO) converter, fulfilling in that way all the required power flows sketched in Fig 1.

A. Circuit description

The converter is directly derived from common and well-known buck and boost topologies. In applications where high voltage gain is not required, buck and boost topologies typically imply improved performance and efficiency [23, 24] due to the low number of passive components and power devices. Furthermore, simplicity of the topology and its well reported modelling equations, eases the design of the power stage as well as the control system.

An important drawback of conventional buck and boost converters are their poor performance for high-power high-current applications since the power is processed by two

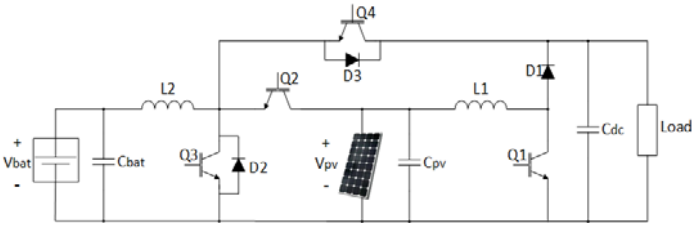


Fig 4. Proposed TPC topology.

power devices and required passive devices increase in size. Interleaving of converters is a common practice in buck and boost converters to increase the power rating and obtain a better performance and reduce passive components [25]. However, it comes with the challenges of unequal current sharing and increased complexity of the power stage. Besides reaching higher power levels, other benefits can be obtained by means of interleaving as have been addressed in other references:

- Input current and output voltage ripple reduction [26].
- Reduced EMI filter [27].
- Phase-shedding to improve efficiency at light load [28]
- Utilization of coupled magnetics to increase power density [29].

The proposed converter is composed by four power devices Q1, Q2, Q3 and Q4 which are the controllable switches to regulate the power flow and the voltages at the different ports. For D2 and D3 integrated freewheeling diodes can be used if IGBTs are utilized. On the other hand, for optimal efficiency operation external fast recovery or SiC diodes can be used. Two inductors are necessary, where L1 belongs to the boost stage for energy transfer from PV to Load and L2 is used for energy storage during the battery charge and discharge operation. Cpv and Cbat refer to the input capacitors of PV panels and battery respectively and Cdc refers to the capacitors of the DC bus. The load emulates the power demand from the household or the grid.

B. Operational principle

In Fig the equivalent circuits for each operating mode are highlighted. Maximum two controllable switches are used for the same operating mode, while the other two are inactive. The different case scenarios are subsequently described:

1. *PV panels to Load/Grid (*Fig 5a): When power is generated from the PV panels and the battery is fully charged, energy is transferred from the PV side to the loads through the boost stage L1-Q1-D1. Only one control signal (d1) for Q1 is required.
2. *PV panels to Battery (*Fig 5b): When there is no load, power generated from PV panels is used to charge the batteries through the buck stage L2-Q2-D2. In this case scenario the direct energy storage PV-Battery sketched in Fig is performed. One control signal (d2) for Q2 is required.
3. *PV panels to Battery and Load (*Fig 5c)*:* When load power is low, power from PV panels is partially used to charge the battery and sent to the load through both the buck and boost stage.

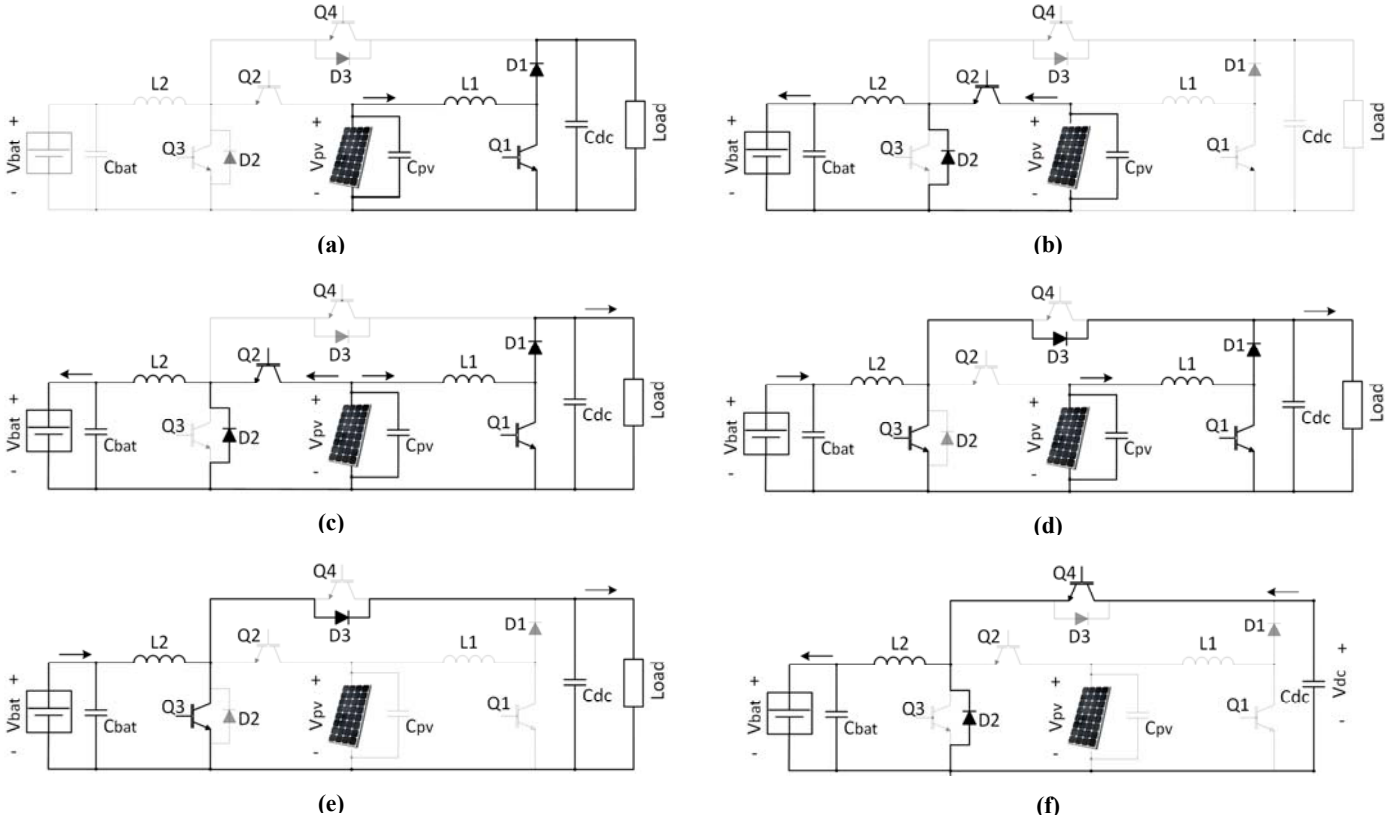


Fig 5. Operational circuitry for all operating modes, (a) PV to Load, (b) Direct storage PV to Battery, (c) PV to Battery and Load, (d) PV and Battery to Load, (e) Battery to Load, (f) Battery charge from Grid.

4. *PV panels and Battery to Load/Grid (*Fig 5d): When the load demand is high or the grid needs to be supported, power can be supplied from both, PV panels and battery. Power from PV panels is again supplied to the load from the boost stage L1-Q1-D1. Power from the battery to the Load is transferred through the boost stage L2-Q3-D3. Two control signals are required, d1 for Q1 and d3 for Q3.
5. *Battery to Load* (Fig 5e)*:* When no power is generated from the PV panels, the load can be supplied with the battery through the boost stage L2-Q3-D3 using one control signal d3.
6. *Grid to Battery* (Fig 5f)*:* For a grid-connected application, the battery can be charged from the grid through the buck converter composed by L2-Q4-D2. Only one control signal (d4) for Q4 is required.

III. DESIGN PROCEDURE

The proposed topology allows an easy modular design to achieve higher power levels by means of interleaving as previously explained. Therefore, for the following design equations, interleaving of stages will also be considered.

A. DC Voltage Gain

Assuming an ideal converter operating in steady-state and CCM, by using the volt-second balance law on inductors L1 and L2 DC voltage gain for each operating mode can be calculated according to Eqs. 1-4.

$$\frac{V_{DC}}{V_{PV}} = \frac{1}{1-d1} \quad PV\ to\ Load \tag{1}$$

$$\frac{V_{Bat}}{V_{PV}} = d2 \quad PV\ to\ Battery \tag{2}$$

$$\frac{V_{DC}}{V_{Bat}} = \frac{1}{1-d3} \quad Battery\ to\ Load \tag{3}$$

$$\frac{V_{Bat}}{V_{DC}} = d4 \quad DC\ bus\ to\ Battery \tag{4}$$

B. DC and AC Current and Voltage of Passive Components

DC current through the inductors and voltage across the capacitors are given in Eqs. (5)-(9). Note that the current sign in the following equations is defined according to the current flow for each case scenario in Fig for a better understanding. With Eqs. (5)-(6) the inductors can be designed accordingly and current ratings of semiconductors can be defined. With Eqs. from (7)-(9), capacitors can be chosen in terms of maximum voltage rating.

$$I_{L1,i} = \frac{I_{PV}}{n} \tag{5}$$

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{PV}}{n \cdot d2} \quad PV\ to\ Battery$$

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{DC}}{n \cdot (1-d3)} \quad Battery\ to\ Load \tag{6}$$

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{DC}}{n \cdot d4} \quad DC\ bus\ to\ Battery$$

$$V_{Cpv} = V_{PV} = V_{DC}(1-d1) \tag{7}$$

$$V_{Cbat} = V_{Bat} \tag{8}$$

$$V_{Cdc} = V_{Load} = V_{DCbus} \tag{9}$$

Where n refers to the number of stages and $i=1..n$.

The AC current through inductors should also be analyzed for each operation mode in order to find the worst case scenario.

$$\Delta i_{L1,i} = \frac{V_{PV}}{L1 \cdot f_s} d1 \tag{10}$$

$$\Delta i_{L2,i} = \frac{V_{PV} - V_{Bat}}{L2 \cdot f_s} d2 \quad PV\ to\ Battery$$

$$\Delta i_{L2,i} = \frac{V_{PV}}{L2 \cdot f_s} d3 \qquad Battery\ to\ Load \tag{11}$$

$$\Delta i_{L2,i} = \frac{V_{PV}}{L2 \cdot f_s} d3 \qquad DC\ bus\ to\ Battery$$

Where f_s refers to the switching frequency.

Battery and DC bus capacitors, C_{Bat} and C_{DC}, should be chosen in the case scenarios when Battery port and DC bus port are operating in output mode to assure a stable output voltage. Therefore AC voltage across these capacitors can be defined as follows:

$$\begin{cases} \Delta V_{Cdc} = \dfrac{V_{DC}}{Load \cdot C_{DC} \cdot n \cdot f_s} d1 & PV\ to\ Load \\ \Delta V_{Cdc} = \dfrac{V_{DC}}{Load \cdot C_{DC} \cdot n \cdot f_s} d3 & Battery\ to\ Load \end{cases} \tag{12}$$

$$\Delta V_{Cbat} = \frac{\Delta i_{Bat}}{8 \cdot C_{Bat} \cdot n \cdot f_s} \tag{13}$$

Where $Load$ is the lead resistance in Ohms, Δi_{L1} refers to the AC current through L1, Δi_{L2} refers to the AC current through L2 in the cases "PV to Battery" and "DC bus to Battery", Δi_{Bat} refers to the AC current contained in I_{Bat}.

The AC current of I_{Bat} can be calculated with equations from (14)-(16) [26].

$$\Delta i_{Bat} = \frac{V_{Bat}}{L2}\left(\frac{1-3\cdot d}{d'}\right)\frac{d'}{n \cdot f_s} \ (0 < d < 0.33) \tag{14}$$

$$\Delta i_{Bat} = \frac{V_{Bat}}{L2}\left(\frac{2-3\cdot d}{d'}\right)\frac{d'}{n \cdot f_s} \ (0.34 < d < 0.66) \tag{15}$$

$$\Delta i_{Bat} = \frac{V_{Bat}}{L2}\left(\frac{3-3\cdot d}{d'}\right)\frac{d'}{n \cdot f_s} \ (0.67 < d < 1) \tag{16}$$

IV. EXPERIMENTAL VERIFICATIONS

A two stages interleaved prototype as shown in Fig. 6 was built and steady-state and efficiency experiments are carried out, which are presented in this section. A photograph of the converter implemented is shown in Fig. 7. The main specifications and parameters of the prototype are shown in Tables I and II. Specification of the converter has been determined according to PV systems for household installations.

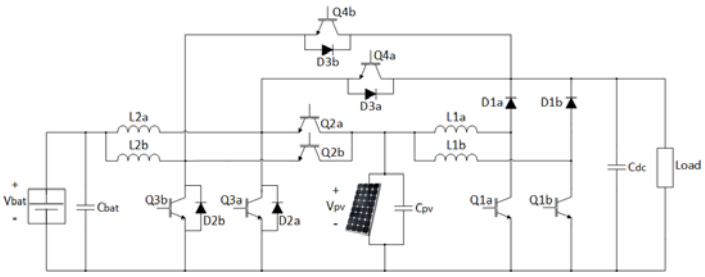


Fig 6. Proposed TPC topology with interleaved stages.

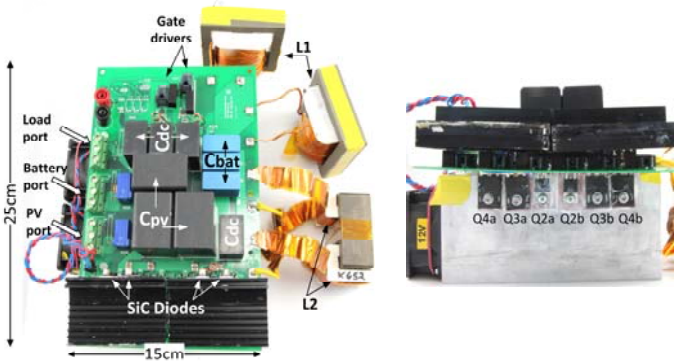


Fig 7. Prototype implemented

Table I. System Specifications.

Parameter	Value
Max. output Power (DC bus)	4000W
Max PV port Power	4000W
Max. Battery Charge/ Discharge Power	2400W
DC Bus Voltage	600V
PV Voltage range	200 – 500V
Battery Nominal Voltage	150V

A. *Seady-State Response of Prototype*

The steady-state waveforms of the prototype developed operating in the different operation modes are shown in Figs. 8-12. Fig. 8 shows the PV and DC bus port current and voltage waveforms when operating under PV to DC Bus operation at 2kW. The voltage ripple at the DC bus port is 1.4V (below than 0.5% ripple) and PV current ripple is reduced to 350mA due to interleaving the power stages. Fig. 9 shows PV port and battery port voltage and current waveforms under PV to Battery operation at 1kW, where the AC current at the Battery port is 100mA and the voltage ripple below 2V (below than 1.5% ripple). Fig. 10 shows battery port and DC bus port current and voltage waveforms in Battery to DC Bus operation at 1.6kW. In that case DC bus ripple is also kept below 0.5% ripple with 2.5VAC voltage. Fig. 11 shows DC bus port and battery port waveforms under DC Bus to Battery operation at 1kW. Fig. 11 shows the waveforms under PV port to Battery and DC Bus ports (SIDO) operation at 2kW delivering approximately 33% of the power to the battery port and 67% to the DC bus port. With the waveforms presented it can verified that the converter is able to operate in steady-state under all operation modes required.

Table II. Converter parameters and components.

Parameter	Value
IGBTs: Q1a, Q1b	IGW25N120H3
IGBTs: Q2a, Q2b, Q4a, Q4b	IGW30N100T
IGBTs: Q3a, Q3b	IGP40N65F5
SiC Diodes: D1a, D1b, D3a, D3b	IDH05S120
SiC Diodes: D2a, D2b	IDH15S120
Inductors: L1a, L1b	1mH
Inductors: L2a, L2b	0.8mH
Magnetic core L1	K8044E026
Magnetic core L2	K6527E060
PV Input Capacitor: Cpv	Film Cap. 15uF*2
Battery Port Capacitor: Cbat	Film Cap. 15uF*3
Load Port Capacitor: Cdc	Film Cap. 5μF*4, 15uF*1
Switching Frequency	20kHz

B. Efficeicny measurements

Conversion efficiency for the converter is determined measuring input and output voltage and current using an Agilent 34401A Precision DMM, with input voltage provided by a programmable power supply (Regatron) and output power dissipated in resistive loads. Power loss due to the fan operation and gate drivers is not considered, this was measured to be 6W in total.

Efficiencies have been measured under all operation modes for different power levels and PV voltage levels. Results are presented in Figs. 13-17. In particular, highest efficiencies are measured in the PV to Battery operation with a maximum efficiency of 98.7% with V_{pv}=500V at 1.2kW and lowest efficiency of 98.1% with V_{pv}=200V at 2.4kW. Lowest efficiencies are measured in Battery to DC bus and DC bus to Battery operation mode, shown in Figs. 15 and 16. Overall, worst case operation in terms of efficiency, is encountered when the converter is operating at high duty cycles, such that the IGBTs experience a high current stress.

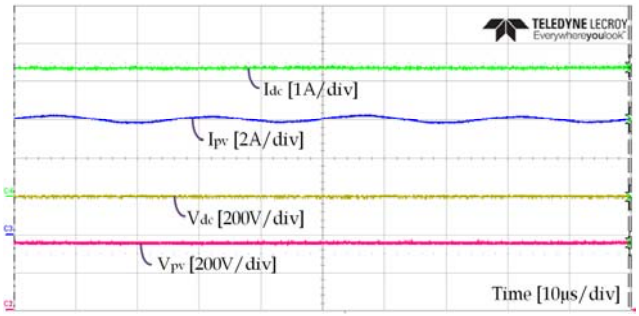


Fig 8. Steady-state waveforms in PV to DC bus operating mode.

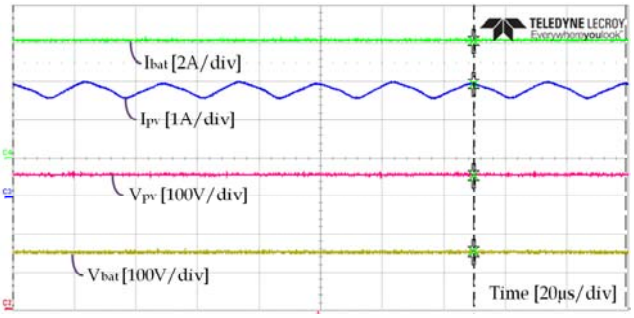


Fig 9. Steady-state waveforms in PV to Battery operating mode.

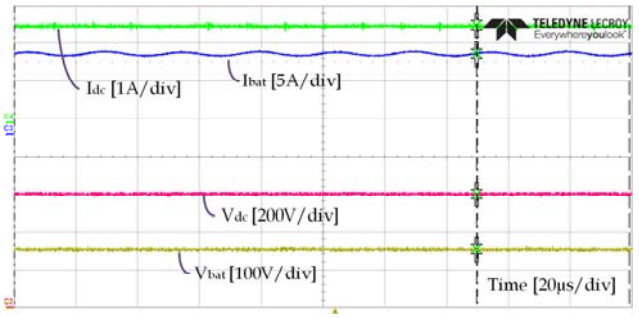


Fig 10. Steady-state waveforms in Battery to DC Bus operating mode.

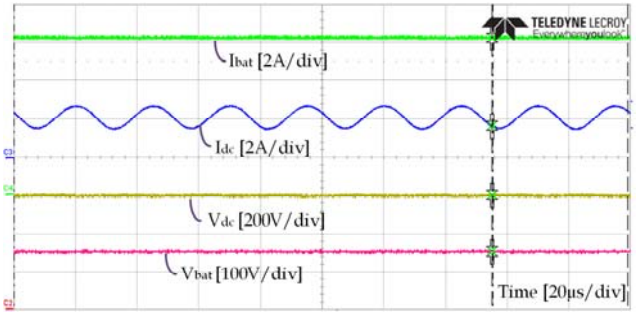
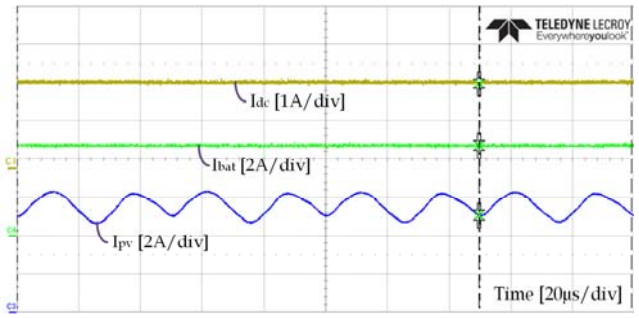
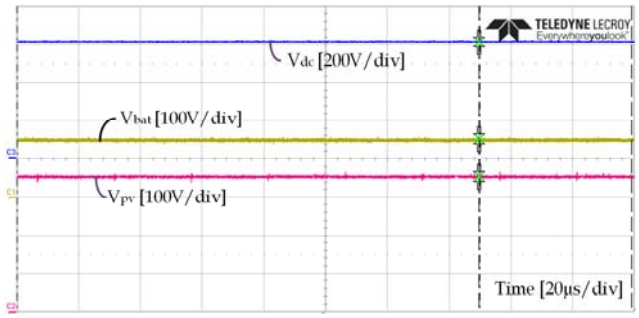


Fig 11. Steady-state waveforms in DC Bus to Battery operating mode**.**



(a)



(b)

Fig 12. Steady-state waveforms under PV to Battery and DC Bus operating mode; voltage (a) and current (b).

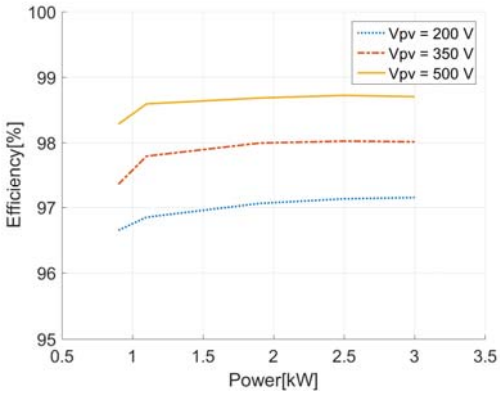


Fig 13. Efficiency results in PV to DC Bus operation.

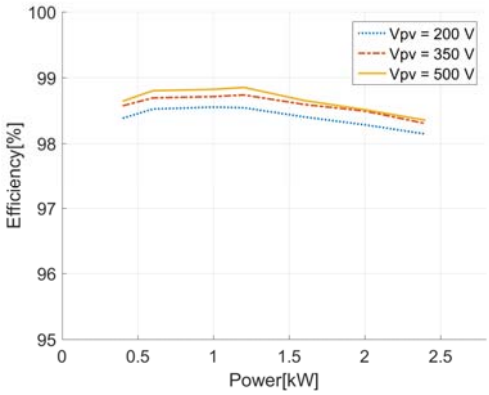


Fig 14. Efficiency results in PV to Battery operation.

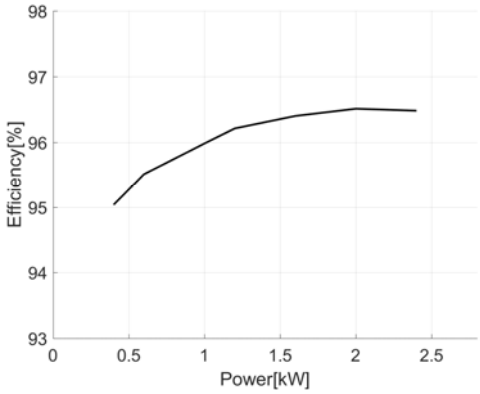


Fig 15. Efficiency results in Battery to DC Bus operation.

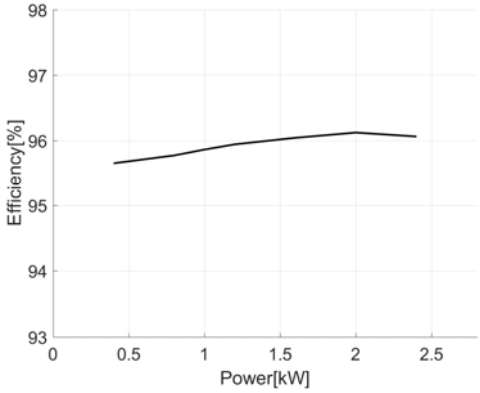


Fig 16. Efficiency results in DC Bus to Battery operation.

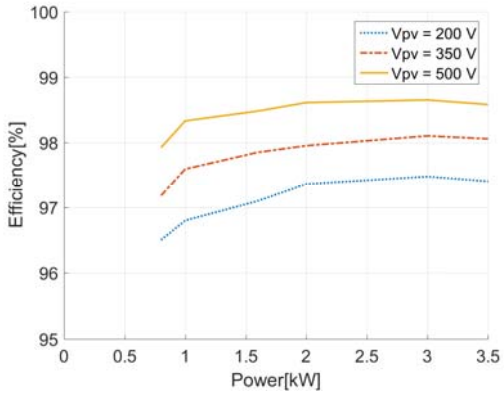


Fig 17. Efficiency results in PV to DC Bus and Battery operation.

V. CONCLUSION

In this paper, a three port dc-dc converter for PV systems with battery storage was presented. The converter was designed for household applications suitable for grid-tied systems, with a maximum power capability of 4kW and a maximum battery charge/discharge power of 2.4kW. This paper presented the topology operation modes and the design procedure. Experimental results show that this topology can operate under high efficiencies under a wide operating range and operation modes. The TPC converter presented is based on the well-known conventional buck and boost converter topologies, thereby easing the design and modelling. Furthermore, converter modularity to increase power rating is achieved by means of interleaving without adding high complexity to the design, as shown with the experimental prototype. Therefore, the proposed converter is suitable for high efficiency PV systems with battery storage where no galvanic isolation is required.

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