InP DHBT Optimization for mm-Wave Power Applications

Midili, Virginio

Publication date:
2018

Document Version
Publisher's PDF, also known as Version of record

InP DHBT Optimization for mm-Wave Power Applications

Virginio Midili

Kongens Lyngby 2017

Technical University of Denmark
Department of Electrical Engineering
Ørsteds Plads, building 348,
2800 Kongens Lyngby, Denmark
Phone +45 45 25 38 00
elektro@elektro.dtu.dk
www.elektro.dtu.dk

Abstract

This work presents the optimization of an InP Double Heterojunction Transistor (DHBT) technology for Power Amplifier (PA) applications in the millimeter-wave frequency range. Starting from an existing InP DHBT technology for high-speed mixed-signal applications, the epitaxial structure of a single-finger DHBT has been designed to fulfill the requirements set for the design of the power cell in terms of maximum cutoff frequency f_{MAX} and breakdown voltage BV_{CEO} . A 2D TCAD modeling approach is proposed to investigate device high-frequency performances for different collector structures. The static and high-frequency performances of devices with different geometrical layout dimensions have been investigated to select the unit finger device with 0.7×10 μm^2 emitter area having f_{MAX} = 400 GHz and $BV_{CEO} > 7$ V for the unit power cell. Single-finger devices are combined in multi-finger structures to increase total output power. The electrical performances of multi-finger devices are investigated with respect to number of fingers and geometrical dimensions. The thermal characterization of multi-finger devices is performed to understand the impact of self and mutual-heating. An approach based on 3D thermal simulations of multi-finger devices is proposed to study heating effects and to extract thermal parameters for the device large-signal model. A 4-finger device with 0.7x10 μm^2 unit finger emitter area is finally selected for the PA power cell. The 4-finger device has f_{MAX} =370 GHz and can deliver P_{OUT} = 16 dBm to an optimal load under class-A operation. As a further improvement to reduce thermal effects in multi-finger devices, the ballasting resistor approach is investigated. The performances of DHBTs with different ballasting resistor networks are compared in terms of static and high-frequency performances. A ballasting solution is finally proposed as a trade-off between the improvement in device Safe Operating Area (SOA) and the degradation of high-frequency performances.

Resumé

Dette arbejde præsenterer optimeringen af en InP Double Heterojunction Transistor (DHBT) teknologi til anvendelse indenfor effektforstærkere i millimeterbølgefrekvensområdet. En eksisterende epitaksial struktur for en enkelt-finger InP DHBT er til at begynde med blevet designet om med henblik påat møde krav opsat til en enkelt effektcelle i term af maksimum afskæringsfrekvens, fmax, og nedbrudsspænding, BV_{CEO}. En 2D TCAD modelleringsmetode er formuleret for at undersøge transistorens højfrekvensegenskaber som funktion af forskellige kollektorstrukturer. Statiske og højfrekvensegenskaber for transistorer med forskellige geometriske layout dimensioner er blevet undersøgt for at udvælge en transistor med f_{MAX} = 400 GHz og $BV_{CEO} > 7$ V til brug i den enkelte effektcelle.
Enkelt-finger transistorer er blevet kombineret til flerfingre transistorer for at øge udgangseffekten. De elektriske egenskaber af flerfingre transistorer er undersøgt med hensyn til antal finger og geometriske dimensioner. Termisk karakterisering af flerfingre transistorer er udført for at forståeffekten af selv- og gensidig opvarmning. En metode baseret på3D termiske simulationer af flerfingre transistorer foreslås her til studium af opvarmningseffekter og for at ekstrahere termiske parameters til brug i storsignal modellering af transistoren. En 4-finger transistor med 0.7×10 μm^2 emitter areal per finger er endeligt blevet udvalgt til brug som enhedscellen i en effektforstærker. 4-finger transistoren har f_{MAX} = 370 GHz og kan levere P_{OUT} =16 dBm til en optimal belastning under klasse-A operation. Som en yderligere forbedring til at reducere termiske effekter i flerfingre transistorer er en metode med ballast modstande undersøgt. DHBT'er med forskellige ballast modstande er sammenlignet med hensyn til deres statiske- og højfrekvensegenskaber. Endeligt er en ballast løsning forslået som et trade-off mellem forbedringer i "Safe Operation Area (SOA)" og forringelse i højfrekvensegenskaberne.

Preface

The PhD study presented in this thesis was carried out in collaboration between III-V Lab and the Electromagnetic Systems (EMS) group at the department of Electrical Engineering at the Technical University of Denmark (DTU) between September 2014 and December 2017. This work is part of the EU project "InP DHBT Optimization for mm-Wave Power Applications" (IN-POWER) within FP7. Financial support was provided by the European Union through a Marie-Curie ITN EID fellowship.
The project supervisor is Associate Professor Tom Keinicke Johansen from DTU while Dr. Virginie Nodjiadjim acted as industrial supervisor.

Kongens Lyngby, Denmark, December 2017

Virginio Midili

Acknowledgements

I feel deeply grateful towards a number of people for their support during my PhD studies both at DTU and at III-V Lab.
First and foremost, I want to thank my supervisors Prof. Tom K. Johansen and Dr. Virginie Nodjiadjim for their guidance, their supervision and their encouragement during these three years. In addition to scientific and technical supervisions, I feel blessed to have had them as a constant example of rigour and passion for research work.
I also want to thank all the people involved in the IN-POWER project: Muriel Riet for the invaluable work and knowledge on DHBT fabrication at III-V Lab, Jean-Yves Dupuy and Agnieszka Konczykowska for providing top-notch insights on research methods and circuit design issues. Many thanks also to Filipe Jorge and Fabrice Blache for their precious help and advice about characterization issues. Last but not least, I want to thank the other fellow student of the IN-POWER project, Michele Squartecchia who shared with me the ups and downs of PhD life in these three years.
Besides the people I had the opportunity to work closely with, I would like to thank all the researchers and staff members of DTU and III-V Lab, especially the PhD students of both institutions that I had the opportunity to meet. The informal discussions, the sharing of ideas and the kind support contributed to my journey and enriched me beyond the scope of my PhD project.
Finally, I want to thank my family and my friends for supporting me through all these three years as they have always done.

Contents

Glossary

Acronyms

AC	Alternating current
BGN	Bandgap Narrowing
CB	Common base
CE	Common emitter
DC	Direct current
DD	Drift-Diffusion
DHBT	Double Heterojunction Bipolar Transistor
EB	Energy balance
EHF	Extremely High Frequency
FEM	Finite Element Model
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HD	Hydrodynamic model
MAG	Maximum available gain
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier

PAE Power Added Efficiency

SDD Symbolically Defined Device

SEM Scanning Electron Microscope

SOA Safe Operating Area

SOLT Short-Open-Load-Through calibration

SRH Shockley-Read-Hall

TCAD Technology Computer-Aided Design

UCSD University California San Diego large-signal model

VNA Vector Network Analyzer

Symbols

α Current transfer ratio I_C /I_E

β Current transfer ratio I_C /I_B

ϵ Dielectric permittivity

μ Carrier mobility

ϕ Thermal-electric feedback coefficient

τ_b Base-transit time

τ_c Collector transit time

A_E Emitter contact area

D_n Electrons diffusion coefficient

E_C Conduction band energy

E_F Fermi level

E_G Energy bandgap

E_T Trap energy level

E_V Valence band energy

g_m Transconductance

h_{21} Short-circuited current gain

J_C Collector current density

N_d	Doping concentration
R_{TH}	Thermal resistance
X_d	Depletion region width
BV_{CBO}	Breakdown voltage in common-base configuration
BV_{CEO}	Common emitter breakdown voltage
f_{MAX}	Maximum oscillating frequency
f_T	Cutoff frequency
I_B	Base current
I_C	Collector current
I_E	Emitter current
V_{BE}	Base-emitter voltage
V_{CB}	Collector-base voltage
V_{CE}	Collector-emitter voltage
v_{sat}	Carrier saturation velocity
k	Boltzmann constant
U	Mason's unilateral gain

Chapter 1

Applications and context

1.1 Applications of mm-wave circuits

The range of radio frequencies between 30 and 300 GHz is designated as Extremely High Frequency (EHF) by the International Telecommunication Union (ITU). Radio waves in this interval have free-space wavelength between 10 and 1 mm thus frequencies in this range are commonly referred as millimeter wave (mm-wave) frequencies. The attenuation for propagating waves in this interval is severe due to absorption by gases in the atmosphere. They have therefore a short range and they are mostly suitable for terrestrial communication.
The mm-wave spectrum was traditionally reserved to military and scientific applications. As the demand for bandwidth continues to grow due to the increased utilization and number of connected devices, this range is slowly being allocated for consumer and commercial applications.
There are several advantages and drawbacks related to the utilization of the mm-wave spectrum. The main advantages in moving up to higher frequencies are mainly related to bandwidth and the size of antenna components.
The large available bandwidth translates directly to higher data-rates that can support high-quality video streaming and other bandwidth intensive applications or simply to increase the capacity of current network connections. For a fixed gain, the size of an antenna working in the mm-wave range is reduced leading to smaller and more compact equipment. In addition, the narrower beam of

a mm-wave antenna allows to achieve greater resolutions. As the propagation range of mm-waves is rather small, communication systems with increased security and immunity to jamming can be designed.
The obstacles in moving applications to the mm-wave spectrum are related to the short range and the cost of the underlying technology. Due to the high atmospheric attenuation, mm-waves have very short transmission range as mentioned above. This range is reduced even more with fog, rain and moisture [1] Increasing this range requires the design of high power transmitters and high-gain antennas along with high-sensitivity receivers. In this way, the trasmission range can be normally increased to about 1 kilometer. However, mm-wave applications require line-of-sight operations as physical objects are blocking obstacles for waves in this range. Besides physical limitations, technological challenges exist to manufacture semiconductor circuits able to generate, amplify, transmit and receive mm-wave signals.
In the past decades, the research focused on designing and improving transistors that could operate at mm-wave frequencies. Several material systems and device designs have been investigated that are suitable for mm-wave applications with different characteristics. Manufacturers are currently able to provide technological platforms that allow the fabrication of Monolithic Microwave Integrated Circuits (MMICs) based on the different technologies at affordable costs, thanks to the increasing demand.
A wide range of applications exists already exploiting the advantages offered by circuits operating at mm-wave frequencies. Besides traditional scientific and military applications there is an increasingly growing number of commercial applications. Among these, single-chip short-range radars, healthcare and imaging applications and telecommunications applications are more widespread and will be described in the following sections.

Scientific and military

The main scientific application of mm-wave circuits is in the astronomy and space domain and for example in the U.S. this band is commonly allocated for radio astronomy and remote sensing applications. Ground-based radio astronomy is limited to high altitude sites due to atmospheric absorption issues. Satellite-based remote sensing near 60 GHz can determine temperature in the upper atmosphere by measuring radiation emitted from oxygen molecules that is a function of temperature and pressure. For example, passive frequency allocation at 57-59.3 GHz is used for atmospheric monitoring in meteorological and climate sensing applications, and is important for these purposes due to the properties of oxygen absorption and emission in Earth's atmosphere. Currently operational U.S. satellite sensors and special sensor microwave/imager make use

of this frequency range [2].

Mm-wave radars

Mm-wave radars have fine resolution that makes them ideal for detecting small movements and objects and allows position determination with millimeter precision. In particular, radars in the 76 to 81 GHz frequency range are widely used in vehicle control and safety devices [3] [4]. The specific applications include sensors for automatic braking, lane intrusion, applications blind spot detection, forward collision detection, cruise control, and more. The radar chipset has a detection range of between 20 and 200 meters and customizable to perform various automotive applications. In-building radars are also used in military and public safety domain. Short range mm-wave radar is used also for ground penetration applications such as mine detection. Radar-like systems at mm-wave are commonly employed also in manufacturing process control. For example, flow measurement of fluids or slurries carrying solid materials or detection systems for undesired materials. Since mm-wave radar are non-optical systems they are employed with optically opaque materials as in the case of pipes and plenums and in the presence of dust and smoke. Among these applications there is level sensing in large tanks such as those found at petroleum refineries and distribution sites.

Imaging

Imaging applications are an extension of radar that are interesting at mm-wave because of high-resolution. Mm-wave imaging systems employing interferometry and holographic techniques can obtain results comparable to X-ray type investigation without the use of ionizing radiation [5] [6]. Holographic techniques can use the reconstructed wavefront to view and analyze the image from multiple observation points simultaneously. Resolution is greatly enhanced when used in combination with multi-frequency or ultra-wide band (UWB) techniques. Existing applications range from scanning baggage for security to ground-penetrating imaging at archaelogical sites. Even if radar scanning is commonly used in the mm-wave spectrum, there is a great interest in passive scanning techniques. Two types of mm-wave imaging are commonly employed using general illumination with a mm-wave source and the utilization of the thermal radiation naturally emitted by the scanned item. In both cases similar radiometric detectors are employed as mm-wave camera. These mm-wave imaging systems can be used to detect concealed objects including ceramic materials and the presence of persons through non-metallic walls. Also, the absorption properties of mm-wave through

water and moisture can be exploited for the imaging of biological structures as shown in Fig. 1.1. Other applications currently being developed include cloud

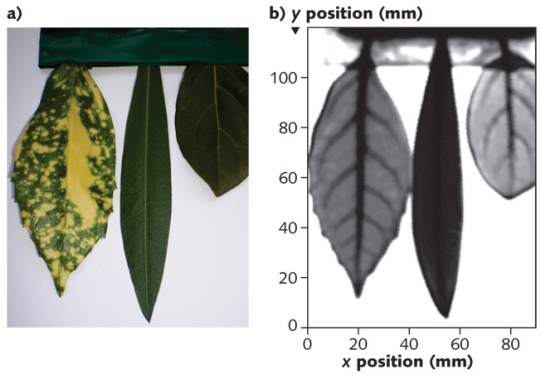

Figure 1.1: Detected image at 300 GHz and visible counterpart [6].

imaging for weather research, high-resolution artificial vision for autonomous agents and aerial terrain mapping where high penetration through vegetation is needed.

High-speed data links

Mixed-signal

Probably the most significant application of mm-wave transistors in terms of commercial demand is for front-end high-speed circuits in the telecommunication sector. Although short range wireless systems are a straightforward use case, high-speed transistors are employed also in front-end sub-systems for wired communication on fiber. The high frequencies capabilities of the devices are well suited to achieve gigabit data rates using increasingly complex wide bandwidth modulation schemes. Circuits based on mm-wave devices can be found in transceiver sub-systems for ADC and DAC components at high-data rates and as drivers for the modulation of optoelectronic components [7].

Wireless link

Future high-speed wireless communication is likely to take place at E-band and higher millimeter-wave frequencies. For communication systems at mm-waves,

PA with large output powers are needed to extend the transmission distance of the wireless communication link. Given the ever growing demand for wide bandwidths and the continuous downscaling of devices, it becomes more and more difficult to obtain decent level of power at the transmitter end. InP DHBT technology has emerged as a very promising choice for high-frequency applications and have demonstrated capability to operate in the sub-terahertz domain [8],[9],[10] (in [8] a DHBT with 130 nm wide emitter is presented with f_{MAX} > 1 THz and BV_{CEO} = 3.5 V, in [9] GaAsSb is used as the base material for a DHBT that presents f_{MAX} > 700 GHz and in [10] f_{MAX} is as high as 470 GHz while still showing BV_{CEO} =12 V). Although PA designs in the same frequency range have been proposed based on competing technologies such as GaN HEMTs and SiGe BiCMOS, InP DHBTs exhibit excellent power handling capability as a good compromise between high output power and frequency of operation. PA designs based on InP HEMTs have already been realized obtaining 427 mW of output power with PAE of 19% at 94 GHz [11]. Advancements in technology process allowed GaN based MMICs to be demonstrated operating at E-Band with 1.3 W of output power and PAE of 27% [12] and in the W-band with 3W/mm of output power and PAE of 27.8% [13]. Thanks to more mature technology process and corresponding reliability InP based HBTs remain however interesting for commercial products targeting E-band and higher frequencies. PA designs based on SiGe technology showed an output power of 22-dBm and PAE of 3.6% at 120 GHz [14]. Although the high operating frequency, SiGe technology provides lower output power density levels compared to InP based technology. For all of the mentioned reasons InP DHBT technology is a good candidate to build PAs for E-band and higher frequencies and several designs have already been demonstrated up to 0.67 THz [15][16].

1.2 State-of-the-art for mm-wave transistors

As it was mentioned above, several competing technologies exist that could fulfill the requirements for high-frequency and high-power applications at mm-waves. Table 1.1 presents a summary of the state-of-the-art transistor technologies for sub-THz applications. The summary includes vertical and planar single-finger devices based on InP, SiGe and GaN and presents relevant performance metrics for PA as cutoff frequency f_T , f_{MAX} and BV_{CEO}. Although the device technology presented in this work has lower frequency performances than the most recent published results of deeply scaled InP DHBTs, it is important to evaluate these same performances with comparable emitter dimensions in order to assess the advantages and drawbacks of different epitaxial design approaches. The scaling of emitter junction width in InP/InGaAs DHBT is a needed step to

Table 1.1: Summary of state-of-the-art transistors for sub-THz applications

[Reference] Year	Technology	f_T (GHz)	f_{MAX} (GHz)	BV_{CEO} (V)
[8] 2011	$0.13 \times 2\ \mu m^2$ InP DHBT	520	1100	3.5
[17] 2013	20 nm GaN HEMT	454	444	10
[18] 2016	130 nm SiGe HBT	505	720	1.6
This work	0.7x5 μm^2 InP DHBT	267	450	7.5

Table 1.2: Published InP-based DHBTs performances by emitter width

[Reference] Year	Emitter dimensions (μm $\times$ μm)	f_T (GHz)	f_{MAX} (GHz)	BV_{CEO} (V)
[20] 2013	0.8 x 6	400	350	-
This work	0.7 x 5	267	450	7.5
[21] 2001	0.5 x 8	171	425	8
[22] 2015	0.5 x 6	290	320	≈ 4
[23] 2016	0.2 x 4.4	495	882	4.1
[24] 2015	0.18 x 2.7	404	901	4.3

reduce charging times and access resistances and capacitances and thus increase device f_{MAX} [19]. The scaling rule for InP based DHBTs derived in [19] predicts a 2:1 bandwidth increase for a 4:1 decrease in emitter width, assuming that also the vertical dimensions are consequently scaled. Based on this assumption, the InP DHBT design presented in this work show a high potential when compared to other published results as presented in Table 1.2. It is evident, however, that further performance improvement of the devices presented in this work will need an effort toward device scaling to smaller emitter widths.

1.3 Objectives of this work

The work done in this thesis is part of the EU Marie Curie ITN EID [1] project "InP DHBT Optimization for Mm-wave Power Applications" (IN-POWER). Starting from the previous generation of InP DHBT fabricated at III-V Lab for high-speed mixed-signal applications [25], the goal of this work is to adapt the existing transistor technology to the design of power amplifiers targeting E-band and higher frequencies. For power amplification (PA) applications, the

[1] Initial Training Network European Industrial Doctorate

maximum oscillation frequency f_{MAX} and breakdown voltage BV_{CEO} of the DHBT are considered two critical figures of merit (FOM) to improve in order to maximize circuit performance. In particular, the objective of this project is to provide InP DHBTs with f_{MAX} approaching 500 GHz and BV_{CEO} above 7 V maximizing at the same time the power cell output power by using multiple devices combined in parallel.

This thesis is structured as follows:
Chapter 2: this chapter is organized in three parts and focuses on the selection of the single-finger device for the PA power cell. In the first section the single-finger InP DHBT technology developed at III-V Lab is presented along with the static and high-frequency performances with respect to different layout dimensions. In the second section a 2D TCAD physical simulation approach is presented including a discussion about different models suitable for InP DHBTs. Finally, a discussion about device collector structure design is presented.
Chapter 3: this chapter is focused on the selection of a multi-finger device to increase the output power of the PA power cell. Firstly, the static and high-frequency characterization of InP multi-finger DHBTs is reported. Then the thermal characterization of the devices from electrical measurements is presented. In addition, a 3D TCAD thermal simulation approach is described and validate against measurements. Finally, the results from thermal characterization and simulations are used to improve the large-signal model of multi-finger DHBTs for SOA simulations.
Chapter 4: in this chapter, different approaches to improve device SOA are introduced focusing on the concept of ballasting resistors. Different ballasting networks are compared in terms of static and high-frequency performances. A modeling approach for ballasted devices is discussed based on EM simulation of passive structures and on the physical modeling with lumped circuit elements. Finally the performances of multi-finger DHBTs in common-base configuration are presented.
Chapter 5: Chapter 5 presents a small selection of PA mm-wave circuits designed and measured by other researchers involved in the IN-POWER project. The objective of this chapter is to briefly showcase the capability of the InP DHBTs selected in this thesis when used within a PA circuit.

Chapter 2

Single finger InP DHBT optimization

2.1 Baseline device structure

Epitaxial structure

The majority of HBTs including the devices discussed in this work, are fabricated according to a triple-mesa structure. The operation of the device is mainly determined by the properties of the different layers in the vertical structure grown in the epitaxy process. For the DHBTs fabricated at III-V Lab, materials are grown by Gas Source Molecular Beam Epitaxy on a 3" semi-insulating InP substrate. The structure consists of a 40 nm InP emitter, a ≈30 nm highly C-doped and compositionally graded InGaAs base and a composite collector. The collector includes a non-intentionally doped (nid) InGaAs spacer, a highly doped InP region and a low doped InP layer. A low-doped InP layer is used to fully deplete the collector at low bias. A simplified structure description of the device is shown in Fig. 2.1 while Fig. 2.2 shows the equilibrium band diagram of a InP/InGaAs DHBT device. The emitter contact structure includes $In_{0.85}Ga_{0.15}As$ highly n-doped cap layer to reduce emitter resistance and InP highly n-doped layer. The base layer is very thin to minimize the base transit

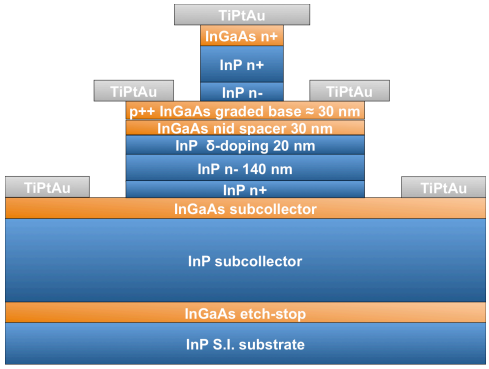

Figure 2.1: Schematic cross-section view and simplified layer structure of a single finger InP DHBT (with 190 nm total collector thickness).

time. It is also highly carbon doped ($\approx$8x10^{19} cm^{-3}) in order to decrease the base sheet resistance to a value of roughly 800-900 $\Omega/\square$. The doping level is chosen high enough to obtain a low total base resistance and thus increase f_{MAX} while still allowing for a static gain β higher than 20.
The epitaxy optimization process includes the reduction of device self-heating effects occurring at high dissipated power levels. As the thermal conductivity of InGaAs is considerably lower than InP, the general approach consists in thinning of InGaAs layers [26]. In particular, the InGaAs subcollector layer is thinned to roughly 5 nm. Besides improving device thermal behavior, the subcollector layer is still thick enough to provide its function as collector contact layer and to behave as an etch-stop layer in the fabrication process.
The results presented in this thesis are based on devices from wafers with different collector thicknesses, as listed in Tab. 2.1. As it will be explained in more detail in Sec. 2.4.3, in order to obtain the desired performances devices with different collector structures were considered including a low doped n$^-$ layer of different thickness. It is worth mentioning, however, that due to a certain degree of variance concerning the epitaxial and technological fabrication process, even devices having the same epitaxial structure but measured on different wafers may exhibit slightly different performances. For all the measurements results presented throughout the thesis it will be specified the corresponding wafer on which the measurements were performed.

Fabrication process

The DHBTs with an hexagonal shape [25] are fabricated using a wet-etch triple mesa technology including a self-aligned emitter-base metallization technique.

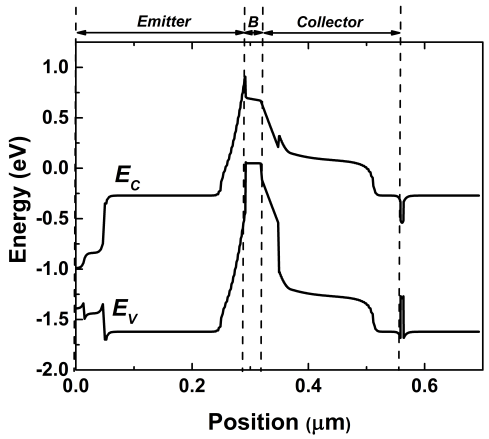

Figure 2.2: Equilibrium energy band diagram of an InP/InGaAs DHBT.

Table 2.1: List of wafers and corresponding collector dimensions for fabricated devices in this work.

Wafer n°	Total collector thickness (nm)
55657	130
55656	190
55660	190
54608	250

In this process the functional parts of the DHBT corresponding to emitter, base and collector result in three separate mesas one on top of the other after etching the epitaxial structure described in the previous section. Figure 2.4 presents the sideview of a single-finger transistor indicating the location of emitter, base and collector contact.

The transistor is typically designed to be emitter-up because this configuration leads to easier fabrication process for high-speed applications [27] however collector up designs have also been demonstrated by other labs [28].
Figure 2.3 shows the simplified layout of a triple-mesa HBT including relevant geometrical parameters as emitter width W_E and length L_E. The width of the emitter contact is 0.7 μm (effective emitter width is approximately 0.6 μm). The base contact extends 0.3 μm on each side of the emitter and includes a plug for the connection. Both contacts are defined by electron beam lithography because of the high alignment precision required for this technology. Other process steps are realized using stepper lithography. The collector contact also includes a plug for connection. TiPtAu is used for all contacts. After encapsulation with

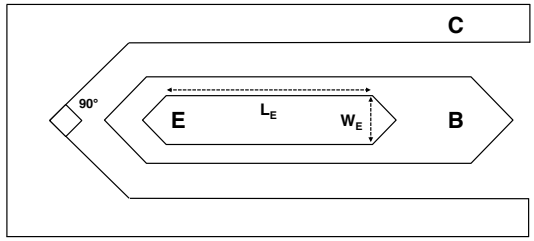

Figure 2.3: Top view simplified schema of a triple-mesa HBT device with hexagonal shape.

SiN and planarization with polyimide, emitter, base and collector contacts are opened by etching to interconnect the devices.

In order to select the most suitable device for the PA power-cell design, single-

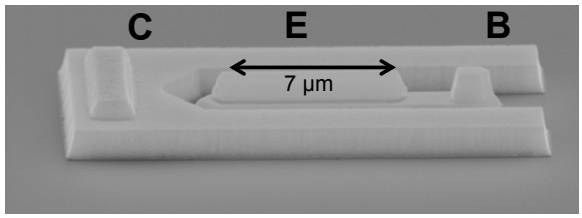

Figure 2.4: Sideview SEM photo of a single-finger DHBT including contact metallization and showing Emitter (E), Base (B) and Collector (C) contacts.

finger DHBTs with different emitter layout geometries were investigated in this work. In particular, measured devices included all the combinations of emitter width W_E equal to 0.5, 0.7, 1 and 1.5 μm and emitter length L_E equal to 5, 7, 10 μm .

2.2 Characterization of single-finger DHBT

In order to assess the functionality and the performances of the different single-finger DHBTs, static and frequency measurements were carried out for each emitter geometry on wafer 55656 available in the beginning of the project. The static measurements include especially Gummel plot and I_C -V_{CE} curves. The investigation of the frequency performances relies on small-signal S-parameters measurements taken at different static bias points.

2.2.1 Static results

The first static characterization method is Gummel plot measurements. During measurements, the device is biased with an increasing emitter-base voltage V_{BE} while keeping the base-collector voltage $V_{BC} = 0$ V. The base current I_B and the collector current I_C are plotted on a logarithmic scale as a function of V_{BE}. The forward static gain β in common-emitter configuration is computed by the ratio of I_C over I_B . In the ideal case the I_B and I_C curves would be parallel over the whole range of V_{BE} and consequently β would stay constant. In real devices, for low current levels base recombination currents become predominant while series resistance, thermal effects and the occurrence of Kirk effect lead to collector current saturation and base current increase. The effect of all of these non-idealities can be seen from a plot of the gain β that increases towards a peak value followed by a continuous drop. Figure 2.5 presents the Gummel plot of a 0.7x10 μm^2 single finger device and the corresponding static current gain (β) versus collector current (I_C) with a peak value around 40.
For the DHBT optimization for high-frequency application a very high static gain is not of paramount importance but a value above 20 is considered the minimum for practical functionality. In addition to the above mentioned non-ideality factors, the geometry of the device affects the magnitude of the parasitic recombination currents and thus the static performance. Lateral dimensions such as emitter width W_E and length L_E directly influence the parasitic surface recombination currents. In order to avoid the predominance of these effects, it is therefore important to keep a high ratio between the device active area and its periphery. For the InP DHBTs discussed in this work, the effect of device dimension on the static gain was investigated for the available geometries. Figures 2.6 shows a plot of the static gain β vs. base-emitter voltage V_{BE} for representative devices with different emitter dimensions. It is immediately clear that for each of the three cases the values of the gain peak values are very close to each other and do not show a clear trend with respect to a geometrical parameter. The average value for the ensemble of the measured devices is 38 with a standard deviation of 1.4. It was concluded that the static gain can be considered mainly independent on device geometrical dimensions. In order to obtain device I-V curves, the collector current I_C is measured as a function of collector-emitter voltage V_{CE} while biasing the device at different I_B (in common-emitter configuration). The final result is a set of curves corresponding to the function I_C =f(V_{CE} ,I_B) where I_B is a stepped parameter.
Although the I-V curves measurements are not used as a direct tool to select the optimal geometry for a single-finger in the power cell, they are employed as a diagnostic tool and to assess the static performance of the devices. Important parameters that can be inferred from the I-V curves are the offset voltage V_{OS} and the knee voltage V_{KNEE}. The former corresponds to the value of V_{CE} for which the collector current is equal to zero when a I_B is forced while the latter is

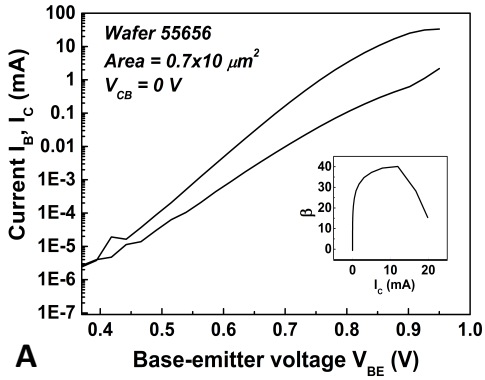

Figure 2.5: Gummel plot and static current gain β of a single-finger DHBT with emitter area 0.7x10 $\mu\mathrm{m}^2$.

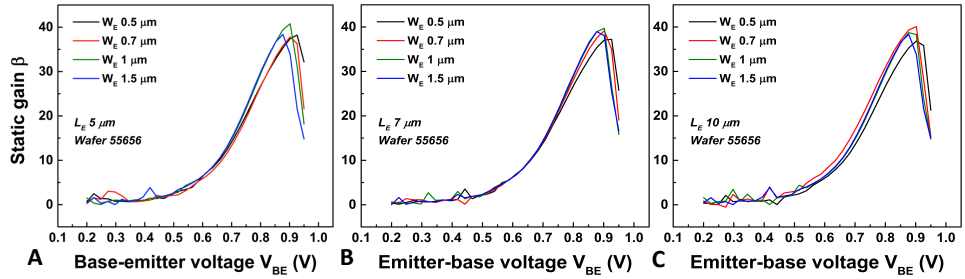

Figure 2.6: A) Static gain β vs base-emitter voltage $\mathrm{V_{BE}}$ for devices with emitter length $\mathrm{L_E}$ equal to A) 5, B) 7 and C) 10 $\mu\mathrm{m}$ and different emitter widths.

the $\mathrm{V_{CE}}$ value for which the collector current has reached almost its maximum value in the linear region. Figure 2.7 shows the output characteristic curves from the measurements of collector current versus collector-emitter voltage up to 2 V for different values of base current $\mathrm{I_B}$ from 0 to 1.1 mA with a 0.22 mA step for a single-finger DHBT with 0.7x10 $\mu\mathrm{m}^2$ emitter area.

2.2.2 High-frequency results

The high-frequency performances of the devices were determined from small-signal scattering parameters (or S-parameters) measurements. The measurements are performed over the frequency range from 250 MHz to 110 GHz using an Anritsu VectorStar Vector Network Analyzer (VNA). The VNA is calibrated using an off-wafer calibration kit. During the measurements the transistors are

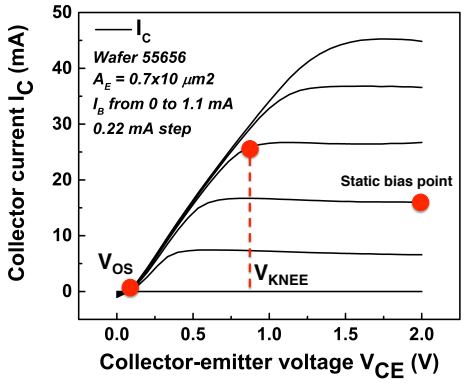

Figure 2.7: I_C (V_{CE}) curves of a single-finger 0.7x10 μm^2 DHBT. The base current I_B is varied from 0 to 1.1 mA with a 0.22 mA step.

biased with different collector current values and fixed collector-emitter V_{CE} voltage. On-wafer dummy structures are included for each transistor geometry in order to de-embed the additional parasitic elements generated by the contact pads from measured data. The de-embedding method is based on a three-step Open-Short procedure as described in [29]. From the measured S-parameters the device small-signal current gain h_{21} can be computed according to:

$$h_{21} = \frac{-S_{21}}{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}} \tag{2.1}$$

Mason's unilateral power gain U can be computed as:

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left(k\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)\right)} \tag{2.2}$$

The two quantities $|h_{21}|$ and U are plotted vs. frequency for each bias point. By definition f_T and f_{MAX} are the frequencies for which $|h_{21}|$ and U become equal to 0 dB. Thus the values of f_T and f_{MAX} are extrapolated by fitting a -20dB/decade line to experimental $|h_{21}|$ and U data in the high-frequency range. Fig. 2.8 illustrates the extrapolation of f_T and f_{MAX} on de-embedded data of a 0.7x10 μm^2 DHBT biased at I_C =15 mA and V_{CE} =2 V. From Fig. 2.8 it can be seen that the fitting of the - 20 dB/decade line in logarithmic scale not extremely accurate for Mason's gain U. As a consequence, a certain degree of uncertainty exists for the extraction of f_{MAX} value.
According to the procedure described above, the high-frequency performance

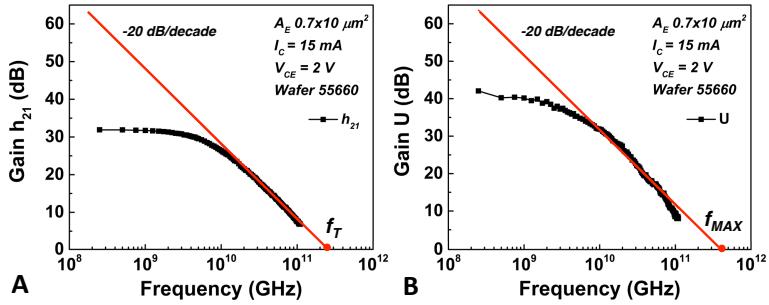

Figure 2.8: Extrapolation of f_T and f_{MAX} from A) $|h_{21}|$ and B) U for a 0.7x10 μm^2 DHBT. The bias point is I_C = 15 mA, V_{CE} = 2 V.

of single-finger DHBTs with different emitter sizes were considered in order to extract their f_T and f_{MAX} operating frequencies. Fig. 2.9 presents values of f_T and f_{MAX} of single finger transistors having emitter length of 5-7-10 μm and emitter width of 0.5-0.7-1-1.5 μm . Reported f_T and f_{MAX} values refer always to the frequency peak value reached by increasing collector current I_C at V_{CE} = 2 V before a drop off due to Kirk effect. In Fig. 2.9-A it can be seen that the cutoff frequency shows at most 10% variation with respect to device geometrical scaling and is only slightly larger for devices with smaller emitter width. Fig. 2.9-B shows that emitter geometrical dimensions have a stronger influence on measured f_{MAX} values. In particular, f_{MAX} approaches 450 GHz for devices with W_E of 0.5-0.7 μm while it is reduced by 30% to 300 GHz for devices with W_E =1.5 μm . From Eq. 2.3 it can be seen that the cutoff frequency depends directly on device lateral dimensions through the RC products related to the emitter layers and junction R_E and C_{je}. Since the resistor and capacitance terms have inverse dependence on device area, f_T in theory should be independent on emitter area. However, due to 2D and border effects the scaling of model parameters may not be exactly proportional to emitter area scaling. In addition, a contribution exist related to cross-products between the emitter resistance and the base-collector capacitance that do not scale proportionally to emitter area. The terms related to base-collector capacitance are distributed between intrinsic and extrinsic capacitance C_{bci} and C_{bcx} with the former related to device active area and (thus proportional to emitter area) and the latter dependent mainly on base mesa dimension thus constant in our case.

From the data reported so far DHBTs with emitter widths of 0.5 or 0.7 μm were selected to be suitable candidates for the unit power cell. As stated in the project objectives, output power is considered an important criteria so the final choice has to take into account the maximization of the transistor active area. In this sense, single-finger DHBT having W_E =0.7 μm offered a good trade-off between frequency performance and device active area.

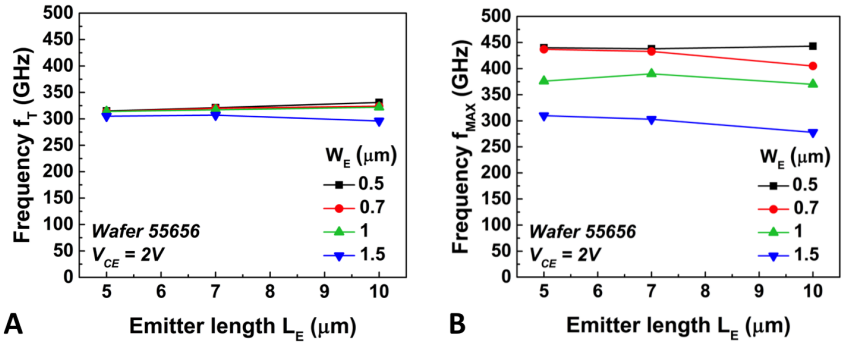

Figure 2.9: Peak cutoff frequency f_T (A) and f_{MAX} (B) as a function of L_E for devices with different emitter width W_E from 0.5 to 1.5 μm .

In the following of this section, additional measurements results concerning the high-frequency performances of single-finger DHBTs with W_E =0.7 μm will be presented. Moreover the parameters of the small-signal model of a 0.7x10 μm^2 DHBT are introduced.
With respect to the hybrid topology representation of the small-signal model shown in Fig. 2.10 the cutoff frequency f_T is defined as:

$$\frac{1}{2\pi f_T} = \tau_b + \tau_c + r_E(C_{je} + C_{BC}) + (R_E + R_C)C_{BC} \tag{2.3}$$

where the extracted τ_b and τ_c are the base and collector transit time respectively, r_E is the dynamic base-emitter resistance divided by the current gain β, C_{BC} is the total base-collector capacitance, C_{je} is the base-emitter junction capacitance, R_E and R_C are the extrinsic emitter and collector resistance, respectively.
According to the approximate expression:

$$f_{MAX} \approx \sqrt{\frac{f_t}{8\pi(R_{bx}(C_{bcx} + C_{bci}) + R_{bi}C_{bci})}} \tag{2.4}$$

f_{max} is optimized by reducing the product of the extrinsic and intrinsic base resistance (R_{bx} and R_{bi}) and base-collector capacitance (C_{bcx} and C_{bci}).

Figure 2.11 presents the extracted f_T and f_{MAX} vs. J_C (V_{CE} = 2 V) for single finger devices with emitter length 5, 7, 10 μm and emitter width 0.7 μm .
The 5 μm length device exhibits highest values with f_T =267 GHz and f_{MAX} =450 GHz at $J_C \approx 3.5$ mA/μm^2 . As a further validation of the trends presented earlier for the previous wafer, increasing the emitter length from 5 to 10 μm , f_T remains constant while f_{MAX} decreases to 410 GHz for a peak current density of $J_C \approx 3$ mA/μm^2. From these results, a device with contact emitter size 0.7x10 μm^2 is then selected because it has the largest active device area while offering

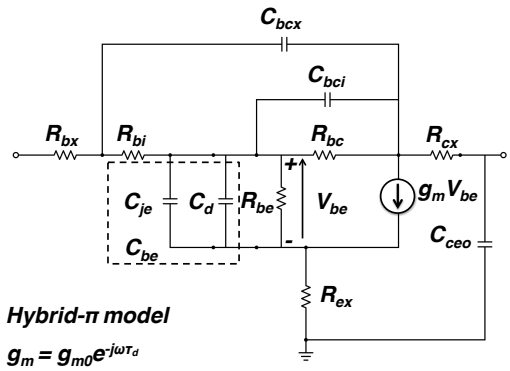

Figure 2.10: Hybrid-π small-signal equivalent model.

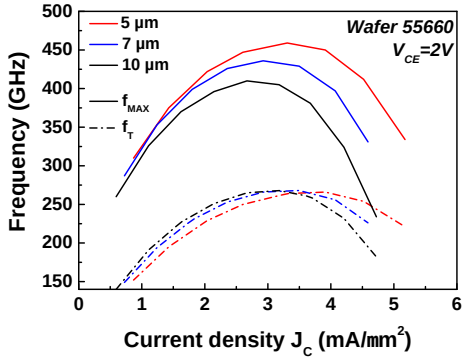

Figure 2.11: f_T and f_{MAX} versus J_C for 0.7 μm emitter width DHBTs with emitter lengths of 5,7 and 10 μm .

frequency performances sufficiently high for the PA power cell. Although the wafer epitaxial structures are nominally the same, the peak f_T values for DHBTs with $W_E = 0.7$ μm reported in Fig. 2.11 are lower than the ones reported in Fig. 2.9 having the same dimensions. In particular, the peak f_T is equal to 320 GHz for 0.7×10 μm DHBTs from wafer 55656 while it is around 270 GHz for the same devices on wafer 55660. Two reasons exist causing this difference related to unwanted variation of the technological and epitaxial process. Firstly, a higher degree of emitter mesa underetching exists for devices from Fig. 2.11 causing a reduction of device active area and thus an increase of the emitter resistance. This leads to a higher R-C product in Eq. 2.3. The second reason is the fact that the lightly n-doped layer in the collector of devices from wafer 55656 is probably thinner, leading to a shorter transit time in the collector.
In order to further investigate the frequency behavior of the devices, the hybrid-

Table 2.2: Small-signal model parameters of single-finger DHBTs with W_E =0.7 μm and L_E = 5,10 μm . The model is extracted at I_C equal to 6.5 mA and 15 mA for L_E equal to 5 μm and 10 μm , respectively and V_{CE} =2V.

Emitter length (μm) $\mathbf{W_E = 0.7\ \mu m}$	$\mathbf{R_{bi}}$ (Ω)	$\mathbf{R_{be}}$ (Ω)	$\mathbf{C_{be}}$ (fF)	$\mathbf{R_{bc}}$ (Ω)	$\mathbf{C_{bci}}$ (fF)	$\mathbf{C_{bcx}}$ (fF)
5	20	190.5	78.3	280.7	1.84	4.5
10	10.9	111	154.4	172.6	5	4.24
	$\mathbf{R_e}$ (Ω)	$\mathbf{R_{bx}}$ (Ω)	$\mathbf{R_{cx}}$ (Ω)	$\mathbf{C_{ceo}}$ (fF)	$\mathbf{g_{m0}}$ (S)	τ_d (ps)
5	4.7	4.28	19.3	6.8	184.6	0.43
10	2.4	5.38	10.9	6.8	323	0.45

π small-signal model components of a devices with $W_E = 0.7$ μm and L_E =5,7,10 μm have been extracted from S-parameters measurements following the procedure described in [30]. The model parameters are extracted at the bias point that corresponds to the peak f_{MAX} value, that is at I_C =15.5 mA for a 0.7x10 μm^2 device and to I_C =15 mA for 0.7x5 μm^2 DHBT. The applied bias voltage is V_{CE} = 2 V in both cases. Table 2.2 summarizes the numerical values extracted for the small-signal model in the two cases. The S-parameters of the extracted model are then simulated in ADS in the same frequency range and the comparison with the measured S-parameters show a good agreement as shown in Fig. 2.12 only for a 0.7x10 μm^2 emitter DHBT.

Large signal performance of a 0.7x10 μm^2 InP DHBT were investigated at 30

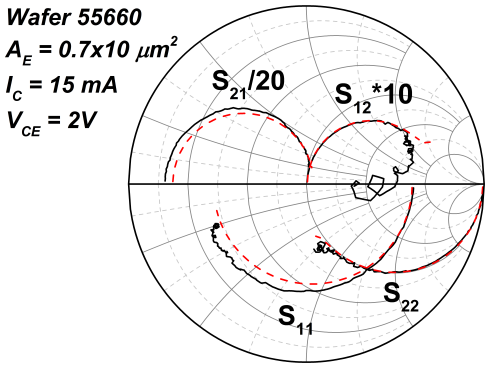

Figure 2.12: Measured (black) (250 MHz-110 GHz) and simulated (red) S-parameters of a 0.7x10 μm^2 single-finger DHBT at bias point I_C =15 mA, V_{CE} =2V.

GHz, which was the maximum operating frequency of the available load-pull

test bench. The bias point was selected for Class A operation, corresponding to (V_{CE} , I_C)=(2 V, 15 mA) for a single-finger device. In measurements, the access pad structure has not been de-embedded, so the values of the optimum loads take into account the contribution of such a structure, and the considered power levels are those present at the probe tips. The optimum load selected in order to obtain maximum output power is Z_L=58.15 + j15.3 Ω. From the P_{IN}-P_{OUT} plot

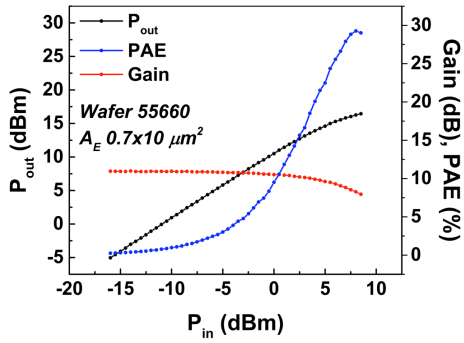

Figure 2.13: Measured power sweep for a 0.7x10 μm^2 single finger InP DHBT at 30 GHz. The device is biased in Class A with V_{CE} =2 V and I_C =15 mA. The impedance value for maximum P_{out} is equal to Z_L=58.15 + j15.3 Ω.

of Fig. 2.13, it can be seen that the saturated output power of the single-finger device is around 15 dBm and the small-signal gain is higher than 14 dB, while the power added efficiency is higher than 25% for a collector thickness of 190 nm. Once the emitter geometry is identified based on high-frequency measurements, the vertical structure is further investigated for collector optimization. In addition to measurements, a TCAD model of a DHBT was realized as an aid to evaluate high-frequency performances of different structures in terms of f_T and f_{MAX}. In the rest of the chapter the details of the TCAD model will be presented and the simulation results will then be compared to static and high-frequency measurements.

2.3 TCAD physical model

One way to accelerate the device design cycle and obtain useful insights for the future generations of fabricated devices is to employ an accurate TCAD physical model. In particular for this work, the main objective was to implement a predictive TCAD model that could be used to investigate the frequency performances of InP DHBTs with different collector structures. Many relevant publications exist pertaining HBT simulations based on SiGe [31] and InP materials [32]. For InP based HBT simulations mostly single heterojunctions have

been considered. Published works concerning InP DHBTs are less numerous. The modeling of carrier transport in DHBT devices proves to be difficult due to a more complex collector structure and carrier velocity relationship with electric field. Previous published works exist regarding simulation of InP DHBTs with InGaAs [33] and GaSbAs base[34][35]. TCAD simulations were employed to investigate device non-idealities and reliability issues concerning the interaction between electrical and thermal mechanisms [36][37][32]. The work in [33] represents probably the most complete reference in which also limited complexity circuits are simulated starting from the physical model. Although being inspired by the approach in [33], we were not able to easily replicate the results because the collector structure is somehow different and because of different commercial software employed. Other published results reach different levels of agreement compared among them and with respect to measurement results. In particular, they often present a very well modeled specific issue of a devices without showing how the model behaves with different simulation conditions (i.e. bias point, frequency range...) and device structures. In this work, an attempt was made to avoid of overfitting of model parameters in order to guarantee the flexibility of simulation for a wide frequency range and different bias conditions.

2.3.1 Simulation environment

Structure definition

The device physical simulations were carried out in the commercial software Silvaco Atlas. In the simulator, the geometry of the structure is described in terms of the epitaxial layer stack with the corresponding layout dimensions of the triple-mesa process. The default simulation results are computed for a 2D section of the device and a third dimension can be defined in the perpendicular out-of-plane direction only as a scaling factor. Taking advantage of the intrinsic symmetry of the device and physical mechanisms involved, only half of the device structure was simulated in order to reduce computational time. Calibration simulations showed that it is possible to reduce the number of simulated nodes by eliminating portions of the peripheal layers in the horizontal and vertical dimension while introducing a negligeable error. For example, the original substrate thickness was reduced from 300 μm to 80 μm and the width of the collector mesa was reduced from 4.4 μm to 2.2 μm to obtain the final simulation structure of Fig. 2.14. This reduces also the number of nodes that are present in inactive parts of the simulated structure as in the insulating layer. To each region is assigned the corresponding material including the surrounding medium. Special regions in the structure are defined to be the electrodes to

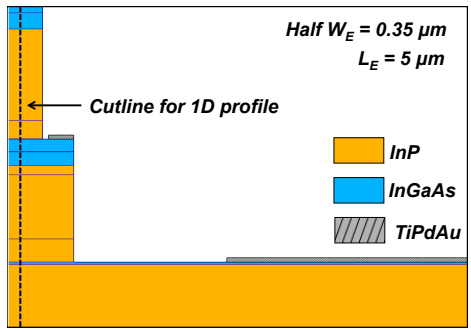

Figure 2.14: 2D section of a simulated single finger InP DHBT with 0.7 μm emitter width. Only half of the real structure is simulated to exploit intrinsic symmetry and reduce computational time.

which current and voltages are applied during simulations Fig. 2.14 also shows the cutline along which all the relevant 1D results will be presented in the next sections.

Meshing

The 2D simulation domain was carefully meshed to avoid numerical error and inaccuracies at the heterojunctions and at the interface between semiconductor and insulating material. The CPU time required for simulation is proportional to N^{α} where N is the number of nodes and α varies between 2 and 3 according to the complexity of the problem. Thus the best practice is to define a mesh fine enough in critical regions to converge to a correct solution and coarser in the rest of the structure. For the DHBT simulation problem, a straight rectangular mesh was defined without iterative refining and optimization during simulation runtime. As can be seen in Fig. 2.15 the meshing domains are finer and do not contain obtuse triangle in the vertical domain corresponding to device active area and where strong electric field exist. In the outer regions corresponding to the passivation material, these conditions are not respected but the convergence of the solution is not compromised as the electric field and conduction in this domain is practically zero. For vertical bipolar devices and in particular for HBTs the most important meshing recommendations are:

- define an adequate meshing density in zones where a high electric field is expected such as in the collector region.
- avoid obtuse triangles along the current path or in high electric field region.
- generally avoid abrupt meshing transitions. This sort of discontinuity may also cause the existence of obtuse triangles. In addition, meshing has to

be finer for frequency simulation as more resolution is needed for spatial variation of the electric field under small-signal excitation. Static simulation can be performed with a coarser mesh definition but in this work the same mesh was defined both for static and high-frequency simulations. This increases the simulation time for DC simulations but ensures the consistency with the static operating point computing during small-signal parameters simulations.

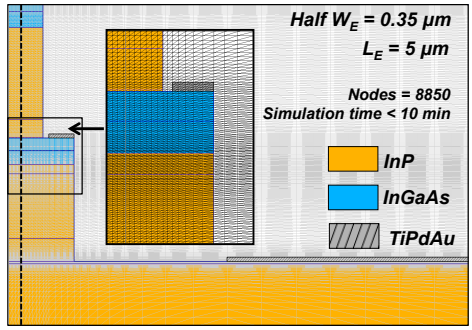

Figure 2.15: 2D section of a simulated single finger InP DHBT including meshing of the structure.

2.3.2 Material parameters

The 2D physical simulation of devices including III-V materials is performed using the hydrodynamic approach in order to correctly take into account effects occurring at the heterojunctions. A careful selection of material parameters related to InP and $In_{0.53}Ga_{0.47}As$ and parameters related to the calibration of empirical models is required. A few parameters are available in the commercial version of the simulation software while most of the values are available in previously published works. Material parameters include electron effective mass, dielectric permittivity and band diagram parameters. Many material parameters are not constant and depend on material properties like doping and device operating conditions like applied electric field and temperature. These dependencies are described by empirical models present in literature and included in the simulations. Table 2.3 summarizes the values used in this work. The emitter cap layers, the base and the subcollector layer are heavily doped at levels exceeding the nominal value of conduction band effective density of states and are thus degenerate semiconductors. In this case, the parabolic band approximation fails and this leads to erroneous simulation results in which the Fermi level reaches too deep within the conduction band. This issue is taken into account by applying the model presented in [38] to compute the relative

	InP	$In_{0.53}Ga_{0.47}As$
Bandgap (eV)	1.35	0.75
Affinity (eV)	4.38	4.59
Electron effective mass ($\frac{m_e^*}{m_0}$)	0.08	0.0463
Hole effective mass ($\frac{m_h^*}{m_0}$)	0.6	0.432
Nc ($cm^{-3}eV^{-1}$)	$5.8{\cdot}10^{17}$	$2.8{\cdot}10^{17}$
Nv ($cm^{-3}eV^{-1}$)	$1.1{\cdot}10^{19}$	$9{\cdot}10^{18}$

Table 2.3: Material parameters at T=300 K used for device simulation of InP DHBTs in this work

electron effective mass m_e^* and then the electron effective density of states N_c using a third order polynomial formula.

Bandgap narrowing (BGN)

Due to the high doping level of the base and of the cap layers ($\approx 10^{19}$) the energy band gap of InP and InGaAs decreases and also the electron affinity value is influenced. This effect has to be included in the simulation because it strongly affects the energy band diagram at the heterojunction interface. The approach used to compute the amount of BGN and its distribution between conduction and valence band is based on the model of Jain-Roulston [39] and is presented in [40]. This numerical model allows to calculate the amount of reduction of energy gap due to doping N distributed between conduction and valence band according to:

$$\Delta E_c^{BGN}(N) = C_1 \left(\frac{N}{10^{18}}\right)^{\frac{1}{\alpha}} + C_2 \left(\frac{N}{10^{18}}\right)^{\frac{1}{2}} \tag{2.5}$$

$$\Delta E_v^{BGN}(N) = C_3 \left(\frac{N}{10^{18}}\right)^{\frac{1}{\beta}} + C_4 \left(\frac{N}{10^{18}}\right)^{\frac{1}{2}} \tag{2.6}$$

with $\Delta E_g^{BGN} = \Delta E_c^{BGN} + \Delta E_v^{BGN}$ and the parameters used in the simulation are presented in [40] for InP/InGaAs abrupt HBTs. In the case of $In_{0.47}Ga_{0.53}As$ with $\approx 6{\cdot}10^{19}$ donor doping, the amount of BGN is around 100 meV and $\Delta E_c^{BGN} \approx 35$ meV and $\Delta E_v^{BGN} \approx 65$ meV.

Graded base

The concentration of Gallium with respect to Indium in the base is varied from 52.5% to 47% from the emitter to the collector side. This compositional grading introduces an additional narrowing of the energy diagram of the base layer decreasing from emitter to collector. This introduces an quasi-electric field that accelerates electrons in addition to the diffusion mechanism. From previous studies on the same technology [41], the variation of energy bandgap estimated from the emitter to collector side of the base layer is between 30 and 40 meV. The combined effect of doping related BGN and compositional grading is that the energy band gap in the base is approximately 630 meV at the collector side and between 660 and 670 meV at the emitter side. The height of the conduction band spike is approaches 200 meV at the emitter-base junction as illustrated in Fig. 2.16.

In Fig. 2.16, the energy band diagram of the base layer used for TCAD

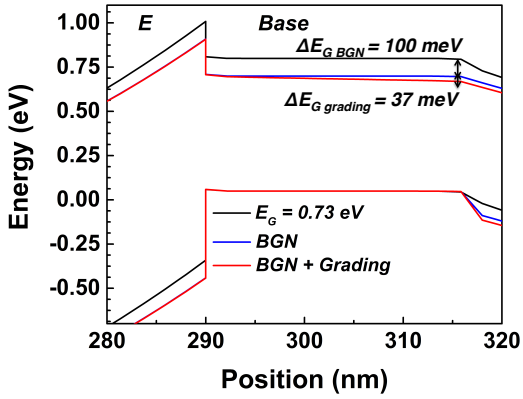

Figure 2.16: Effect of Bandgap Narrowing and compositional grading on the energy bandgap profile in the base layer taken into account in TCAD simulations.

simulations is shown when the default InGaAs E_G is used and when BGN and compositional grading effects are taken into account. The reduction of E_G at the collector side in the base with respect to the default value is of 100 meV and 37 meV for BGN and grading respectively.

2.3.3 Recombination models

For the correct simulation of DHBT current gain, recombination mechanisms need to be taken into account in different layers including recombination due to

bulk traps and surface traps. Regarding bulk traps recombination, three physical mechanisms are taken into account for 2D simulations: Shockley-Read-Hall (SRH), Auger and radiative recombination.

Bulk and surface SRH

SRH recombination rate R^{SRH} is computed for every layer according to:

$$R^{SRH} = \frac{np - n_i^2}{\tau_p \left(n + n_i e^{\frac{E_T}{k_B T}} \right) - \tau_n \left(p + n_i e^{\frac{-E_T}{k_B T}} \right)} \tag{2.7}$$

where τ_n and τ_p are electron and hole lifetimes respectively and E_T is the trap energy level with respect to the valence (conduction) band for donors (acceptors). Starting from the results of previously published works based on the same technology [37], recombination centers are assumed to be located at mid gap and and since n$\gg$p in the emitter layer, τ_n and τ_p are assumed to have the same value. τ_n and τ_p are both set to 1 ns for InP and to 1 ns and 5 ns for InGaAs.

Radiative recombination

Radiative recombination is taken into account in every layer according to:

$$R^{rad} = C^{rad} \left(np - n_i^2 \right) \tag{2.8}$$

where the coefficient C^{rad} is set to $6.6{\cdot}10^{-11}$ for InP and $1.4{\cdot}10^{-10}$ for InGaAs.

Auger recombination

For doping levels higher than 10^{19} Auger recombination mechanism becomes dominant especially in the InGaAs base layer. Auger recombination rate can be computed using the following equation:

$$R^{Auger} = C_n^{Auger} \left(pn - nn_i^2 \right) + C_p^{Auger} \left(pn - pn_i^2 \right) \tag{2.9}$$

Auger recombination coefficients for InGaAs are usually in the range 10^{-30}-10^{-28} cm^6/s and were set to C_n^{Auger}=$5{\cdot}10^{-30}$ and C_p^{Auger}=$3{\cdot}10^{-29}$ based on recombination current measurements.

Surface traps

Surface traps (ST) are surface defects of the semiconductor lattice caused for example by missing interface atoms and have strong influence on device electrical performance. From the energy point of view, STs are located within the forbidden material bandgap and can contribute to carrier capture and emission according to SRH model. The impact of surface defects needs to be included in DHBTs simulations in order to obtain a good correlation with the static experimental results concerning Gummel plot and output characteristics. In a DHBT triple-mesa structure, it was shown that traps mostly critical for device simulation are located on the emitter lateral sidewall and on the base ledge between emitter and base contact as shown in Fig.2.17.

The main parameters to define in the simulation models are the location of the

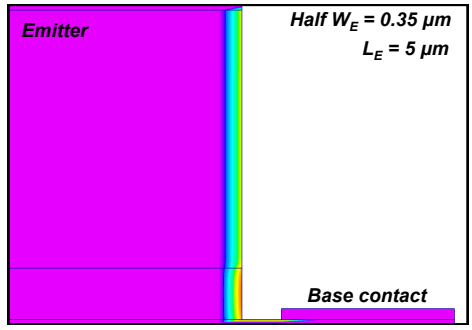

Figure 2.17: Location of surface traps at emitter sidewall and base ledge for device simulation.

surface traps, the trap density and energy level and the capture cross-section. The values used in this work are based on [42] and [37], although some slight modification in trap energy level has to be applied between different devices to better fit the base current in Gummel plot. Table 2.4 summarizes the parameters for surface trap implemented in ATLAS.

2.3.4 Transport models

Heterojunction current transport

The interface between the InP emitter and the InGaAs base and between the InGaAs spacer and the InP collector of a DHBT is an abrupt heterojunction. Carriers' flow is controlled by two main physical mechanisms involved shown schematically in Fig. 2.18:

Material	Missing atom	Type of trap	E_T - E_V	ST density
InP	In	Donor	1.2	N_T
	P	Acceptor	1	N_T
InGaAs	In	Donor	0.61	$0.53\times N_T$
	Ga	Donor	0.24	$0.47\times N_T$
	As	Acceptor	0.36	N_T
N_T is equal to 3×10^{12}				

Table 2.4: Parameters for surface trap model

- Thermionic emission of electrons *over* the emitter-base barrier
- Tunnel effect *through* the emitter-base spike

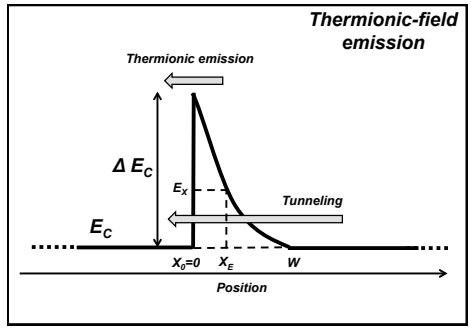

Figure 2.18: Schematic illustration of physical mechanism for carrier transport at heterojunction

The carrier transport between the two regions is described by the *thermionic field-emission* model that takes into accounts both effects [43]:

$$J_n = qv_{Tn}(1+\delta)(n_E - n_B e^{\frac{-\Delta E_c}{k_B}}) \tag{2.10}$$

where J_n is the electron current density and v_{Tn} is the electron thermal velocity. The superscript E and B denotes the emitter and base region. The parameter δ accounts for the contribution of the tunneling current and can be calculated from:

$$\delta = \frac{1}{kT}\int_{E_{min}}^{{E_C}^E} e^{\left(\frac{E_c^E - E_x}{kT}\right)} e^{\left(\frac{-4\pi}{h}\int_0^{X_E}[2{m^*}_n(E_C-E_x)^{0.5}]dx\right)} dE_x \tag{2.11}$$

where $E_{min} = max[E_C(0^-), E_C(W)]$ and E_x is the energy component in the x direction as described in Fig. 2.18 for the case E_{min}=$E_C(0^-)$=E_C(W)

The thermal velocity is defined as:

$$v_{Tn} = \frac{{A_n}^* {T_L}^2}{qN_c} \tag{2.12}$$

where T_L is the lattice temperature, N_c is the electron effective density of states in the emitter and ${A_n}^*$ is the effective Richardson constant. For simulations, it is sufficient to consider bias points with $V_{BE} > 0.75$ V as this is often the region of operation of the device. Since the height of the emitter-base spike is quite reduced for this bias, the thermionic emission is the dominant effect at the emitter base junction while tunneling could be neglected. The thermionic field-emission model is not activated at collector-base junction.

Energy balance model

Starting from Boltzmann transport equation two transport models can be derived:

- Drift-Diffusion (DD)
- Energy Balance (EB) and its simplified form Hydrodynamic Model (HD)

The DD transport model is the simplest from the conceptual and numerical point of view. The main advantage is that the only independent variables are electron and holes concentration n and p and the potential ϕ. Despite being the most popular transport model for device simulation, it can lead to erroneous results for submicron InP DHBT. Indeed it does not take into account important phenomena as *hot electrons* that occur in devices with submicron dimensions. On the other hand, the EB and HD models are more advanced and include additional variables to be explained later, leading to more accurate physical results. The trade-off between DD and EB models comes in the form of additional simulation time and added difficulty to converge of the resolution algorithm. The EB model follows from a simplified form of the Boltzmann transport equation according to Stratton derivation [44]. The HD model is further derived from the EB model by changing suitable parameters as it will be described in the next sections. In the EB model two additional variables are added to the systems of equations already defined for the DD model. These variables are the electron and holes temperatures (related to their respective energies) defined as T_n and T_p respectively. A new term is added to the current density expressions:

$$\begin{aligned} J_n &= qD_n\nabla n - qn\mu_n\nabla\psi + qn{D_n}^T\nabla T_n \\ J_p &= qD_p\nabla p - qp\mu_p\nabla\psi - q + p{D_p}^T\nabla T_p \end{aligned} \tag{2.13}$$

where $D_n{}^T$ and $D_p{}^T$ are coefficients of thermal diffusion. In addition to third term in Eq.2.13, the concept of *energy flux density* between carriers and lattice is introduced for electrons and holes as S_n and S_p , respectively. These terms are described as:

$$\begin{aligned} S_n &= -K_n \nabla T_n - \left(\frac{k_B \delta_n}{q}\right) J_n T_n \\ \nabla \cdot S_n &= \frac{J_n E}{q} - W_n - \frac{3k_B}{2}\frac{\partial (nT_n)}{\partial t} \\ S_p &= -K_p \nabla T_p - \left(\frac{k_B \delta_p}{q}\right) J_p T_p \\ \nabla \cdot S_p &= \frac{J_p E}{q} - W_p - \frac{3k_B}{2}\frac{\partial (pT_p)}{\partial t} \end{aligned} \tag{2.14}$$

where W_n and W_p are the energy loss rates , K_n and K_p are thermal conductivities and δ_n and δ_p are transport parameters for electrons and holes, respectively. The above-mentioned parameters are defined as (here shown for electrons as equations for holes are analogous):

$$\begin{aligned} \delta_n &= \frac{5}{2} + \xi_n \\ D_n{}^T &= \frac{k_B \mu_n}{q}(1 + \xi_n) \\ K_n &= q n \mu_n \left(\frac{k_B}{q}\right)^2 \delta_n T_n \end{aligned} \tag{2.15}$$

In these equations a new parameter was introduced, ξ_n that describes the dependence of the transport model on the temperature dependent carrier mobility according to:

$$\xi_n = \frac{d(ln\mu_n)}{d(lnT_n)} = \frac{T_n}{\mu_n}\frac{\partial \mu_n}{\partial T_n} \tag{2.16}$$

According to the value of ξ_n the EB or HD model can be selected:

- ξ_n=-1 implements the EB model. In this case $D_n{}^T$ is equal to zero and the third term in the current density equation is eliminated.
- ξ_n=0 implements the HD model.

The energy rate loss W_n and W_p quantify the physical mechanisms through which carriers exchange energy with the lattice. These mechanisms include: carrier heating through increased lattice temperature, energy exchange through

generation-recombination processes. The generation-recombination relation for electrons is defined as (analogous for holes):

$$U = R_{SRH} + {R_n}^A - G_n \tag{2.17}$$

where R_{SRH} and ${R_n}^A$ refer to Shockley-Read-Hall and Auger respectively and G_n is generation through impact ionization. The energy loss rate can thus be expressed as:

$$W_n = \frac{3}{2} n \frac{k_B(T_n - T_L)}{\tau_{en}} + \frac{3k_B}{2} T_n R_{SRH} + E_g(G_n - {R_n}^A) \tag{2.18}$$

where T_L is the lattice temperature and E_g is the bandgap of the material. In Eq. (2.18) the parameter τ_{en} is the electron relaxation time (τ_{ep} for holes). The relaxation time defines the first-order time constant for the energy exchange between carrier and lattice. The value of the relaxation time for each material is based on the empirical model extracted from MonteCarlo simulations as presented in [45]. Although the range for the relaxation time is considered to be between 10^{-13}-10^{-11} s for InP and InGaAs materials, the exact value may differ in the different regions of the device and have a significant impact on the final results concerning accuracy and ability of the algorithm to converge. In ATLAS simulator the parameters to be set for EB and HD simulation are ξ_n and τ_{en} and their influence on final results will be discussed later in this chapter. The transport parameters set for every simulation model presented in this work are presented in Appendix A.

Description of hot electron transport

As mentioned in the previous section, one important feature of the EB and HD models is to take into account additional physical effects in the constituent formulas of the model. The carrier drift velocity in a semiconductor under the influence of an uniform electric field is proportional to the strength of this field *E*. Only in the limit where E tends to zero the proportionality constant is a property of the semiconductor material called mobility. When an electric field is applied to the material, carrier move as an ensemble and their velocity v follows a Maxwellian distribution *f(v)*. The application of an electric field produces a change in the average carrier kinetic energy that in thermodynamic equilibrium is equal to $3/2k_BT_L$ where k_B is the Boltzmann constant and T_L is the equilibrium lattice temperature. Thus, if we express the dependence of carrier average kinetic energy from electric field as $3/2k_BT(E)$ the temperature *T(E)* is referred to as *carrier temperature*. Along their path, carriers however lose part of their kinetic energy because of collisions with the crystal lattice. In thermodynamic equilibrium the kinetic energy gained by the carriers under an

applied external force is equal on average to the energy transfered to the lattice by collisions. Under high electric field the kinetic energy acquired by the carriers can exceed the one transferred to the lattice and as a result the field dependent temperature *T(E)* increases. These carriers are called *hot electrons* and are typically present in the base and collector region of InP DHBTs. EB and HD models can take this phenomena into account and allow to define carrier mobility as a function of electric field through the dependence on carrier temperature *T(E)*. During EB and HD simulations an effective electric field is computed for electrons starting from the definition of carrier kinetic energy:

$$E_{eff}^2 = \frac{3}{2}\frac{k_n(T_n - T_L)}{q\mu(E_{eff})\tau_{mob}} \tag{2.19}$$

where k_n is the Boltzmann constant, T_n is the equivalent electron temperature, $\mu(E_{eff})$ is the chosen energy dependent mobility model for EB simulation and τ_{mob} is an electron relaxation time parameter related to the mobility. Formally, the electron relaxation time of the EB model in Eq. 2.18 and τ_{mob} are two distinct parameters but the same numerical value is set for τ_{en} and τ_{mob}. Equation 2.19 does not contain spatially varying terms and the effective electric field is then inserted in the chosen mobility model until convergence to a consistent solution.

Low-field mobility

For each semiconductor layer a low-field mobility μ_{n0} (μ_{p0} for holes) has to be defined. This parameter depends mainly on scattering processes with lattice atoms and ionized impurities due to doping. For the simulations in this work the empirical doping dependent low-field mobility model was used based on the results published in [46]:

$$\mu_0 = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N}{N_{REF}})^{\lambda}} \tag{2.20}$$

where μ_{max} is the mobility value for very low doping levels, μ_{min} is the lower limit of the material mobility and occurs at very high-doping levels, N_{REF} is the doping concentration at which the material mobility is half of the μ_{max} value and λ is an empirical parameter . The values for this parameters are provided in [46] for InP and $In_{0.53}Ga_{0.47}As$. The value of μ_0 is computed for each layer both for electrons and holes and inserted as a constant value at 300 K in the simulator. The temperature dependence of all the parameters model can be taken into account in order to compute $\mu_0(T)$.

High-field mobility

In the presence of high electric fields, carrier velocity saturates to a constant value. Differently from Silicon, carrier velocity as a function of electric field in InP and InGaAs reaches a peak value and then decreases before saturation. Nevertheless, the choice and implementation of the correct high-field mobility model for the simulations is one of the most critical factors to assure both the numerical convergence and the physical correctness of the results. The models available in the Silvaco commercial software are based on two fundamental formulas to describe the transition between the low-field and high-field mobility: a Silicon-mobility based model and a mobility model that takes into account the velocity overshoot present in InP and InGaAs material. The Silicon mobility model is based on Caughey-Thomas work [47]:

$$\mu(E) = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E}{v_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{2.21}$$

where μ_0 is the doping dependent mobility at low electric fields, v_{sat} is the carrier saturation velocity at high-electric fields and beta is a model parameter. In the simulations presented in this work, the coupled equations of the EB transport model are solved only for the electrons and energy dependent mobility model are not employed for holes. The reason for this approximations is that holes are mostly confined in the base layer and in the spacer of the DHBT because of the high valence band barriers at the heterojunctions with emitter and collector. This means that hole injection should not occur in normal operating regime. A comparison has been made to verify the simulations of holes both with EB and DD models and the results showed no significant difference. The high-field mobility model implemented for holes is always the Silicon mobility model without dependence on carrier energy.
The high-field mobility description that includes the physical effect of velocity overshoot takes into account the negative differential mobility region after the peak velocity. The empirical model is based on the formula from Barnes et al. [48]:

$$\mu(E) = \frac{\mu_0 + \frac{v_{sat}}{E}\left(\frac{E}{E_{crit}}\right)^{\gamma_n}}{1 + \left(\frac{E}{E_{crit}}\right)^{\gamma_n}} \tag{2.22}$$

where γ is a model empirical parameter, v_{sat} is the final saturation velocity and E_{crit} is the electric field value where carrier velocity reaches its peak. Figure 2.19 shows the velocity computed using the two models of Eq. 2.21 and 2.22 applied to an InGaAs and InP layer with low-field mobilities μ_{n0} of 10000 and 4000 $cm^2/(Vs)$, respectively. The value for both models are listed in Tab. 2.5 and Tab. 2.6

From Fig. 2.19 it can be seen that for high-electric fields the two models are ba-

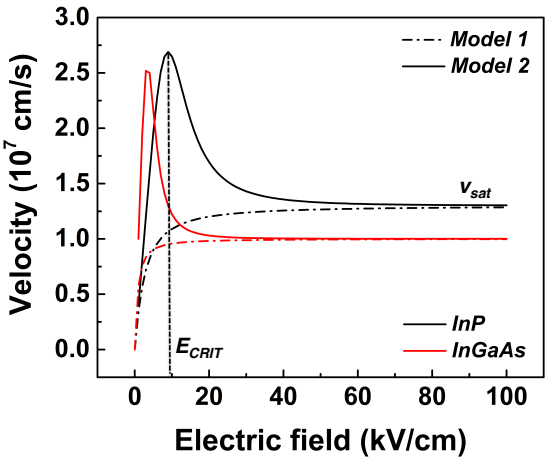

Figure 2.19: Electrons velocity profile computed using both mobility models of Eq. 2.22 (Model1) and 2.21 (Model2) for InP and InGaAs layers with μ_{n0} equal to 4000 and 10000 $cm^2/(Vs)$, respectively.

Table 2.5: List of parameters used for high-field mobility model of InP and $In_{0.53}Ga_{0.47}As$ of Eq. 2.21.

	$v_{sat_n}(cm/s)$	$v_{sat_p}(cm/s)$	β_n	β_p
InP	1.3×10^7[49]	6.6×10^6 [50]	1.25	1
$In_{0.53}Ga_{0.47}As$	1×10^7[51]	4.9×10^6 [52]	1.25	1

sically equivalent and they converge to the same saturation velocity. Therefore it makes sense to compare them in terms of accuracy with respect to measurements. It is important however to verify that neglecting their main difference, the description of the velocity overshoot effect, does not affect critically the simulations whenever a transition between low and high-field regime occurs (i.e. in I-V simulations). Figure 2.19 is an analytical computation of the carrier velocity based on the local electric field: the actual velocity profile during simulation depends also on the carrier energy and the related effective field (see Eq.2.19). Since the relation between mobility and carrier energy is based on coupled non-linear equations, running complete simulations is needed to obtain the total velocity profile across the structure.

Table 2.6: List of parameters used for high-field mobility model of InP and $In_{0.53}Ga_{0.47}As$ of Eq. 2.22 . The subscripts n and p refer to electron and holes.

	v_{sat} (cm/s)	E_{crit} (V/cm)	γ
InP	1.3×10^7 [49]	1×10^4	4
$In_{0.53}Ga_{0.47}As$	1×10^7 [51]	4×10^3	4

2.4 Simulation results and discussion

This section presents the simulation results based on the TCAD 2D model discussed earlier in this chapter. The reference device chosen for model implementation and parameters calibration is a 0.7x5 μm^2 single finger DHBT with a total collector thickness of 190 nm. The desired requisites for the TCAD model are the following:

- Convergence for static simulations of reverse and forward Gummel plot, I_C -V_{CE} curves
- Convergence for frequency simulations at different bias points.
- Consistence of physical and model parameters with respect to published literature and real physical effects.

In the next paragraphs static and high frequency-simulation results will be compared with measurements. In particular, the results will be based on the four combinations of mobility models and transport parameters described in Sec. 2.3.4. Starting from available published data, a calibration procedure was applied to each model in order to reproduce the measurement results while respecting all the above-mentioned requisites. In particular, in this work the focus has been set to have a good fit with S-parameter measurements while ensuring reasonable results for the simulation of static characteristics. The schema of Fig. 2.20 summarizes the logical steps needed to calibrate the models and eventually select the best one in terms of agreement with measurement results and compliance with the chosen requisites. The procedure has to be applied to every different model separately and then the different results have to be compared as it will be shown in the next sections. The first step is Gummel plot simulation starting from published data. The alignment between base and emitter layer has to be determined to have a good fit between the simulated and measured I_C as described in [35]. Parameters related to surface trap can also be adjusted to have a better fit of I_B current in the low V_{BE} range. I-V curves are then compared in order to assess the numerical convergence of the chosen mobility

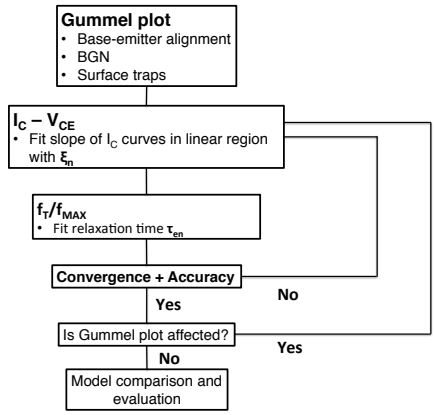

Figure 2.20: Procedure for the calibration of model parameter and model evaluation

model and the transport parameters. The following step is the simulation of f_T and f_{MAX} at different bias points in order to verify the agreement between the predicted peak value and the degradation due to high-injection effects. Since both simulations involve the presence of high electric field at the base-collector junction, the two last steps are usually performed in a feedback loop in which the default transport parameters are modified focusing on f_T and f_{MAX} simulations. When a modification to the transport parameters leads to a good f_T and f_{MAX} prediction it has to be tested with an I-V simulation with the same parameters to ensure convergence and to evaluate the effects of the modifications (i.e. the parameter ξ_n on the slope of I_C -V_{CE} curves [31]) . Indeed, the calibration of transport parameters ξ_n and τ_{en} is strongly related to the choice of the high-field mobility model in order to obtain the correct result. After the feedback iterations between I_C -V_{CE} and f_T and f_{MAX} simulations, the model including the new parameters is tested again in a Gummel plot simulation to ensure that the process does not affect the results at low-electric fields. Finally, the last step is the evaluation of the resulting set of parameters for the model based on their performances and their physical consistency. As it will be shown in the following sections, in some cases different models with different set of parameters might both lead to a correct result in some specific cases. Before deciding that they are equivalent, their consistency in all bias conditions should be assessed. In addition, just in order to allow numerical convergence the choice of some models might force the adjustment of physical parameters (i.e. band alignment or saturation velocities) more than what is allowed from the limits of what is published knowledge. Even if some alternatives can provide simulations fairly in agreement with measurement results, it is good practice to try to adopt a model that requires the less amount of "strain" on physical parameters. Even

if the procedure presented in this work could fail to find a solution, the main objective is to ensure that the set of chosen parameters is consistent through all the bias conditions and is robust in terms of numerical convergence. Results from equivalent simulations including three different high-field mobility descriptions will be compared and discussed in the following sections. In particular, four combinations of high-field mobility models and EB transport parameters (carrier relaxation time and thermal diffusion coefficient) will be considered in the following of this chapter:

- Model 1: Silicon-like mobility that does not take into account velocity overshoot of InP and InGaAs but defines the same saturation velocity v_{sat} . Default EB transport parameters.

- Model 2A: III-V compounds based model that take into account both velocity overshoot and carrier temperature dependence of the velocity. Default EB transport parameters.

- Model 2B: same mobility description as Model 2 but EB transport parameters fit to f_T and f_{MAX} measurements following the procedure described above.

- Model 3: III-V compounds based model that take into account both velocity overshoot but implements only an electric field dependent velocity. Default EB transport parameters.

For Model 2 two cases will be presented: one using the default parameters for the relaxation time and energy dependent diffusion coefficient (2A) and one using the parameters calibrated for a correct f_T and f_{MAX} simulation of the reference device (2B). The electric field E used at runtime for the calculation of the high-field mobility in Model 1 and 2 corresponds to the effective electric field introduced in Eq. 2.19.
Model 3 implements an energy independent mobility model starting from the same definition of Eq. 2.22: in this case, the electric field appearing in the equation is actually the local electric field at the node where the equation is computed and does not take into account the effect of carrier temperature. In the following sections simulations results for the different models will be presented and compared. For the four models investigated in this chapter, the final list of mobility and transport parameters can be found in Appendix A

2.4.1 Static simulations

Gummel plot

Figure 2.21 shows TCAD simulation results when the device is at equilibrium condition. Figure 2.21-A presents the equilibrium electric field in the vertical direction across the structure computed for the different models. The simulated electric field profile is very similar for all the considered models. At the base-collector interface the profile of a p-i-n structure can be observed between the high p-doped base, the intrinsic spacer layer and the n-doped collector. Figure 2.21-B shows the simulated 1D profile of the electron mobility across emitter, base and collector layers. Since the device is in the equilibrium condition, the low-field mobility model of Eq. 2.20 based on ionized dopants is the predominant model in the computation of the equilibrium mobility. In this case, the main difference between the model is in the low-field mobility value assigned to the InGaAs spacer layer. All the models, except Model 3, simulate a high-mobility value of approximately 11000 cm^2/Vs predicted by Eq.2.20 for a very low-doped layer. In the case of Model 3 the simulated equilibrium mobility for the InGaAs spacer is critically lower at 200 cm^2/Vs.

Figure 2.22 presents the comparison between the measured and simulated

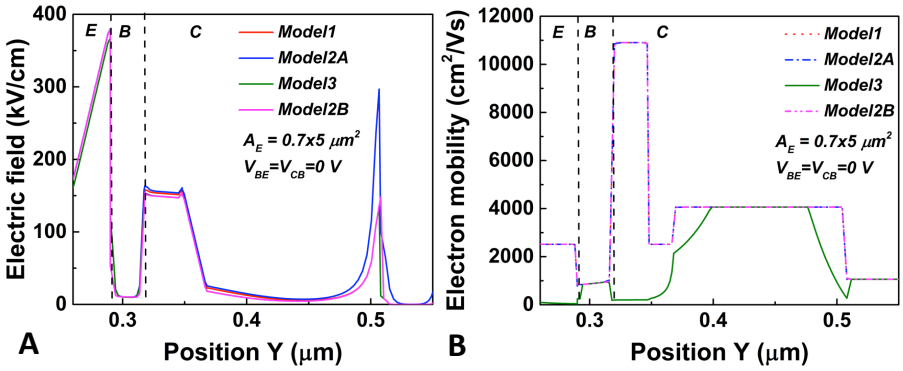

Figure 2.21: A) Electric field and B) low-field mobility of a 0.7x5 μm^2 single-finger DHBT simulated by 2D TCAD.

Gummel plot. Figure 2.22-A shows the comparison between Model 1, Model 2A and Model 3 while Fig. 2.22-B presents the results obtained by simulations using the optimized Model 2B. Model 1 and Model 2A in Fig. 2.22- A obtain comparable results and the simulated I_C is in agreement with the measured values up to 0.8 V; the simulated value of I_B is in agreement with measurements in the lower V_{BE} range but it is overestimated for $V_{BE} > 0.75$ V. From the Gummel plot of Fig. 2.22-B it can be seen that the collector and base current

simulated using Model 2B are in reasonable agreement with the measured quantities across the whole V_{BE} range. In this case the base current is well predicted for $V_{BE} > 0.75$ V while the difference between simulation and measurements is larger in the range $V_{BE} < 0.75$ V. The ideality factor of the base current I_B in the mid-low range for these devices depends strongly on the energy level set for interface traps. This is considered an acceptable result since the operating region for the device in this work lies in the upper V_{BE} range.

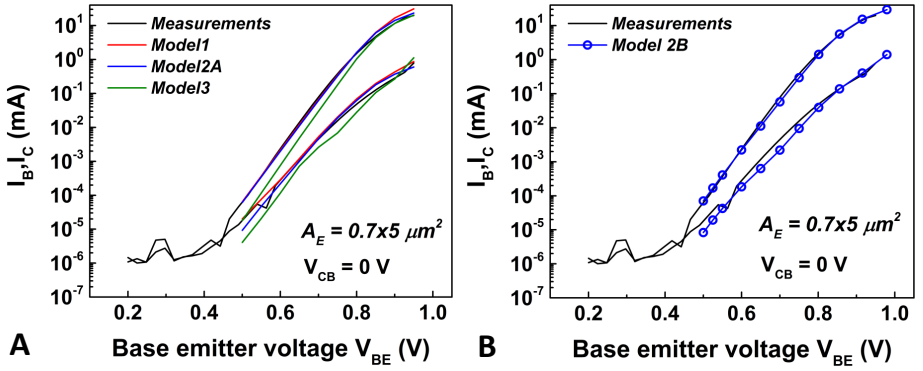

Figure 2.22: A) Comparison of the different models and B) of Model 2B after fitting with measured Gummel plot of 0.7x5 μm^2 single-finger DHBT.

Figure 2.23 is a plot of the static forward gain β vs. V_{BE} computed from the Gummel plot results presented in 2.22. The simulated curves in Fig.2.23 are in general agreement with the value extracted from measurements in particular Model 1, Model 2A and 2B. According to the figure, Model 1 and Model 2 do not predict gain collapse in the simulated V_{BE} range. Even if from Fig. 2.23-B Model 2B seems to correctly predict the critical current at which the collapse occurs, a closer look to the upper part of Fig. 2.22-B shows that in reality the current I_B does not increase with the same slope as in the measurements. A plot of the simulated β is not sufficient to evaluate the accuracy of the model for what concerns the prediction of the critical current at which current gain collapse occurs.

In order to further investigate this point, the electric field profile is presented for the different models correponding to the bias point with $V_{BE} = 0.95$ V and $V_{BC} = 0$ V and the result is presented in Fig. 2.24-A for all the considered models. When the V_{BE} is increased to 0.95 V and thus the current injection increases, a spike in the electric field in the collector region can be observed. This electric field inversion starts to occur corresponding to the interface between highly n-doped and low n-doped InP layers. In particular, for the considered bias point for Model 1 and Model 3 the inversion has occurred while for Model 2A-B the field is still negative. For Model 1 and Model 3 the inversion of the

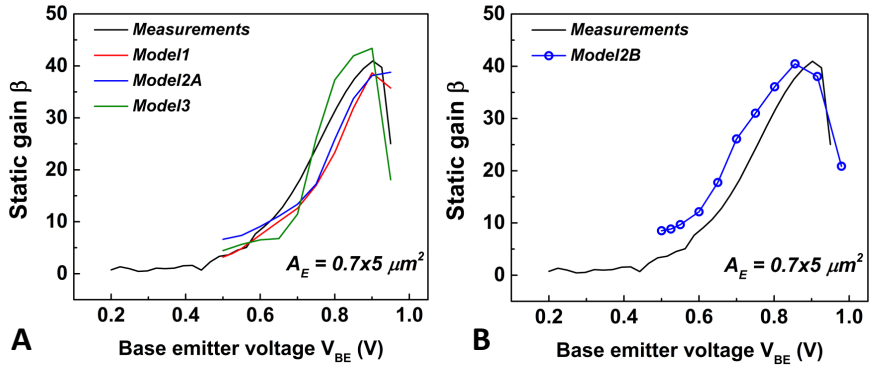

Figure 2.23: Comparison of the different models and B) of Model 2B after fitting with static forward gain β of a 0.7x5 μm^2 single-finger DHBT.

electric field occurs at $J_C \approx 3$ mA/μm^2 while for Model 2A and Model 2B it occurs at $J_C \approx 3.8$ mA/μm^2 . This effect, common in DHBTs, is associated with the appearance of a barrier at the base-collector junction due to the presence of the valence band discontinuity as described in [53]. Since in the measured curves the collapse of the current gain has already occurred at the considered bias point, it can be concluded that the current at which the gain collapse occurs for simulation using Model 2A-B is underestimated and the gain collapse is predicted to occur at higher current densities.
From Fig. 2.24-B it can be seen how the different transport and mobility parameters impact the carrier mobility profile during device operation. In particular, it is important to notice how the mobility (and thus the carrier velocity) is affected in the spacer layer with respect to the electric field profile shown in Fig. 2.24-A. The different models simulate a different field profile in the InGaAs spacer region with Model 2A having the highest absolute value and Model 3 and 2B having a value close to zero. This strongly affects the simulated mobility profile for electrons in the same layer, with the mobility value being higher for lower electric fields, as described in Sec. 2.3.4.On the other hand, the mobility profile in the InP n$^-$ layer in the collector is constant for Model 1 and 2 A-B while it starts from a peak value and then decreases monotonically for Model 3. Model 1 and Model 2 A-B are the ones that show comparable results and the best fit with Gummel plot measurements as discussed earlier. Thus, it can be concluded that the same result can be obtained with different modeling choices concerning the InGaAs spacer while the velocity profile in the other collector regions is the most critical quantity to have a good fit with the measurements.

In order to further investigate how the different models describe the current transport through the base-collector junction, simulation results were compared with reverse Gummel plot measurements. For these measurements the base-

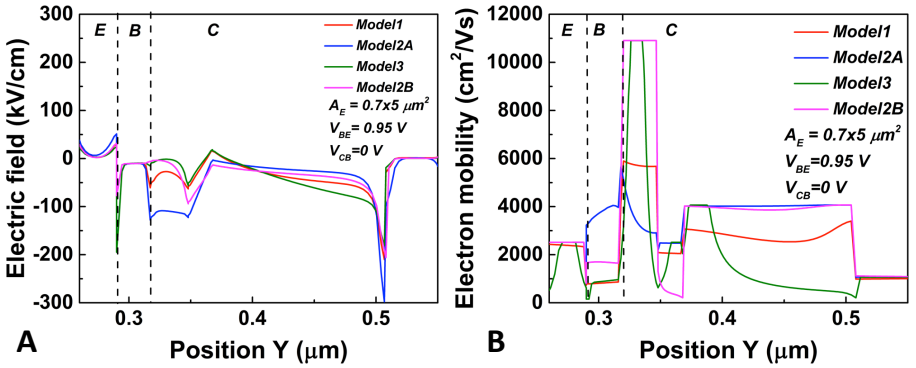

Figure 2.24: Comparison of the different model for (A) electric field and (B) electron mobility in the Y direction for a 0.7x5 μm^2 DHBT biased at V_{BE} = 0.95 V and V_{CB} = 0 V.

collector voltage V_{BC} is swept from 0 to 0.9 V with V_{BE} = 0 V. This kind of simulation shows consistent convergence when using Model 2B while it fails when using any other model. Fig. 2.25 shows the comparison between measurements and simulations of a reverse Gummel plot using Model 2B. The agreement between the I_C and I_B ideality factor indicates that the BC junction DC back-injection is well modeled for the largest part of the voltage range. The current value saturates to a slightly higher value in the TCAD results, meaning that the simulated series resistance at the emitter or collector side have a lower value than in reality. Also, in the simulations the currents I_C and I_B are equal for most of the V_{BE} interval, I_E is equal to zero indicating that there is no injection from the base to the emitter. Only for higher values of V_{BE} the difference between the two currents starts to appear. This is not the case in the measurements, where a difference between I_C and I_B can be observed for a large part of the sweeping interval.

Output I-V curves

Figure 2.26 show the comparison of simulated and measured output curves of a 0.7x5 μm^2 single-finger DHBT. The measurement conditions were reproduced in simulation and the device was biased with different base currents I_B ranging from 0 to 0.48 mA with a 0.12 mA step. The collector-emitter voltage V_{CE} is swept from 0 to 2 V. This simulation requires a precise calibration of mobility and transport parameters to predict the collector current for the entire voltage range from 0 to 2 V. In particular, the slope of I_C (V_{CE}) (the device output conductance) strongly depends on the ξ_n value and relaxation time set in the

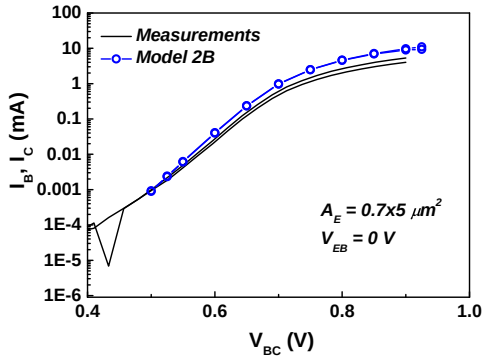

Figure 2.25: Measured and simulated reverse Gummel plot of 0.7x5 $\mu\mathrm{m}^2$ single-finger DHBT. The base-collector voltage V_{BC} is swept with V_{BE} = 0 V.

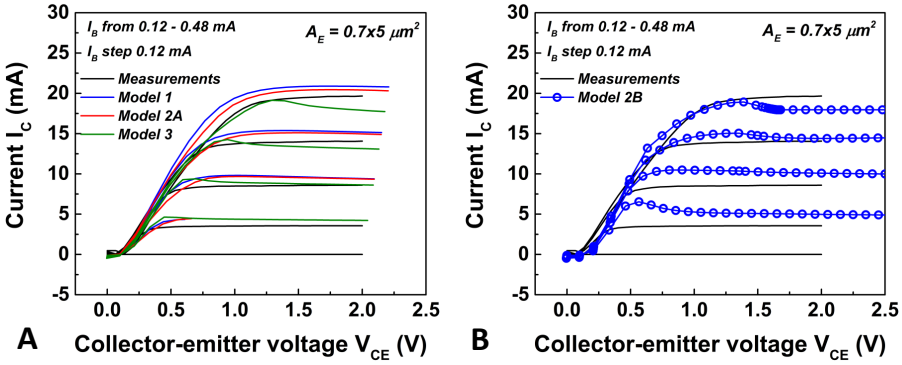

Figure 2.26: A) Comparison of measurements with different models and B) fitted Model 2 of I_C (V_{CE}) curves of a 0.7x5 $\mu\mathrm{m}^2$ DHBT. The bias current base is varied from 0 to 0.48 mA with a 0.12 mA step.

base and collector layers as it was shown in [31] for SiGe HBTs.
Figure 2.26-A shows the comparison of measurements with simulated results using Model 1, 2A and 3. The simulation including Model 1 and 2A do not converge for low bias current value as shown by the absence of the curve corresponding to $I_B = 0.12$ mA. The part of the output curves corresponding to the knee region presents a smooth transition towards the linear region for Model 1 and 2A while an overshoot can be observed for Model 3. In the linear region, the curves simulated with Model 1 and 2A always flatten to a constant value. The curves obtained with Model 3 instead reach lower I_C current values with increasing bias current I_B and at the same time exhibit a negative slope. The first effect is due to the collapse of current gain occurring early for Model 3 simulations as shown earlier. The second effect depends on the relationship

between the chosen high-field mobility model and the carrier temperature and can be modified by a different choice of the parameter ξ_n occurring in Eq. 2.16. The comparison between Model 2B simulations and measurements is shown in Fig. 2.26-B. Since Model 2B is based on Model 2A after a parameter calibration based on f_T and f_{MAX} measurements it is worth to compare the effect of the calibration process on the static performances. It was already shown earlier that the impact was not significant for the forward Gummel plot simulations while it is more evident in the case of I-V curves. A significant deviation exists between physical simulations and measurements in the knee region. The overshoot in the output I_C current can be observed especially at low I_B bias currents. The V_{CE} voltage needed for the collector current to flatten to a constant value is higher with respect to model 2A. However in Model 2B simulations the I_C curves do not exhibit the negative slope for sufficiently high V_{CE} values. Also, an offset voltage is present greater than what is observed in measurements. This means that in the physical model, the BE junction needs a larger applied voltage to be more conductive than the BC junction. Additional simulations indicate that this could be corrected by changing affinity level in the emitter or cap layers. This however affects other model parameters and numerical convergence thus was not applied. Furthermore, even in the active region the simulated and measured curves do not perfectly overlap and they are at higher current level in simulations. This is because the forward current gain is slightly higher in the simulated device due to absence of some recombination mechanism that is not properly modeled.

To compare how the choice of a different transport and mobility model affects the simulation of device operation the carrier temperature profile and velocity across are presented in Fig. 2.27. The two profiles are simulated for a device biased with $I_B = 0.36$ mA and $V_{CE} = 2$ V. In this operating condition the voltage drop across the base-collector region is high to highlight the differences between the considered high-field mobility models. The simulated carrier temperature profile for Model 1 and Model 2A in Figure 2.27-A are very similar considering the spatial variation and the maximum value. In both cases, the equivalent carrier temperature (and thus their kinetic energy) increases already from the spacer layer and reaches its peak in the initial part of the low doped collector layer. Model 2B and 3 instead simulate a carrier temperature with a profile much more skewed towards the end of the collector structure. The peak value for Model 2B is comparable to the value obtained in Model 1 and 2A simulations around 5000 K. A significantly lower value around 2000 K is obtained from Model 3 simulations.

Figure 2.27-B shows the results obtained by simulations when the temperature profile is coupled with the corresponding mobility model. It is important to notice that even though Model 1 and 2A have almost identical temperature profiles the resulting carrier velocity is not exactly the same due to the different high-field mobility models used. In particular, the carrier velocity profiles for Model 1 and 2A have the same qualitative behavior but the average veloc-

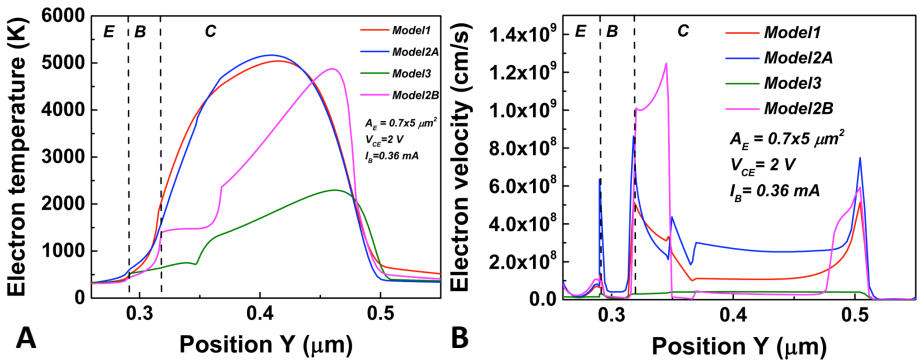

Figure 2.27: Comparison of A) carrier temperature profile and B) electron velocity of a 0.7x5 μm^2 single-finger DHBT simulated with different transport models. For all the simulations the device is biased at V_{CE} = 2 V and I_B = 0.36 mA.

ity value in the low-doped collector layers is 4 times higher at a value around 4×10^8 cm/s. In both cases the average velocity in the collector higher than 10^8 cm/s seems unrealistic from the physical point of view. The carrier velocity profile corresponding to Model 3 simulations predicts an average velocity in the low-doped collector layer equal to 4×10^7 cm/s that is more physically sound and in agreement with previously published results [33][34]. Model 2B presents a velocity profile in which the carriers reach a physically impossible velocity in the InGaAs spacer ($\approx 10^9$ cm/s) before arriving in the InP collector region where the average velocity is 4×10^7. The velocity value simulated for the spacer region is clearly unrealistic even in an entirely ballistic transport regime in the spacer layer. According to the simulation results, the electrons would travel across the spacer without scattering and almost instantaneously before being collected. The consequence is that the transit time associated with this zone is therefore negligible compared to the terms associated with the transit time in other layers. This constitutes also a major limitation of this model since eventual modification to InGaAs layer properties (in particular its thickness) may not have an impact on the overall simulation results as if this layer was considered "transparent" for what concern electron transport. Further investigations on DHBTs including collector structures with different spacer layers are needed to confirm this hypothesis. The same velocity overshoot can be observed at the junction between the InP and InGaAs layer in the subcollector, where it does not matter.

2.4.2 Frequency simulations

Figure 2.28 shows the comparison between simulated and measured S-parameters for a fixed bias-point at V_{CE} =2 V and I_C =10 mA. The measurement results show data already de-embedded from external pads. The chosen bias point corresponds to the maximum value of f_T as a function of I_C for a single-finger 0.7x5 μm^2 DHBT. The maximum frequency is 110 GHz for both simulation and measurements. From Fig. 2.28-A, it can be seen that all the models pre-

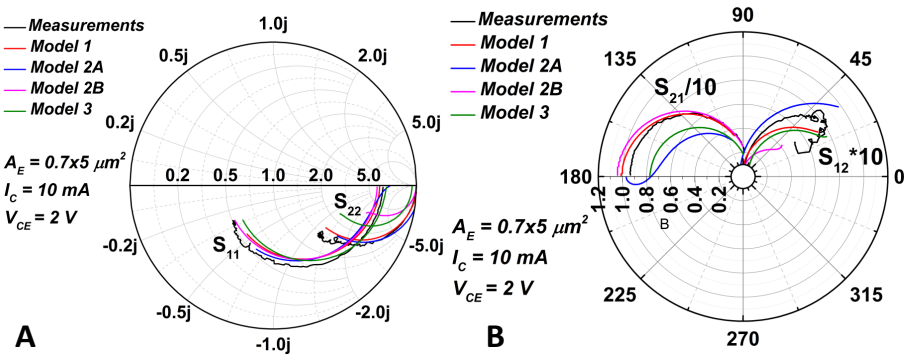

Figure 2.28: Simulation and measurements of S-parameters of a 0.7x5 μm^2 single-finger DHBT. The bias point is V_{CE} =2 V and I_C =10 mA.

dict correctly the parameter S_{11}. The parameter S_{22} is well modeled only by Model 1 and 2A simulations. The S_{22} parameter simulated by Model 2B and Model 3 do not agree with the one extracted from measurements. By comparison with small-signal model extraction and S-parameters simulation in ADS, it is determined that the intrinsic and extrinsic base capacitances C_{bci} and C_{bcx} are underestimated. In particular the values extracted from the simulations are C_{bci}=1 fF and C_{bcx}=1.35 fF. The values extracted from measurements are 2 fF and 5.5 fF for C_{bci} and C_{bcx}, respectively. Fig. 2.28-B shows the comparison concerning simulated and measured S-parameters S_{21} and S_{12}. The data series have been rescaled to fit in the same plot. Model 1 and Model 2B predict properly the S_{21} parameter, although a small-difference exists in the low-frequency range. Model 2A and 3 are definitely underestimating the S_{21} value in terms of magnitude for the whole frequency range. The parameter S_{12} is uncorrectly predicted by all the models with different degree of error and further parameter calibration could not fix it.

Figure 2.29 presents the comparison between simulated and measured f_T and f_{MAX} as a function of collector current I_C . The collector-emitter voltage V_{CE} is fixed at 2 V when I_C is varied. Both for simulation and measurements, the frequency values are extracting by fitting a line with slope -20 dB/decade to the

small-signal current gain h_{21} and to the gain U for f_T and f_{MAX} , respectively at the different bias points.

Model 1 and 2A overstimate both f_T and f_{MAX} value with Model 2A showing

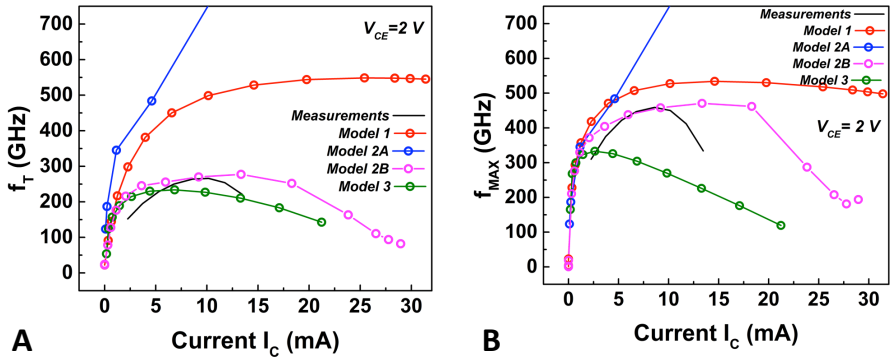

Figure 2.29: Simulation and measurements of f_T and f_{MAX} of a 0.7x5 μm^2 single-finger DHBT as a function of collector current.

additional convergence issues. On the other hand, Model 3 underestimates the measured values. Concerning Model 2B, the simulated values of the peak value of f_T and f_{MAX} is in reasonable agreement with values extracted from measurements with a simulated peak f_T =277 GHz and f_{MAX} = 470 GHz. However the current value for which the maximum occurs is higher than what expected from measurements. The value of the current at which the peak f_T occurs depends on when high-injections effect occur. As it was shown in Sec. 2.4.1 for static results, Model 2B predict a considerably higher value for this critical current. Also, an important difference in the two cases is the rate at which f_T and f_{MAX} decrease as a function of collector current. This deviation is attributed to the inaccurate modeling of high-injection effects. In particular, the effect occurs at bias points corresponding to higher current densities in TCAD simulations with respect to measurement results and the rate of gain degradation as a function of collector current is lower.

2.4.3 Collector optimization

In order to design the DHBT for the PA power cell, the collector structure has been designed to obtain a higher value of f_{MAX} and a higher breakdown voltage to deliver higher output power. The main design parameter in our approach is the thickness of the low doped InP n layer in the collector: by changing its thickness it's possible to obtain different trade-offs between the small-signal base-collector capacitance C_{bc} and the forward collector transit time τ_c that

contributes to the total cutoff frequency f_T . It can be seen that the two parameters are inversely related in the expression of f_{MAX} in Eq. (2.4). However the choice of the thickness has to take into account also the requirements on the desired breakdown voltage and in general of the device SOA. A thicker n^- layer in the collector allows the device to be operated at higher voltage levels and lower operating currents before electrical breakdown occurs but at the same time it degrades the static performance in the knee region. This is because of the increase in collector resistance with thicker n-layer in the collector.
To investigate all these aspects, single finger DHBTs with different epitaxial structures with 130, 190 and 250 nm thick collectors have been fabricated and measured. Each of these structures includes a 80, 140 and 200 nm low doped InP n layer. The devices are compared for the same emitter length of 10 μm . To have a qualitative idea about the static properties of the above mentioned devices, energy band diagrams were computed at the same bias conditions of I_B = 0.36 mA and V_{CE} =1.2 V, as shown in Fig. 2.30. It can be seen that the electron blocking effect in the collector is emphasized for thicker layers as in the case of the 250 nm collector because the voltage drop on the base-collector junction is reduced. This phenomenon is characterized by a less steep profile of the conduction band at the base-collector junction and the physical consequence is an impeded carrier flow that degrades the static performances.

Concerning frequency performance, to estimate the dependence of f_T and

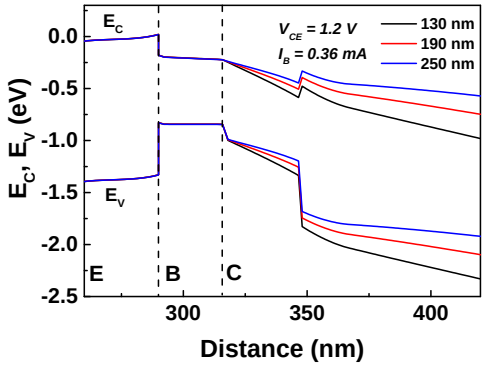

Figure 2.30: Band diagram of 0.7 x 10 μm^2 single finger DHBTs with total collector thickness of 130, 190, 250 nm. The devices are biased at I_B =0.36 mA at V_{CE} =1.2V

f_{MAX} on the thickness of the n^- layer in the collector, Eq. (2.3) and (2.4) can be used by taking into account the dependence on the depletion region width X_d of the base-collector junction of each term. As the emitter and base structure is the same in the considered devices, the terms τ_b, R_e,R_{bi},R_{bx} and C_{je} can be considered constant. The collector transit time is expressed as $\tau_c = X_d/2v_{sat}$, the intrinsic base-collector capacitances $C_{bci} = A_e\epsilon_{InP}/X_d$ and

extrinsic $C_{bcx} = (A_c - A_e)\epsilon_{InP}/X_d$ where A_c is the base-collector junction area. The assumption made in this formula is that the collector is fully depleted for some applied voltage V_{cb} for which X_d=X_c, X_c being the thickness of the n^- layer in the collector. The V_{cb} required to deplete the collector layer increases for higher values of X_d.
TCAD simulations f_T and f_{MAX} for the three different vertical structures were also performed to validate this approach. Figure 2.31 is a comparison of the computed f_T and f_{MAX} as a function of X_d, simulation results and of the measurement of single-finger devices having the corresponding n^- layer thickness. Although a significant deviation exist, it can be seen that both the analytical formula and the TCAD results follow the same trend of the measured devices for what concerns f_T . Regarding f_{MAX} both methods fail to predict the presence of a maximum and thus the decrease observed in measurements when the thickness of the n^- layer is greater than 140 nm. In particular for TCAD simulations, the predicted results for f_T deviates significantly from measurements for the thickness of 80 nm. The main reason is that the constant carrier relaxation times calibrated for a 190 nm collector DHBT are not correct when the thickness is reduced. In addition energy dependent carrier relaxation time should be used to improve accuracy for shorter dimensions. It can be concluded that although TCAD simulations are a valid tool to evaluate device performances for a given epitaxial structure, they are somehow inaccurate in the prediction when sub-micron dimensions are considered for InP/InGaAs DHBT as it is confirmed also by [54]. Concerning static performances, the DHBTs with 250 nm collec-

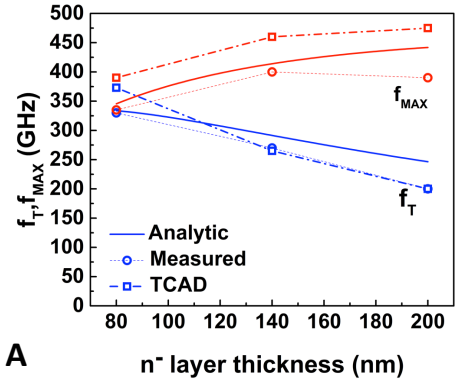

Figure 2.31: Comparison between TCAD simulations, analytical expression and measurements of f_T and f_{MAX} as a function of the InP n^- layer thickness in the collector. It is assumed that the collector is fully depleted so layer thickness is equal to the depletion region width of the base-collector junction.

tor exhibit a higher breakdown voltage of 10 V at I_c=100 μA compared to the other options. The 190 nm collector shows a breakdown voltage around 7.5 V for the same conditions. For what concern f_T/f_{MAX} we obtain 210/390 GHz and

Table 2.7: Summary of static and maximum frequency performances for single-finger 0.7x10 μm^2 with different collector thicknesses.

Collector thickness (nm)	Bias point (I_C ,V_{CE})	f_T (GHz)	f_{MAX} (GHz)	BV_{CE0} @$I_c = 100$ μA (V)
130	30 mA, 1.6 V	330	330	4.5
190	15 mA, 2 V	269	414	7.7
250	15 mA, 2.8 V	210	390	9.8

260/450 GHz for 250 and 190 nm thickness respectively. The bias point for each device is chosen esperimentally to measure the optimum value for f_T and f_{MAX} . To the first order, the difference between the measurements and the analytical results is due to the constant value of v_{sat} used to compute the transit time τ_c. In the analytical formula an average value was considered that overestimates the real carrier velocity profile in the collector region. The measurement results are summarized in Table 2.7.

From these considerations, the 190 nm collector structure is chosen since it allows a good compromise between high breakdown voltage ($BV_{CE0} > 7.5$ V) and high f_{MAX}.

2.5 Conclusions

This chapter presented the optimization steps to choose a single finger DHBT for a mm-wave PA. Different device geometries were compared to choose the most suitable emitter dimensions for further development. In particular, the static and high-frequency characterization of single-finger devices having different emitter width and length was performed. Taking into account the project objectives, from the comparison of the results a 0.7x10 μm^2 emitter DHBT was selected. In order to investigate f_T and f_{MAX} performances of different epitaxial structures a TCAD physical model was implemented and validated against measurements. Although the current model shows a good agreement with measurement results, the limitations of this approach were highlighted. Finally, the performances of different collector epitaxial structure of single-finger DHBTs were investigated in terms of f_T and f_{MAX} . In particular, measurement results were compared with an analytical model and the TCAD model. The chosen collector structure approached the target performances in terms of f_{MAX} and definitely achieved the target breakdown voltage. In the following chapters the next step regarding the parallel combination of single-finger DHBTs in multi-

finger structures will be discussed.

Chapter 3

Multi-finger InP DHBTs for mm-wave Power Amplifiers

Based on the results from electrical characterization, the emitter geometrical dimensions of the single-finger DHBT for the PA power cell were selected. This decision was based mainly on consideration about f_T and f_{MAX} performances and in order to maximize device active area and thus its output power. The increase in device output power is indeed one of the key objectives for the PA unit cell design. For this reason, multi-finger DHBTs are designed in which single-finger devices are combined in parallel in order to increase the total output power. The idea is that this configuration would provide an output power directly proportional to the number of devices (fingers) connected in parallel. In this chapter, firstly the characterization of multi-finger devices will be presented. Then the thermal behavior of these devices will be investigated both by thermal characterization and 3D thermal simulations. Finally a modeling approach will be presented in which the electrical and thermal properties of the DHBTs are combined into a single electro-thermal model.

3.1 Device description

The emitter geometrical dimensions of the single-finger DHBT for the PA power selected in Chapter 2 are $L_E = 10$ μm and $W_E = 0.7$ μm . In order to increase the capability of the device to deliver higher power, multi-finger transistors have been designed. The multi-finger DHBTs consists of several 0.7x10 μm^2 unit fingers physically placed one next to the other with the same orientation as shown in Fig. 3.1. The devices maintain separate mesas and contacts but share

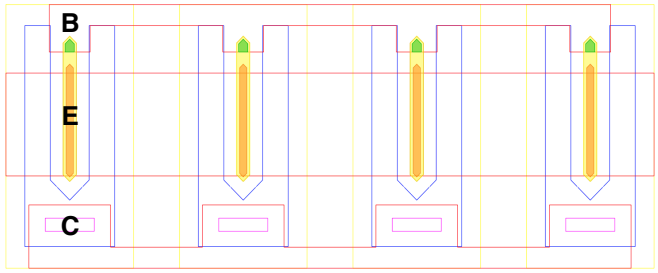

Figure 3.1: Layout schema of a 4-finger DHBT with 0.7x10 μm^2 emitter area unit fingers. The unit fingers share the same emitter, base and collector interconnection lines but have separated collector mesas.

the same interconnection metal. The multi-finger devices investigated in this work and presented in the following sections have a number of finger between 1 and 8. Based on studies on previous generations of devices [55], the inter-finger spacing considered between the center of two adjacent emitters is 17 μm to reduce mutual heating effect.

3.2 Characterization of multi-finger DHBTs

In this section the electrical performances of multi-finger devices are presented. Following the same process as in Chapter 2 Gummel plots, I-V curves and device SOAs are introduced.

3.2.1 DC measurements

Figure 3.2 presents the Gummel plots of multi-finger devices having from 1 to 8 fingers and single-finger emitter area of 0.7x10 μm^2 . The measurements are taken at the same conditions as for single-finger devices by sweeping the V_{BE}

Table 3.1: Effective area taking into account underetching for single-finger DHBT with L_E equal to 5, 7, 10 μm and W_E = 0.7 μm .

Emitter length (μm) $\mathbf{W_E = 0.7}$ μm	A_{Eff} (μm^2)
5	2.8
7	3.9
10	6

voltage from 0 to 0.95 V and keeping the V_{BC} voltage equal to to 0 V. The results are normalized to device active area computed as fingers $\times$ A_{Eff}, where A_{Eff} is the effective device area taking into account underetching beneath the emitter contact.The values of A_{Eff} are reported in Tab. 3.1 for single-finger devices. The curves are superposed for large part of the V_{BE} range and the

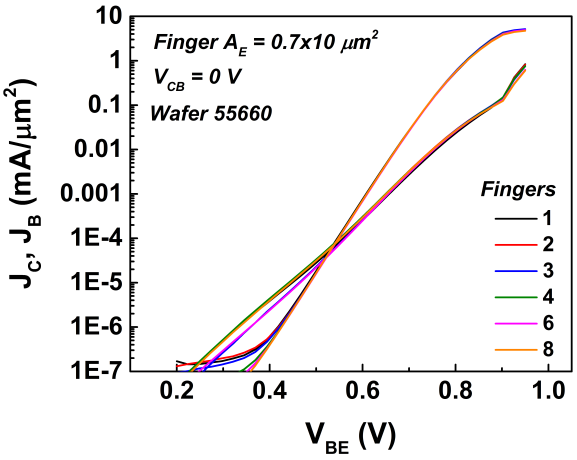

Figure 3.2: Gummel plot of multi-finger devices from 1 to 8 finger. The unit finger emitter area is 0.7x10 μm^2 . Collector and base current are normalized to device active area.

main differences emerge at high current-injection levels for $V_{BE} > 0.85$ V. In Fig. 3.2 it can be seen that for increasing number of fingers the base current density reaches lower values for the same V_{BE} voltage. The collector current density instead is basically not affected by the increase in number of finger. The forward β as a function of V_{BE} is shown in Fig. 3.3 for the multi-finger DHBTs of Fig. 3.2. Fig. 3.3 shows that the static gain as a function of V_{BE} is not affected by the increasing number of finger concerning both peak value and roll-off current density. Figure 3.4 shows the output I-V curves corresponding to the devices of Fig. 3.2. The collector current is measured as a function of V_{CE} with different bias currents I_B applied to the base. In order to compare the

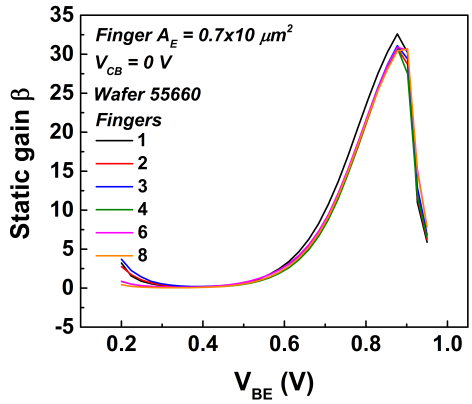

Figure 3.3: Static forward gain of multi-finger devices from 1 to 8 finger. The unit finger emitter area is 0.7x10 μm^2 .

different geometries, I_C and I_B are normalized to device active area. The base current density I_B is swept from 0 to 0.135 mA/μm^2 with a 0.027 mA/μm^2 step. The comparison of the I-V curves in Fig. 3.4 highlights an effect occurring with increasing number of fingers related to the decrease of the slope of J_C vs. V_{CE} in the saturation region. This might be due to self and mutual-heating effects consequences, becoming more evident at higher current levels.
In order to investigate the temperature dependence of device performances for higher number of fingers the static forward gain β and the I-V curves for 6 and 8-finger devices at different temperature values are shown in Fig. 3.5 and Fig. 3.6 respectively. The devices are measured on a hot plate with temperature control and it is assumed that the junction temperature reaches the same value of the chuck temperature in equilibrium. The static gain of Fig. 3.5 A and B has been calculated from Gummel plot measurements at 30°, 50° and 80° and it is shown as a function of collector current I_C . The applied voltage V_{BE} is the same for the two devices at all temperature ranging from 0 up to 0.95 V. For both devices it can be seen that β is not strongly dependent on temperature for most of the I_C range and differences emerge only at high current levels. In particular, Fig. 3.5 A and B show that for the same range of V_{BE} the devices reach higher current levels due to emitter-base junction temperature increase. Fig. 3.6 shows the output I-V curves at different temperatures for the devices of Fig. 3.5. The collector current is affected by the increase in temperature only for high-current levels.

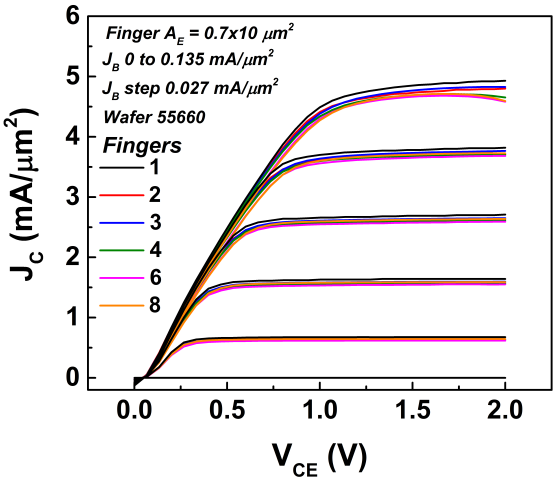

Figure 3.4: Output I_C -V_{CE} curves of multi-finger devices from 1 to 8 finger. The unit finger emitter area is 0.7x10 μm^2 . Collector current is normalized to device active area. Base current density is swept from 0 to 0.135 mA/μm^2 with a 0.027 mA/μm^2 step.

3.2.2 High frequency measurements

This section presents the high-frequency measurement results for multi-finger DHBTs. The number of fingers varies from 1 to 8. Unit fingers have emitter length L_E equal to 5, 7 and 10 μm and emitter width $W_E = 0.7$ μm . Similarly to single-finger devices, for each multi-finger DHBT S-parameters measurements are carried out up to 110 GHz at different current values with $V_{CE} = 2$ V. On-wafer structures are employed to de-embed the contribution of parasitics due to contact pads for each multi-finger device.

Figure 3.7 show the extraction of f_T as a function of current density J_C for multi-finger devices with emitter area 0.7x10 μm^2 . The devices are biased with $V_{CE} = 2$ V. The trend of the peak f_T of Fig. 3.7-A reflect the values already shown in Fig. 3.8 with f_{MAX} decreasing by 25% from a single-finger to an 8-finger device. In addition, the reduction of $J_{C\ max(f_T)}$ with increasing number of fingers can be noticed from Fig 3.7-A. In particular, $J_{C\ max(f_T)} \approx 3.7$ mA/μm^2 for a single-finger device while it's only equal to 1.8 mA/μm^2 for a 8-finger device. If the current was equally distributed among all the fingers, the peak f_T value would be expected to occur at the same current density for any number of finger. Since this does not happen, it can be concluded that the current is not conducted uniformly through the device but some fingers have higher current densities and incur already in Kirk-like effects. The same effect can be observed in a lesser way for what concern f_{MAX} as shown in Fig. 3.7-B. In this case, $J_{C\ max(f_{MAX})} = 1.8$ mA/μm^2 for a single-finger device while it drops to 1.6 mA/μm^2

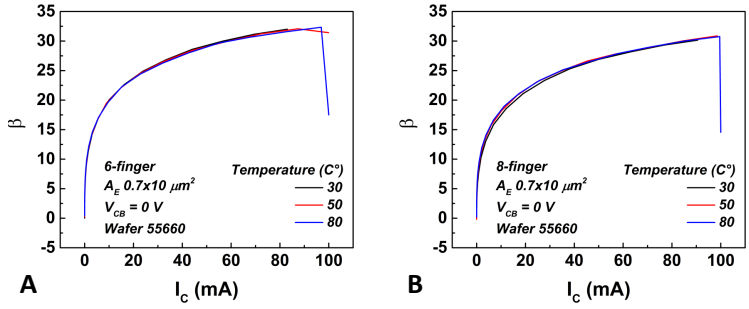

Figure 3.5: Static forward gain as a function of collector current I_C of multi-finger devices with A) 6 and B) 8 fingers measured at different temperature values. The unit finger emitter area is 0.7x10 μm^2 .

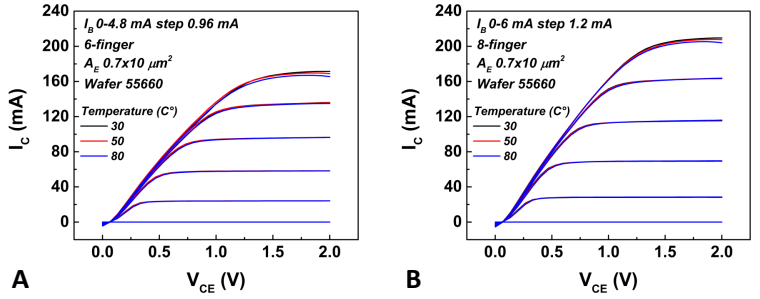

Figure 3.6: I-V output curves for 6 and 8 finger devices at different temperature values.

for a 8-finger device. Figure 3.8-B presents the results for the extracted cutoff frequency f_T as a function of emitter length for different number of fingers. The values reported in Fig. 3.8 refers to the peak f_T values that occur at different current densities as a function of device total active area. The current density value at which a device attains peak f_T for a given V_{CE} is referred to as $J_{C\ max(f_T)}$ (the corresponding current value is $I_{C\ max(f_T)}$). From Fig. 3.8 it can be seen that cutoff frequency f_T presents a 10% maximum decrease with increasing emitter length for a given number of finger. f_T does not depend strongly on emitter length, at least for small number of fingers. However, f_T peak values decrease as the number of fingers increases, going from 250 GHz for single and 2-finger DHBTs down to 240 GHz for an 8 finger device with L_E =10 μm . This effect can be explained in part by a junction temperature increase with increasing number of fingers that might be responsible of a reduced average carrier velocity leading to an increased base-collector transit time τ_{cb}.
Fig. 3.8-B shows the extraction of f_{MAX} peak values as a function of emitter length. In this case, the peak values correspond to different current density values $J_{C\ max(f_{MAX})}$ (and current $I_{C\ max(f_{MAX})}$) defined analogously to the f_T case. Contrary to what emerged for f_T , Fig. 3.8-B highlights the degradation of the

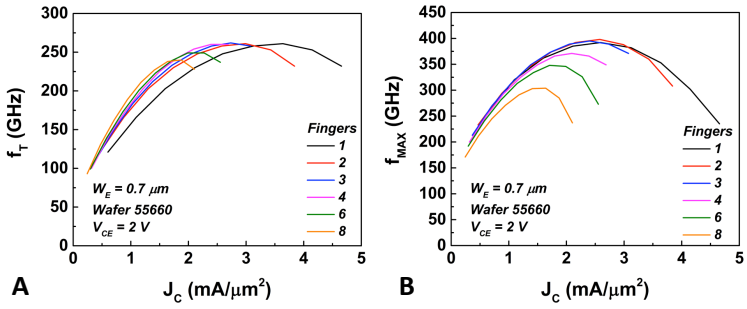

Figure 3.7: A) f_T and B) f_{MAX} vs. J_C for multi-finger devices with emitter area 0.7x10 μm^2 and 1 to 8 fingers.

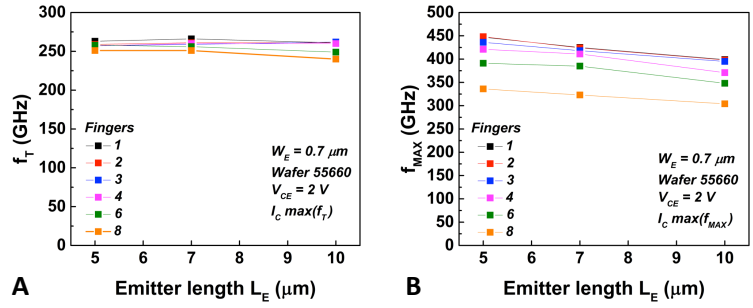

Figure 3.8: Peak values for A) f_T and B) f_{MAX} as a function of emitter length L_E for different number of fingers. The emitter width is 0.7 μm . Devices are biased at V_{CE} = 2 V.

peak value of maximum oscillating frequency with increasing emitter length for any number of finger. In addition, f_{MAX} steadily decreases when the number of fingers goes from 2 to 8. The peak value reported for a single-finger DHBT is approximately 450 GHz for $L_E = 5$ μm ; f_{MAX} drops by 24% to 338 GHz for 8-finger DHBTs having the same L_E . Two concurrent effects can explain this tendency affecting the numerator and denominator of Eq. (2.4). The first reason is the decrease of f_T with higher junction temperatures as already mentioned above. The second effect is the presence of unwanted parasitics related to inter-finger capacitances and external metal access lines impedance that become relevant with a high number of fingers.

In order to choose the most suitable number of finger in the range 1-8 for the power-cell DHBT, a trade-off is needed between the increase in output power and the consequent frequency performance degradation for every additional finger. Firstly, the 8-finger DHBT is discarded because f_{MAX} =296 GHz is considered not sufficient for the targeted PA designs. In addition, if the simplifying as-

sumption is made that the output power increases linearly with the number of finger, it can be seen from Fig. 3.7 that a number of finger greater than 3 is a convenient tradeoff as for example between a 2- and a 4-finger the f_{MAX} is degraded by about 10% with an expected 100% increase in power. The choice between 4 and 6 fingers is less evident as in this case the frequency drops of less than 10% for a 50% increase in output power thus a 6-finger DHBTs would be a good solution. However, considering Fig. 3.7, in a 6-finger device the degradation of f_T and f_{MAX} occurs at much lower J_C compared to a 4-finger device thus providing less output power overall. The decision has to take into account also circuit design considerations. Firstly, as the final design involves multiple power-cells combined in parallel limitations arise concerning available layout space and impedance matching. In particular, the impedance matching of 6-finger DHBT at the frequency of interest requires lossier networks with respect to a 4-finger with a consequent loss of RF power that eliminates the benefits of the additional fingers. In addition, as it will be discussed in the Section 3.2.3, the use of ballasting resistors to limit thermal effects in multi-finger device would increase excessively the layout space taken by a 6-finger transistor. Based on these consideration about static and high-frequency resuls for multi-finger devices a 4-finger DHBT with emitter area 0.7x10 μm^2 is considered the most promising candidate for the PA unit cell. In the following, the limits of the device operating region and its thermal behaviour will be further investigated.

3.2.3 Safe Operating Area analysis

The SOA is defined as the range of output voltages and currents for which the device can be operated reliably without incurring in breakdown [56]. It is related to the total swing of output collector voltage available during device static operation at a given current. From the PA design perspective, a wide SOA is desirable for improved performances. One figure of merit related to SOA measurements is common-emitter breakdown voltage BV_{CEO} at zero base current. Concerning SOA measurements, BV_{CEO} is considered in this work as the V_{CE} value for which the collector current I_C increases to 100 μA when no I_B is applied. In order to reach higher values of BV_{CEO} , materials with higher energy gap are used [57][58] [59]. When the collector material has a wide energy bandgap, the accelerated electrons will need higher energies to create additional electron-hole pairs that trigger the avalanche breakdown mechanism. InP/InGaAs DHBTs can provide a high value of BV_{CEO} thanks to the larger bandgap and the low doped InP collector with respect to a SHBT. In addition, composite structures can be designed to further improve the SOA of the device [60]. The two main concurring mechanism in device breakdown and SOA limitation are impact ionization and thermal effects. In particular for multi-finger devices, thermal effects become relevant at higher current values when the heat

generated from each finger has an impact on adjacent fingers. It is worth stating that only the SOA during static device operation is considered in this work. During RF operation the device might exceed the boundaries of the SOA according to dynamic thermal properties and applied signal frequency [61].
In order to show the impact of the instabilities triggered by self and mutual heating on device SOA in multi-finger devices, single and multi-finger devices can be compared.
Figure 3.9 shows the SOA measurements for devices with 0.7x10 μm^2 emitter and 1, 2 and 4 fingers. The current I_C is normalized to the effective emitter area in order to compare the devices at the same collector current density J_C . The measurements were performed by biasing the devices at a constant I_B and then sweeping the collector-emitter voltage V_{CE} until the I_C current deviates from the flat value of the linear region and enter the breakdown zone and is eventually destroyed. For the sake of comparison, the I_B values are proportional to device total active area. From the inspection of the lower part of Fig.3.9 up

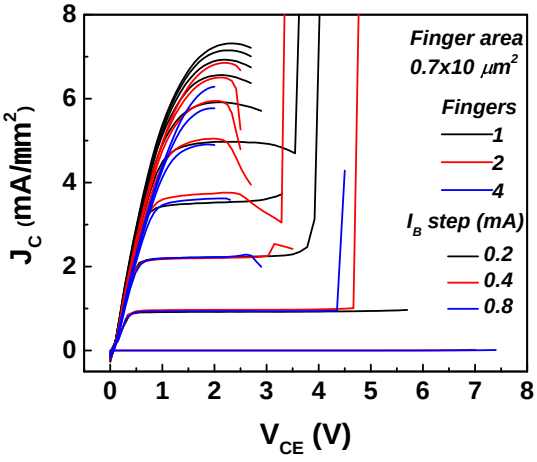

Figure 3.9: SOA comparison of multi-finger devices with 1-2-4 fingers and 0.7x10 μm^2 emitter area.

to $J_C = 1$ mA/μm^2 , it can be seen that when the three devices are operated at low current levels they can sustain higher operating voltage. In this operating range, even if thermal instabilities occur due to high dissipated powers, the consequences of an even current distribution among the finger is less severe due to the lower collector current levels. Also, at $J_C = 1$ mA/μm^2 the destruction points for 2 and 4 finger devices are quite similar while the single-finger DHBT can be operated at higher V_{CE} voltage. When the current I_B is increased and the upper part of Fig.3.9 it is clear that both multi-finger devices break at lower V_{CE} than a single-finger device, with the 4-finger breaking down earlier than a 2-finger. Thus it can be concluded that the SOA is degraded at higher collec-

tor current densities for multi-finger devices. Although the physical mechanism causing device failure remain probably the same, this behavior can be explained by the occurrence of additional mutual heating effects in multi-finger devices that cause an uneven current distribution among the fingers and a premature breakdown in the fingers carrying more current [62].
As it was shown, the thermal properties of multi-finger devices have important consequences on device static and frequency performance. In the following sections these issues will be further investigated from the experimental and simulation point of view.

3.3 Thermal behavior of multi-finger DHBTs

3.3.1 Characterization

Methodology

Multi-finger DHBTs are normally operated at higher power dissipation levels and, as it has been shown earlier in this chapter, the additional heat generation degrades the overall device performances and characteristics. Thermal properties of the devices are to be determined to deal with self-heating and additional effects such as thermal coupling between the fingers.
The results in this section present a comparison of the impact of the different geometrical parameters on device electrical and thermal characteristics. The multi-finger DHBTs investigated in this section have from 1 to 8 fingers. The unit fingers have emitter width $W_E = 0.7$ μm and different emitter lengths L_E of 5, 7, 10 μm .
The thermal characteristics of the devices were extracted using a method based on [63] and the results on the same technology are reported in [64] for single and multi-finger transistors.
InP DHBT exhibits the property, as does any bipolar junction transistor, that the base-emitter voltage V_{BE} required to reach a defined current density J_C , decreases at higher junction temperatures. The thermal-electric feedback coefficient ϕ takes this effects into account and is defined as

$$\phi = -\frac{\partial V_{be}}{\partial T} = \frac{\beta^*}{q} - \frac{\eta k}{q} \ln \frac{I_C}{I_{s_0}} \tag{3.1}$$

where β^* is the band gap shrinking coefficient, η is the ideality factor and I_{S_0} is the saturation current at room temperature.
Based on the approach from [63], the ϕ coefficient was computed from I_C vs. V_{BE}

measurements on a single finger transistor with emitter area 0.7x5 μm^2 . Figure 3.10 shows measured collector current I_C plotted as a function of base emitter voltage V_{BE} at different temperature values. Measurements were performed at temperature T equal to 20°, 30°, 40°, 50°, 60°, 70°, 80° C. In Fig. 3.10 the dis-

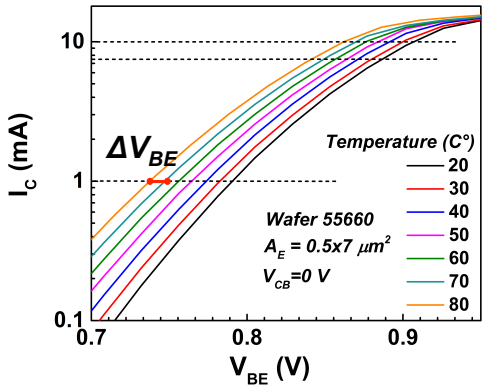

Figure 3.10: Collector current I_C as a function of the number of V_{BE} at different temperatures for a single finger DHBT with emitter area 0.7x5 μm^2 .

placement of the I_C curves towards lower V_{BE} voltage values when temperature increases can be observed. Fixing a current value, the corresponding V_{BE} can be extracted for each temperature value. In particular, three current values are shown in Fig. 3.10 corresponding to 1, 7.5 and 10 mA. For each current level, the corresponding variation in V_{BE} as a function of temperature was extracted from the plot of Fig. 3.10.

The extracted V_{BE} values can be plotted against temperature in order to obtain the V_{BE} vs. T relationship. The results are shown in Fig. 3.11 for the three current levels above mentioned. From Fig. 3.11 it can be seen that the required V_{BE} voltage to provide a given current density decreases with increasing temperature. By fitting the data points for each current level, the coefficient ϕ is equal to the slope of the fitting straight line with the opposite sign. Figure 3.11 shows also that the slope of the fitting line, and thus the value of the ϕ coefficient, depend on the current value at which they are computed. This can be explained by looking at Fig. 3.10 where it is highlighted that the value of ΔV_{BE} decreases at higher current levels. In this work, the electrical-thermal coefficient ϕ is computed at a current level of 10 mA for a single finger device with emitter dimension 0.7x5 μm^2 as this corresponds to the peak f_T for this device. In addition, ϕ is assumed constant across the wafer and the same value is employed in the case of single and multi-finger devices.

The coefficient ϕ is then used to extract a critical parameter used to describe transistor static thermal properties: the self-heating thermal resistance R_{TH} . As power dissipation increases at high current densities, a large value of thermal

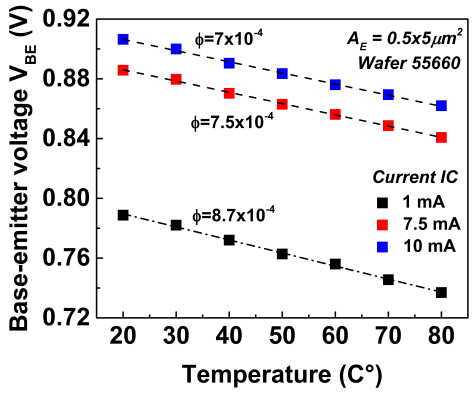

Figure 3.11: Base-emitter voltage V_{BE} data points as a function of temperature T at different collector currents. Data points are fitted with a straight line whose slope is the inverse of the electric feedback coefficient ϕ

resistance is responsible for high increase in junction temperature: this in turn leads to variations in other device parameters and to a potential failure. For a multi-finger device an additional mutual thermal resistance exists among the fingers. Total thermal resistance values for single and multi-finger devices were computed according to:

$$R_{TH} = \frac{\Delta V_{BE}}{\Delta P \phi} = \frac{\Delta V_{BE}}{\Delta V_{CE} I_C \phi} \tag{3.2}$$

In the case of multi-finger transistors, the result from Eq. (3.2) represents a total thermal resistance that includes mutual heating effects among the fingers. For the DHBTs in this work, thermal resistance values were determined from measurements as follows. For every device, first collector current I_C was measured as a function of V_{BE} at different collector-emitter voltage V_{CE} ranging from 0.9 to 2.1 V. For a given I_C value, the variation in base-emitter voltage ΔV_{BE} as the distance between the curves, as shown in Fig.3.12. The increase in dissipated power is constant between each curve and equal to $\Delta P = \Delta V_{CE} \times I_C$. Inserting ΔV_{BE} , the coefficient ϕ and ΔP in Eq. 3.2 allows to compute thermal resistance values for each transistor for different values of dissipated power.

Results

Figure 3.13 presents the value of thermal resistance R_{TH} extracted from electrical measurements following the procedure illustrated in the previous section. The devices have 1 to 8 fingers and emitter width $W_E = 0.7$ μm . The emitter length L_E is equal to 5, 7, 10 μm . For the sake of comparison among devices

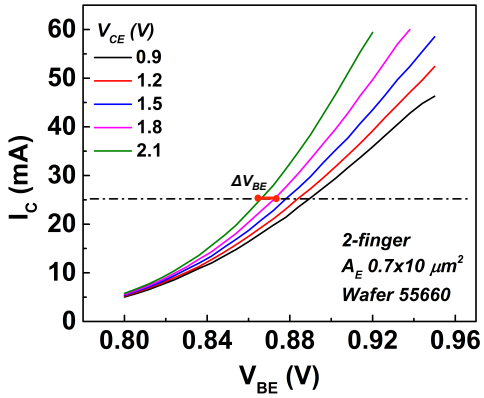

Figure 3.12: Measured collector current I_C as a function of V_{BE} for a 2-finger device of area $2 \times 10 \times 0.7 \mu m^2$. The horizontal line represents a given current value at which ΔV_{BE} is extracted as the difference between two adjacent curves.

having different dimensions and number of fingers (and thus different active areas) the results are normalized to device active area. R_{TH} is then extracted at the same current density for all the DHBTs. The current density at the extraction point is J_C =2.8 mA/μm^2 and V_{CE} =2 V. Thermal resistance varies

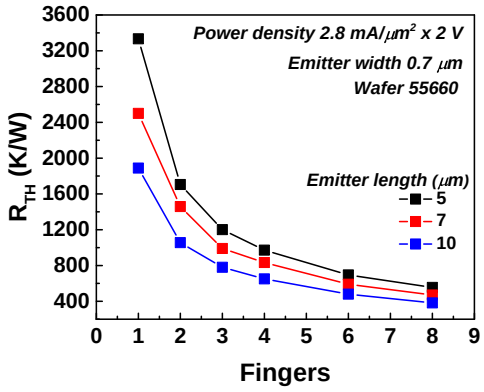

Figure 3.13: Thermal resistance R_{TH} as a function of the number of fingers for 5, 7, 10 μm emitter lengths. R_{TH} was computed at a constant power density with J_C =2.8 mA/μm^2 and V_{CE} = 2 V

non-linearly with the number of fingers and ranges from 3300 to 1900 C°/W for single finger devices when the L_E varies from 5 to 10 μm . The difference is evident for low number of fingers while it tends to be reduced when the number of fingers increases, independently by the emitter length. Starting from thermal resistance at a constant power density, specific thermal resistance for unit area is computed and results are presented in Fig. 3.14. The specific thermal resistance

is calculated by multiplying the thermal resistance value for each device by the corresponding active area. From Fig. 3.14 it can be seen that while having

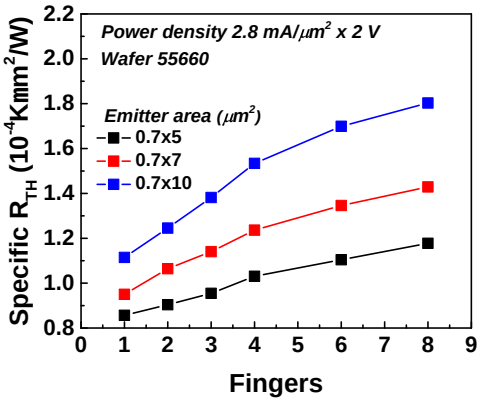

Figure 3.14: Specific thermal resistance R_{TH} as a function of the number of fingers for 5,7,10 μm emitter lengths. R_{TH} was computed at a constant power density with J_C =2.8 mA/μm^2 and V_{CE} = 2 V

higher thermal resistance, devices with L_E =5 μm have the lowest specific thermal resistance. This indicate that heat conduction through the surroundings is better managed by shorter devices. Since the collector mesa width is the same for devices with L_E equal to 5 or 10 μm , this suggests that a lower ratio of emitter/collector mesa might improve heat management. Another hypothesis is the different heat distribution across the finger for devices with different emitter lengths: devices with longer emitter might have a larger specific R_{TH} because of a higher localized increase in temperature for a constant power density. This point needs however further investigation by comparing different structures and possibly using 3D TCAD simulations. Specific R_{TH} increases with the number of finger and a possible reason is the contribution of additional mutual heating effects to the total increase in device temperature.

The extraction of thermal resistance from electrical measurement gives important information about the thermal properties of single and multi-finger devices. However, concerning multi-finger DHBTs, the extracted value is based on an approximation of the device average temperature. In addition, the method described above does not allow to have information about the mutual coupling between the fingers. This information could be obtained experimentally by using specific measurement structures designed to have electrical access to individual fingers in a multi-finger configuration. This solution requires the design of several of these structures each time a new structure has to be investigated thus consuming time and wafer space. In the next sections, an approach based on 3D thermal simulations is pursued to further investigate the thermal properties of multi-finger DHBTs.

3.3.2 3D thermal simulations

Methodology

The thermal behavior of multi-finger devices has been investigated using the FEM software COMSOL. The software solves the heat-equation across a 3D domain including the multi-finger DHBT and the substrate. The 3D structure of single and multi-finger devices of up to 8 fingers was reproduced starting from the epitaxial structure and layout data. The devices were incapsulated in a polyimide dielectric layer. Metal contacts were initially included in the simulated structures to take into account dissipation through the metal layers, as shown in Fig. 3.15. However the simulated results differed only slightly in comparison to simulated structures that included semiconductor layers only. Since the difficulties concerning structure meshing increase significantly, it was chosen to neglect the influence of the metal contacts being aware that this leads to more conservative results.

The full structure was assumed to be initially in equilibrium at room tempera-

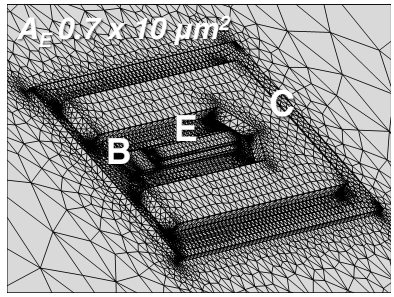

Figure 3.15: Meshed 3D structure of a single-finger DHBT with 0.7x10 $\mu\mathrm{m}^2$ including metallization.

ture namely at T_0=300 K. The simulations were carried out considering material parameters constant as a first approximation and then by taking into account the temperature dependence of thermal conductivity k [65] [66] according to:

$$k = k_{300} \frac{T_L}{T_0}^{\alpha_k} \tag{3.3}$$

Table 3.2 lists the thermal conductivity for each material used for the 3D solution of stationary heat-equation. Concerning the boundary conditions the heat sink of the structure is placed at the bottom of the substrate layer and all the system boundaries are considered adiabatic. Usually the heat generated by the device is considered to occur at the base-collector junction and to a lesser extent in the base-emitter junction [67][68]. This is expressed later on in Eq. 3.6. Thus, two constant boundary heat sources were defined for each finger in the simulations at

Table 3.2: Material parameters for thermal simulation

	Thermal conductivity k_{300} (W/m·K)	α_k
InP	68	-1.4
InGaAs	5	-1.25
Polyimide	0.12	

the emitter-base interface and at the base-collector junction. A dissipated power density was associated with each source according to Eq. 3.6 and normalizing by the effective emitter area. This approach is a first order approximation that does not take into account lateral heat distribution effects internal to the device. In addition, a coupled electro-thermal model would provide a much more accurate estimation of the generated heat power due to a given bias condition. However the additional computational and modeling efforts were traded-off retaining a reasonable estimation error.

Results

From the results of the thermal simulations the temperature distribution across the 3D structure is obtained including the surface temperature and the depth of the heat spreading towards the substrate as shown in Fig. 3.16 for the case of a 4-finger device. The geometrical center of each finger is the point that heats

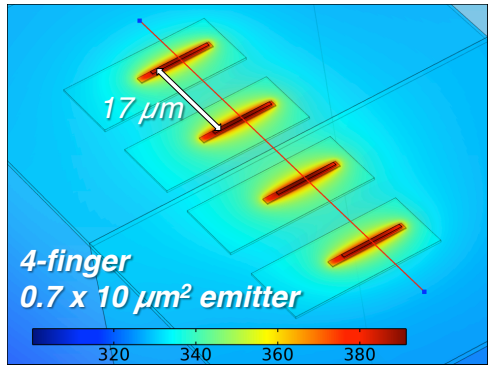

Figure 3.16: 3D temperature distribution of a 4-finger InP DHBT simulated at 30 mW/finger. In red, the cutline used to compute the 1D temperature profile along the structure.

up the most under a constant power excitation. Fig. 3.17 shows the 1D surface temperature profile along a cut line perpendicular to the fingers and passing for the center of each finger (Fig. 3.16) for the devices simulated at a constant power

density of $P = 30$ mW/finger. It is implicitly assumed that the temperature at the surface of the finger is the same as the one in the layer where the power source is set and the 3D temperature distribution along the vertical direction confirms that this is a valid assumption. The temperature profile shown in Fig. 3.17 can be used to compute important devices properties as the self-heating thermal resistance R_{th} and the mutual thermal resistance $R_{th_{ij}}$ between finger i and j according to Eq. 3.5. In the case of multi-finger devices the peak temperature is not uniform between the fingers as the central ones are heated up more by the surroundings in comparison to the peripheral fingers. The value of ΔT used to compute the corresponding thermal resistance of the ensemble is the average of the peak temperatures of the different fingers. However also in the case of the R_{th} value for multi-finger devices extracted from measurements we still deal with an averaged value as we do not have access to the individual current of each finger but only on their sum. Finally, the corresponding heating power P is the sum of the applied heat sources that in this case is simply P times the number of fingers.

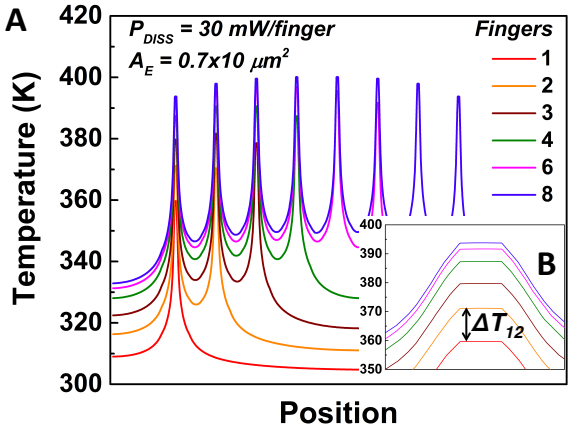

Figure 3.17: Temperature profile of multi-finger devices from 1 to 4 fingers simulated at P=30 mW/finger.

Fig. 3.18 shows the comparison between the thermal resistance of single and multi-finger DHBTs extracted from electrical measurements and the values computed from thermal simulations including both constant and temperature dependent material parameters. The electrical measurements were performed at collector current and collector-emitter voltage corresponding to 30 mW/finger and the same power was considered as a constant boundary heat source for the simulations. The graph shows a good comparison between measured and simulated values: the highest difference is observed for single finger devices where the simulated thermal resistance differs from the measured value by about 5%. This difference decreases with a larger number of fingers as the uncertainties related to the measurement method and the simulations are averaged out. It

can also be observed that including the temperature dependence of material parameters in the simulation leads to a slight overestimation in comparison to measured values. This difference is probably partly compensated by the fact that dissipation in the upward vertical dimension through metal contacts is not taken into account in these simulations.

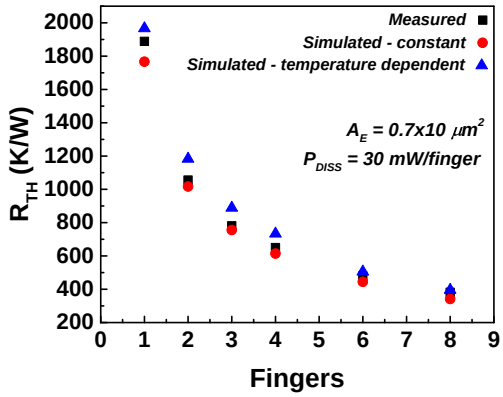

Figure 3.18: Comparison of measured and thermally simulated R_{TH} for devices from 1 to 4 fingers at 30 mW/finger. Simulations are compared considering constant (red circle) and temperature dependent material parameters (blue triangle).

Parameters for electro-thermal model

In this approach the temperature rise in a given finger is given as the sum of the power generated in that finger multiplied by its thermal self-resistance and the power generated in all other fingers multiplied by their respective thermal coupling resistances [69]. Mathematically this can be written as:

$$\begin{aligned} \Delta T_{Q1} &= P_1 R_{11} + P_2 R_{12} + ... + P_m R_{1m} \\ \Delta T_{Q2} &= P_1 R_{21} + P_2 R_{22} + ... + P_m R_{1m} \\ \Delta T_{Qm} &= P_1 R_{m1} + P_2 R_{m2} + ... + P_m R_{mm} \end{aligned} \tag{3.4}$$

where the influence from the thermal capacitors are omitted for simplicity (static case). From Eq. 3.4 the thermal resistance matrix is defined as:

$$R_{TH} = \begin{pmatrix} R_{11} & \cdots & R_{1m} \\ \vdots & \ddots & \vdots \\ R_{m1} & \cdots & R_{mm} \end{pmatrix} \text{ where } R_{ij} = \left.\frac{\Delta T_i}{P_j}\right|_{i\in[1...m], P_{i\neq j}=0} \tag{3.5}$$

The power dissipated by each finger i P_i in Eqs. 3.4-3.5 is defined as:

$$P_i = I_{Ei} V_{BE} + I_{Ci} V_{BC} \tag{3.6}$$

In the case of a 4-finger device we have for example at $P = 30$ mW/finger:

$$R_{th} = \begin{pmatrix} 1990 & 382 & 285 & 262 \\ 382 & 1990 & 382 & 285 \\ 285 & 382 & 1990 & 382 \\ 262 & 285 & 382 & 1990 \end{pmatrix}$$

To better model the thermal properties of the DHBTs it's important to consider the nonlinearities associated to the temperature dependence of the heat propagation equation and of the material parameters such as the thermal conductivity as described by Eq. 3.3. Transistors structures with 1 to 4 fingers were thus simulated at different power levels from 15 to 75 mW/finger. Figure 3.19 shows

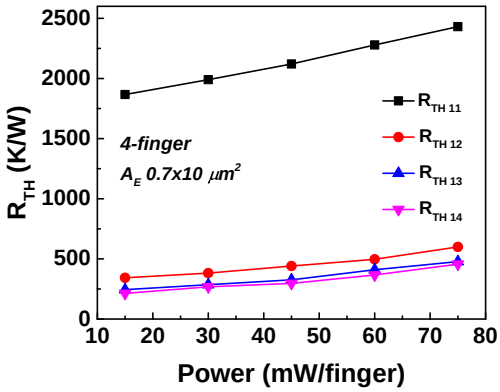

Figure 3.19: Thermal resistance matrix parameters

the evolution of the terms of the thermal resistance matrix as a function of the dissipated power per finger in the case of a 4-finger device. The self-heating terms R_{th11} increases by roughly 30% from 1866 K/W at 15 mW/finger up to 2430 at 75 mW/finger. All the other mutual heating terms approximately double in the same range of dissipated power. A 2nd order polynomial fit was applied to these results to model the dependence on dissipated power of the terms of the thermal resistance matrix. The elements of the first row of the R_{th} matrix are expressed as:

$$\begin{aligned} R_{th_{11}} &= 27407 \cdot P_1^2 + 6975 \cdot P_1 + 1755 \\ R_{th_{12}} &= 39563 \cdot P_2^2 + 633.14 \cdot P_2 + 326.01 \\ R_{th_{13}} &= 30547 \cdot P_3^2 + 1193 \cdot P_3 + 219.16 \\ R_{th_{14}} &= 35605 \cdot P_4^2 + 692.89 \cdot P_4 + 200.7 \end{aligned} \tag{3.7}$$

To include the terms of the thermal resistance matrix in the model, 3D thermal simulations were performed on single and multi-finger devices. The results were then compared with thermal resistance values extracted from electrical measurements.

Inter-finger spacing

As already mentioned, the emitter-to-emitter distance in the multi-finger DHBTs discussed so far is 17 μm. Since the self and mutual heating properties of multi-finger devices depend in part on their layout geometrical dimensions, it is worth to examine the influence of inter-finger spacing. In particular, an increase of finger spacing can be thought as a solution to improve device thermal resistance by reducing mutual heating. The simulation approach described in the previous section can be used to further investigate this issue. 3D thermal simulations of 2-finger devices with 0.7x10 μm^2 emitter are performed for different values of finger spacing from 13 to 26 μm. The minimum distance is defined by the limit of proximity of the collector mesas of the two devices. The power density applied to the device is equal to 30 mW/finger. Figure 3.20, shows the simulated 1D temperature profile along the center of the two emitters for each value of finger spacing. Qualitatively, it is immediately evident that when the two finger are placed more closely the average temperature of the device increases. In the case of a 26 μm spacing the average device temperature is 368 K and it increases to 373 K for a 13 μm spacing. Using the approach described in Sec. 3.16, the

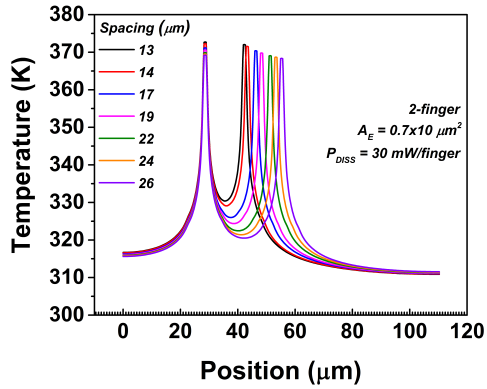

Figure 3.20: Temperature profile from 3D simulations of a 2-finger DHBTs with different inter-finger spacing. The finger emitter area is 0.7x10 μm^2 . The applied power density is 30 mW/finger.

change in self and mutual heating can be quantified by looking at the relative increase in temperature for each spacing value. By definition, the self-heating thermal resistance $R_{TH_{11}}$ is:

$$R_{TH_{11}} = \frac{\overline{\Delta T}}{\sum_j P_j} \tag{3.8}$$

where $\overline{\Delta T}$ is the average value of the peak values from the simulated temperature profiles for multi-finger devices and P_j is the dissipated power in each finger.

The computation of the mutual heating term $R_{TH_{12}}$ is based on the definition:

$$R_{TH_{12}} = \frac{\Delta T_1}{P_2} \tag{3.9}$$

where ΔT_1 is the increase in the peak temperature of Finger 1 when P_2 is applied to Finger 2. The value of ΔT_1 can be computed from the temperature profiles shown in Fig. 3.20 obtained from 3D thermal simulations. The reference value T_0 used to compute the temperature increase is the peak temperature of a single-finger at the considered dissipated power: this corresponds to a case when a second finger is placed at an infinite distance and mutual heating is negligible. From simulation results $T_0 = 359$ K for a 0.7x10 μm^2 DHBT at 30 mW. Thus $\Delta T_1 = T_X - T_0$, where T_X is the peak temperature value of Finger 1 for each value of spacing.
Figure 3.21 shows the computed value for the self-heating term $R_{TH\ 11}$ and the mutual heating term $R_{TH\ 12}$ as a function of inter-finger spacing. In the

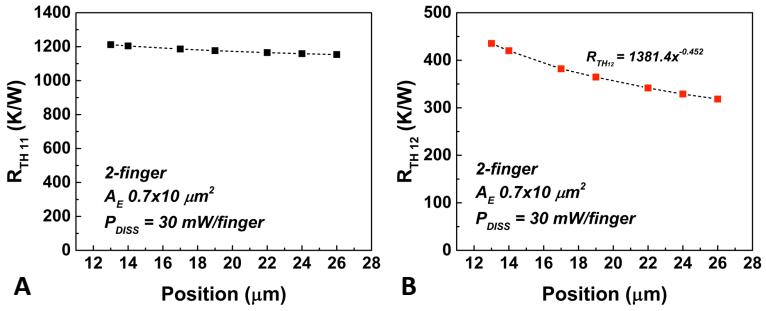

Figure 3.21: Coefficient $R_{TH\ 11}$ A) and $R_{TH\ 12}$ B) as a function of inter-finger spacing for a 2-finger DHBT with emitter area 0.7x10 μm^2 . The dissipated power density is 30 mW/finger.

considered devices, the thermal resistance $R_{TH\ 11}$ basically is not affected by increasing the distance between the finger emitters as the variation is less than 10%. The mutual heating term on the other hand is strongly dependent on the inter-finger spacing: for the closest distance at 13 μm it is almost equal to 450 K/W while dropping by around 20 % at 26 μm . The data points for $R_{TH\ 12}$ have been fitted with a curve following a power law as:

$$R_{TH_{12}} = 1381.4 \cdot x^{-0.452} \tag{3.10}$$

Considering the simulation results and layout considerations, the spacing between fingers over 17 μm has been retained for all the following designs of the multi-finger unit-cell designs.
In the next sections, it will be shown how the parameters extracted from 3D thermal simulation can be used to improve the electro-thermal model of multi-finger DHBT to concerning device SOA.

3.4 Electro-thermal model of multi-finger DHBT

Figure 3.22 shows a schematic representation of the multi-finger modeling approach [69]. The total structure is divided into three domains: the "passive" part corresponding to contact pads and metal lines, the "active" part corresponding InP DHBTs and a thermal network describing device self and mutual healing. For a N-finger DHBT, the active part is composed by N large-signal

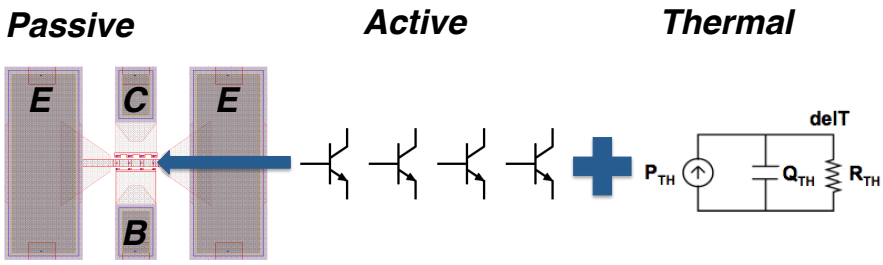

Figure 3.22: Schematic representation of multi-finger model structure: the "active" part is connected to an EM simulated passive structure and to a thermal subcircuit through a thermal node.

models of single-finger devices operated in parallel. The active part is coupled to the thermal network through the power dissipated by each finger. Also, the active part is embedded into the passive part through a multi-port parasitic network. The large-signal model for single-finger DHBTs used in this work has been improved with respect to the original UCSD model [70] and implemented as a multiport SDD in Keysight's ADS by Prof. Tom K. Johansen. The multiport nonlinear SDD is then inserted in proper simulation setup to reproduce measurement conditions to compare the results. In the next sections, the three parts will be first introduced and then the modeling results of the combined model will be presented in the case of a 4-finger device. In particular, an improvement of the thermal network description will be proposed, based on the 3D thermal simulation results of the previous section.

3.4.1 EM simulation

The first component of the multi-finger DHBT model is the EM simulation of the contact pads, metallization and the surrounding of the devices. The structure

is reproduced in Keysight ADS including layout and layer stack information. Excitation ports are defined where the internal device models will be connected to the structure and where the real measurement probes will be in contact with the pads. Thereferore the simulation result is a multi-port S-parameters matrix from 0 to 110 GHz that includes the external ports for bias and RF excitation and internal ports to be connected to the large-signal single-finger model. Fig. 3.23 shows the 3D view of the EM simulation setup as implemented in Keysight Momentum. The setup is similar to that previous employed by the authors for their electromagnetic simulation based de-embedding approach [71]. Clustered ports at the input and output pad structure resembles the coplanar waveguide type of excitation coming from the GSG probes with 125 μm pitch. This port excitation becomes electrically large at frequencies above 75.8 GHz. The EM simulation accuracy is expected to degrade above this frequency. Fig

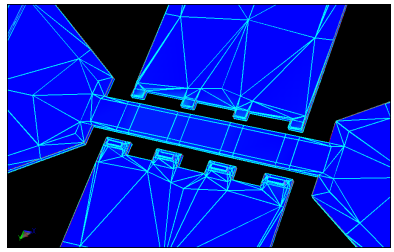

Figure 3.23: 3D view of electromagnetic simulation setup for four finger InP DHBT.

3.24 shows the measured and modeled S-parameters for the 4-finger InP DHBT at the bias point of I_C =45 mA, V_{CE} = 2 V is shown in Fig. 3.24 up to 75.8 GHz. In general, a very good agreement is observed. Measured and modeled responses begin to deviate at frequencies above 75.8 GHz. This deviation is believed to be caused by complications associated with on-wafer characterization at millimeter-wave frequencies such as parasitic modes, probe-to-chuck and probe-to-probe coupling. Furthermore, the EM simulation results above 75.8 GHz loose accuracy due to the electrically large port excitation.

3.4.2 Large-signal single-finger model

The active part of the electro-thermal model for multi-finger devices is composed by N large-signal models of single finger devices operated in parallel. The unit finger large-single model used in this work is based on the UCSD model definition [72] and is shown in Fig. 3.25. As can be seen in Fig. 3.25, the intrinsic DC

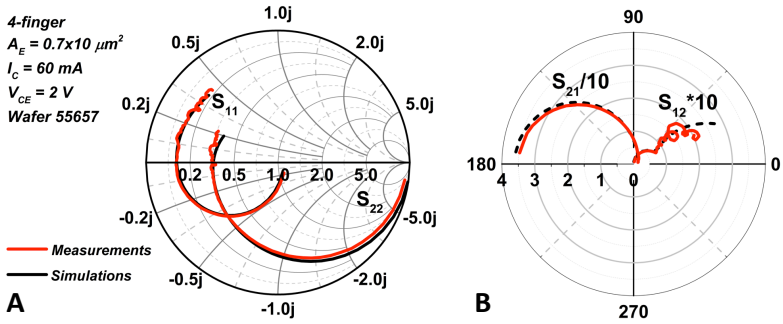

Figure 3.24: Measured (solid line) and modeled (dot line) S-parameters for four-finger InP DHBT. The bias point is I_C = 45 mA, V_{CE} = 2 V.

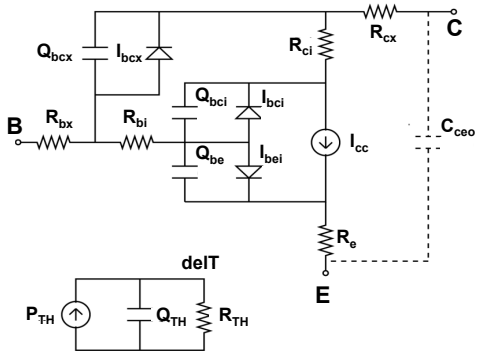

Figure 3.25: UCSD large-signal HBT model.

part is based on the Gummel-Poon model. For what concern the transfer current I_{cc} instead of using the definition based on the normalized base charge q_b, a function is implemented that take into account the variation of the emission coefficient due to the spike at the emitter-base junction of HBTs. Additionally the model takes into account several physical effects as Kirk effect, carrier velocity modulation in the collector region and electrical breakdown mechanisms due to impact ionization based on parameters extracted from measurements. The default UCSD model takes into account self-heating through a thermal subcircuit composed of a thermal resistance R_{TH} and a thermal capacitance C_{TH}. Most importantly it provides an additional thermal node that can be coupled to more sophisticated thermal networks [73]. The equivalent thermal current flowing in the thermal circuit is calculated by adding together the components I·V of dissipated powers in all the branches of the model. The equivalent current flow in the thermal subcircuit generates an equivalent voltage corresponding to the

increase in junction temperature T_j with respect to the nominal temperature of the substrate. The increase in junction temperature is used to update all the temperature dependent functions in the model including all the currents of the intrinsic transistor and emission coefficients.

3.4.3 Thermal network

The default thermal network included in the UCSD model allows to describe the relationship between the temperature increase and the power dissipated individually by each finger. However this description is not adequate for multi-finger devices since it does not take into account the contribution from the power dissipated in all the other adjacent fingers. In the case of multi-finger devices the thermal model can be modified to implement the thermal matrix described in Sec. 3.3.2 in which the temperature increase is based on Eq. 3.4 [69]. Other published approaches describe the mutual coupling through the finger temperature instead of dissipated power [74]. In this work the approach involving dissipated power was chosen because it makes it easier to be related with the results from 3D thermal simulations where the dissipated power can be set as an independent variable. The basic principle of the thermal network implemented to take into account self and mutual heating during device simulation is illustrated in Fig. 3.26. The thermal resistance parameters of Fig. 3.26 are defined

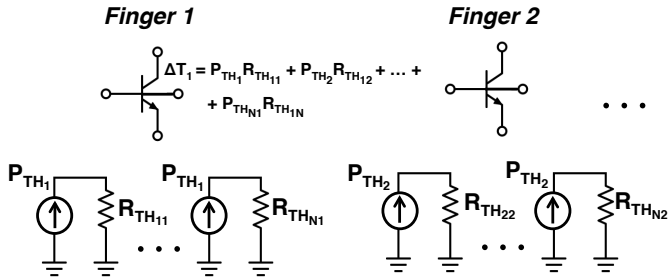

Figure 3.26: Schematic representation of mutual coupling network for multi-finger devices. The dissipated power from each finger is used to compute the increase in the finger itself and in all the other fingers through mutual coupling thermal resistances.

as real positive values constant for all device operating conditions. In addition, the schematic illustration of Fig. 3.26 is implemented in a more compact way for a N-finger device by defining a NxN thermal resistance matrix according to Eq. 3.5. This matrix describes a linear application that given as input an N-dimensional vector with the power dissipated by each finger computes as output

the N-dimensional vector of the corresponding temperature increase.
In this work we propose an incremental improvement of the thermal model in which the parameters of the thermal resistance matrix are a function of the dissipated power in the form R_{TH} (P_{diss}). The mathematical relationship between the terms of the thermal network and the dissipated power is defined as a 2^{nd}-order polynomial according to the result of 3D simulations, as presented earlier in Eq. 3.7 in the case of a 4-finger DHBT. This relationship can be expressed as:

$$\mathbf{\Delta T = P_{diss} \cdot R_{TH}(P_{diss})} \tag{3.11}$$

where all the quantities are intended as vectors. In Eq. 3.11 it can be seen that the dissipated power P_{diss} appears both in the input vector and in the definition of the thermal resistance matrix. From the computational point of view, this means that the solver will have to perform several iteration in order to update the values of P_{diss} and ΔT dynamically until a consistent solution is found. Fig. 3.27 shows the schematic implementation of a 4-finger active part coupled to a thermal subnetwork in Keysight ADS.
In the following paragraph the effect of this non-linear terms will be investigated

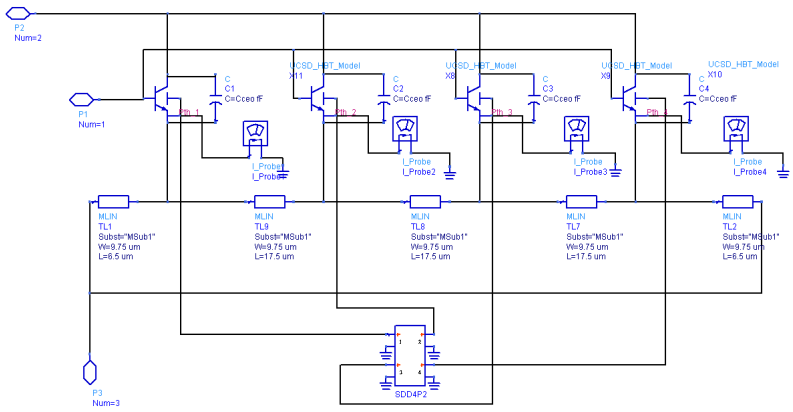

Figure 3.27: Implementation of 4-finger model with thermal network in Keysight ADS.

on device SOA comparing large-signal model simulations and measurements for a 4-finger DHBT with 0.7x10 μm^2 emitter.

3.4.4 Results of large-signal model

In order to verify the contribution of power dependent mutual heating terms implemented in the thermal circuit of the large-signal model the SOA of a 4-finger

device with 0.7x10 μm^2 emitter finger was simulated for different parameters and compared to measurements. In particular, simulations with three different thermal subcircuits are considered.

- Case A: the thermal network includes only the average self-heating terms from single-finger device measurements and the associated 4x4 resistance matrix is diagonal. this represents the case when the model is based on thermal parameters extracted from electrical measurements.
- Case B: the R_{TH} matrix is symmetric and it includes all the mutual heating terms extracted from the temperature profiles of simulated transistors
- Case C: R_{TH} matrix including power dependent parameters according to the 3D thermal simulation results.

Device output curves were simulated by applying a constant base current I_B from 0 to 4 mA and by sweeping the collector-emitter voltage V_{CE} from 0 to 7 V. The large-signal model simulations are compared to measured output curves to measurement performed in the same conditions. Figure 3.28 shows the comparison between the simulated output curves in the two cases and the corresponding measurements. It is evident that the large-signal model simulations based on

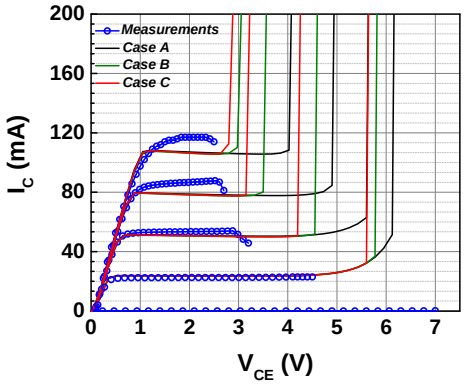

Figure 3.28: Comparison between simulated and measured I-V curves for a 0.7x10 μm^2 4-finger DHBT for three different set of parameters for the thermal network.

thermal resistance extracted from electrical measurements overestimate the real extension of the device SOA. In particular for the top curve breakdown is predicted to occur at voltage values above 4 V. Simulations taking into account also the mutual-heating terms and power dependent terms predict the breakdown to occur at 3 V for the same bias condition. The improvement in SOA prediction depends on the way the increase in finger temperature, and most importantly,

the unbalance between central (finger 2 and 3) and peripheal (finger 1 and 4) fingers is computed by the large signal models equations. Figure 3.29 further illustrates this point by showing the comparison between temperature increase in individual fingers of a 4-finger DHBT. In Fig. 3.29 the comparison is shown at different base currents from 0 to 3.2 mA with a step of 0.8 mA. The results are presented for the network of Case B (constant mutual heating terms) and Case C (power dependent mutual heating). Fig. 3.29-B shows the comparison of temperature increase in finger 2 for a fixed base current corresponding to 60 mA between Case A, B and C. The simulated profile of the pair of central central fingers 2 and 3 is identical so only one is presented. In Fig. 3.29-A it can

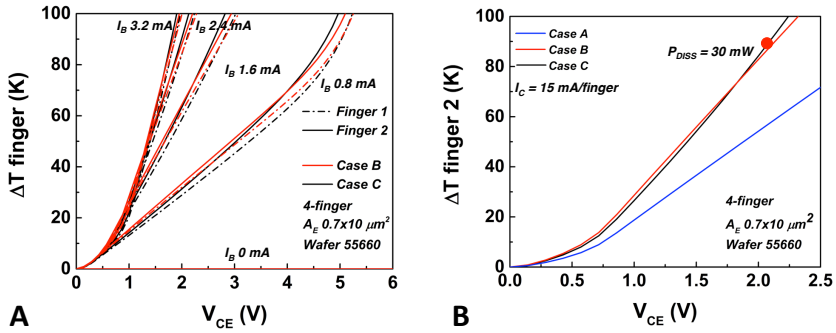

Figure 3.29: A) Temperature as a function of V_{CE} in individual fingers of a 4-finger devices with 0.7x10 μm^2 emitter from large-signal model simulation at different base currents for different thermal network parameters. B) Temperature as a function of V_{CE} in central finger of a 4-finger devices at 30 mW comparing three different thermal network parameters.

be seen that when the power dependence of mutual heating terms is considered the temperature distribution in the device is computed differently: the simulated ΔT computed in Case C (black) is consistently higher for finger 2 (solid) than finger 1(dash) at a given current level in comparison to Case B (red). In addition, with respect to Case C, the temperature increase predicted in Case B is higher at low V_{CE} and lower at high V_{CE} . This is because in Case B the ΔT is computed from linear equations with constant parameters extracted at a specific power level and thus overestimate the heating relationships at lower dissipated powers and understimate the ΔT at higher powers. The two models parameter have similar result in the region where the constant parameters where extracted. For further comparison, Fig. 3.29-B shows the ΔT for the central finger 2 for the Case A, B and C when I_C =15 mA/finger ($I_B \approx$ 1.8 mA). It is evident that a simple model based only on the results extracted from measurements as in Case A strongly underestimate the temperature increase in the device. The results for Case B and C substantially agree among them. For V_{CE} = 2 V the dissipated power correspond to 30 mW/finger . The value of ΔT from large signal simulations is 84 K while the result from 3D thermal simulations in Fig. 3.16 is 90 K. The difference between the two values is probably due to

the fact that in 3D simulations all the fingers are supposed to dissipate 30 mW while the large signal model predicts a different current distribution (and thus dissipated power) among the fingers.
The results extracted from 3D simulations clearly improves the accuracy of curves simulated from a large-signal model in comparison to parameters extracted only from measurements. Although significant improvement is obtained, additional phenomena must be taken into account and included. In particular, instabilities deriving from technological asymmetry between the fingers and current hogging have to be included to describe the behavior of real devices especially at higher current values. The inclusion of these aspects is necessary for correct SOA modeling and should be further investigated.
Concerning the RF performances of the large-signal model, load-pull simulations were performed. The accuracy of the large signal model can be verified by comparing simulated and measured load-pull data at 30 GHz. In measurements, the access pad structure has not been de-embedded, so the values of the optimum loads take into account the contribution of such a structure, and the considered power levels are those present at the probe tips. In order to reflect this scenario, an EM-circuit co-simulation comprising the pad structure layout has been implemented by means of ADS Momentum. For the 4-finger DHBT with 0.7x10 μm^2 emitter area, the measured and simulated optimum impedances are reported on the Smith chart of Fig. 3.30. The device was biased in Class A with V_{CE} =2 V and I_C =60 mA. The load selected for maximum output power is Z_L=20.6 - j3.6 Ω. The impedance values corresponding to the optimum Γ coefficients shown

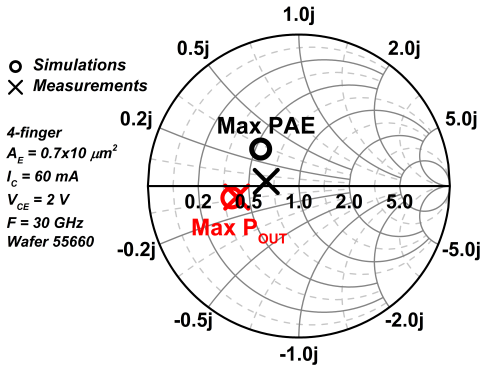

Figure 3.30: Measured and simulated optimum loads for maximum output power for a 0.7x10 μm^2 4-finger InP DHBT. The impedance values corresponding to the optimum Γ coefficients shown on the Smith Chart are Z_L=20.6 - j3.6 and Z_L=32.2 + j2 Ω to obtain maximum P_{OUT} and PAE, respectively. The device is biased in Class A with V_{CE} =2 V and I_C =60 mA.

in Fig. 3.31 are Z_L=20.6 - j3.6 Ω for maximum P_{OUT} and Z_L=32.2 + j2 Ω to obtain maximum PAE, respectively.The value of optimum load for maximum power is then selected to perform a power sweep as shown in Fig. 3.31. For the

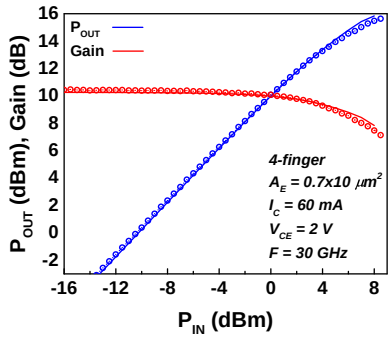

Figure 3.31: Measured and simulated power sweep for a 0.7x10 μm^2 4-finger InP DHBT. The device is biased in Class A with V_{CE} =2 V and I_C =60 mA.

4-finger DHBT the power limit of the measurement equipment did not allow us to fully saturate the device. However it was possible to assess the large-signal performance at the compression point. The highest measured output power is of about 15.5 dBm and the small signal gain is of approximately 11 dBm. The PAE peaks at 29%, slightly higher than for the measured single-finger device. Despite the frequency and power limitations of the test bench, the good agreement between simulations and measurements for both single and 4-finger devices is a good indication of the level of accuracy of the model.

3.5 Conclusions

In this chapter, the static and high-frequency performances of multi-finger DHBTs with 1 to 8 fingers and emitter length equal to 5, 7 and 10 μm have been presented. Also, the degradation of the SOA with increasing number of finger was discussed in relation to device thermal effects. To further investigate the thermal capabilities of the devices, thermal resistance measurements were performed using a method based on electrical measurements at different temperatures. The experimental thermal characterization results were then compared with the results of an approach based on 3D thermal simulations showing good agreement. The simulation results were also used to investigate the mutual coupling between the fingers and to extract power dependent parameters for the thermal resistance matrix of the large-signal model. From the results of thermal characterization for different multi-finger layouts, the final choice for the power-cell is a 4-finger DHBT in which the parallel fingers have separated collector contact and mesa while sharing the same emitter interconnection metal. The chosen distance between the center of emitter fingers is 17 μm . Finally, a modeling

approach is discussed for multi-finger DHBTs focusing on the chosen 4-finger DHBT. The individual fingers are represented by a UCSD HBT model and embedded into a multiport parasitic network. The thermal interaction between fingers is modeled by an electro-thermal coupling network and the influence of the power dependent mutual-heating parameters was compared with measurements. Also, a comparison of simulations and load-pull measurements at 30 GHz was presented. The simulated load-pull results for a 0.7x10 μm^2 4-finger DHBT are quite close to the measured values, especially concerning the load for maximum PAE. Also, the power sweep simulation results using the presented modeling approach for a 4-finger DHBT are in very good agreement with measurements.

Chapter 4

Improvement of multi-finger InP DHBT Safe Operating Area

In this chapter the results concerning the improvement of device SOA are presented focusing on a 4-finger device with 0.7x10 μm^2 finger area. The first section presents a general overview of the methods to improve device thermal management and thus improve the SOA in multi-finger devices. In particular, the ballasting approach chosen in this work is introduced concerning multi-finger devices. The static and high-frequency performances of ballasted devices are presented and compared with different solutions. An approach for ballasted device modeling is also presented based on EM and lumped elements simulations. Finally as a further investigation, the static performances of single and multi-finger transistors in common-base configuration are presented.

4.1 Overview of SOA improvement techniques

Several methods exist to limit the thermal instability and extend the SOA of multi-finger DHBTs: the general idea is to either improve device thermal properties either to avoid uneven current distribution between the fingers. In the

following, a brief overview of the most common approaches is presented that try to optimize the device at the material level or by different fabrication techniques and layouts. The overview includes material, thermal and an electro-thermal approach. For each method, advantages and drawbacks are discussed and along with the reasons for the solution adopted in this work.

4.1.1 Material approach

The ultimate reason for DHBT self-heating and subsequent thermal instability is the property that the turn-on voltage decreases with increased temperature. The voltage decrease with temperature is measured through the thermal-electric feedback coefficient ϕ and a low value is thus desirable. The thermal behavior of DHBTs could be improved by modifying the properties of the materials in the epitaxial structure or the material system altogether. In the first case, as shown in [75], the thermal-electric feedback coefficient is not critically affected by modifications of emitter-base junction properties such as conduction band spike and grading in the base for the devices based on the same material system.
Different material systems provide indeed different values of ϕ ranging from 0.7-1 mV/K for InP/InGaAs [64] or InP/GaAsSb [76] to 2 for AlGaAs/GaAs [75]. Theoretically, the coefficient ϕ is a complicated function of I_C and depends on various material parameters such as the energy gap and the temperature coefficients of the carrier mobilities [63]. Therefore for a given technology it is difficult to produce relevant changes of the value of ϕ without rethinking epitaxial and technology process.

4.1.2 Thermal approach

In the thermal approach the objective is to reduce the device thermal resistance by improving the heat dissipation in the fabricated structure. In [77], HBTs with collector-up structure and thermal-via-hole were fabricated showing a 20% reduction in thermal resistance compared to the initial structure. Also in [78] thermal via in the center of the multi-finger structure is used to reduce the overall thermal resistance of the device. In [79] a thermal shunt is adopted for microwave HBTs. In [76], the transfer substrate technique is employed were the fabricated device is moved from the original substrate to a more thermally conductive one. Another approach consists in the wafer integration of a thin film of high thermally conductive material like diamond used as a heat-sink for the HBT [80]. Other techniques include the localized thinning (also known as bathtub) of the heat sink under the device as shown in [81] The airbridge technique aims to reduce the difference between the self and mutual heating terms by inserting

a thick Au bridge that connects the emitters of all the fingers. This bridge of highly conductive material eventually transports all the heat to the heat sink but it also help to achieve a more homogenous heat distribution among the fingers [82] [83]. Multi-finger DHBT thermal properties can be enhanced by choosing different layout options concerning inter-finger spacing and placement. One approach is to increase inter-finger spacing in order to reduce the mutual-coupling between fingers. Another way is to decrease the spacing to reduce the difference between $R_{TH\ 11}$ and $R_{TH\ 12}$ (see Sec. 3.3.2): in this way the heat distribution is more homogeneous between the fingers to avoid possible thermal instabilities. In addition, other approaches have been proposed concerning non-uniform finger spacing and devices with segmented fingers [84] [85] [86].

4.1.3 Electrical approach: ballasting

The solution employed at III-V Lab for power applications consists in the implementation of an electrical feedback that reduces the excess current flowing in the fingers when it increases because of self and mutual thermal heating [68]. This is accomplished practically by ballasting technique with the introduction of a resistor between the emitter contact and ground of each finger, as shown in Fig.4.1 for a 4-finger DHBT. This solution implements a trade-off between static

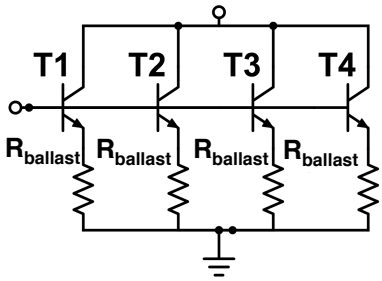

Figure 4.1: Circuit schema of a 4-finger device with ballasting resistor.

performance in terms of SOA and h_{21} gain at higher frequencies. As ballasted devices require a higher DC bias in order to reach the same bias point with respect to a non-ballasted DHBT it can be stated that the PAE of ballasted devices is reduced while a higher absolute P_{OUT} can be obtained.
To estimate the ballasting resistor value to be used, the effects of thermal resistance and of the emitter resistance can be included in the expression for the collector current of a single-finger device :

$$I_C = I_S e^{\frac{1}{\eta V_{th}}\left(V_{BE}+\phi R_{TH} I_c V_{CE} - I_C R_{E_{total}}\right)} \tag{4.1}$$

where I_s is the saturation current,η is the base-emitter junction ideality factor, v_{th} is the thermal voltage, $\phi = \frac{-\partial V_{BE}}{\partial T}$ is the thermal electric feedback coefficient as in [63] and R_{TH} is the self-heating thermal resistance for a single-finger device. From Eq. (4.1), the product ϕ R_{TH} V_{CE} corresponds to the total resistance R_{Etotal}=$R_E + R_{ballast}$ to be applied on the emitter in order to avoid thermal effects. For a 0.7x10 μm^2 single-finger DHBT with $\phi = 0.8mV/K$, R_{TH} = 1990 K/V and V_{CE} =2 V, R_{Etotal}=3 Ω. As this value is computed for a single-finger device, it can be considered a minimum value as the effect of mutual heating in a multi-finger configuration is not taken into account.

4.2 Impact of ballasting on DHBT performance

4.2.1 Static performance

In order to further investigate the improvement and the trade-off associated to different ballasting solutions, 4-finger DHBTs with different values of emitter ballasting resistors were considered, namely $R_{ballast}$ = 5, 7, 10 Ω. This result about the static characterization of ballasted 4-finger DHBTs are presented in this section. Figure 4.2-A is a Gummel plot of 4-finger DHBTs with $R_{ballast}$ = 5, 7, 10 Ω compared to a non-ballasted device. The static forward gain β associated to these devices is shown in Fig. 4.2-B). From Fig. 4.2-A it can be seen that an

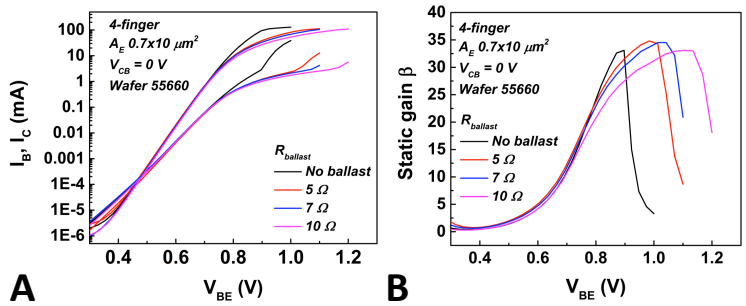

Figure 4.2: Gummel plot A) and static forward gain β of 4-finger devices with 0.7x10 μm^2 emitter area for different values of ballasting resistance.

increasing value of $R_{ballast}$ affects the Gummel plot mostly in the high-injection regime. For higher I_E values, most of the voltage between the emitter and base contact drops on the increased external emitter series resistance instead that on the intrinsic emitter-base junction. This means that a higher V_{BE} voltage needs to be applied externally to provide a given I_C value. The reduction of the

effective intrinsic junction voltage for an externally applied V_{BE} also delays to higher V_{BE} values the occurrence of Kirk-like effects and the following collapse of gain β. This is shown in Fig. 4.2 where it can be seen that the collapse of β occurs at higher V_{BE} for increasing $R_{ballast}$ values. The peak value of β is not directly affected by different $R_{ballast}$ values. Figure 4.3 shows the comparison of the SOA of a 4-finger DHBT for different values of $R_{ballast}$ with respect to a non-ballasted device. The devices were biased with I_B from 0 to 4.8 mA with a 0.8 mA step. From the I-V output curves of Fig. 4.3 it can be seen that an

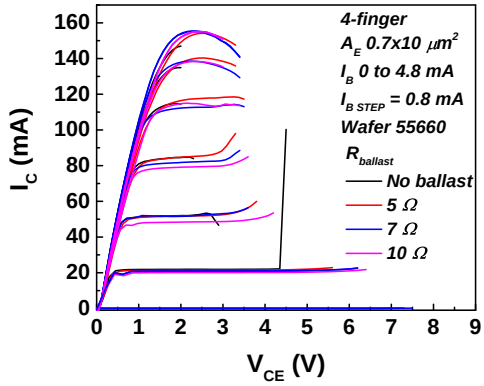

Figure 4.3: Gummel plot of 4-finger devices with 0.7x10 μm^2 emitter area for different values of ballasting resistance.

increasing value of $R_{ballast}$ provides a corresponding improvement in the V_{CE} voltage range the device can sustain at a given current level. This improvement is more immediately evident at high and medium current levels where the electric feedback I_E $R_{ballast}$ provided by the ballasting resistor is stronger. Concerning the low current performances, the measured BV_{CEO} value is similar in the 4 configurations and is around 7.2 V when I_C reaches 100 μA.

To further illustrate the improvement of static SOA by ballasting for multi-finger devices, Fig. 4.4 shows the comparison of SOA measurements between ballasted multi-finger DHBTs with A) 1, B) 2 and C) 4 fingers ballasted with a 5 Ω resistance and non-ballasted devices. For single finger devices I_B is increased from 0 to 1.6 mA with a 0.2 mA step, for 2-finger I_B varies from 0 to 2.4 mA with a 0.4 mA step while for a 4-finger device I_B is increased up to 4.8 mA with a 0.8 mA step. In Fig. 4.4-C two additional breakdown curves corresponding to I_B =1.2 mA are shown for the 4-finger devices. The output characteristics for I_B =1.85 mA are also shown to investigate the SOA for the corresponding collector current I_C =60 mA where the maximum value of f_{MAX} is reached. The graph in Fig. 4.4 presents I-V characteristics of multi-finger devices to show the effects of ballasting on multi-finger devices SOA with and without ballasting resistor. It can be seen from the figure that the introduction of an equivalent 5

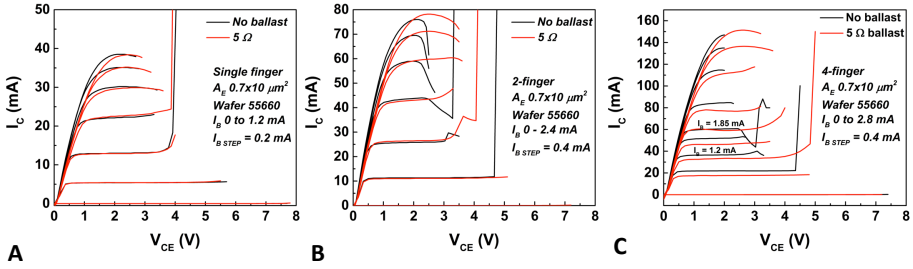

Figure 4.4: I_C -V_{CE} curves of multi-finger devices with 0.7x10 μm^2 emitter area for 1 (A), 2 (B), 4 (C) fingers and $R_{ballast}$= 5 Ω.

Ω resistance modifies the boundary of the SOA. It is also evident that the slope of the output characteristics in the saturation region is slightly degraded. This is due to the fact that the total emitter resistance is now higher and this constitutes an additional reason to minimize the value of the ballasting resistor. On the other hand, the electrical feedback caused by the ballasting resistor improves the range of V_{CE} where the device can be operated reliably. This is indicated by the red curves (corresponding to the ballasted device) that remain flat while the corresponding black curves (non-ballasted device) already start to ramp up because of breakdown mechanisms. In the end, the improvement due to a higher available voltage swing compensates for the reduction due to the reduced slope in the saturation region. The comparison of the SOA for 4-finger devices clearly illustrates the improvement in available collector emitter voltage for the same current level due to ballasting. This can be seen especially for higher current values where the heating effects lead to uneven current distribution in the device and premature degradation of device performances.
In order to compare the SOA of different devices it was chosen to compare the maximum output power given by the DHBT when used in a Class A common emitter power amplifier configuration as described in Eq. (4.2):

$$P_{OUT} = \frac{1}{4} I_{MAX} \times (V_{CE,Q} - V_{knee}) \tag{4.2}$$

where I_{MAX} is defined as twice the value of I_C at which the peak value of f_{MAX} occurs for these devices, $V_{CE,Q}$ is the voltage at the Q-point and V_{knee} is the knee voltage of the corresponding output characteristic. The value of I_C for maximum f_{MAX} was extracted from the results in Fig.2.11 and Fig. **??** and it is equal to 16, 32 and 51 mA for 1-, 2- and 4-finger devices, respectively. The value of $V_{CE,Q}$ and V_{knee} are estimated from SOA measurements comparing ballasted and non-ballasted transistors as in Fig. 4.4. The results in Table 4.1 show quantitatively the improvement in output power that could be potentially obtained at the chosen biasing point in class A operation. Assuming a load-line

Table 4.1: Improvement in the output power for ballasted devices with 0.7x10 μm^2 emitter.

Number of fingers	P_{OUT} without ballast (mW/finger)	P_{OUT} with ballast (mW/finger)	% change
1	21.7	22.7	4.8
2	23	34.6	50
4	21.7	38.3	76.5

tangent to the SOA and passing through $V_{CE,Q}$ it can be seen that ballasted devices can be biased at higher output voltages in comparison to non-ballasted ones. The results show also that the improvement is more effective for transistors with higher number of fingers.

4.2.2 Frequency performance

In the previous paragraph it was shown that an increasing value of $R_{ballast}$ improves the boundary of the static SOA of the device. In this paragraph the experimental results concerning the high-frequency performances of ballasted are presented. In Fig.4.5 the f_T as a function of collector current I_C with different emitter ballasting resistors $R_{ballast}$ is reported for 4-finger DHBTs. The devices are biased with I_C =15 mA/finger and V_{CE} = 2 V. Concerning frequency

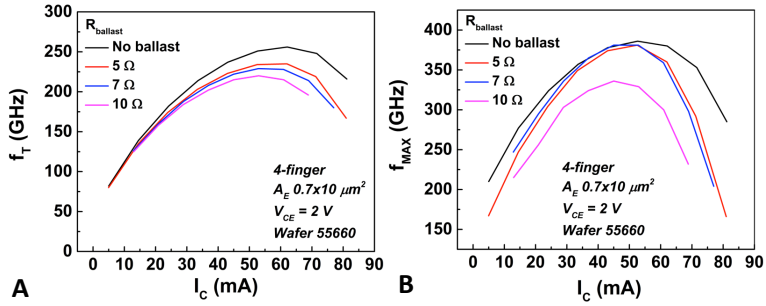

Figure 4.5: Measured A) f_T and B) f_{MAX} of a 4-finger DHBT with 0.7x10 μm^2 emitter with different values of ballasting resistor $R_{ballast}$.

performance, in Fig. 4.5-A it is shown that f_T decreases for increasing values of $R_{ballast}$ because the small-signal forward current gain h_{21} is further reduced. From the plot of Fig. 4.5-B it can be seen that the peak value of f_{MAX} is almost the same for 4-finger DHBTs without ballasting and with $R_{ballast}$=5, 7 Ω around 375 GHz. However, the current at which the roll-off of f_{MAX} can be observed

is slightly lower for ballasted devices. The DHBT with $R_{ballast}$=10 Ω exhibit a lower f_{MAX} peak value of 325 GHz.
Besides the nominal resistance value, the layout of the resistor must be carefully considered to avoid unwanted additional parasitic effects that can degrade frequency performances and eventually lead to instability. From the static and high-frequency results presented in this section, a value of $R_{ballast}$ = 5 Ω is selected for the ballasted 4-finger DHBT in the power cell.

4.3 EM and lumped parameters modeling

The modeling of devices including ballasting networks for RF simulations has to take into account the additional effects deriving from the particular layout used to implement the resistor network. In particular, parasitic effects due to additional inductive and capacitive parasitic components between the metal layers. The proposed modeling approach for ballasted DHBTs is based on the combination of the small signal models of the unit finger with a separate model of the ballasting network. The small-signal model is equivalent to the one presented in Chapter 2 where the parameters are extracted from S-parameters measurements.
On the other hand, two methods are presented to model the ballasting network: EM simulations and a physical-based approach with lumped components. In the first method, the single finger device small-signal models are connected through internal ports to the ballasting network and the distributed effects are modeled using EM simulations. In order to simulate the complete structure surrounding the devices, the mask layout and all the corresponding metal layers is reproduced in ADS. The frequency behavior of the structure is then simulated by defining and exciting multiple ports corresponding to the contacts and device terminals in the frequency range of interest. The coplanar waveguides in Ground-Signal-Ground (GSG) configuration are excited at input and output ports and the reference planes are placed at GSG contact pads. The result of the EM simulation is the S-parameter matrix of the passive multi-port structure. These results are embedded in a symbolic component as shown in Fig. 4.6 for a 4-finger ballasted DHBT. Combining this component with the single-finger device models connected to the corresponding ports, the S-parameters of the complete structure including contact pads can be simulated and compared with measurements without de-embedding. This approach is also useful to compare relative AC performances of different layout solutions when including the same intrinsic device model.
The second method is based on the physical model of the ballasting network with lumped elements. This model is connected to the emitter port of the small

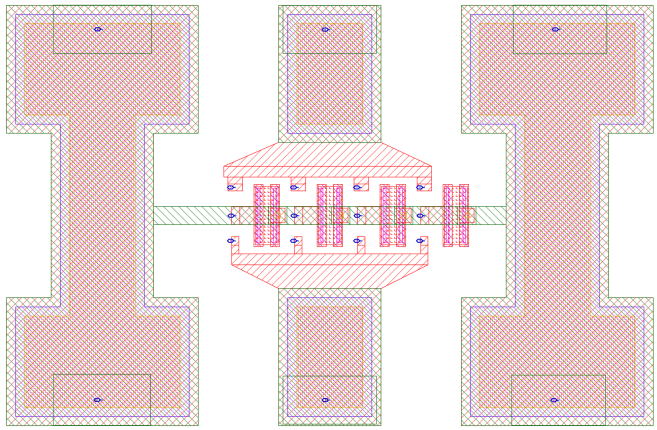

Figure 4.6: Layout of a ballasted 4-finger DHBT with 0.7x10 μm^2 emitter EM simulated from 0 to 170 GHz. The ballasting resistor has a value of 5 Ω and it is physically placed on the right-side of individual device fingers.

signal model of single finger devices through access nodes thus defining a new unified component. This new component has 2 terminals for the base and collector of each finger and two terminals for the ballasting network. This new component can then be inserted in an EM simulated structure including only the contact pads to be compared with the totally EM based approach described earlier. In order to further illustrate the representation of the ballasting network based on lumped components, the model of a ballasted network for a 4-finger DHBTs will be presented. Fig. 4.7 shows the layout of a ballasting network with $R_{ballast} = 5\ \Omega$. The equivalent resistance is obtained by the parallel connection of two resistors of 10 Ω connected on each side of the fingers emitter. Although the equivalent resistance is the same, it can be seen that the layout implementation is different with respect to Fig. 4.6. Fig. 4.8 illustrates the physical description of half of the ballasting network of Fig. 4.7. $R_{ballast}$ is the nominal value of the ballasting resistor. L_{M_2} and L_{M_3} describe the inductance of metal lines, $C_{M_2-M_3}$ is the overlapping capacitance between metal layer 2 and 3, C_{res-M_3} is the capacitance between the resistor and metal layer 3. L_{sub-M_3} models the microstrip line at metal layer 3 connecting the DHBTs emitters to the contact pads. The values of the lumped components network are computed starting from the analytical description of a distributed transmission line with the addition of the ballasting resistor. In particular, the series inductance and the overlapping capacitance components corresponding to the two metal layers are taken into account along with the resistor value and its capacitance with the metal layer. The inductive and capacitive components of the metal layers

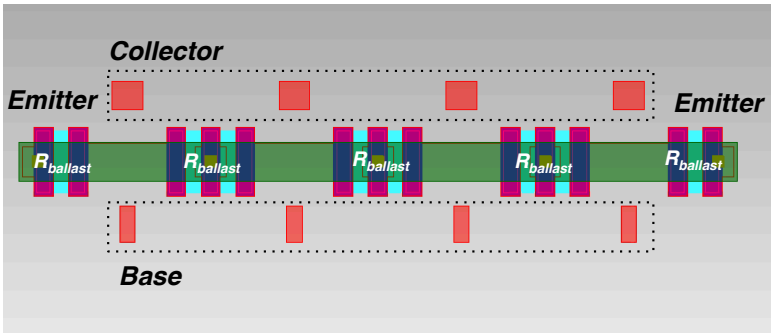

Figure 4.7: Layout of a ballasting network for a 4-finger DHBT showing the connection of the intrinsic small-signal models of each finger. The resistance $R_{ballast}$ is obtained by two resistor components with a value twice as large connected in parallel.

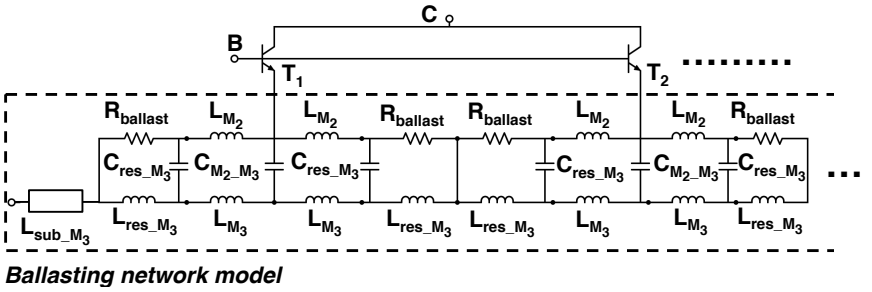

Figure 4.8: Physical model with lumped components of the ballasting network for a multi-finger device.

are computed according to:

$$\begin{aligned} L_{m_i} &= 2000\left[\ln\left(\frac{2l_i}{w_i + t_i}\right) + 0.5 + \frac{w_i + t_i}{3l_i}\right] \quad \text{H} \\ C_{m_i - m_j} &= \epsilon_{polyimide}\epsilon_0\left(\frac{w_i l_i}{d_i}\right) \quad \text{F} \end{aligned} \tag{4.3}$$

where the physical dimensions l_i, d_i and t_i are shown in the cross-section of the metallization layers in Fig. 4.9.

Fig. 4.10 shows the comparison between the MAG extracted from measurement results and computed from simulations results using the two approaches described above. The simulated and measured MAG agree reasonably for frequencies lower than 30 GHz. From 30 GHz to 65 GHz the simulated MAG is definitely overestimated with respect to measurements. The simulations have been performed up to 170 GHz for the EM and physical model and the results are consistent for both approaches over the entire range. The results from sim-

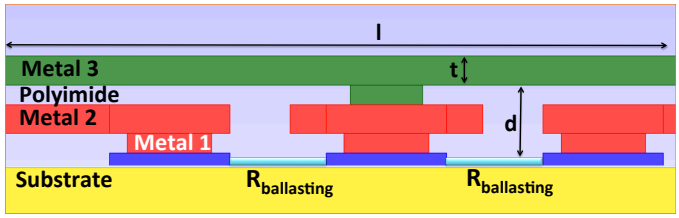

Figure 4.9: Cross-section schema of on-wafer metal levels used to compute lumped parameters model elements.

ulated DHBTs using ballasting networks models are used to assess the MAG at 170 GHz. For the 4-finger ballasted device under investigation a MAG of 2-4 dB is predicted by this modeling approach. This result suggests that ballasted devices could be included in D-band power amplifiers designs with a marginal gain.

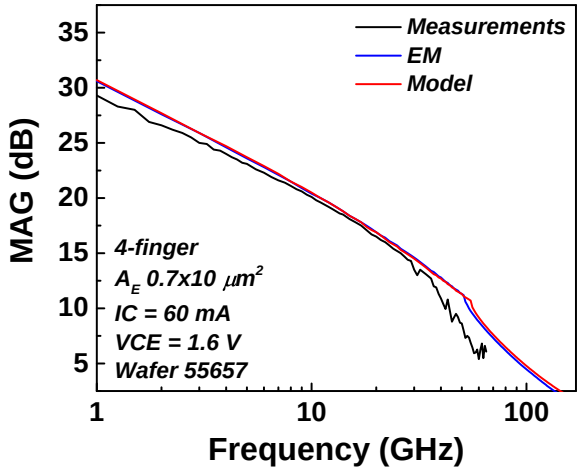

Figure 4.10: Comparison of maximum available gain for EM simulation, physical model and measurements up to 65 GHz for a 4-finger ballasted device with 0.7x10 μm^2 emitter. The MAG predicted by EM simulation and physical model is plotted up to 170 GHz.

4.4 Alternative ballasting topologies

In the traditional ballasting network scheme each resistor provides an electric feedback for a single DHBT cell. The fingers are coupled only at the thermal

level as described by the thermal resistance matrix terms. The only electrical constraint is that the sum of all the currents I_C through the finger must be constant. Thus when the current is reduced in a transistor through the ballasting resistor action the current in another finger should increase. Alternative ballasting network topologies were implemented in order to investigate the effect of an increased coupling between the fingers also at the electric level as it is presented in [87] for base-ballasted transistors. In [87] it is claimed that the increased coupling between the ballasting resistors connected to the base of each finger leads to a better temperature distribution among the fingers. This concept is implemented as a tree-like structure for a base ballasted DHBTs. This section presents the results about an application of the same concept to emitter ballasting resistors with different topologies. The devices presented in this section are based on an epitaxial structure with a 130 nm collector.
The resistors in the network presented in Sec. 4.1.3 have a constant value of 5 Ω. However, from the results about thermal simulations of Sec. 3.3.2, it is evident that central fingers reach higher temperatures with respect to the periphery during device operation. Thus the value of the corresponding emitter ballasting resistor could be increased in order to provide a stronger electrical feedback with respect to adjacent fingers. The alternative resistor topologies with stronger electrical coupling have been designed to naturally include different equivalent resistances seen by each finger in order to evaluate this aspect.
Figure 4.11 shows the circuit schematic of three additional ballasting networks. For ease of comparison, the ballasting networks were all fabricated for 4-finger DHBTs with 0.7x10 μm^2 emitters. Fig.4.12 present the EM simulated layout

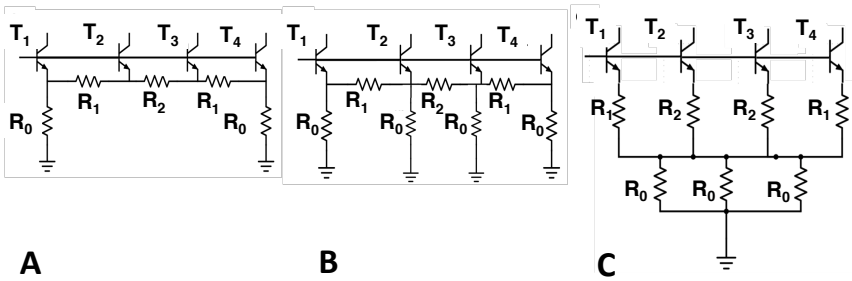

Figure 4.11: Circuit schematic of emitter ballasting resistor networks for DHBTs.

for the above mentioned devices including the different ballasting networks and the contact pads. For the ballasting network in Fig. 4.11-A, the equivalent resistance for transistors T_1 and T_2 expressed in literal form is:

$$\begin{aligned} R_{T1} &= R_0//(2R_1 + R_2 + R0) \\ R_{T2} &= (R_0 + R_1)//(R_1 + R_2 + R_0) \end{aligned} \tag{4.4}$$

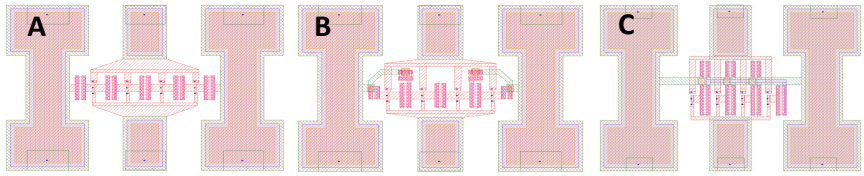

Figure 4.12: Layout of different ballast networks for 4-finger DHBT with 0.7x10 μm^2 emitter for EM simulation from DC to 170 GHz.

The resistor values were chosen to be R_0=R_1=R_2=5 Ω, thus according to Eq. (4.4) we obtain R_{T1}=4 Ω and R_{T2}=6 Ω.
In the case of solution of Fig. 4.11-B, the equivalent resistance for transistors T_1 and T_2 can be expressed as:

$$\begin{aligned} R_{T1} &= R_0//(R_1 + R_0//(R_2 + R_0//(R_1 + R_0))) \\ R_{T2} &= (R_1 + R_0)//(R_0//(R_2 + R_0//(R_1 + R_0)) \end{aligned} \tag{4.5}$$

The resistor values are R_1=R_2=5 Ω and R_0=10 Ω, thus according to Eq. (4.5) we obtain R_{T1}=5 Ω and R_{T2}=3.6 Ω. The equivalent resistance seen by each finger for the network in Fig. 4.11-C can be expressed as:

$$R_T = R_1 + R_0/3 \tag{4.6}$$

Given the values R_1=4 Ω and R_0=9 Ω the equivalent resistance seen by each finger is R_T=7 Ω.
In the next sections, the characterization results for the three cases will be presented and compared for what concern device static and high-frequency performances.

4.4.1 Static performances

This section presents the result of static measurements of 4-finger DHBTs with 0.7x10 μm^2 including the alternative ballast networks presented in Sec. 4.4. Devices are referred to according to the same naming convention presented in Fig. 4.11. A DHBT ballasted with a single 5 Ω resistor is chosen as a reference to compare the characterization results.
In Fig, 4.13 the Gummel plot of the different ballasted devices A) and the corresponding static forward gain β B) are presented. In the Gummel plot of Fig. 4.13-A the effect of the emitter resistance of the different networks can be observed for high V_{BE} values. The I_C and I_B curves are led to saturation for increasing values of equivalent resistance seen by the emitter of each finger described in 4.4. The peak value of static gain β of the devices ranges from 35 for

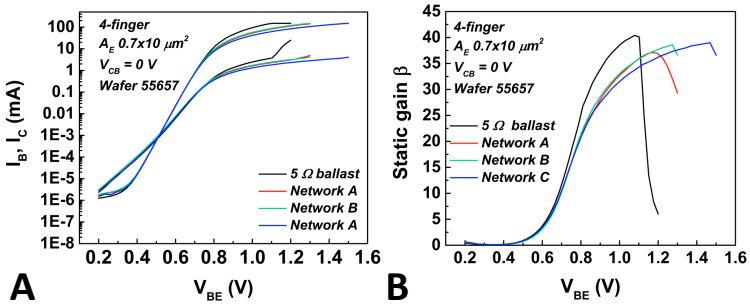

Figure 4.13: Gummel plot A) and β of 4-finger devices with 0.7x10 $\mu\mathrm{m}^2$ emitter area for the ballasting network presented in 4.4.

network B to 40 for a DHBT ballasted with a single resistor. Most importantly, the collapse of β occurs at higher $\mathrm{V_{BE}}$ with increasing emitter resistance as shown in Fig. 4.13-B. This is analogous to what observed in Sec. 4.2.1 ballasted with a single resistor of different values. In addition, it can be seen that in network A and B configuration each finger has approximately the same equivalent resistance as the collapse of β occurs at the same $\mathrm{V_{BE}}$ value. This agrees with the results corresponding to Eq. 4.4 and 4.5.
The SOA of the devices was determined by measuring I-V curves for different values of $\mathrm{I_B}$. The base current was varied from 0 to 4 mA with a 0.4 mA step. Figure 4.14 shows the measurements results for the four type of devices, including DHBTs with the initial ballasting network presented in Sec. 4.1.3. From Fig. 4.14 we can immediately see that the ballasting networks A and C

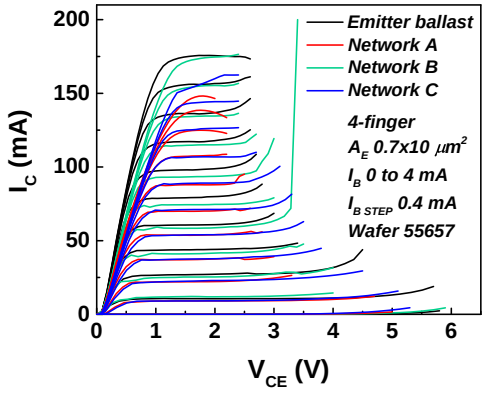

Figure 4.14: SOA measurements for DHBTs with different ballasting networks presented in Sec. 4.4. The DHBTs are 4-finger devices with 0.7x10 $\mu\mathrm{m}^2$ emitter.

perform poorly with respect to the normal ballasting scheme and to network of type B. The curves corresponding to topologies A and C reach lower collector current level for the same I_B with respect to the two other topologies. As the device gain is reduced as I_B increases, it can be deduced that the current is unevenly distributed among the fingers due to current hogging triggered by instability effects. The asymmetry of the equivalent resistor seen by each finger emitter and the increased current coupling among fingers do not improve the static performance of the device but they actually worsen it.
Although the results for the network B are comparable with the ones for the original ballasting network in terms of current gain, it is evident from Fig. 4.14 that performances are degraded for low current levels below 50 mA. In particular, in this operating region the SOA boundary and the breakdown voltage are considerably reduced for network of type B. Furthermore, some ripples exist in the knee region that could be due to an unbalanced conduction in the fingers for low V_{CE} . On the other hand, for higher current levels the boundaries of the SOA of devices using network B are slightly pushed towards higher voltages. From the static point of view there is no clear advantage in implementing an alternative ballasting network of type B including stronger electrical coupling and unbalanced resistors. In contrast to what presented in [87], the presence of a stronger coupling at the electrical level worsen the performance of the device in terms of thermal stability. This is shown by the DC measurements of devices with a network of type C where all the fingers see the same equivalent resistance of 7 Ω according to Eq. 4.6: the performance of these devices is considerably worse than devices with normal ballasting resistors of 5-7 Ω for each finger. For what concerns the utilization of unbalanced resistors in the ballasting network, additional data point should be added to draw a final conclusion: with the current set of fabricated devices it is not possible to isolate the effects of unbalanced equivalent resistors on each finger and additional electrical coupling. In a future iteration, devices should be fabricated including only single resistors with unbalanced values that are not coupled electrically as in the initial ballast configuration. In addition to DC data, frequency performances are also presented in the next section in order to give a complete overview of the different design choices.

4.4.2 Frequency performances

From the discussion in earlier sections, adding a ballasting network is an improvement for what concern DC properties and in particular device SOA. However, the additional emitter resistance degrades the frequency performances of the device. Also, different layout solutions for the ballasting network may have a different impact on device performance. In order to investigate these issues and to improve device design, the results from high-frequency characterization

of ballasted devices are presented. In this section, f_T and f_{MAX} results from frequency characterization of 4-finger DHBTs are presented for the devices including the networks of Sec. 4.4 (same naming convention applies). Finally, EM simulation results obtained using the approach described in Sec. 4.3 for the considered ballasted devices are presented. Fig. 4.15 shows the comparison of f_T and f_{MAX} as a function of I_C extracted from S-parameter measurements for the different DHBTs. The devices are biased at V_{CE} =1.6 V. The measured S-parameters were not de-embedded using on wafer structures in order to have a preliminary comparison of the relative impact of the different network layouts and to compare them with EM simulation results that include the total measurement structure. For a more complete investigation oriented to circuit design applications, all the measurements should be de-embedded from additional structures that are not included in the final circuit. This requires specific on-wafer structures to be measured and should be taken into account in future investigations.

The plot of f_T vs. I_C in Fig. 4.15-A shows that the peak value of f_T measured

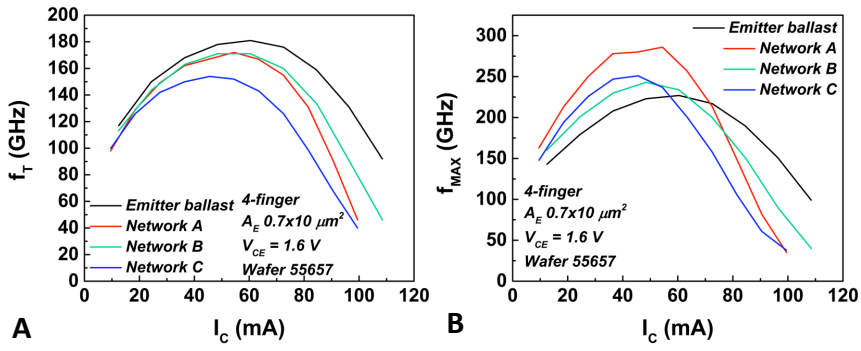

Figure 4.15: Measurement results of A) f_T and B) f_{MAX} for 4-finger DHBTs with 0.7x10 μm^2 emitter including different ballasting networks. The naming convention follows from Sec. 4.4

for the different devices decreases with the increasing value of the equivalent resistance seen by the fingers. The peak value for the DHBT with a single resistor ballasting network reaches the highest value of f_T = 180 GHz. This value is lower compared to what is shown in Fig. 4.5 for a similar device. However it has to be reminded that the result from Fig. 4.5 has been de-embedded from the influence of contact pads. The decrease in f_T is in agreement with the increase of the term R_E in Eq. 2.3. This can be further confirmed by the fact that Network A and B have the same equivalent resistance and show approximately the same f_T peak value. For the same reason, the performance of Network C in terms of peak f_T value are strongly degraded. Also interestingly, from Fig. 4.15-A the point at which the collapse of f_T occurs for the different devices can be compared. Devices with a single 5 Ω resistor connected to ground exhibit

the best performances from this point of view compared to the other ballasting network solutions. The collapse of f_T can be related to the insurgence of Kirk-life effects. The premature collapse in the alternative networks can be a further indication of uneven current distribution between the fingers in which only one or two fingers end up conducting most of the current and incurring in high-injection degradation effects.
Figure 4.15-B shows the result concerning cutoff frequency f_{MAX} as a function of I_C . The highest peak value is reached by device with ballasting Network A at 275 GHz. Network B and C have lower values of 240 and 230, respectively. The devices ballasted with only one resistor connected to ground shows f_{MAX} close to 225 GHz. Even though the devices with alternative ballasting network reach higher f_{MAX} peak values, a trend similar to the f_T case can be observed related to the collapse of f_{MAX} as a function of I_C . Devices employing ballasting network A and C exhibit a premature collapse with respect to the two other alternatives and this is probably related to the appearance of Kirk-like effects in fingers conducting most of the current. In addition, the I_C values at which peak f_{MAX} is attained are lower for devices with network A and C and the simple ballasting resistor being 40 mA for the former and 60 mA for the latter.
As already mentioned, besides the value of the ballasting resistors, the layout of the ballasting resistors can have significant impact on RF performances due to the influence of additional parasitics. The three alternative structures were simulated using the EM based approach described earlier in this chapter. The aim is the comparison of simulated f_T and f_{MAX} as a function of I_C . The EM simulation of the layouts of Fig.4.12 was carried out from 0 to 170 GHz exciting the structure at the contact pads and all the ports where the single-finger devices are then connected. The large-signal model used for simulations is adapted to the 130 nm collector technology. The f_T and f_{MAX} are then computed by simulating the complete device biased in the same conditions as in the measurements. From Fig. 4.12 it can be seen that the layout of Network A presents a more compact structure with respect to network B and a more symmetric structure with respect to network C. Indeed the original idea behind this design was to increase the RF performances while leaving unvaried the DC ballasting effect. This would be obtained by eliminating the vias connecting all the internal resistor to ground as discussed earlier and by avoiding the third metallization layer to pass over the entire cell, thus reducing parasitic inter-layer capacitances. Fig. 4.16 shows the simulation results in terms of f_T and f_{MAX} for the 4-finger DHBTs discussed in this section. The results from f_T simulation exhibit higher peak values for all the considered ballasting networks with respect to the measured results from Fig. 4.15-A discussed earlier. Most importantly, the current value $I_{max(f_T)}$ to reach the peak f_T is higher for simulated devices and f_T degradation occurs at higher current values. Also simulated f_{MAX} peaks at higher values with respect to measurements. In particular, simulation show peak f_{MAX} values above 300 GHz for devices using Network A and B while the corresponding measured results are 280 GHz and 225 GHz. One of the objec-

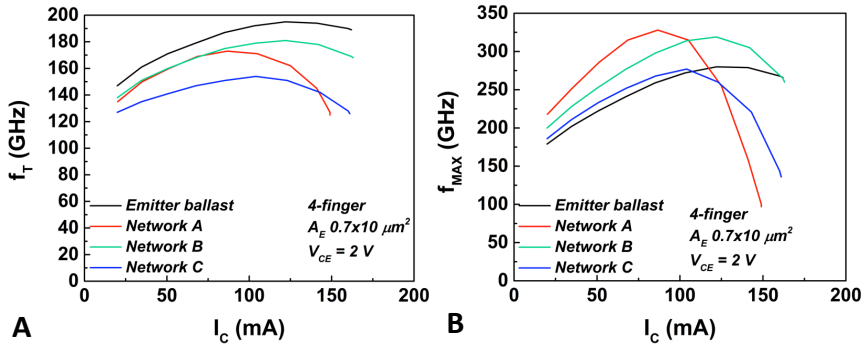

Figure 4.16: Simulation results of A) f_T and B) f_{MAX} for 4-finger DHBTs with 0.7x10 μm^2 emitter including different ballasting networks. The naming convention follows from Sec. 4.4

tive in implementing the alternative ballasting scheme of Network A is to obtain an higher f_{MAX} values by eliminating the vias to the emitter layer and overall reducing the impact of the interconnection lines as shown in Fig. 4.12. Even though f_{MAX} performance is better for DHBTs with Network A, the $I_{max(f_{MAX})}$ value is low compared to the other network topologies and the degradation of f_{MAX} occurs at much lower current level. Considering the static and frequency results presented thus far, it can be concluded that the original choice for the multi-finger ballasting network actually leads to better performance and it is maintained for the unit cell and PA design.

4.5 DHBT in common-base configuration

As it will be shown in the next chapter, the concept of stacking for PA design includes DHBTs operating in common-base (CB) configuration. The performance of the devices in this configuration were investigated in order to improve the design and understand existing limitations. In particular, the results concerning the SOA of 4-finger devices with 0.7x10 μm^2 emitter will be presented. The epitaxial structure for each DHBT includes a 130 nm collector.

Figure 4.17-A presents the plot of I_C and I_E as a function of emitter-base voltage V_{EB} . As the base terminal is connected to electrical ground the emitter-base voltage is swept from zero to negative values in order for the transistor to turn-on. The collector-base V_{CB} voltage is set equal to 0 V. Figure 4.17-B is a plot of the I_C -V_{CB} output curves of a single-finger DHBT measured in common-base configuration. The device is biased with a constant I_E current and the output I_C is measured for different V_{CB} voltages. The I_E is swept from 0 to

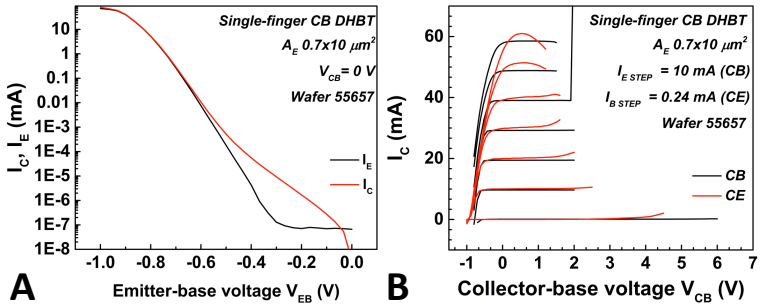

Figure 4.17: A) I_C and I_E vs. V_{EB} of a single-finger 0.7x10 μm^2 DHBT in common-base configuration. B) I_C -V_{CB} characteristic of single-finger 0.7x10 μm^2 DHBT in common-base configuration.

60 mA with a 10 mA step. The collector-base voltage V_{CB} is swept starting from the turn-on voltage that occurs for negative values in common-base configuration. The turn-on voltage is the value for which the collector current I_C is equal to zero as a function of V_{CB} : it occurs when the collector terminal is biased at a negative voltage value such that the base-collector juntion is forward biased to compensate for the current of the base-emitter junction. As it can be seen from Fig. 4.17-B, the value of the turn on voltage is not constant but decreases towards more negative values with increasing emitter current I_E . In the common-emitter (CE) definition of turn-on voltage, this effect is much less apparent because the voltage V_{CE} swept in the measurements directly controls the offset between base-emitter and base-collector junction voltages. To further investigate this point it is possible to start from the Gummel-Poon model equations using the approach described in [88] [89] and rewrite the equation for V_{CE} in common-emitter configuration as:

$$V_{CB} = V_{EB} + I_B R_B + V_{th} \cdot \ln\left[\left(\frac{I_B}{I_s}\right)^{\eta_f} \cdot \left(\frac{I_{sc}}{I_B}\right)^{\eta_r}\right] \tag{4.7}$$

where V_{CB} and V_{EB} are the collector and emitter voltage in common-base configuration respectively, I_s is the saturation current, I_{sc} is the saturation current related to space-charge recombination in the base and η_r and η_f are the ideality factors related to the emitter-base and collector-base junctions. The turn-on voltage is defined as the value of V_{CB} for which the current I_C is equal to 0. As it can be seen from Eq. 4.7, V_{CB} depends on the emitter-base junction voltage V_{EB} that increases with increasing applied I_E current. This means that in the CB configuration the turn-on voltage will shift towards more negative values at different I_E current levels. This is different with respect to CE configuration where the device can be turned off by setting V_{CE} voltage to 0. In order to compare the difference of the SOA for a single-finger device in CB and CE configurations, the measured I-V characteristics of a single-finger device in CE

configuration are superposed to the measured curves for a similar device in CB configuration in Fig. 4.17-B. For the sake of comparison, the I_B step applied to the device in CE configuration is chosen to have an output I_C current equivalent to the CB case. Also, the curves of the single-finger CE DHBT are shifted by an amount equal to the turn-on voltage on the V_{CE} axis. From Fig. 4.17-B also the BV_{CBO} of a single-finger device can be extracted to be around 5.6 V at I_C =100 μA in this technology. The value of BV_{CBO} is higher with respect to the value of BV_{CEO} of 3.3 V for the devices of the same technology in common-emitter configuration. Analogously to a single-finger device, Figure 4.19 presents the I_C and I_E curves as a function of V_{EB} and the SOA measurements of a 4-finger DHBT with 0.7x10 μm^2 emitter area per finger. Also a comparison with the SOA of a 4-finger DHBT in CE configuration is shown in Fig. 4.19-B. From

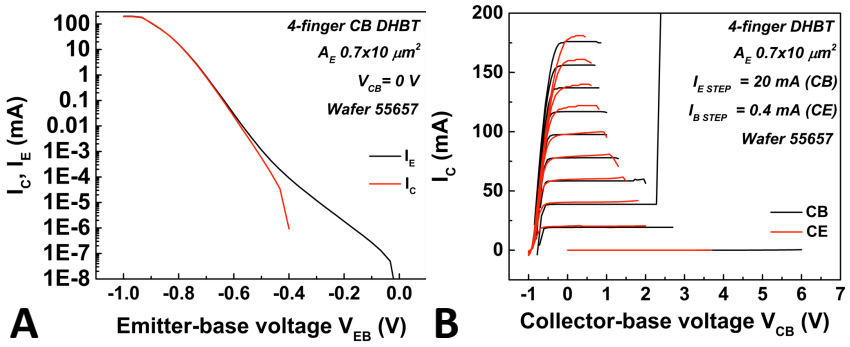

Figure 4.18: I_C and I_E as a function of V_{EB} A) and I_C -V_{CB} characteristics of 4-finger 0.7x10 μm^2 DHBT in CB configuration. The I_C -V_{CE} curves of a 4-finger device in CE configuration are superposed by applying a shift corresponding to V_{EB} difference on the V_{CB} axis.

Fig. 4.17 it can be seen that the SOA boundaries are more extended for a device biased in CB rather than CE configuration at every current level. In particular at high current levels, the effects of asymmetric current distribution and thermal heating are less evident in CB configuration. This also suggests that in the stacked configuration used for PA design the DHBTs in CE configuration are more likely to be responsible for circuit failure than the CB devices. The measured BV_{CBO} for the 4-finger DHBT is equal to 5.8 V at I_C =100 μA/finger while the BV_{CEO} in CE configuration is equal to 3.7 V. Table 4.2 summarizes the value of BV_{CBO} and BV_{CEO} for single-and 4-finger devices.

The utilization of a ballasting network to improve the boundary of device SOA can be extended to devices in CB configuration. Normally, the stacked CB devices in PA circuits are ballasted on the emitter. While keeping the same electric feedback effect described for CE transistors, CB DHBTs with base ballasting were investigated to be used in stacked PA topologies. In order to keep the same electric feedback effect on the E-B junction, the value of the base ballast

Table 4.2: Measured BV_{CEO} and BV_{CBO} of single and 4-finger DHBT at I_C =100 μA per finger

	$\mathbf{BV_{CBO}}$ **(V)** **100** μ**A/finger**	$\mathbf{BV_{CEO}}$ **(V)** **100** μ**A/finger**
1-finger	5.6	3.3
4-finger	5.8	3.7

resistance was chosen in order to keep the product I_B $R_{B_{total}}$=I_E $R_{E_{total}}$:

$$R_{B_{total}} = \frac{I_E R_{E_{total}}}{I_B} \approx \frac{I_C R_{E_{total}}}{I_B} = \frac{\beta I_B R_{E_{total}}}{I_B} = \beta R_{E_{total}} \tag{4.8}$$

where $R_{B_{total}}$ and $R_{E_{total}}$ take into account the external base and emitter resistance respectively and the ballasting resistor. The gain β is assumed to be equal to 30 for these devices. Given also the constraint of technology and unit cell layout two values of base ballasting resistors used equal to 100 and 150 Ω. Figure 4.19 shows the measured SOA of a 4-finger DHBT in common-base configuration with and without ballasting resistor. The devices are biased with a constant I_E from 0 to 160 mA with a 20 mA step. From Fig. 4.19 it can be

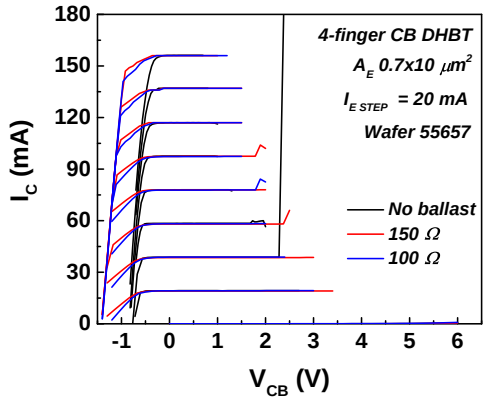

Figure 4.19: I_C -V_{CB} characteristic of 4-finger 0.7x10 μm^2 DHBT in common-base configuration.

seen that the boundary of the SOA is pushed towards higher V_{CB} values for CB devices with base ballast of 100 and 150 Ω. For example, at the current level I_C =80 mA, a non-ballasted DHBT can be biased up to V_{CB} = 1.6 V before breakdown while a base ballasted DHBT can arrive up to 2.4 V. Nevertheless, adding a base ballasting resistor in CB configuration strongly affects the device output I-V curves at low V_{CB} levels. In particular, the voltage drop on the ballasting resistor affects the turn-on voltage by requiring the application of a more negative V_{CB} value as described in Eq. 4.7. Also, the presence of an additional

base resistance degrades the I-V characteristics of the device in the proximity of the knee voltage: a resistive behavior can be observed in the I_C curves where a higher V_{CB} voltage is needed for the I_C current before flattening to a constant value. This is probably due to the fact that part of the externally applied V_{CB} voltage does not contribute directly to the reverse biasing of the B-C junction but drops instead on the ballasting resistor. This could be further confirmed by the fact that this degradation is more severe with a higher ballasting resistor value as it is shown in Fig. 4.19 by the slope of the I_C curves before the knee voltage.

4.6 Conclusions

In this chapter, the improvement of single and multi-finger DHBTs SOA through ballasting method was presented. The static and high-frequency performances of DHBTs with different ballasting resistor networks were presented in order to select the optimal configuration. Based on these results, a value of $R_{ballast}$ = 5 Ω was selected for a 4-finger with 0.7x10 μm^2 emitter in common-emitter configuration for the unit-cell. A small-signal modeling approach based on EM simulation and lumped parameters of the ballasting network was discussed. By using this approach, the MAG of 4-finger DHBTs was evaluated up to 170 GHz to assess the possibility to design PA for D-Band applications at 140 GHz. Alternative ballasting networks were presented for devices including a 130 nm collector to investigate the possibility to improve the RF performances of the devices by modifying the cell layout and exploiting the concept of increased current coupling and asymmetric resistors for central and peripheral fingers. The static and high-frequency results of these solutions were compared and finally the original network with a single 5 Ω resistor was retained for future designs. Finally the static characterization of DHBTs in common-base configuration were presented as a further investigation related to the design of stacked PA. In particular, the SOA of single and 4-finger CB DHBTs was presented and compared with CE devices. It was shown that devices in CB configuration have better SOA properties compared to CE devices. Also the value of BV_{CBO} was measured for CB devices to be used for the large-signal model. Finally the results concerning the SOA of 4-finger DHBTs with base ballasting were presented and compared to non-ballasted CB devices.
In the next chapter, a selection of demonstrator circuits will be presented in order to illustrate the capability of this technology for PA applications at mm-wave.

Chapter 5

Circuit examples

This chapter presents a selection of PA circuits designed and measured by other researchers involved in the IN-POWER project. These designs are presented to illustrate the capabilities of the InP DHBTs discussed in this thesis for PA at mm-wave. The circuits in this chapter are based on the series combination of DHBTs in a stacked architecture. By stacking n devices, the voltage swing over the stacked structure can be n times larger than a single-device thus producing a n times higher output power [90]. The structure is implemented as a power-optimized version of a traditional cascode configuration by designing inter-stage matching networks between the stacked DHBTs and by applying an additional capacitance to the base of the stacked devices [91].

5.1 Stacked InP DHBTs circuits

To demonstrate the power capabilities of this InP DHBT technology, an E-band MMIC demonstrator has been fabricated and tested [92]. The MMIC demonstrator consists of two 4-finger devices with 0.7x10 μm^2 finger in a stacked power cell configuration. The DHBTs in this circuit have a 190 nm collector designed for higher f_{MAX} and breakdown voltage. A microphotograph of the

developed demonstrator MMIC is shown in Fig. 5.1. The size of the chip is 1.2 $\times$ 1.5 μm^2 . The bias point for each device corresponds to V_{CE} =2.4 V,I_C =58

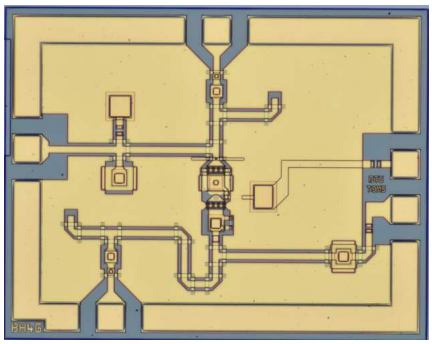

Figure 5.1: Microphotograph of demonstrator MMIC. The chip size is 1.2 $\times$ 1.5 μm^2 .

mA, well within the safe-operation-area of the 4-finger unballasted device. The measured S-parameters are shown in Fig. 5.2. The small-signal gain peaks at

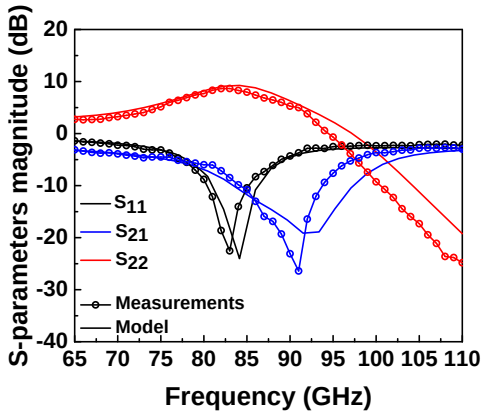

Figure 5.2: Measured S-parameters for demonstrator MMIC.

9.2 dB at the frequency of 84 GHz. The input return loss at 84 GHz is better than 23 dB while the best output return loss of 26.6 dB is slightly up-shifted to a frequency of 87.8 GHz. Concerning measured large signal performance, the maximum available power level at the probe-tips at 84 GHz is around +10.3 dBm. Fig. 5.3 shows the measured large-signal performance at 84 GHz. It is seen that the available input power is not really sufficient to fully saturate the matched power cell fully. The measured output power at the highest input power level of +10.3 dBm is around 15.8 dBm. This makes this technology highly

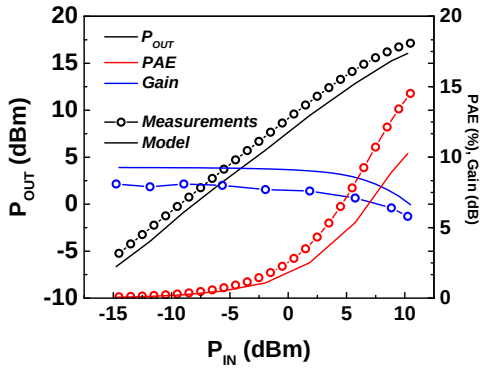

Figure 5.3: Measured large-signal performance for demonstrator MMIC. The frequency is 84 GHz.

suitable for power applications at E-band and possible also higher millimeter-wave frequencies. The associated PAE for our matched power cell peaks around 8.8%.

5.2 Two-stage Power Amplifier

This section presents a two stage 75 GHz InP DHBT power amplifier shown in Fig. 5.4 [93]. The devices used in this designed have a 130 nm collector. The power stage is composed of eight power cells combined in parallel by means of a corporate combiner implemented in CPW technology. As shown in Fig. 5.5, the maximum measured output power is 21.4 dBm and the 1-dB compression point is 18.6 dBm. The linear power gain is 12.6 dB. The maximum PAE resulted quite low (≈3 %), due to the high DC current absorbed by the power amplifier and flowing to the resistive self-bias networks.

5.3 Two-stacked transistor with ballasted common-base

Multi-finger ballasted devices with a 130 nm collector structure, have been included in the design of the power amplifier output stage in order to increase the power delivered to the load. Figure 5.6 shows an example of such a circuit in which a ballasted 4-finger DHBT is used in the stacked configuration. The results from large signal measurement are shown in Fig. 5.7. The maximum

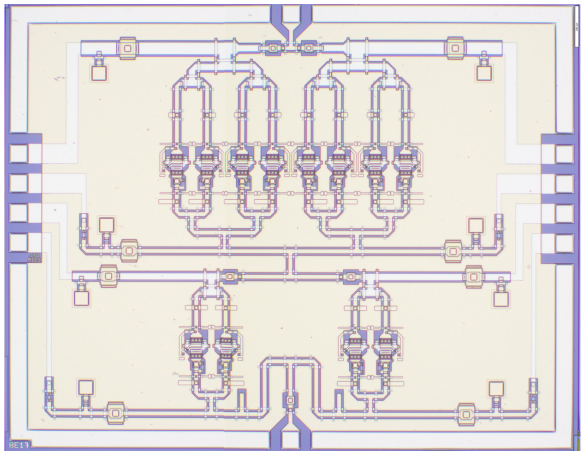

Figure 5.4: Chip microphotograph of two-stage InP DHBT power amplifier. The MMIC size is is 2.4x3.0 $\mu\mathrm{m}^2$

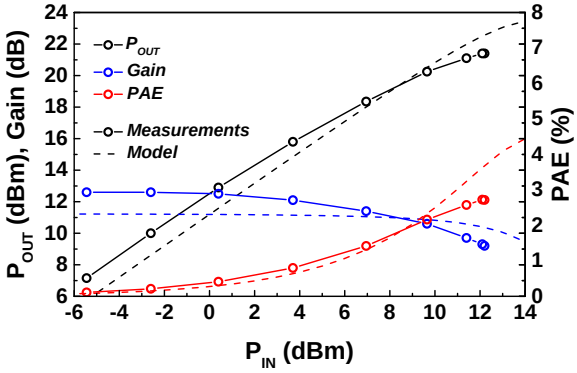

Figure 5.5: Large signal performance of two-stack amplifier at 75 GHz. $\mu\mathrm{m}^2$

measured $\mathrm{P_{OUT}}$ is 14 dBm and the linear power gain is 10 dB. The maximum PAE is 2%.

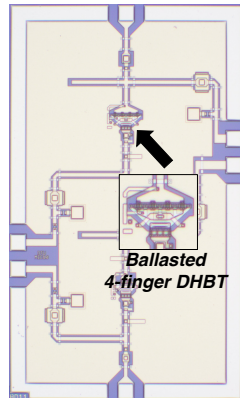

Figure 5.6: PA amplifier with ballasted devices.

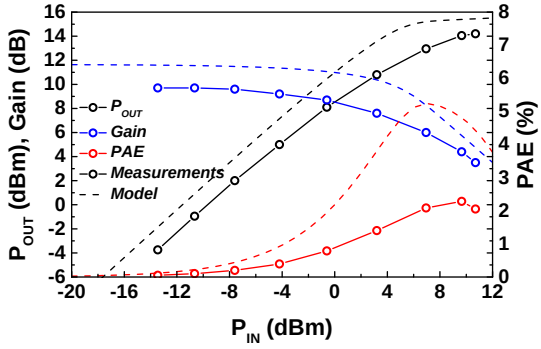

Figure 5.7: Large signal performance of PA with stacked ballasted device

Chapter 6

Conclusion

6.1 Summary of Results

This work presented the optimization of an InP DHBT technology for PA applications at mm-wave. The most important points are summarized below:

- Firstly the investigation focused on the optimization of a single-finger InP DHBT. In particular, layout geometry and epitaxial structure were considered. Different device geometries were compared to choose the most suitable emitter dimensions for further development. In particular, the static and high-frequency characterization of single-finger devices having different emitter width and length was performed. Devices with $L_E = 5$ μm and $W_E = 0.7$ μm demonstrated $f_T = 270$ GHz and $f_{MAX} = 450$ GHz. By comparing the results and taking into account the project objectives a 0.7x10 μm^2 emitter DHBT with $f_T = 260$ GHz and $f_{MAX} = 400$ GHz was selected. As an aid to investigate the impact of different collector structures on devices electrical performances a 2D TCAD physical simulation model was implemented and compared with measurements. The different measurement conditions and the corresponding parameters are indicated for the TCAD model calibration based on an iterative procedure. Although the current model shows a good agreement with measurement

results, the limitations of this approach were highlighted. Finally, the perfomances of different collector epitaxial structure of single-finger DHBTs were investigated in terms of f_T and f_{MAX} and BV_{CEO} . In particular, measurement results were compared with an analytical model and the TCAD model. The chosen collector structure approached the target performances in terms of f_{MAX} and definitely achieved the target breakdown voltage $BV_{CEO} > 7$ V.

- In order to increase the output power, single-finger DHBTs were combined in multi-finger structures. The static and high-frequency performances of multi-finger DHBTs with 1 to 8 fingers and emitter length equal to 5, 7 and 10 μm have been investigated. The degradation of the device SOA with increasing number of finger was discussed in relation to device thermal effects. The thermal capabilities of the devices were investigated by means of thermal resistance measurements and of 3D TCAD numerical simulations. The comparison between experimental and simulation results showed a reasonable agreement within 10%. A simulation based approach was also proposed to investigate the mutual coupling between the fingers and to extract power dependent parameters for the thermal resistance matrix of the large-signal model. Based on the results presented, a 4-finger DHBT with 0.7x10 μm^2 emitter has been selected for the PA unit power cell exhibiting $f_T = 260$ GHz and $f_{MAX} = 370$ GHz and $BV_{CEO} > 7$ V and capable to deliver $P_{OUT} = 16$ dBm to an optimal load under class-A operation. The DHBT has parallel fingers with separated collector contacts and mesa sharing the same emitter interconnection metal. The distance between the center of emitter fingers is 17 μm . A modeling approach is discussed for multi-finger DHBTs focusing on the chosen 4-finger DHBT. The individual fingers are represented by a UCSD HBT model and embedded into a multiport parasitic network. The thermal interaction between fingers is modeled by an electro-thermal coupling network and the influence of the power dependent mutual-heating parameters was compared with measurements.

- In order to reduce the effects of self and mutual heating on device SOA, ballasting resistors are designed for multi-finger DHBTs. The static and high-frequency performances of DHBTs with different ballasting resistor networks were presented in order to select the optimal configuration. Based on these results, a value of $R_{ballast} = 5\ \Omega$ was selected for a 4-finger with 0.7x10 μm^2 emitter in common-emitter configuration for the unit-cell. A small-signal modeling approach based on EM simulation and lumped parameters of the ballasting network was discussed. By using this approach, the MAG of 4-finger DHBTs was evaluated up to 170 GHz to assess the possibility to design PA for D-Band applications at 140 GHz. Alternative ballasting networks were presented for devices including a 130 nm collector to investigate the possibility to improve the RF performances

of the devices by modifying the cell layout and exploiting the concept of increased current coupling and asymmetric resistors for central and peripheral fingers. The static and high-frequency results of these solutions were compared and finally the original network with a single 5 Ω resistor was retained for future designs. The static characterization of DHBTs in common-base configuration were also presented as a further investigation related to the design of stacked PA. In particular, the SOA of single and 4-finger CB DHBTs was presented and compared with CE devices. It was shown that devices in CB configuration have better SOA properties compared to CE devices. Also the value of BV_{CBO} was measured for CB devices to be used for the large-signal model. Finally the results concerning the SOA of 4-finger CB DHBTs with base ballasting were presented and compared to non-ballasted CB devices.

6.2 Perspectives

This work embraced several aspects of DHBT design, characterization and modelling. However, some issues need a deeper study and analysis leaving a list of open points for further investigation. In particular:

- Collector structure and device scaling: in order to reach higher f_T /f_{MAX} levels, the scaling of the current technology is needed in terms of vertical and lateral scaling. In addition, a further investigation is needed to reduce the thickness of δ-doping layer while increasing its doping in order to optimize the base-collector transistion and reduce the collector transit time τ_C

- TCAD simulations: further investigation is needed to improve the agreement with measurements and to correct some unphysical results. The focus should be on improving the model parameters calibration in order to be predictive for any given modification in the vertical structure. The description of breakdown mechanisms should be included in the 2D TCAD model to investigate the trade-off between high-frequency operation and SOA. In addition, the 3D thermal simulations and the electrical simulations should be integrated in the same software in order to have a full electro-thermal physical model. 3D TCAD thermal simulations could be improved by using volumetric dissipated powers instead of planar surfaces. Also, the next step would be to investigate the self and mutual-heating under RF operation by including also thermal capacitance and RF power dissipation.

- The thermal resistance description for the large-signal electro-thermal model should be improved by applying a definition based on an integral relation rather than a differential one. In addition, on-wafer structures dedicated to thermal resistance measurements should be included to validate the results about mutual heating in multi-finger devices from 3D thermal simulations.

- Different multi-finger layouts could be investigated including non-uniform finger spacing and segmented emitters in order to reduce the average temperature increase in the overall device. This could limit heating effects and average temperature increase and avoid the use of ballasting resistor networks.

Appendix A

Appendix A

Parameters of TCAD models

Table A.1: List of parameters used for high-field mobility model of Eq. 2.21 for Model 1 .

	$v_{sat_n}(cm/s)$	$v_{sat_p}(cm/s)$	β_n	β_p
InP	4×10^7	6.6×10^6 [50]	1.25	1
InGaAs	3×10^7	4.9×10^6 [52]	1.25	1

Table A.2: Relaxation time τ_{en} and transport parameter ξ_n across the simulated structure of Model 1

	ξ_n	$\tau_{en}(s)$
InP Emitter	0	$1x10^{-12}$
InGaAs Base	0	$1.4x10^{-12}$
InGaAs spacer	0	$1x10^{-12}$
InP delta doping	0	$1x10^{-12}$
InP n^-	0	$1x10^{-12}$

Table A.3: List of parameters used for high-field mobility model of Eq. 2.22 for Model 2A.

	v_{sat} (cm/s)	E_{crit} (V/cm)	γ
InP	1.8×10^7	1.8×10^4	4
InGaAs	2.2×10^7	3.3×10^3	4

Table A.4: Relaxation time τ_{en} and transport parameter ξ_n across the simulated structure for Model 2A

	ξ_n	$\tau_{en}(s)$
InP Emitter	0	$1x10^{-12}$
InGaAs Base	1	$1.4x10^{-12}$
InGaAs spacer	0	$1x10^{-12}$
InP delta doping	0	$1x10^{-12}$
InP n^-	0	$1x10^{-12}$

Table A.5: List of parameters used for high-field mobility model of Eq. 2.22 for Model 2B.

	v_{sat} (cm/s)	E_{crit} (V/cm)	γ
InP	1.3×10^7	1×10^4	4
InGaAs	1×10^7	4×10^3	4

Table A.6: Relaxation time τ_{en} and transport parameter ξ_n across the simulated structure of Model 2B

	ξ_n	$\tau_{en}(s)$
InP Emitter	0	$1x10^{-12}$
InGaAs Base	0	$0.5x10^{-12}$
InGaAs spacer	0	$3.5x10^{-12}$
InP delta doping	-0.5	$0.1x10^{-12}$
InP n^-	-0.5	$1x10^{-12}$

Table A.7: List of parameters used for high-field mobility model fof Eq. 2.22 for Model 3.

	v_{sat} (cm/s)	E_{crit} (V/cm)	γ
InP	4×10^7	1×10^4	4
InGaAs	3×10^7	4×10^3	4

Table A.8: Relaxation time τ_{en} and transport parameter ξ_n across the simulated structure of Model 3.

	ξ_n	$\tau_{en}(s)$
InP Emitter	0	$1\text{x}10^{-12}$
InGaAs Base	0	$1\text{x}10^{-12}$
InGaAs spacer	0	$0.15\text{x}10^{-12}$
InP delta doping	0	$0.1\text{x}10^{-12}$
InP n^-	0	$0.1\text{x}10^{-12}$

List of Figures

List of Tables

Bibliography

[1] "Millimeter Wave Propagation: Spectrum Management Implications," *Bulletin 70*, 1997.

[2] I. Geoscience and R. S. Society, "Comments to the proposed revision of the Commission Rules Regarding Operation in the 57-64 GHz Band," *Federal Communications Commission*.

[3] N. Pohl, T. Jaeschke, and K. Aufinger, "An Ultra-Wideband 80 GHz FMCW Radar System Using a SiGe Bipolar Transceiver Chip Stabilized by a Fractional-N PLL Synthesizer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 3, pp. 757–765, 2012.

[4] D. Guermandi, Q. Shi, A. Dewilde, V. Derudder, U. Ahmad, A. Spagnolo, I. Ocket, A. Bourdoux, P. Wambacq, J. Craninckx, and W. Van Thillo, "A 79-GHz 2x2 MIMO PMCW Radar SoC in 28-nm CMOS," *IEEE Journal of Solid-state Circuits*, vol. 52, no. 10, pp. 2613–2626, 2017.

[5] D. Coquillat, V. Nodjiadjim, A. Konczykowska, N. Dyakonova, C. Consejo, S. Ruffenach, F. Teppe, M. Riet, A. Muraviev, A. Gutin, M. Shur, J. Godin, and W. Knap, "InP Double Heterojunction Bipolar Transistor for detection above 1 THz," *International Conference on Infrared, Millimeter, and Terahertz Waves*, 2015.

[6] F. Schuster, H. Videlier, A. Dupret, D. Coquillat, M. Sakowicz, J. P. Rostaing, M. Tchagaspanian, B. Giffard, and W. Knap, "A broadband THz imager in a low-cost CMOS technology," *Digest of Technical Papers - IEEE International Solid-state Circuits Conference*, pp. 5746211, 42–43, 2011.

[7] A. Konczykowska, J.-Y. Dupuy, F. Jorge, M. Riet, V. Nodjiadjim, and H. Mardoyan, "Extreme Speed Power-DAC: Leveraging InP DHBT for Ultimate Capacity Single-Carrier Optical Transmissions," *Journal of Lightwave Technology*, 2017.

[8] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130nm InP DHBTs with $f_T > 0.52$ THz and $f_{MAX} > 1.1$ THz," *Device Research Conference - Conference Digest, Drc*, pp. 5994532, 281–282, 2011.

[9] R. Fluckiger, R. Lovblom, A. M., O. O., and C. R. Bolognesi, "Type-II InP/GaAsSb double-heterojunction bipolar transistors with $f_{MAX} > 700$GHz," *Applied Physics Express*, vol. 7, no. 3, p. 034105, 2014.

[10] N. Kashio, K. Kurishima, M. Ida, and H. Matsuzaki, "InP/InGaAs double heterojunction bipolar transistors with $BV_{CEO} = 12$ V and $f_{MAX} = 470$ GHz," *Electronics Letters*, vol. 51, no. 8, pp. 648–649, 2015.

[11] Y. Chen, D. Ingram, R. Lai, M. Barsky, R. Grunbacher, T. Block, H. Yen, and D. Streit, "A 95-GHz InP HEMT MMIC amplifier with 427 mW power output," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 11, pp. 399–401, 1998.

[12] A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. F. Brown, A. L. Corrion, H. P. Moyer, S. Burnham, D. C. Regan, R. M. Grabar, C. McGuire, M. D. Wetzel, R. Bowen, P. S. Chen, H. Y. Tai, A. Schmitz, H. Fung, A. Fung, and D. H. Chow, "GaN Technology for E, W and G-band Applications," *Technical Digest - IEEE Compound Semiconductor Integrated Circuit Symposium*, p. 6978559, 2014.

[13] B. Romanczyk, M. Guidry, S. Wienecke, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "W-Band N-Polar GaN MISHEMTs with High Power and Record 27.8% Efficiency at 94 GHz," *IEEE Electron Devices*, pp. 3.5.1–4, 2016.

[14] J. F. Buckwalter, S. Daneshgar, J. Jayamon, and P. Asbeck, "Series Power Combining: Enabling Techniques for Si/SiGe Millimeter-wave Power Amplifiers," *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems (sirf)*, pp. 116–119, 2016.

[15] J. Hacker, M. Urteaga, M. Seo, A. Skalare, and R. Lin, "InP HBT Amplifier MMICs Operating to 0.67 THz," *IEEE MTT-S-s International Microwave Symposium Digest*, p. 6697518, 2013.

[16] K. Eriksson, S. E. Gunnarsson, V. Vassilev, and H. Zirath, "Design and Characterization of H-Band (220-325 GHz) Amplifiers in a 250 nm InP DHBT Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 1, pp. 56–64, 2014.

[17] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic, "Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 2982–2996, 2013.

[18] B. Heinemann, H. Rucker, R. Barth, F. Barwolf, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel, J. Katzer, J. Korn, A. Kruger, P. Kulse, T. Lenke, M. Lisker, S. Marschmeyer, A. Scheit, D. Schmidt, J. Schmidt, M. A. Schubert, A. Trusch, C. Wipf, and D. Wolansky, "Sige hbt with fx/fmax of 505 ghz/720 ghz," *Technical Digest - International Electron Devices Meeting, Iedm*, pp. 7838335, 3.1.1–3.1.4, 2016.

[19] M. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. Martin, R. Smith, S. Jaganathan, S. Krishnan, S. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom, "Submicron scaling of HBTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2606–2624, 2001.

[20] T. Kraemer, I. Ostermay, T. Jensen, T. K. Johansen, F.-J. Schmueckle, A. Thies, V. Krozer, W. Heinrich, O. Krueger, G. Traenkle, M. Lisker, A. Trusch, P. Kulse, and B. Tillack, "InP-DHBT-on-BiCMOS technology with f_T /f_{MAX} of 400/350 GHz for heterogeneous integrated millimeter-wave sources," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2209–2216, 2013.

[21] S. Lee, H. J. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahlstrŏm, and M. Rodwell, "Transferred-substrate InP/InGaAs/InP double heterojunction bipolar transistors with $f_{MAX} = 425$ GHz," *Electronics Letters*, vol. 37, no. 17, pp. 1096–1098, 2001.

[22] M. Nagatani, H. Wakita, H. Nosaka, K. Kurishima, M. Ida, A. Sano, and Y. Miyamoto, "75 GBd InP-HBT MUX-DAC module for high-symbol-rate optical transmission," *Electronics Letters*, vol. 51, no. 9, pp. 710–711, 2015.

[23] C. R. Bolognesi, R. Fluckiger, M. Alexandrova, W. Quan, R. Lovblom, and O. Ostinelli, "Inp/gaassb dhbts for thz applications and improved extraction of their cutoff frequencies," *2016 Ieee International Electron Devices Meeting (iedm)*, pp. 29.5.1–4, 2016.

[24] J. C. Rode, H.-W. Chiang, P. Choudhary, V. Jain, B. J. Thibeault, W. J. Mitchell, M. J. W. Rodwell, M. , D. Loubychev, A. Snyder, Y. Wu, J. M. Fastenau, and A. W. K. Liu, "An InGaAs/InP DHBT With Simultaneous f_T /f_{MAX} 404/901 GHz and 4.3 V Breakdown Voltage," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 1, pp. 54–57, 2015.

[25] J. Godin, V. Nodjiadjim, M. Riet, P. Berdaguer, O. Drisse, E. Derouin, A. Konczykowska, J. Moulu, J.-Y. Dupuy, F. Jorge, J.-L. Gentner, V. Krozer, T. K. Johansen, and A. Scavennec, "Submicron InP DHBT technology for high-speed high-swing mixed-signal ICs," *Proceedings of the IEEE Compound Semiconductor Integrated Circuits Symposium*, 2008.

[26] I. Harrison, M. Dahlstrom, S. Krishnan, Z. Griffith, Y. Kim, and M. Rodwell, "Thermal limitations of InPHBT's in 80 and 160 Gbits IC's," *IPRM Conference Proceedings - International Conference on Indium Phosphide and Related Materials*, pp. 160–163, 2003.

[27] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid-state Electronics*, vol. 28, no. 11, pp. 1101–3, 1101–1103, 1985.

[28] B. Li and S. Prasad, "Intermodulation analysis of the collector-up InGaAs/InAlAs/InP HBT using Volterra series," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 9, pp. 1321–1323, 1998.

[29] L. Tiemeijer and R. Havens, "A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 822–829, 2003.

[30] T. K. Johansen, R. Leblanc, J. Poulain, and V. Delmouly, "Direct Extraction of InP/GaAsSb/InP DHBT Equivalent-Circuit Elements From S-Parameters Measured at Cut-Off and Normal Bias Conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 1, pp. 115–124, 2016.

[31] G. Wedel and M. Schroeter, "Hydrodynamic simulations for advanced SiGe HBTs," *IEEE Bipolar/bicmos Circuits and Technology Meeting*, pp. 237–244, 2010.

[32] N. G. Tao, C.-P. Lee, A. S. Denis, and T. Henderson, "InGaP/GaAs HBT safe operating area and thermal size effect," *2013 International Conference on Compound Semiconductor Manufacturing Technology, Cs Mantech 2013*, pp. 219–222, 2013.

[33] J. M. Ruiz-Palmero, U. Hammer, and H. Jaeckel, "A physical hydrodynamic 2D model for simulation and scaling of InP/InGaAs(P) DHBTs and circuits with limited complexity," *Solid-state Electronics*, vol. 50, no. 9-10, pp. 1595–1611, 2006.

[34] J. M. Ruiz-Palmero, U. Hammer, H. Jackel, H. Liu, and C. R. Bolognesi, "Comparative technology assessment of future InP HBT ultrahigh-speed digital circuits," *Solid-state Electronics*, vol. 51, no. 6, pp. 842–859, 2007.

[35] C. Maneux, M. Belhaj, B. Grandchamp, N. Labat, and A. Touboul, "Two-dimensional DC simulation methodology for InP/$GaAs_{0.51}Sb_{0.49}$/InP heterojunction bipolar transistor," *Solid-state Electronics*, vol. 49, no. 6, pp. 956–964, 2005.

[36] B. Grandchamp, V. Nodjiadjim, M. Zaknoune, G. A. Kone, C. Hainaut, J. Godin, M. Riet, T. Zimmer, and C. Maneux, "Trends in Submicrometer InP-Based HBT Architecture Targeting Thermal Management," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2566–2572, 2011.

[37] G. A. Kone, B. Grandchamp, C. Hainaut, F. Marc, N. Labat, T. Zimmer, V. Nodjiadjim, M. Riet, J.-Y. Dupuy, J. Godin, and C. Maneux, "Submicrometer InP/InGaAs DHBT Architecture Enhancements Targeting Reliability Improvements," *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1068–1074, 2013.

[38] J. C. Li, M. Sokolich, T. Hussain, and P. M. Asbeck, "Physical modeling of degenerately doped compound semiconductors for high-performance HBT design," *Solid-state Electronics*, vol. 50, no. 7-8, pp. 1440–1449, 2006.

[39] S. Jain and D. Roulston, "A Simple Expression for Band-gap Narrowing (BGN) in Heavily Doped Si, Ge, GaAs and Ge_xsi_{1-x} Strained Layers," *Solid-state Electronics*, vol. 34, no. 5, pp. 453–465, 1991.

[40] J. LopezGonzalez and L. Prat, "The importance of bandgap narrowing distribution between the conduction and valence bands in abrupt HBT's," *IEEE Transactions on Electron Devices*, vol. 44, no. 7, pp. 1046–1051, 1997.

[41] V. Nodjiadjim, "Transistor bipolaire a double heterojonction submicronique InP/InGaAs pour circuits numeriques ou mixtes ultra-rapides," *PhD Thesis, Universite Lille I Sciences et Technologies*, 2009.

[42] J. Ruiz-Palmero and H. Jackel, "Impact of surface traps on downscaled InP/InGaAs DHBTs," *2004: 7th International Conference on Solid-state and Integrated Circuits Technology, Vols 1- 3, Proceedings*, vol. 2, pp. 1003–1006, 2004.

[43] K. Yang, J. East, and G. Haddad, "Numerical Modeling of Abrupt Heterojunctions Using a Thermionic-field Emission Boundary-condition," *Solid-state Electronics*, vol. 36, no. 3, pp. 321–330, 1993.

[44] R. Stratton, "Semiconductor current-flow equations (diffusion and degeneracy)," *IEEE Transactions on Electron Devices*, vol. ED-19, no. 12, pp. 1288–92, 1288–1292, 1972.

[45] B. Gonzalez, V. Palankovski, H. Kosina, A. Hernandez, and S. Selberherr, "An energy relaxation time model for device simulation," *Solid-state Electronics*, vol. 43, no. 9, pp. 1791–1795, 1999.

[46] M. Sotoodeh, A. Khalid, and A. Rezazadeh, "Empirical low-field mobility model for III-V compounds applicable in device simulation codes," *Journal of Applied Physics*, vol. 87, no. 6, pp. 2890–2900, 2000.

[47] D. Caughey and R. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proceedings of the Institute of Electrical and Electronics Engineers*, vol. 55, no. 12, p. 2192, 1967.

[48] J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite-element simulation of GaAs MESFET's with lateral doping profiles and submicron gates," *IEEE Transactions on Electron Devices*, vol. ED-23, no. 9, pp. 1042–8, 1042–1048, 1976.

[49] W. Fawcett and G. Hill, "Temperature dependence of Velocity-field Characteristic of Electrons in InP," *Electronics Letters*, vol. 11, no. 4, pp. 80–81, 1975.

[50] S. Datta, S. Shi, K. Roenker, M. Cahay, and W. Stanchina, "Simulation and design of InAlAs/InGaAs pnp heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 45, no. 8, pp. 1634–1643, 1998.

[51] V. Balynas, A. Krotkus, A. Stalnionis, A. Gorelionok, N. Shmidt, and J. Tellefsen, "Time-Resolved, Hot-electron conductivity measurement using an electrooptic sampling technique," *Applied Physics A-materials Science and Processing*, vol. 51, no. 4, pp. 357–360, 1990.

[52] T. Tauqeer, J. Sexton, F. Amir, and M. Missous, "Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors," 2011.

[53] B. Mazhari and H. Morkoc, "Effect of Collector-base Valence-band Discontinuity on Kirk Effect in Double-heterojunction Bipolar-transistors," *Applied Physics Letters*, vol. 59, no. 17, pp. 2162–2164, 1991.

[54] P. Chevalier, M. Schroter, C. R. Bolognesi, V. D'Alessandro, M. Alexandrova, J. Bock, R. Flickiger, S. Fregonese, B. Heinemann, C. Jungemann, R. Lovblom, C. Maneux, O. Ostinelli, A. Pawlak, N. Rinaldi, H. Rucker, G. Wedel, and T. Zimmer, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 7879275, 1035–1050, 2017.

[55] V. Nodjiadjim, M. Riet, A. Scavennec, P. Berdaguer, O. Drisse, E. Derouin, J. Godin, P. Bove, and M. Lijadi, "InP/GaAsSb/InP Multi-Finger DHBTs for Power Applications," *IPRM Conference Proceedings - International Conference on Indium Phosphide and Related Materials*, p. 395, 2008.

[56] W. Liu, H. Chau, and E. Beam, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 43, no. 3, pp. 388–395, 1996.

[57] R. M. Flitcroft, P. A. Houston, B. C. Lye, C. C. Button, and J. P. David, "Breakdown behaviour in wide bandgap collector GaInP/GaAs double heterojunction bipolar transistors," *Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications, Edmo*, pp. 273–278, 1997.

[58] R. Flitcroft, B. Lye, H. Yow, P. Houston, C. Button, and J. David, "Wide bandgap collectors in GaInP/GaAs heterojunction bipolar transistors with increased breakdown voltage," *Institute of Physics Conference Series*, vol. 156, pp. 435–438, 1998.

[59] R. J. Malik, A. Feygenson, D. Ritter, R. A. Hamm, M. B. Panish, J. Nagle, K. Alavi, and A. Y. Cho, "Temperature dependence of collector breakdown voltage and output conductance in HBT's with AlGaAs, GaAs, InP, and InGaAs collectors," *International Electron Devices Meeting 1991. Technical Digest (cat. No.91ch3075-9)*, pp. 805–8, 805–808, 1991.

[60] Z. Abid, W. Mckinnon, S. Mcalister, and M. Davies, "InP Double-heterostructure Bipolar-transistors With a Quaternary Collector for Improved Breakdown Behavior," *Fifth International Conference on Indium Phosphide and Related Materials*, pp. 432–434, 1993.

[61] S. Heckmann, R. Sommet, J. Nebus, J. Jacquet, D. Floriot, P. Auxemery, and R. Quere, "Characterization and modeling of bias dependent breakdown and self-heating in GaInP/GaAs power HBT to improve high power amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2811–2819, 2002.

[62] L. La Spina, V. d'Alessandro, S. Russo, N. Rinaldi, and L. K. Nanver, "Influence of Concurrent Electrothermal and Avalanche Effects on the Safe Operating Area of Multifinger Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 483–491, 2009.

[63] W. Liu, "Handbook of III-V heterojunction bipolar transistors," 1998.

[64] V. Midili, V. Nodjiadjim, T. K. Johansen, M. Riet, J. Dupuy, A. Konczykowska, and M. Squartecchia, "Electrical and thermal characterization of single and multi-finger InP DHBTs," *Proceedings of 2015 10th European Microwave Integrated Circuits Conference*, pp. 148–151, 2015.

[65] K. Asakawa, "Indium phosphide and related materials, processing, technology and devices," *Advanced Materials*, vol. 5, no. 3, pp. 228–229, 1993.

[66] S. Tiwari, "Compound semiconductor device physics," 2013.

[67] R. P. Arnold and D. S. Zoroglu, "Quantitative Study of Emitter Ballasting," *IEEE Trans Electron Devices*, vol. ED-21, no. 7, pp. 385–391, 1974.

[68] G. Gao, M. Unlu, H. Morkoc, and D. Blackburn, "Emitter Ballasting Resistor Design for, and Current Handling Capability of AlGaAs/GaAs Power Heterojunction Bipolar-transistors," *IEEE Transactions on Electron Devices*, vol. 38, no. 2, pp. 185–196, 1991.

[69] J. Ge, Y. Cao, D. Wu, Y. Su, Z. Jin, and X. Liu, "A Combined Model With Electrothermal Coupling and Electromagnetic Simulation for Microwave Multifinger InP-Based DHBTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 673–679, 2012.

[70] T. K. Johansen, V. Midili, M. Squartecchia, V. Zhurbenko, V. Nodjiadjim, J. Dupuy, M. Riet, and A. Konczykowska, "Large-signal modeling of multi-finger InP DHBT devices at millimeter-wave frequencies," *Proceedings of 2017 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits*, p. 7927301, 2017.

[71] T. K. Johansen, V. Krozer, A. Konczykowska, and J. Vidkjær, "Modeling of High-Speed InP DHBTs using Electromagnetic Simulation Based Deembedding," *Proceedings of the 2006 IEEE MTT-S*, 2006.

[72] "UCSD model documentation." `http://hbt.ucsd.edu`.

[73] M. Rudolph, *Introduction to Modeling HBTs*. Norwood, MA, USA: Artech House, Inc., 2006.

[74] A. D. D. Dwivedi, A. Chakravorty, R. D'Esposito, A. K. Sahoo, S. Fregonese, and T. Zimmer, "Effects of BEOL on self-heating and thermal coupling in SiGe multi-finger HBTs under real operating condition," *Solid-state Electronics*, vol. 115, pp. 1–6, 2016.

[75] W. Liu and a. Yuksel, "A Survey of Thermal-electric Feedback Coefficients in GaAs-based Heterojunction Bipolar-transistors," *Solid-state Electronics*, vol. 38, no. 2, pp. 407–411, 1995.

[76] A. Thiam, Y. Roelens, C. Coinon, V. Avramovic, B. Grandchamp, D. Ducatteau, X. Wallart, C. Maneux, and M. Zaknoune, "InP HBT Thermal Management by Transferring to High Thermal Conductivity Silicon Substrate," *IEEE Electron Device Letters*, vol. 35, no. 10, pp. 1010–1012, 2014.

[77] Y. X. Horng, M. Y. Hsu, and H. C. Tseng, "An Efficient Thermal-Removal Design of GaAs/InGaAs/InGaP HBT-Based Power Amplifiers," *Asia-pacific Power and Energy Engineering Conference*, vol. 2015-, no. March, p. 7066028, 2014.

[78] Y. Chen, H. Shen, and X. Liu, "A New Layout Method to Improve the Thermal Stability of Multi-finger Power HBT," *2009 IEEE 8th International Conference on Asic, Vols 1 and 2, Proceedings*, pp. 344–346, 2009.

[79] L. Liou, B. Bayraktaroglu, C. Huang, and J. Barrette, "The Effect of Thermal Shunt on the Current Instability of Multiple-emitter-finger Heterojunction Bipolar-transistors," *Proceedings of the 1993 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 253–256, 1993.

[80] K. Nosaeva, T. Al-Sawaf, W. John, D. Stoppel, M. Rudolph, F.-J. Schmueckle, B. Janke, O. Krueger, V. Krozer, W. Heinrich, and N. G. Weimann, "Multifinger Indium Phosphide Double-Heterostructure Transistor Circuit Technology With Integrated Diamond Heat Sink Layer," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1846–1852, 2016.

[81] L. Yang, J. Komiak, M. Kao, D. Houston, D. Smith, and K. Norheden, "E-Beam Re-aligned Hbts and a New Broadband MMIC Power Amplifier Using Bathtub as Heat Sink," *International Electron Devices Meeting 1994 - Iedm Technical Digest*, pp. 203–206, 1994.

[82] S. Hua-jun, G. Ji, Y. Wei, C. Yan-hu, W. Xian-tai, L. Xin-yu, and W. Dexin, "Analysis of DC and RF characterizations of InGaP/GaAs HBT with emitter air-bridge interconnection," *Chinese Journal of Electron Devices*, vol. 30, no. 1, pp. 1–4, 1–4, 2007.

[83] R. Hattori, T. Shimura, M. Kato, T. Sonoda, and S. Takamiya, "Three-dimensional modeling of thermal flow in multi-finger high power HBTs," *1995 IEEE MTT-S International Microwave Symposium Digest (cat. No.95ch3577-4)*, pp. 461–4 vol.2, 1995.

[84] D. Jin, W. Zhang, P. Shen, H. Xie, J. Yin, Y. Wang, W. Zhang, L. He, Y. Sha, J. Li, and J. Gan, "Layout Design of Multi-finger Power SiGe-HBTs for Thermal Stability Improvement," *2008 2nd IEEE International Nanoelectronics Conference, Vols 1-3*, pp. 829–832, 2008.

[85] L. Chen, C. Z. Hu, and C. L. Jiang, "Design and thermal analysis of SiGe HBT with segmented emitter fingers and non-uniform emitter finger spacing," *Applied Mechanics and Materials*, vol. 462-463, no. 462-463, pp. 592–596, 2014.

[86] R. D'Esposito, S. Fregonese, A. Chakravorty, P. Chevalier, D. Celi, and T. Zimmer, "Innovative SiGe HBT Topologies With Improved Electrothermal Behavior," *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2677–2683, 2016.

[87] H. Gao, R. Wang, H. Xue, and G. P. Li, "Novel ballast resistor network for power amplifier design," *Microwave and Optical Technology Letters*, vol. 50, no. 3, pp. 711–713, 2008.

[88] M. Hafizi, C. Crowell, and M. Grupen, "The DC Characteristics of GaAs/AlGaAs Heterojunction Bipolar-transistors With Application to Device Modeling," *IEEE Transactions on Electron Devices*, vol. 37, no. 10, pp. 2121–2129, 1990.

[89] N. Bovolon, R. Schultheis, J. Muller, P. Zwicknagl, and E. Zanoni, "Theoretical and experimental investigation of the collector-emitter offset voltage of AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 46, no. 4, pp. 622–627, 1999.

[90] M. Squartecchia, T. K. Johansen, and V. Midili, "Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers," *2015 Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMIC)*, 2015.

[91] T. K. Johansen, L. Yan, J. Dupuy, V. Nodjiadjim, A. Konczykowska, and M. Riet, "Millimeter-wave INP DHBT power amplifier based on power-optimized cascode configuration," *Microwave and Optical Technology Letters*, vol. 55, no. 5, pp. 1178–1182, 2013.

[92] V. Midili, V. Nodjiadjim, T. K. Johansen, M. Squartecchia, M. Riet, J. Y. Dupuy, and A. Konczykowska, "InP DHBT technology for power amplifiers at mm-wave frequencies," *Microelectronics Journal*, vol. 67, pp. 111–19, 2017.

[93] M. Squartecchia, V. Midili, T. K. Johansen, V. Dupuy, Jean-and Nodjidjm, M. Riet, and A. Konczykowska, "75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors ," *Asia Pacific Microwave Conference (APMC)*, 2017.