Higher power density amplifiers

Iversen, Niels Elkjær; Dahl, Nicolai Jerram; Knott, Arnold; Andersen, Michael A. E.

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Towards higher power density amplifiers*

Niels E. Iversen, *AES Student Member*, **Nicolai J. Dahl,** *AES Student Member*, **Arnold Knott,** *AES Member*, **Michael A.E. Andersen,** *AES Member*,
(neiv@elektro.dtu.dk) (s134066@student.dtu.dk) (akn@elektro.dtu.dk) (ma@elektro.dtu.dk)

Technical University of Denmark, Kgs. Lyngby, Denmark

This paper proposes a new switching strategy for switch-mode power audio amplifiers beneficial for the power dissipation in the switching devices of the power stage. The strategy is based on a thorough analysis of the loss mechanism and operating conditions of the power stage and how they relate to the audio input. The strategy utilizes a high ripple current combined with full state control improve soft switching capabilities. This result in a shift of losses from switching devices to filter inductors which are less sensitive to loss variations due to a larger form factor. Measured results on 100 W test amplifiers show that the proposed strategy reduces the power dissipation within the switches causing up to 45°C temperature reduction locally in the switches and up to 35°C globally in the amplifier. THD+N levels are down to 0.03 % and power density of implemented amplifiers are 6 W/cm^3.

0 Introduction

Switch-mode technology has during the last decade become the conventional choice for audio amplification. This is due to the superior efficiency this technology offers compared with classical amplifier topologies as class-A and -AB. The efficiency of a switch-mode audio power amplifier (class-D) can theoretically reach an efficiency of 100%. In practice efficiencies well above 90 % have been achieved [1]. Furthermore the audio performance of these amplifiers have improved over time so that very low Total Harmonic Distortion plus Noise (THD+N) levels can be achieved [2, 3, 4, 5]. The high efficiency of switch-mode technology enables high power density amplifiers. This has resulted in a selection of integrated amplifiers for low- and mid-level output powers [6, 7, 8]. However for higher output powers ($\geq$100 W) integrated amplifiers as well as small packaged discrete switching devices become less viable as the power dissipation increases and thus the need for cooling. In previous work the power density has been improved by using Gallium Nitride (GaN) devices combined with high switching frequency thus minimizing the size of bulky components in the output filter [9]. However, by increasing the switching frequency more switching losses are introduced causing undesired high operating temperatures. In addition to this temperature changes can affect the audio performance [10]. Therefore the management of power dissipation remains the main challenge to overcome in order to increase the power density of audio amplifiers.

This paper will deal with this challenge by proposing an improved switching strategy utilizing a high output filter ripple current in conjunction with full state control [11] to improve soft switching capabilities while keeping good audio performance. The result is that the power dissipation is distributed more evenly across the different elements of the amplifier leading to a decrease of operating temperature in limiting parts of the power stage, i.e. the switching devices. The method is demonstrated on 100 W test amplifiers with low THD+N levels, down to 0.03 %. A temperature reduction of up to 45 °C on the switching devices is observed while global hotspots are reduced with up to 35 °C.

1 Switch-Mode Audio Power Amplifiers

This section proposes an improved switching strategy for switch-mode audio power amplifiers. However, to improve the switching strategy a thorough understanding of the basic operation principles of the amplifiers, their inherent loss mechanism and their relation to the music input signal must be established. Therefore, this section is organized as follows: Firstly, a presentation of the main blocks of the amplifier and their functions. Secondly, a detailed analysis of loss mechanisms. Thirdly, this section presents an analysis of the dynamics of the music input signals and their relation to the operating conditions they will force the amplifier to operate in. Finally, the findings from the loss- and music-analysis is combined so that an improved switching strategy can be proposed.

*Arnold Knott, e-mail: akn@elektro.dtu.dk

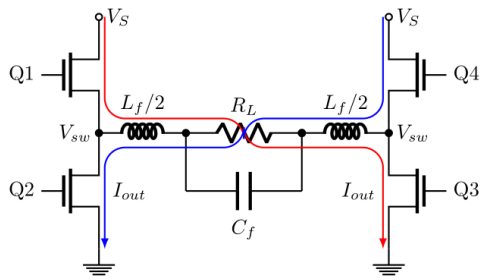


Figure 1: Full bridge configuration (BTL) of switch-mode audio power amplifier buck power stage.

Switch-mode audio power amplifiers can be split into three essential blocks. They are:

- Modulator
- Power stage
- Output filter

The basic operation of the modulator is to generate a Pulse Width Modulated (PWM) signal representing the amplifier input. This is typically done by comparing the low frequency input signal (20 Hz to 20 kHz) with a high frequency carrier, typically of triangular shape, which generates a pulse train at a given frequency, the switching frequency. The length or on-time of the pulses is also known as the duty cycle, D, of the PWM signal. Modulators can also be of a self-oscillating topology (SO) where the carrier signal is generated directly from the input [12, 13, 14]. These type of modulators will generate a varying switching frequency which decreases as the level of modulation increases. The PWM signal is used to drive the switching power stage. The power stage is where the amplification takes place. The PWM representation of the input signal is amplified according to the amplifier gain. The output filter is used to suppress switching noise for Electro Magnetic Interference (EMI) reasons.

1.1 Power stage

The power stage consists of switching devices which are switched on and off using the PWM signal. The most common switching device for switch-mode power applications is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The power stage of switch-mode audio power amplifiers are typically using a buck topology. This topology can be realized either in a half- or full-bridge configuration. The half bridge requires a dual voltage supply while the full bridge only requires a single supply. This paper focuses on a full-bridge configuration also referred to as a Bridge Tied Load (BTL). Fig. 1 shows the full bridge configuration. Q1 to Q4 are the switching devices, L_f, C_f and the load impedance (here modelled as the resistor R_L) forms the output low pass filter attenuating the switching frequency on the output while V_{sw} denotes the switch-node voltages. The factor two division on the output filter inductance ensures that equations presented in this paper is equally valid for a half bridge configuration. The switches in the half bridges are driven 180° out of phase. The current flow is highlighted in Fig. 1 where the red line shows the current flow when Q1 and Q3 conduct and the blue line when Q2 and Q4 conduct. Note that opposed to conventional DC-DC converters the audio amplifier power stage needs to be synchronous rectified as the current should be able to flow in both directions through the load. To prevent an undesired short circuit through the half bridge a period where both switches are off should be implemented. This period is known as the dead time, t_{dt} [15].

The buck topology is very attractive for audio applications due to an ideally linear transfer function which minimizes the distortion:

$$V_{out} = (2D-1)V_{DD}$$
$$I_{out} = \frac{V_{out}}{R_L} \tag{1}$$

Where V_{out} is the output voltage, D is the duty cycle, R_L is the load resistance and V_{DD} is the rail to rail voltage, i.e. $-V_S$ to V_S in half bridge- and ground to V_S in full bridge-configuration. The inductor in the output filter introduces a ripple. The magnitude of this ripple relates to the filter inductance, the switching frequency and the output voltage generated from one half bridge at a given duty cycle.

$$\Delta i_L = \frac{V_{DD}D(1-D)}{2L_f f_{sw}} \tag{2}$$

The four switches are not ideal and therefore the switch model shown in Fig. 2 is introduced. It includes the parasitic components which are the parasitic capacitances, C_{ds}, C_{gs} and C_{gd}, the on resistance R_{ds} and the drain to source body diode which will have a given forward voltage drop, V_f. There exists four different switching conditions which are relevant in order to estimate the losses in the power stage [16, 17].

1. Hard switching occurs when the parasitic drain source capacitance, C_{ds}, of the switching device can not be charged/discharged by the inductor current I_L during the dead time period t_{dt}. This can either be due to a very small dead time period, a large parasitic capacitance or an insufficient inductor current. The switching

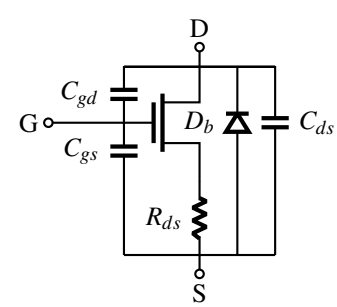


Figure 2: Switching device, e.g. MOSFET, including the parasitic on resistance, R_{ds}, the drain source capacitance, C_{ds}, the gate capacitances, C_{gs} and C_{gd} and the drain to source body diode, D_b. G = Gate, D = Drain and S = Source.

node voltage, V_{sw}, will ramp up and down together with the drain current, I_D, in the switching device, causing switching losses.
2. Reduced Voltage Switching (RVS) and Zero Voltage Switching (ZVS), on the other hand occur when the parasitic drain source capacitance of the switching device can be partially or completely charged/discharged (respectively) by the inductor current during the dead time period minimizing switching losses.
3. When the ripple in the inductor current is larger than the output current, $\Delta i_L > |I_{out}|$, a situation can occur where the parasitic drain source capacitance is charged or discharged beyond the rail to rail voltage, V_{DD}. In this situation the body diode of the switching device start conducting which causes some losses in the switching device due to the forward voltage drop of the body diode.
4. Finally, when the output current is larger than the ripple, $|I_{out}| > \Delta i_L$, the body diode of the switching device will continue conducting after turn off causing additional losses.

Fig. 3 shows the waveforms for the four described switching condition. Since the power stage is intended for audio use the duty cycle of the PWM signal driving the switching devices will vary according to the audio input. This means that power stage most likely will undergo all four switching conditions. This will be elaborated in section 1.4.

1.2 Output filter

As mentioned the output filter is formed by the filter inductor, L_f, the filter capacitance, C_f and the load impedance which can be simplified as a purely resistive load, R_L. The filter is a second order low pass filter with the simplified transfer function:

$$H_f(s) = \frac{1}{\left(\frac{s}{s_0}\right)^2 + \frac{1}{2Q}\left(\frac{s}{s_0}\right) + 1} \tag{3}$$

Where s is the Laplace operator, s_0 is the pole of the filter indicating the cut-off frequency, f_c, and Q is quality factor of the filter indicating how much the filter is dampened at its' resonance.

$$s_0 = \frac{1}{\sqrt{L_f C_f}} \tag{4}$$

$$f_c = \frac{s_0}{2\pi} \tag{5}$$

$$Q = \frac{R_e}{\sqrt{\frac{L_f}{C_f}}} = \frac{R_e}{2\pi 2 L_f f_c} \tag{6}$$

This resonance frequency is also commonly referred to as the cut-off frequency. It should be placed well below the switching frequency as the main purpose of the filter is to remove the switching transient from the output for efficiency and EMI reasons. The filter should have a flat frequency response in the audio bandwidth, i.e. 20 Hz to 20 kHz, while attenuating with 40 dB/decade above the cut-off frequency. The filter will have a quality factor, Q, which determines how much the filter is dampened at its resonance.

A high Q introduces a resonant peak in the filters frequency response as shown in Fig. 4. This peak is unwanted especially within the audio band thus conventional filter designs will aim for a maximum flat response, i.e. $Q = 0.7$ [18]. There exist parasitic components within the filter that will affect the filter characteristics. These parasitics include the series resistance, R_{Lf} and parallel capacitance, C_{Lf}, for the filter inductor and the equivalent series resistance and inductance, ESR and ESL, of the filter capacitance. Special care should be taken when choosing the filter capacitance due to the fact that its' ESR will introduce a zero placed at:

$$f_z = \frac{1}{2\pi C_f ESR} \tag{7}$$

If this zero is placed too close to the cut-off frequency it will affect the filter performance. First of all the roll off of the filter will be decreased from 40 to 20 dB/decade. Secondly the resonating current formed by the filter inductor and capacitance will be attenuated as the ESR will cause some power to be dissipated within the capacitance. For these two reasons the ESR of the capacitance should be kept to a minimum. This yields for a practical implementation using ceramic SMD capacitors. In the same manner the series resistance of the inductor will attenuate the resonating current as some power is dissipated. The series resistance is frequency dependent so it is important to ensure that the AC resistance is fairly low at the switching frequency to minimize losses. The parasitic capacitor of the inductor sets the self-resonance frequency, SRF, of the filter inductor which indicates when the inductor stops working inductive but instead becomes capacitive.

$$\mathrm{SRF}_{Lf} = \frac{1}{2\pi\sqrt{L_f C_{Lf}}} \tag{8}$$

Equally the equivalent series inductance of the capacitance generates a self-resonating frequency after which the capacitance becomes inductive.

$$\mathrm{SRF}_{Cf} = \frac{1}{2\pi\sqrt{C_f ESL}} \tag{9}$$

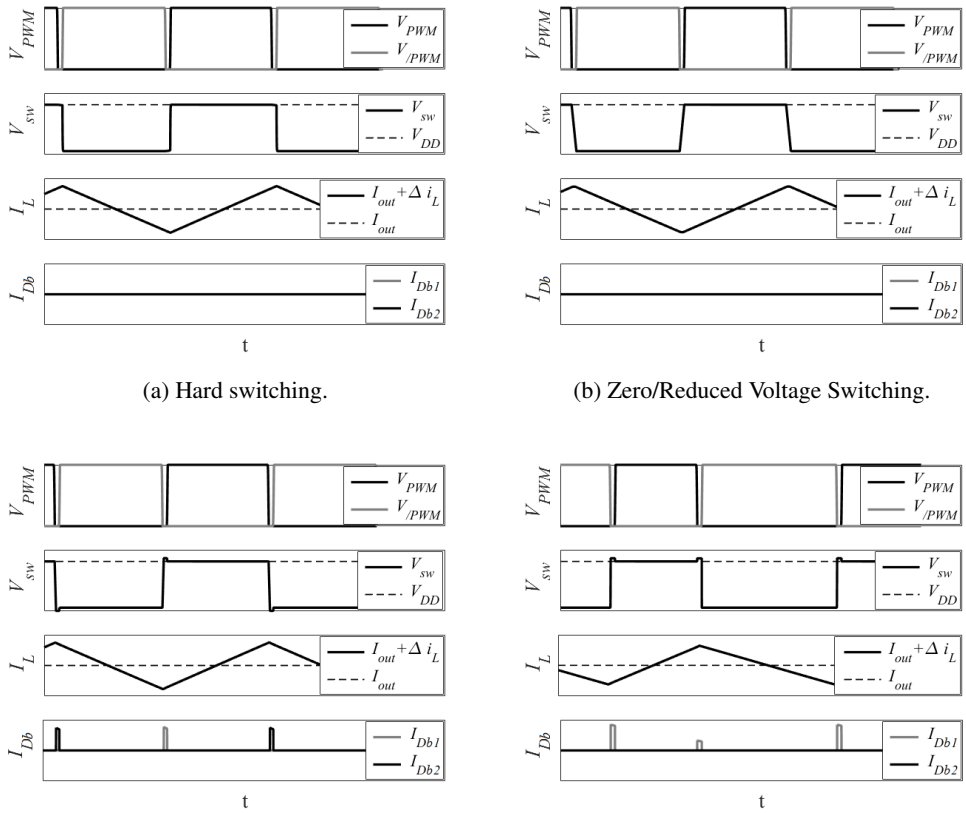
1.3 Loss mechanism

This section will describe loss mechanism related to the switching power stage and the output filter. The main loss mechanisms will be described and equations for estimating the losses presented.

1.3.1 Gate loss

Gate losses are generated by charging and discharging the gate capacitances, C_{gd} and C_{gs}, of the switching device. The needed charge is normally specified in transistor data sheet as the total gate charge, Q_g. The gate losses can be determined knowing the gate source voltage of the switching device, V_{gs}, and the switching frequency.

$$P_{gate} = Q_g V_{gs} f_{sw} \tag{10}$$



(a) Hard switching.

(b) Zero/Reduced Voltage Switching.

(c) Body diode conduction ($|I_{out}| < \Delta i_L$).

(d) Body diode conduction ($|I_{out}| > \Delta i_L$).

Figure 3: Waveforms in Buck power stage for different switching conditions. V_{PWM} is PWM gate signals, V_{SW} is switch-node voltage, I_L is inductor current and I_{Db} is body diode current.

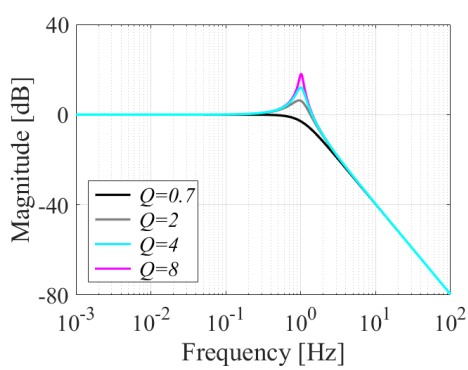


Figure 4: Frequency response of output filter for different quality factors.

1.3.2 Conduction loss

Conduction losses are generated when the switching device is on. During this state the drain current, I_D, is flowing causing some power to be dissipated in the on resistance.

$$P_{cond} = I_D^2 R_{ds} \tag{11}$$

1.3.3 Switching loss

Switching losses occur during the switching events between the on and off states. The drain current is flowing during the on state while no current flows in the off state. This current ramps up and down and together with the drain source voltage this will cause power to be dissipated. This power is actually dissipated in the parasitic drain source capacitance of the switching device, C_{ds}, as it is charged/discharged by the drain current.

$$P_{sw} = 4\left(\frac{1}{2}\left(C_{ds} + C_{gd}\right) V_{ds}^2 f_{sw}\right) \tag{12}$$

The factor four is introduced as the loss happens two times during one switching period, during rise and fall, and as the effective capacitance is doubled as two switches are tied to the switch-node. However, the switching loss can be minimized if the parasitic capacitances is charged/discharged by the instantaneous inductor current, $i_L(t)$, during the dead time period effectively reducing the drain source voltage, V_{ds}, facilitating RVS and ZVS.

$$V_{ds} = V_{DD} - V_{Cds} \tag{13}$$

Where V_{Cds} is the voltage over the parasitic capacitance. To facilitate ZVS for Q1 and Q3 in the full bridge shown in Fig. 1, V_{Cds} should be charged to the rail voltage prior to turn on and discharged to ground prior to turn off. V_{Cds} can

be estimated knowing the charging current and the charge time which are the inductor current and the dead time period respectively. The instantaneous inductor current during the dead time period can be assumed to be the sum of the output current and the amplitude of the ripple.

$$i_L = I_{out} + \Delta i \tag{14}$$

The voltage over the parasitic capacitance thus become:

$$V_{Cds} = \frac{t_{dt} i_L}{2C_{ds}} \tag{15}$$

However, if the capacitance voltage theoretically can be charged beyond the sum of the rail to rail voltage and the forward voltage drop in the diode, the body diode will start conducting thus clamping the voltage to $V_{DD} + V_f$. The same relation applies for discharging where the capacitance will be clamp to $-V_f$. Thus the voltage over the parasitic capacitance can be described as:

$$V_{Cds} = \begin{cases} -V_f & \forall \frac{t_{dt} i_L}{2C_{ds}} < -V_f \\ V_{DD} + V_f & \forall \frac{t_{dt} i_L}{2C_{ds}} > V_{DD} + V_f \\ \frac{t_{dt} i_L}{2C_{ds}}, & \text{otherwise} \end{cases} \tag{16}$$

1.3.4 Reverse conduction loss

This loss occur in the situation where the body diode in the switching device starts or continues conducting the instantaneous inductor current during the dead time period. Due to the forward voltage drop in the body diode some power will be dissipated.

$$P_{reverse} = i_L V_f t_{cond} f_{sw} \tag{17}$$

t_{cond} denotes the conducting period of the body diode. This period depends on the charge/discharge time of the drain source capacitance. The conduction period can be described as:

$$t_{cond} = \begin{cases} t_{dt} - \left| \frac{(V_{DD}+V_f)2C_{ds}}{i_L} \right| & \forall \left| \frac{t_{dt} i_L}{2C_{ds}} \right| > V_{DD} + V_f \\ 0 & \text{otherwise} \end{cases} \tag{18}$$

1.3.5 Filter loss

The loss in the output filter is mainly due to the filter inductance. These losses can be separated into winding losses and core losses.

$$P_{Lf} = P_{winding} + P_{core} \tag{19}$$

The winding losses can furthermore be separated into DC and AC losses.

$$P_{wire} = I_L^2 (R_{DC} + R_{AC}) \tag{20}$$

The core losses relates to the core material and the flux, B, in it. The flux should be kept at a level so that the core does not saturate. In the case of an air core inductor the core is lossless. Core losses can be estimated quite well [16]. However, this paper assumes core losses to be a fraction of the wire losses for simplification.

1.3.6 Total loss

The total loss can now be expressed as the sum of the different loss components:

$$P_{tot} = P_{gate} + P_{cond} + P_{sw} + P_{reverse} + P_{Lf} \tag{21}$$

For maximum output power the conduction losses, P_{cond} and the filter losses, P_{Lf}, will normally be the dominant losses. In that sense these losses limit the maximum efficiency. However, in idle operation, or close to idle operation, where the output power is low, the losses related to the parasitic capacitances become significant, i.e. P_{gate} and P_{sw}. The reverse conduction losses are normally negligible, due to the fact that the forward voltage drop of the body diode and its' conduction time in many cases is rather small. Keeping this in mind switching scenario shown in Fig. 3(c) will in many cases only cause very low switching losses since the voltage over the device is equal to the forward voltage of the body diode. However, if the output current is large a significant loss can be generated. For amplifiers with high output power the switching losses can become challenging since the supply voltage increases. Significant switching losses will heat up the device and ultimately destroy it if the heat is not dissipated elsewhere. Cooling fans can be used to secure safe operation however they increase the overall size and cost of the amplifier and produce undesired audible noise. In section 1.5 alternative method of dealing with this challenge will be presented.

1.4 Audio dynamics

The input signal to the audio amplifier is naturally a dynamic audio signal. For test purposes sine waves are a commonly used signal. However, sine waves do not represent real audio signals [19, 20, 21, 22]. In previous work a large music library have been analysed in terms of amplitude distribution [22]. Fig. 5 shows the amplitude distribution of a sine wave and the audio tracks from the music library. With the 90 % distributions marked for comparison it is clear that there exists a fundamental difference between real audio signals and sine waves. As shown in Fig. 5 the amplitude distribution can be directly translated into a duty cycle distribution when a linear input to out-

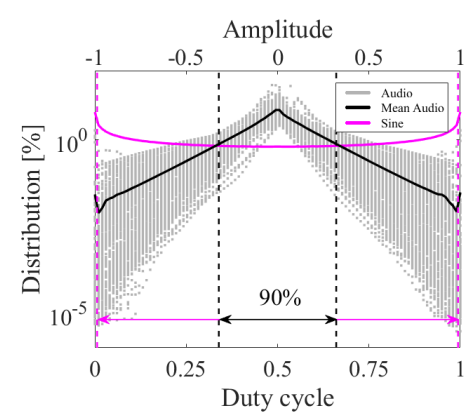


Figure 5: Amplitude and duty cycle distribution for audio tracks and sine wave.

put transfer function is assumed. It is observed that a sine wave signal will utilize almost full modulation 90 % of the time while real music in average only utilize one third of that. However this distribution is not universally true since that this analysis assumes that the amplifier is driven at full modulation, i.e. clipping or maximum output power. In reality this is a rarely used playback condition. The most typical playback conditions are at background- and listening-levels where the output power is significantly smaller than at clipping [23], meaning that the distribution will be centred more around zero amplitude corresponding to 50 % duty cycle. These typical playback conditions account for 99 % of the amplifier usage, leaving only 1 % usage for party- and clipping-conditions [23]. This should be kept in mind when designing the amplifier power stage as it make sense to optimize the amplifier for the intended use, i.e. low output power, though the amplifier still should be able to handle full power sine waves for short periods of time.

1.5 Improved switching strategy

Switching losses can be of significant magnitude even at low power causing the temperature of the switching device to rise eventually destroying it. Therefore it is relevant to secure that ZVS, RVS and body diode conduction are the most typical switching conditions, shown in Fig. 3(b) and 3(c), as the switching losses in theses cases will be fairly low. From Fig. 5 the 90 % duty cycle distribution span for real music can be evaluated to be from $D = 0.34$ to $D = 0.66$. Optimizing the switching condition for this duty cycle span will decrease the switching losses, and thus also the temperature of the switching device securing a more robust design.

To facilitate ZVS and RVS for a given duty cycle span the reactive ripple current in the output filter inductor must be dimensioned so that the ripple current is larger than continuous output current for all duty cycles within that span. That is $\Delta i > I_{out}$. This requirement can be written using (1) and (2).

$$\frac{V_{DD}D(1-D)}{2L_f f_{sw}} > \frac{(2D-1)V_S}{R_L} \tag{22}$$

Examining the above equation it is realized that as the duty cycle moves away from idle, $D = 0.5$, the ripple current will decrease for a power stage with a fixed switching frequency. This makes it challenging to facilitate ZVS and RVS over a large duty cycle span. Therefore a self-oscillating modulation scheme should be preferred since the switching frequency will decrease with the level of modulation [12]. In fact it can be shown that the ripple current will be more or less constant for all duty cycles using self-oscillating modulators. Shaping the ripple current's amplitude can be done by adjusting the quality factor of the output filter according to (2) and (6). Fig. 6 illustrates how the ZVS/RVS region increases with higher quality factors and a self-oscillating modulation scheme as it shows the ratio between the ripple- and the continuous output-current vs. duty cycle for various quality factors for both conventional fixed frequency- and self-oscillating-modulation. As long as the ratio is larger than one (22) is satisfied and RVS and ZVS can in principle be facilitated on all switching devices. A high ripple current increases the AC losses in the filter inductors causing their temperature to rise. This means that amplifiers utilizing this switching strategy does not improve in terms of overall losses necessarily when compared to conventional designs. However, it is expected amplifiers utilizing the proposed switching strategy will improve on overall operating temperatures. The improved soft switching capabilities will lower the losses in the switching devices. These switching devices will typically have quite high junction to ambient thermal resistance, R_{thJA}, if no cooling strategy is applied due to their small form factor. This means that their operating temperature is very sensitive to the power loss. It is not uncommon for conventional MOSFET power switch to have junction to ambient thermal resistance in the range $R_{thJA} \approx 60$ K/W [24, 25]. Opposed to that inductors are typically in a much larger package compared to the switching devices and their losses are scattered between core and wire providing them with a lower overall thermal resistance. Therefore, their operating temperature is less sensitive to variation in their power loss and it makes sense to dissipate some extra energy in them to lower the power dissipation in the switches. The amount of soft switching present in the individual power stage switch can be expressed as a soft switching factor, V_P [26, 27]. For the switches in the amplifier power stage the soft switching factor can be written as:

$$V_P = \frac{V_{Cds}}{V_S} = \frac{t_{dt} i_L}{2C_{ds}V_s} \tag{23}$$

To control amplifiers using this switching strategy, full state control can be used. Opposed to conventional output control techniques, such as PI and PID regulators, full state control is derived from a state space modelling of the amplifier. Using all the available states in the amplifier as feedback paths this control technique provides high control

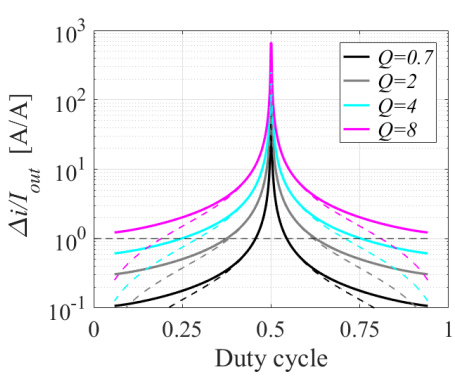


Figure 6: Ratio between ripple- and continuous output-current vs. duty cycle current for various quality factors. Self-oscillating modulation (solid) and fixed frequency modulation (dashed).

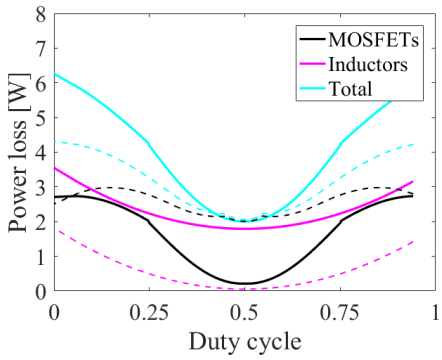


Figure 7: Estimated amplifier losses. Proposed amplifier (solid) and prior art amplifier (dashed).

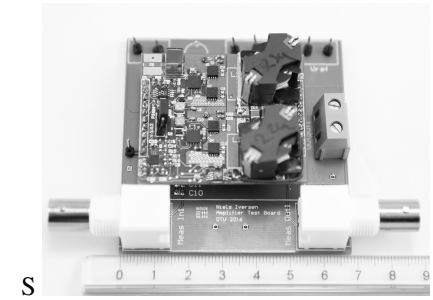


Figure 8: Realized switch-mode power audio amplifier.

the placement of the system's poles. This is a desired feature for a switch-mode power audio amplifier with a high filter quality factor as the resonant peak in the frequency response can be effectively removed while keeping good audio performance. The focus of this paper is not on the controller design and will not be elaborated further. However, the design of the full state controller for switch-mode audio power amplifiers is described in great detail in [11].

2 Design and Implementation

Two amplifiers were designed and implemented on two layer 4 x 5 cm^2 Printed Circuit Boards (PCBs). The amplifiers are identical in their structure and use same topology for modulator, power stage, output filter and control and can deliver a continuous output power of 100 W. The boxed volume power density is 6 W/cm^3. The specifications of the amplifiers are shown in Table 1. Both amplifiers use a self-oscillating modulator and full state control. The states used for feedback in this implementation is the inductor current, I_L, the output current, I_{out}, and the output voltage, V_{out}. Both amplifiers use a 100V MOSFET from infineon in a small 3.2 X 3.2 mm^2 PG-TSDSON-8 package [24]. In addition to that the filter inductors of both amplifiers are wound with litz wire on RM7 cores using N87 material to keep the AC resistance as low as possible. The amplifiers differ on filter design where one use prior art methods, i.e. a low quality factor of $Q = 0.7$, while the other use the proposed switching strategy with a high quality factor of $Q = 4$. This difference makes a huge impact on the power losses in the amplifier. Fig. 7 shows the predicted losses in the proposed amplifier (solid line) and the prior art amplifier (dashed line). Even though the total losses are slightly higher in the proposed amplifier it is observed that power dissipation within the switching MOSFETs is reduced with a factor of two for duty cycles ranging from 0.34 to 0.66, corresponding to the 90 % distribution of average music, as explained in section 1.5. The reduction of power losses within the MOSFETs is expected to lower the operating temperature, especially for music signals. Fig. 8 shows one of the implemented amplifiers connected to a dedicated measurement board.

Table 1: Specifications of implemented amplifiers

	Prior art	Proposed	
Cutoff frq (f_c)	40	40	kHz
Filter ind. (L_f)	23	4	μH
Filter cap. (C_f)	0.35	2	μF
Quality Factor (Q)	0.7	4	
Idle switch Frq (f_{sw})	500	500	kHz
Supply voltage (V_S)	50	50	V
Dead time (t_{dt})	10	10	ns
Gain (G)	32.5	32.5	dB
Load (R_L)	8	8	Ω
Power stage	BTL Buck	BTL Buck	
Modulation	SO	SO	
Control	Full state	Full state	

3 Measurements

A series of measurements has been performed on the implemented amplifiers to investigate their performance on key parameters. They include measurements of amplifier distortion, soft switching capabilities and operating temperatures.

3.1 Total Harmonic Distortion

Fig. 9 shows the measured Total Harmonic Distortion plus Noise (THD+N) vs. output power for a 100 Hz sine wave measured A-weighted with the UPP Audio Analyzer from Rohde & Schwarz. 100 Hz is used as it is a commonly used test frequency. Both amplifiers show excellent performance with THD+N down to 0.03% which is comparable to available consumer products [7, 8]. This demonstrates that full state control is applicable for audio applications.

3.2 Soft switching capabilities

The soft switching capabilities are measured by driving the power stage at fixed duty cycles and measuring the switching waveforms. Fig. 10(a) and 10(b) show the rising edge of the switching waveforms for both amplifiers. The voltage over the parasitic capacitance, V_{Cds}, at the switching event is highlighted. This provides information concerning the soft switching capabilities on the high

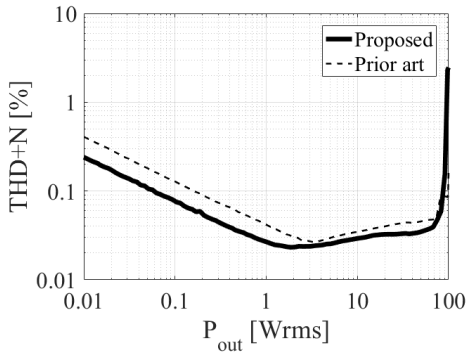


Figure 9: THD+N @100 Hz. Proposed amplifier (solid) and prior art amplifier (dashed).

side MOSFET. Knowing the voltage over the parasitic capacitance the drain source voltage of the MOSFET and the soft switching factor can be found using (13) and (23). Fig. 10(c) and 10(d) show improved soft switching capabilities in the proposed amplifier as ZVS and RVS are achieved for a larger duty cycle span. The measurements corresponds very well with predictions derived from (13), (16) and (23). The amplifiers are effectively hard switching at a soft switching factor of $V_P = 0$ % and for the prior art amplifier this limit is found to be at 55 % duty cycle while for the proposed amplifier it is at 75 %. The measurements are performed for the high side MOSFETs, while by assuming symmetry in the power stage design, they are equally valid for the low side MOSFETs.

3.3 Operating temperature

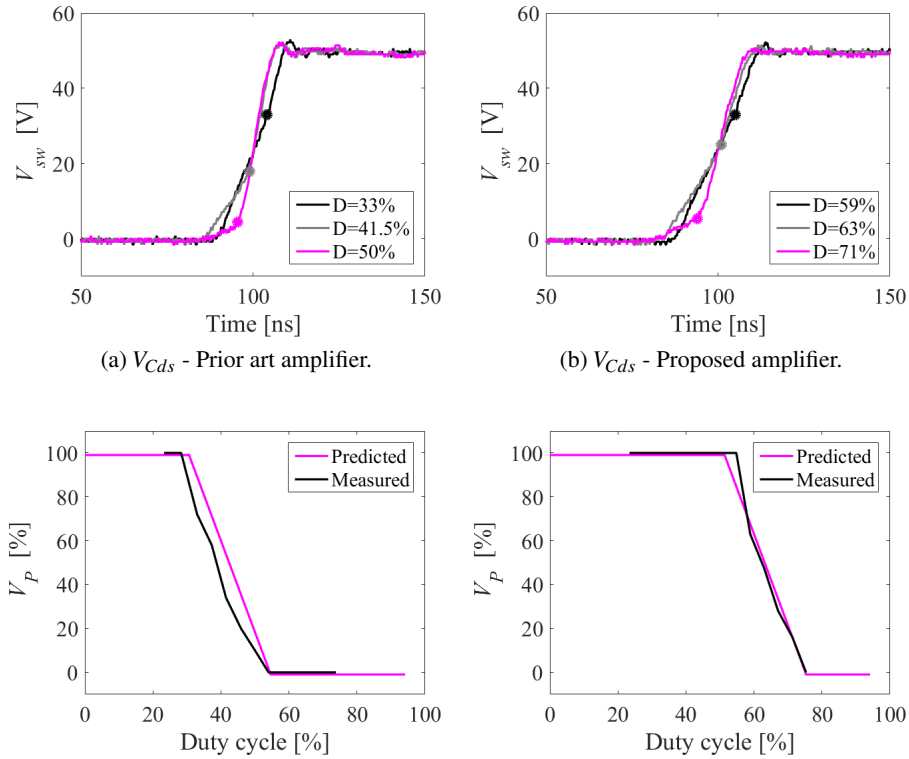
The operating temperature is measured when using a dynamic test signal, representing audio [22], and sine waves. Measurements were performed with the T650 SC thermal camera from FLIR. To ensure steady state conditions measurements was performed after 20 minutes of continuous operation. Fig. 11(a) and 11(b) show thermal pictures of the two amplifiers at full power using the dynamic test signal. The temperature of the switching MOSFETs are strongly reduced in the proposed amplifier ($\Delta T_{1-4} \approx 45°$C) while the output filter temperature is increased ($\Delta T_{5-6} \approx 13°$C) due to higher inductor losses. In addition to this the inductors are now the temperature hotspot in the amplifier with $T_{5-6} \approx 64°$C which is a reduction of 35°C. Fig. 11(c) and 11(d) show thermal pictures of the two amplifiers at a relative high power level, $P_{out} = 85$ W, using a sine wave signal. Is is seen that the temperatures of the switching MOSFETs are reduced in the proposed amplifier design ($\Delta T_{1-4} \approx 15°$C). This temperature reduction is less than observed for the dynamic test signal. This is expected as the switching strategy of the proposed amplifier is mainly designed for improving the switching losses for real audio signals as illustrated in Fig. 7. However a clear improvement is still observed.

4 Conclusion

This paper has described the main challenge to overcome in order to achieve high power density audio amplifiers. This is management of the power dissipation within the switching power stage. A thorough analysis of the inherent loss mechanisms in switch-mode audio power amplifiers and their relation to the amplifier input signal has been presented. A new switching strategy, based on a high inductor ripple current, to improve soft switching capabilities of the switching devices has been proposed. The high inductor ripple current is realized when designing the output filter with a high quality factor. Though this design method improves the soft switching capabilities the frequency response of the amplifier is affected as a significant resonance is introduced. However, this is compensated with the use of full state control.

Two amplifiers were implemented to verify that the presented switching strategy in fact reduces the power dissipation in the MOSFETs. One amplifier utilizing conventional switching strategy and the other one the proposed. Both amplifier were capable of delivering 100 W into 8 Ω with a 32.5 dB gain and power densities of 6 W/cm^3. Measured results showed that the soft switching capability was improved when using the proposed switching strategy. This was especially evident when amplifying signals with dynamic properties similar to real audio as thermal pictures revealed a temperature reduction of 45 °C on the switching devices and a 35 °C reduction of global hotspots. Even for sine wave operation at 85 W a temperature reduction of 15 °C was measured. The proposed method causes higher inductor losses. However, as the heat capacity of the inductors are much larger than that of the small MOSFET packages this does not give rise to thermal issues. The proposed method ensures that the power dissipation is spread more evenly between the MOSFETs and the filter inductors when compared to the prior art methods. Moreover, the implemented amplifiers showed excellent THD+N levels, down to 0.03 %.

The authors believe that by applying the proposed switching technique combined with full state control power densities of 10 to 20 W/cm^3 are a realistic future scenario.



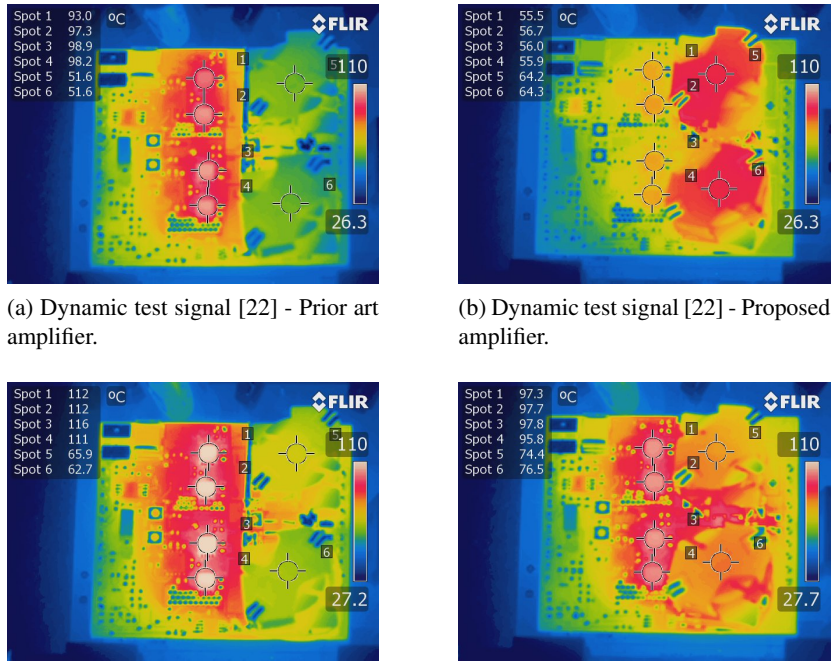
(a) V_{Cds} - Prior art amplifier.

(b) V_{Cds} - Proposed amplifier.

(c) V_P - Prior art amplifier.

(d) V_P - Proposed amplifier.

Figure 10: Measured soft switching capabilities.



(a) Dynamic test signal [22] - Prior art amplifier.

(b) Dynamic test signal [22] - Proposed amplifier.

(c) Sine signal - Prior art amplifier.

(d) Sine signal - Proposed amplifier.

Figure 11: Temperatures of amplifiers after 20 minutes of operation. a) and b) uses dynamic test signal [22] at 300 Hz (P_{out} = 7.5 W). c) and d) uses 1000 Hz sine (P_{out} = 85 W). Spot 1 to 4 are switching MOSFETs and spot 5 and 6 are output filter inductors.

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THE AUTHORS

Niels Elkjær Iversen

Nicolai J. Dhal

Arnold Knott

Michael A. E. Andersen

Niels Elkjær Iversen is a Ph.D student at the electronics group at the Technical University of Denmark, Kongens Lyngby, Denmark. He received his M.Sc degree in December 2014. His research interest include electrical aspects of audio such as switch-mode power audio amplifiers, measurement techniques and transducer modelling.

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Nicolai J. Dahl is an Electrical Engineering student at Technical University of Denmark where he started in 2013. His main focuses in his studies are: control theory, audio electronics and signal processing and he has since early 2014 continuously worked with class D amplifiers and their power supplies. Currently Nicolai working on his M.Sc. degree specializing in control theory for automation.

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Arnold Knott received the Diplom-Ingenieur (FH) degree from the University of Applied Sciences in Deggendorf, Germany, in 2004. From 2004 until 2009 he has been working with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications. In 2010 he earned the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark working on a research project under the title ”Improvement of out of band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology”. From 2010 to 2013 he was Assistant Professor and since 2013 Associate Professor at the Technical University of Denmark. His interests include switch-mode audio power amplifiers, power supplies, integrated circuit design, transducers, radio frequency electronics and electromagnetic compatibility.

●

Michael A.E. Andersen received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark. Since 2009, he has been Deputy Head of Department at the Department of Electrical Engineering. He is the author or coauthor of more than 300 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers