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Highly Efficient EV Battery Charger Using Fractional Charging Concept with SiC Devices

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***Abstract*—This paper describes the implementation of the fractional power conversion concept for use in an on-board charger for Electric Vehicles (EV). High gain step up topologies are required and an efficiency analysis of the full bridge boost converter is made. A comparison of many power devices including Si, GAN and SiC devices concludes that SiC devices are well suited for this application. Using loss equations and battery charging characteristics the converter is optimized for low loss in a full battery charge cycle. Switching-average methods model the small signal characteristics and a PI controller is implemented. The fractional charging configuration results in a very high current gain. A $100\,\mathrm{kHz}$ prototype was tested on a $300\,\mathrm{V}$ EV battery, achieving a converter efficiency of 97.6%. For a $400\,\mathrm{V}$ battery the charger can charge $4\,\mathrm{kW}$ at more than 98% efficiency. The power density of the charger is $3.6\,\mathrm{kW/L}$.**

***Index Terms*—Battery chargers, DC-DC power converters, Control system analysis, Control theory, Design optimization**

I. Introduction

The number of electric vehicles (EVs) in the world is rapidly increasing, due to their environmental advantages, increasing attractiveness and governmental initiatives. However, electric vehicles still have several challenges such as limited range, high cost, slow charging and limited charging opportunities in cities. Increasing the EV battery charger efficiency and decreasing the size can help increase the charging rate and reduce the cost. This can boost the transition to electric cars and has become a hot research topic.

Several converters with comparable specifications to the one in this paper is found in existing literature. [1] lists a few relevant converter prototypes: [2] [3] [4] [5] [6], while some other are discussed in: [7] and [8]. These converters all have peak efficiencies in the range from 96% to slightly below 98%.

In the fractional charger concept, the power flowing into the converter is only a fraction of the power flowing into the battery (Fig. 2). This is different to the conventional configuration where all the power flows through the converter as seen in Fig. 1.

The principle of fractional charging is not new [9], but is getting increased attention. Previous published research have documented the benefits of this configuration, i.e. the efficiency improvement and reduction of power that flows through converter [10] [11] [12].

The charger presented here take advantage of the fractional charging concept and proposes it as a solution for on-board EV chargers. It is both highly efficient, and allows for the DC/DC converter itself to have a lower power rating than the battery charging power. This makes it possible to use a smaller and cheaper converter, and to reduce the amount of power loss and heat generation.

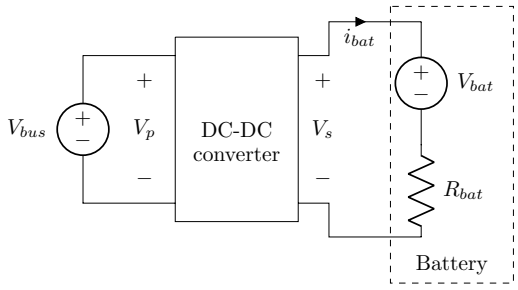

Fig. 1. Conventional Charging Configuration

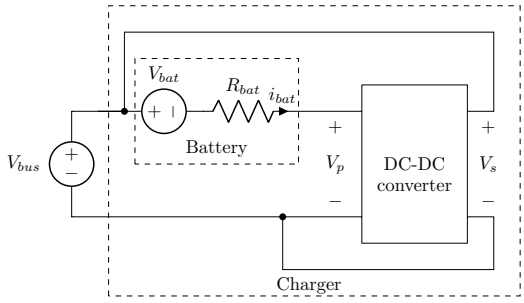

Fig. 2. Fractional Charging Configuration

II. System Description

The specifications of the charger is given in Tab. I. This implemented prototype is designed to be able to charge the battery pack of a *Tesla Model S* and from a DC bus with the voltages that come from rectified 3-phase EU mains. The prototype is designed to have a smaller power rating than most other onboard chargers as this simplifies testing in the laboratory.

TABLE I
CHARGER SPECIFICATIONS

Symbol	Parameter	Rated Value
V_{bus}	DC-bus voltage	$[489\,\mathrm{V}, 566\,\mathrm{V}]$
V_{bat}	Battery voltage	$[288\,\mathrm{V}, 403\,\mathrm{V}]$
i_{bat}	Battery current	$10\,\mathrm{A}$
$P_{battery}$	Battery charging power	$4.0\,\mathrm{kW}$
$P_{converter}$	Converter power	$2.8\,\mathrm{kW}$
Δi_{bat}	Peak-to-peak ripple	$1.0\,\mathrm{A}$

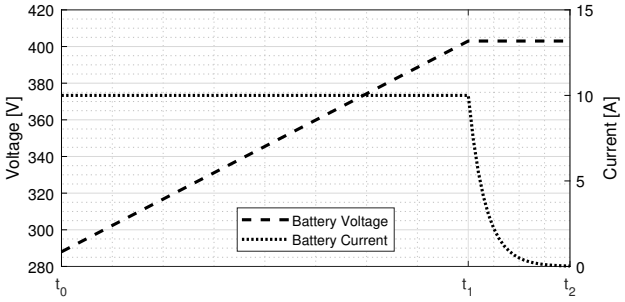

Fig. 3. Battery current and voltage during charging

A. Fractional Battery charging

The conventional charging configuration in Fig. 1 has the battery in parallel with the converter. This means that all the power that is used to charge the battery has to pass through the power converter and $V_s = V_{bat}$. In the fractional concept in Fig. 2, the battery is placed in series with the converter. This makes it possible to charge with a lower converter input voltage, $V_p < V_{bat}$, while maintaining the desired battery current and voltage, resulting in a lower power flow through the converter than the battery. This assumes that the battery voltage is lower than the bus voltage, $V_{bat} < V_{bus}$. Also, the battery voltage should be larger than half the bus voltage $V_{bat} > \frac{1}{2}V_{bus}$ for this configuration to be advantageous. Otherwise, the converter power will be higher than the battery charging power, which is inefficient.

The battery charging profile has constant current for most of the charging and constant voltage with a decaying current in the end of the charging cycle, shown in Fig. 3. The converter is assumed as a current source for design and testing purposes as this is how most of the energy will be charged to the battery.

B. Efficiency Improvement

As mentioned, the power flowing into the converter primary side, $P_{converter}$, is only a fraction of the power flowing into the battery, $P_{battery}$. This relation is given in (1) and the efficiency improvement compared to a conventional charger is given by (2). Here $\eta_{charger}$ is the efficiency of the entire charger system, while $\eta_{converter}$ is the efficiency of the DC-DC converter. These equations show that the fractional charging configuration is most feasible compared to the conventional configuration when the k in (2) is low. This happens when the battery voltage is slightly lower than the bus voltage. If the bus voltage is much greater than the battery voltage, the advantage of this configuration diminishes.

$$k = \frac{P_{converter}}{P_{battery}} = \frac{V_{bus} - V_{bat} - R_{bat}\, i_{bat}}{V_{bat} + R_{bat}\, i_{bat}} \approx \frac{V_{bus} - V_{bat}}{V_{bat}} \tag{1}$$

$$\eta_{charger} = \frac{1}{1 + k \cdot (1 - \eta_{converter})} \tag{2}$$

C. Power Density Improvement

According to (1) the power rating for a DC/DC converter used in the fractional concept can be much lower than that of a conventional configuration with the same charging power. This means that smaller converters can be designed, improving the power density of the system significantly.

D. Topology and Voltage - Current Relationships

The battery current i_{bat} is what needs to be controlled, and this is achieved by adjusting the duty cycle of the converter. As seen in Fig. 2 the secondary side voltage of the converter is fixed to the bus voltage, $V_s = V_{bus}$. Thus, the volt-second balance in the converter makes the primary side voltage, V_p, change as a function of the duty cycle. The change in V_p causes a change in the voltage across the battery, which changes the battery current. A positive change in duty cycle decreases V_p which increases the battery charging current i_{bat}. Furthermore, the current drawn from the DC bus will be lower than the charging current, as some current is fed back from the converter.

An important difference to the conventional configuration is that a step-up rather than a step-down converter is needed as the voltage at the primary side of the converter will be lower than the secondary side. Another difference is that the primary and secondary side will not be isolated as the two ground leads are connected. Nevertheless, isolated converter topologies such as Dual Active Bridge (DAB) and Full-Bridge Boost (FBB) were considered as they can achieve high efficiency at high voltage gains. The FBB in Fig. 4 was selected as it has been proven to achieve a high efficiency at very high voltage gains [13], and as the topology have an primary side inductor which makes it easy to control the battery current. Also, the hard-switching control scheme is simple and lends itself to a very broad efficient operating range .

The relationship between the secondary side and primary side voltage in a FBB is given by (3), where $n = \dfrac{n_s}{n_p}$ is the transformer turns ratio and d is the inductor duty cycle. Eg. the ratio of time where the inductor current increases to the inductor current period. The primary side and battery voltages can be found from this relationship combined with KVL in Fig. 2. $V_p = V_{bus}\,\frac{1-d}{n}$ and $V_{bat} + i_{bat}\,R_{bat} = V_{bus}\,(1 - \frac{1-d}{d})$,

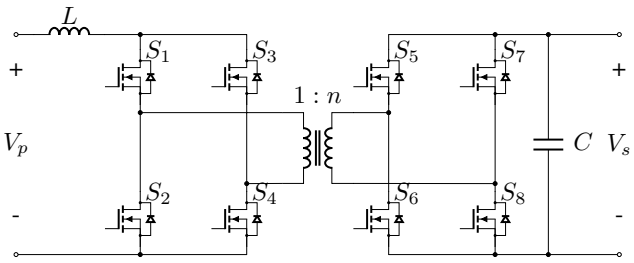

Fig. 4. FBB converter with synchronous rectification

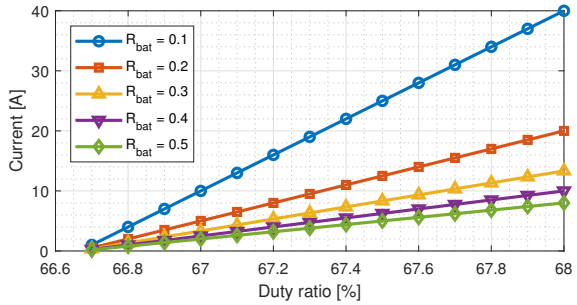

Fig. 5. The resulting steady-state current for small variations in duty cycle with five different battery series resistance values. $n = \frac{10}{6}$, $V_{bat} = 400$, $V_{bus} = 500$.

with the assumption that R_{bat} is the dominant resistance in series with the battery current. This leads to the expression for the battery current given in (4). This expression is extremely sensitive to variations in duty cycle. If the actual duty cycle of the converter deviates slightly from the theoretical one, the steady-state battery current will be much different than anticipated. Fig. 5 illustrates the current sensitivity to duty cyle with different equivalent series resistances, R_{bat}.

$$\frac{V_s}{V_p} = \frac{n}{1-d} \tag{3}$$

$$i_{bat} = \frac{V_{bus}\left(1 - \frac{1-d}{n}\right) - V_{bat}}{R_{bat}} \tag{4}$$

III. Design Considerations

For design purposes, the FBB converter must operate as a current source which makes it undesirable to have large capacitors at the primary side. This, and the fact that the secondary side is connected to the bus makes it possible with few capacitors. Furthermore, as the battery voltage V_{bat} approaches the bus voltage V_{bus}, the voltage gain $\frac{V_s}{V_p}$ approaches infinity. This means that potentially very large voltage gains are required, and that there is an upper limit to the ratio $\frac{V_{bat}}{V_{bus}}$.

Efficiency, rather than power density was the priority during the design phase. First, an optimization was done in the transistor selection. Afterwards, the ideal switching frequency was estimated in order to minimize the energy loss for an entire charging cycle. The power loss formulas used are given in Tab. II.

TABLE II
Equations for estimation of power loss

Description	Expression
Primary side conduction loss	$4\, I_{p\,rms}^2 R_{DS\,ON}$
Primary side switch loss	$2\, f_{sw}\,(Q_g V_{GS} + W_{oss} + (i_{bat} - \frac{\Delta i}{2})\,\frac{V_s}{n}\,t_{rise} + (i_{bat} + \frac{\Delta i}{2})\,\frac{V_s}{n}\,t_{fall})$
Secondary side conduction loss	$4\, I_{s\,rms}^2 R_{DS\,ON}$
Secondary side switch loss	≈ 0 (Active rectification)
Inductor conduction loss	$I_{bat\,DC}^2 R_{L\,DC} + I_{bat\,AC}^2 R_{L\,AC}$
Inductor core loss	≈ 0 (DC current $\gg$ AC current)
Primary side winding loss	$I_{Tp\,rms}^2 R_p$
Secondary side winding loss	$I_{Ts\,rms}^2 R_s$
Transformer core loss (iGSE [14])	$\frac{1}{T}\int_0^T k_i \lvert\frac{dB}{dt}\rvert^\alpha (\Delta B^{\beta-\alpha}) dt$, $k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}\lvert cos(\theta)\rvert^\alpha \cdot 2^{\beta-\alpha} d\theta}$

A. Transformer Turns Ratio

According to Tab I, the maximum DC-bus voltage V_{bus} is 566 V. At the lowest battery voltage $V_{bat} = 288$ V, the maximum converter input voltage is found as (5), resulting in a minimum converter voltage gain $\frac{V_s}{V_p} \approx 2$. The maximal gain is found in the same manner at the lowest bus voltage with the highest battery voltage, giving $\frac{V_s}{V_p} \approx 6$.

$$V_{p,max} = V_{bus,max} - V_{bat,min} = 566\,\text{V} - 288\,\text{V} = 278\,\text{V} \tag{5}$$

As the minimum gain of the FBB converter in equal to the transformer turns ratio n, the turns ratio must be slightly less than 2, to comply with the minimal gain constraint. The turns ratio $\frac{10}{6} = 1.67$ satisfies this and is practical for implementation.

B. Selecting FETs

Both Si, SiC and GaN field effect transistors (FETs) were considered, and a junction temperature of 70 °C was assumed. The primary side FETs are expected to have the greatest power loss as this side has higher currents and as the secondary side is a rectifier with close to zero voltage switching. This is because the secondary switches are turned on shortly after their body diodes starts conducting. Thus, the selection of primary FETs is more critical than the selection of secondary FETs. The result from this optimization is shown in Fig. 6, and show that *UnitedSiC's UJC506505K* SiC cascode has the lowest losses for switching frequencies below $\approx$ 200 kHz, while *GaN System's GS66508* is better at higher frequencies. The UJC506505K SiC is selected. Another advantage with this SiC cascode is that it can be driven by a normal MOSFET gate driver. This FET was also selected for the secondary side FETs as it proved to have fast body diode behaviour and high $\frac{dV}{dt}$ capability during tests. Actually the body diode outperformed external anti-parallel SiC diodes (*Rohm SCS304AP*). The switching frequency, f_{sw}, is here defined as the frequency

TABLE III
DESIGN SUMMARY

Part / Parameter	Details
Inductor	Foil wound, 400 µH
Inductor Core	Ferroxcube ER51, 3C92
FETs	8× UJC06505K
f_{sw}	100 kHz
Transformer	Wire wound
Transformer Core	2× Ferroxcube E58, 3C95
Turns ratio n	$\frac{10}{6}$
Box Volume	1.1 L

of each switch. In a Full-Bridge Boost converter, the frequency of the inductor current will be twice of this, i.e. $2\,f_{sw}$.

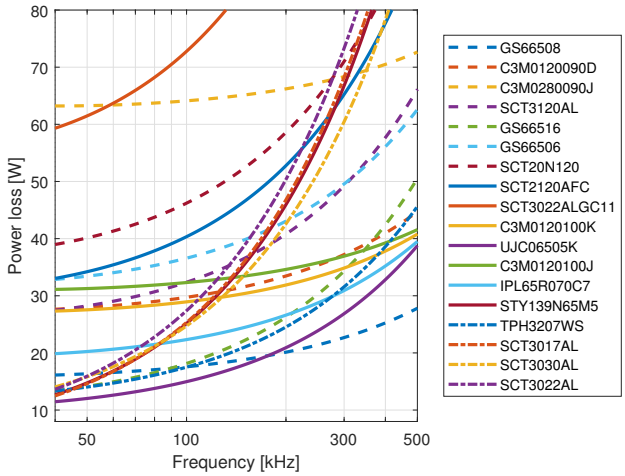

Fig. 6. Estimated primary side FET loss vs. frequency for different FETs

C. Optimizing for Charging Profile and Switching Frequency

When a preliminary design has been made, it is possible to look at how the changing battery voltage during charging affects the converter operation with regards to losses. As the battery voltage increases, the converter will operate with decreasing input voltage. A method for optimizing with regards to both battery charging and frequency is proposed here.

For any steady-state operating point, the converter losses can be estimated using the equations shown in Tab. II. This results in the loss function $P_{loss}(f_{sw}, V_{bat})$, which depends on the switching frequency f_{sw} and the battery voltage V_{bat} and is a sum of the losses at a specific operating point. The function $P_{loss}(f_{sw}, V_{bat})$ is shown for different battery voltages in Fig. 8. Integrating this function from the minimum battery voltage $V_{bat,min}$ to the maximum battery voltage $V_{bat,max}$ with respect to V_{bat} yields a number which can be described as the sum of losses across the entire operating range, or

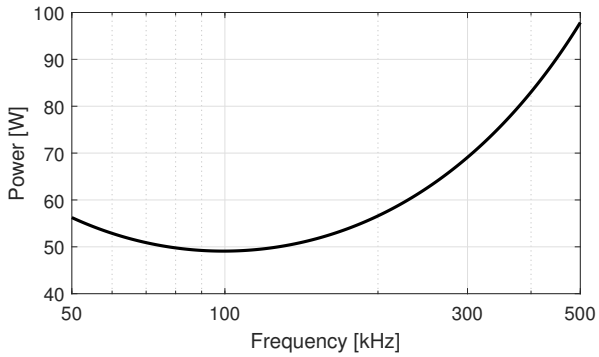

Fig. 7. Calculated average power loss vs. switching frequency during a full battery charging cycle

battery charging cycle. When done numerically, this number becomes very large, depending on how many operating points are included. This makes it useful to divide by the voltage interval between the minimum and maximum battery voltage. The result is a number which can be described as the average power loss across all operating points, or across the entire battery charging cycle. This number eases comparison between different designs, so the the optimal can be found. The mathematical description of this function is in (6). This method assumes that the battery voltage increases linearly with time as the battery is charged.

Because the expressions are frequency dependent, it is possible to sweep across relevant switching frequencies to determine the optimal switching frequency for a specific converter design. For the final design, with a constant battery current of $i_{bat} = 10\,\mathrm{A}$ and battery voltages $V_{bat,min} = 288\,\mathrm{V}$ $V_{bat,max} = 403\,\mathrm{V}$, the estimated average loss versus frequency from (6) is shown in Fig. 7. As shown, the converter is optimized for a switching frequency of 100 kHz.

$$P_{loss,cycle}(f_{sw}) = \frac{\int_{V_{bat,min}}^{V_{bat,max}} P_{loss}(f_{sw}, V_{bat})\, dV_{bat}}{V_{bat,max} - V_{bat,min}} \tag{6}$$

The design choices are summarized in Tab. III.

IV. MODELLING AND CONTROL

As seen in Fig. 2 the battery is represented by the Rint model although it does not take the capacitive and inductive effects of batteries into account [15]. This, combined with the fact that any secondary side capacitance will have its independence cancelled by the connection to the bus, makes the model of the charger system a first order one. A small signal model is made in order to design a controller. This model is derived by waveform averaging of the full-bridge boost as done in [16]. Here, the expressions describing the voltage across the inductor gives the differential equation (7).

$$L\,\frac{di_{bat}}{dt} = (V_{bus} - V_{bat} - R_{bat}\,i_{bat})\,d + (V_{bus} - V_{bat} - R_{bat}\,i_{bat} - \frac{V_{bus}}{n})\,(1-d) \tag{7}$$

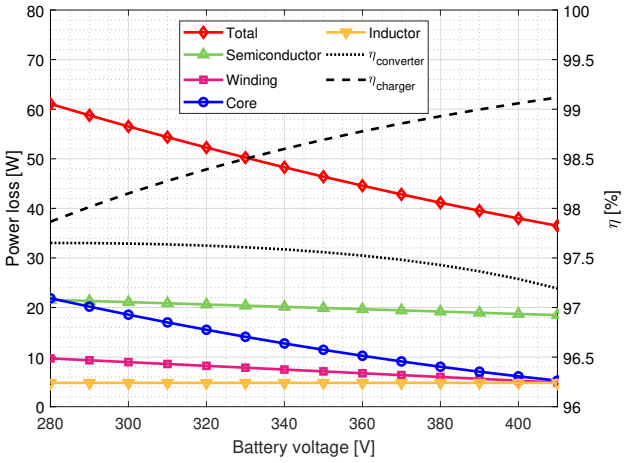

Fig. 8. Estimated power losses for the battery voltages seen during a full charging cycle, $f_{sw} = 100\,\text{kHz}$

A perturbation is added to the duty cycle such that $d = D + \hat{d}$ and the response in battery current will be $i_{bat} = I_{bat} + \hat{i}_{bat}$. By removing the DC terms, this equation is used to create a transfer function G_{id} which relates a duty cycle change to a battery current change (8). It should be noted that this is an approximation which does not include parasitic capacitance and inductance in battery, converter and wires. Furthermore, internal resistances in the converter are here neglected as they are assumed lower than the battery series resistance. Inclusion of these resistances would add an operating point dependent resistance in Fig. 9, which would decrease the DC gain and move the pole of the system to a higher frequency.

$$G_{id}(s) = \frac{\hat{i}_{bat}(s)}{\hat{d}(s)} = \frac{V_{bus}}{n}\frac{1}{s\,L + R_{bat}} \tag{8}$$

(8) can also be represented as an AC equivalent circuit as seen in Fig. 9.

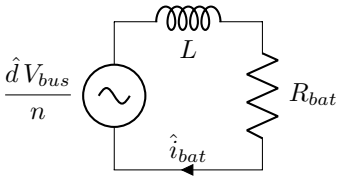

Fig. 9. Small signal model of charger (perturbation in duty cycle to change in battery current)

A. Current Control in Fractional Charging

Som new challenges are specific to the fractional concept, especially the high current gain. As the bus voltage normally is fairly high compared to the battery series resistance, the DC gain of this system will be high, which requires high PWM resolution. If the digital PWM resolution is insufficient, the smallest possible duty cycle change results in a current step of several amperes. Because of this, a high PWM resolution is required to reduce oscillations with the current going between the two nearest current levels.

In this work, a first order PI controller was successfully implemented on a Texas Instruments TMS320f28335 micro-controller unit.

V. Experimental Results

The implemented converter prototype is shown in Fig. 10.

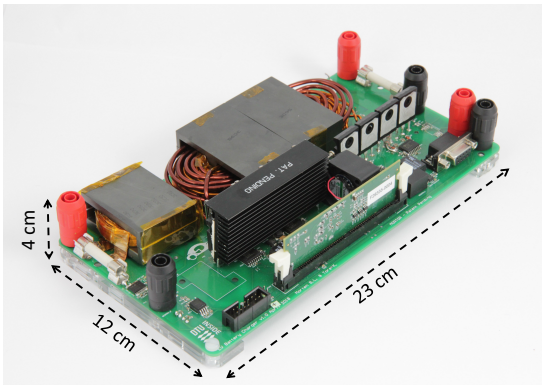

Fig. 10. The converter prototype

A. Efficiency Measurements

Several different variants of the DC-DC converter were tested in a conventional configuration with a resistive load to begin with. Designs with wire wound transformer and planar PCB transformer windings were compared. Different switching frequencies and types or rectification in the secondary side were also tested. These results are shown in Fig. 11, where the blue series mark the final design. The transformer with the PCB windings have low leakage inductance, but caused large switching losses as the terminal capacitance is high. The most efficient design was actually the one with $f_{sw} = 75\,\text{kHz}$, but this resulted in high transformer losses and overheating.

With the final design, a peak efficiency of $\eta_{converter} = 97.6\%$ is achieved at a converter input power of $1.63\,\text{kW}$. And the efficiency stay above 97% for powers between $400\,\text{W}$ and $2.8\,\text{kW}$.

The converter is placed in the fractional charging concept (Fig. 2), and new efficiency measurements are performed while charging an electric vehicle. As stated by (1) and (2), the efficiency improvement due to this configuration depends on the bus and battery voltages. Fig. 12 and 13 show the efficiency measurements for the same battery voltage, but different DC-bus voltages. In Fig. 12 the converter efficiency is almost as high as the charger efficiency because the k factor is close to 1. This shows only a modest improvement with the fractional configuration. In Fig. 13 the charger efficiency is markedly higher than the converter efficiency, as the k factor is much lower than 1. This shows a clear improvement with the fractional configuration, even as the converter itself actually

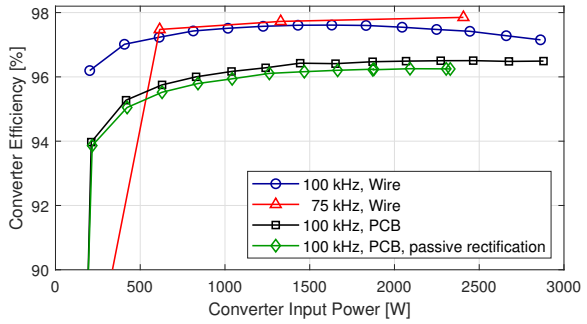

Fig. 11. Converter Efficiency vs. Input Power for different switching frequencies and transformers

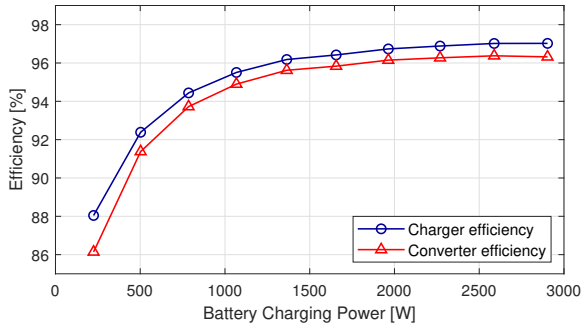

Fig. 12. Converter and charger efficiency vs. battery charging power. $V_{bat} = 273\,\mathrm{V}$, $V_{bus} = 540\,\mathrm{V}$, $k = 0.9$

shows lower efficiency compared to Fig. 12. This is because the converter is operating with a higher gain, further away from its most efficient operating point. This shows that the highest efficiencies will be achieved if the converter itself has a high efficiency at high voltage gains.

B. Converter Waveforms

The most important converter waveforms are shown in Fig. 14, where the converter is in the fractional configuration and charging with 10 A and 3.01 kW. There is seen some ringing on the drain-source voltage for the primary side switches, but a

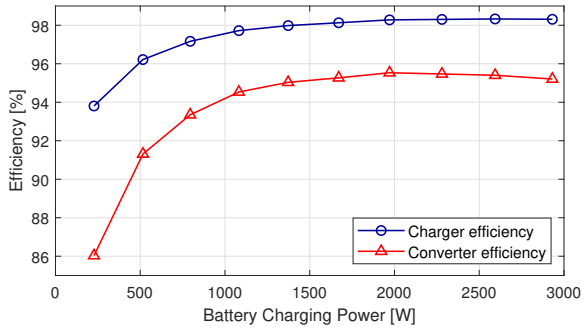

Fig. 13. Converter and charger efficiency vs. battery charging power. $V_{bat} = 273\,\mathrm{V}$, $V_{bus} = 400\,\mathrm{V}$, $k = 0.4$

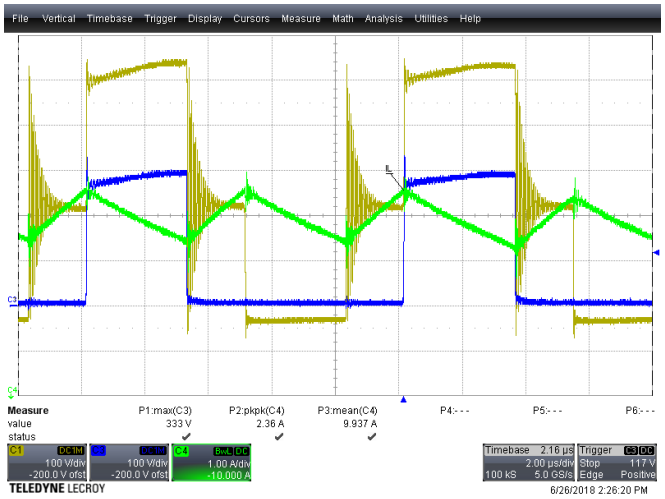

Fig. 14. Converter waveforms. ■: i_{bat} (1 A/div), ■: $V_{DS_{S_2}}$ (100 V/div), ■: $V_{DS_{S_8}}$ (100 V/div), $Bandwidth = 150\,\mathrm{MHz}$

lot more at the secondary side. This MHz-ringing is due to the leakage inductance and causes high losses in the transformer windings.

C. Loss Distribution

Accurately measuring loss distribution can be challenging in power electronics. For this project the loss distribution is estimated using a combination of electrical measurements, thermal measurements and calculated estimates. Firstly, a thermal model of the FETs with mounted heatsink is made, similar to [17], as shown in Fig. 15. This is done by controlling a constant DC current trough the devices and measuring the electrical power and the temperature rise on the shared heat sink with a thermal camera. This gives the thermal resistance $R_{th,priFET}$ of the 4 primary side FETs plus heat sink. The same procedure was used for the secondary side, but without the heat sink, resulting in $R_{th,secFET}$. The switching loss P_{sw} is the difference between the conduction losses P_{cond} and the total loss P_{total}, found as (9) and (10) from the heatsink temperature T_{HS}.

$$P_{sw} = P_{total} - P_{cond} \tag{9}$$

$$P_{total} = \frac{T_{HS} - T_A}{R_{th}}, \qquad P_{cond} = I_{rms}^2 \cdot R_{on} \tag{10}$$

For the secondary side FETs, used for synchronous rectification (SR), the swithing loss is not measured seperately. Inductor losses were estimated based on the measured resistance up to 1 MHz, 5 times the inductor current frequency of 200 kHz, measured with an impedance analyzer. Using a spectrum of the current up to the 1 MHz this gives the inductor loss. This accounts mostly for the copper losses as the core losses can not be measured using small signals. Transformer core losses are estimated using the improved Generalized Steimetz Equation (iGSE) found in Tab. II. Control power for the microcontroller and gate drive is measured from a power

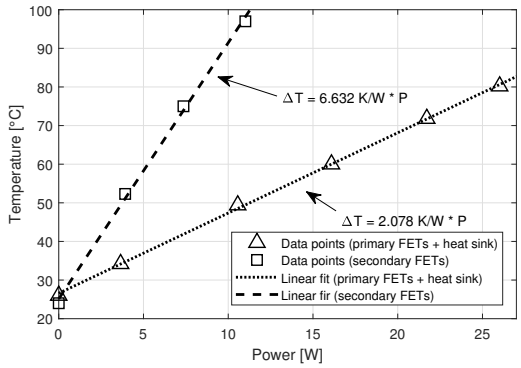

Fig. 15. Temperature versus dissipated power in the FET power devices of the converter and the linear fit used to find the thermal resistance

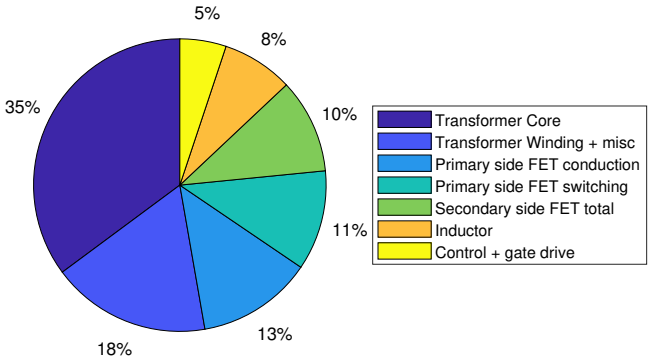

Fig. 16. Measured loss distribution for converter operating at 2.4 kW power, 10 A charging current. Total loss = 60 W

supply. The remaining power is assumed to be mostly copper loss in the transformer windings and various trace losses in the PCB. The resulting loss distribution is shown in Fig. 16. Transformer core loss and winding loss contribute to about half of the total loss. The winding losses are slightly higher than the estimate, which can be caused by high frequency oscillations in transformer current, which would have high losses due to proximity and skin effect.

D. Charging Current Steps

Fig. 17 shows a step in the battery charging current with a rise time of $t_r \approx 0.6\,\mathrm{ms}$. Here the resistance in wires and battery were measured to $R_{bat} = 0.46\,\Omega$. Currents steps were also performed with added resistances to investigate the effect on the system dynamics. The tests were done with total resistances of $R_{bat} = 0.99\,\Omega$ and $R_{bat} = 2.16\,\Omega$, and yielded rise times of $t_r \approx 0.8\,\mathrm{ms}$ and $t_r \approx 1.2\,\mathrm{ms}$ respectively. This verifies that the system response is slowed down by R_{bat} as expected from the AC analysis. However, the system response is overall slower than expected, which might be caused by battery capacitances and inductances which are not modelled.

There are some oscillations in i_{bat} at 20 kHz which corresponds to the control bandwidth. This might be due to the duty cycle resolution of the micro-controller, where the smallest

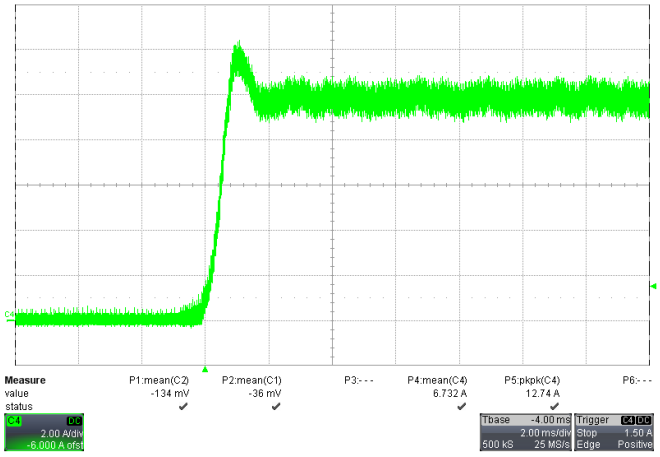

Fig. 17. 0 to 10 A battery current step for $V_{bus} = 540$ volt and $V_{bat} = 272$ volt

step in duty cycle creates a change of more than 1.1 A due to the high DC gain of the system.

VI. Conclusion

This work has demonstrated the fractional charging for EV applications and the efficiency improvements in a fractional charging system, and given insight into modelling and control of such a system. It was found that the first order model presented is usable for controller design, but that it lacked information to describe the much slower rise time of the tested system. Furthermore, an optimization procedure for the design of a highly efficient DC-DC converter is explained.

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