Buried Heterostructure Photonic Crystal Lasers

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Publication date:
2019

Document Version
Publisher's PDF, also known as Version of record

Danmarks Tekniske Universitet

PhD Thesis

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January 31, 2019

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Abstract

Growing interest in integrated optical communications and data processing applications drives the development of ultra-small and energy efficient on-chip photonic components. High performance small footprint laser integrated on silicon is one of the key ingredients in this scheme. As a part of an entire photonic crystal platform for realizing components with required functionalities, lasers based on photonic crystal cavities stand out as rapidly progressing technology.

Majority of demonstrations utilize photonic crystal lasers where the active material is extending across the entire device region. Such structure is far from optimal as heating and absence of carrier confinement degrade device characteristics. The buried heterostructure concept, which is well-known in semiconductor lasers technology, can be implemented with the photonic crystals and address the critical requirements for on-chip applications: device operating speed, output power and energy consumption.

This thesis is focused on the development of buried heterostructure photonic crystal lasers. Critically important material etching and re-growth processes are analysed in detail to increase understanding of involved physical mechanisms. The feasibility and limitations of accurate alignment between formed buried heterostructure regions and photonic crystal cavities are addressed by studying fabrication process-induced distortion of bonded InP-on-Si wafers. Combined all together, high performance optically-pumped photonic crystal cavity lasers with embedded quantum wells active material are realized. Among them the single- and multi-mode buried heterostructure Fano lasers are demonstrated for the first time ever.

The buried heterostructure photonic crystal lasers on Si platform promise exciting opportunities in the future for novel device design demonstrations as well as for photonic integrated circuits applications.

Resumé

En stadig øget interesse i integreret optisk kommunikation og data processerings-applikationer driver udviklingen af ultra små og energi effektive on-chip fotoniske komponenter. Her er lasere med et lille fodaftryk og høj ydeevne integreret på silicium et centralt element. Som en del af en fotonisk krystal platform der kan realisere de nødvendige funktionaliteter fremstår lasere baseret på kaviteter i en fotonisk krystal som en teknologi i kraftig udvikling.

Størstedelen af demonstrationer med fotonisk krystal lasere har aktivt materiale der strækker sig over hele enheden. En sådan udformning er langt fra optimal da opvarmning og fraværet af ladningsbærerindespærring degraderer enhedens karakteristika. En begravet heterostruktur, et koncept der allerede er kendt i halvleder laser teknologi, kan anvendes sammen med fotoniske krystaller og adressere de kritiske behov der er for on-chip anvendelser: enhedens driftshastighed, udgangseffekt og energiforbrug.

Denne afhandling fokuserer på udviklingen af begravet heterostruktur fotonisk krystal lasere. Ætsning og genvækst af materiale er kritisk vigtige processer og de analyseres i dybden for at opnå en forståelse af de underliggende fysiske mekanismer. Realiserbarheden og begrænsningerne i at opnå en præcis placering af både de begravede heterostruktur regioner og herefter kaviteterne i fotonisk krystal adresseres ved en undersøgelse af den forvrængning af bundne InP-på-Si wafere der opstår som følge af fabrikationsprocesserne. Når alt arbejdet kombineres kan optisk pumpede fotonisk krystal lasere med begravede kvantebrønde som aktivt materiale realiseres med en høj ydeevne. Iblandt disse demonstreres enkelt- og multimode begravet heterostruktur Fano lasere for første gang nogensinde.

De begravede heterostruktur fotonisk krystal lasere på Si lover spændende muligheder for fremtidig udvikling og demonstration af nye særskilte enheder og også til anvendelse i integrerede fotoniske kredsløb.

List of Publications

The following publications have been authored or co-authored during the course of the Ph.D. project:

Journal Publications

- ☐ **A. Sakanas**, E. Semenova, L. Ottaviano, J. Mørk, K. Yvind, "*Comparison of processing-induced deformations of InP bonded to Si determined by e-beam metrology: direct vs. adhesive bonding*", *accepted for publication in Microelectronic Engineering*, arXiv:1808.06888 (2018)

- ☐ **A. Sakanas**, K. S. Mathiesen, Y. Yu, E. Semenova, L. Ottaviano, J. Mørk, K. Yvind, "*Single- and multi-mode photonic crystal Fano lasers with the buried heterostructure*", *in preparation*

Conference Proceedings and Contributions

- ☐ **A. Sakanas**, Y. Yu, E. Semenova, L. Ottaviano, H. K. Sahoo, J. Mørk, K. Yvind, "*Fabrication and Experimental Demonstration of Photonic Crystal Laser with Buried Heterostructure*", Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO-EQEC) (2017), pp. 1 – 1

- ☐ J. Mørk, Y. Yu, D. A. Bekele, K. S. Mathiesen, T. S. Rasmussen, E. Semenova, L. Ottaviano, **A. Sakanas**, K. Yvind, "*Photonic crystal Fano lasers and Fano switches*", Proceedings of the 22nd Microoptics Conference (MOC) (2017), pp. 88 – 89

☐ J. Mørk, Y. Yu, D. A. Bekele, K. S. Mathiesen, T. S. Rasmussen, A. Rasoulzadeh, E. Semenova, L. Ottaviano, **A. Sakanas**, K. Yvind, "*Lasers, switches and non-reciprocal elements based on photonic crystal Fano resonances*", Proceedings of the 17th International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD) (2017), pp. 1 – 2

☐ D. A. Bekele, Y. Yu, H. Hu, Y. Ding, **A. Sakanas**, L. Ottaviano, E. Semenova, L. K. Oxenløwe, K. Yvind, J. Mørk, "*Photonic crystal Fano resonances for realizing optical switches, lasers and non-reciprocal elements*", Proceedings of SPIE Optics and Photonics, Active Photonic Platforms IX, vol. 10345 (2017), pp. 103451V-1 – 7

☐ **A. Sakanas**, Y. Yu, E. Semenova, L. Ottaviano, H. K. Sahoo, J. Mørk, K. Yvind, "*Photonic Crystal with Buried Heterostructure Platform for Laser Devices Directly Bonded to Si*", Frontiers in Optics/Laser Science XXXIII (FIO-LS) (2017), pp. 1 – 2

☐ K. Yvind, **A. Sakanas**, Y. Yu, A. Marchevsky, K. S. Mathiesen, H. K. Sahoo, D. A. Bekele, L. Ottaviano, E. Semenova, J. Mørk, "*Photonic crystal lasers on silicon substrates*", SPIE Photonics West, Novel In-Plane Semiconductor Lasers XVII (2018), pp. 1 – 1

☐ **A. Sakanas**, Y. Yu, E. Semenova, L. Ottaviano, H. K. Sahoo, J. Mørk, K. Yvind, "*Investigation of the Expansion in InP layer bonded to Si and its Effects on the Performance of the Photonic Crystal Lasers with the Buried Heterostructure*", Semiconductor and Integrated Optoelectronics conference (SIOE) (2018), pp. 1 – 1

☐ K. Yvind, Y. Yu, E. Semenova, L. Ottaviano, D. A. Bekele, **A. Sakanas**, T. S. Rasmussen, K. S. Mathiesen, J. Mørk, "*Photonic Crystal Fanolasers*", SPIE Photonics Europe (2018), pp. 1 – 1

☐ **A. Sakanas**, Y. Yu, E. Semenova, L. Ottaviano, H. K. Sahoo, J. Mørk, K. Yvind, "*Consequence of Non-Uniform Expansion of InP-on-Si Wafers for the Performance of Buried Heterostructure Photonic Crystal Lasers*", Advanced Photonics Congress (APC) (2018), pp. 1 – 2

□ **A. Sakanas**, Y. Yu, E. Semenova, L. Ottaviano, H. K. Sahoo, J. Mørk, K. Yvind, "*Quantifying non-uniform InP-on-Si wafer expansion with a sub-50 nm precision using E-beam metrology*", 44th International Conference on Micro & Nano Engineering (MNE) (2018), pp. $1-2$

Acknowledgement

This work was carried out at DTU Fotonik, financially supported by the Villum Fonden via the NATEC (Nanophotonics for Terabit Communications) Centre of Excellence.

I wish to thank various people who made this work possible.

Foremost, I am very grateful to my main supervisor Kresten Yvind, who trusted me from the very beginning and whose guidance throughout the entire PhD played very important part for the overall project success. He gave me freedom and inspired me to look for creative solutions, while always providing support and wisdom in difficult situations.

I would also like to express my gratitude to Jesper Mørk and Elizaveta Semenova, my co-supervisors, who had their doors open for me whenever I needed. I highly appreciate their constant support and encouragement.

I really value all the knowledge, insight, inspiration, motivation, patience and friendly atmosphere that Kresten, Jesper and Lisa provided. They became not just my supervisors, but mentors. Working together I gained valuable experience beyond just career.

I would like to thank Luisa Ottaviano, who was my unofficial co-supervisor, for all her help in the cleanroom as well as for her smile and friendly conversations outside of it.

Big thanks to my colleagues Yi Yu and Kristoffer S. Mathiesen, who, besides helpful discussions, helped with sample preparation in the cleanroom and device characterisation in the lab. A special thanks to Kristoffer for his help with translating the abstract into Danish. Tak!

This PhD would not have been possible without the help of DTU Nanolab (Danchip) personnel, their training and support. Daily work was much easier thanks to all helpful DTU Fotonik administration personnel. My thanks also go to colleagues with whom I worked in Natec project.

I am very thankful and feel lucky for all the precious memories with those who were not only my good colleagues, but also good friends outside the office. For healthy balance between work and life. And for always making me look forward to lunch breaks, not only because of food!

We had a fun time working together (if it is fun, it is not work, right?) with DTU-Lys student chapter as well as an entire IONS Scandinavia team. What we managed to do together is truly amazing, and I will always feel proud of being a part of such an awesome group of people.

I also want to thank everyone who made working at DTU so memorable: those who were waking up early on Friday mornings to play football; those who I could join for weekly runs; those who were always there for a good coffee break and those who I could relax with in Friday bar.

Finally, I am very grateful to my family for teaching me the value of hard and honest work, and my lovely wife for her continuous encouragement to stay positive, open-minded and always move forward.

Contents

1 Introduction

> *It doesn't matter what you do... so as long as you change something from the way it was before you touched it into something that's like you after you take your hands away.*
>
> — **Ray Bradbury**
> Fahrenheit 451

Since the earliest human attempts to transmit information over long distances using fire, up to this day and its most advanced technologies, the basic need for communication has not changed. Only the methods have. Sending signals as far and as fast as possible has been the main focus for a very long time. In today's communication age, with enormous amounts of data circulating around the world, efficiency and low energy consumption is becoming one of the most important factors for further technological development. As paradoxical as it sounds, present-day long-distance communication critically depends on the information transmission efficiency over the shortest distances.

This work contributes to current research trying to improve short-distance communication by developing novel integrated laser devices. This work is about photonics!

1.1 The big picture

The importance of silicon-based integrated circuits for the global development during last decades cannot be overemphasized. Immense investments and man-hours advanced the technology making it the foundation on which further progress in many areas depends. ICT, information and communications technologies, perfectly illustrate how rapid and life-transforming advancement this has been. Naturally, new problems emerge

on the way requiring creative solutions to move further. This time, the challenge seems to be so fundamental, that drastically new measures have to be taken to tackle it.

The continuous shrinking of circuit sizes and increase in transistors count have been indistinguishable features of integrated circuits during last decades. However, such rapid technological development is starting to reach its fundamental limits [1]. While smaller transistors do reduce energy-per-bit for logic operations, the energy that is used to move data inside information-processing machines does not scale down in the same way [2]. Thus, the source of energy dissipation is gradually shifting from logic operations to electrical interconnections, while efficient removal of heat is becoming a more and more complicated task. At the same time, the limited capacity of electrical wires makes it difficult to keep up with increasing data transfer rate requirements, and potential solutions for reducing signal distortion and loss add significant design complexity and power [3].

Power dissipation by electrical interconnects in modern microprocessors is substantial and is expected to grow with further scaling-down of complementary metal–oxide–semiconductor (CMOS) technology nodes. According to one estimate [4], interconnects contributed to over 50% of dynamic power consumption (the sum of switching power and short-circuit power) at the 130 nm node (industry standard approximately during years $2001 - 2002$) in a microprocessor designed for power efficiency. A more recent study addressed the issue of over-estimating the power consumption and proposed a distance-based microbenchmarking [5]. With this approach data access power was separated out from data movement power, indicating the more conservative dynamic interconnects power dissipation estimate of 14% in a graphics processing unit (GPU) built in the 28 nm technology (used in between 32 and 22 nm nodes from 2011), possibly increasing to 22% in the 7 nm node (commercial mass production began in 2018 and is expected to be replaced by 5 nm process around $2020/21$). Isolating and estimating power dissipation from electrical interconnects alone is a complicated task, nevertheless it is generally believed to be an increasingly serious issue for future information-processing systems.

To understand the magnitude of power dissipation by interconnects in integrated circuits and its influence on ICT, consider it from the perspective of data centres. These are very large scale data storage and computing

infrastructures which possess high economic, environmental and performance impact. Recent in-depth study of energy consumption by data centres tries to summarize and compare some of the important data figures of various components [6]. According to this study, a major share of the total power of a server is consumed by the central processing unit (CPU), and depending on configuration can range from 30 to 60%. The same study shows that together servers and storage make up a quarter of the total energy consumption in the data centre facility, while at the same time an overwhelming 50% is attributed to the facility cooling. The international technology roadmap for semiconductors (ITRS) [7] estimated considerably less power was spent for cooling an ordinary data centre in 2015. However, its growing contribution to the total power consumption by the data centre from $\sim$ 5% in 2015 to almost 25% by 2029 was recognized. Meanwhile, global electricity consumption by data centres is expected to increase from $1.1-1.5\%$ ($1.7-2.2\%$ in the US) in 2010 [6] to $3-13\%$ by 2030 [8]. While these are big numbers by themselves, data centres constitute really only a part of the ICT, which is expected to boom in the near future and in the worst case scenario could consume one fifth of global electricity in the beginning of next decade, or in a more realistic case by 2030 (Fig. 1.1). Besides global energy consumption of different ICT sectors, considerable

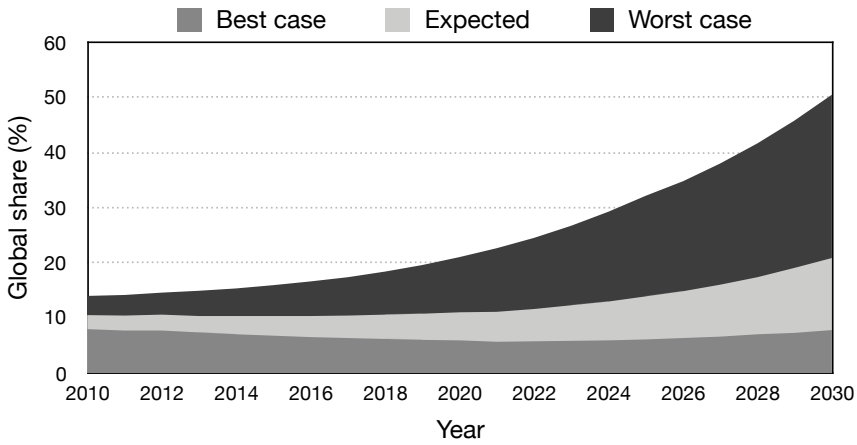


Fig. 1.1.: Share of information and communications technologies of global electricity usage for years 2010 - 2030. Adapted from [8].

carbon footprint is also recognized [8, 9]. ICT accounted for roughly 1.7% of the total CO_2 emissions in 2012 and are steadily growing.

All in all, while due to multiple factors it might be hard to precisely estimate the power dissipation due to electrical interconnects in the CPU just as much as the ICTs global energy consumption, even the most conservative approach reveals that the energy saving potential by improving interconnects in communications is enormous. Emerging photonics technologies aim at addressing these issues while bringing additional benefits.

1.2 From electrical to optical interconnects

Just as optical fibres have undertaken the role of long-distance communication channels from electrical cables, the idea of using optical interconnects within otherwise electronic information-processing machines has been long recognized [10, 11], with one possible implementation into integrated circuits represented in Fig. 1.2.

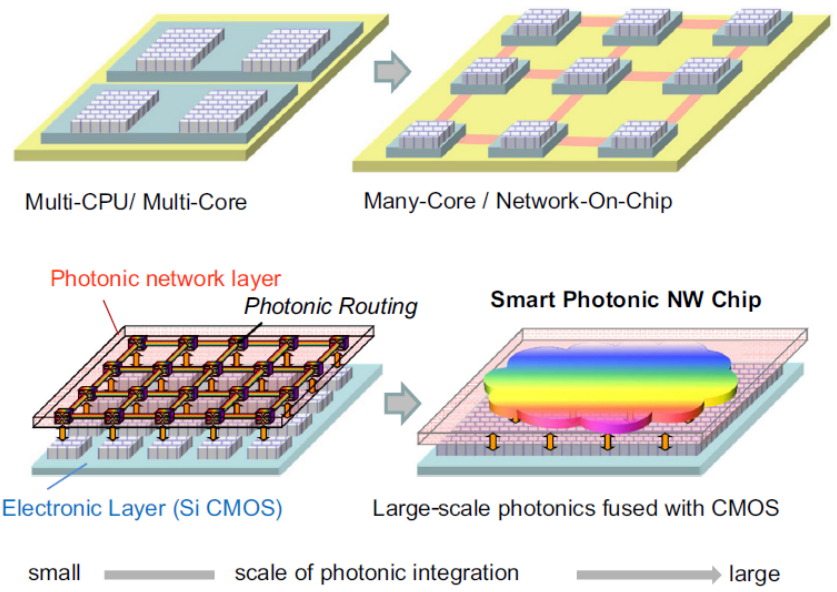


Fig. 1.2.: Envisioned future co-integration of electronics and photonics in integrated circuits. Reprinted from [12].

Underlying differences between optics and electronics is the carrier frequency ν, free-space wavelength λ and photon energy E_p (choice of

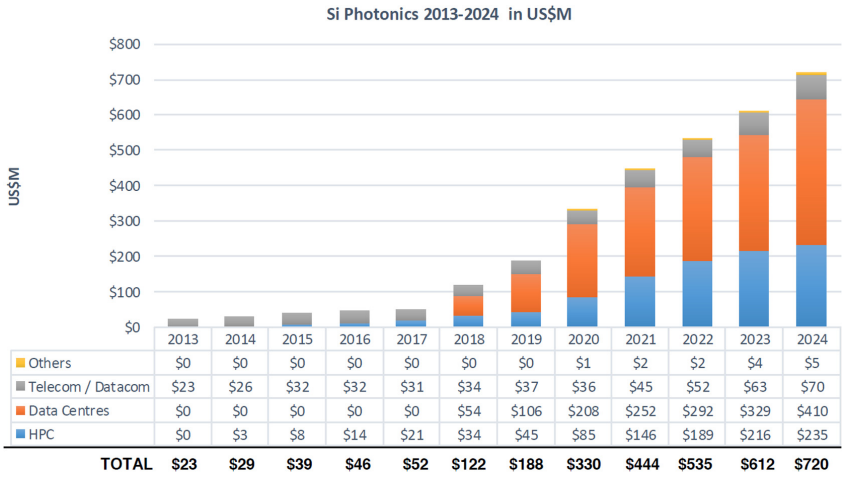
Tab. 1.1.: Fundamental differences between optics and electronics for communication. Adapted from [13].

	Optics	Electronics
Frequency	$200 - 1000$ THz	10 MHz -10 GHz
Wavelength	$1500 - 300$ nm	30 m -3 cm
Photon energy	$0.8 - 4$ eV	40 neV -40 ueV

one of them uniquely defines the other through the relations $\lambda = c/\nu$ and $E_p = h\nu/q_e$, where h is Planck's constant, q_e is the electron charge and c is the speed of light), compared in table 1.1. As the direct consequence, optics can offer practical advantages regarding interconnect density, signal loss and distortion at high modulation frequencies, interference and cross-talk as well as clock and signal timing, summarized in detail by Miller [13].

Importantly, comparison between optical and electrical interconnects indicate the potential for reduced energy consumption with optics [11, 14, 15]. Recently, Miller proposed more concrete research targets for optical devices and their systems that should be met in order for optics to be competitive with current and near future electrical interconnect technology on energy grounds alone [2, 3]. The analysis suggests 10 fJ or lower total energy per bit requirement for 1 cm -10 m interconnects, which currently consume in the range of picojoules or larger, with optoelectronic device operating energies in that case reaching sub-femtojoule or attojoule levels. While these targets are aggressive and not yet commercially viable, Si photonics technologies are now being widely recognized as key technology in future generations of communications systems and data interconnects with a strong research and industrial interest [16–20]. Commercial products involving integration of Si photonics is already starting to be deployed in some data centres and for the high-performance computing (HPC) applications on the backplanes and busses between boards. It is expected that Si photonics will provide connection on the smaller scale between chips or even on chips in the near future, following the market growth (Fig. 1.3).

Faster and wider market penetration is significantly slowed down due to current high cost of optical interconnect technologies. Even if energy consumption by interconnects is reduced, electrical wires on chips and boards are very inexpensive to produce, and are essentially free at chip scale. Therefore, it is really a combination of energy benefits and bandwidth improvements that is driving the commercial implementation of optics for interconnections. The most bandwidth-hungry areas such as data



	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Others	$0	$0	$0	$0	$0	$0	$0	$1	$2	$2	$4	$5
Telecom / Datacom	$23	$26	$32	$32	$31	$34	$37	$36	$45	$52	$63	$70
Data Centres	$0	$0	$0	$0	$0	$54	$106	$208	$252	$292	$329	$410
HPC	$0	$3	$8	$14	$21	$34	$45	$85	$146	$189	$216	$235
TOTAL	**$23**	**$29**	**$39**	**$46**	**$52**	**$122**	**$188**	**$330**	**$444**	**$535**	**$612**	**$720**

Fig. 1.3.: Si photonics market forecast for years $2013 - 2024$. Reprinted from [21].

centres and HPCs are naturally expected to be early market adaptors for carrying the technology to the chip-level. As an example, breaking through limited bandwidth and packaging constraints for exascale computing applications would anyway require implementation of expensive and exotic solutions using contemporary electrical technologies, which may force a movement towards optical links [22].

At the core of the optical interconnect technology problem are photonic devices capable of meeting targets of extremely low energies. The international roadmap for devices and systems (IRDS) [23], which was established in 2016 as the successor to the ITRS, lists the device technology needs for integrated lasers, modulators, multiplexers/demultiplexers, photodetectors and single-mode connectors. Innovative solutions for each component are crucial in delivering complete and efficiently functioning optical interconnects technology.

1.3 Small-footprint lasers for on-chip communications

Perhaps the largest technological challenge in addressing energy cost and limited bandwidth issues associated with current interconnects is the development of compact, low power and high output integrated lasers [23]. In order to appreciate the difficulties in meeting requirements imposed

on the device, it is useful to consider two simple expressions for energy requirements[1]:

- ☐ definition of the average energy required to transmit 1 bit (assuming that transmitting "0" value does not cost anything) given the data transmission rate:

$$\text{Energy cost / bit} = \frac{1}{2}\frac{I_\text{b} \cdot V_\text{b}}{\text{Data rate}} \tag{1.1}$$

  where I_b and V_b are laser bias current and voltage, respectively;

- ☐ device average operating energy related to carrier injection considering physical principles:

$$\text{Energy cost} \approx \frac{1}{2} T_\text{bit} \cdot \frac{N_\text{th}}{\tau} \cdot q_\text{e} \cdot V \cdot \text{Active volume} \tag{1.2}$$

  where T_bit is the bit transmission time, N_th and τ is the threshold carrier density and lifetime, q_e is the electron charge and V is the driving voltage. Whole expression is multiplied by $1/2$, again assuming that transmitting "0" value does not cost anything. For high speed, lasers are operated far above the threshold [24], thus an additional multiplying factor (>1) could be included.

The value of these expressions is that the order of magnitude for operating energies can be easily estimated and necessary intuition can be gained with regard to laser parameters. Considering as an example a hypothetical semiconductor laser with the active volume of $(1\ \mu\text{m})^3$, the energy involved in running it under the injection of 10^{18} cm^{-3} carrier density (corresponding to the population inversion of 10^6 carrier pairs) would be approximately 160 fJ (Table II in [2]), as given by Eq. 1.2. When operated at the bias point of 500 μA and 2 V with the modulation rate of 10 Gbit/s, such laser would consume 100 fJ/bit energy for data transmission (Eq. 1.1). In addition, the electrostatic energies associated with the necessary voltage swing across the device should also be considered, as discussed in detail in [2]. The conclusions are that compact laser devices are not just desired for dense on-chip integration, but they are necessary in order to achieve low operating energy values for optical interconnects. Thus, approaching

[1] Valid only in the lasing regime.

sub-femtojoule or attojoule device operating regime discussed in section 1.2 requires significantly smaller active volume than $(1\ \mu\text{m})^3$ (while still maintaining its high cavity Q-factor) with low bias current (while still keeping the injection current density above the threshold and providing high enough output power), which in principle can only be met by the most radical laser structures.

Considering optical output devices for future on-chip interconnects, a few types of potential candidates emerge. Standard in-plane emitting distributed feedback (DFB) and distributed Bragg reflector (DBR) semiconductor laser structures have unacceptably high operating energies of several picojoules per bit, as can be inferred from parameters given in Tables 2 and 5 from [25] (approximately estimated using eq. 1.1 and assuming typical driving voltage range of $1 - 5$ V). Recent developments of membrane buried heterostructure (BH) distributed reflector (DR) lasers on Si substrate focused on reducing the active region width, while simultaneously increasing the optical confinement factor. With reduced cavity length, the operating energies were lowered to 100s femtojoules range with sub-mW output powers [26–29]. It is possible that these type of lasers will gain popularity for on-chip communications due to their favourable in-plane emission geometries for planar integration if further reduction of the operating energy values and increase in the output powers is achieved.

Employing small active volume, typical GaAs-based short wavelength ($850 - 1060$ nm) and InP-based long wavelength (typically around 1.3 and 1.5 μm) vertical-cavity surface-emitting laser (VCSEL) consumes on the order of 100 fJ/bit (Tables 3 and 4 [25]). On the other hand, smaller active volumes also mean that the output powers are lower than for previously discussed DR lasers. Nevertheless, due to ease of fabrication and low production cost, GaAs-based VCSELs are nowadays widely used for short-distance optical links inside data centres. Being inherently out-of-plane emitting devices, VCSELs enable efficient and low-cost fibre-coupling solutions, and could be envisioned as transmitters in two-dimensional array for free space optical communications (facing another chip with an array of integrated photodetectors), however the downside of this approach is a departure from contemporary planar integrated circuits technology [3]. As a practical alternative, VCSEL designs for in-plane output coupling to Si-based waveguides have been proposed for both short [30] and long [31] wavelength range.

The development timeline of the first truly small-footprint laser devices started with VCSELs in 1970s, and continued further with microdisk, photonic crystal, metal non-plasmon and metal plasmon lasers [32]. Likely for the main reason of being the oldest, VCSEL is so far the only laser type from this group that has been matured enough to leave research laboratories and enter commercial markets. While much younger, the other laser structures are very promising for on-chip future optical communications and are examined next.

Very high Q-factors can be realized in the microdisk, microring, microsphere and microtoroid cavities, which possess whispering-gallery modes circulating around the edge of the structure [33]. Sub-100 μA threshold currents have been demonstrated for continuous-wave microdisk lasers under electrical injection [34], however further reducing structure diameter generally results in increased radiative losses and electrical resistance, making it difficult to achieve high-performance with active volume smaller than for VCSELs. Very low output powers also impede their wider applicability. In general, research interest in developing these type of lasers for on-chip communications seems to be declining, with the focus shifting towards improved modulator designs, such as recently demonstrated sub-fJ vertical junction microdisk modulator [35].

Possibly the largest progress in the shortest amount of time has been achieved for photonic crystal (PhC)[2] laser devices [36, 37]. The first proof-of-concept experimental demonstration of (low-temperature, pulsed) lasing from an air-suspended PhC cavity fabricated in an InGaAsP material platform was reported 20 years ago [38]. Impressive performance in terms of energy efficiency has been demonstrated for a number of consistently improved compact PhC laser devices with the buried heterostructure designed for on-chip optical communications by researchers from the NTT Basic Research Laboratories: optically pumped device with the InGaAsP active region fabricated on an InP platform showed remarkably low 13 fJ/bit transmission energy [39], which was then further decreased to 8.8 fJ/bit [40]. After a couple of years, electrically pumped version of this lambda-scale-embedded active region photonic crystal (LEAP) laser was introduced with the threshold current of 7.8 μA and the energy cost of 14

[2] Correct usage of this term requires stating dimensionality of the structure, whether it is 1D, 2D or 3D. Ambiguity arises because traditional high-reflectivity multilayer thin film structure used in VCSEL is now frequently called 1D photonic crystal. In this work, if not stated specifically, photonic crystals refer to 2D structures for in-plane emission.

fJ/bit [41], and by introducing current leakage-blocking trenches in the structure these values were pushed down once again to 4.8 μA and 4.4 fJ/bit [42]. The most recent demonstration in short cavity LEAP lasers set the record values of 4 μA and less than 1 fJ/bit for any type of semiconductor laser operating at room temperature ever reported [43]. Heterogeneous integration of a LEAP laser coupled to a Si waveguide on a Si substrate has also been demonstrated recently [44]. The reported energy values for transmitting one bit with these lasers come closest to the research targets stated in section 1.2. On the other hand, while the maximum achievable output powers are so far below 10 μW, another promising 1D PhC laser design with an efficient electrical injection scheme was proposed, which demonstrated near-100 μW output power [45]. Thus, the PhC lasers demonstrate great potential for becoming future solution for the integrated optical interconnects technologies. It is also necessary to mention other perspective developments in the field, namely PhC lasers with a nanowire selectively placed onto the cavity [46], with quantum dots as an active material (extending across the entire device layer) [47, 48], or just a single dot inside the cavity [49].

Further miniaturization progress resulted in the development of plasmon and non-plasmon mode metallic lasers [32]. Even though extreme field localization and high intensities are advantageous for specific applications, high losses inherent to metals make it challenging for these lasers to be implemented as light sources for on-chip communications.

To fully benefit from optical interconnect technologies, it is necessary to transmit data at high rates. In communications, two main methods exist for modulating an optical carrier by an electrical signal: external modulation [2, 50] and direct modulation [25, 51]. The comparison of their advantages and disadvantages is given in Table III in [2]. The modulation bandwidth of conventional directly modulated lasers typically lies in the range of few 10s of GHz as limited by the relaxation oscillation (resonance) frequency, which is proportional to the square root of the differential gain and photon density (power), and inversely proportional to the photon lifetime in the cavity [24]. An extensive list of 3-dB bandwidths for various laser designs collected in Table I in [51] reveals that pushing the limit beyond 100 GHz is immensely complicated (and most probably cost ineffective due to complexity involved). Recently, a possibility of frequency modulating a photonic crystal Fano laser with a modulation bandwidth

exceeding 1.5 THz has been theoretically predicted [52]. Thus, seeking for unusual properties in novel types of laser devices might provide new opportunities (beyond basic expectations).

In an attempt to summarize this brief overview and to provide some perspective about which of these promising laser technologies could be chosen for the future on-chip optical interconnections, it is useful to separate them into two groups: (1) more "traditional" DFB/DBR and VCSEL devices need to be further steadily improved until they meet the target requirements; (2) more "exotic" microdisk, photonic crystal and metallic laser technologies need to have serious standardization and reproducibility improvement efforts, so that it would actually be possible to benefit from their superior performance. From this second group, photonic crystals seem so far the most realistic candidates to rival matured device technologies from the first group. The photonic crystal platform also has an additional advantage that no other technology possesses: it allows realizing a wide range of optical components functionalities important for properly functioning on-chip communications [12]. Finally, the possibility of confining light to diffraction-limited volumes and strongly enhancing light-matter interaction at the nanoscale renders photonic crystals as an important technology for fundamental studies in photonics.

1.4 Thesis overview

This work is a contribution to the field of photonic crystal lasers, with the ambition of providing deeper understanding of device physics and technology that could help developing light sources for future on-chip optical communications needs. In particular, the aim is: (1) to develop a complete device processing method that would bring about functioning optically-pumped InP photonic crystal cavity laser with the buried heterostructure heterogeneously integrated on Si substrate; (2) to implement and investigate novel types of photonic crystal designs with Fano mirrors. In addition, (3) to establish and optimize fabrication technique simultaneously producing multiple high-aspect ratio structures that would simplify sample preparation for the atom probe tomography experiments with quantum dots, which are used in active photonic devices.

In photonic crystal laser device processing, two types of active materials are implemented: quantum wells and quantum dots. Quantum wells are

technologically more advanced and easier to fabricate, however quantum dots possess unique features that indicate possibility of improved device performance. Better understanding of those features could be achieved both through implementation into the device structure and detailed characterisation as well as dedicated material analysis using high-resolution techniques such as the atom probe tomography.

The key results and findings of this work are organized and presented in the following order:

Chapter 2 provides essential theory of semiconductor laser structures and photonic crystals, taking the bottom-up approach in basic reasoning behind the photonic crystal cavity designs, material choice for the active-passive platform as well as characteristics of quantum wells and quantum dots used as the active material in the buried heterostructure fabrication as one of the most effective carrier confinement structural designs.

Chapter 3 summarizes the e-beam metrology investigation results of the alignment accuracy achievable for the bonded InP-on-Si wafers. Two types of wafer bonding techniques in three different processing configurations are compared, providing explanation of the observed misalignment in the fabricated laser devices together with realistically obtainable limits and suggesting possible strategies to account for them.

Chapter 4 lists 3 generations of the fabricated buried heterostructure photonic crystal laser devices during the course of this work. Differences between the buried heterostructure and non-buried heterostructure photonic crystal platforms are illustrated, and the optimized fabrication overview is then presented for the 3^{rd} generation buried heterostructure laser device.

Chapter 5 is dedicated to an extended discussion of the material etching followed by the epitaxial re-growth used to form the buried heterostructure regions. These two major processing steps are of key importance for the overall device fabrication success, thus deserving a more detailed look at the physical principles and mechanisms involved.

Chapter 6 shifts the focus from the device fabrication to the experimental characterisation and performance analysis. Results for the low-performance misaligned and high-performance well-aligned quantum wells buried heterostructure devices with the line-defect photonic crystal cavities are presented, along with the first-ever experimental demonstration of the single- and multi-mode Fano buried heterostructure photonic crystal lasers. No lasing was observed from the quantum dots devices, and an attempt is made to explain the possible reasons. Throughout the chapter, characteristics of the measured buried heterostructure photonic crystal lasers are compared with other relevant studies reported in literature.

Chapter 7 is a bonus chapter reporting the side project of this PhD in an attempt to develop a convenient sample preparation method for the atom probe tomography studies of the quantum dots. Innovative pillar-shaped sample dry etching strategy (based on the etching used for the buried heterostructure device fabrication), simultaneously producing a number of specimens is proposed and an optimization process is described.

Chapter 8 is where the conclusions are drawn and the results are put into perspective. Further possibilities are discussed.

2

Device Theory

In this chapter, the most relevant theory of the device "building blocks" is discussed: the transition from conventional semiconductor lasers to compact semiconductor lasers, ordinary methods for optical mode and carrier confinement, photonic crystals and their cavity designs, and finally semiconductor materials from which the structures are made as well as the active materials that provide necessary gain.

2.1 From conventional to compact semiconductor lasers

The basic principle of any laser is to amplify light within the gain medium inside a resonant optical cavity producing a monochromatic, highly directional, intense beam of high spatial (and possibly temporal) coherence. From a range of different laser classes, laser diodes [24, 53] are ideal for optical communications applications, as they are entirely fabricated on semiconductor wafers.

As discussed in chapter 1, the energy required to operate an integrated laser scales with its size. However, the development of novel compact laser structures [54] not only reduces the energy consumption, but also enables the access of new device regimes, such as the thresholdless operation [55–57]. For lasers with small mode volume V and high cavity Q-factor, the spontaneous emission factor β, defined as a fraction of the total spontaneous emission coupled into the lasing mode [24], can approach 1. Early lasing onset enabled by the high β-factor suggests that very efficient lasers with low energy consumption could be realized.

2.2 Laser structures for optical and carrier confinement

Inherently planar fabrication technology of semiconductor lasers is more restricting than that of other types of lasers, as large dimensions of resonators and active media allow for simple and well controlled structural modifications. Thus, implementation of creatively designed structures is the only way to realize high-performance semiconductor laser device operation.

Historically, several designs have been proposed and developed to address transverse mode and/or current confinement in edge-emitting (in-plane) semiconductor lasers [24, 58]. The simplest modification of the broad-area double-heterostructure laser, which does not have any transverse confinement, is the gain-guiding. The gain-guided laser has a dielectric stripe with an opening in it, through which the current is injected and, to some extent, confined. Weak index-guiding is provided in the structure that has a ridge etched on the wafer, which results in transverse confinement from three sides. The full confinement is realized in the strongly index-guided laser structure, which is fabricated by etching a mesa protected with a dielectric mask through the active material layers, followed by the re-growth of passive layer around. The final structure is called buried heterostructure (BH), as an active material region is surrounded, i.e. buried, from all sides by lower refractive index passive material. Despite the fact that it is difficult to fabricate, the superiority in operational parameters over other semiconductor laser designs due to strong optical made and carrier confinement has led to its wide commercial applicability in different optimized forms in the optical communications. Out-of-plane emitting VCSELs are inherently different, however many of the same structural modifications can be applied [24].

In modern lasers with active materials of reduced dimensionality, such as quantum wells or quantum dots, additional layer structures for conduction and valence band confinement are usually introduced during the initial growth. Conventional types of these structures are: standard separate confinement heterostructure and graded-index separate confinement heterostructure [24, 58].

Many examples given in chapter 1 section *Small-footprint lasers for on-chip communications* manifest that incorporation of the BH in compact lasers designed for on-chip communications can lead to radical improve-

ment in performance and energy efficiency. In particular, advancement from pulsed lasing [59] to continuous-wave lasing [41] in electrically pumped photonic crystal lasers at room temperature has only been achieved with implementation of the BH in the cavity. Even if only optical pumping scheme is used, obtaining continuous-wave operation at room temperature is still difficult as a result of excess heating in the photonic crystal membranes [60], which can also be solved with the BH [39].

The difficulty of fabricating the BH in standard semiconductor lasers is much greater for the compact on-chip devices. The challenges are mostly associated with much smaller dimensions, requiring significantly higher precision during the device processing. Reduced sizes also mean that the ratio of surface area to volume for the BH increases, while the optical mode size and carrier number is reduced. Thus, the impact of the surface roughness introduced at the interface between active and passive materials, surface states and interfacial defects functioning as charge carrier traps will be significantly higher at the small scale.

2.3 Photonic crystals as laser cavities

Photonic crystal (PhC) is a structures with a wavelength-scale periodic refractive index modulation [61]. Owing to its unique band structure (ω vs. $\boldsymbol{k}$ representation, where ω is frequency and $\boldsymbol{k}$ is the wave vector) and the appearance of photonic bandgaps, propagation of electromagnetic (optical) waves can be controlled. Spatial confinement of photons by photonic bandgap effect is more powerful than by the total internal reflection, providing means for reducing the effective mode volume to the order of $\left(\lambda/2n\right)^3$, where n is material's refractive index, while maintaining large cavity Q-factor. The possibility of designing PhC cavities with very high Q/V ratios has drawn strong attention of quantum optics [62, 63] and laser communities [36, 37], and is one of the main reasons in rapid development and uses of compact PhC devices for on-chip optical communications [12].

A special type of PhC structure suitable for integration with planar semiconductor technology is the PhC slab [61] (Fig. 2.1). It is a hybrid structure with a two-dimensional periodicity but a finite thickness. The most common PhC semiconductor slab, referred to as the membrane, has a triangular arrangement of (drilled) holes, and is suspended in air to

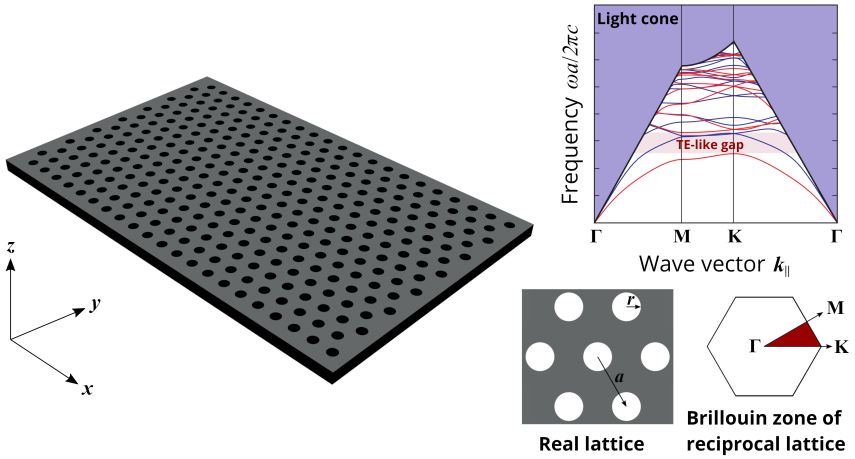


Fig. 2.1.: Photonic crystal slab with its corresponding triangular lattice in real space, Brillouin zone representation of the reciprocal lattice and the band diagram (adapted from [61]). The irreducible zone in the Brillouin zone representation is coloured in red. In the real structure, r is the hole radius and a is the lattice constant. In the band structure, TE-like modes are indicated in red, TM-like in blue; purple colour indicates the light cone region.

increase the refractive index contrast relative to surroundings. It can confine light due to the total internal reflection if an in-plane wave number satisfies the condition $\boldsymbol{k}_{||} > \omega/c$ (c is the speed of light in vacuum), that is, if the corresponding mode is outside the light cone and therefore coupled to the slab. In addition, periodicity (lattice constant a) of the PhC pattern determines the in-plane light propagation (ω vs. $\boldsymbol{k}_{||}$). Structural symmetry in the z-direction allows to classify the modes as TE-like and TM-like, with the bandgap opening for the TE-like mode (electric field component in the $x-y$ plane) [61]. The principle of the PhC laser cavity formation is thus to introduce defect states within this bandgap.

Standard photonic crystal cavities. The simplest kind of PhC cavity is formed from the perfectly periodic structure (Fig. 2.2a) by perturbing a single lattice site (or its surroundings). This perturbation is referred to as a point-defect, and can be introduced by any kind of localized modification on the order of one hole. If the defect has proper size to support a (resonant) mode, a peak is introduced into the crystal's density of states

within the bandgap. In terms of the band structure, the effect is that the defect with its dielectric permittivity $\varepsilon_{\text{defect}}$ lower than that of surrounding lattice sites (e.g., enlarged single hole) shifts the frequency of a defect state up into the bandgap from a band below [61]. Correspondingly, the frequency is decreased and the defect state is pushed into the bandgap from the band above in case $\varepsilon_{\text{defect}}$ is larger (e.g. reduced single hole, or an absence of it). A single point-defect in a triangular PhC can have different types of resonant modes, which are termed corresponding to the symmetry of the out-of-plane electric field component pattern: monopole, dipole, quadrupole and hexapole [61]. In the PhC slab, where the simplest kind of point-defect is formed by means of omitting one hole (Fig. 2.2b), the defect state is pulled into the bandgap from the above-lying band, thus having dipole or higher mode-symmetry. However, the Q-factor of the resulting dipole mode is low, because a substantial portion of the field is distributed inside the light cone, i.e. coupled to radiation modes. Optimized structural modification obtained by displacing the neighbouring six holes away from the defect by a fraction of the lattice constant a can increase the Q-factor above one million [62]. The idea of this structural PhC modification is to suppress radiation losses by tailoring the (Gaussian) envelope function of the electric field in real space, so that its Fourier-transformed spectrum would not have components inside the leaky region, and it was extensively investigated and successfully applied by researchers in order to reach record high cavity Q-factors [64].

A line-defect cavity (Fig. 2.2c) can be understood as a linear modification of lattice sites in sequence, that is, as an expansion of the point-defect cavity [48, 65]. The supported modes resemble standing waves inside a waveguide, with fields exponentially decaying at the ends of the defect. Line-defect cavities have larger mode volumes, therefore their Q-factors can be higher (comparing designs without shifted neighbouring holes) [65]. As in the previous case with forming point-defects inside the PhC slabs, the simplest type of line-defect can be realized by omitting a number of holes in a row.

The PhC waveguide shown in Fig. 2.2d is a further extension of the line-defect cavity concept. Guides modes that satisfy a certain combination of frequencies and wave vectors in the direction of the waveguide that lie inside the bandgap of the crystal can propagate along this channel. Depending on the operating point in the Brillouin zone representation and

corresponding group velocity $v_g = d\omega/dk$, the guided mode can propagate in the fast (away from the zone edge) and slow (near the zone edge) light regime [66]. The fast-light mode behaves much like a regular waveguide mode. The slow-light, on the other hand, enhances interaction between the propagating electromagnetic mode and the material as a result of reduced v_g and deeper mode's penetration into the PhC [67], which can be desirable for increased effective spatial gain coefficient in compact structures [68]. An adverse effect is the simultaneous enhancement of propagation losses due to fabrication-disorder related scattering [60, 69]. Theoretically, PhC waveguides could be used as on-chip light-guiding channels for optical communications, however propagation losses constitute a serious problem for the actual implementation. It might just be more practical to couple light into silicon waveguides and use them for guiding [45, 70], while using the PhC structures for other applications in which their implementation is significantly more beneficial.

Point- and line-defect cavities are in principle isolated inside the otherwise periodic PhC structure. In order to provide paths for light to actually enter and leave the cavity, some kind of coupling structure is necessary. In case where the PhC structures are implemented together with Si waveguides, allowing direct light-coupling between the cavity and Si waveguide might be unfavourable for the device functioning, as the cavity Q-factor might drastically reduce. From this perspective, introducing input and output cross-ports directly in the PhC structure is advantageous due to design flexibility and optimization potential. Light can then be coupled to the Si waveguide using these auxiliary PhC ports without detrimental impact on the device performance. An illustrative example of a line-defect PhC cavity with input and output waveguides is given in Fig. 2.2e. The optimization process would involve tuning the coupling from/to the cross-ports by choosing the correct distance to the cavity and shifting the holes around while simultaneously monitoring and maintaining the desired cavity Q-factor.

A somewhat distinctive PhC design is so called double heterostructure, which does not form an isolated cavity, but rather allows localization inside the specifically engineered waveguide region. The double heterostructure can be constructed by replacing a part of the PhC waveguide with the structure having slightly different lattice constant. In Fig. 2.2f, the cavity region (red guidelines) is shown with largely exaggerated difference between

lattice constants, which would in reality be around a few percent. Two different guided modes inside the bandgap correspond to two waveguides with different lattice constants. A frequency interval called the mode gap exists in which the light can only propagate inside the waveguide with a larger lattice constant. Thus, the confinement of photons in the waveguide direction results from the existence of this mode gap, and not directly due to the photonic bandgap effect. Extremely high Q-factors were demonstrated with this structure [71].

Fano resonances in photonic crystals. Various complex physical systems involving interaction between a discrete resonance and a continuum of modes exhibit a generic Fano interference phenomenon [72, 73]. The characteristic features associated with Fano resonances are asymmetric and sharp spectral responses, as opposed to symmetric and wider Lorentzian found in conventional resonant systems. In photonic devices, demonstration of a Fano resonance typically involves a waveguide which is split into two parts either by a resonant cavity in-between, or by introducing a side-coupled cavity just next to it. In an elegant recent experimental demonstration on the PhC platform, a smooth development of the spectrum from symmetric inverse Lorentzian shape, via characteristic asymmetric Fano shapes, all the way to typical Lorentzian has been realized by introducing partially transmitting elements (holes) into the waveguide just below the side-coupled cavity [74]. Red- and blue-parity Fano shape tuning by varying the distance between the side-coupled cavity and the partially transmitting element has also been theoretically investigated [75]. The richness of the Fano resonance phenomenon has been successfully applied in demonstrating various high-performance on-chip components, such as channel drop filters [76], ultrafast all-optical modulators [77], switches [74, 78], light diodes [79], pulse carving [80] and signal reshaping/noise suppressing structures [81].

A particularly important application in the framework of this thesis is the PhC Fano lasers. It was theoretically proposed that is could be possible to achieve frequency-modulation of such laser with its bandwidth exceeding 1 THz [52, 82]. In addition, with the possibility of ultrashort pulse generation in the ps range [52], Fano laser boosts an excitement about opportunities for on-chip optical communications. Recently, the Fano laser

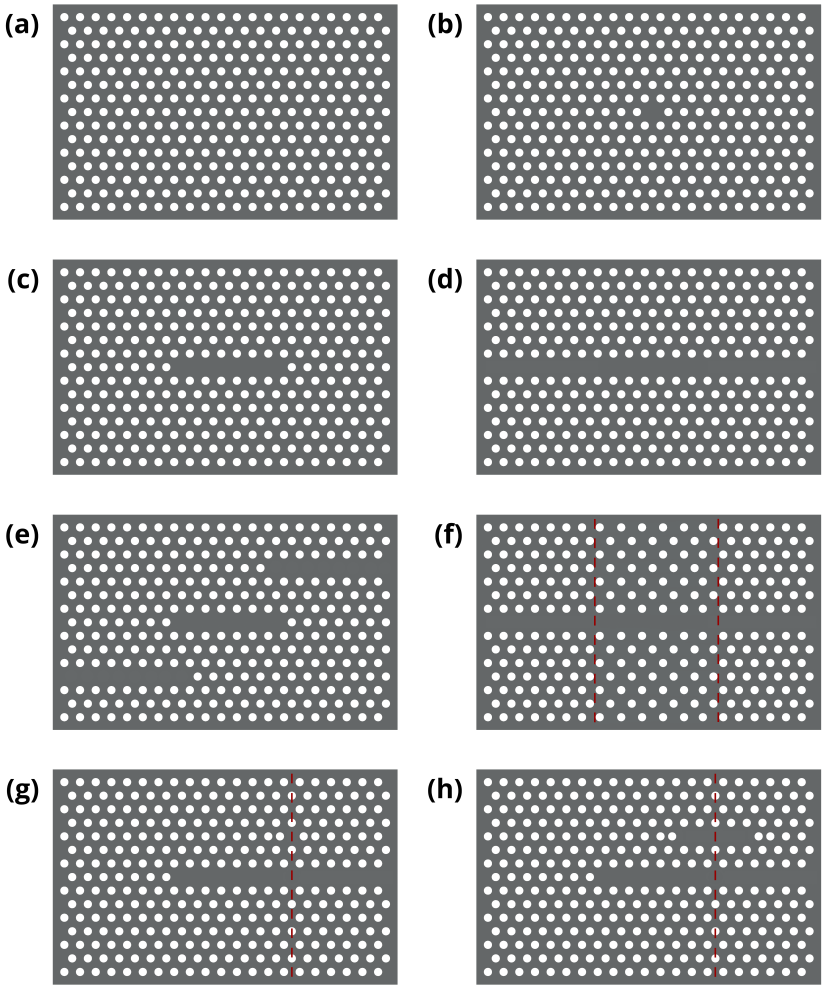


Fig. 2.2.: Photonic crystal designs: (a) periodic non-modified structure; (b) H1 (L1) point-defect cavity; (c) L7 line-defect cavity; (d) waveguide; (e) L7 line-defect cavity with input and output cross-ports; (f) double-heterostructure cavity; (g) L7 line-defect cavity with right-side Fano-mirror forming interference between side-coupled H0 point-defect cavity and the waveguide mode; (h) L7 line-defect cavity with right-side Fano-mirror forming interference between side-coupled L4 line-defect cavity and the waveguide mode.

has been experimentally demonstrated using a sample with 3 layers of quantum dots embedded in the device layer, using a line-defect PhC cavity with a broadband mirror on one side (formed by terminating the PhC waveguide) and a narrowband mirror on the other (formed by Fano interference between the waveguide mode and a side-coupled H0 nano-cavity) [83], as illustrated in Fig. 2.2g. The investigated Fano lasers were single-mode with a wavelength independent of the cavity length, clearly distinct from ordinary multi-mode line-defect lasers with wavelengths red-shifting with increasing cavity length. In addition, with increase in pump power there was a transition from the continuous-wave lasing to self-pulsing, explained as a consequence of a dynamical mirror reflectivity change due to absorption in the non-pumped quantum dots inside the H0 nano-cavity [84]. It is believed to be the first demonstration of passive pulse generation realized in nano-lasers. Further interesting design extensions of the Fano laser include incorporation of a line-defect side-coupled cavity instead of nano-cavity, as shown in Fig. 2.2h, and absence of active material inside of it to prevent self-pulsing. These two structural modifications have not yet been reported and are targeted in this work.

2.4 Material considerations

Device platform: InP-on-Si. The importance of crystalline silicon for the semiconductor industry has already been discussed in chapter 1. Suitable properties has made it "material choice number one" for integrated circuits, which is why Si has the most developed low-cost and high-scale infrastructure of all semiconductors. It is one of the main reasons for the progress and success of Si photonics.

The applications of Si as "all-in-one" semiconductor material in photonics is, however, limited by its band structure. Si has an indirect bandgap, meaning that in the electron energy vs. wave vector diagram representation the valence band maximum and the conduction band minimum do no line up vertically. Indirect optical transitions are inefficient and weak, because photons with negligible momentum alone are not sufficient for the momentum conservation, requiring participation of a phonon. Direct bandgap III-V semiconductor materials are superior in terms of light emission and absorption. As the name suggests, the structure of direct bandgap

material is such that the valence band maximum is directly below the conduction band minimum, allowing much stronger vertical transitions as viewed in the $E - \boldsymbol{k}$ diagram.

III-V semiconductors, made from Group III (Ga, In, Al) and Group V (As, P, Sb, N) elements, form a family of compound materials. By combining a few of these elements with different ratios into ternary (3 components) or quaternary (4 components) alloys grown on III-V substrates, material properties can be controlled and tailored for both electronics and photonics applications in a wide range (Fig. 2.3). Industrial and research interest in III-V semiconductors closely relate to progress in the optical fibre communications, reflecting to some extent technology-driven Si platform development. For standard optical silica glass fibres, attenuation of light limiting the transmission of signals has a few characteristic minima (operation windows) near 850, 1300 and 1550 nm. Naturally, material research is largely focused on semiconductors with optical properties matching characteristics of the transmission medium.

GaAs is one of the first III-V materials that has attracted significant interest first for electronic and then for photonic applications. Its high electron mobility is important for high-frequency and high-speed electronics applications, while a wide range of visible and near-infrared wavelengths covered by its lattice-matched $Al_xGa_{1-x}As$ ternary alloys have long been used for fabricating light emitting diodes (LEDs). GaAs-based diode lasers and LEDs served as transmitters when the 850 nm operation window was initially used, but even to this day, as the main long-haul fibre communications window has shifted, GaAs/$Al_xGa_{1-x}As$ VCSELs are almost exclusively utilized for short-connections (<100 m) in data centres due to their low cost.

InP is another very important binary III-V semiconductor material, which for many years did not acquire such industrial importance as GaAs. However, the situation started changing rapidly once the fibre communications operation windows moved to 1300 nm (lowest dispersion) and to 1550 nm (lowest losses), as these wavelengths are complicated to reach with GaAs-based lasers. On the contrary, InP (near) lattice-matched $In_xGa_{1-x}As$ ternary or even quaternary alloys cover a much wider near-infrared wavelengths range. Now, InP-based semiconductor lasers are the mainstay technology for fibre communications, especially long- and medium-range systems.

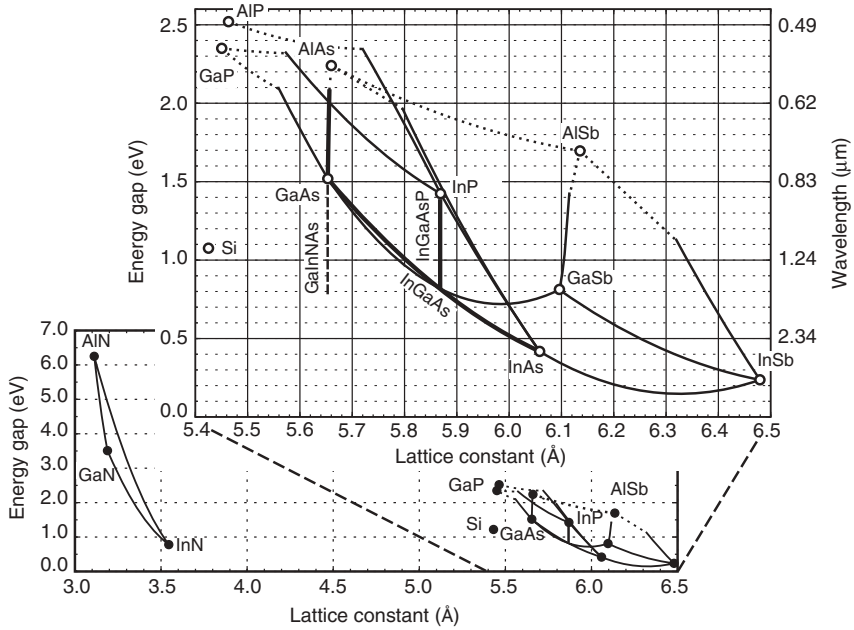


Fig. 2.3.: Bandgap energy (wavelength) vs. lattice constant at $T = 0$ K. Ternary alloys are defined by lines connecting binary III-V materials, quaternaries – by areas enclosed by lines. Reprinted from [24].

Today, much of the integrated photonics with active functionality are realized by utilizing InP. Applications drive the cost down, which is why devices operating around 1550 nm can greatly benefit from the abundance of equipment designed for this wavelength. To be completely fair, there is nothing exceptionally unique about the InP material for integrated photonics, and in fact a lot of today's research and development is undertaken on other material platforms. For example, wide-bandgap nitride semiconductors (GaN, AlN, InN) can offer particular advantages for specific on-chip applications [85]. On the other hand, InP can also be integrated on other materials than Si. Using SiC as a substrate material is particularly attractive due to its thermal expansion coefficient being well-matched to InP and its extremely large thermal conductivity [86]. Still, future perspectives of these other platforms are less clear due to high production cost of high-quality materials and in general lesser development. Most likely no other semiconductor platform will ever scale as much as Si did, therefore it makes a perfect sense to utilize Si as the main platform onto which samples of III-V or other material are integrated for the required functionality.

The choice of InP-on-Si as a device platform for this work is based on the aforementioned practical reasons, combined with the desire to continue on the foundation built previously by other people with their research efforts and transferred technological know-how. The physical insight and understanding gained throughout this project is by all means not limited to one material platform and could be transferred to other systems.

Gain materials: quantum wells and quantum dots. From the carrier confinement point of view, every "revolutionary" semiconductor laser device performance improvement is essentially marked by a quantum mechanical engineering novelty in reducing threshold current density [87]. Starting from the first homogeneous diode laser in the early 1960s, followed by the double-heterostructure (bulk) laser concept, and finally to the use of quantum wells (QWs) and quantum dots (QDs) [58]. As these new approaches become better optimized, successive "evolutional" engineering improvements follow, first of all, transition from pulsed to continuous-wave (cw) operation, then increase of the output power and enhancement of stability and long-term reliability.

When the active semiconductor material layer is reduced in size, population inversion is easier to achieve simply because the amount of material is smaller (less carriers). However, substantial size reduction results in the quantum confinement of charge carriers which alters the density of states (DOS), that is, energy distribution. The DOS governs the overall bounding shape of the maximum material gain, an essential parameter of any laser. For bulk semiconductor material, the DOS rises with the square root dependence on energy, and the density of electrons (holes) per unit energy forms a smooth curve given by the product of the density of states and the (quasi-) Fermi-Dirac distribution function. QWs and QDs, on the other hand, have 2D step-like and 0D singular DOS, respectively.[1] The uniqueness of these is reflected as improvements in laser characteristics and is discussed next for each active material separately.

In the QW structure, the initial lasing wavelength is determined by the separation between the lowest allowed $n = 1$ energy subbands. While in bulk material the lasing wavelength would tend to higher photon energies following the shift in the gain peak with increased carrier injection, for

[1] Quantum wires are in between, having 1D DOS, however they are not discussed in this thesis.

the (ideal) QW it would remain fixed at the point where the density of states rises abruptly at $n = 1$. It would not change as more carriers are injected and the maximum number of states are filled (the gain saturates) following the Fermi-Dirac distribution, up until the point when the next allowed $n = 2$ subband transition is reached and the lasing wavelength suddenly shifts. In reality, lineshape broadening effects due to the energy uncertainty and physical dimension (thickness) variation in the epitaxial structure smooths out ideal discontinuous features of the gain spectrum, however the distinct characteristics of the QWs remain [24]. Less carriers needed to achieve population inversion in QWs than bulk material thus decreases the threshold current density, provides larger overall gain and increases differential gain dg/dN, so the gain can be changed faster for high-speed applications [24].

Almost every QW laser device characteristic can be significantly improved by deliberately growing active layer in a strained-state, with its tailored composition having different lattice constant than the substrate's[2] [88]. These improvements are attributed to two main mechanisms: 1) reduction of the hole effective mass as a result of increased valence band curvature, which allows population inversion to be achieved with a lower injected carrier density; 2) distortion of the bulk crystal symmetry, thus matching it more closely to the symmetry of the laser beam, which leads to a higher proportion of carriers in the active region contributing to the laser gain [88]. Both of them depend on the type of strain in the well alloy, that is, if its lattice constant is larger (compressive) or smaller (tensile) than the substrate's. The well and the barrier are grown oppositely strained (strain-compensated) so that dislocations would not form in the stack. The particular choice of strain is dictated by the desired application, as otherwise incorrect strain-type can lead to dire consequences for the device performance. In particular, photonic crystal slabs with the cavity mode states lying within the TE-like bandgap benefit from the compressively strained QW layers.

A choice of different III-V material compositions exist for QWs on InP substrates [89, 90]. The easiest to grow are ternary InGaAs/InAlAs alloys, however they have limited simultaneous wavelength-lattice con-

[2] Being significantly thicker, the substrate imposes its lattice constant on the layer that is grown, causing the build-up of strain in that layer. As the overall lattice volume must stay the same, compression/expansion in-plane is accompanied by the corresponding proportional change in the perpendicular direction.

stant tunability. Quaternaries form richer family of alloys with a wide tunability range. In this work, the InGaAsP/InAlGaAs system is chosen for wells/barriers, allowing to design high material gain and high differential gain strain-compensated QWs on InP substrate for operation around 1550 nm [91]. On the other hand, the device fabrication is complicated by the use of Al in the barriers that make it difficult to etch through with the standard O_2 containing dry etching chemistries, as Al is easily oxidized and thus becomes resistant to etching; an appropriate dry etching recipe without O_2 has been adapted and optimized in this work, and is discussed in detail in chapter 5 section *Buried heterostructure fabrication by etching*.

Appendix C contains more specific InGaAsP/InAlGaAs QWs parameters used for the devices discussed in this work: well and barrier compositions, thicknesses, photoluminescence spectra.

The ultimate limit in charge carrier confinement is represented by the quantum dot (QD) structures. Their uniqueness stems from the δ function-like DOS and an effective overlap of the spatially localized electron and hole wave functions [92]. For lasers, these characteristic features imply rapid population inversion, emission wavelength solely determined by the discrete energy levels, temperature insensitive threshold current density, very high material gain and differential gain [93–95].

The most successfully applied epitaxial growth method producing high optical quality self-assembled flat-top (truncated) pyramid shape QDs [96] is performed in the Stranski-Krastanow regime, whereby the dots formation process is driven by the strain energy reduction in the deposited thin material layer with largely different lattice constant than the substrate's [93, 97]. As the critical layer thickness is reached, a spontaneous formation of isolated, non-uniformly arranged material islands occurs during the growth interruption step. A continuous, couple of monolayers thick wetting layer of the same material is left underneath the dots, which resembles a quantum well and acts as a reservoir supplying carriers to the QDs ensemble [94]. The growth is completed by capping QDs with a continuous material layer, which strongly influences the final shape, size, and consequently emission properties of the QDs [96].

With current QDs fabrication technologies it is unfortunately not possible to realize devices which would make full use of theoretically predicted QDs potential. While individual QDs have discrete energy levels with homogeneously broadened (due to the energy uncertainty [24]) transitions,

a naturally non-uniform size and shape distribution of the self-assembled QDs results in a large inhomogeneous gain spectrum broadening [94]. Although this broadband gain is undesirable for single-mode lasers and if higher output powers are needed, it is advantageous for tunable lasers, as well as for the optical amplifiers [97]. In addition, threshold current density variation with temperature is very small only below 300 K, but it varies strongly approaching room temperature due to insufficient carrier localization energy [93, 95].

The optical confinement factor Γ characterizes an overlap between the active material and the optical mode in laser [24]. The vertical confinement factor is small for both QWs and QDs, however it can be increased by stacking multiple layers on top of each other [97]. The limit on how closely two QD layers can be separated from each other is set by the residual strain in the capping material, as the strain-coupling from below affects properties of the above-lying dots [97]. Considering the in-plane confinement factor, it is much larger for the QWs forming continuous layers than for isolated QDs [93, 98]. High surface density of dots is needed for increasing the modal gain and the output power [24].

Considering group III-V semiconductor QDs, the majority of earlier investigations have been directed to InAs on GaAs system for the 1-1.3 μm emission range [95], with a current focus towards InAs on InP for 1.55 μm and beyond [96, 97, 99–101]. Two primary reasons for that are [97]: 1) during the epitaxial material growth, a change of group III source is required for InAs growth on GaAs, while group V change is required for InAs on InP. The former is easier to implement, considering that group III species control the reaction, as typically group V overpressure is maintained. Switching from As to P during the QDs formation step results in a much more complicated growth mechanism and its dynamics due to exchange of the group V on the surface during switching. In addition, pyrolysis of group V species is only partial at relatively low growth temperatures (<500 °C); 2) InAs and GaAs lattice constant difference (6.7%) is more than twice larger than InAs and InP (3.1%). Strain-driven QDs formation mechanism is weaker for the system with a smaller lattice mismatch, implying that larger (longer wavelength emission) InAs dots form on InP.

More specific information about the epitaxially grown InAs QDs used for the device fabrication in this work is given in appendix C.

2.5 Chapter summary and final considerations

The buried heterostructure concept has been exploited in the semiconductor lasers for many years, however realizing the structure with small enough dimensions suitable for embedding into the photonic crystal cavities is a challenging task. This chapter intended to provide the necessary understanding of the key principles and reasoning behind the choice of materials, structures and designs. In the following chapters of this thesis, all is put into practice as the device fabrication and characterisation is presented and analysed.

3 Alignment Precision Metrology

Accurate positioning of the buried heterostructure with respect to the laser cavity is crucial for device operation. Uncontrollable misalignment can result in devices with the buried heterostructure performing worse than standard ones with the gain material across an entire sample. Although exact efficiency decrease due to misalignment is not trivial to estimate, its principle is easily understood: active material absent from the cavity does not contribute to the useful gain while adding absorption losses outside, an overlap between carriers and an optical mode is reduced, and in case of the photonic crystal, surface defect states are formed as the active material is exposed to an ambient inside the etched holes. In a nutshell, information about the positioning tolerance is not only useful, but essential for misalignment compensating strategies and optimized device performance.

The purpose of this chapter is to present the e-beam metrology investigation results of processing-induced deformation of an exposed pattern of alignment marks in heterogeneously bonded InP on silicon substrate. Despite a wide variety of semiconductor devices fabricated on III-V-on-Si platform, there is a lack of systematic experimental data in literature attempting to quantitatively estimate the degree of wafer-scale misalignment on such wafers. Experimental configurations and methods described in this chapter were devised to represent real conditions encountered in photonic device fabrication, and therefore they directly represent achievable alignment accuracy that can be expected for the buried heterostructure photonic crystal lasers and similar devices in general.

The metrology method described could be customized and used as a convenient tool to monitor processing-induced pattern deformation during device fabrication. This knowledge could be applied when accounting for and correcting fine residual-errors prior to the multilayer exposure(s).

This chapter is based on the "*Comparison of processing-induced deformations of InP bonded to Si determined by e-beam metrology: direct vs. adhesive bonding*" journal publication listed in the publications list.

3.1 III-V integration on Si

Integration methods. As pointed out in chapters 1 and 2, III-V material integration on Si seems to be inevitable for the efficient realization of active functionality of photonic on-chip devices and reduced fabrication cost.

Many different technologies exist for III-V integration on Si, where integration can be understood in terms of material growth/bonding or transfer of material stacks/components. The later, hybrid integration (pick-and-place, transfer printing [102]), is out of scope of this thesis. Here, two main categories of III-V material (partially processed or not processed) realization on Si will be discussed: monolithic and heterogeneous integration.

Very promising, however probably the hardest one to achieve is monolithic material integration, where group III-V semiconductor is epitaxially grown on group IV silicon. The fundamental difficulty is defect-free growth of materials having different parameters than the substrate on which the growth is performed. These include lattice constants, thermal expansion coefficients and mismatch between polar/non-polar interfaces [92]. Common strategy to fight these issues is the introduction of some sort of spacers or defect-blocking structures, localizing and preventing defects from propagating into main III-V device layers [103–106].

Heterogeneous material integration (or, loosely speaking, wafer bonding) is a promising technique, where two already grown semiconductor wafers are bonded together either directly [107–110] or using some intermediate layer that assists the bonding process, such as metals in case of the eutectic bonding [109], organic/inorganic adhesives in case of adhesive (else referred as glue) bonding [109, 111, 112], or others. The strength of the heterogeneous wafer bonding lies in that (almost) any kind of material can be integrated on the desired substrate.

In contrast to using a single material platform, thermal budget after the integration is one of the major limitations for subsequent device processing. Mismatch of the thermal expansion coefficients has a major role in high temperature treatment processes, such as oxidation, diffusion, contact annealing, and material (re-)growth. Specifically for this work, the linear thermal expansion coefficient for InP ($4.6 \cdot 10^{-6}\ ^{\circ}\mathrm{C}^{-1}$) is almost twice that of Si ($2.6 \cdot 10^{-6}\ ^{\circ}\mathrm{C}^{-1}$). Thus, for the directly bonded InP on Si wafer, the stress in the InP exceeds the critical stress limit and dislocations are generated above $300\ ^{\circ}\mathrm{C}$ temperatures [113]. After a substrate removal,

the temperature limit of the critical stress value in the III-V on Si depends on the III-V layer thickness, which for the InP falls somewhere between 350 and 500 nm [114].

Other post-integration issues and limitations are more specifically linked to the type of material integration used. For monolithic integration, defects may be activated and start propagating from the interfacial layer at high temperatures. For heterogeneous wafer bonding, de-bonding can result if the adhesion between layers is not strong enough [115]. In addition, the glass transition temperature exists for the adhesive polymer used in the adhesive bonding integration method. For instance, a widely used adhesive benzocyclobutene (BCB) polymer is generally not suitable for processing where prolonged high temperature exposure is required or certain chemical resistance limitations apply, as after curing the glass transition occurs above 350°C temperature [116]. Strict processing requirements, such as CMOS compatibility, can ultimately determine which type of integration is needed or allowed.

Requirements and challenges for high precision alignment for modern semiconductor devices. Alignment during the multilayer exposure is a standard procedure in the modern semiconductor device fabrication process, however the required level of accuracy for advanced integrated devices is constantly increasing. Without the obvious application for the realization of the buried heterostructure photonic crystal lasers presented in this work, a wide variety of other relevant examples include lasers [117], modulators [118] and photodetectors [119], contacts for electrical operation of nanodevices [120], light coupling to/from active III-V layer into passive Si circuitry [45, 70], or even combinations of these. The drop in the light coupling efficiency as a result of misalignment was calculated for the last example.

Initially, even before device processing, semiconductor wafer is far from being planar, and although the extent of curvature is commonly specified by a supplier [121], the exact shape is generally not given. During multiple processing steps in-between lithography exposures, wafer shape together with device structures defined on it and their relative positions to alignment marks are subject to change. Complex modifications to the wafer geometry arise due to many factors, including non-uniformities in the deposited and processed films [122], direct wafer bonding-induced

strain [123], curvature and shape mismatch between wafers being bonded [124], in-plane stretching deformations induced by wafer chucking during lithography [125], etc. In advanced Si electronics manufacturing, high-resolution wafer geometry measurements combined with mechanics-based models are used as standard process control methods of predicting and correcting processing-induced alignment errors between lithography steps [122] to meet the ever-tightening error budgets. Unfortunately, implementation of such sophisticated methods in practice is a complicated task and may not apply for less-mature Si photonics processing, thus semi-automatic (or even manual) alignment in less-modern DUV or e-beam lithography systems is generally used [70].

Wafer bonding adds additional level of complexity in the process, and affects the alignment accuracy depending on the type of bonding used [126]. Unless some special self-aligning device designs [127] or pattern distortion compensation methods are adapted, integration precision usually only relies on a high density of dedicated alignment marks near device structures. Needless to say, alignment marks occupy precious wafer area that could otherwise be used for devices, they usually have larger dimensions extending e-beam exposure times, which in turn increase fabrication costs. Better understanding of the wafer-scale non-uniformities of the bonded III-V on Si wafers is therefore needed for the design and processing optimization.

3.2 Experimental procedures and e-beam metrology principle

Wafer bonding and formation of alignment marks. Multiple test wafers have been prepared in a MOVPE reactor by epitaxially growing a 250 nm InP layer on top of a lattice-matched etch-stop InGaAs layer on a 2" (100)-orientation InP substrates. These wafers were then divided into two groups for the BCB and direct bonding experiments.

For the BCB bonding, dry etching was used first to define the alignment marks in the top epitaxial layer on InP wafer. For this purpose, ZEP520A positive e-beam resist of ~ 500 nm was spin-coated onto the PECVD-deposited non-stoichiometric 200 nm silicon nitride (SiN_x) etch-mask. An array of 21×21 alignment marks (crosses, with an arm length

of 375 μm and a width of 2 μm) was exposed in e-beam with a distance of 1.5 mm between the centres of two neighbouring marks, defining an array pattern of 3×3 cm in size. After development, the pattern was transferred to the underlying SiN_x layer using RIE dry etching with CHF_3/O_2, and after the resist strip to the 250 nm InP layer[1] by a chlorine-based ICP etch. The rest of SiN_x was removed by another RIE etch step. Finally, a 1 μm thick SiO_2 layer was deposited on the InP wafer in PECVD, while a 1.3 μm thick SiO_2 layer was thermally grown on a 2" (100)-orientation Si wafer. The choice of introducing SiO_2 on both wafers is partially related to increased adhesion to the BCB, but it also commonly has a specific purpose for device operation, whether it is for the sacrificial layer release to form a free-standing photonic crystal membrane [60], or as an intermediate optical-coupling layer between III-V and underlying Si [45, 70].

Proceeding with the BCB bonding, both InP with the defined alignment marks and Si wafers were treated with AP3000 adhesion promoter, and then a ∼2.5 μm thick layer of BCB (Cyclotene $3022-46$) was spin-coated on the Si wafer, followed by 5 min soft-bake at 90 °C. The wafers were then stacked on top facing each other and placed inside a wafer bonder to cure/polymerize the BCB for 1 hour at 250 °C temperature in vacuum under an applied force of 2 kN. After the bonding was complete, the InP substrate was removed by wet etching in an agitated HCl, and the etch-stop InGaAs layer was removed in H_2SO_4:H_2O_2:H_2O 1:8:8 solution.

The wafer processing and bonding flow described previously can be considered as an example of the double-sided process, in which the initial structures are first formed on the top-side of the III-V layer, followed by wafer bonding, and subsequent alignment and processing from the back-side of the III-V layer after uncovering it by the substrate/sacrificial layer removal. If wafer bonding precedes formation of the initial structures, the alignment and further processing are realized from the same side of the III-V layer, hence denoted as the single-sided process. These methods are schematically illustrated in Fig. 3.1.

While physical limitations of the adhesive layers make BCB bonding in principle only suitable for the double-sided processing scheme, both single- and double-sided processing methods were used to prepare a batch

[1] The openings are etched into the InP layer instead of having isolated material as the alignment marks, because in this way measured deviations from the designed positions would not be not caused by possible localized distortions or adhesion issues of the alignment marks, but they would actually represent deformations of the surrounding bonded InP layer.

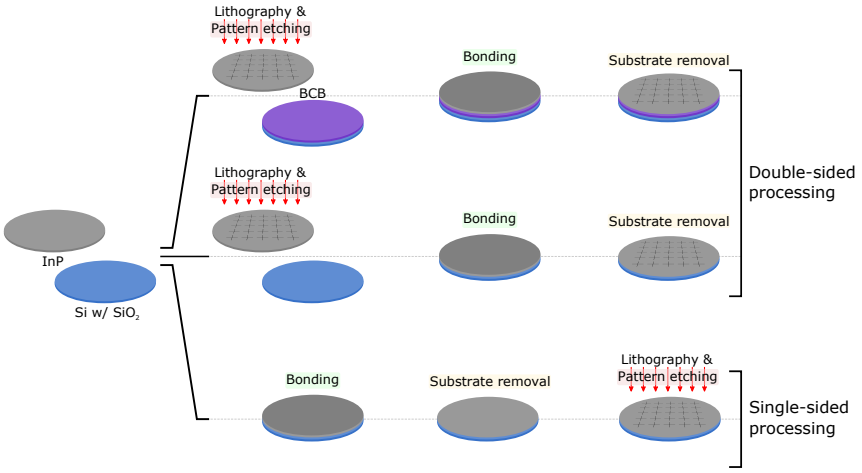


Fig. 3.1.: Schematic representation of double-sided and single-sided processing methods used for metrology experiments.

of directly bonded wafers for the metrology experiments. The double-sided process flow for fabricating the alignment marks in the top InP layer before the direct bonding is very similar to the one presented earlier, with two exceptions: 1) for transferring the alignment marks from the SiN_x mask to the InP layer with reduced sidewall roughness, anisotropic crystallographic-orientation dependent H_3PO_4:HCl solution with $1{:}4$ ratio was used instead of the ICP etching, and 2) no PECVD SiO_2 layer was deposited on the InP side before the wafer bonding, as no thick adhesive layer separates the InP from the thermal glass on silicon in the final stack. These also apply to the single-sided process, except that bonding is performed first.

The direct InP to Si wafer bonding uses an intermediate thin Al_2O_3 layer[2] [110] to achieve a high bond-strength and avoid problems associated with bonding of two dissimilar surfaces. Both InP and Si (with thermal glass) wafers were placed in an ALD chamber, where a thin 2 nm Al_2O_3 layer was deposited at 200 °C on each side of the wafer. Al_2O_3 provides surfaces rich in OH-groups, which results in immediate hydrogen bonding facilitated by the Van der Vaals forces after placing the wafers together [115]. The surfaces were further bound and the bond strength was increased by placing the wafer stack in the wafer bonder for 1 h at 300 °C in vacuum with a force of 2 kN applied to the stack. Next, the InP

[2]It is referred to as the direct bonding, because Al_2O_3 layer is very thin, on the order of native oxide thickness.

substrate and InGaAs etch-stop layer was removed as described previously, leaving the 250 nm InP layer on Si.

From the fabrication standpoint, the single-sided processing approach is advantageous as the crucial bonding step is performed early in the III-V processing stage. This reduces the chance of introducing particles on the wafer surface, which cause the decrease of bonding yield and in the extreme case can even lead to bonding failure. In terms of wafer surface preparation prior to bonding, no special cleaning was done neither for the InP wafers taken directly from the MOVPE reactor after the epitaxial growth, nor for the InP wafers with the pre-etched alignment marks. While in the first case it was possible to obtain defect-free bonding due to a low-level surface contamination, preventing voids from appearing on the pre-processed wafers after the InP substrate removal is a much more difficult task, which is in principle achievable with proper cleaning strategy and/or chemical-mechanical polishing (CMP) procedures.

Finally, in a similar fashion, identically-sized arrays of alignment marks were also exposed and transferred to a 2" and centre of a 4" (100)-orientation bare Si wafers of 350 μm thickness. These test wafers were used to determine the overall accuracy and limitations of the e-beam system used in the metrology experiments.

E-beam metrology measurements procedure. The main tool, which allows to determine processing-induced deformations for different InP to Si wafer bonding and processing approaches with such a high precision is the JEOL JBX-9500FSZ e-beam system, used both for lithography and as a metrological SEM. Quality control of the overlay[3] accuracy for standard Si processing demonstrated the achievable performance to be well within the specifications from the manufacturer [129]. While the machine itself is very well capable of operating below 10 nm regime (for writing and aligning), performing quantitative overlay accuracy or processing-induced deformation measurements across the entire wafer with minimized errors is by far not an easy task, requiring careful planning and rigorous implementation of the experimental procedures.

For pattern writing, 2" wafers[4] were clamped in the central slot of a

[3] The definition of an overlay, as given in [128]: A vector describing the positional accuracy with which a new lithographic pattern has been printed on top of an existing pattern on the wafer, measured at any point on the wafer.

[4] Except for a case where a 4" Si test wafer was used.

titanium cassette, loaded onto the e-beam stage, and thermally stabilized for a few hours to limit temperature drift to within 0.01 °C during the 5 min writing sequence in between stage drift re-calibration[5]. Thermal drift is the most dominant overlay error source [130], thus Ti cassette has been chosen to allow for better thermal stability, as its thermal expansion coefficient is a few times smaller than that of aluminium. Next, the instrument column was thoroughly calibrated for an electron beam current of 6 nA, which in conjunction with an aperture size of 80 μm corresponds to a beam diameter just below 10 nm.

Apart from the temperature stabilization and calibration described above, the e-beam metrology procedure consists of three main parts: sample positioning using any two alignment marks, measurement of an array of alignment marks, comparison and correction of designed and measured positions.

Sample positioning is realized by placing the bonded InP-on-Si wafer into the cassette, manually adjusting it in the cassette window, and then tightly clamping from the back-side with the leaf-spring-loaded back-plate. The cassette is then loaded onto the e-beam stage, where a 100 keV beam scans across arms of two (global) alignment marks in x- and y-directions, resulting in a detectable backscattered-electrons signal from the topography and Z (atomic number) contrast, which in turn allows to determine the centre positions of the scanned marks. Measured centre positions are then compared to designed values, and wafer magnification (gain), shift and rotation are corrected by the machine for subsequent array scanning procedure.

Metrology scanning is performed right after the e-beam calibration and wafer position correction. A metrology scan file contains the design coordinates of an array of alignment marks and parameters for optimal signal detection. Six independent scans are performed on each wafer in total, where each mark in the array is scanned at three different arm-positions and each measurement is performed twice by changing the stage movement pattern (x- and y-raster type scans) with a fine-scan width of 12 μm or less. Scanning at different positions allows to obtain a complete set of data even if some of the experimental values are corrupt due to, for example, particles or bonding defects at parts of the alignment mark. Also,

[5]Temperature change of 0.01 °C corresponds to ~ 0.65 nm shift from the wafer centre to its edge (for the 2" Si wafer), or to ~ 15 nm shift from the Ti cassette centre to its edge in a perpendicular direction (175 mm).

averaging over multiple measurements reduces random position detection errors.

Finally, a data file is generated for each array scan in which the difference value between the designed and measured position of each individual alignment mark is recorded. After removing any possibly corrupted data points by erroneous detection, six independent measurements are averaged, followed by calculation and correction of the linear components of the magnification M_x and M_y, shift ΔX and ΔY, and rotation $\Delta\theta$ [131]. The aim is to find the coefficients that simultaneously minimize the sum of squared residuals for x and y in the following expressions:

$$r_x = \sum \Big(x_{meas} - \big(M_x \cdot x + \Delta X - \Delta\theta \cdot y \big) \Big)^2 \tag{3.1}$$

$$r_y = \sum \Big(y_{meas} - \big(M_y \cdot y + \Delta Y + \Delta\theta \cdot x \big) \Big)^2 \tag{3.2}$$

After correction, the underlying wafer-scale residual deviations are disclosed, which are present when the wafer is further used for alignment, and they represent the multilayer alignment error. Linearly-corrected vector maps are plotted for the visual representation, where each and every vector depicts the direction and magnitude of deviation in *x*- and *y*-directions from the designed alignment mark position.

Quantifying baseline accuracy for e-beam metrology. In order to quantitatively estimate accuracy and limitations of the e-beam metrology method, including any systematically induced errors, the metrology measurements were performed on bare 2" and 4" Si wafers without any bonding. Pattern exposure and dry etching followed similar procedure described under the paragraph *Wafer bonding and formation of alignment marks*, after which the metrology measurements were performed as described in *E-beam metrology measurements procedure*. In addition, the wafers were also rotated in the cassette by $90°$ and $180°$ and measurements were repeated to reveal the existence of any possible wafer orientation dependence.

Overall uniformity and repeatability of measurements is assessed by subtracting vector maps obtained after placing/measuring, and replacing/re-measuring Si wafers keeping the same orientation in the cassette slot. The data for 2" Si wafer is plotted in a form of histogram for

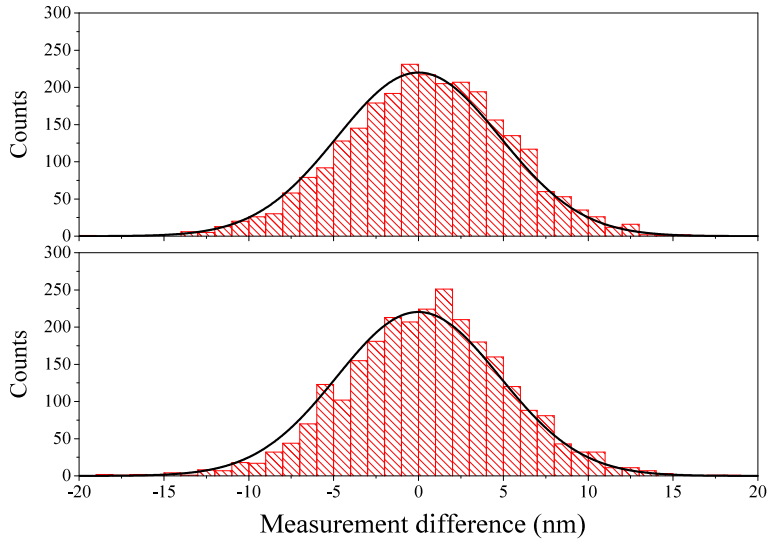


Fig. 3.2.: Histograms representing metrology reproducibility as measured differences between repeated metrology scans for (top) *x*- and (bottom) *y*-coordinates of alignment marks in the 21×21 size array defined on the Si wafer. Solid lines are fitted normal distribution curves.

x- and *y*-coordinates separately (Fig. 3.2), and the statistical 3σ standard deviation is found to be 15 nm for both directions. These residual values include alignment marks detection errors, and as Si dry etching process is well optimized and the resulting alignment marks have very smooth sidewalls afterwards, they set the achievable alignment precision limit for the III-V samples, which have worse quality alignment marks.

Analysing vector maps obtained for 2" and 4" bare Si wafers after linear corrections, deviations within 10 nm are observed across the inner part of the patterns, with increased values around the pattern edges for both. However, these deviations increase significantly for the 2" Si wafer rotated in the cassette slot by $90°$ and $180°$. It is especially clearly visible in the difference vector maps, obtained by subtracting the measurement values of the wafer rotated in the cassette slot from the measurements of the non-rotated wafer[6] (Fig. 3.3). Interestingly, no such orientation dependence is observed for the bare 4" Si (Fig. 3.4). These results indicate

[6] In order to compare "apples to apples", the data set from the rotated-wafer measurements after correction is rotated backwards, so that the subtraction is performed between the same alignment marks. This way, any possible systematic error induced during the pattern writing is eliminated from the results.

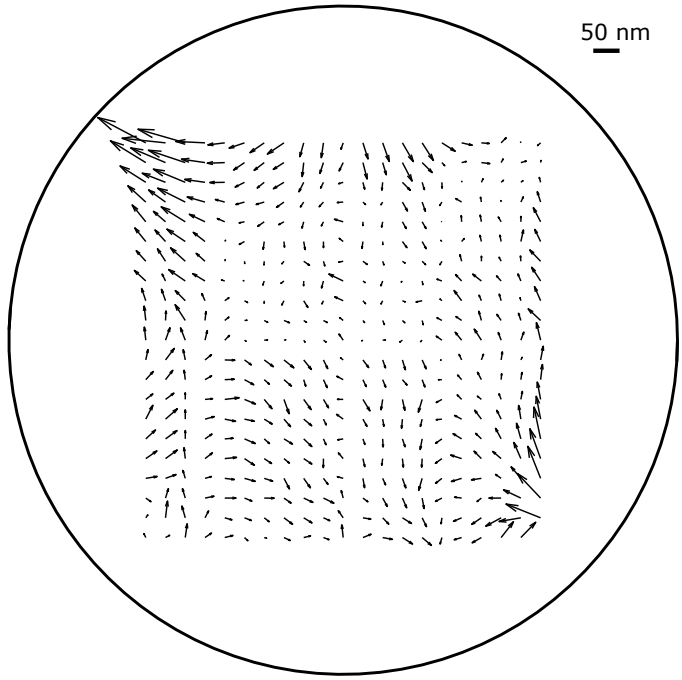


Fig. 3.3.: Difference vector map obtained by subtracting the metrology measurements of the 2" Si wafer rotated in the cassette window by 180° from the non-rotated wafer. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors.

that, first of all, pattern distortion increases closer to the wafer edge[7], and secondly, changing wafer orientation in the cassette slot with respect to its original orientation during the initial pattern exposure introduces significant non-uniform deformations. It is thus verified that due to complex and non-symmetric shape of the semiconductor wafer (as discussed in the paragraph *Requirements and challenges for high precision alignment for modern semiconductor devices*), high precision alignment requires consistency when wafer clamping in the e-beam cassette slot is performed, otherwise significant pattern distortions can be introduced. Already from the measurements of non-bonded Si test wafers it can be concluded that in order to minimize pattern distortion, the effective wafer area must be significantly

[7] Although it is certainly true that linearly-corrected data is minimized due to correction with respect to the wafer centre, there is no signature of radially increasing deviation observed for the pattern exposed on the 4" Si wafer. Hence, this effect is not artificial, and is expected to emerge even if proportionally larger pattern was exposed on the 4" wafer.

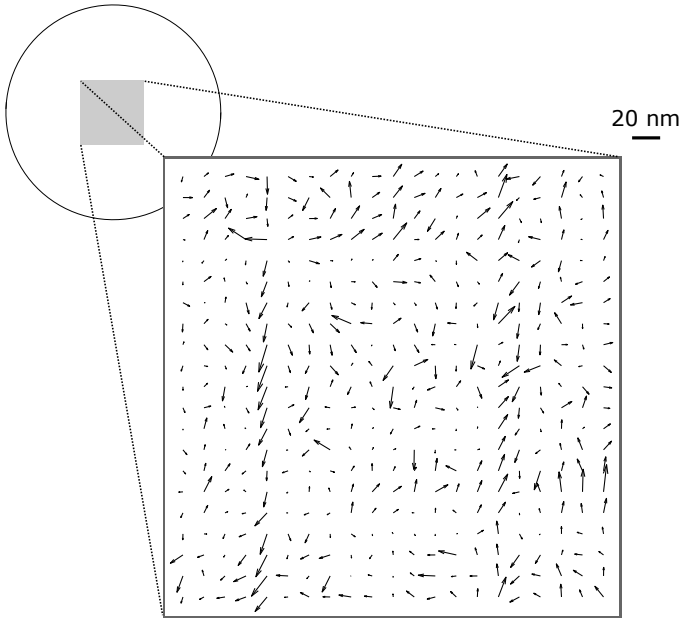


Fig. 3.4.: Difference vector map obtained by subtracting the metrology measurements of the 4" Si wafer rotated in the cassette window by 180° from the non-rotated wafer. Top left schematic indicates the position of the pattern on the 4" wafer (black circular outline); the scale bar is for the vectors.

reduced beyond that of the wafer diameter, and the wafer should be always oriented the same way in the e-beam cassette slot, as standard linear data correction methods used by conventional e-beam systems are not sufficient to account for this type of distortion.

All the metrology measurements presented next were performed on 2" InP wafers bonded to 2" Si. Clearly, bonding to 4" Si wafers would have been beneficial, however 2" to 4" bonding procedure was not optimized at the time of the metrology experiments. Careful consideration of observed pattern distortion origin is thus very important.

3.3 E-beam metrology of bonded samples

In this section, processing-induced deformation of the alignment marks patterns are quantified using the e-beam metrology measurement results

for the BCB and directly bonded wafers processed in the double- and single-sided manner. After discussion of the observed characteristic features in each case, a comparison is made.

Distortion of BCB bonded double-side processed wafers. As discussed in section 3.2, the array of alignment marks on the BCB bonded wafers is scanned from the side opposite to which it was defined, representing the double-sided processing approach. Using identical approach as for test Si wafers, the 3σ standard deviation for the detection of dry etched alignment marks in InP was estimated to be below 40 nm for both x- and y-directions, significantly worse than for Si. Nevertheless, the pattern distortion determined after the correction of magnification, shift and rotation is found to be much greater than that (Fig. 3.5). In fact, in large parts of the wafer away from the centre, the measured distortion is on the order of 1 μm and in some parts exceeds even 2 μm. It seems that rather thick 2.5 μm BCB layer allows for stress relaxation between InP and Si wafers, and after the InP substrate and sacrificial layer removal, the 250 nm InP layer is found to be predominantly expanded along one diagonal direction, while contracted along another (implying the presence of an orthogonal distortion component [131]). Although linear, orthogonality correction is beyond the standard e-beam correction capabilities, meaning that the pattern distortion in Fig. 3.5 represents a typical situation after correction for the multilayer exposure in device fabrication. Repeated measurements on the BCB bonded wafers show qualitatively similar orthogonal distortion signatures, but of different orientations. This indicates that such BCB bonding-induced distortion is generic, but with randomly oriented orthogonality for each specific case.

It was previously reported [132] that partially curing BCB prior to wafer bonding can prevent polymer re-flow and to some extent improve the alignment between two Si wafers. While many optimization strategies besides partial curing could be implemented, such as, for example, using thinner BCB layer or temperature compensation of the thermal expansion coefficients differences for InP and Si (by adjusting top and bottom chuck temperatures in a wafer bonder), and they could potentially reduce pattern distortion, this is a matter of a whole separate study.

The consequences of this significant non-uniform deformation observed for the double-side processed BCB bonded wafer is that proper

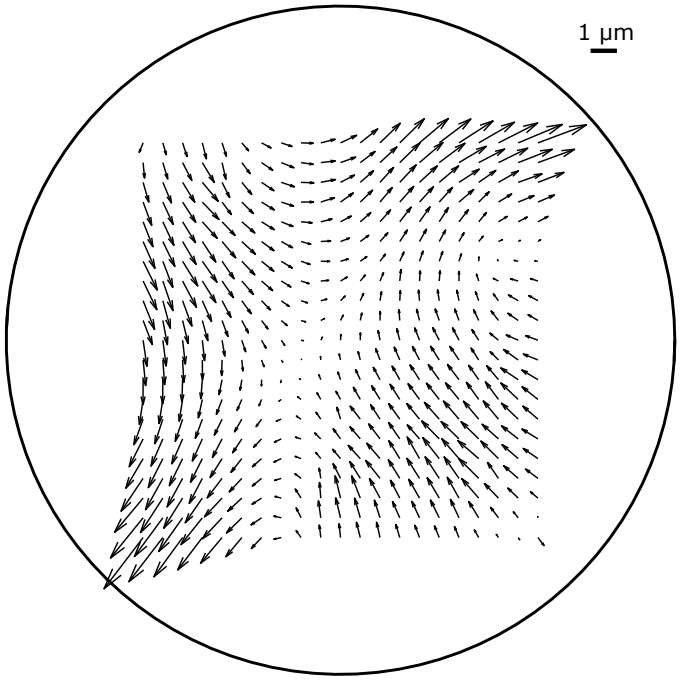


Fig. 3.5.: Vector map representing processing-induced deformation of the double-side processed InP layer BCB bonded to 2" Si wafer. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors. A uniform linear expansion ($M_x - 1 = 1.4 \cdot 10^{-4}$, $M_y - 1 = 1.6 \cdot 10^{-4}$) has been subtracted from the measured data, pattern shift and rotation are corrected.

wafer-scale correction by using alignment marks with larger-spacing is very difficult, and achieving high-accuracy alignment to the initial exposure on the InP wafer after the BCB bonding is difficult. These results adequately explain previously observed random distortions appearing on the InP wafer after BCB bonding to Si [133], as well as difficulties encountered in the alignment process during the device fabrication in this work. Sadly, the amount of induced deformations were high enough to prevent demonstrations of working BCB bonded devices in both cases. Although higher density or even the use of dedicated alignment marks for individual devices could potentially improve the situation, it would inevitably result in drastically prolonged pattern writing time in e-beam, increased design complexity and added overall fabrication cost. If possible, transitioning to another bonding scheme can eventually become a simpler and more beneficial solution.

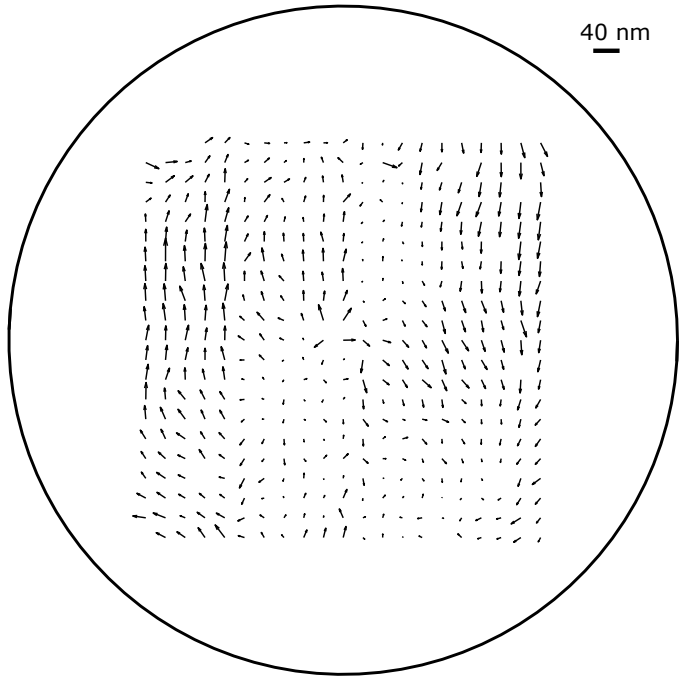


Fig. 3.6.: Difference vector map obtained by subtraction of the metrology measurements of the InP layer BCB bonded to 2" Si wafer before and after RTA. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors.

In section 3.1, BCB integration method limitations in terms of temperature have been addressed. The glass transition occurring at around 350 °C limits the wafer processing after bonding. To assess stability of the BCB bonded wafer after a short, high temperature exposure, a rapid thermal annealing (RTA) was performed at 420 °C for 5 s, which is a standard contact-annealing method used for improving electrical characteristics of the n-type metal contacts to semiconductors. Afterwards, the e-beam metrology was repeated and the measurement results were subtracted from before the RTA step (Fig. 3.6). Practically no change in the wafer deformation pattern is observed for this short duration higher temperature exposure. On the other hand, it has to be kept in mind that any other longer annealing, oxidation, deposition and/or growth/regrowth steps could be detrimental to the quality of the BCB bonded wafer, making it

impractical choice for the buried heterostructure photonic crystal laser fabrication using the double-sided processing approach.

Distortion of directly bonded double- and single-side processed wafers. For the direct bonding, both double- and single-sided processing approaches were utilized. Double-sided processing adds additional requirements for wafer handling to avoid particle deposition on the surface before bonding. While a thick BCB layer can embed some of the smaller particles and prevent the formation of bonding defects in the InP layer, the thin Al_2O_3 used as an intermediate layer for the direct bonding is incapable of that. The InP wafers in these experiments are subject to multiple processing steps during the formation of the alignment marks. Thus, the appearance of bonding defects is expected, and indeed is seen in Fig. 3.7 as a void in the vector map. Obtaining high bonding yield is challenging for any kind of direct bonding, however the use of the single-sided processing approach reduces the number of wafer handling steps prior to bonding, since the InP wafer can be bonded to the Si substrate right after the epitaxial growth and Al_2O_3 deposition in ALD.

Wet instead of dry etching of the alignment marks was used for the directly bonded wafers to reduce sidewall roughness and avoid high temperature during transfer (which is the same procedure used for the buried heterostructure photonic crystal laser fabrication), however only minor improvement was determined, with 3σ below 35 nm for *x*- and *y*-directions. The metrology measurements of the directly bonded double-side processed wafer shows deformations on the order of a few hundred nm's across the wafer (Fig. 3.7). Disproportional expansion between the centre and outer parts might be caused by the improper pre-bonding if the initial bonding did not originate from a single-site, but rather multiple locations [115]. Deformation asymmetry around the bonding defect region indicates its localized influence.

Significant improvement of the direct bonding over the BCB bonding is readily observed, which would allow for reasonable alignment precision in most parts of the wafer even with the use of distantly-spaced alignment marks.

Finally, pattern distortion for the directly bonded wafer using the approach of single-sided processing is shown in Fig. 3.8. After linear data correction, the central part of the wafer has high uniformity with

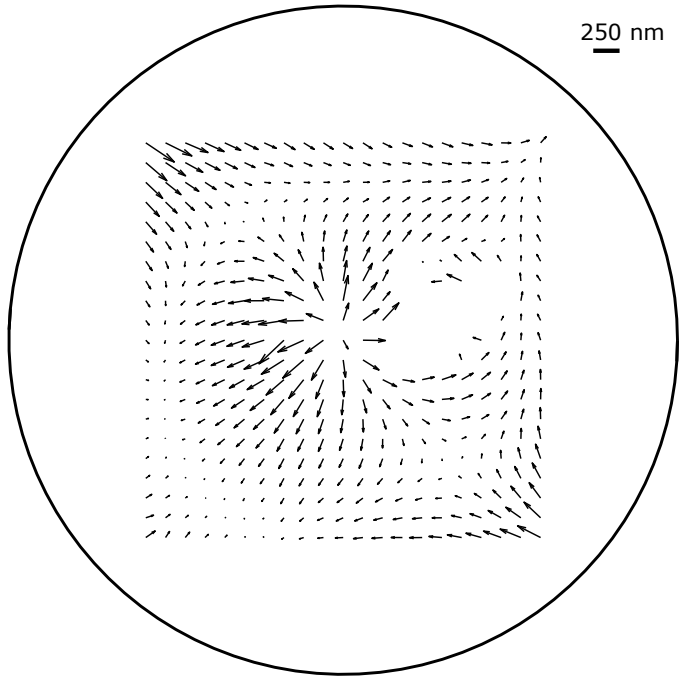


Fig. 3.7.: Vector map representing processing-induced deformation of the double-side processed InP layer directly bonded to 2" Si wafer. Empty vector map regions correspond to the bonding defects. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors. A uniform linear expansion ($M_x - 1 = 3.4 \cdot 10^{-5}$, $M_y - 1 = 2.2 \cdot 10^{-5}$) has been subtracted from the measured data, pattern shift and rotation are corrected.

the residual pattern distortion variations below 50 nm. However, larger deformations are observed in the corners, especially the lower left. Pattern exposure, transfer by wet etching and metrology for the single-sided processing are performed after the bonding, thus it is certain that these deformations are induced by post-bonding wafer processing.

Simple mechanical calculations based on [125] can very well illustrate the connection between the wafer shape change and induced pattern distortion on the surface (in-plane distortion). Assuming a parabolic wafer warp (Fig. 3.9) with a reasonable value of 12 µm [121], the corresponding curvature κ can be found from either geometrical considerations (by definition $\kappa = \frac{1}{R}$, where $R = \frac{x^2 + y^2}{2y}$) or by using a small angle approximation ($\kappa = 8\frac{y}{D^2}$, as $y = R - R\cos(\varphi)$ and $\varphi = \frac{D}{2R}$). In either

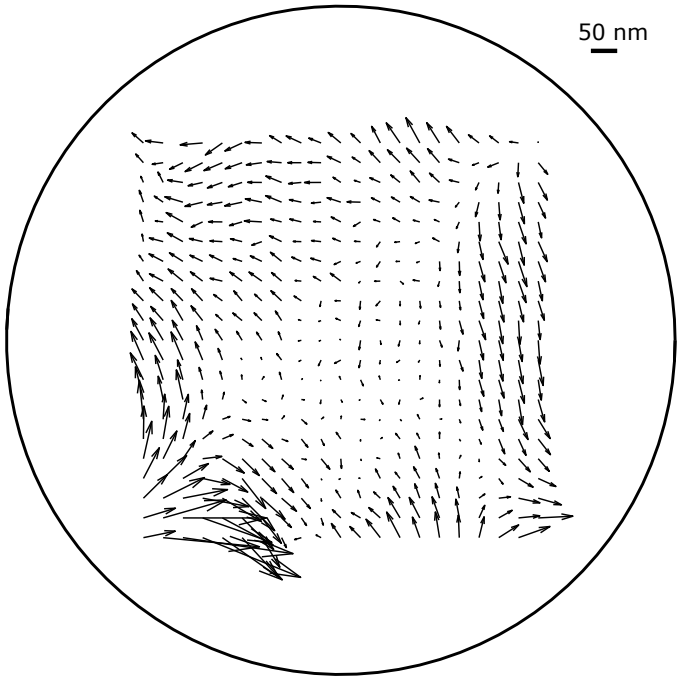


Fig. 3.8.: Vector map representing processing-induced deformation of the single-side processed InP layer directly bonded to 2" Si wafer. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors. A uniform linear expansion ($M_x - 1 = 5 \cdot 10^{-6}$, $M_y - 1 = 3.7 \cdot 10^{-6}$) has been subtracted from the measured data, pattern shift and rotation are corrected.

case, $\kappa \approx 0.0384$ m^{-1} for a 2" wafer. If the wafer is flattened, for example by clamping in the e-beam cassette, the surface of the wafer is placed in tension or compression depending on the initial curvature, and as a result distances between surface features increase or decrease. The induced strain due to bending is

$$\varepsilon = \kappa \frac{h}{2} \approx 6.51 \cdot 10^{-6} \tag{3.3}$$

where $h = 350$ µm is the wafer thickness. The corresponding induced change in distance Δl between the wafer centre and a corner of 3×3 cm array used in this work ($l \approx 2.12$ cm) is

$$\Delta l = \varepsilon l \approx 138 \text{ nm} \tag{3.4}$$

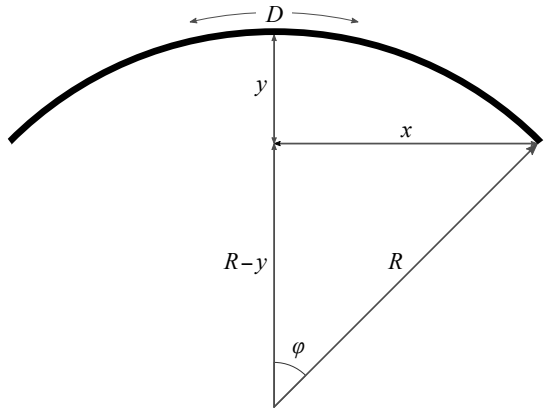


Fig. 3.9.: Diagram illustrating parameters for the wafer curvature calculation.

Of course, the wafer is clamped the same way into the e-beam cassette before the exposure of alignment marks and after the pattern transfer for the metrology experiment. There is, however, a difference in that the SiN_x layer is used as an etch-mask for the exposed pattern transfer into the InP layer, as discussed in section 3.2 *Wafer bonding and formation of alignment marks*. For SiN_x deposited in the PECVD machine used in this work, typical measured stress values are around ~ 430 MPa (tensile stress). Stoney's equation [134] can be used to calculate the radius of wafer curvature due to the deposition of stressed nitride layer:

$$R = \left(\frac{Y_\mathrm{s}}{1-\nu_\mathrm{s}}\right)\frac{t_\mathrm{s}^2}{6\sigma_\mathrm{f} t_\mathrm{f}} \tag{3.5}$$

where Y_s, ν_s and t_s refer to Young's modulus, Poisson's ratio and thickness of the substrate, respectively, stress σ_f and thickness t_f is for the film (nitride). In the case of a bonded wafer, the substrate parameters should take effective values for the stack InP−thermal SiO_2−Si, however in order not to overcomplicate these simplified calculations, bare Si substrate is assumed. In that case, $Y_{\mathrm{s}(100)} = 1.3 \cdot 10^{11}$ Pa, $\nu_{\mathrm{s}(100)} = 0.28$ and $t_\mathrm{s} = 350$ µm. Deposition of $t_\mathrm{f} = 200$ nm thickness tensile stressed SiN_x with $\sigma_\mathrm{f} = 430$ MPa results in a curvature $\kappa \approx 0.0234$ m^{-1}, as found using eq. (3.5) and previously used inverse relation between the radius and curvature. Repeating steps using eq. (3.3) and (3.4), the calculated change in distance Δl is around 87 nm. At this scale, additional distortion components may contribute, such as localized stress variations (particles on

the wafer surface when clamping in the e-beam cassette, deposited film non-uniformity) and/or electromagnetic effects near the e-beam cassette slot edges. These reasonable assumptions and simple calculations clearly demonstrate that surface pattern deformations on the order of 100 nm can be easily induced by wafer clamping in the e-beam cassette, and thus they can explain pattern distortion features observed for the directly bonded single-side processed wafer (Fig. 3.8).

High uniformity of the central part of the wafer allows for precise alignment using even distantly spaced alignment marks compatible with the standard DUV stepper reticle field size. This is very important for transferring wafer processing from research and development applications-oriented e-beam system to a more industrially-focused DUV lithography, which could ideally increase device throughput without sacrificing high alignment accuracy between exposures.

Finally, to assess stability of the directly bonded wafers at high temperatures, annealing at 650 °C temperature in the phosphine atmosphere in the MOVPE was performed twice for 15 min, followed by the metrology after each step. The difference vector map between the initially measured wafer, and after the second annealing (Fig. 3.10) indicates that high temperature processing for even extended durations does not introduce considerable additional InP layer deformations. The surface quality of the wafer also does not seem to change, although some degradation of the alignment marks was observed, which reduced the metrology precision. Some kind of protection might be needed if the alignment marks are already fully defined in the InP layer prior to the annealing step. For the optimized buried heterostructure photonic crystal device fabrication alignment marks are wet etched after the 2nd regrowth, posing no issues. Ultimately, using alignment marks etched into Si before bonding is desired (and only possible for the single-sided processing approach).

Appendix D links the metrology alignment precision measurements on the single-side processed directly bonded wafer presented here to the buried heterostructure photonic crystal laser device fabrication, which is based on this approach, by illustrating the alignment accuracy achievable when using the chip-marks alignment procedure.

Comparison of deformations in bonded wafers. Comparing the adhesive-BCB and directly bonded InP to Si wafers (and inherently double- and

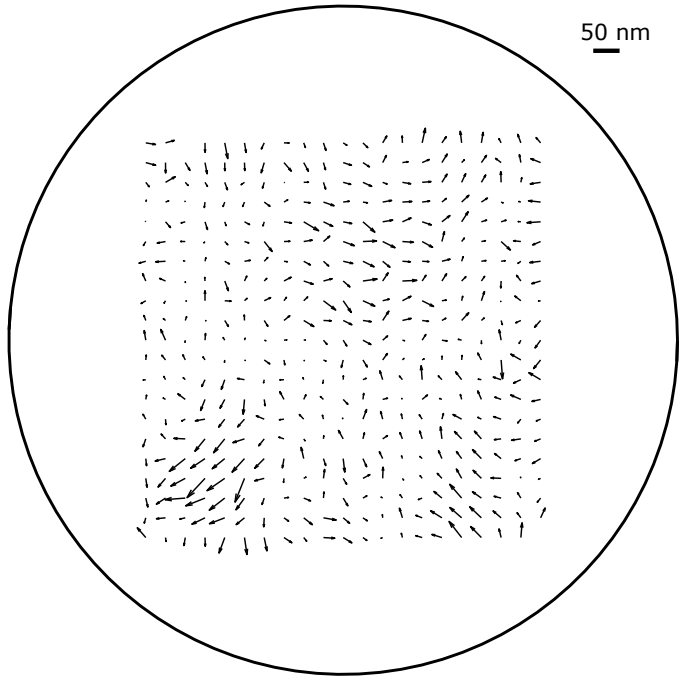


Fig. 3.10.: Difference-vector map obtained by subtracting metrology measurements of the pattern on the InP layer directly bonded to 2" Si wafer before and after the MOVPE anneal. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors.

single-sided type processing), several characteristic features are observed.

The pattern defined by the alignment marks in the InP layer is distorted after the BCB bonding non-uniformly and with a significantly greater magnitude than for the directly bonded wafer using the double-sided processing approach. It means that to achieve the same level of multilayer exposure alignment accuracy, considerably denser array of alignment marks would be needed for the BCB bonding, complicating the design, increasing the exposure as well as the alignment time in e-beam, and subsequently the overall cost. Furthermore, processing temperatures are greatly limited by the BCB polymer at the interface between bonded wafers. On the other hand, the process of direct wafer bonding is more demanding than BCB bonding. It requires greater care when dealing with particles, including wafer handing, chemical cleaning and/or polishing, thus the high bonding yield is in principle much harder to achieve without these additional steps.

The highest wafer-scale alignment precision is achievable on the directly bonded and single-side processed wafer with relaxed requirements for the density of alignment marks. Keeping wafer surface clean is easier, as the critical bonding step is performed early in the processing. Subsequent wafer exposure to high temperatures is tolerable, and does not introduce further deformations. In essence, there exists a great resemblance to non-bonded Si wafer, making this bonding and processing scheme the most desirable for the device fabrication, and is thus applied in this work.

3.4 Chapter summary and final considerations

An e-beam metrology technique was employed to study processing-induced deformation of the exposed pattern in 2" InP wafers bonded to Si substrates of the same size processed in three different ways. The conclusions are twofold: first, bonding-induced pattern deformation is dominant for the double-sided processing approach, where the initial processing is performed from one InP wafer side, followed by bonding and substrate removal, revealing another InP side from which the alignment is then performed. When using thick adhesive BCB bonding, deformation on the order of 1 μm is observed across an entire 2" wafer. It can be significantly reduced by using direct wafer bonding instead, however requirements for surface cleanliness are largely increased in this case to achieve high bonding yield after wafer processing. Second, the smallest deformation was experimentally determined for the direct wafer bonding combined with the single-sided processing approach, in which case the processing and alignment is performed after the InP wafer is bonded to Si. At this scale, the alignment accuracy approaches the case when a bare InP or Si wafer is used and is limited by the pattern deformation (in-plane distortion) induced during wafer processing by the wafer clamping in the e-beam cassette. This holds true even after prolonged treatment in the MOVPE at 650 °C temperature.

As noted previously, at the time of these metrology experiments, 2" to 4" bonding procedure was not optimized. However, all signs indicate that optimal, e-beam precision limited alignment should be achievable for the single-side processed 2" InP directly bonded to the central part of the 4" Si substrate, and with alignment marks etched into Si prior to bonding. This should be the "smallest-investment highest-impact" target to pursue.

4 Device Fabrication Overview

The chapter begins with an illustrative comparison of the buried heterostructure and non-buried heterostructure configurations, followed by a list of the device processing generations throughout the PhD project. The biggest transition happened between the 1^{st} and the 2^{nd} generations, which involved changing the BCB wafer bonding process to the direct bonding. Further transitioning to the 3^{rd} generation was minor, however overall change brought about the alignment precision needed for demonstrating high performance lasers. The optimized processing overview is given in the rest of this chapter.

The detailed processing flows including all fabrication steps and recipes used is given in appendix A.

4.1 Buried heterostructure vs. non-buried heterostructure

In this short section, the concept of the buried heterostructure photonic crystal laser is illustrated and compared to the non-buried heterostructure configuration.

The simplest realization of the photonic crystal laser requires an epitaxially grown sample with an active material layer and a sacrificial layer underneath. The designed photonic crystal pattern is then exposed and transferred by etching to the device layer. Finally, by wet etching the sacrificial layer underneath, an air-suspended membrane structure is realized (Fig. 4.1, left).

In order to form the photonic crystal laser with a buried heterostructure, the device layer has to be prepared prior to the photonic crystal pattern etching. Once the buried heterostructure is formed, an alignment step is necessary to position both structures properly, so that the active material would only reside inside the cavity region (Fig. 4.1, right).

Realizing the buried heterostructure on such a small scale is tricky,

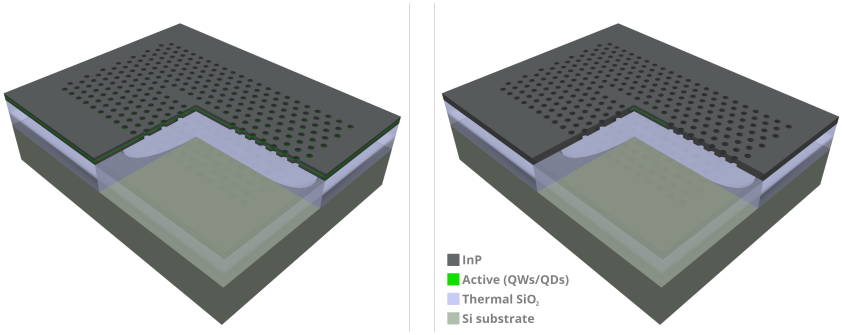


Fig. 4.1.: 3D cross-sectional representation of an air-suspended InP photonic crystal membrane device region: (left) without the buried heterostructure, where the holes are etched through the active material layer across an entire device region; (right) with the buried heterostructure embedded in the photonic crystal cavity only.

however worthwhile due to various improvements, as was discussed in chapter 1 and 2 and will be discussed further on.

4.2 Buried heterostructure device processing generations

During the time of this PhD project, three device processing generations were used for fabricating the photonic crystal lasers with the buried heterostructure:

- The 1st generation devices had the buried heterostructure fabricated and planarized on the InP wafers which were subsequently BCB bonded to 2" Si substrates. The major drawbacks associated with this type of processing are significant misalignment induced during the wafer bonding (chapter 3) as well as the bonding itself executed at the late processing stage. In case of the bonding failure, a lot of hard work is wasted. No lasing was observed for the fabricated devices from this generation.

- The 2nd generation devices have only become possible to realize after the direct bonding procedure for the 2" wafers was developed. The bonding itself happens early in the processing stage, which means that in case of a bonding failure not a lot of time and effort is lost.

The potential of good alignment for this generation devices was worsened due to deteriorated quality of the alignment marks during the 2^{nd} material re-growth step (performed after the alignment marks are formed). Only a couple of samples were processed in this way, and despite quite significant misalignment the (first ever during this PhD!) lasing from the buried heterostructure was demonstrated.

- The 3^{rd} generation addressed the issue of the alignment marks deterioration during the re-growth by forming (etching) the marks afterwards. This allowed to fabricate well-aligned devices on the directly bonded 2" wafers as expected from the alignment metrology experiments (chapter 3), and thus high performance lasers have been demonstrated.

In addition, one more possible device generation is proposed:

- The (hypothetical) 4^{th} generation is the logical next step in the device processing. As predicted by the metrology experiments (chapter 3), using a 4" Si wafer on which the pattern size is limited to 2", and the alignment marks are defined in Si, the alignment accuracy could be increased even further. Thus, by directly bonding the 2" InP wafer to the 4" Si substrate and only slightly altering the already optimized processing technology, even better alignment accuracy is expected, and as a result, higher performance devices could be realized. Initial tests for this generation started and wafers were bonded successfully, however further fabrication was halted at an early processing stage due to the lack of time.

The illustrative alignment results for three described device generations is presented in Fig. 4.2. Different structures were used to check the alignment for different generations. The most convenient and reliable high precision method has not been found yet, and currently requires the destructive sample cleaving followed by the selective wet etching of the active material to enhance the contrast for the cross-section examination with the SEM.

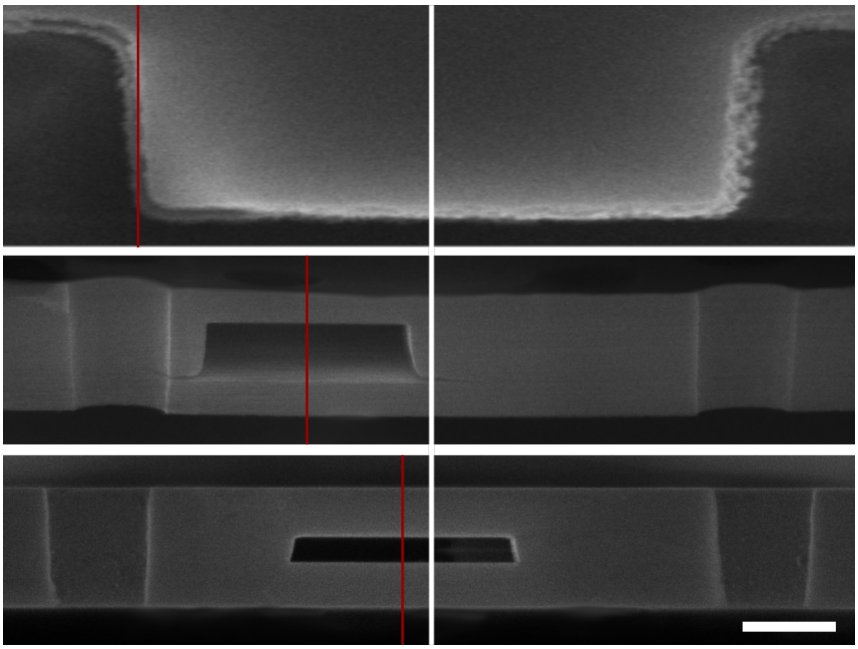


Fig. 4.2.: SEM images representing the typical misalignment expected for three generations of the buried heterostructure devices: (top) ~ 630 nm in the 1^{st} generation test structure imaged at a highly oblique angle (the BCB bonding scheme); (middle) ~ 270 nm in the 2^{nd} generation photonic crystal line-defect cavity imaged at cleaved edge (the direct bonding scheme before the optimization of alignment marks); (bottom) ~ 60 nm in the 3^{rd} generation photonic crystal test structure cavity imaged at cleaved edge (the direct bonding scheme after the optimization of the alignment marks). All the images are aligned so that the white vertical line goes through the centre of each test structure. Red lines indicate the centres of the buried heterostructure with quantum wells that were selectively wet etched to enhance the contrast. The scale bar is 200 nm for all the images.

4.3 Optimized fabrication process overview

This section is a quick walkthrough of the optimized 3^{rd} generation device processing. Each important fabrication step is briefly described and presented with a relevant "real" image taken during the processing, together with a schematic illustration.

Direct wafer bonding. The device fabrication starts with the direct wafer bonding procedure, during which the epitaxially grown InP wafer with the active material layers (quantum wells or quantum dots) and an InGaAs etch-stop layer is bonded to the 2" Si substrate with a thermally grown oxide layer. A thin Al_2O_3 layer required for the bonding is deposited in the ALD on both surfaces, after which the pre-bonded wafer stack is placed in a wafer bonder. The InP-on-Si wafer (Fig. 4.3) is prepared for the device processing once the InP substrate and the InGaAs sacrificial layers are removed by wet etching.

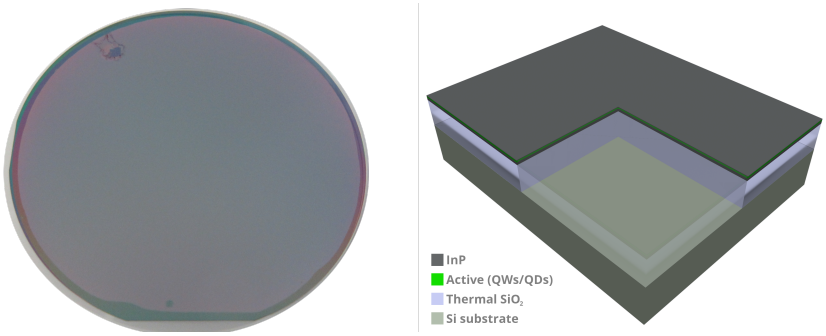


Fig. 4.3.: Heterogeneously integrated 2" InP-on-Si wafer prepared for the device processing: (left) camera image displaying a very high surface area yield (>95%) after the direct bonding; (right) 3D cross-sectional representation of a single device region.

Buried heterostructure formation: mask exposure in e-beam. Following surface preparation procedures and spin coating of high-resolution negative HSQ resist [135], the buried heterostructure mask is formed by an e-beam exposure and subsequent resist development (Fig. 4.4).

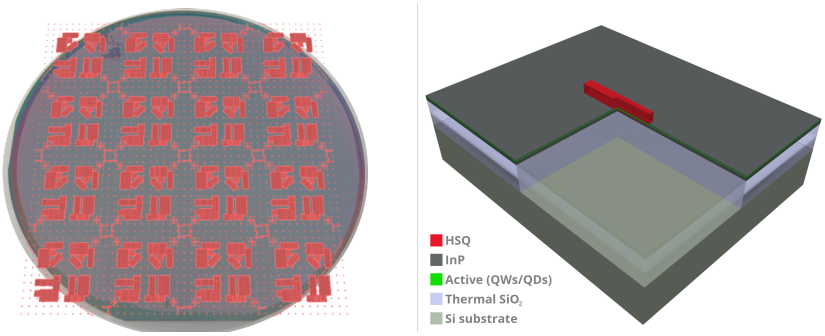


Fig. 4.4.: The buried heterostructure HSQ mask exposure in the e-beam machine: (left) camera image of the 2" InP-on-Si wafer with an overlayed outline of the design mask containing arrays of device structures, test structures and the alignment marks; (right) 3D cross-sectional representation of a single device region.

Buried heterostructure formation: dry etching. Next, the wafer is dry etched with the HBr-based chemistry in the ICP (Fig. 4.5). During the etch, InP and active material layers are removed around the masked mesa-structures with just enough of InP left for the subsequent material re-growth.

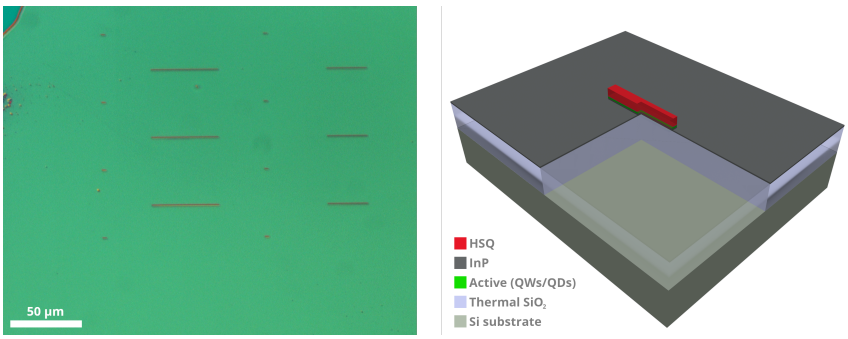


Fig. 4.5.: HSQ mask-protected mesa-structures formed after the dry wafer etching: (left) optical microscope image displaying an array of different length mesa-structures with the HSQ mask; taken with the 20x magnification objective and the Nomarski technique; (right) 3D cross-sectional representation of a single device region.

Buried heterostructure formation: the 1st regrowth. After the dry etching, the wafer is prepared and the InP is re-grown in the MOVPE to bury the active material left under the HSQ mask (Fig. 4.6). No growth takes place on the glass-like HSQ mask during this selective area growth step.

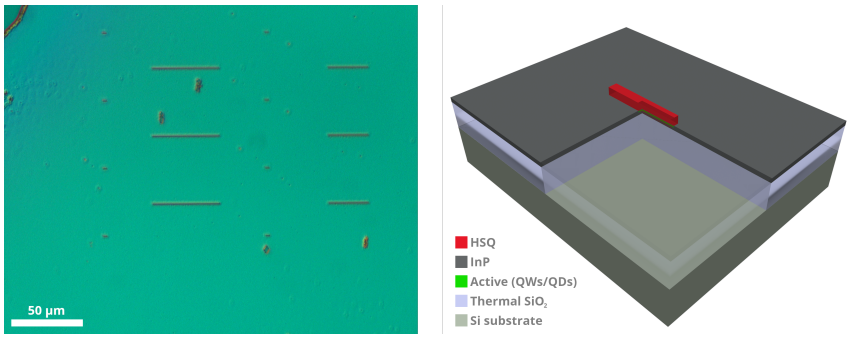


Fig. 4.6.: InP re-grown instead of the etched material around the HSQ-protected regions during the selective area growth: (left) optical microscope image displaying an array of different length buried heterostructure regions with the HSQ mask (identical locations as in Fig. 4.5); taken with the 20x magnification objective and the Nomarski technique; (right) 3D cross-sectional representation of a single device region.

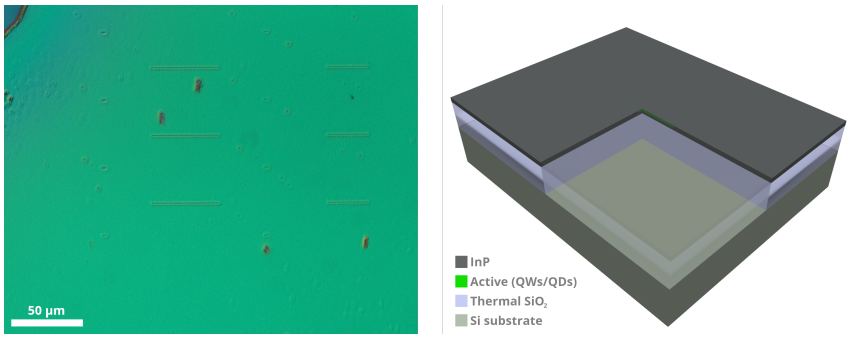


Fig. 4.7.: HSQ mask removed from the buried heterostructure regions after the 1st re-growth: (left) optical microscope image displaying an array of different length buried heterostructure regions without the HSQ mask (identical locations as in Fig. 4.5 and 4.6); taken with the 20x magnification objective and the Nomarski technique; (right) 3D cross-sectional representation of a single device region.

Once the 1st re-growth is complete, the HSQ mask is removed by wet etching (Fig. 4.7), except at the alignment marks (not shown here).

Buried heterostructure formation: the 2nd regrowth. The 2nd InP material re-growth step is performed after the HSQ mask removal (Fig. 4.8). The resulting wafer surface is (nearly) planar and the InP layer is 250 nm thick as intended for the specifically designed photonic crystals. The buried heterostructure is (vertically) centred in the InP layer.

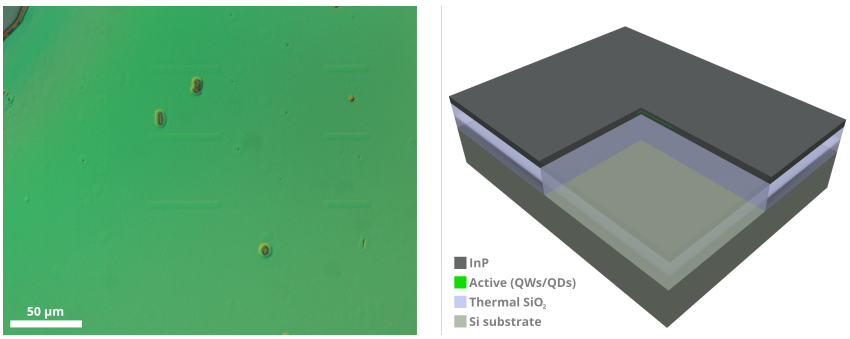


Fig. 4.8.: Planarized surface after the 2nd InP re-growth: (left) optical microscope image displaying an array of different length buried heterostructure regions after surface planarization (identical locations as in Fig. 4.5, 4.6 and 4.7); taken with the 20x magnification objective and the Nomarski technique; (right) 3D cross-sectional representation of a single device region.

The alignment marks are formed after the 2nd re-growth by wet etching, with the rest of the wafer protected. An example of the alignment mark is shown in Fig. 4.9.

Photonic crystal formation: alignment and pattern transfer. A hard-mask (SiN_x) is deposited by PECVD, followed by spin coating of a high-resolution positive ZEP e-beam resist. The wafer is then pre-aligned using the previously formed alignment marks and loaded into the e-beam, where the high-precision alignment procedure takes place to position the photonic crystal patterns directly above the already formed buried heterostructure regions. The e-beam written photonic crystal structures are dry etched into

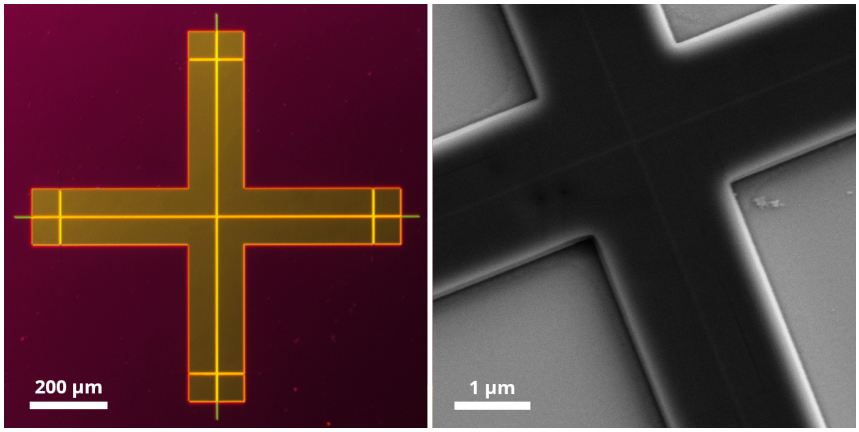


Fig. 4.9.: Alignment mark used for the photonic crystal pattern positioning on top of the fabricated buried heterostructure region: (left) optical microscope image after the final wet etching, with the alignment mark visible in the middle of the cross-shaped mask protecting the wafer surface; taken with the 5x magnification objective and the Nomarski technique; (right) SEM close-up image of the centre-part of the mark with the HSQ mask after the ICP etch of the mesa-structures formation step.

the SiN_x hard-mask in an RIE chamber (Fig. 4.10), the resist is stripped, and the structures are transferred from the hard-mask into the InP layer by additional dry etching step again in the RIE.

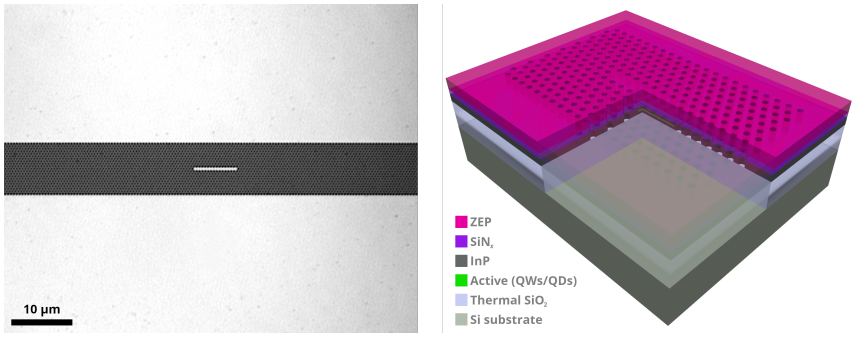


Fig. 4.10.: Photonic crystal structures aligned to the underlying buried heterostructure regions and etched from the resist into the hard-mask and into the InP: (left) optical microscope image of the formed photonic crystal L15 line-defect cavity structure; taken with the 150x magnification objective in the confocal mode; (right) 3D cross-sectional representation of a single device region.

Device completion: membranization. The device is completed by the final wet etching step, during which both the SiN_x hard-mask and the thermal SiO_2 under the InP is removed. An air-suspended InP photonic crystal membrane with the buried heterostructure is realized (Fig. 4.11).

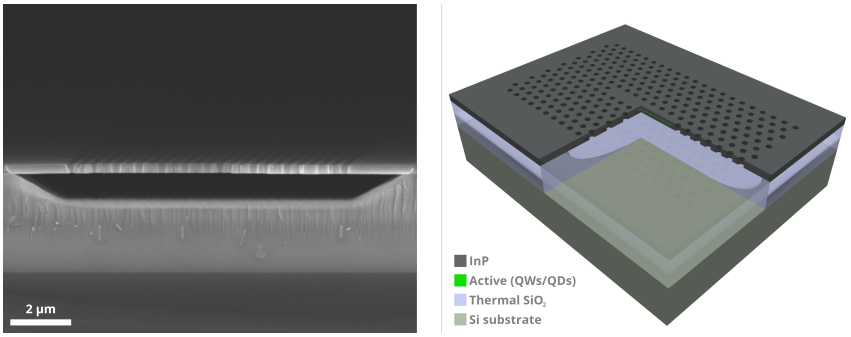


Fig. 4.11.: Free-standing InP membrane after the membranization step: (left) SEM image of a cleaved device region: the photonic crystal pattern in the air-suspended InP membrane on the top, the thermal glass layer etched under the membrane in the middle, and the Si substrate under the glass at the bottom; (right) 3D cross-sectional representation of a single device region.

4.4 Chapter summary and final considerations

After a numerous optimization and processing runs and 3 device generations, the most important fabrication elements for a working buried heterostructure photonic crystal laser have been presented here. The issue of the alignment accuracy achievable on the bonded wafers analysed in the previous chapter has been nicely illustrated by a consistent alignment accuracy improvement throughout laser device generations. Before continuing with the laser characterisation, next chapter is dedicated to a detailed examination of the buried heterostructure formation by the dry etching and the re-growth processes.

5 Etching and (Re-)growth

A buried heterostructure for optical mode and carrier confinement in semiconductor lasers can be made in two ways: (1) by starting with a passive material layer only, in which an opening in a masked region is formed, and then growing an active material inside, followed by a mask removal and complete encapsulation by an overgrowth process; (2) by starting with active/passive material layer structure, which is covered with the mask in specific places, and then removing all material by etching around the mask, followed by re-growth of solely passive instead of removed active/passive material for encapsulation. Both approaches employ the selective growth mechanism on non-planar wafer surface [136]. The first method, however, requires a challenging thickness and composition control, which makes it difficult to produce high-quality active material inside localized regions for devices, as described in detail elsewhere [137]. This work takes the second approach which has been applied with great success to many high performance semiconductor laser devices, as described in chapter 2 section *Laser structures for optical and carrier confinement*. Bringing about this high-quality integrated devices with small scale buried heterostructure regions embedded into the photonic crystal cavities is a demanding task which is worthy to look at in detail.

This chapter is aimed at describing the main principles of etching and re-growth mechanisms employed in the buried heterostructure formation, and optimization efforts to establish and to understand the underlying optimal conditions. High performance on-chip active devices are possible only if both of these parts are realized equally well.

5.1 Equipment: dry etching and epitaxial growth

Before proceeding with a detailed discussion about the buried heterostructure formation, this section briefly introduces general principles

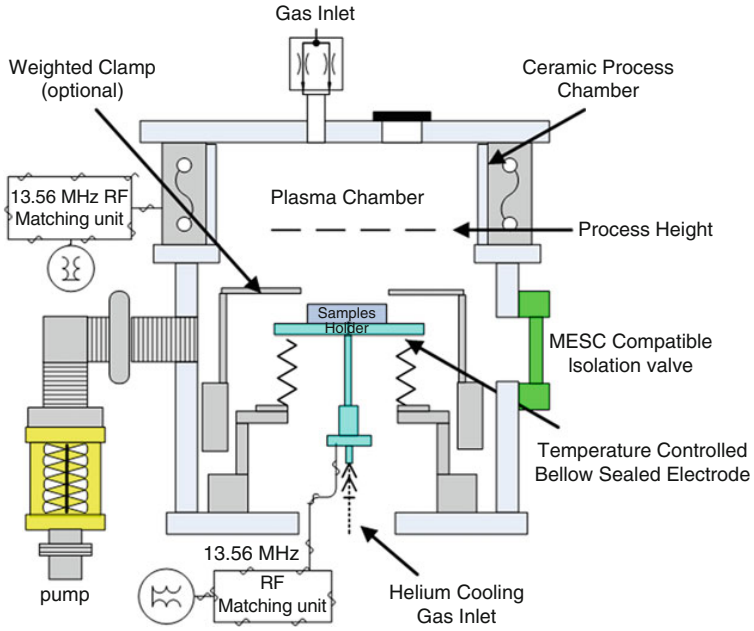


Fig. 5.1.: Schematic diagram of the ICP etching system. Reprinted from [138].

of the main equipment used for this purpose: ICP-RIE for dry etching and MOVPE for epitaxial growth and re-growth.

Dry etching with ICP-RIE. The high-density inductively coupled plasma (ICP) etching system is the improvement of the standard reactive ion etching (RIE) method. While the main working principles remain, as the system generates plasma containing highly reactive radicals and ions, which are then accelerated towards the electrode on which the sample is placed, the high-density plasma system uses two separate power supplies for independent control of plasma generation (ion and radical flux) in the chamber and acceleration (ion energy) towards the platen electrode (Fig. 5.1). This results in $2-3$ orders of magnitude larger density of radicals and ions in an ICP than in standard RIE with reduced chamber pressure and ion bombardment energies, meaning that anisotropic etching with high rates and minimal sample damage can be achieved. Overall, the process becomes more controllable and flexible.

Wafers are loaded into the load-lock before entering the ICP etch chamber, which speeds up the loading process by reducing the pump time

needed to achieve low system pressure. The wafer handler requires 4" substrates, which means that standard 2" InP wafers (or smaller chips) used for the device fabrication in this work have to be placed on larger Si carriers. Surprisingly, the wafer carrier can have notable influence on the etching process, which has to be accounted for. In addition, the platen temperature of the ICP system used in this work can be heated up to 180 °C which is very important for halogen-based etching chemistries. This and other specificities will be discussed in depth further in this chapter.

The final note is that while etching of the photonic crystal holes for the devices used in this work is performed with previously optimized RIE method and results in sufficient quality, achieving smooth post-etch surface with little damage required for subsequent material re-growth to form the buried heterostructure relies on ICP characteristics. Thus, its overall importance in the device processing scheme should not be underestimated.

MOVPE growth. Epitaxial growth of semiconductor materials, where crystalline layers are formed in an ordered manner on epi-ready substrates, is ordinarily performed by one of two mainstream methods: metal-organic vapour phase epitaxy (MOVPE)[1] and molecular beam epitaxy (MBE). Whereas the later technique utilizes a directed flux of atomic source materials in ultra-high vacuum, MOVPE is just the opposite, involving chemically reacting flow of metal-organic, hydride and carrier-gas precursor mixtures. Material growth process in the MOVPE is exceedingly complex and more times than not based on the trial-and-error method. However, simplified "virtual reactor" models capturing the most important features of the system have been developed and they provide valuable basic physical/chemical understanding [139].

A schematic of the rotating disk reactor-type MOVPE system utilized in this work is shown in Fig. 5.2. Group III and V species carried by H_2 gas are injected into the system, where they are mixed and directed onto the rotating heated substrate. There, the reactants progress through a number of different processes such as dissociation (cracking) into elemental group III and V species, surface and gas phase diffusion, adsorption to and desorption from the surface, until they are finally incorporated into

[1] In literature, alternative process names are metal-organic chemical vapour deposition (MOCVD), organometallic vapour phase epitaxy (OMVPE) and organometallic chemical vapour deposition (OMVPE).

the growing structure. Exhaust gas is then sent into the filter (scrubber system), which removes highly toxic unreacted species.

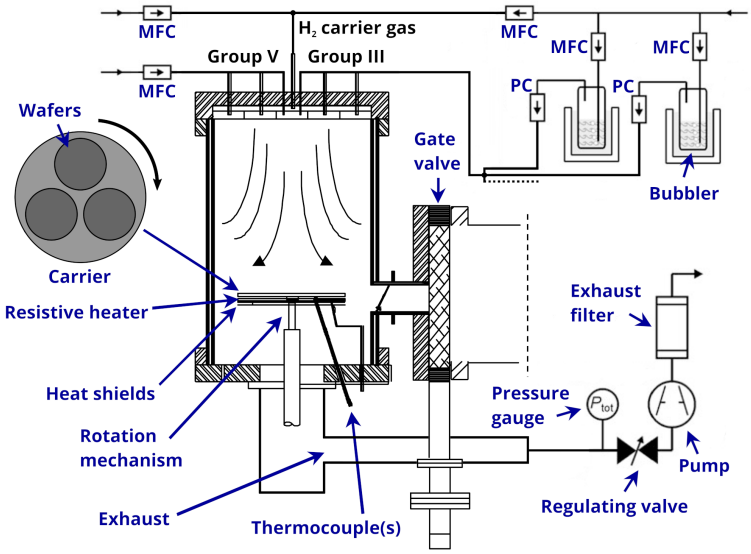


Fig. 5.2.: Schematic diagram of the rotating disk MOVPE reactor. MFC stands for mass-flow controller, PC for pressure controller. Adapted from [92, 140].

MOVPE is typically operated in the mass transport (group III) limited regime at around $600 - 650$ °C, with a group V overpressure (V/III ratio $\gg 1$) to prevent its loss from the growing compound. Conventionally used group V sources are hydride gases such as PH_3 and AsH_3. Group III sources are metal-organic alkyl compounds such as TMIn (solid), TMGa and TMAl (both liquid). They are contained in the temperature-controlled bubbler vessels, through which the carrier gas H_2 is passed and transported to the chamber in the vapour form.

This chapter is focused on a more specific type of epitaxial process in which non-planar selective material growth is performed [136]. This post-etch re-growth ultimately completes the buried heterostructure fabrication enabling to proceed with the last processing step, formation of the photonic crystal.

5.2 Buried heterostructure fabrication by etching

Once the designed glass-like HSQ mask pattern is defined on the sample surface (chapter 4 section *Optimized fabrication process overview*), the next step is to remove the active/passive material layers around to form mesa structures[2] with remaining active regions, which will then be buried by the re-growth step. The aspects of etching in the formation of these mesas are discussed next.

General aspects of wet and dry etching. There are three possible ways of removing material layers surrounding mesa-structures in forming the buried heterostructure: using solely wet etching, dry etching, or a combination of both. Material re-growth is highly sensitivity to the surface roughness, therefore a high etch quality is of utmost importance no matter the process choice. Besides that, there are additional expectations for the etching: process should be well controlled, so that the active material is fully removed while still enough of passive material is left below; it should be simultaneously suitable for removal of desired materials with enough of selectivity towards the mask; it should be uniform across the wafer. Below, the pros and cons of material removal methods are weighed and discussed.

On top of the list is the requirement to produce smooth and defect-free top remaining material surface after the etch. During epitaxial growth, the surface acts as a template by providing nucleation sites for atoms, and although high growth temperature and other conditions are typically chosen to promote surface material reorganization and recovery of the damaged crystalline structure, excessively poor initial surface quality would generally remain even after the re-growth. Due to its inherently chemical nature, wet etching does not deteriorate electronic surface quality, and is thus suitable for this process. As a possible downside, any existing damaged material region or defects would be preferentially attacked, resulting in unevenly etched surface. Dry etching, on the contrary, degrades the electronic surface quality by means of mechanical displacement and ion-induced damage to the crystal lattice, or by micromasking effect as a mask or low-volatility III-V material is re-deposited on the sample surface. However, it is much less selective to local material quality variations.

[2] A mesa is a structure with a flat top and steep sidewalls, and is protruded above the area surrounding it.

Besides the top remaining surface, producing smooth, damage-free and vertical profiles is another desirable aspect. This is especially the case for small structures where the sidewall area makes a significant portion of the total surface area, so that the interfacial effects become more pronounced. In forming the buried heterostructure, the material is eventually re-grown around the etched regions. While some passivation procedures are supposedly taken before the interfaces are encapsulated [141], the fact that in the end these are not exposed to the ambient makes the complete device significantly more resistant and stable.

Highly controllable etch process is one of the main reasons for choosing dry over wet type of etching, especially considering typical small mask dimensions used in this work. For wet etching, dimensional control is limited due to mask undercut, while profile control is either diffusion- (isotropic) or reaction- (anisotropic) rate limited, which in the later case depends on the mask shape and orientation with respect to crystallographic material planes. On the other hand, when using dry etching the dimensional and profile control can be achieved much more easily, as the physical and chemical etch mechanisms can be adjusted by changing various plasma parameters. If the physical component is dominating, the etching is highly anisotropic, whereas increasing chemical contribution leads to isotropic etching with increased mask undercutting, while also smoother sidewalls.

In addition, if the buried heterostructure is being fabricated on already bonded wafers, where thin III-V material layers are integrated on silicon [114], there is a difficulty in vertical (depth) process control. The upper constraint is set by the requirement to fully remove the active material, while the lower one is that there has to be still enough of passive material left after etching for the consecutive regrowth[3]. Wet etching process fully depends on precise timing calibration and well regulated environmental conditions, while dry etching can be monitored in real-time with dedicated end-point detection techniques.

The choice of specific etchant chemistry depends, on the active and passive materials to be removed. In case of wet etching, the use of a few separate solutions for different layers would most probably be needed, which increases the count of sample handling steps. On the bright side, high selectivity between materials, including the mask, could relax requirements for the vertical dimensional control. If the etching becomes

[3]More details about the importance of these limits are provided further in this chapter.

self-limiting after reaching etch-stop layer for particular etchant, accurate control is then only needed for the last layer. Horizontal dimensional control is a serious difficulty, especially for quantum wells, because of different etch rates of wells and barriers [142]. Dry etching is generally a more universal method, where suitable etchant combination can be used for multiple different materials simultaneously. On the other hand, selectivity towards the mask is much worse, especially if the physical dry etching component is dominant.

Etch uniformity is a concern for the dry etching systems. Even though it is expected that a uniform flux of reactants is produced across the surface of the platen electrode, differences in the consumption rate of reagents at the sample, carrier wafer and the platen lead to etch non-uniformities generally known as loading effects. At the micro scale, etch rate varies locally in the vicinity of masked regions or trenches (etch lag), and it depends on the ratio between masked and exposed surface area or opening depth. At the macro scale, this shows up as monotonous etch depth variations from the sample centre towards its edges. These variations can be reduced by placing the sample on a larger wafer of the same (or similar) material, which is unfortunately hard to accomplish for many III-V materials when etching full-sized (usually 2") wafers, as oftentimes larger sizes are commercially not available or very expensive to produce. Etch non-uniformity can also exist for the wet etching, if the sample is damaged or defective. Moreover, if the process is transport-limited, agitation is needed to avoid problems associated with transfer/removal of species to/from the surface.

Summing up, both wet and dry types of etches seem to have very appealing, but also unfavourable features. In principle, complicated process control and undercutting are the major drawbacks of the wet etching, while it is mainly the surface damage that limits the employability of dry etching. Seeking supporting examples, the photonic crystal laser devices with the active region structure inside the cavity formed by only wet etching have been reported [127, 143], although the final structure technically should not be called the buried heterostructure. Potential reliability issues exist due to the active region being exposed to the ambient, and the process reproducibility is supposedly limited as well as not easily scalable. A combination of wet and dry etching in fabricating record-performance buried heterostructure photonic crystal lasers have been reported by NTT [39], although little information has been provided with regards to fabrication

procedure. For solely dry etching, no working compact laser devices of this type have yet been reported. This work aims at this category, as the dry etching is the main chosen method for the mesa-structure formation, only using a mild surface wet etching/cleaning prior to the material regrowth.

Dry etching chemistries for InP materials. A variety of chemistries exists for the dry etching of III-V compounds, however only a few, mainly based on methane/hydrogen and halogens (chlorine and bromine), have been explored in greater detail for the InP and related materials. These particular chemistries are overviewed and compared here.

Methane/hydrogen (CH_4/H_2) is a standard choice for InP/InGaAs(P) etching in RIE systems. While sufficiently good sidewall surface quality and etch anisotropy can be achieved, a number of serious drawbacks exist for methane/hydrogen etching: slow etch rates [144, 145]; indium enrichment [144, 145]; hydrogen passivation of donors and acceptors [146]; very slow etch rates of Al-containing compounds [147] due to low reactivity with the etchant and rapid Al oxidation in the presence of O_2 used for polymer removal; excessive deposition of carbon-based polymer on mask edges may cause overcut and/or curved sidewall profiles [148], as well as limited etching inside narrow tranches, small holes and other enclosed structures. Related to the previous, and more technologically important aspect is the deposition of amorphous-carbon on the RIE chamber walls, requiring frequent periodic O_2 plasma cleaning.

Cyclic RIE methane/hydrogen ($CH_4/H_2 = 1:4$) etching with intermediate O_2 plasma cleaning steps has in fact been extensively used in this work for fabricating photonic crystal holes, based on previously optimized recipe [149, 150]. Unfortunately, the major drawback of this chemistry associated with inability to etch Al-containing layers made it difficult to fabricate photonic crystal buried heterostructure devices with InGaAsP/InAlGaAs quantum wells. Any overlap between the active material region and the photonic crystal results in holes etched only from the top side (Fig. 5.3). Impartial structure obviously drastically reduces cavity Q-factor and could possibly lead to non-lasing device. While this reason not only did not allow testing the influence of laterally enlarged buried heterostructure quantum well regions on the device performance, even more importantly, any larger misalignment (chapter 4 section *Buried heterostructure device processing generations*) affected the etching of holes, and thus device performance.

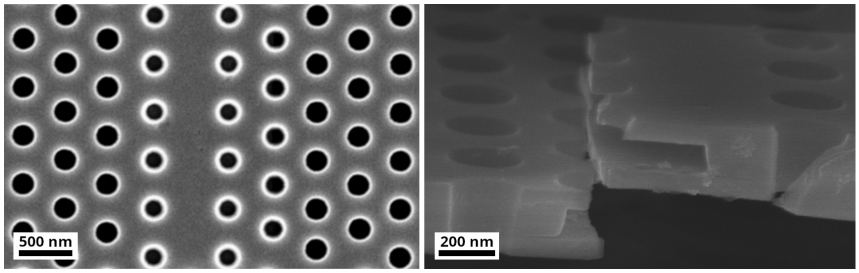


Fig. 5.3.: SEM images of the photonic crystal cavities with Al-containing quantum wells buried heterostructure etched with CH_4/H_2 chemistry in RIE: (left) top-view of the sample with enlarged buried heterostructure region overlapping inner photonic crystal holes which are etched differently (bright rings around the edges); (right) cross-section of the broken cavity region with selectively etched quantum wells which reveals that holes are etched only from the top side.

Chlorine-based chemistries (Cl_2, BCl_3) are used in both conventional RIE and ICP systems. The main disadvantage of these etching chemistries is the high-temperature requirement (>100 °C) due to low volatility of $InCl_x$ [146], resulting in group V-deficient surfaces and pronounced micro-masking ("grassy" surface) effect. In addition, pure Cl_2 leads to significant mask undercut, therefore addition of other gases is needed for InP surface passivation and reduced lateral etching. For example, addition of H_2 was shown to enhance sidewall passivation with Si-rich amorphous layer either when Si wafer was used as a sample tray [151] in the commercial ICP system or independently of sample carrier by adding Si-containing gases such as SiH_4 [152].

Bromine-based chemistries (Br_2, or mostly HBr) have historically been used less, and only relatively recently started attracting more attention [144, 145]. A possible reason is that Br-containing gases are very corrosive to gas pipes [146]. Other downsides are similar to those of chlorine-based etches, such as significant undercut when pure HBr is used, thus needing additional gases for passivation, etc. Reported vapour pressures of $InBr_x$ species are relatively lower than their counterparts with substituted Cl [153, 154], and although volatility generally correlates with etching rate, the more important aspect is the volatility under ion-enhanced conditions. Using HBr provides both halogen- and hydrogen-driven etching mechanisms with Br atoms controlling the ion-assisted chemical reaction rate [155, 156]. In addition, combining HBr with CH_4 can be beneficial

for obtaining better surface quality and stoichiometry as methane can enhance the removal of group-III element In through the formation of volatile $(CH_3)_3In$ (TMIn) species, while simultaneously promoting more anisotropic etching through the formation of passivating polymer layer due to increased fraction of C [157] or H_2, if the Si carrier wafer is used [151].

Optimization of HBr-based InP materials etching. Based on previous considerations of various chemistries conventionally used for dry etching InP and related materials, a number of tests were performed in the ICP to find the most suitable candidate for etching mesa-structures to form the buried heterostructure. Initial results using chlorine-based chemistries BCl_3 and Cl_2 were unsatisfactory due to considerable surface roughness and an abundant formation of particulates of unknown origin. On the other hand, HBr at once showed very promising results with smooth InP material surface after the trial etching. Henceforward, it was decided to focus on HBr-based recipe optimization.

The optimal etching recipe parameters and the main experimental findings are:

- ☐ The chemistry is $HBr/CH_4/Ar$ with flows of $10/5/2$ sccm[4], coil and platen powers set to 600 and 50W, respectively, and the chamber pressure set to 5 mTorr. Chapter 7 contains more information regarding the influence of the parameter changes, such as CH_4 flow and addition of other gases.

- ☐ The wafer is heated and kept at 180 °C (maximum temperature of the system) throughout the material etching to promote an effective removal of In etch products from the surface, as discussed previously. It was found that almost no etching occurs at room temperature, while it is also suspected that uncontrolled sample heating results in decreased surface quality.

- ☐ Prior to device sample etching, the chamber is thoroughly cleaned by running a 30 min long cleaning recipe based on O_2 plasma, and afterwards the chamber is pre-conditioned by running the HBr etching

[4] Standard cubic centimetres per minute.

recipe for 15 min with the dummy Si carrier wafer inside the chamber. Essentially, the chamber walls are coated with the etching species during preconditioning, so that consistent etch rates can be achieved during the actual run. This is especially important for reproducible short duration etches requiring precision, as otherwise the etchants would be simultaneously consumed by the chamber walls.

- Prior to the HBr etching, the sample surface is gently treated with the oxygen plasma in a barrel-type etching system to remove any possible organic contamination which could affect the etching, and then crystalbonded to a dedicated clean 4" Si carrier wafer. Using the 4" Si carrier is necessary due to the construction of the ICP handling system, while Si also plays an important role in enhancing etch anisotropy as discussed before. Crystalbonding is crucial to guarantee a proper contact and heat transfer between the InP sample and the carrier wafer, which is cooled by helium gas flow from the backside. Simple placement is not enough in guaranteeing reproducibility, as any particles or other reasons preventing contact in between the surfaces would result in poor InP sample cooling.

- During the process run, etching is monitored in real-time by using the laser interferometry etch depth monitoring system Intellemetrics LEP 400, and the data is recorded and compared with the constructed sample structure model in "EtchDirector" software package [158]. The process is stopped manually when the required depth is reached.

- After the sample is unloaded from the chamber, it is immediately dipped into de-ionized water to remove the remaining Br species from the surface that would otherwise react with air, form HBr and continue sample etching. Although no specific tests were made to prove its importance, it is generally a good practice for reproducibility.

Experimental data for the etch depth and rate for a number of calibration and device samples with different active material layers is collected and plotted in Fig. 5.4. The data for these graphs is obtained either by the analysis of the recorded process runs with the interferometric system, or by pre- and post-etch thickness comparison, measured with the ellipsome-

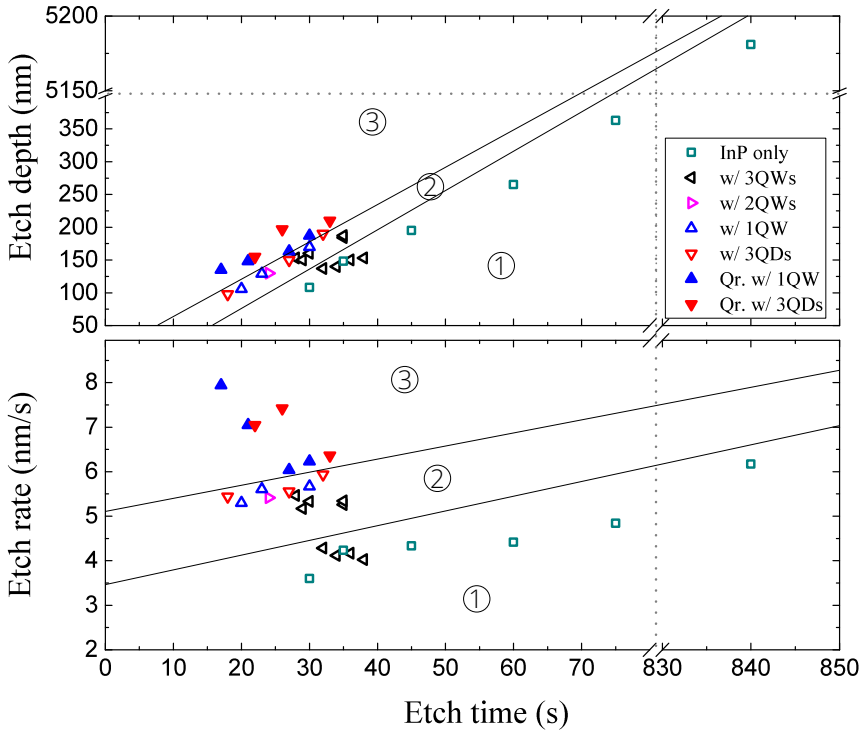


Fig. 5.4.: Etch depth (top) and etch rate (bottom) dependence on time. Open symbols represent results obtained when using 2" wafers, closed ones are for quarters (Qr.) of a 2" wafer. The legend indicates the type of sample used: InP only or InP with an indicated number of active material layers (nQWs: n layers of quantum wells, nQDs: n layers of quantum dots). The graphs are approximately divided by guidelines into three regions, the meaning of which are explained in the text.

ter. The graphs are artificially divided by guidelines into three regions: (1) the region below the lower guideline represents process development period during the initial recipe calibration as well as when the behaviour of the ICP system was unusual, and the processes were run at wrong chamber pressure ($1-2$ instead of 5 mTorr); (2) the region in between the guidelines correspond to the ordinary processing conditions; (3) the third region above the top guideline is for the samples with reduced dimensions (quarters of a 2"). A few conclusions can be drawn. First, it seems that active layers do not have observable influence and InP, InAs quantum dots/wetting layers, and InGaAsP/InAlGaAs quantum wells all have very similar etching rates for this optimized HBr recipe. Secondly, as intuitively

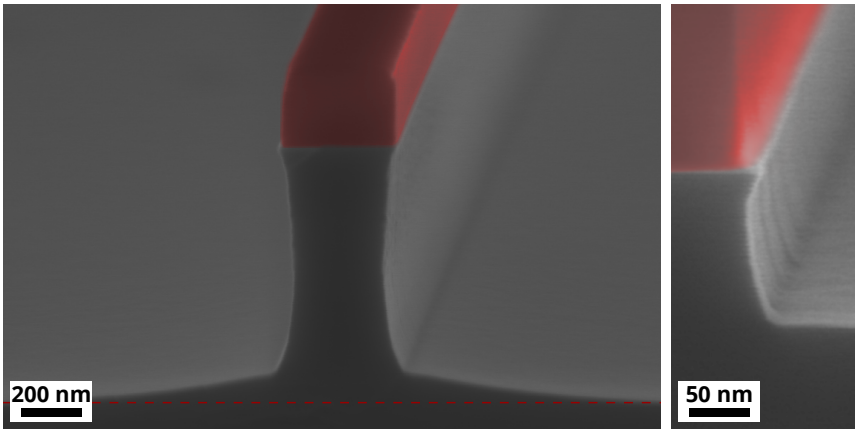


Fig. 5.5.: SEM cross-section image of the buried heterostructure-like profile after the optimized HBr etch in ICP: (left) prolonged 2 min etch; (right) 30 s etch, representing the typical process run time during the actual buried heterostructure fabrication. HSQ mask is artificially coloured in red.

expected, using smaller samples (quarters of a 2" wafer) leads to increased etching rates due to reduction in the etch load. Finally, etching rate seems to be lower for the samples etched at reduced chamber pressure, agreeing with previously reported values for HBr chemistry in this range [144, 153].

A close-up of the buried heterostructure-like profile after the HBr etch using the optimized recipe is presented in Fig. 5.5. Etching seems to produce concave, rather symmetric profiles, with an angle between the surface and the sidewall around $87°$ for the top, and $95°$ for the lower part. Shorter etching used for the actual buried heterostructure fabrication results in larger asymmetry and larger lower part angle. The etch lag effect is clearly visible on the left side of Fig. 5.5 as "foot" around the structure. It is undesirable, however unavoidable effect which makes it more difficult to accurately estimate when the process run should be stopped, as some of the active material might still remain in the "foot" region even though it is fully removed further away. Incomplete active material removal around the fabricated buried heterostructure region is visible under careful inspection of the cross-section in Fig. 5.3 (small "foot" on the bottom of selectively wet etched quantum wells region).

It is difficult to evaluate sidewall roughness quantitatively, however it seems to be overall quite smooth, with larger observed roughness for the shorter etch. Inspecting the top surface quality, on the other hand, is much

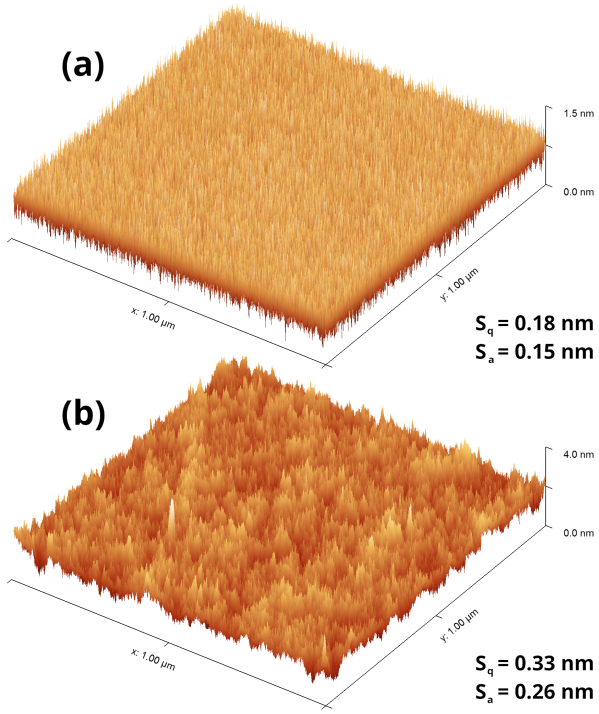


Fig. 5.6.: AFM scans of 1 μm^2 InP surface area together with given RMS (S_q) and mean (S_a) roughness values: (a) after initial MOVPE growth; (b) after 30 s etch using the optimized HBr recipe.

easier and has been done using AFM. Fig. 5.6 compares the InP sample surface before and after the HBr 30 s etch. As can be seen, the surface stays very smooth, with approximately only doubled roughness values. These compare vary favourably with experimental HBr/Ar etch results found in literature [144, 145], indicating appropriately chosen process parameters with beneficial influence of added CH_4. The obtained results are very promising and suitable for subsequent material re-growth in the MOVPE for the buried heterostructure fabrication.

Etching limits for successful re-growth. The real challenge associated with material removal in forming mesa-structures is an accurate etching time control (and correspondingly depth), so that the process run is stopped in the optimal region; coloured in green in Fig. 5.7 (middle). Continuing with the InP re-growth after stopping before the minimum etching limit

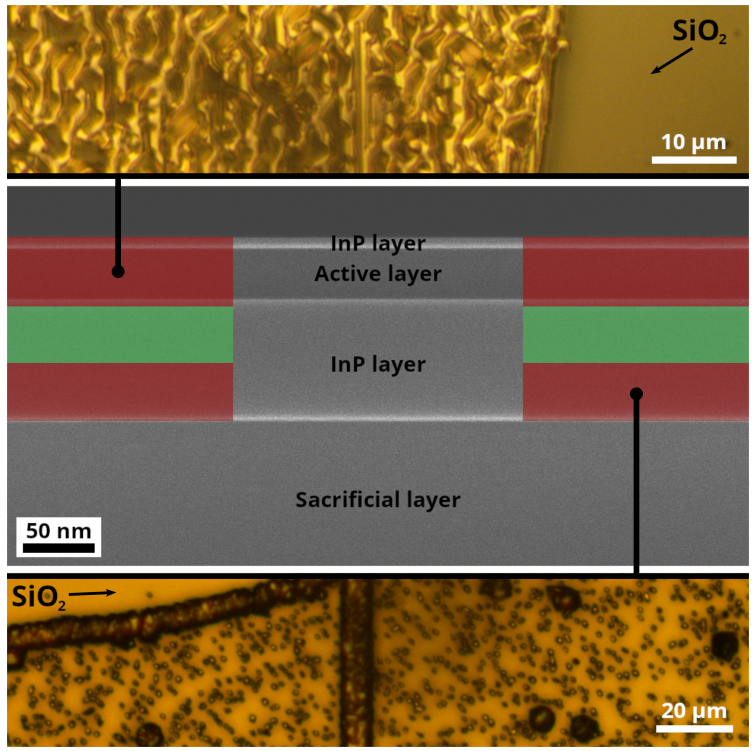


Fig. 5.7.: Etching limits highlighted in the sample structure (middle) used for the buried heterostructure fabrication. Artificially coloured parts correspond to: (1) upper critical region (top red); (2) optimal region (green); (3) lower critical region (bottom red). (Top) Optical microscope image representing failed re-growth after the etching was stopped in the upper critical region. (Bottom) Optical microscope image representing failed re-growth after the etching was stopped in the lower critical region.

(Fig. 5.7, in the top red coloured part) or after the maximum etching limit (Fig. 5.7, in the bottom red coloured part) would result in failure.

Upper critical region, before the minimum etching limit is reached, is bound by the active material. In principle, this also includes the "foot" near the etched mesa-structures due to the etch lag effect (constituting roughly 10% of the total region thickness). The optical microscope image in the top part of Fig. 5.7 was taken after failed re-growth as the HBr etching was stopped too early and resulted in incomplete InGaAsP/InAlGaAs quantum wells removal. While not all active materials would cause the same result, Al-containing compounds rapidly oxidize in the ambient and become hard to de-oxidize during the short re-growth process, resulting in severely dis-

torted and deformed re-grown InP layer not suitable for further processing.

Lower critical region lies just below the optimal one, and corresponds to the minimum required InP thickness above the sacrificial layer for successful re-growth. It has not been verified and in fact it is not expected that this region exists when the lattice-matched (to InP) InGaAs is used as the sacrificial layer in the processing scheme where bonding is performed after the re-growth. However, it is an important aspect for the directly bonded sample, where the III-V material layers are being processed on the Si wafer with thermal SiO_2. Performing re-growth on the sample having less InP left than needed results in material clustering into droplets (Fig. 5.7, bottom optical microscope image) which resembles epitaxial growth of materials with largely mismatched lattice constants (e.g., InP on Si or SiO_2). Careful experimental investigation revealed that there has to be at the very least 25 nm of InP material template left on SiO_2 to obtain good quality InP after re-growth. In case surface wet etching/cleaning treatment is used before the re-growth, additionally removing some more InP material ($\sim$15 nm for 3 min concentrated H_2SO_4 as discussed in detail in the next section), then the minimum value becomes larger (in this specific case, $\sim$40 nm). For now it is not clear why this minimum limit exists, requiring a more detailed analysis.

As can be seen, the optimal region in which the dry etching has to be stopped (Fig. 5.7, green part) is rather narrow, which puts strict process control requirement on the etching. For a typical region thickness below 50 nm and assuming a round etch rate value of 5 nm/s (Fig. 5.4), the etching has to be stopped within less than 10 s after passing over the boundary between the upper critical and the optimal regions. This 10 s value includes the uncertainty in the structural model due to limited knowledge of the material thicknesses and refractive indices, etching non-uniformity across the wafer, delayed ICP system response to the control, etc., thus making material etching more challenging task than it might initially appear.

Visible in both optical microscope images in Fig. 5.7 are also SiO_2 regions that appeared as defects during the bonding. After re-growth they remain smooth and mostly not covered by InP (except some possible individual crystalline particles) as expected from the selective area growth mechanism which is discussed in detail in the following section.

5.3 Material re-growth

Material re-growth is the final step towards realizing the buried heterostructure which can then be implemented with the device design. This section starts with a brief explanation of the surface preparation before the re-growth, and then proceeds to describe a two-step re-growth process needed to produce planar surface suitable for devices.

Surface preparation. The desired function of chemical etching/cleaning before the material re-growth is many-fold: it is supposed to clean the surface from organic residues and other contaminants, which can later affect device performance, but are also undesirable in the MOVPE reactor; it should remove the native oxide as a preparation for further material growth or surface treatment such as passivation; it should etch away material damaged during the dry etching. The second step, thermal cleaning, can then be performed inside the MOVPE reactor before the actual growth takes place. Its main purpose is the complete disposal of the remaining oxidized layers, and in addition surface material reorganization.

While Si surface preparation procedures with RCA1 and RCA2 solutions are highly standardized, efficient wet etching/cleaning and oxide removal of III-V materials is by far less definite. From the procedures investigated in literature, the majority of them focused on the planar top binary III-V semiconductor surface [159–162]. Much less attention was paid to properly optimize the treatment of ternary or quaternary surfaces which are opened, for example, during the buried heterostructure fabrication, with suggestions for Al-containing layers ranging from using simply HF [163], to much more demanding three-step process involving solutions of bromine-methanol, sulphuric acid-hydrogen peroxide-water and finally BHF [164]. Concerning InP, it has been demonstrated that oxide-free (100) surfaces can be obtained with a two-step chemical etching process, where first H_2O_2-based solution oxidizes the surface [159, 161] and then acid or base is used to etch it away [159, 162]. Methods of using either low concentration HCl as well as H_2SO_4 with very small surface etch rates [162] or strong acid solutions were both shown to be able to remove the surface oxide [160]. Unlike when the HF solution is used for the oxide removal, hydrophobic hydrogen-terminated surfaces are created after HCl or H_2SO_4 treatment which is desirable to reduce the possibility of later

re-oxidation of the wafer or re-contamination by carbon [160]. It should be noted that only undamaged InP (100) surfaces were considered in all of these investigations, and the results regarding etch rates might be drastically different if processed device samples were used.

Limitations on wet etching/cleaning solutions used for the device processing described in this work are imposed by the buried heterostructure. HCl and H_2O_2 would etch quantum well and quantum dot active layers exposed from the sides of the mesa-structures etched in the ICP. Difficult control of the wet etching process is highly undesirable and is exactly the opposite that this work is aiming for. Therefore, the wet etching/cleaning procedure based on previous considerations, but tailored to this work consists dipping the sample into the concentrated H_2SO_4 for 3 min, then rinsing it with de-ionized water followed by thorough 3 min cleaning in water bath with strong injected N_2 stream. The determined etch rate is non-linear while also dependent on the material quality, as around 15 nm of ICP-damaged InP is removed during 3 min in H_2SO_4 before the 1^{st} material re-growth, with this value dropping below 10 nm afterwards (before the 2^{nd} regrowth).

Immediately after the initial surface preparation steps, the sample is loaded into the MOVPE load-lock which is then pumped down to high vacuum. As a part of the re-growth procedure, the sample is thermally annealed (cleaned) inside the MOVPE reactor by keeping it at 650 °C for 15 min under phosphine atmosphere to prevent desorption of phosphorus from the InP surface. These conditions correspond to typical de-oxidation process step used under conventional sample growth in the MOVPE and therefore were transferred to the re-growth process without significant modifications. The influence of numerous annealing parameters on the InAlGaAs/InP buried heterostructure laser performance were studied earlier [165], and it was shown that 650 °C temperature and PH_3 atmosphere conditions resulted in the lowest non-radiative recombination velocity and the highest device performance. On the other hand, the optimal annealing duration was determined to be between 30 and 60 min. Keeping in mind that the buried heterostructure devices described here are fabricated on the InP layer bonded to the Si substrate, and extended high temperature exposures might have detrimental effect to the material quality and subsequent alignment accuracy, 15 min annealing duration is retained as a compromise between the two aspects.

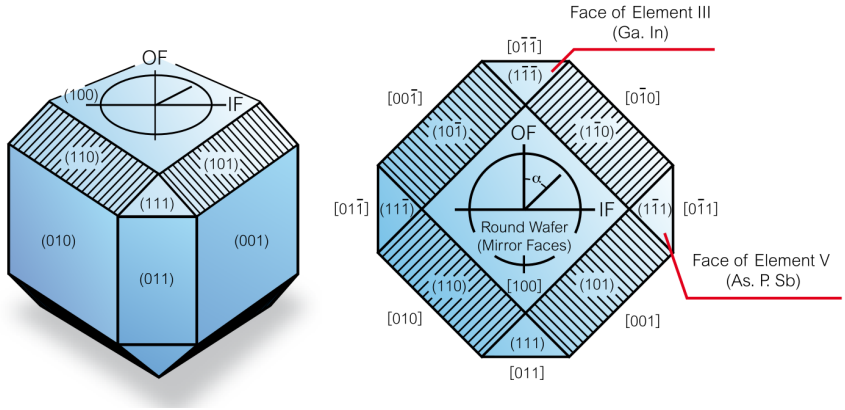


Fig. 5.8.: Cubic (left) and planar (right) representations of the crystallographic planes corresponding to InP wafers used in this work. OF and IF denote major and minor wafer flats, respectively, in EJ (European-Japanese) convention. Adapted from [167].

Two-step re-growth process: selective area growth and planarization Material re-growth for the buried heterostructure formation is a two-step process: (1) the purpose of the first one is to re-grow InP instead of etched active layers, and is called the selective area growth (SAG) or the selective area epitaxy (SAE), because material deposition is inhibited on top of the mesa structure by an insulating mask [136, 166]; (2) the second re-growth step is performed after the mask removal, and is needed for surface planarization.

Three different buried heterostructure orientations on the wafer have been investigated: parallel to the major flat ($[0\bar{1}1]$-direction, Fig. 5.8), $45°$ rotated ($[001]$) and perpendicular ($[011]$). AFM surface scans after the 1^{st} MOVPE re-growth and glass-like HSQ mask removal are shown in Fig. 5.9 (left) for 3 μm length and 350 nm width buried heterostructure to be implemented into the L7 line-defect photonic crystal cavities. Similarly, Fig. 5.10 (left) represents the same surface regions after the 2^{nd} regrowth.

First of all, the characteristic growth enhancement effect is clearly visible around the buried heterostructure regions in Fig. 5.9. Cross-sections of the surface scans (Fig. 5.9 (right)) reveal that the excess growth thickness is around 25 nm for this particular sample (the origin for the vertical direction is taken at the top of the buried heterostructure, so that it corresponds to the initial wafer surface before any processing). Its extent in the lateral direction is from 2 to >4 μm, limited by the AFM scan size,

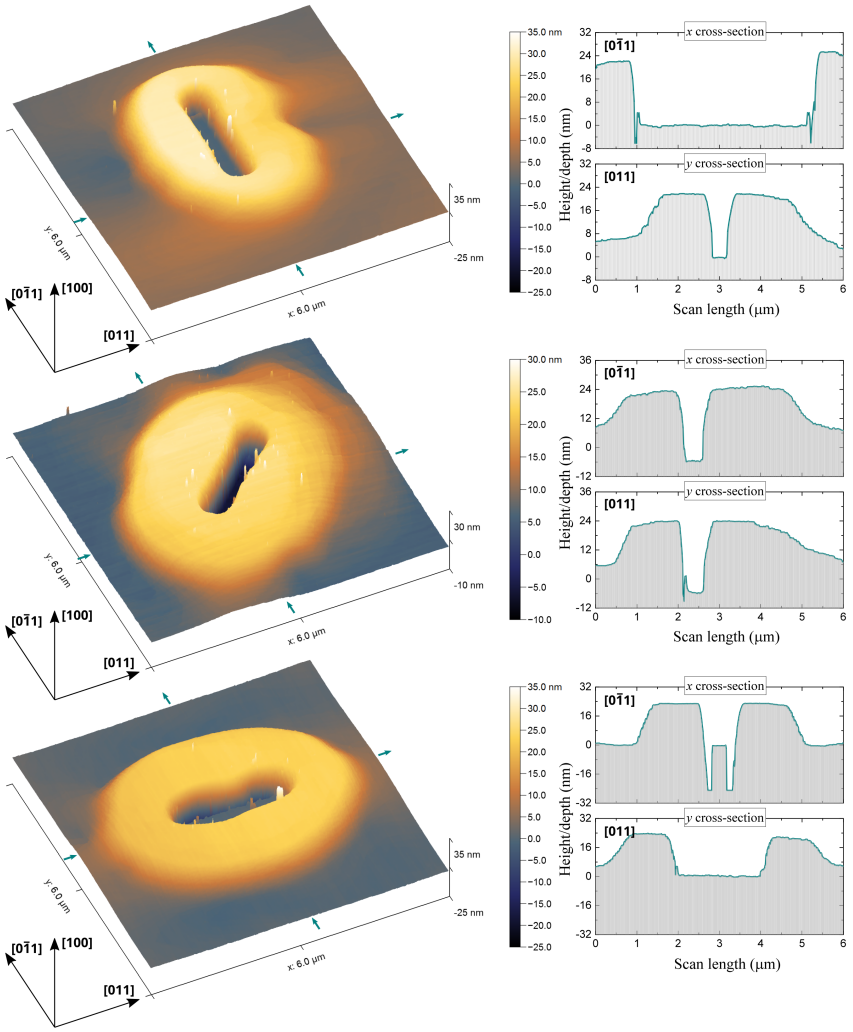


Fig. 5.9.: AFM surface scans (left) and cross-sections (right; positions are indicated by teal coloured arrows on the surface edges) of differently-oriented 3 µm long and 350 nm wide buried heterostructure regions after the 1st MOVPE re-growth. The glass-like HSQ masks have been removed.

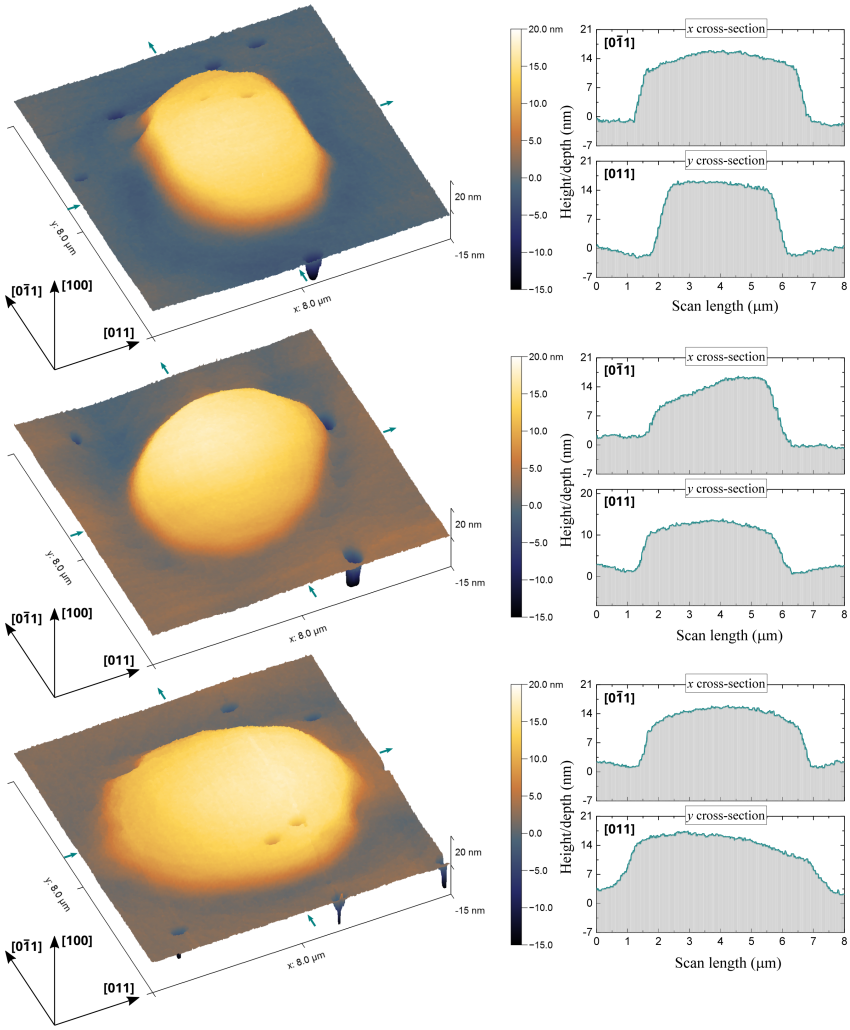


Fig. 5.10.: AFM surface scans (left) and cross-sections (right; positions are indicated by teal coloured arrows on the surface edges) of differently-oriented 3 µm long and 350 nm wide buried heterostructure regions after the 2nd MOVPE re-growth.

and is dependant on the buried heterostructure orientation. While the selective area growth experiments using a gap of several micrometers opened between two mask stripes showed effective diffusion lengths on the order of tens of micrometers [136, 168], the results presented here imply that much smaller extent of the growth perturbation is imposed by small buried heterostructure masks. Furthermore, by approximately comparing height/depth values above the buried heterostructure and outside where the excess thickness drops towards unperturbed growth thickness (measured across the diagonal cross-sections for the extended range, not shown here), it can be stated that the InP material re-growth instead of the etched active/passive layers was accurate to within 5 nm for this sample. Re-growth precision is of course desired to reach the intended final device thickness.

After the 2^{nd} material re-growth (planarization) shown in Fig. 5.10, surface around the buried heterostructure regions was surprisingly found to be non-flat. The height of these protruded features are approximately $10 - 15$ nm for this sample, as indicated by the surface cross-sections (5.10 (right)). This result is rather puzzling, because it was originally expected that accurate 1^{st} re-growth would automatically lead to the planar material surface after the 2^{nd} re-growth. Interestingly, some other fabricated samples (not measured by the AFM) which were accurately re-grown during the 1^{st} step had such pristine surface quality and flatness after the 2^{nd} re-growth that the buried heterostructure regions were not visible by any used surface imaging method. Only light emission measurements during the photonic crystal laser characterisation confirmed their indeed very successful fabrication. Generally, no clear correlation was found between the accuracy in thickness of the re-grown material and the final surface flatness.

A solution to this problem of obtaining flat sample surface after the buried heterostructure fabrication might be implementation of the controllable *in-situ* etching during the material re-growth in the MOVPE, as was examined for InP by introduced carbon tetrabromide [169] or tertiarybutylchloride [170] into the reactors. Such methods could possibly be applied for pre-etching protruded regions before continuing with the planarization growth. An added benefit is the possibility for more flexible sample surface cleaning procedure.

Finally, it is worthy to point out that the size of the excess growth

region also depends on the buried heterostructure mask orientation. It was found to be the largest along the $[011]$ direction. It is an important information, because a few periods from each side of the L7 line-defect photonic crystal cavity fits onto such protruded region. In that case, it is likely that the optical mode inside the cavity, and correspondingly laser device performance, is not affected much by an uneven sample surface. These protrusions could of course have more critical impact on other types of photonic crystal cavities and waveguides in particular, causing light scattering at the edges. More detailed investigations are needed for better understanding.

Growth dependence on mask orientation. AFM scans of differently oriented buried heterostructure regions after the 1^{st} re-growth also reveal some orientation-dependent features appearing at the edges and corners. To analyse them in more detail, all the scans were performed again on a smaller scale (Fig. 5.11).

The difference in growth kinetics for involved different crystallographic planes originates due to variation in a relative surface dangling bonds density of phosphorus atoms (assuming that the surface is always covered with group V atoms) [166]. In that case, bond density per unit area for (111)A surface (face of element III, Fig. 5.8) will be 3 times larger than for (111)B (face of element V, Fig. 5.8). This would cause group III reactants to migrate from slow-growing planes ((111)B) to fast ones ((111)A). While migration length in general is critically important in this process, it is most certainly larger than at least two of the buried heterostructure mask dimensions (height and width) for the small structures used in this work. Therefore, dips visible at the end of the $[0\bar{1}1]$ direction and sides of the $[011]$-direction oriented structures correspond to nothing else but the slow-growing (111)B planes. Small edge spikes are presumably created by the growth species migrating along the sidewall.

Considering the buried heterostructure mask oriented at a $45°$ angle with respect to the other two structures, asymmetry can be observed at its corners. Interpreting this exact shape would require more definite assumptions about the involved growth mechanisms, however the qualitative principle presented above still remains.

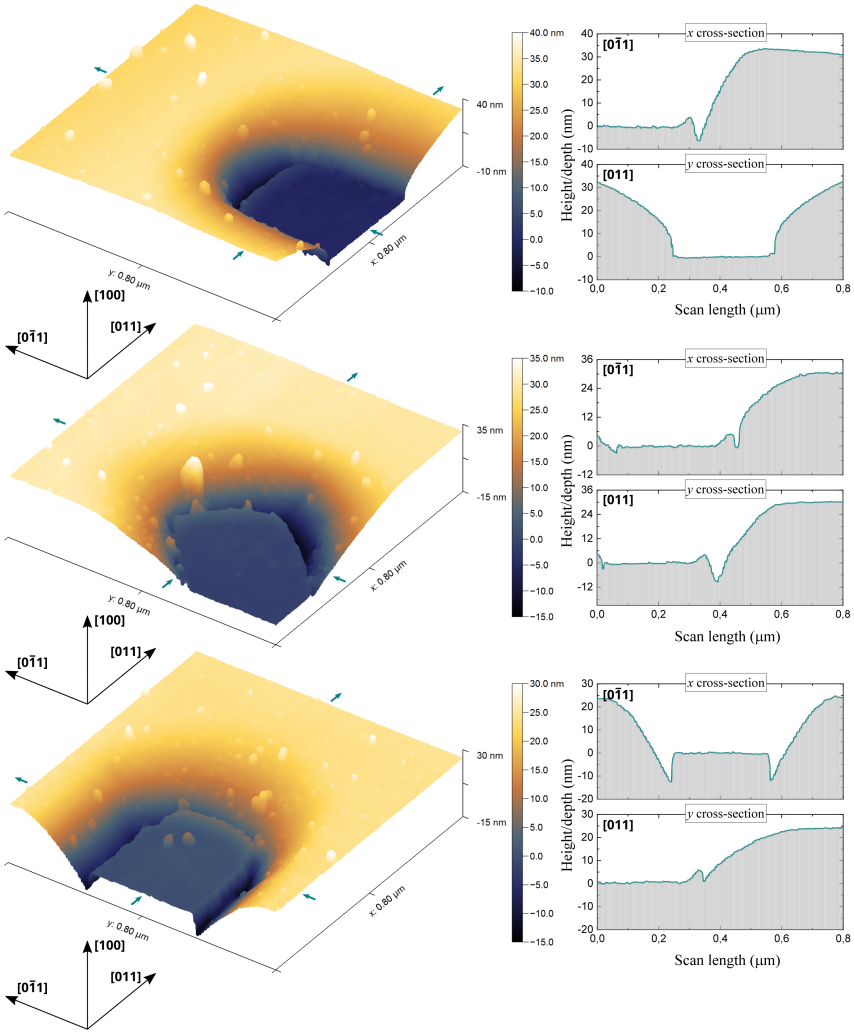


Fig. 5.11.: AFM surface scans (left) and cross-sections (right; positions are indicated by teal coloured arrows on the surface edges) of edges in differently-oriented 350 nm wide buried heterostructure regions after the 1st MOVPE re-growth. The glass-like HSQ masks have been removed.

5.4 Chapter summary and final considerations

This chapter presented the main aspects of material etching and re-growth strategies involved in the buried heterostructure formation. There

are no doubts about the importance of these steps for the overall fabrication outcome success, because they form the structural foundation of the laser device. On the other hand, the small scale of these structures also put considerable requirements on the alignment between the buried heterostructure and the photonic crystal cavity, the issue that was covered in chapter 3. A combination of these buried heterostructure formation and subsequent alignment aspects have the greatest impact on the device performance and constitute the main fabrication challenge. The device performance is the main subject of the following chapter on the experimental laser characterisation.

6 Device Characterisation

The complicated small-scale buried heterostructure fabrication technology described in a few previous chapters required numerous repeated optimization process runs to achieve the initial goal of the first laser demonstration from the simplest line-defect photonic crystal cavity. From that point on, the further development is focused on increasing the performance from the same type of laser cavity, while simultaneously attempting to realize devices with novel photonic crystal cavity designs.

In this chapter, after presenting the optical characterisation setup, the laser demonstration and subsequent process improvement is illustrated by comparing the standard line-defect photonic crystal cavity laser devices fabricated on different samples with quantum wells. Along the analysis of measured characteristics, the performance results are compared to the best-in-class reported relevant lasers. Next, the first ever Fano-type photonic crystal laser with the buried heterostructure is demonstrated.

After the discussion focused on the laser cavity designs realized in devices with InGaAsP/InAlGaAs quantum wells, the efforts in demonstrating lasers with InAs quantum dots as the active material in the buried heterostructure are discussed. The chapter ends with a brief overview of the performance improvement trend throughout the course of this work and in addition a few possible future improvements are mentioned.

6.1 Optical characterisation setup

All the fabricated samples were characterized at room temperature using the optical pumping micro-photoluminescence setup (Fig. 6.1), schematically represented in Figs. 6.2 and 6.3. The pump laser light is focused on the sample via a microscope objective, which also collects the vertically emitted light. The measurement spectrum range is limited at shorter wavelengths by the low-pass filter cut-off at around 1520 nm, and

Fig. 6.1.: Image of the optical characterisation setup with the main components highlighted.

at higher wavelengths by the spectrometer detector at around 1640 nm.

The main pump source in the setup is a 1480 nm continuous-wave (cw) multi-mode laser diode (Fitel FOL1404), except when the pulsed-pumping is needed which is provided by a 980 nm laser. A fixed 300 mW output of the cw laser is connected to an attenuator controlled via a home-made LabView program. After the attenuator, the power is split by a 2×2 fused fibre coupler, with a 1% tap output fed into a power metre for monitoring. The polarization controller is used at the signal output path, and at this point two different variations of the setup exist.

Characterisation setup with a common pump and collection port. The first version of the setup (Fig. 6.2) uses only one port for inputting the pump light and outputting the emitted light from the laser sample. A single-mode optical circulator sends the 1480 nm pump light into the microscope setup through a collimator, which is then directed by a beamsplitter to the sample via a 50x magnification objective with an NA of 0.65. The precise

pump spot is controlled by adjusting the stage on which the sample is placed and monitored by an infrared (IR) camera attached on top of the microscope. The majority of the emitted light from the sample is reflected by a beamsplitter back to the circulator, which directs it to the optical spectrum analyser (Yokogawa AQ6470D).

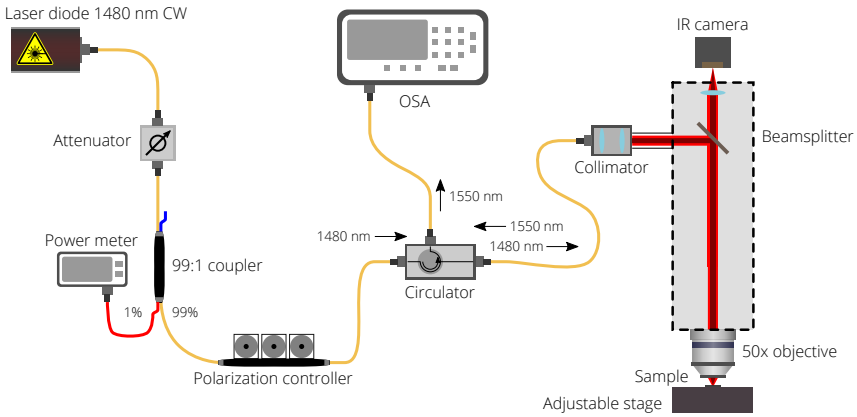


Fig. 6.2.: Characterisation setup with a common pumping-collection port.

The main advantage of this setup is that a single collimator is used, which makes an entire setup more stable and easier to calibrate. However, the pump light is not filtered in the path towards the IR camera, therefore monitoring of much weaker emitted light from the laser sample is not possible.

The total power loss in this setup is around 5 dB: approximately 1 dB is lost in the path towards the collimator, and additional 4 dB from there to the laser sample.

Characterisation setup with separate pump and collection ports. The second version of the setup (Fig. 6.3) has two separate ports: one of them is used for inputting the pump light, the other for directing the light emitted from the laser sample to the spectrum analyser.

Using this setup, the pump laser light in the path towards the IR camera is filtered (although not completely), therefore light emitted from the laser sample can be monitored simultaneously (Fig. 6.4). This is desired for tracking pumping position more accurately for specific samples (e.g.

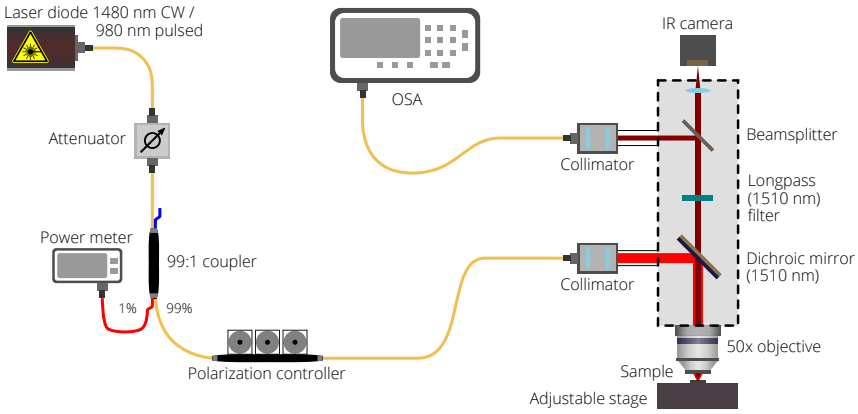


Fig. 6.3.: Characterisation setup with separate pumping-collection ports.

Fano photonic crystal lasers). The disadvantage is a reduced setup stability and the need to collimate both ports separately to guarantee an optimal overlap between the focus positions. While the pump laser spot is used for this purpose while adjusting one collimator, another laser source has to be connected to the collection port during its adjustment. Once the overlap is optimized, the collection port is connected back to the OSA.

The total power loss in the second setup is larger than in the first, and

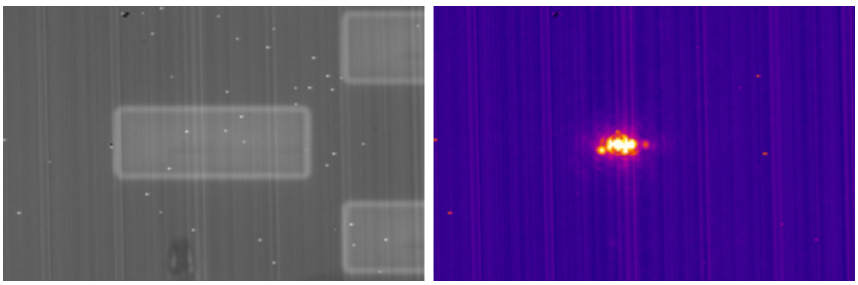


Fig. 6.4.: IR camera image of the photonic crystal laser device structure (left) and the corresponding recorded laser light emission under the optical pumping (right).

is around 8 dB: roughly the same 1 dB is lost combining paths towards the collimator used for the pumping and from the collection port to the OSA, while the loss from the collection port to the laser sample is around 7 dB.

This second characterisation setup is also used for experiments with the pulsed-pumping.

6.2 Laser devices with quantum wells

Photonic crystal lasers with quantum wells as the active material demonstrated the best performance from all the buried heterostructure devices fabricated during the course of this work. Here, a detailed comparison will be made between lasers from two sample processing generations (chapter 4 *Buried heterostructure device processing generations*), "Sample A" from the 2^{nd} and "Sample B" from the 3^{rd}. Both of them were epitaxially grown with 3 InGaAsP/InAlGaAs quantum well layers, which are very similar in composition and quality (appendix C), however with moderately different emission peak wavelengths (Fig. 6.5) due to growth re-calibration. The major difference between the samples is a degree of misalignment, which is estimated for the "Sample A" to be on the order of 250 nm, while only around 50 nm for the "Sample B" (chapter 4 *Buried heterostructure device processing generations*).

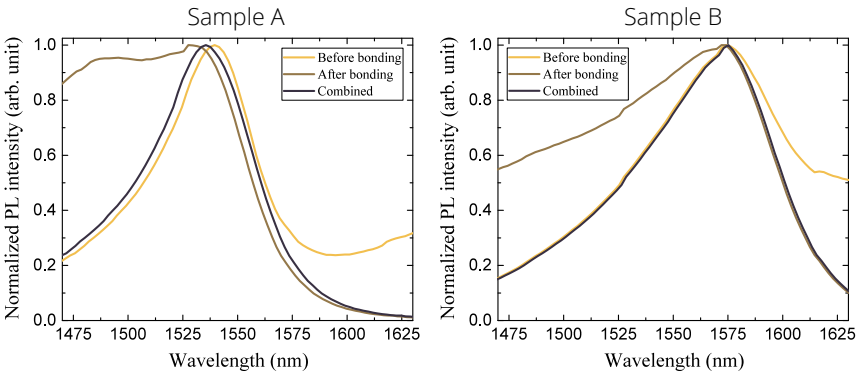


Fig. 6.5.: Photoluminescence emission spectra (normalized to 1) measured from 3 InGaAsP/InAlGaAs quantum well layers epitaxially grown for the device samples from 2 different processing generations ("Sample A" from the 2^{nd} and "Sample B" from the 3^{rd}). The PL spectra were measured with 404 nm laser for the "Sample A", and 570 nm laser for the "Sample B". Measurements on the longer wavelength-side are affected before the bonding by a sacrificial InGaAs layer emission, and from the shorter wavelength-side after the bonding by the membrane effect (Appendix B). Combined spectra are re-constructed from both measurement sets to indicate the expected unaltered emission, assuming there is no processing-induced active material degradation.

Line-defect photonic crystal cavities. Line-defect cavity discussed in chapter 2 section *Photonic crystals as laser cavities* is the simplest type of photonic crystal cavity to fabricate, and is therefore appealing to use in experiments demonstrating novel active materials or structures. Despite this simplicity, it is actually rich in physical phenomena involving complex light-matter interactions, and thus stands out as an attractive platform for theoretical and experimental investigations of technologically important aspects, such as fabrication-induced disorder in the active devices [48, 171, 172]. However, the excess heating and absence of the carrier confinement is a serious problem for the structures containing active material across the entire device layer [60]. For room temperature experiments performed with cw-pumping, quantum dots are required instead of quantum wells or bulk semiconductor [48]. Therefore, the standard line-defect cavity laser is a candidate to benefit at once from the technology allowing quantum wells buried heterostructure to be embedded in the photonic crystal cavity.

The results presented here for the device "Sample A" are actually also from the first lasing buried heterostructure device fabricated during the course of this work. Fig. 6.6 contains the characteristic L9 line-defect photonic crystal cavity laser measurements. Output peak power versus the pump power curves are shown in logarithmic and linear scale in Fig. 6.6 (a) and (b). The lasing onset is clearly visible with the estimated threshold value at the pump power delivered to the sample slightly above 40 mW. Lasing saturation is not completely observed for the used pump power range, which is limited by the maximum output of the pump laser. Nevertheless, at this excitation level some of the photonic crystal samples were not very stable and had a tendency to burn.

A few peaks corresponding to the L9 cavity modes are visible in the spectrum plotted over a wide wavelength range in Fig. 6.6 (c). The threshold characteristics in (a) and (b) represent the fundamental (lowest order) mode at around 1577 nm. This mode has the highest Q-factor for increasing line-defect cavity length [172] and clearly dominates over the other modes. A zoomed-in region of the main peak measured with higher sensitivity and resolution (Fig. 6.6 grey box, right) reveals that there are actually multiple side-peaks positioned around the centre-peak. Such effect has already been observed for multiple other photonic crystal laser devices measured with the experimental setup described in the section *Optical characterisation setup*, and has been identified as the mode-beating

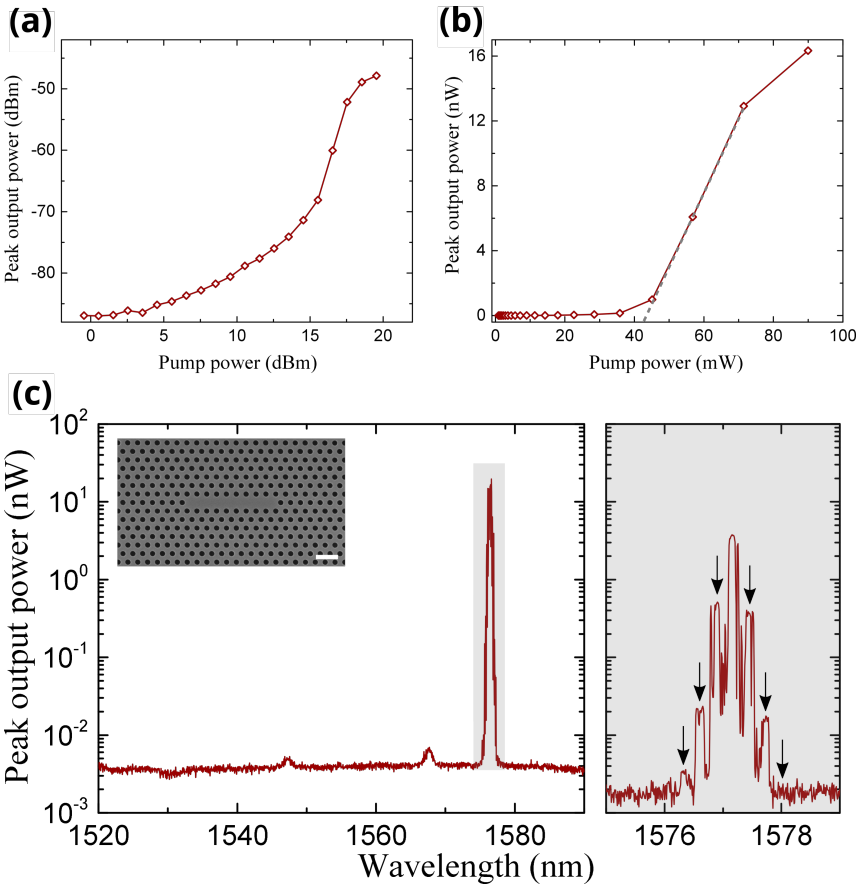


Fig. 6.6.: Measured "Sample A" characteristics of the L9 cavity photonic crystal laser with the buried heterostructure containing 3 layers of quantum wells: (a) logarithmic- and (b) linear-scale light-in light-out curves; (c) wide-range spectrum (0.5 nm resolution) and an enlarged view (0.2 nm resolution) of the main laser peak at around 1577 nm (grey box, right) at an input power delivered to the sample of 90 mW. The arrows are pointing at the side-peaks (their origin is discussed in the text). Inset shows SEM image of the L9 cavity region; the scale bar is 1 μm.

of the multi-mode pump laser transferred to (modulating) the examined device. By measuring a wavelength separation between the centre and the "modulation side-band" peaks in Fig. 6.6 and converting that to frequency via relation $\Delta\nu = c\Delta\lambda/\lambda^2$, the value of 34.0 ± 0.8[1] GHz is determined. This corresponds well to the mode spacing of 33.6 GHz estimated for the multi-mode pump laser, and at least qualitatively explains appearance of the side-peaks in the photonic crystal laser spectrum.

Although emission line-width narrowing is observed at the lasing transition (not shown here), the peak modulation and observed drifting of an entire group of peaks with time (due to sample's thermal variation, mechanical vibrations, etc.) does not allow the laser line-width value to be estimated using the current setup. In any case, it is expected to be way below the available 0.02 nm resolution (~ 2.5 GHz) of a spectrum analyser, somewhere in the range of a couple hundred megahertz [173, 174].

The characteristic "Sample B" laser measurements of the L17 line-defect photonic crystal cavity are provided in the same form in Fig. 6.7 for a convenient comparison. The threshold lies way below 1 mW of the pump power delivered to the sample, which is only evident from the logarithmic light-in light-out representation (Fig. 6.7 (a)), but not the linear representation in the given range (Fig. 6.7 (b)). This gives an immediate feeling of how drastic the improvement is with respect to reduced lasing threshold and increased output peak power. The maximum pump power is still not large enough to observe a complete saturation of the emission from the L17 cavity, with the highest measured value close to 400 nW. In contrast to the "Sample A", a much more stable device operation without signs of overheating was observed.

The spectrum measured over a wide wavelength range is plotted in Fig. 6.7 (c) together with a higher sensitivity and resolution measurement of the main lasing peak (grey box, right). "Modulation side-band" peaks analogous to those observed for the previous sample are still present, and the calculated separation of 33.5 ± 0.4 GHz is again very close to the mode spacing of the multi-mode pump laser.

In this case, the lasing peak was measured with a maximum achievable resolution of a spectrum analyser, however the result is very similar to the one previously presented for the "Sample A". Therefore, the same arguments can be applied here.

[1] The uncertainty is estimated by considering ambiguity in wavelength measurement due to broadened peaks.

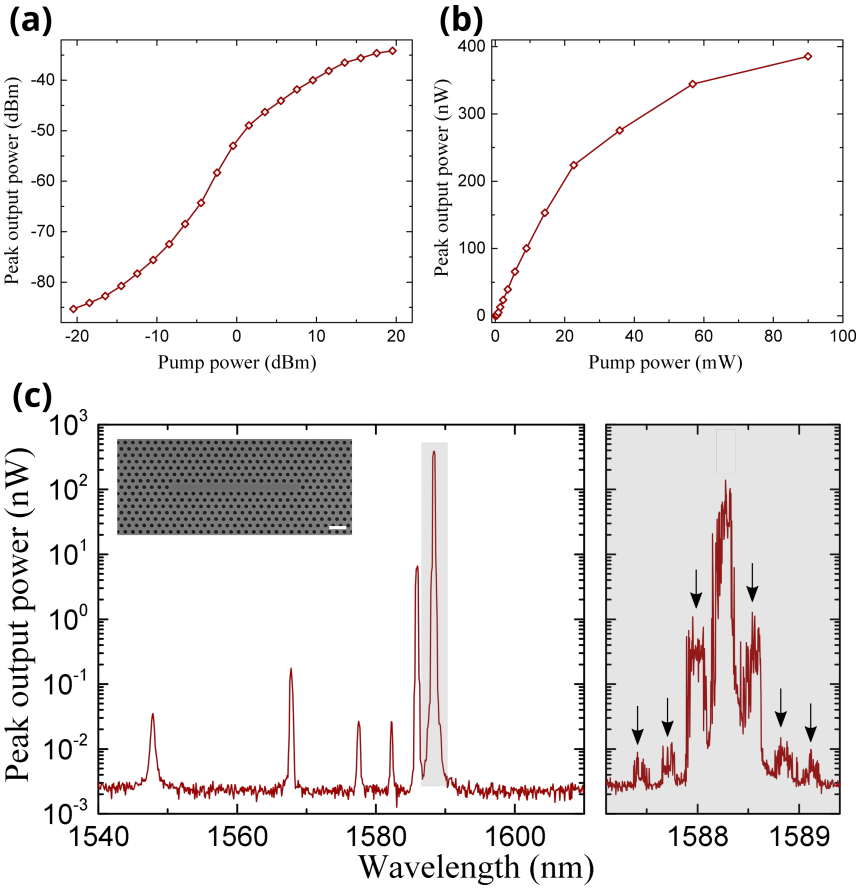


Fig. 6.7.: Measured "Sample B" characteristics of the L17 cavity photonic crystal laser with the buried heterostructure containing 3 layers of quantum wells: (a) logarithmic- and (b) linear-scale light-in light-out curves; (c) wide-range spectrum (0.5 nm resolution) and an enlarged view (0.02 nm resolution) of the main laser peak at around 1588 nm (grey box, right) at an input power delivered to the sample of 90 mW. The arrows are pointing at the side-peaks (their origin is discussed in the text). Inset shows SEM image of the L17 cavity region; the scale bar is 1 μm.

The standard line-defect photonic crystal lasers operate in the slow-light regime, with modes approaching the Brillouin zone edge as the cavity length increases (chapter 2 section *Photonic crystals as laser cavities*). Indeed, mode shifting behaviour towards the zone edge at around 1590 nm is visible in Fig. 6.8 for studied L2−L20 cavities in the "Sample B". The overall picture generally resembles results for the quantum dot photonic crystal lasers reported in [48, 83]. However, instead of observed 5 or 7 cavity modes, a total of 8 modes are found for the L20 line-defect cavity with the quantum wells buried heterostructure. Quantum dots can normally provide gain with little variation over a few times wider range than quantum wells, therefore the opposite situation could be expected. Most likely the additional mode emerges due to a refractive index increase in the cavity from the embedded quantum wells buried heterostructure. The refractive index at $\sim$1550 nm for the InGaAsP wells ($n \approx 3.6$) and InAlGaAs barriers ($n \approx 3.26$) in the buried heterostructure is quite higher than for the InP membrane with embedded InAs quantum dots ($n \approx 3.17$). Describing the line-defect photonic crystal as an effective one-dimensional Fabry-Perot cavity, a free spectral range (FSR) given by $\Delta\lambda = \lambda^2/(2Ln_g)$ (where n_g is the group index and L is the Fabry-Perot cavity length) would decrease as a result of the refractive index increase. Such simple picture provides an intuitive explanation for a higher number of observed cavity modes, however detailed numerical computation is needed for more certainty.

Previously, peak output power dependencies on the pump power for the buried heterostructure photonic crystal lasers were plotted using the pump power delivered to the sample values. These were determined prior to the laser measurements by placing a photodiode sensor under the microscope objective. However, in such optical pumping setup, where the photonic crystal samples are pumped from above through the objective, a large portion of the circular pump beam is outside the small laser cavity region (unless some modified technique is used where a better overlap can be realized by employing a cylindrical lens [68]). In case where the active material extends across an entire sample, this leads to carriers generated outside the cavity region, and the cavity size itself becomes not well-defined. In case where the active material is embedded inside of it, just as with the buried heterostructure considered in this work, the pump light is only absorbed in the small active region, but not by the InP membrane (InP is transparent at 1480 nm, which lies within its elec-

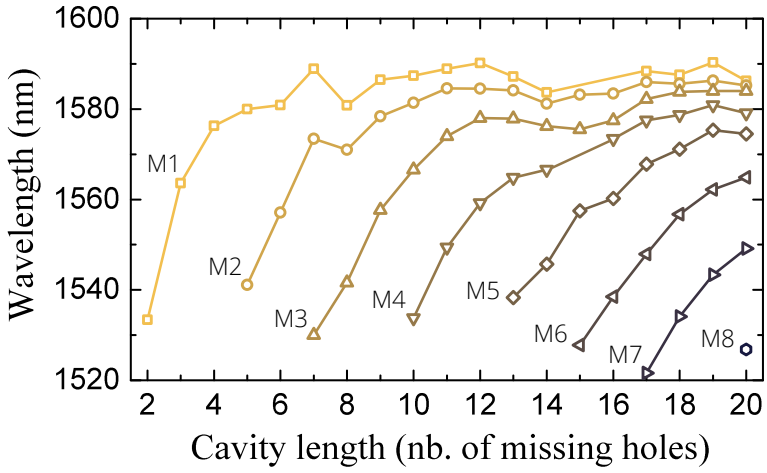


Fig. 6.8.: Modes of the line-defect photonic crystal with the embedded quantum wells buried heterostructure in cavities of different lengths approaching the Brillouin zone edge with increasing wavelength. Measured on the "Sample B".

tronic bandgap). Thus, to the first order the laser threshold power can be estimated more accurately by considering an overlap ratio between the buried heterostructure in-plane area and the total area illuminated by the pump beam spot. Its diameter in the characterisation setup is around 3 μm when well-focused, corresponding to the L7 line-defect cavity length, and is approximately 10 times larger than the buried heterostructure area in the L4 cavity. By estimating this area ratio for the cavities of different lengths and multiplying corresponding numbers with the excitation power, the revised threshold power values were extracted and compared for the "Sample A" and "Sample B" in Fig. 6.9. The threshold of each laser was calculated by using the second derivative method [175].

In the comparison, cavities only up to L10 are included as the partial pumping of the active layer would result in the threshold power increase (due to absorption in the unpumped portion of the active material). Defocusing the beam would decrease the pump power density, therefore the pump laser with a higher output power would be needed to compensate for the decrease.

It can be seen from Fig. 6.9 that the lowest estimated threshold power value for the "Sample A" is around 8 mW from the L9 cavity, whereas three orders of magnitude lower power of just below 10 μW is determined for

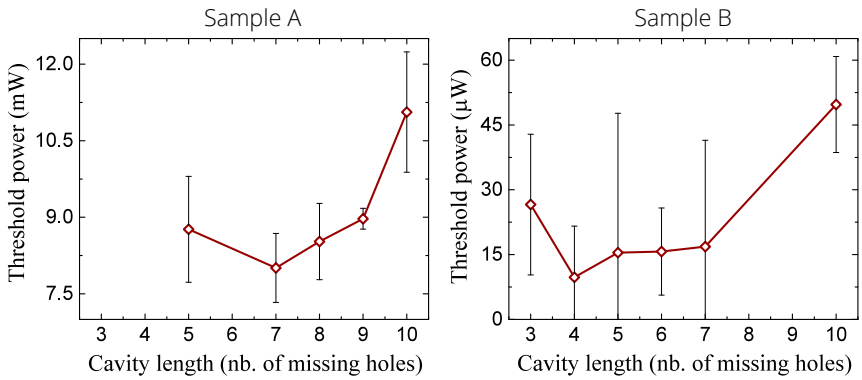


Fig. 6.9.: Threshold power dependence on the photonic crystal line-defect cavity length for the "Sample A" and "Sample B" lasers with 3 layers of quantum wells buried heterostructure. Accuracy of determining the threshold values is limited by a number of measured data points.

the "Sample B" from the L4 cavity. The overall trend of the threshold power dependency on the cavity length looks alike the threshold density curves reported in [48, 171] (threshold density values were obtained by dividing the threshold power by the corresponding cavity length): there is an initial decrease as a consequence of reduced mirror loss in inverse proportion to the slow-down factor S, followed by an increase that could be attributed to the fabrication-induced disorder losses. For the results presented here, more experimental points are needed for longer line-defect cavities (measured with enlarged pump beam spot) to comment more on the nature of the increasing threshold powers (and corresponding threshold power densities).

As a result of comparable quantum well active layers used in both "Sample A" and "Sample B", as well as closely similar conditions during the fabrication process (with an exception of the alignment marks formation as discussed in chapter 4 section *Buried heterostructure device processing generations*), the huge difference between the laser threshold powers and the maximum output powers can be attributed solely to the contrast in the alignment between the buried heterostructure regions and the photonic crystal cavities. Due to the misalignment in the "Sample A", almost half of the active region lies outside the cavity, resulting in the photonic crystal holes etched only from the top side (due to Al-containing quantum wells resistant to the dry etching chemistry used during the processing, as discussed in detail in chapter 5 section *Buried heterostructure fabrication by*

etching). It is actually very surprising to see any lasing from this sample, and the poor device performance is easily explained. Nevertheless, it seems that improvements in the thermal conductivity and carrier confinement are enough to realize room-temperature cw lasing not achieved before in the InGaAsP-based material configuration without the buried heterostructure [60]. "Sample B", on the other hand, should be compared to the best performing optically-pumped photonic crystal laser devices. It is evident by direct comparison that 3 InGaAsP/InAlGaAs quantum well layers buried heterostructure line-defect photonic crystal laser performs better than an equivalent device with 3 InAs quantum dot layers in the non-buried heterostructure configuration [48] (at least with respect to the parameters in consideration). Comparing to the double-heterostructure photonic crystal cavity laser with a single quantum well layer with the estimated threshold absorbed power of 1.5 μW [39] and related record-performance devices reviewed in chapter 1 section *Small-footprint lasers for on-chip communications*, it is a very positive overall result with a perspective to improve further. Although very different laser pumping setup configurations were used which make a fair comparison rather complicated, the power threshold values presented in this work are most likely underestimated rather than overestimated. For instance, a limited absorption by the quantum wells is not included. Single-pass absorption should be around a few percent for 3 quantum well layers [176], however this number may be increased to above 10% due to the membrane device structure (multiple reflections from the layers underneath).

Consistent progress in the buried heterostructure device fabrication technology with respect to the alignment accuracy has led to a qualitatively measurable improvement in the photonic crystal laser performance. Even tighter process control below 50 nm becomes complicated as many factors affect the wafer distortion at this level, as has been pointed out in chapter 3 section *E-beam metrology of bonded samples*. Nevertheless, many new exciting experimental demonstrations are expected with this device platform in the near future.

Fano-type photonic crystal cavities. Laser cavities based on narrowband mirrors realized by the Fano interference phenomenon display intriguing features as discussed in chapter 2 section *Photonic crystals as laser cavities*.

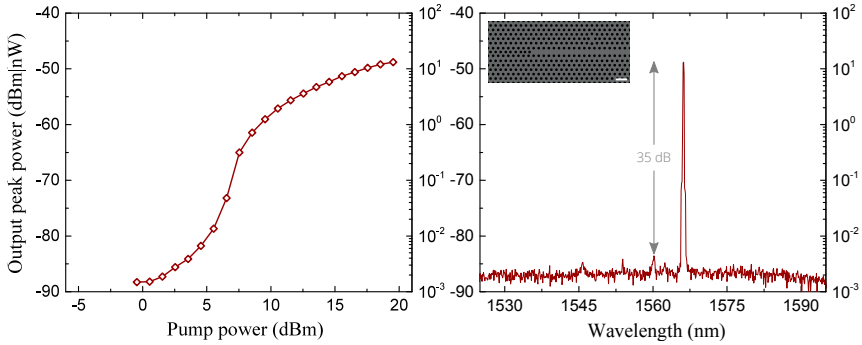


Fig. 6.10.: Measured characteristics of the single-mode photonic crystal Fano laser with the buried heterostructure: (left) the output power dependence on the pump power delivered to the sample; (right) the wide-range spectrum indicating the SMSR of 35 dB. Inset shows an illustration of the Fano design with the laser cavity length of L12, and the H0 side-coupled nano-cavity; the scale bar is 1 μm.

Until now, experimental laser demonstration was only realized in structures where the quantum dots extend across the entire device layer [83]. In this section, the first ever photonic crystal Fano laser with the buried heterostructure inside the laser cavity is demonstrated for the "Sample B".

Experimentally determined characteristics for the Fano laser with the L12 laser cavity and the side-coupled H0 nano-cavity are shown in Fig. 6.10. The light-in light-out curve (Fig. 6.10, left) exhibits a clear kink indicating the onset of lasing. The measured spectrum (Fig. 6.10, right) indicates a single-mode behaviour, as expected from the earlier quantum dots non-buried heterostructure Fano laser measurements [83]. No spectrum broadening was observed indicating cw-lasing, confirming the previously explained self-pulsing mechanism for the lasing observed in the non-buried heterostructure sample (chapter 2 section *Photonic crystals as laser cavities*).

Photonic crystal buried heterostructure Fano laser characteristics for the L9 cavity laser with the L7 side-coupled cavity are shown in Fig. 6.11. Again, the light-in light-out curve (Fig. 6.11, left) clearly indicates the lasing transition, however the spectrum (Fig. 6.11, right) resembles a multi-mode laser behaviour due to the presence of multiple supported lasing or amplified spontaneous emission (ASE) peaks. Interestingly, the indicated side-mode suppression ratio (SMSR) value is large and more

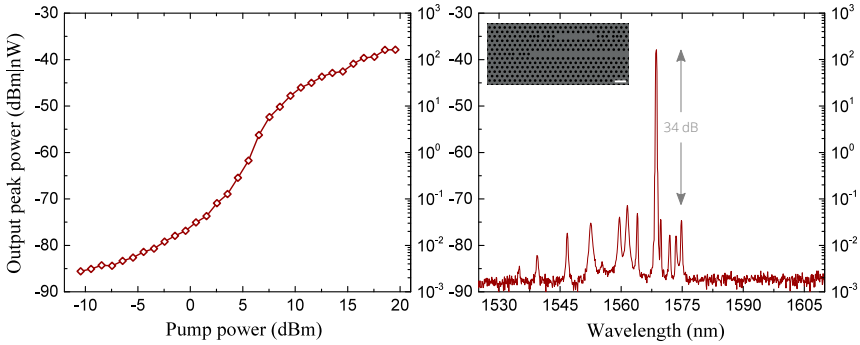


Fig. 6.11.: Measured characteristics of the multi-mode photonic crystal Fano laser with the buried heterostructure: (left) the output power of the dominant mode dependence on the pump power delivered to the sample; (right) the wide-range spectrum indicating the SMSR of 34 dB. Inset shows an illustration of the Fano design with the laser cavity length of L9, and the L7 side-coupled cavity; the scale bar is 1 μm.

typical for the single-mode laser. While characterizing a lot of different L7 side-coupled cavity Fano laser samples with varying laser cavity lengths, a rather non-systematic trend of the dominating peak wavelengths and the SMSR values was observed.

The most interesting feature of the multi-mode Fano laser is shown in Fig. 6.12. Despite a very large number of modes supported by the Fano laser design, practically all of them have wavelengths independent of the laser cavity length. This general property of the Fano laser was demonstrated previously for the single-mode laser, where a narrowband mirror formed by the H0-type side-coupled nanocavity set the lasing condition [83]. It is remarkable to see how the same features are preserved in the multi-mode laser as the lasing conditions can be fulfilled for many modes of the L7 side-coupled cavity. The problem of separating these modes then arises, as many of the closely-spaced "real" cavity modes can be mixed up with the "modulation side-band" peaks discussed previously.

Finally, the buried heterostructure configuration in the Fano laser could also enable to access the self-pulsing regime by selectively embedding the active material inside the side-coupled cavity in addition to the laser cavity. This provides a lot of experimental freedom for the future Fano laser demonstrations.

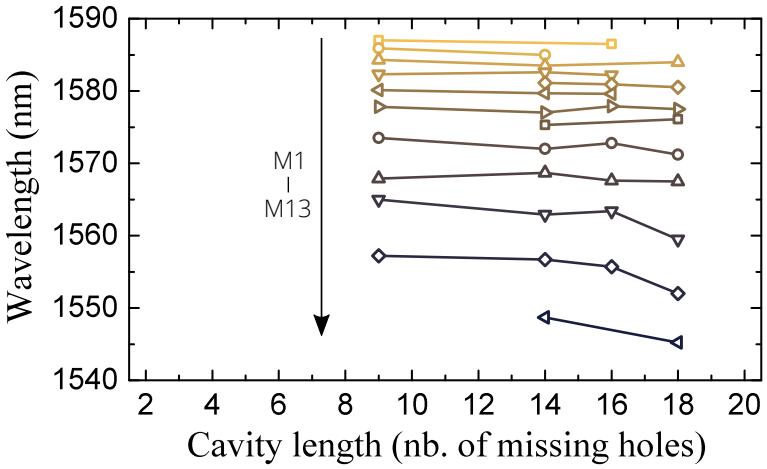


Fig. 6.12.: Modes of the multi-mode photonic crystal Fano laser with the embedded quantum wells buried heterostructure in cavities of different lengths with the L7 side-coupled cavity. Markedly different behaviour from the line-defect cavity lasers is observed, with almost no dependency of the wavelengths of modes on the laser cavity length.

6.3 Laser devices with quantum dots

In this section, some selected attempts to realize working photonic crystal laser devices with quantum dots as the buried heterostructure active material will be presented. No lasing was observed from these structures, and a few possible explanations for that will be given.

Optimized line-defect photonic crystal cavities. Along the development of quantum wells laser devices, identical if not larger focus was devoted to developing the buried heterostructure photonic crystal lasers with quantum dots. A common result was the same: observation of the amplified spontaneous emission peaks with increasing output power in relation to the increased pumping, however no lasing threshold crossing.

The most promising result in relation to the expected high alignment accuracy is shown in Fig. 6.13 (the corresponding PL spectra of the sample are given in Fig. 6.15). Here, an optimized[2] L7 line-defect photonic crystal cavity (Q-factor increased through the selective shifting of the nearest holes at both ends of the cavity [65]) was used. In any case, no lasing was

[2]Optimization performed by Yi Yu.

observed neither under the cw-pumping with 1480 nm laser, nor 980 nm pulsed-pumping. In the second case, a clear roll-off of the output power is visible, indicating excess sample heating.

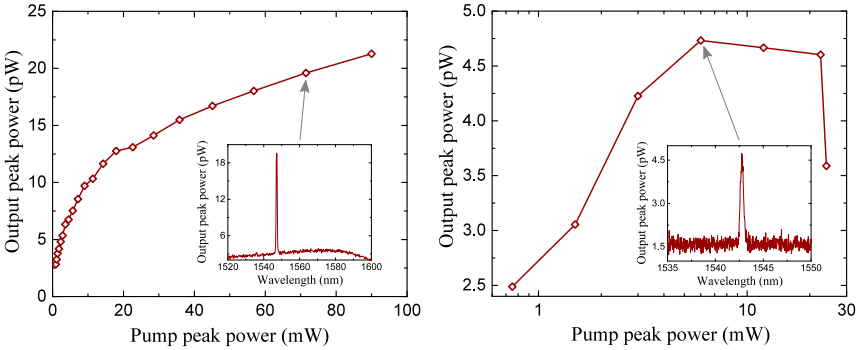


Fig. 6.13.: Measured characteristics of the non-lasing buried heterostructure photonic crystal laser where the active material consists of 3 layers of self-assembled InAs quantum dots and the photonic crystal cavity is an optimized L7 line-defect cavity. The light-in light-out measurements were performed under the cw- (left) and pulsed- (right) pumping. Insets show spectra where the amplified spontaneous emission peaks are visible for indicated data points.

Buried heterostructure vs. non-buried heterostructure test. Earlier fabricated photonic crystal laser devices with 3 self-assembled InAs quantum dot layers extending across an entire sample were used in numerous reported experiments discussed earlier. With the active material region reduced to the photonic crystal cavity dimensions, a number of quantum dots becomes very small. Considering the surface density of dots used in this work ($\sim 5 \cdot 10^{10}$ cm^{-2}, appendix C) and 3 µm $\times$ 350 nm dimensions of the buried heterostructure in the L7 line-defect cavity, only around 500 dots are left. Because of large inhomogeneous distribution, only a part of those quantum dots contribute at the designed lasing wavelength. Finally, a small optical confinement factor for the quantum dots (chapter 2 section *Material considerations*) means that the resulting modal gain is also small. These considerations put the buried heterostructure photonic crystal laser at a disadvantage compared to the non-buried heterostructure one, which might not be enough to compensate with the benefits brought about by the buried heterostructure.

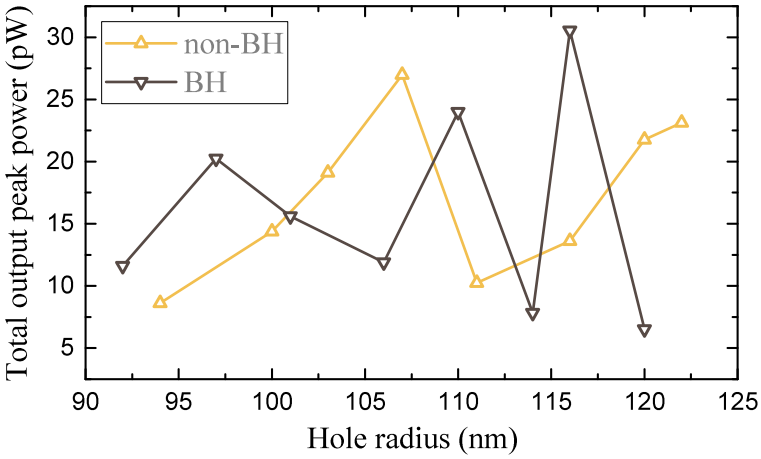


Fig. 6.14.: Total amplified spontaneous emission output peak power summed over all detected L7 cavity modes for the quantum dots buried heterostructure and non-buried heterostructure photonic crystals with a variable hole radius.

In order to obtain a better understanding of why the buried heterostructure devices with quantum dots do not work, enlarged active material regions were left on the wafer for test purposes. On those structures, some compact L7 line-defect photonic crystal cavities were placed during the fabrication to realize conditions resembling the non-buried heterostructure quantum dot devices. Their measurements together with the standard L7 photonic crystal cavity structures with the buried heterostructure on the same sample were performed and the comparison is given in Fig. 6.14. Possibly due to alterations introduced to the compact photonic crystals, different cavity modes were observed. In order to make a comparison more meaningful, an output peak power was summed over all of the detected peaks for structures with varying photonic crystal hole radius.

Unfortunately, as can be seen from Fig. 6.14, the experimental results are inconclusive. Neither of the measured device was lasing, and the total output peak powers show no systematic change. The idea of this experiment is, nevertheless, promising, if better preparation is made and much larger active material regions are preserved on the sample from the very beginning, so that the full-sized photonic crystal cavities can be placed to realize non-buried heterostructure device conditions.

Other related experiments with quantum dot samples. A couple of other experiments in testing quantum dots samples used for the buried heterostructure device fabrication are listed here.

The PL measurement example of the fabricated quantum dots sample before and after the direct bonding to the Si substrate is given in Fig. 6.15 (left). A largely reduced emission from the bonded sample is observed. This could be explained by the "membrane effect" (appendix B) that is interfering with the PL measurements. On the other hand, as the "membrane effect" calculations did not prove to be universal in every case, a possibility of some kind of fabrication process-induced damage (e.g., during the dry etching) to the sample with the quantum dots remains.

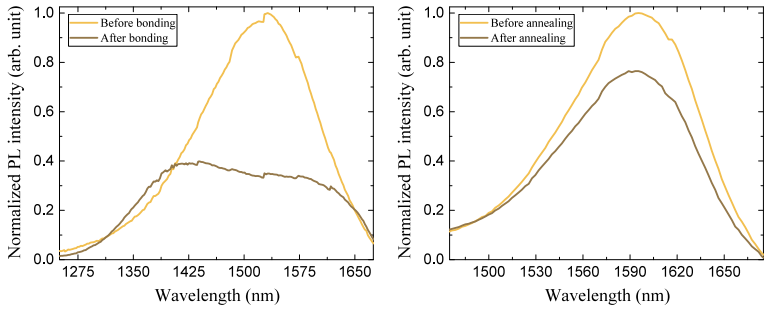


Fig. 6.15.: Photoluminescence emission spectra measured from the epitaxially grown samples with 3 InAs self-assembled quantum dot layers: (left) spectra indicating suppressed emission after the direct InP wafer bonding to the Si substrate with 1.3 μm thermal SiO_2 layer, possibly due to the "membrane effect" (appendix B); (right) spectra indicating reduced emission intensity after 1 hour sample annealing at 300 °C temperature for the directly bonded test sample. All the spectra were measured with 570 nm laser. Spectra measured before any processing are normalized to 1, after the processing normalized with respect to the first to retain the representative change.

A special experiment was made to test the sample annealing influence on the directly bonded sample with the quantum dots. The bonded sample was kept at 300 °C temperature for 1 hour, and the PL spectra before and after were compared. The PL intensity reduction of around 25% was observed, indicating some possible process-induced sample degradation related to defects [114]. During the device fabrication, the sample is annealed twice at even higher 650 °C temperatures (but shorter times) in

the MOVPE during the re-growth (chapter 5), which might have even more negative impact. Further investigations are thus needed.

6.4 Laser performance improvement trend

Finally, it is interesting to compare the evolution of the buried heterostructure laser devices developed during the course of this work. Fig. 6.16 is a representation of the maximum recorded output peak powers from the quantum well and quantum dot photonic crystal lasers from different processing generations (chapter 4 *Buried heterostructure device processing generations*). It is self-evident that technological bonding approach change, marking the transition from the 1^{st} to the 2^{nd} generation (i.e. from the BCB to the direct bonding), was a crucial component in demonstrating lasing. The step to the 3^{rd} generation is marked by further performance improvement.

However, this "book story"-like trend is only valid for devices with the quantum wells as the active material in the buried heterostructure. Only a minor general improvement in the maximum recorded amplified spontaneous emission output peak powers is visible for the quantum dot devices, despite identical progression through the processing generations. Implication is that the alignment accuracy improvement for the buried heterostructure positioning with respect to the photonic crystal cavity is of lesser importance for devices with the quantum dots than for the quantum wells. This is most likely true only for as long as other issues discussed in the previous section are addressed.

6.5 Chapter summary and final considerations

Demonstration of lasing from various photonic crystal structures with the buried heterostructure was presented and discussed in this chapter.

By comparing lasers with the quantum wells active material, an obvious device performance improvement as a result of better alignment between the photonic crystal cavity and the buried heterostructure was observed. The maximum recorded output power from the line-defect cavity laser was nearly 400 nW, with the estimated lowest threshold power below 10 μW. These values compare favourably even to the best reported

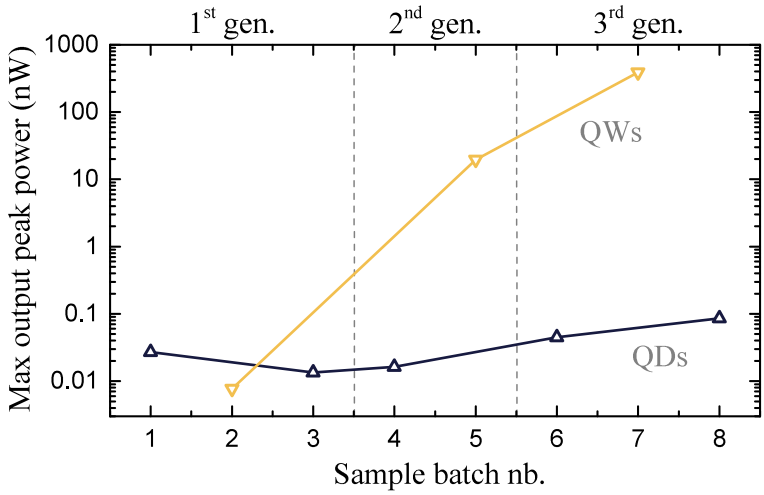


Fig. 6.16.: Comparison of the maximum recorded output peak powers for the buried heterostructure photonic crystal laser devices from different fabrication batches from 3 processing generations.

optically-pumped photonic crystal lasers.

In addition to that, multi-mode photonic crystal Fano lasers with the buried heterostructure in the laser cavity were demonstrated in this work for the first time. Characterisation of the multi-mode Fano lasers appears to be difficult due to a large number of modes involved, while the general properties of the Fano laser remain. The benefit of being able to freely decide where the buried heterostructure should be incorporated in the Fano design is very attractive for future experiments. A lot more detailed systematic study is needed to fully grasp the potential of these laser devices.

Following these successful demonstrations, attempts in realizing the laser with quantum dots as the active material in the buried heterostructure were discussed. Unfortunately, no lasing was observed and no decisive conclusions about the reasons for that can be given. In general, quantum dots appear to be more sensitive to the buried heterostructure fabrication than the quantum wells. More gain by, e.g. incorporation of higher number of quantum dot layers, and reduced losses by, e.g. a better quality etching of the photonic crystal holes, are needed to break this demonstration barrier.

7

Specimen Preparation for Atom Probe Tomography

Until now, the study of quantum dots presented in this thesis focused mostly from the device characterisation perspective. To unlock their full potential, extensive material investigation is needed as well. This is, however, a complicated task given their small scale (on the order of ten nanometres), which is challenging even for the most advanced scientific instruments. In addition, quantum dots properties are highly dependent on their size, shape and surroundings.

The "standard" microscopy techniques, such as transmission electron microscopy (TEM) and atomic force microscopy (AFM), have enough spatial resolution for studying individual quantum dot features. Nevertheless, sample preparation for the TEM is cumbersome, the imaging is depth-limited, and although tomographic 3D reconstruction of the analysed structures is possible, chemical composition of III-V materials is difficult to reliably determine [177]. The drawback of using the AFM is that quantum dots must be uncapped (i.e. their top cladding layer must be removed or not grown initially), which is known to alter their size and shape [97]. The more "exotic" microscopy techniques, such as the cross-sectional scanning tunneling microscopy (XSTM) and the atom probe tomography (APT), are emerging and can readily complement the study of quantum dots due to their unprecedented resolution [178–181].

This chapter deviates from the photonic crystal laser processing and characterisation described in the rest of this work. Here, the process optimization of fabricating a sample structure suitable for the APT characterisation is presented. This process is more scalable, less damaging and convenient than today's standard preparation methods. Incorporated into this sample structure, quantum dots could be investigated in great detail, helping to develop them further and leading to a subsequently higher fabricated quantum dots device performance.

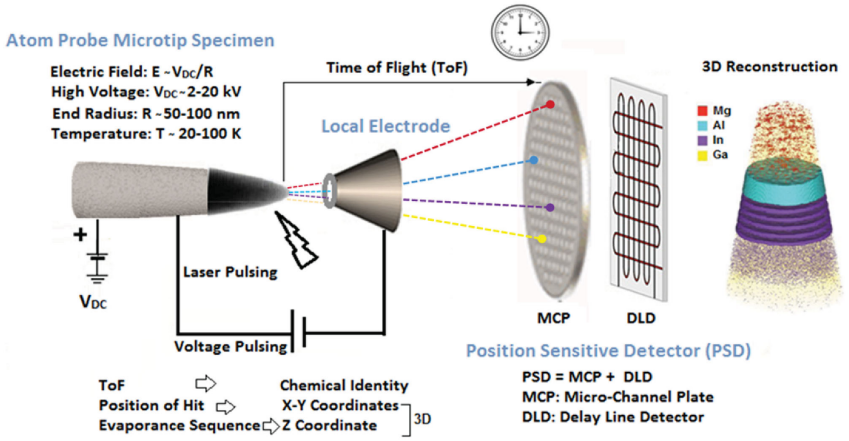


Fig. 7.1.: Schematic diagram of the atom probe tomography instrument illustrating its main working principles. Reprinted from [183].

7.1 Atom probe tomography technique

This section briefly overviews the main principles on which the APT technique is based and the sample requirements for the characterisation.

Working principle. Conceptually, the APT technique [182, 183] combines field ion emission (evaporation) microscopy and mass spectrometry (Fig. 7.1). A high positive voltage is applied to a needle-shaped specimen with a tip-radius on the order of hundred nanometres, cooled to cryogenic temperatures in an ultra-high vacuum. Due to the resulting field enhancement in the vicinity of the tip, very high field strengths (tens of V/nm) ionize the atoms which are pulled from the specimen and directed towards the detector. There, by means of the ion position detection and the time-of-flight (ToF) measurement, a complete 3D model reconstruction of the evaporated sample is possible.

In order to make sure that the detection system is able to correctly identify each atom (ion), the standing voltage on the specimen is chosen to be slightly below the field-evaporation value. A high voltage (voltage-pulsed mode) or a short laser pulse (laser-pulsed mode) that generates a sufficiently high field for an ionization event is then applied to the sample. The pulse parameters are generally chosen so that usually less than 0.1 atom is field-evaporated per pulse.

The mass-to-charge-state ratio $\left(\frac{m}{n}\right)$ is the fundamentally important concept for identification of the detected elements. By assuming that potential energy of a surface atom, neV (where n specifies a number of removed electrons from the atom during the field evaporation, e is the electron charge, and V is the sum of the total voltage applied to the specimen), is completely converted into kinetic energy $\frac{1}{2}mv^2$ (where m is the mass of the atom[1], v is the speed of the atom (ion), expressed as the distance from the specimen to the detector over the ToF) after the ion has left the specimen, the $\frac{m}{n}$ ratio can be calculated. These ratios are generally known and tabulated for the atom probe instruments [184]. Generally, charge states may overlap complicating spectral deconvolution.

Modern APT instruments are able to achieve atomic resolution surpassing any other microscopy method. It is able to provide ~ 0.2 nm resolution in the $x - y$ plane, which is limited by atom's (ion's) trajectory aberrations due to interactions with neighbouring atoms just before the field-evaporation event. The depth resolution is ~ 0.1 nm. Combined with a high analytical sensitivity, the APT can provide compositional 3D images ideally suitable for analyzing buried features at the nanoscale. The main drawbacks and limitations of this technique are [182]: difficult and time consuming specimen preparation; high mechanical stress on the specimen, approaching the cohesive strength of the material it is made of; detection efficiency limited to around 60%; long data collection process with a limited analysis volume; possibility of artefacts during specimen model reconstruction [185].

Sample requirements and standard preparation methods. Early APT investigations were solely focused on metallic samples. The main reason was a high specimen conductivity needed for the pulsed-voltage operation. Adaptation of the pulsed-laser excitation method in the APT enabled the analysis of semiconductor or even dielectric samples.

The essential geometry of an APT specimen is a needle-shaped structure with a sharp tip ($50 - 150$ nm apex radius). A few conventional sample preparation methods exist [182, 183], however, probably the most widespread in use today is the focused ion beam (FIB). During specimen preparation, a post or blank of the material is extracted from the region of interest of the sample, which is then formed by etching (milling) with

[1] To the close proximity, the field-evaporated ion as well.

high-energy ions [186, 187]. Two biggest disadvantages of this method are a long and tedious single specimen preparation process and the damage caused to it by the ion beam.

7.2 Fabrication of pillar-shaped structures with quantum dots

The sample preparation method proposed here is targeting one of the main limitations of the wider APT applicability, that is, time consuming and manual single specimen preparation, as multiple specimens are typically needed for a successful measurement. The idea is to start with a wafer having a layer of quantum dots just below the surface, pattern it with an array of circular HSQ mask elements in e-beam, and then proceed with a deep dry material etching in ICP. The resulting pillar-shaped structures would have very high aspect-ratio with quantum dots located near the top of small diameter apices. With such method, a numerous pillar-shaped specimens could be produced simultaneously in a parallel manner, avoiding damage to the quantum dots during preparation.

In this section, a systematic approach to choosing and tuning the appropriate etching process parameters for producing high aspect-ratio pillar-shaped structures is presented.

Optimized pillar-shaped structures etching. The dry etching recipe optimization for the pillar-shaped structures was greatly influenced (and vice versa) by the development of the InP material etching for the buried heterostructure photonic crystal laser fabrication (chapter 5 section *Optimization of HBr-based InP materials etching*). However, as the process requirements are rather different for both applications, the determined optimal etching conditions are also quite different.

The optimized pillar-shaped specimen dry etching conditions in the ICP are the following:

- The chemistry is HBr/CH_4/Ar with flows of $10/15/2$ sccm, coil and platen powers set to 600 and 50W, respectively, and the chamber pressure set to 5 mTorr.

- ☐ The sample is heated and kept at 180 °C throughout the material etching.

- ☐ Prior to the sample etching, the chamber is thoroughly cleaned by running 30 min long cleaning recipe based on the O_2 plasma, and afterwards the chamber is pre-conditioned by running the HBr etching recipe for 15 min with the same Si carrier wafer on which the sample etching will take place. This is a very different requirement than for the buried heterostructure sample etching. The reason is that some sort of passivating layer is formed on the Si carrier wafer during the pre-conditioning, which afterwards assists the vertical pillar-shaped structure etching.

- ☐ Prior to the HBr etching, the sample surface is gently treated with the O_2 plasma in a barrel-type etching system to remove any possible organic contamination. The sample is not crystalbonded to the Si carrier wafer, as it was found that it had an adverse effect for forming the vertical structures.

- ☐ After unloading from the chamber, the sample is immediately dipped into de-ionized water to remove any remaining Br species from the surface that would otherwise react with air, form HBr and continue sample etching. Given a smaller scale, this step is likely more important than it is during the buried heterostructure fabrication.

- ☐ In order to remove the passivating layer formed around the pillar-shaped structures, the sample is placed for 10 min in the barrel-type etching system, with the CF_4 added to the O_2 plasma (1:7 ratio).

- ☐ Finally, the sample is dipped in the BHF for around a minute. This removes the rest of the HSQ mask left after the dry etching process.

Optimization of pillar-shaped structures etching. To provide a better understanding of the mechanisms involved in the pillar-shaped structures etching, a number of different process parameters were tested.

The influence of adding N_2 or H_2 gas to the etching recipe is shown in Fig. 7.2. The standard buried heterostructure etching recipe was used

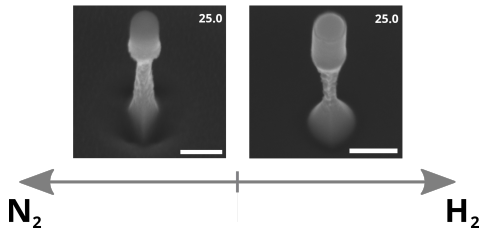


Fig. 7.2.: SEM images of the pillar-shaped structures of 150 nm diameter etched for 2 min with the HBr-based recipe. All the process parameters were fixed, with only 5 sccm of N_2 or H_2 gas added. Scale bars correspond to 200 nm. The numbers given in both images represent an angle by which the SEM sample stage was tilted (approximately out-of-the-page direction). Neither passivating layer, nor the HSQ mask (visible as a cylindrical top part) was removed from the pillars.

(HBr/CH_4/Ar flows fixed at 10/5/2 sccm), with an additional 5 sccm flow of one of the above mentioned gases. Visible in the SEM images is increased mask undercut with the addition of N_2, while in case of the added H_2 the etching profile is narrowing downwards. Addition of O_2 gas was not possible due to the internal machine safety lock.

Next, the influence of CH_4 gas addition was investigated. All the other process parameters and the gas flows were fixed (HBr/Ar 10/2 sccm), no additional gases were used. Fig. 7.3 shows how the sidewall passivation is gradually increased with increasing the CH_4 flow. When little CH_4 is added, the pillar-shaped structures are etched with rapidly decreasing radius towards the bottom. When the flow is 20 sccm, sample surface overpassivation occurs with no (or little) etching. Thus, the flow of 15 sccm was determined to be optimal for forming the high aspect-ratio structures.

Identification and removal of the passivating layer formed on the pillar-shaped structures during the dry etching process proved to be difficult. TEM images[2] in Fig. 7.4 reveal the specimen structure hidden by the passivating layer. Although its exact composition was not determined, increased level of carbon, silicon and oxygen traces indicate the origin related to CH_4 gas (the passivating layer gets thicker with more added CH_4) as well as the Si carrier used [151]. It was found that the layer removal is possible in the O_2 plasma with added CF_4 (used for SiO_2 etching).

[2]Characterisation performed by S. Kadkhodazadeh.

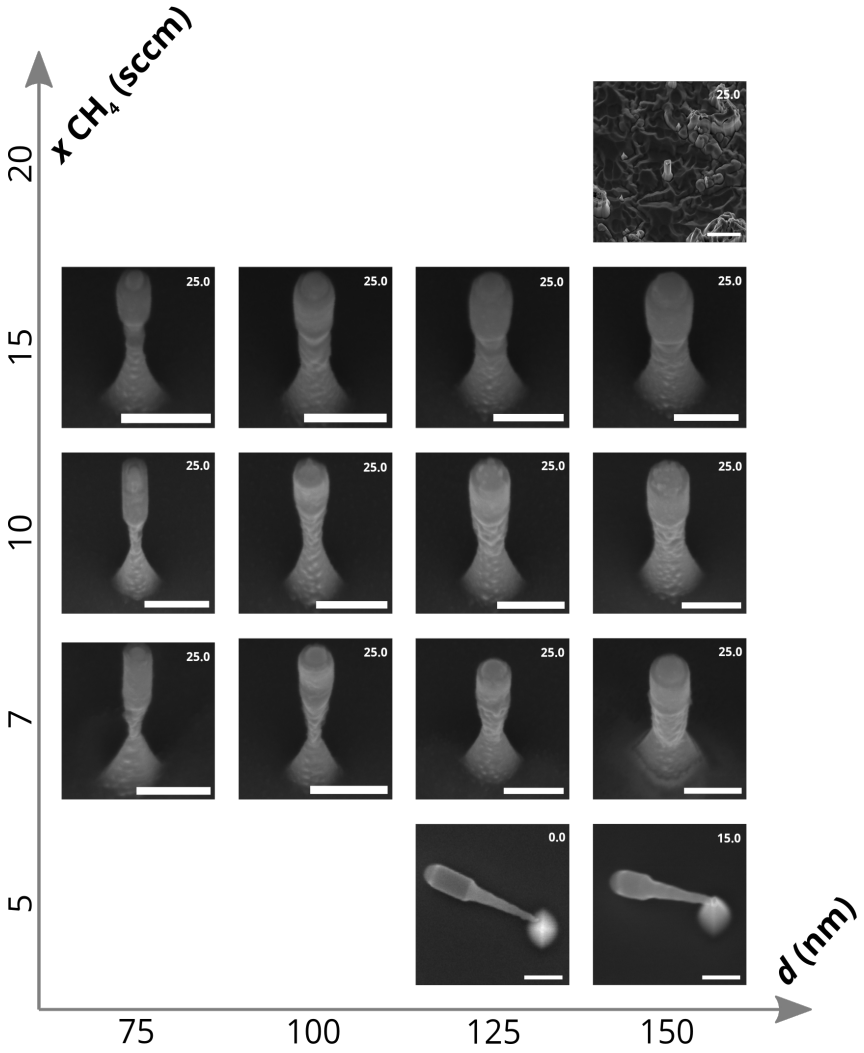


Fig. 7.3.: SEM images of the pillar-shaped structures of different diameters d etched for $2 - 2.5$ min with the HBr-based recipe. All the process parameters were fixed, while only CH_4 gas flow x was varied. All the scale bars correspond to 200 nm, except for the top image in which it is 2 µm. The number given in each image represents an angle by which the SEM sample stage was tilted (approximately out-of-the-page direction). Neither passivating layer, nor the HSQ mask (visible as a cylindrical top part) was removed from the pillars.

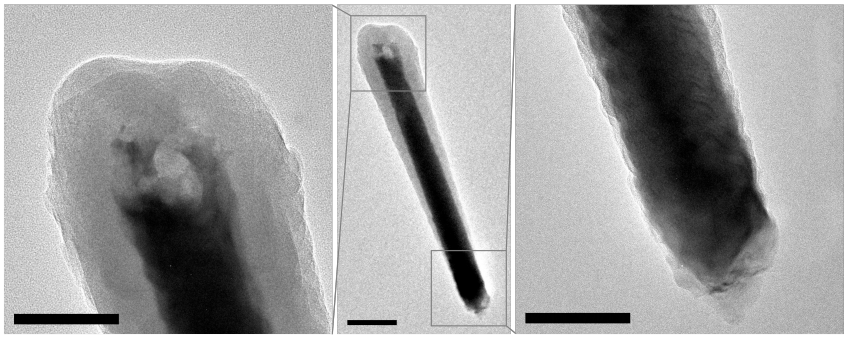


Fig. 7.4.: TEM images of a top part of the pillar-shaped structure harvested after the dry etching. The scale bar for the full structure (middle) is 200 nm, for the close-ups (left,right) it is 100 nm.

Various etch durations were tested to find the maximum obtainable pillar-shaped structure height. Fig. 7.5 summarizes these tests. Remarkably, it was found that different etching time combinations can result in various structural shapes. While the original intention was to use a single long duration etching (Fig. 7.5, bottom row), using intercepts in between etch runs allow to increase the pillar-shaped structures height due to a step-like etching (most likely due to sample cooling down during the intercept). The limitation is then set not by the narrowing of the structure during the etch, but by the etching selectivity towards the mask. The limited thickness HSQ mask can only survive a limited duration etching.

Optimization of the etching recipe for the pillar-shaped structures resulted in a very interesting study of an interplay between the passivation and etching mechanisms. With the conditions described here and by intercepting the etching process, fabrication of a number of pillar-shaped structures with heights exceeding 5 μm and with the tip diameters below 100 nm is possible. These numbers seem suitable for the specimen characterisation with the APT technique.

Optimization of pedestal structures etching. While a very promising dry etching recipe for the pillar-shaped structures was demonstrated, the first quantum dots specimen characterisation attempt failed due to inability to position them accurately enough with respect to the APT electrode. Despite suitable dimensions, visibility of the structures on a planar sample surface with the positioning camera inside the APT chamber is generally poor.

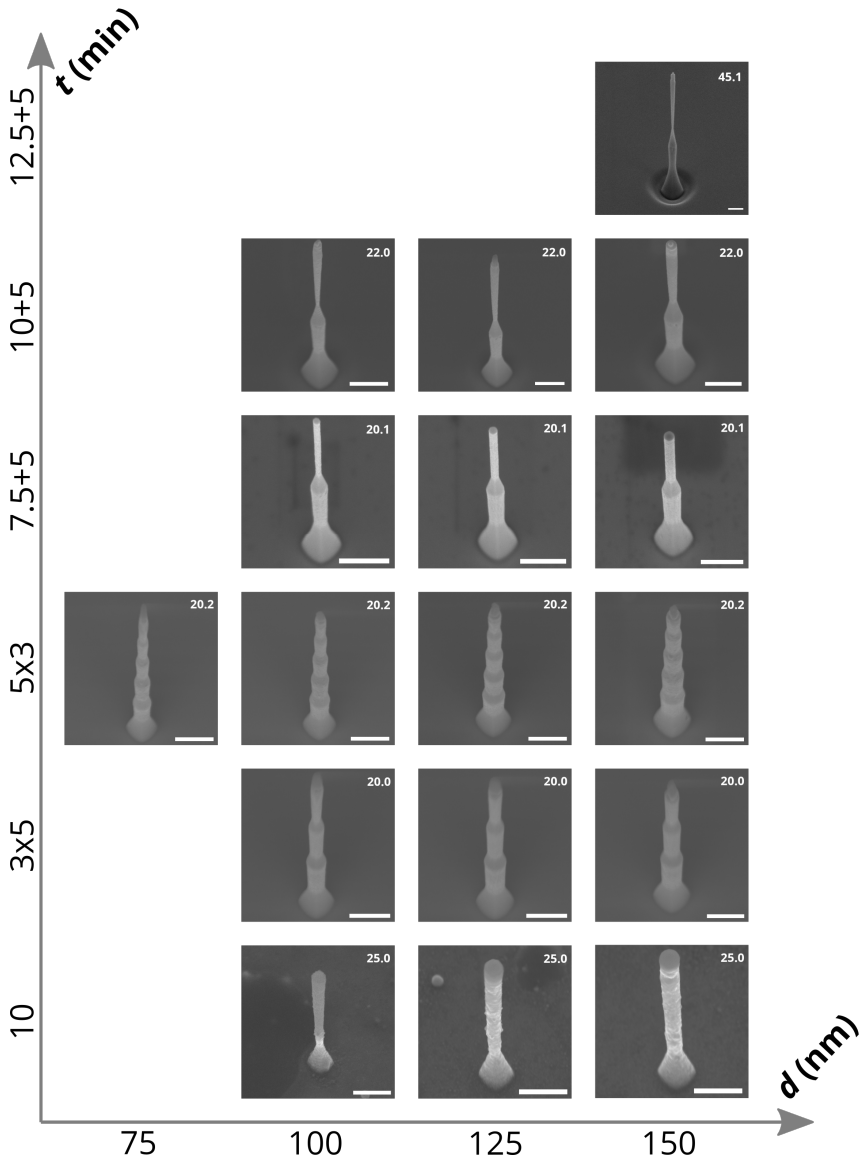


Fig. 7.5.: SEM images of the pillar-shaped structures etched for different durations with the optimized HBr-based recipe. All the scale bars correspond to 500 nm. The number given in each image represents an angle by which the SEM sample stage was tilted (approximately out-of-the-page direction). Passivating layers and the HSQ masks were removed from all the structures, except those etched with 3 or 5 interrupts.

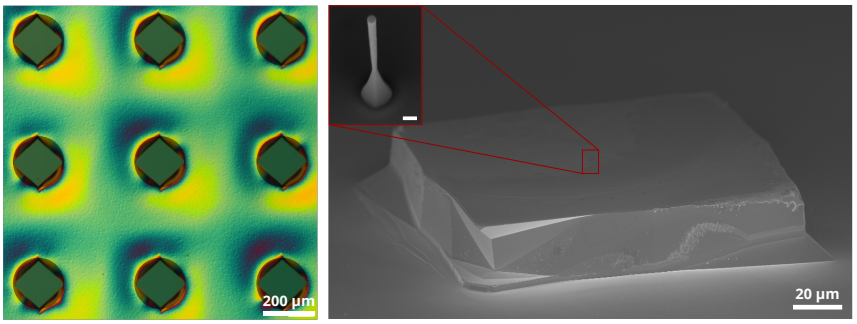


Fig. 7.6.: Pedestals pre-formed on the sample before dry etching of the pillar-shaped structures for easier specimen positioning with the APT electrode: (left) optical microscope image (taken with the Normaski technique) of an array of $\sim$35 µm height and $\sim$200 µm width (diagonally) structures, and an overlay of the used photolithography mask (black transparent circles); (right) SEM image of the pedestal structure (stage angle $\sim$70°) and the pillar-shaped structure dry etched in the middle (inset, the scale is 200 nm).

In order to overcome this issue, an approach of pre-forming high and wide flat-topped pedestals on the sample surface before etching of the pillar-shaped structures was devised. In this case, the APT electrode needs to be positioned above large pedestal visible with the positioning camera, requiring only fine adjustments to detect the pillar-shaped structure with quantum dots located near the middle of the pedestal.

The following procedure was used to form the pedestals: after the e-beam exposure of the mask for the pillar-shaped structures and in addition the alignment marks, a thin layer of Al_2O_3 was deposited in ALD in order to improve adhesion to the InP surface; the sample was then treated in the HMDS furnace resulting in the hydrophobic surface suitable for covering with the resist; the standard positive photo-resist was spin coated, the mask aligned to the alignment marks defined earlier in the e-beam, and a circular pedestals mask pattern exposed; finally, the sample was wet etched in HCl for 5 min and the resist was stripped.

An array of formed $\sim$35 µm high pedestal structures is shown in Fig. 7.6 (left). The use of the circular mask resulted in a number of different crystallographic planes exposed during an anisotropic InP sample etching in HCl. In general, as sharp features (except, of course, the specimen) are not desirable in the APT, mask optimization would be needed to end up with a more circular wet etched pedestal structure [188]. Nevertheless,

the formed pedestal structure does not interfere with the dry etching of the pillar-shaped specimen, as shown in Fig. 7.6 (right), and in this way controllable positioning with respect to the APT electrode is enabled.

7.3 Chapter summary and final considerations

From a number of existing microscopy methods, which are suitable for the quantum dots study, the atom probe tomography has possibly been used the least, despite its great potential. One of the main reasons for this is a very time consuming individual sample preparation with the focused ion beam, when actually a number of specimens are usually needed for the complete characterisation. This chapter focused on addressing this issue and proposed another, highly parallel, specimen formation method by dry etching the pillar-shaped structures on the pedestals pre-formed on the sample wafer.

Investigation of the quantum dots in the proposed pillar-shaped structures by the atom probe tomography, combined with other microscopy methods [189] as well as the micro-photoluminescence measurements [190, 191] would provide a comprehensive material information. This could potentially be used in further optimizing epitaxial growth conditions of quantum dots and subsequently better performance and understanding of semiconductor devices utilizing them.

8 Conclusions and Outlook

The last chapter of this thesis summarizes and concludes the main results and achievements. Future possibilities are then discussed.

8.1 Summary and conclusions

Optical interconnects are recognized as an integral part in the development of future on-chip optical communications and data processing applications. Central to this technology is achieving high speed and low energy consumption optical output devices. Two groups of potential integrated small-footprint laser devices are: (1) more "traditional" semiconductor lasers, steadily progressing in terms of energy consumption, output powers and operating speeds; (2) novel lasers that could bring radical change due to their unique characteristics. From the latter, the photonic crystal technology emerges not only as a way of realizing compact lasers, but also a number of optical components with a wide range of functionalities.

The aim of this work was to develop a process of transferring the buried heterostructure technology, well-known in standard semiconductor lasers, to the photonic crystal cavity lasers. In ordinary photonic crystal lasers, the active material layer extends across the entire device layer. This has a negative impact for the laser performance, because of the lack of carrier and optical mode confinement. Using quantum dots as the active material in these non-buried heterostructure laser devices, room temperature continuous-wave operation has been demonstrated. On the other hand, photonic crystal lasers with quantum wells are difficult to operate under such conditions because of excess heat and surface defect states as the active material is exposed to the ambient inside the etched photonic crystal holes. All of these problems are addressed if the buried heterostructure is embedded inside the photonic crystal cavity. However, forming the buried heterostructure with small dimensions is a challenging task as it

requires highly controllable etching process (or processes), which would leave smooth surfaces suitable for the subsequent material re-growth.

During the course of this work, three device processing generations are distinguished with respect to the fabrication process. Each transition was marked by a change that had a profound impact on the overall device performance.

In the first generation, the buried heterostructure regions were fabricated on the InP wafers that were then BCB bonded to 2" Si substrates. Subsequently, the photonic crystal patterns were aligned and transferred to the InP layer. No lasing was observed for the fabricated devices from this generation, as this double-sided processing approach results in significant misalignment between the buried heterostructure and the photonic crystal. The e-beam metrology experiments performed on the 2" InP-on-Si BCB bonded wafers confirmed large bonding-induced deformations of the device layer, unsuitable for the laser technology relying on high-precision alignment.

The second generation became possible as the direct wafer bonding was developed. The e-beam metrology experiments demonstrated that for the directly bonded wafers the alignment accuracy is limited not by bonding, but by process-induced wafer deformations. Single-sided processing became possible, in which the wafer bonding is performed at an early processing stage and the entire buried heterostructure photonic crystal laser is fabricated on already bonded InP-on-Si. Although the first laser with quantum wells was demonstrated, still significant misalignment between the buried heterostructure and photonic crystal cavity was caused by non-optimal fabrication of the alignment marks.

The third device processing generation addressed the issue with the alignment marks, and the resulting buried heterostructure photonic crystal lasers with quantum wells demonstrated more than two orders of magnitude better performance in terms of the threshold powers and the output powers. The best performing line-defect photonic crystal laser was determined to have sub-10 μW threshold power (estimated by considering an overlap between the optical pump laser beam and the buried heterostructure size, but not considering limited absorption by quantum wells) with a maximum output peak power of nearly 400 nW. These results compare favourably with similar photonic crystal laser devices which are the best-in-class.

Optimized device processing technology allowed the first-ever demonstration of the photonic crystal Fano lasers with the buried heterostructure. Besides Fano laser with the H0-type side-coupled nanocavity, which was demonstrated before using the sample with quantum dots extending across the entire device layer, the laser with larger L7 side-coupled cavity was also realized. The same single-mode laser behaviour was observed in the buried heterostructure Fano laser with the H0 nanocavity, with an exception that the device operates in the cw regime, without the observed self-pulsing, which was earlier caused by the active material inside the nanocavity. Interestingly, multi-mode behaviour was recognized in the laser with the L7 side-coupled cavity, with all the observed modes being wavelength-independent on the laser cavity length.

Unfortunately, no working laser devices with the quantum dots were realized. It is difficult to provide enough of gain for lasing due to a small optical mode confinement when quantum dots in the buried heterostructure are embedded into the photonic crystal cavity. In addition, the buried heterostructure fabrication process might be damaging to the quantum dots layer. Better dots might be required for lasing demonstration with the buried heterostructure.

In order to investigate quantum dots in detail, a special fabrication process was developed for realizing high aspect-ratio pillar-shaped structures with the embedded quantum dots suitable for the atom probe tomography study.

8.2 Outlook

The buried heterostructure photonic crystal laser fabrication method developed in this work has potential for demonstrating high performance and low energy consumption devices in the future. Demonstrations presented in this work relied on optical-pumping, however an efficient electrical-pumping scheme is ultimately required for real application value.

Numerous possible processing improvements exist that could increase the output powers and decrease the threshold power values of current lasers. First of all, these are related to the buried heterostructure fabrication. A more accurate control of the dry etching procedure is needed to stop at the required layer during the mesa-structures formation to guarantee a successful InP material re-growth afterwards. Also, it is important to

figure out how to make the surface planar after the 2^{nd} material re-growth, as otherwise it introduces scattering losses that have negative impact for the device performance. On top of that, improved quality of the photonic crystal holes for achieving higher cavity Q-factors is very important.

If the aforementioned improvements are realized, it could lead to the first-ever demonstration of the buried heterostructure photonic crystal laser with quantum dots. It seems difficult to expect lasing from the samples fabricated using the current technology. On the other hand, there is also a possibility of increasing the density of quantum dots during the epitaxial growth or increasing the number of stacked quantum dot layers. More detailed material information of dots would be very helpful for the process improvement, therefore analysing quantum dots embedded in the developed pillar-shaped structures with the atom probe tomography is highly anticipated.

In order to improve the device performance by improved alignment, the 4^{th} processing generation was proposed. As indicated by the e-beam metrology experiments, bonding 2" InP wafers to 4" Si substrates and restricting the exposure and alignment region to 2" size can result in very small processing-induced deformations. With a smaller controlled misalignment, larger buried heterostructure regions could be fabricated.

Finally, in terms of the device designs, interesting future demonstrations are expected by employing the developed buried heterostructure photonic crystal platform. In particular, the Fano laser offers many possibilities that need closer investigation. Placing the buried heterostructure by choice into the Fano laser cavity and/or side-coupled cavity, both cw and self-pulsing operation regions could be accessed. Finally, the possibility of realizing theoretically proposed terahertz frequency modulation in Fano lasers could have a major impact for the on-chip optical communications.

A

Process Flows

A.1 Direct bonding

Full process details are given below for the optimized fabrication of the buried heterostructure photonic crystal lasers directly bonded to silicon.

MOVPE sample growth.

Equipment: MOVPE (Emcore D125).

Epitaxial structures of selected quantum wells and quantum dots samples are given in appendix C.

Equipment: PL-mapper (Accent RPM2000).	
PL mapping	
PL mapper	532/980 nm, surface-map/wide-scan

Si wafer preparation.

Thermal SiO_2 growth on Si wafers.

Prepare a batch of samples (e.g. 25) at once.

Optimize SiO_2 thickness for the desired InP membrane thickness.

Wafer bonding.

Preferably done right after the InP wafer growth for the optimal surface cleanliness.

Wear a facial mask (shield) and a new pair of gloves for optimal cleanliness.

Equipment: ALD1 (Picosun R200).

Al_2O_3 deposition in ALD	
Temperature	250 °C
Dummy run (empty chamber)	25×(Al_2O_3+H_2O), 4× H_2O
Wafer loading	Gently place wafers on the metal grid, close the chamber, evacuate
Deposition run	25×(Al_2O_3+H_2O), 4× H_2O

Equipment: Teflon bonding chuck and teflon pressing tool.

Pre-bonding	
Si wafer unloading	Place and align on the teflon chuck (face up)
InP wafer unloading	Position and align a few mm above the Si wafer (face down)
Putting in contact	Release the InP wafer, let it drop on Si
Applying pressure	Quickly press with the teflon tool in the middle of the InP wafer, then press around*

*At this point, wafers should be locked together.

Equipment: Wafer Bonder 02 (Süss Microtec Substrate Bonder SB6 Gen2).

Bonding in the wafer bonder	
Loading	Place on the chuck, cover with the glass top
Bonding process	300 °C, 2 kN, vacuum, 1 h bonding (∼ 2.5 h total)
Unloading	Inspect if no cracks are visible

Equipment: III-V ICP (SPTS Multiplex ICP).

Substrate removal	
Al_2O_3 back-side etch	BCl_3/Ar, recipe: "Al_2O_3 etch", 1 min
HCl etch	∼ 1 h, use magnetic stirrer
DI water	rinse
N_2 blow dry	

Sacrificial later removal	
(10 %)H_2SO_4:H_2O_2=1 : 1 etch	30 s
DI water	rinse
N_2 blow dry	

Equipment: PL-mapper (Accent RPM2000).

PL mapping	
PL mapper	532/980 nm, surface-map/wide-scan

Equipment: Ellipsometer VASE (J.A. Woollam VASE Ellipsometer).

Thickness mapping	
Ellipsometer	Angle scan: $65° - 70° - 75°$, acq. time: 5 s

E-beam exposure of the buried heterostructure.

HSQ Fox-15 e-beam resist should be taken out of the refrigerator $15 - 30$ min before the spin coating. Surface preparation can be done meanwhile.

Surface preparation*	
BHF	>10 s
DI water	rinse
N_2 blow dry	

*A very important step for proper HSQ adhesion to the InP surface.

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating	
Wafer baking	5 min, 220 °C
HSQ coating	60 s, 6000 RPM, 3000 /s^2
Wafer baking	2 min, 120 °C
Wafer baking	2 min, 220 °C

Equipment: E-beam Writer 9500 (JEOL JBX-9500FSZ).

Buried heterostructure mask exposure	
Loading*	preferably 2" Ti cassette, slot D
Condition file	45na_ap8
Dose	3800 μC/cm^2, with PEC

*Keep the cassette inside the e-beam for >30 min to stabilize the temperature, check it with the temperature monitor software.

HSQ development	
AZ400K:H_2O=1 : 3	2 min 40 s
DI water	rinse
N_2 blow dry	

Formation of mesa-structures by dry etching.

Equipment: III-V ICP (SPTS Multiplex ICP).

III-V ICP dry etching	
Chamber preparation	Heat up to 180 °C, 30 min O_2 clean
Chamber preconditioning	15 min “HBr etch”, dummy Si wafer
Sample crystalbonding (Crystalbond 509, clear color)	on 4” Si carrier, use hotplate
Etching	$20 - 30$ s “HBr etch”, use EtchDirector to stop on time
Unloading	Put into the glass beaker with DI water to neutralize Br
Chamber cleaning	30 min O_2 clean if no more InP etching is done
Sample crystal(un-)bonding	from 4” Si carrier, use hotplate

Equipment: Ellipsometer VASE (J.A. Woollam VASE Ellipsometer).

Thickness mapping	
Ellipsometer	Angle scan: $65° - 70° - 75°$, acq. time: 5 s
Data analysis	Estimate how much InP+active material was etched

1st MOVPE re-growth (selective area growth).

Equipment: III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

Sample preparation for the re-growth	
Plasma Ashing*	5 min, 0.2 mbar, 40% power/
	5 min, 0.8 mbar, O_2 = 300 ml/min, 400 W
H_2SO_4 cleaning/etching**	3 min ($\sim$ 15 nm InP etch assumed)
DI water	1 min
DI water (bubbler)	3 min
N_2 blow dry	No more tweezers, use vacuum handler
Loading into the load-lock	As soon as the sample is dried***

*Plasma asher 1 might be cleaner, confirmation is needed.

**Use new H_2SO_4, because based on experience re-using it can caused problems (particles after re-growth).

***Make sure wafer backside is completely dry!

Equipment: MOVPE (Emcore D125).

InP regrowth in the MOVPE	
Re-growth thickness	Estimated from the EtchDirector data and from comparing ellipsometer thickness maps

Equipment: Ellipsometer VASE (J.A. Woollam VASE Ellipsometer).

Thickness mapping	
Ellipsometer	Angle scan: $65° - 70° - 75°$, acq. time: 5 s
Data analysis	Estimate how much InP was re-grown

Alignment marks protection/HSQ mask removal.

Surface preparation	
Wafer baking	5 min, 110 °C
Surpass4000	1 min dip
DI water (beaker)	1 min dip
DI water	rinse
N_2 blow dry	

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating AZ nLOF2020 resist	
Resist coating	10 s, 500 RPM, 1000 /s^2
	30 s, 2000 RPM, 3000 /s^2
Wafer baking	60 s, 110 °C

Equipment: Aligner MA6 – 2 (Süss MA6/BA6 contact mask aligner and bond aligner).

UV lithography exposure alignment marks protection	
Mask	"BH PhC Alignment Marks 05 2017": Alignment Marks Longer
Mode	Hard
Time	10 – 12 s
Intensity	11 – 13 mW/cm^2

AZ nLOF2020 cross-linking	
Wafer baking	60 s, 110 °C

Equipment: TMAH Manual.

AZ nLOF2020 development	
AZ726MIF: 2.38% TMAH	120 s
DI water bath	a few min
N_2 blow dry	

HSQ removal from the buried heterostructure regions	
BHF	2 min
DI water	rinse
N_2 blow dry	

Equipment: Ultrasonic bath; III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

AZ nLOF2020 resist strip	
Remover 1165	15 min
Ultrasonic bath	Level 1, room temperature
Acetone	5 min
IPA	rinse
ethanol	rinse
N_2 blow dry	
Plasma Ashing	5 min, 0.2 mbar, 40% power/
	5 min, 0.8 mbar, $O_2 = 300$ ml/min, 400 W

2nd MOVPE re-growth (planarization).

Equipment: III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

Sample preparation for the re-growth	
Plasma Ashing	5 min, 0.2 mbar, 40% power/
	5 min, 0.8 mbar, $O_2 = 300$ ml/min, 400 W
H2SO4 cleaning/etching	3 min ($\sim$ 10 nm InP etch assumed)
DI water	1 min
DI water (bubbled)	3 min
N_2 blow dry	No more tweezers, use vacuum handler
Loading into the load-lock	As soon as the sample is dried

Equipment: MOVPE (Emcore D125).

InP regrowth in the MOVPE	
Re-growth thickness	Estimated from comparing
	ellipsometer thickness maps

Equipment: Ellipsometer VASE (J.A. Woollam VASE Ellipsometer).

Thickness mapping	
Ellipsometer	Angle scan: $65° - 70° - 75°$, acq. time: 5 s
Data analysis	Estimate how much InP was re-grown

Alignment marks etching/sample protection.

Surface preparation	
Wafer baking	5 min, 100 °C
Surpass3000	1 min dip
DI water (beaker)	1 min dip
DI water	rinse
N_2 blow dry	

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating AZ5214E resist	
Resist coating	10 s, 500 RPM, 1000 /s2
	30 s, 3000 RPM, 3000 /s^2
Wafer baking	90 s, 90 °C

Equipment: Aligner MA6 − 2 (Süss MA6/BA6 contact mask aligner and bond aligner).

UV lithography exposure wafer surface protection	
Mask	"BH PhC Alignment Marks 05 2017": Alignment Marks Shorter
Mode	Hard
Time	10 s
Intensity	11 − 13 mW/cm^2

Equipment: TMAH Manual.

AZ5214E development	
AZ726MIF: 2.38% TMAH	120 s
DI water bath	a few min
N_2 blow dry	

Equipment: III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

Surface preparation for wet etching	
Plasma Ashing	20 s, 0.2 mbar, 40% power/
	20 s, 0.8 mbar, O_2 = 300 ml/min, 400 W
Wafer (hard) baking	120 s, 90 °C

InP etching around the alignment marks	
$HCl:H_3PO_4 = 1:4$	1 min
DI water	rinse
N_2 blow dry	

Equipment: III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

AZ5214E resist strip	
Acetone	5 min
IPA	rinse
ethanol	rinse
N_2 blow dry	
Plasma Ashing	5 min, 0.2 mbar, 40% power/
	5 min, 0.8 mbar, O_2 = 300 ml/min, 400 W

Hard-mask deposition.

Equipment: PECVD4 (SPTS Multiplex PECVD).

SiN_x hard-mask deposition in PECVD	
Test deposition	recipe: "HF SIN with wafer clean", dummy Si
Ellipsometer	Determine SiN_x thickness on Si
Real deposition	recipe: "HF SIN with wafer clean", around 17 min
Thickness	around 200 nm (deep red-violet colour)

E-beam alignment/exposure of the photonic crystal patterns.

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating ZEP520A	
Wafer baking	5 min, 180 °C
Resist coating	5 s, 500 RPM, 200 /s^2
	60 s, 2600 RPM, 1500 /s^2
Wafer baking	3 min, 180 °C

Equipment: E-beam Writer 9500 (JEOL JBX-9500FSZ).

Alignment/photonic crystal mask exposure	
Loading	preferably 2” Ti cassette, slot D
Pre-alignment	P and Q global marks
Condition file	2na_ap4
Alignment*	P and Q global marks
	Chip marks for individual chips
Dose	$260 - 290$ μC/cm^2, with PEC

*Optimized e-beam alignment marks detection parameters	
BE Coarse gain	60|1
BE Middle gain	3|14
BE Fine gain	130|128
WAVE offset	128|121
BE offset	1550|2040

ZEP development	
ZED N50	3 min
IPA	30 s
N_2 blow dry	

Wafer cleaving into quarters
Manual

Transfer of the photonic crystal patterns into the hard-mask

Performed on a quarter of a 2" wafer.

Equipment: III-V RIE (Plassys MG300).

RIE dry etching	
Etching	17 min “Si3N4STD” on 2” GaAs
Chamber cleaning	10 min “CLEAN”, empty chamber

Wafer cleaving into chips
Manual

Equipment: Ultrasonic bath; III-V Plasma Asher (Diener Pico)/Plasma Asher 1 (TePla 300).

ZEP resist strip in the ultrasonic bath	
Remover 1165	2 hours
Ultrasonic bath	Level 1, 60 °C temperature
Acetone	5 min
IPA	rinse
ethanol	rinse
N_2 blow dry	
Plasma Ashing	5 min, 0.2 mbar, 40% power/
	5 min, 0.8 mbar, $O_2 = 300$ ml/min, 400 W

Transfer of the photonic crystal patterns into the InP

Performed on a chip.

Equipment: III-V RIE (Plassys MG300).

RIE dry etching	
Chamber pre-conditioning	10 min “PRECOND”, empty chamber
Etching	14 cycles (around 2 h) “CYC8CH42”
	on a quarter of a 2” InP
Chamber cleaning	30 min “VLCLEAN”, empty chamber

Membranization

SiN_x wet etch and membranization	
SiOetch	$\sim$ 10 min (etch rate $\sim$ 80 nm/min)
DI water	rinse
N_2 blow dry	

A.2 BCB bonding

For completeness, the process details for the buried heterostructure photonic crystal laser fabricated with the BCB bonding are also given (indicated are only different processing steps).

In this fabrication scheme, ellipsometer measurements might be very difficult.

As no bonding is performed at the beginning of the processing, it starts from the "*E-beam exposure of the buried heterostructure*" step.

"*Alignment marks etching/sample protection*" step must be performed right after the "1st *MOVPE regrowth (selective area growth)*" step.

After the "2nd *MOVPE regrowth (planarization)*" step, the entire wafer surface is covered with a thick glass layer:

Equipment: PECVD4 (SPTS Multiplex PECVD).

SiO_2 deposition in PECVD	
Test deposition	recipe: “HF SiO2 with wafer clean”, dummy Si
Ellipsometer	Estimate SiO_2 thickness on Si
Real deposition	recipe: “HF SiO2 with wafer clean”, around 16 min
Thickness	around 1 μm

Then, BCB is spin coated:

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating AP3000 adhesion promoter on InP	
Wafer baking	5 min, 160 °C
Adhesion promoter coating	5 s, 500 RPM, 1000 /s^2
	60 s, 2000 RPM, 2000 /s^2
Wafer baking	60 s, 160 °C

Equipment: Spin Coater: Labspin 02/03 (Süss MicroTec model LabSpin6 TT).

Spin coating AP3000 and BCB 3022 − 46 on Si w/ SiO_2	
Wafer baking	5 min, 160 °C
Adhesion promoter coating	5 s, 500 RPM, 1000 /s^2
	60 s, 2000 RPM, 2000 /s^2
Wafer baking	60 s, 160 °C
BCB spin coating	60 s, 5500 RPM, 4000 /s^2
Wafer baking	5 min, 90 °C

Expected BCB thickness is around 2 μm.

Then, wafers are bonded:

Equipment: Wafer Bonder 02 (Süss Microtec Substrate Bonder SB6 Gen2).

Bonding in the wafer bonder*	
Loading	Place on the chuck, cover with the glass top
Bonding process	250 °C, 2 kN, vacuum, 1 h bonding ($\sim$ 2.5 h total)
Unloading	Inspect if no cracks are visible

*BCB bonding in the Wafer Bonder 02 is no longer allowed. Use Wafer Bonder 03 (NILT CPB: Compact Polymer Bonder) instead. Bonding parameters need to be re-optimized.

Equipment: Plasma Asher 1 (TePla 300).

Substrate removal	
BCB removal (backside, edges)	recipe: 04
in plasma asher	O_2=350 sccm, CF_4=50 sccm, P=600 W
	10 min
HCl etch	$\sim$ 1h, use magnetic stirrer
DI water	rinse
N_2 blow dry	

Sacrificial later removal	
(10 %)H_2SO_4:H_2O_2=1 : 1 etch	30 s
DI water	rinse
N_2 blow dry	

The processing is then continued at the "*Hard-mask deposition*" step and the rest is the same.

B

Membrane Effect

Important, but easily overlooked feature encountered in the layered structure of bonded materials is the "membrane effect". In essence, refractive index differences between various material layers cause reflections at the interfaces, resulting in interference inside the stack and altered light emission properties.

All photonic crystal membrane lasers fabricated and used in this work have a design thickness of 250 nm, forming a resonator in the vertical direction for the wavelength range centred around the standard optical communications wavelength of 1550 nm:

$$\frac{\lambda}{2n} \approx \frac{1550 \text{ nm}}{2 \cdot 3.17} \approx 244.48 \text{ nm} \tag{B.1}$$

where the refractive index n for InP around that wavelength is taken as 3.17[1]. Therefore, suppression of the out-of-plane emission from the membrane and increased overall efficiency for the in-plane radiation is expected. However, the sample structure is different during fabrication process, before the membrane is suspended in air. The actual layered structure at the beginning of the device processing is shown in Fig. B.1. Multiple interfaces exist in the directly bonded stack, which can significantly alter photoluminescence (PL) emission from the active layer inside the InP and thus complicate the material characterisation during wafer processing.

Fig. B.2 compares normalized PL spectra of as-grown epitaxial InP wafer with 10 layers of InGaAsP/InAlGaAs quantum wells and identically grown 1 quantum well sample after the direct bonding to a bare Si substrate. No noticeable spectral shape difference is observed for the bonded stack, as there is no significant refractive index variation of the material layers. On the other hand, clear differences are observed in Fig. B.3, which compares two 1 quantum well layer wafers from the same growth batch directly bonded to the Si substrate with thermally grown SiO_2 of around

[1] Active layers of different refractive indices inside the membrane are not considered in this simple estimate.

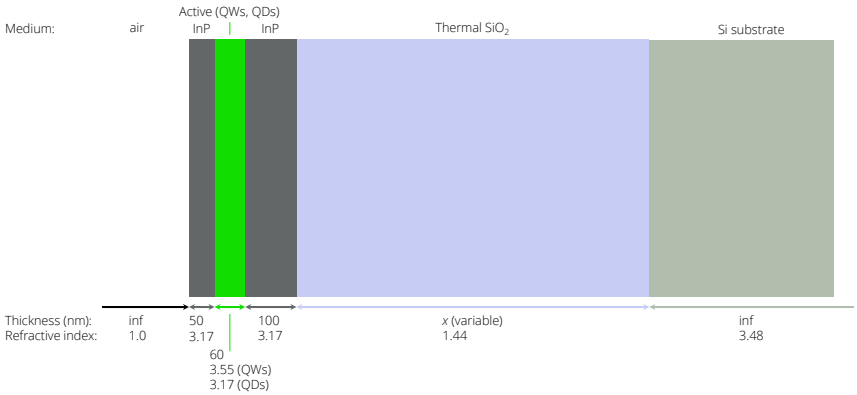


Fig. B.1.: Material layers after the direct wafer bonding at the beginning of device processing (turned on the side). Refractive indices are given at 1550 nm wavelength.

2.77 (left) and 2.89 μm (right). "Dips" and peak "plateaus" appear in the measured spectra. The "real" spectral shape from Fig. B.2 is "hidden" by the "membrane effect" in Fig. B.3.

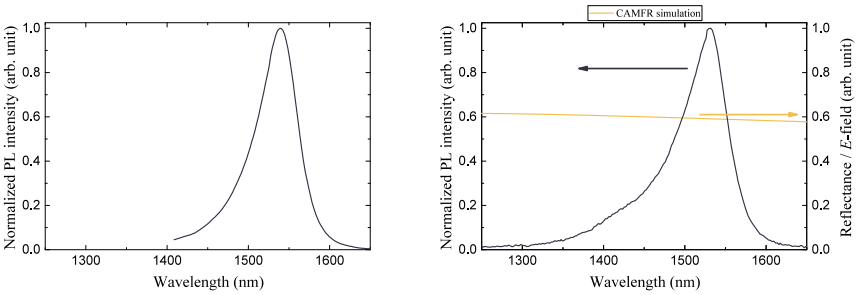


Fig. B.2.: Normalized PL spectra for: (left) as-grown epitaxial InP wafer with 10 InGaAsP/InAlGaAs quantum well layers; (right) identically grown 1 quantum well layer InP sample directly bonded to a bare Si substrate. Simplified CAMFR package simulation represents the fundamental mode amplitude reflectance of a field impinging on the stack in Fig. B.1.

The "membrane effect" can be qualitatively understood by considering the free spectral range (FSR) of the sample stack, given by the formula $\Delta\lambda_{FSR} = \lambda^2/(2dn)$. Assuming a weak Fabry-Perot cavity formed by the material stack, the detected light that is emitted outwards from the active

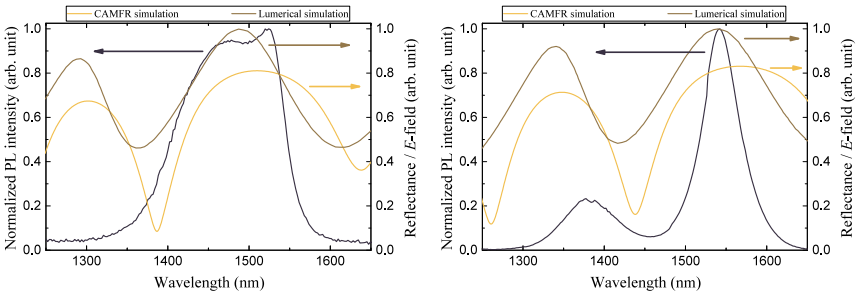


Fig. B.3.: Normalized photoluminescence spectra for: (left) 1 quantum well layer InP sample (identical to the sample from Fig. B.2, left) directly bonded to a Si substrate with 2.77 μm thermal glass; (right) 1 quantum well layer InP sample (identical to the sample from Fig. B.2, left) directly bonded to a Si substrate with 2.89 μm thermal glass. Simplified CAMFR package simulation represents the fundamental mode amplitude reflectance of a field impinging on the stack in Fig. B.1; a full 3D Lumerical package simulation represents a normalized E-field amplitude detected above the stack emitted by the dipole placed inside the active material of the InP wafer.

layer will have periodic "dips". Corresponding FSR for the InP membrane of 250 nm thickness is around 1.5 μm, and does not influence the characterisation of the structure. On the other hand, a few μm's thick InP and SiO_2 stack will have FSR on the order of a few hundred nm's, which can significantly interfere with the PL measurements such as represented in Fig. B.3.

A simplified vectorial eigenmode expansion simulation using the freeware CAMFR package [192] and a full 3D FDTD simulation with the commercial Lumerical package[2] [193] are compared with the measured PL spectra in Figs. B.2 and B.3. Qualitative agreement exists between the compared experimental measurements and simulations.

An optimum thermal SiO_2 layer thickness of around 1.3 μm was determined for the sample stack in Fig. B.1 from the simulations, and it was used for fabricating devices characterized in chapter 6. Nevertheless, the photoluminescence spectra abnormalities have still been observed for a number of directly bonded wafers, indicating that more detailed investigations are needed.

[2]Performed by K. S. Mathiesen.

C

Parameters of Quantum Wells and Quantum Dots

This appendix contains specific parameters of the quantum wells and quantum dots device samples used in this work.

All the samples used in this work were epitaxially grown with the MOVPE (chapter 5). For quantum wells, quaternary InGaAsP/InAlGaAs were used. More details about the growth procedure can be found in [194, 195]. The quantum dots are InP-capped self-assembled InAs quantum dots grown on InP. More information about the growth principle can be found in [96, 99].

Layer	Thickness (nm)
InP	73
$In_{0.52}Al_{0.48}As$	10
3x $Al_{0.286}In_{0.458}Ga_{0.256}As$	10
3x $Ga_{0.217}In_{0.783}As_{0.846}P_{0.154}$	7.7
3x $Al_{0.286}In_{0.458}Ga_{0.256}As$	10
$In_{0.52}Al_{0.48}As$	10
InP	25
$In_{0.53}Ga_{0.47}As$	250
InP buffer	200
InP substrate	350 um

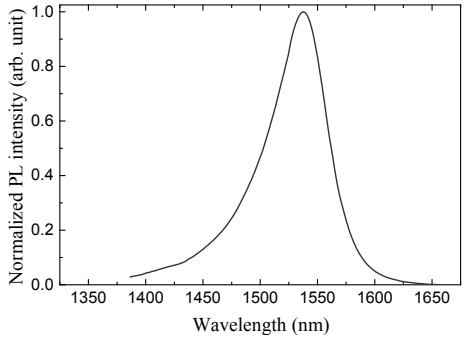


Fig. C.1.: Layer structure of the device sample ("Sample A" from chapter 6) with 3 layers of quantum wells (InGaAsP well compressively strained, InAlGaAs barrier tensile strained) and the normalized photoluminescence spectrum of the corresponding calibration sample with 10 layers of quantum wells; the measured FWHM is 59 nm.

Layer	Thickness (nm)
InP	68
$In_{0.52}Al_{0.48}As$	10
3x $Al_{0.291}In_{0.469}Ga_{0.24}As$	11.3
3x $Ga_{0.224}In_{0.776}As_{0.846}P_{0.154}$	8.1
3x $Al_{0.291}In_{0.469}Ga_{0.24}As$	11.3
$In_{0.52}Al_{0.48}As$	10
InP	20
$In_{0.53}Ga_{0.47}As$	200
InP buffer	130
InP substrate	350 um

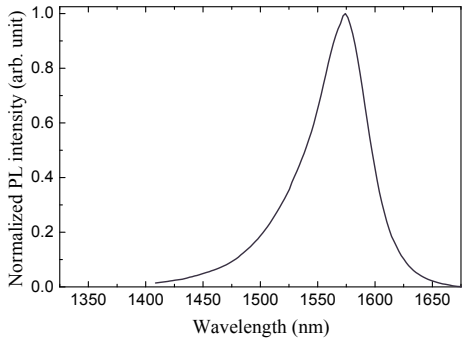


Fig. C.2.: Layer structure of the device sample ("Sample B" from chapter 6) with 3 layers of quantum wells (InGaAsP well compressively strained, InAlGaAs barrier tensile strained) and the normalized photoluminescence spectrum of the corresponding calibration sample with 10 layers of quantum wells; the measured FWHM is 58 nm.

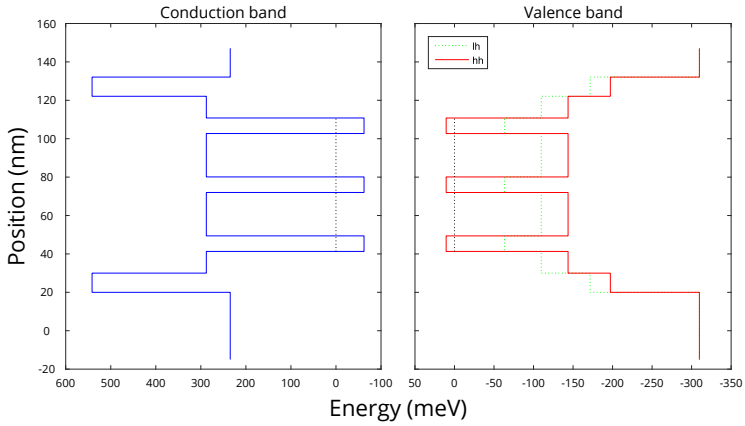


Fig. C.3.: As-grown band diagram calculated for the 3 quantum well layers sample in Fig. C.2. Black dashed lines indicate the position of the lowest quantum confined state.

	Layer	Thickness (nm)
	InP	66
3x	InP HT	15.6
3x	InP LT	13.6
3x	InAs	0.4
	InP	20
	$In_{0.53}Ga_{0.47}As$	250
	InP buffer	130
	InP substrate	350 um

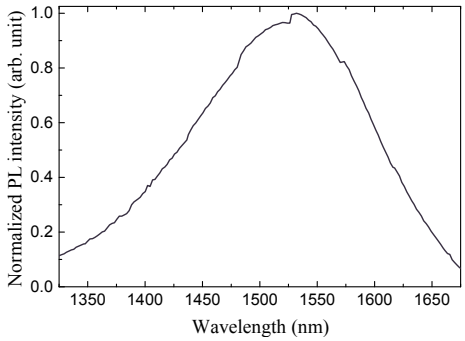


Fig. C.4.: Layer structure of the device sample (the best performing device with quantum dots from chapter 6) with 3 layers of InAs quantum dots and the normalized photoluminescence spectrum of the corresponding calibration sample with 1 quantum dot layer; the measured FWHM is 180 nm.

	Layer	Thickness (nm)
	InP	84
5x	InP HT	11.2
5x	InP LT	9
5x	InAs	0.4
	InP	34
	$In_{0.53}Ga_{0.47}As$	200
	InP buffer	170
	InP substrate	350 um

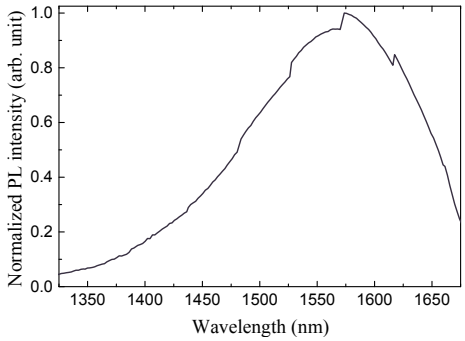


Fig. C.5.: Layer structure of the device sample (not used in this work, however it shows that spacing between quantum dot layers can be successfully reduced) with 5 layers of InAs quantum dots and the normalized photoluminescence spectrum of the corresponding calibration sample with 5 layers of quantum dots; the measured FWHM is 175 nm.

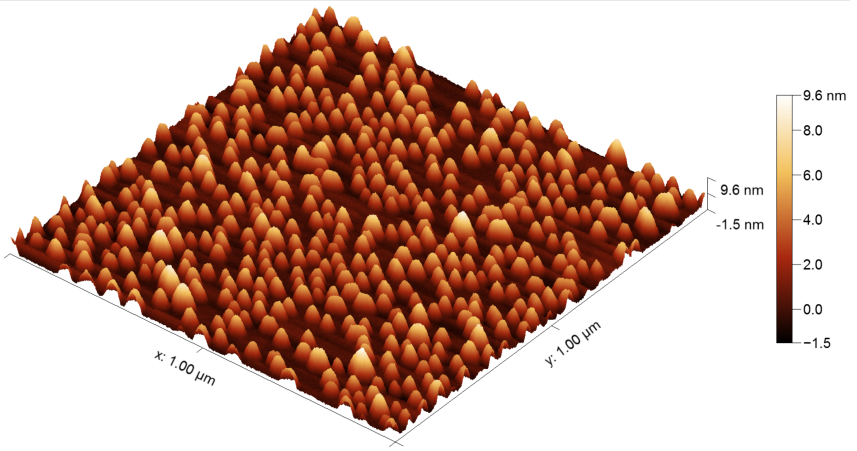


Fig. C.6.: AFM surface scan of the uncapped InAs self-assembled quantum dots, typical for the quantum dots samples used in this work. The measured surface density is $4.8 \cdot 10^{10}$ cm^{-2}.

D

Alignment Precision Metrology on Wafer Quarters

Chapter 3 was dedicated to examining distortion induced in the bonded InP-on-Si wafers. Here, a link between the general analysis and the specific case relevant to the device-processing is provided.

An illustrative example of the measured distortion of the directly bonded single-side processed wafer was given in Fig. 3.8 in chapter 3. During the actual device processing, when the alignment between the photonic crystal and the buried heterostructure is performed, dedicated chip alignment marks are used for different wafer quarters. Using Fig. 3.8 from chapter 3 as an illustration, the achievable alignment accuracy on each wafer quarter after the chip alignment is shown in Fig. D.1. For this specific case, 4 chip marks separated by 1.2 cm were used for each quarter. The alignment procedure is identical as explained in detail in chapter 3 section *Experimental procedures and e-beam metrology principle*, except that instead of all, only 4 of the alignment marks were used to determine the optimal linear correction components, which were then applied to the rest of them inside each quarter (thus, its overall distortion is not necessarily minimized). Comparing Fig. 3.8 from chapter 3 and Fig. D.1, it can be seen that the distortion of each quarter is reduced when the wafer area enclosed by the alignment marks is smaller. The quarter in the bottom left stays the most distorted even after the chip alignment.

After the experiments on a full 2" wafer were completed, it was manually cleaved into 4 quarters. Two of them were re-measured in the e-beam using the same metrology procedure as described in chapter 3 section *Experimental procedures and e-beam metrology principle*, except that a special cassette was used suitable for mounting smaller chips. The repeated experimental measurements and the 4 chip marks alignment is shown in Fig. D.2, where the placement of each quarter in the figure corresponds to its original position in a full 2" wafer. Significant shift in the alignment marks positions are observed, justifying observations and conclusions given

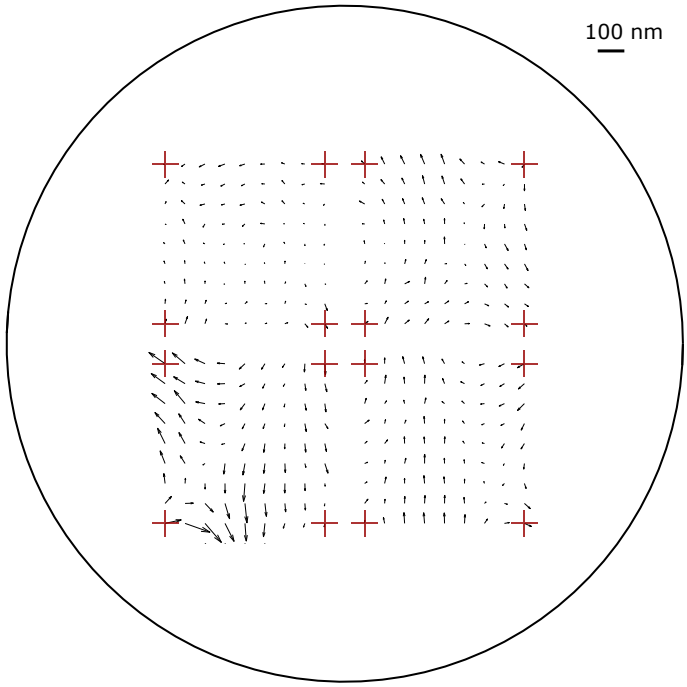


Fig. D.1.: Vector map representing processing-induced deformation of the double-side processed InP layer directly bonded to 2" Si wafer. Selected 4 alignment marks from each quarter were used for calculating and applying the linear correction components. The data for the plot is taken from Fig. 3.8 from chapter 3. Black circle indicates outline of the 2" wafer; the scale bar is for the vectors.

in chapter 3 section *E-beam metrology of bonded samples*. More specifically, it shows that the achievable alignment accuracy is decreased when the processed wafer is cleaved into smaller pieces, suggesting that the entire processing until and including the alignment step should be carried out on a full 2" wafer. This approach was applied to fabricating most of the devices presented in this work.

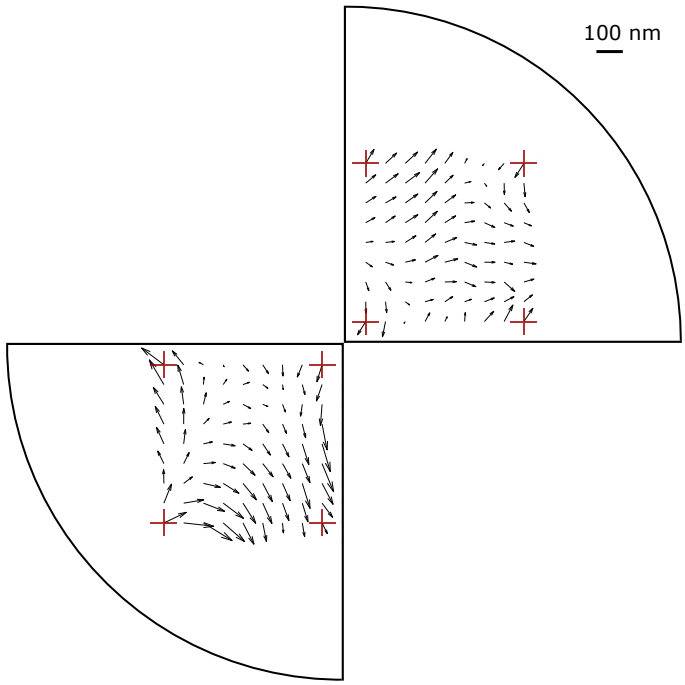


Fig. D.2.: Vector map representing processing-induced deformation of the double-side processed InP layer directly bonded to 2" Si wafer after manually cleaving it into separate quarters. The placement of each quarter in the figure corresponds to its original position in Fig. D.1. Selected 4 alignment marks from each quarter were used for calculating and applying the linear correction components. Black enclosing lines indicate outline of the quarter of the 2" wafer; the scale bar is for the vectors.

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Acronyms

AFM atomic force microscopy. 76, 81–86, 111, 148

ALD atomic layer deposition. 36, 46, 57, 120

APT atom probe tomography. 11–13, 111–114, 118, 120, 121, 125, 126

ASE amplified spontaneous emission. 102, 104–106, 108

BCB benzocyclobutene. 33–35, 43–46, 50–54, 56, 108, 124, 137

BH buried heterostructure. 8, 9, 11–13, 16, 17, 30, 31, 33, 46, 50, 53–63, 65–72, 75–77, 79–87, 89, 93–95, 97–109, 114, 115, 123–127, 137, 149

BHF buffered HF. 115

CMOS complementary metal–oxide–semiconductor. 2, 33

CMP chemical-mechanical polishing. 37

CPU central processing unit. 3, 4

DBR distributed Bragg reflector. 8, 11

DFB distributed feedback. 8, 11

DOS density of states. 18, 26, 28

DR distributed reflector. 8

DUV deep ultraviolet. 34, 50

FIB focused ion beam. 113, 121

FSR free spectral range. 98, 142, 143

FWHM full width at half maximum. 145–147

GPU graphics processing unit. 2

HMDS hexamethyldisilazane. 120

HPC high-performance computing. 5, 6

HSQ hydrogen silsesquioxane. 57–61, 67, 75, 81, 82, 86, 114–119

ICP inductively coupled plasma. 36, 58, 61, 64, 65, 71–75, 78, 80, 114

ICT information and communications technologies. 1–4

IR infrared. 91, 92

IRDS international roadmap for devices and systems. 6

ITRS international technology roadmap for semiconductors. 3, 6

LEAP lambda-scale-embedded active region photonic crystal. 9, 10

LED light emitting diode. 24

MBE molecular beam epitaxy. 65

MOCVD metal-organic chemical vapour deposition. 65

MOVPE metal-organic vapour phase epitaxy. 34, 37, 50–52, 59, 64–66, 76, 79–84, 86, 108, 145

OMVPE organometallic chemical vapour deposition. 65

OMVPE organometallic vapour phase epitaxy. 65

OSA optical spectrum analyser. 91, 92

PECVD plasma-enhanced chemical vapour deposition. 35, 36, 49, 60

PhC photonic crystal. 9–13, 17–21, 23, 30, 31, 33, 46, 50, 53, 54, 56, 60–63, 65, 66, 69–71, 81, 84, 85, 87, 89, 92, 94–106, 108, 109, 111, 114, 123–127, 137, 141, 149

PL photoluminescence. 89, 93, 104, 107, 121, 141–143, 145–147

QD quantum dot. xiv, 10–13, 26, 28, 29, 57, 74, 80, 89, 94, 98, 101, 102, 104–109, 111, 114, 118, 120, 121, 123, 125, 126, 145, 147, 148

QW quantum well. xiv, 11–13, 26–29, 56, 57, 69–71, 74, 75, 77, 80, 89, 93–95, 97–101, 103, 104, 108, 109, 123, 124, 141–143, 145, 146

RIE reactive ion etching. 35, 61, 64, 65, 70, 71

RMS root mean square. 76

RTA rapid thermal annealing. 45

SAE selective area epitaxy. 81

SAG selective area growth. 78, 81, 84

SEM scanning electron microscope. 55, 56, 61, 62, 71, 75, 95, 97, 116, 117, 119, 120

SMSR side-mode suppression ratio. 102, 103

TEM transmission electron microscopy. 111, 116, 118

ToF time-of-flight. 112, 113

VCSEL vertical-cavity surface-emitting laser. 8, 9, 11, 16, 24

XSTM cross-sectional scanning tunneling microscopy. 111