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34.3 fJ/conv.-step 8 MHz Bandwidth 4th-Order Pseudo-Differential Ring-Amplifier Based Continuous-Time Delta-Sigma ADC in 65 nm

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Abstract—This work presents two pseudo-differential ring amplifiers suitable for continuous-time operation as an alternative to traditional amplifiers. The designs retain the advantages of ring amplifiers, scale with process technology and do not require a periodic reset. The ring amplifiers are designed to operate in an integrator configuration and they use different methods to achieve stability in continuous time. A prototype was fabricated in 65 nm CMOS containing two versions of a continuous-time delta-sigma ADC using the two ring amplifiers presented. The ADCs consist of a 4th-order loop filter with optimized zeros, a single-bit quantizer that operates at a sampling frequency of 320 MHz and a DAC. The best design proposed achieves a measured peak SNDR of 50.6 dB for an 8 MHz bandwidth, a DR of 53.2 dB and consumes 152 μ W at a supply of 1.1 V. The obtained figure of merit is 34.3 fJ/conv.-step which outperforms state-of-the-art delta-sigma ADCs in that specification range and is 77% superior to its traditional OTA-based ADC counterpart.

Index Terms—Analog to Digital Converter, Continuous-Time, Delta-Sigma, Oversampled, Ring Amplifiers.

I. INTRODUCTION

An amplifier is a fundamental signal processing block that is typically implemented as an operational transconductance amplifier (OTA). However, the decreasing supply voltage and transistor output impedance due to process scaling makes it difficult to design high-gain, power efficient and stable OTAs. Furthermore, the supply voltage scales faster than the threshold voltage (V_t) which limits the output swing. These challenges constrain the performance of OTAs, and thereby degrade the overall performance of the systems that contain them. There are two approaches to overcome the performance limitations of OTAs in advanced process technologies. The first one is to improve the OTA performance with gain, gain-bandwidth and output swing enhancement techniques. The second approach is to use scalable amplification structures such as ring amplifiers (RA) [1], which are used in discrete-time (DT) systems.

An RA is an amplifier derived from a ring oscillator and its basic structure can be seen in Fig.1. It consists of three inverter stages and an embedded offset or dead-zone (V_{DZ}) that creates two operating regions. For input voltages (V_{in}) within the input-referred value of the dead-zone, the embedded offset reduces the gate-source voltage (V_{gs}) of the transistors of the last inverter stage, M_{3p} and M_{3n} , below their V_t . In this region, the output current (I_{out}) supplied by the last inverter stage is low due to the sub-threshold operation. Alternatively, when V_{in} is outside the input-referred value of the dead-zone, either M_{3p} or M_{3n} shifts from sub-threshold to active region boosting the output current I_{out} .

The RA is an attractive DT alternative to OTAs since it has high gain, rail-to-rail output swing, efficient slew-based charging capabilities, and it scales with process technology [1]. However, due to the non-linear nature and several operating regions of the RA, traditional small-signal analysis is not sufficient to characterize its behaviour and stability. For instance, the small-signal stability criterion of positive phase margin (PM) is a necessary but not sufficient condition to guarantee stability, i.e. in a feedback configuration, an RA can still oscillate even with a positive PM in the dead-zone. To ensure transient stability, the RA and feedback should be designed such that input overshoots attenuate in each successive oscillation [2].

RAs are used in DT systems such as switched-capacitor structures [2], [3], where they operate in two phases: reset and amplification. In these systems, the RA is reset periodically and its output is only used after it has stabilized within the dead-zone. Therefore, the non-linear behaviour of the RA minimally degrades the performance of the DT system. Furthermore, during the reset phase, the systematic offset of the RA can be cancelled and stabilization techniques can be applied [2]. This enables DT systems to utilize the advantages and scalability of RAs while still achieving stable high-performing systems.

In the last years, there has been a lot of research on DT RAs. In [2], a dynamic dead-zone implemented with a resistor was presented, which was used in [4] to create a fully differential RA. In [5], a second-stage bias-enhanced RA showed improved performance, and in [6], the bias-enhancing technique was used in conjunction with a degenerated dead-zone to improve the linearity and bandwidth of the RA.

Fig. 1. Ring amplifier basic structure, consisting of three inverter stages and an embedded offset or dead-zone (V_{DZ}).

Fig. 2. Schematic of the first continuous-time pseudo-differential ring amplifier topology presented, CTP-RA1, in an integrator configuration.

The RA has been considered unsuitable for continuous-time (CT) operation, since its non-linear behaviour compromises the system stability and performance when it can not be reset periodically and its output needs to be available continuously. As a result, CT systems have not been able to benefit from the scalability and advantages of the RA. There has only been simulation-based work on CT operation of RAs [7].

This paper presents two continuous-time pseudo-differential ring amplifiers (CTP-RA), CTP-RA1 and CTP-RA2. The designs use two different stabilization techniques to allow them to operate in CT without requiring a periodic reset. As a result, the structures proposed enable the use of RAs in a wider range of applications. The designs scale with process technology and maintain the inherent advantages of RAs achieving an efficient amplification structure. As a proof of concept, the two designs are used to implement two versions of a continuous-time delta-sigma (CTDS) ADC in a 65 nm process.

II. CONTINUOUS-TIME RING AMPLIFIERS

In this section, the design of the CTP-RAs is presented. Due to the non-linear nature of RAs, their stability depends on the feedback, hence, a specific configuration has to be defined. In this work, the CTP-RAs are used in a CTDS ADC, hence, they are configured as the first integrator of the loop filter, which is the integrator with the highest performance requirements.

A. CTP-RA1: Load Stabilization

The structure of CTP-RA1 is shown in Fig. 2. It consists of two single-ended CT RAs and a CT common-mode feedback (CMFB). The single-ended CT RAs contain three inverter stages, and the offset is embedded at the input of the third stage using a resistor ($R_{split} = 28 \text{ k}\Omega$) as suggested in [2]. The last stage is implemented using high V_t transistors to achieve higher output impedance and to increase the robustness to process, voltage and temperature (PVT) variations [2]. Furthermore, using high V_t transistors, the dead-zone can be implemented with less current in the second inverter stage and a smaller R_{split} . In this design, a 100 fF capacitive stabilization load (C_{SL}) is added at the output (V_{out}) to achieve stability in CT operation. Firstly, it creates a dominant pole at V_{out} that improves the phase margin (PM) and leads

Fig. 3. Schematic of the second continuous-time pseudo-differential ring amplifier topology presented, CTP-RA2, in an integrator configuration.

to small-signal stability. Secondly, it limits the slew rate (SR) at V_{out} to ensure that voltage overshoots at V_{in} decrease in each successive oscillation.

CTP-RA1 is designed to be used in a CTDS ADC, which has low CMFB requirements compared to other circuits. Hence, a passive CMFB consisting of four resistors (R_{CM}) is used for simplicity. A value of 200 k Ω for R_{CM} is chosen as a compromise between size and performance. Due to its scalability, the design can operate at a supply voltage (V_{DD}) of 1.1 V which is lower than the 1.2 V typical supply of the process. The design used in the integrator configuration shown in Fig. 2, with $R_{in} = 80 \text{ k}\Omega$, $R_L = 250 \text{ k}\Omega$ and $C_{int} = 100 \text{ fF}$, consumes 50.9 μW at the reduced V_{DD} of 1.1 V.

B. CTP-RA2: Current Starving Stabilization

The structure of CTP-RA2 is shown in Fig. 3. It also consists of two single-ended CT RAs and the same resistor-based CMFB. Similarly to CTP-RA1, the single-ended RAs have three inverter stages, an offset embedded with an R_{split} of 28 k Ω and high V_t transistors in the third stage. However, the stabilization method used is different. In this design, stability is achieved by current starving the first and second inverter stages. The currents are trimmable to compensate for process variations. Reducing the current of the first two

Fig. 4. Transient response across variations of CTP-RA1 and CTP-RA2 in an integrator configuration for a full-scale square differential input signal.

Fig. 5. Structure of the 4th-order single-bit continuous-time delta-sigma ADC implemented.

stages decreases the transconductance of M_{1p} , M_{1n} , M_{2p} and M_{2n} , which improves the PM to obtain small signal stability. Furthermore, it also decreases the gain and limits the SR of the first and second inverter stages which is the method through which transient stability is achieved. The design used in the integrator configuration shown in Fig. 3, with the previous values of R_{in} , R_L and C_{int} , consumes $27.4 \mu\text{W}$ at the reduced 1.1 V supply. CTP-RA2 consumes less power than CTP-RA1, however, it requires more transistors stacked and, hence, scales worse with process technology.

Transient response across variations of CTP-RA1 and CTP-RA2 used as integrators for a full-scale square differential input signal is seen in Fig. 4. When the input changes, the RAs leave the dead-zone and start oscillating with a decreasingly smaller amplitude until they lock into the dead-zone again. The integrating error has to be designed to not degrade the ADC performance, as is the case for any CTDS ADC.

III. ADC PROTOTYPE

As a proof of concept, CTP-RA1 and CTP-RA2 are used to implement two versions of a CTDS ADC in a 65 nm process, ADC-RA1 and ADC-RA2. A third version of the ADC is implemented using OTAs, ADC-OTA, to accurately assess the performance of the proposed RAs compared to their traditional alternative. The ADCs are specified for a 64-channel beamforming ultrasonic probe with an 8 MHz bandwidth (BW), a 320 MHz sampling frequency (fs), 1-bit output and a minimum required peak signal-to-noise and distortion ratio (SNDR) of 48 dB. A 1-bit CTDS ADC was chosen to simplify the implementation of the fine digital delay required to align the signals of the 64 channels. The CTDS ADC structure implemented for these specifications is shown in Fig. 5. It consists of a 4th-order loop filter with a cascade-of-resonators feedback structure and a single-bit quantizer. Active RC integrators used in the loop filter have a 3-bit trimmable capacitor array with a nominal value of 100 fF to increase the robustness of the ADC to PVT variations. The single-bit quantizer consists of a clocked comparator, a clocked latch and a pulse generator that creates the clock signals. Two one-bit digital-to-analog converters (DACs) provide the voltage feedback signals for the loop filter. The ADCs have identical quantizer and DACs, however, the four integrators have been implemented using CTP-RA1, CTP-RA2 and a

traditional symmetrical OTA respectively. The schematic of the symmetrical OTA is not shown in this work since it is not novel. Due to the scalability of the presented CTP-RAs, the ADCs can operate at a supply of 1.1 V, which is lower than the typical 1.2 V or the process. The simulated maximum stable amplitude (MSA) of the designs is -6 dBFS.

The signal-to-quantization noise ratio was designed 9 dB higher than the target SNDR of 48 dB, allowing for a maximum input referred thermal noise and distortion of $2.09 \mu\text{V}^2$. The noise and distortion of the ADCs is dominated by the first integrators, due to the noise shaping nature of CTDS ADCs.

ADC-RA1 and ADC-RA2 were simulated with extracted parasitics and transient noise achieving an SNDR of 52.9 dB and 53.1 dB for a -6 dBFS input, respectively. The simulations showed full functionality across PVT variations.

IV. MEASUREMENTS

The prototype die containing the ADCs was fabricated in a 65 nm CMOS process. Ten dies were packaged and measured successfully verifying their functionality, and the results of the median die are presented. The measured SNDR versus the input amplitude in dBFS for the ADCs can be seen in Fig. 6, showing a measured dynamic range (DR) of 54.1 dB and 53.2 dB respectively. The measured differential output spectra of ADC-RA1, ADC-RA2 for a 1 MHz differential input at -6 dBFS is shown in Fig. 7, 8, achieving 51.8 dB and 50.6 dB peak SNDR for an 8 MHz BW. The designs

Fig. 6. SNDR versus differential input amplitude for 1 MHz input frequency.

Fig. 7. Measured differential output spectra for a 1 MHz, -6 dBFS differential input of ADC-RA1. Hanning window and 2^{16} samples used.

Fig. 8. Measured differential output spectra for a 1 MHz, -6 dBFS differential input of ADC-RA2. Hanning window and 2^{16} samples used.

consume 259 μW and 152 μW , respectively, including all the circuitry. A die micrograph can be seen in Fig. 9.

V. RESULTS AND DISCUSSION

The performance of the presented CTDS ADCs is compared to state-of-the-art delta-sigma ADCs in the same specification range in Table I. The best design proposed, ADC-RA2, consumes 152 μW at a 1.1 V supply, achieving a DR of 53.2 dB and a peak SNDR of 50.6 dB for a BW of 8 MHz. The obtained Walden figure of merit (FoM) is 34.3 fJ/conv.-step, which outperforms the state-of-the-art delta-sigma ADCs for that specification range. The ADCs are also contrasted to their OTA-based ADC counterpart, ADC-OTA, in Table I. The designs are in the same die and measured using the exact same setup, hence, the comparison is as accurate as possible. The best design proposed, ADC-RA2, consumes 70% less power and achieves a 77% better FoM than ADC-OTA.

This work presents two continuous-time RAs, CTP-RA1 and CTP-RA2, as an efficient alternative to traditional amplification structures that scale with process technology. CTP-RA2 consumes less power than CTP-RA1 leading to a superior ADC FoM, however, it requires bias adjustments across variations. Despite their several operating regions and non-linear behaviour, they show to be suitable for low-to-mid resolution CTDS ADCs, obtaining state-of-the-art FoM.

Fig. 9. Die micrograph. Only the pad openings of test structures and a dummy ADC-RA2 for the micrograph are not covered by metal-filling.

TABLE I
DELTA SIGMA ADC COMPARISON TABLE

ADC	-RA1	-RA2	-OTA ^a	[3]	[7] ^b	[8]	[9]	[10]
Tech. [nm]	65	65	65	65	65	40	55	28
Year	2018	2018	2018	2016	2018	2012	2015	2015
V_{DD} [V]	1.1	1.1	1.2	1.2	0.9	-	1.2/1.8	1.8/0.9
BW [MHz]	8.0	8.0	8.0	1.0	1.0	10	2.2	5.0
f_s [MHz]	320	320	320	102.4	104	300	140	432
SNDR [dB]	51.8	50.6	48.4	62.0	61.7	70.0	90.4	80.5
DR [dB]	54.1	53.2	54.3	63.0	-	70.6	92.0	83.9
P [μW]	259	152	508	1000	490	2570	4500	3160
Area [mm^2]	0.016	0.015	0.017	0.025	-	0.051	0.090	0.066
^c FoM _S	159.0	160.4	156.3	153.0	-	166.5	178.9	175.9
^d FoM _W	50.9	34.3	148	483	247	50.0	37.8	36.4

^aTraditional OTA-based ADC implementation for comparison.

^bSimulation results.

^cFoM_S = $DR + 10 \cdot \log(BW/P)$ [dB]

^dFoM_W = $P/2 \cdot BW \cdot 2^{(SNDR-1.76 \text{ dB})/6.02 \text{ dB}}$ [fJ/conv.-step]

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