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Fractional Charging Converter with High Efficiency and Low Cost for Electrochemical Energy Storage Devices

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Abstract—High efficiency and low cost power converters for interfacing energy storage have become critical in renewable energy systems. In this paper a fractional charging converter (FCC) is proposed to reduce power rating as well as cost of the dc-dc converter for hydrogen production by alkaline electrolyzer cells. The FCC configuration only processes the partial power resulting from the voltage difference between the source and the energy storage element. Moreover, the converter employed in such configuration can be either isolated or non-isolated, which simplifies topology selection. An analysis and comparison of two dc-dc topologies using a high-frequency transformer based on component stress factor (CSF) is performed to determine the optimal solution for the evaluated application. Based on the results of the CSF analysis, and due to its capability of handling wide input voltage, the isolated full-bridge boost (IFBB) converter is designed, built and tested. Experimental results prove the feasibility of the fractional charging configuration with a reduction of 80% of the power rating compared to the traditional interconnection, which implies a reduction in cost, weight and an increase in efficiency. The converter's maximum voltage gain achieved is 25 and the highest measured system efficiency is 98.2 %.

Keywords—energy storage, converter, fractional, electrolysis.

I. INTRODUCTION

Electrochemical energy storage is an emerging technology, which can provide high flexibility in terms of energy density and power capacity [1]-[2]. Power-to-X (P2X) is a promising option for storing intermittent sustainable renewables and providing clean energy to residential, industrial, transportation users, etc. For example, alkaline water electrolysis (H₂, Al and Cl) have a global capacity >100 GW and its demand is growing fast in recent years [3]-[5]. The advantages of hydrogen is that it can be produced locally, and it offers high energy density, long-term scalable storage and low environmental impact. However, the cost of the initial investment is high and there are safety considerations. Thus, in order to make electrolysis units practical and economic in renewable energy systems, a complete system powered by renewables, including the renewable power source, electrolyzer, and interfacing power electronic devices, must be effectively integrated and optimized to improve system efficiency as well as reduce cost [6].

The conventional way of interconnecting energy storage systems (ESS) to a dc bus is shown in Fig. 1 (a), where a positive and a negative terminal of a bidirectional dc-dc converter are connected to the ESS, while the other positive and negative terminals of the dc-dc converter connected to a regulated dc bus [7]. With the conventional power conversion system, the dc-dc

Fig. 1: Block diagram of dc power conversion system for energy storage systems (ESS). (a) Traditional parallel connection and (b) proposed fractional charging converter (FCC) configuration.

converter must be rated, at least, at the maximum operating power of the ESS. Therefore, efficiency improvement and cost reduction are very challenging to achieve for full power bidirectional dc-dc converters, in particular for electrolyzer or fuel cells with wide input voltage range and high current.

Therefore, fractional or partial power processing technologies were proposed to reduce power rating of power electronic devices and systems in different applications. For instance, in wind generation, the power converters used in doubly fed induction generators (DFIG) are typical 30% of the generator rated power. This reduces the cost as well as power losses in power electronics [8]. In spacecraft powered by photovoltaics, the idea of the series connection of source and load originated in [9]. The proposed configuration, called series connected boost unit (SCBU), showed numerous advantages compared to the traditional interconnection. High efficiency and high power density can be achieved because the dc-dc converter only processes a fraction of the total power of the system, which results in small, lightweight and low cost power supplies, which

in space implementations are extremely important. Depending on the requirements of the application, the series connection of source and load can be performed at the input (input-series-output-parallel ISOP) or at the output of the dc-dc converter (input-parallel-output-series IPOS) [10]. For PV systems, [11] discussed and summarized the various topologies incl. both isolated and non-isolated converters, which can achieved partial power regulation. Reference [12] reviewed the differential power conversion techniques and pointed out that cost reduction and reliability improvement is still challenging. As an example, in [13], a dual active bridge (DAB) converter based universal dc-dc optimizer was proposed by stacking PV strings and batteries, however, without power efficiency reported. Besides PV applications, in [14] and [15], Flyback and DAB converters are used to achieve partial power processing in the applications of wearable devices and fast battery charging, respectively. Nevertheless, due to stacking connection between input and output, isolated topologies must be adopted for such systems in [9], [10] and [13]-[15]. On the other hand, in [16], a 6.7 kW dc-dc converter has been implemented which aims to be able to regulate 27 kW solid oxide electrolysis cells (SOEC) and can achieve a peak system power efficiency of 98.9%. In [17], GaN-based converter with a peak equivalent efficiency of 99.63% was reported. However, an auxiliary load or source is needed in both [16] and [17] to absorb the circulated power.

In this paper, a directly coupled configuration as shown in Fig. 1 (b), so-called fractional charging converter (FCC) is proposed. The ESS is connected between the positive terminals of the dc-dc converter and dc-bus, and its operation principles have been briefly described in [18]. The input voltage of the dc-dc converter V_{in} is set by the differential voltage between the dc bus and the energy storage system ($V_{bus} - V_{ESS}$). Hence, the dc-dc converter only processes the differential power between the dc bus and the ESS. The smaller the voltage difference, the lower the power that needs to be processed. Moreover, due to the common ground connection, either isolated or non-isolated dc-dc converters can be applied. Based on the theoretical analysis of component stress factor (CSF), an isolated boost converter, which can deal with wide input voltage, is designed and system test is carried out with alkaline electrolyzer cells. The converter achieves the maximum voltage gain of 25 and the highest measured system power efficiency of 98.2 %.

This paper is organized as follows. After this introduction, an energy storage system based on alkaline electrolyzer cells (EC) as well as its power converter specifications is introduced in Section II; in Section III CSF compares DAB and isolated full-bridge boost (IFBB) converters; then, the IFBB converter design is presented in Section IV and the experimental results are given in Section V. Finally, Section VI gives a conclusion.

II. SYSTEM ANALYSIS

The system being analyzed is an ESS based on alkaline electrolyzer cells (EC); nevertheless, the system configuration can be applied to battery charge systems as well. Fig. 2 shows the electrolyzer stack voltage as a function of the current and Table I presents the specifications of the system in the FCC configuration.

Fig. 2. Electrolyzer stack voltage (V_{ESS}) as a function of the current (I_{ESS}).

Fig. 3. FCC dc-dc converter input voltage (V_{in}) as a function of the ESS power (P_{ESS}) for different output voltages.

Fig. 4. FCC dc-dc converter input power as a function of the ESS power (P_{ESS}) for different output voltages.

TABLE I
SYSTEM SPECIFICATIONS

V_{bus}	50 ~ 58 V
V_{ESS}	35 ~ 48 V
I_{ESS}	1 ~ 72 A
$V_{in} = V_{bus} - V_{ESS}$	2 ~ 23 V
Maximum electrolyzer power, P_{ESS}	3456 W
Maximum dc converter power, P_{dc-dc}	733 W

Fig. 5. DAB converter and its typical waveforms, top and bottom, respectively.

Fig. 6. IFBB converter and its typical waveforms, top and bottom, respectively.

As shown in Table I, such an arrangement results in the maximum input power processed by the converter to be $P_{dc-dc} = 733$ W. Compared to the traditional parallel connection, where the converter would have been rated at the maximum ESS power of $P_{ESS} = 3456$ W. Therefore, a reduction of nearly 80% of the required power of the dc-dc converter is achieved, which considerably reduces the cost and weight of the dc-dc converter, as well as increasing the power density and efficiency of the system. For the fractional charging configuration the converter input voltage is defined as $V_{in} = V_{bus} - V_{ESS}$, and the converter output voltage is defined as V_o . Fig. 3 and Fig. 4 show the input voltage and input power of the dc-dc converter in FCC configuration, respectively, as a function of the power of the ESS, for different values of the output voltage. As it can be observed, the FCC configuration has the disadvantage of a large variation of the converter input voltage, which requires the selected topology to operate efficiently within a wide input to output voltage range. It is important to notice that the point at which the converter power is maximum, will not correspond with the maximum power of the ESS, as the characteristic electrolyzer stack curve will make the voltage at the input of the converter decrease as the power increases. It is also important to observe that the system needs to be designed so the amount of power processed by the converter tends to zero, thus, reducing

the losses inserted in the system. Therefore, maximizing the efficiency of the direct power flow, which corresponds to the path to charge the ESS, will minimize the power processed by the dc-dc converter and maximize the efficiency of the system.

III. COMPARING DAB AND IFBB CONVERTER BY COMPONENT STRESS FACTOR

The topology selection is a key factor in achieving high efficiency, since it will determine the performance of the overall system. From the system specifications, it can be observed that the power stage presents a large input/output voltage variation. The challenge is to select a topology that can provide high power conversion efficiency over the whole operating range.

An analysis and review of high efficiency bidirectional dc-dc converters with high voltage gain is performed [19]. Based on the analysis and the system specifications, the topology selection is narrowed down to two candidate topologies: dual active bridge (DAB) and isolated full bridge boost (IFBB) converter. The selection is performed based on complexity in terms of number of active switches, passive components and control. These components will affect the efficiency, cost and reliability of the entire system. Both DAB and IFBB topologies have been proved to achieve high efficiency, with a reduced component number (low complexity). Fig. 5 and Fig. 6 show the

schematic of the DAB and IFBB topologies and their operating waveforms, respectively. As it can be observed, both converters present the same number of active switches and passive components. In the DAB, the power is delivered to the output through an ac inductor, whose charge and discharge is controlled with the phase-shift angle of the half bridge switching legs. In the IFBB converter, the control parameter is the duty cycle of the primary switches and the input inductor is the component that transfers the energy to the output port.

The analysis of the DAB and IFBB topologies is performed based on component stress factor (CSF) [20]. CSF is a derivation of the component load factors approach (CLF) [21]. CLF is a numerical method, which is calculated based on the components voltage and current stress and normalized to the processed power (volt-amp/watt figure), which makes the calculation dimensionless.

The approach of the CSF analysis is based on the assumption that the evaluated topologies have the same amount of resources: silicon for semiconductors, magnetic material and copper for windings and capacitor volume for energy storage/filter components. A weighing factor is applied to distribute the resources within the topology. The result of the CSF analysis provides an effective way to evaluate the losses in the individual components of the circuit, and consequently, an estimation of the converter performance. Therefore, the analysis gives a quantitative measure to compare the performance of different topologies for a specific application [22].

The CSF method adopts two assumptions in order to simplify the calculations, i.e., the power losses in the converter are neglected (efficiency 100%) and the inductors are large enough to have no ripple current (square waveform).

The stress factor is calculated independently for each component: semiconductors (SCSF), windings (WCSF) and capacitors (CCSF), as shown in (1), (2), (3), respectively. The CSF is related to the power dissipated in the component. In the semiconductors, the conduction losses are calculated with the squared root mean square (*rms*) current through the device multiplied by the channel on-resistance of the switch. For a given die size, the channel on-resistance is proportional to the voltage rating to the power of 2.5, higher voltage rating will result in a longer channel with smaller cross section. Taking the rated voltage squared gives a good approximation to relate the maximum voltage and the channel on-resistance. Therefore, SCSF is calculated with the breakdown voltage squared, times the *rms* current squared, and normalized to the square of the processed power, to provide a dimensionless quantity.

Regarding the calculation of the stress factor of magnetic components, to perform a fair comparison, each topology should have the same amount of copper volume, and hence, the same winding area. The windings losses in magnetic components are calculated with the *rms* current squared, times the winding resistance. The winding resistance is related to the number of turns and the cross-sectional area of the copper. The voltage applied to the windings is proportional to the number of turns. Therefore, the resistance will increase with the square of the number of turns, which is proportional to the voltage squared. The WCSF is then computed as the maximum voltage applied to the windings squared, multiplied by the *rms* current squared (2).

The maximum voltage applied to the winding is calculated as the average voltage applied to the winding over a period, as shown in (4).

The stress factor of capacitors is determined by the resistive losses due to the equivalent series resistance (ESR). The ESR is related to the capacitor volume, and the volume is proportional to the energy storage capacity, thus, the CCSF is calculated with the squared maximum voltage and the *rms* current as presented in (3).

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^2 \cdot I_{rms}^2}{P_{in}^2} \quad (1)$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max_avg}^2 \cdot I_{rms}^2}{P_{in}^2} \quad (2)$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^2 \cdot I_{rms}^2}{P_{in}^2} \quad (3)$$

$$V_{\max_avg} = \sum_i D_i \cdot |V_i| \quad (4)$$

The distribution of the resources is implemented by the term $\sum_j W_j / W_i$, which represents the weighting factor for component *i*, where $\sum_j W_j$ is the sum of the individual weights

of all components of the same type and W_i is the weight assigned to the component *i*. In the first iteration, the resources are distributed equally. Based on the results, the weight distribution can be adjusted. As a result, the component with higher CSF can be assigned with a larger amount of the resource in order to reduce the stress factor.

Once the stress factor for each component is calculated, the total CSF is computed as the sum of component stress factors of the same type as in shown in (5).

$$\begin{cases} SCSF = \sum_i SCSF_i \\ WCSF = \sum_i WCSF_i \\ CCSF = \sum_i CCSF_i \end{cases} \quad (5)$$

From the procedure of the CSF calculation, we can observe that the analysis accounts for the conduction losses in switches, magnetic components and capacitors. However, it does not consider the switching losses in the semiconductors and the magnetic core losses. From the system specifications presented in Table I, the application under analysis is a low voltage, high current application; therefore, the conduction losses in the semiconductors will dominate over the switching losses. Regarding the magnetic components, the core losses are a function of the magnetic material, the volts-seconds, the peak-to-peak ac flux density and the switching frequency. As discussed before, the system is characterized by a low input voltage to the dc-dc converter, and the switching frequency is limited to 50 kHz. Therefore, the CSF approach is considered a valid method to compare the topologies for the application under analysis.

Fig. 7. CSF analysis. (a) DAB's SCSF, (b) DAB's WCSF, (c) DAB's CCSF, (d) IFBB's SCSF, (e) IFBB's WCSF and (f) IFBB's CCSF.

Fig. 7 (a) to (f) shows the results of the CSF analysis for the DAB and the IFBB topologies for semiconductors (SCSF), windings (WCSF) and capacitors (CCSF), respectively. The graphs show the stress factor values as a function of the power of the ESS for different values of the output voltage. The CSFs are normalized to the maximum stress value, which occurs in the DAB topology. At low power levels the DAB converter presents very high CSF in semiconductors, winding and capacitors compared to the IFBB topology. This is because the DAB topology presents a large *rms* circulating reactive current. At low

power levels, the *rms* current is very large compared to the processed power, which results in large CSF values. As the power of the electrolyzer stack increases, the ratio of the *rms* current to the processed power is reduced and thus, the CSF. In the IFBB converter, the highest CSF occurs at the maximum ESS power level (maximum ESS current) and minimum output voltage. As we can observe from the SCSF, the DAB presents a minimum value for the different output voltages, which corresponds to the point where the converter reactive current is minimized. The IFBB presents higher stress as the input to

output voltage transformation ratio is increased, which is an expected result from boost-derived topologies. The DAB therefore, shows a reduced SCSF compare to the IFBB, but only in a small range of the operating region. However, the WCSF for the DAB is significantly worse than that of the IFBB in all the operating range due to the increased voltage stress in the magnetic components and the alternating current nature in the resonant inductor. Based on the results of the CSF analysis, the IFBB converter is the selected topology to implement the energy storage system in FCC configuration.

IV. IFBB CONVERTER DESIGN

A 750W prototype of the IFBB converter is designed, constructed and tested in order to verify the theoretical analysis and test the FCC configuration.

A. Magnetic components

Due to the practical height constraint in the electrical power supply unit for the stack of electrolyzer cells, planar magnetic design for the inductor and the transformer is adopted. Planar magnetics offers low profile structure with high surface area and good thermal characteristics. Moreover, it helps implementing interleaving techniques to achieve low leakage inductance and ac resistance. However, in terms of loss, selecting PCB winding or wire-wound winding highly depends on required specifications as discussed in [23].

The IFBB inductor is designed for inductance of $L = 2.4 \mu\text{H}$, with the maximum current ripple of $\Delta i = 25 \text{ A}$ under the worst condition (maximum volt-sec). Three different core sizes and number of turns are compared as shown in Table II. From Table II, it can be observed that, for the same number of windings (3 turns), the loss efficiency ($P_{\text{loss}}/P_{\text{dc-dc}}$) difference of the inductors with cores ELP43/10/28 and ELP58/11/38 is only 0.1%. ELP43/10/28 (volume = 11500 mm³) has almost half of the volume of ELP58/11/38 (volume = 20800 mm³), which gives higher power density and lower price, therefore, this core is finally selected. The inductor is manufactured in a six layers PCB with 210 μm (6 oz.) copper thickness. Two PCBs are stack in parallel in order to reduce the dc resistance.

The transformer is manufactured in an eight layers PCB with 210 μm (6 oz.) copper thickness with the turns-ratio of 1:2. The primary winding (Prim) is formed by two turns in parallel, which are fully interleaved with four turns of the secondary winding, in a structure as shown in Fig. 8. Full interleaving winding technique is implemented in order to reduce the transformer leakage inductance, in this case $M=8$ in (6). Achieving a low leakage inductance is critical in full bridge boost configurations without any clamp circuit, because the energy stored in the leakage inductance will cause an overshoot in the primary MOSFETs. The measured transformer leakage inductance is $L_{lk} = 19.4 \text{ nH}$. Full interleaving technique can also help reducing the ac resistance, as the magneto motive force (MMF) is always equal to one i.e. $m = 1$ in (7).

$$L_{lk} \approx \mu_0 \frac{l_w h_w N^2}{3b_w M^2} \quad (6)$$

where μ_0 represents permeability of free space, l_w is mean turn length, b_w is breadth of winding, M is number of primary-

TABLE II
INDUCTOR DESIGN

Core	Winding	Current ripple	Loss
ELP38/8/25	2 turns	$\Delta i = 44.0 \text{ A}$	3.4 W
	3 turns	$\Delta i = 26.6 \text{ A}$	4.3 W
ELP43/10/28	2 turns	$\Delta i = 36.0 \text{ A}$	3.3 W
	3 turns	$\Delta i = 22.3 \text{ A}$	4.1 W
ELP58/11/38	2 turns	$\Delta i = 25.2 \text{ A}$	2.9 W
	3 turns	$\Delta i = 15.8 \text{ A}$	3.6 W

Fig. 8. Transformer winding structure.

secondary intersections and N is number of winding turns.

$$\frac{R_{ac}}{R_{dc}} = \varphi \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} + \frac{2(2m^2 - 1)}{3} \varphi \frac{\sinh(\varphi) + \sin(\varphi)}{\cosh(\varphi) - \cos(\varphi)} \quad (7)$$

where $\varphi = h/\delta$, and h and δ are height of conductor and penetration depth in material.

B. Converter prototype

Besides the magnetic components, the converter is designed with a 4-layer PCB and a special attention is paid to minimize the ac current loops i.e. the source and return paths are on top of each other. Due to the high current application, 140 μm (4 oz) PCB copper thickness is used in order to minimize the resistive losses [24]. The main converter components are listed in Table III. The design is based on Silicon (Si) MOSFETs with low R_{DS} on-resistance in order to reduce the conduction losses. DirectFET technology from Infineon is selected, which provides low package inductance and maximized thermal transfer due to copper drain clip. The high rms current on the IFBB primary side, which is around $I_{rms_prim_MOS} = 40 \text{ A}$, will cause high conduction losses, therefore, primary MOSFETs with very low on-resistance are selected, $R_{DS} = 0.34 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$. The maximum rms current on the secondary side is $I_{rms_sec_MOS} = 15 \text{ A}$, which allows to select devices with higher on-resistance than in the primary side. The converter switching frequency is $f_{sw} = 50 \text{ kHz}$, to limit the switching losses.

The control law is implemented in a digital signal processor (DSP) TMS320F2808 from Texas Instruments. The reading of the inductor current is performed with a high precision Hall-Effect current sensor, which inserts an extremely low resistance of $R_{sens} = 0.1 \text{ m}\Omega$. Fig. 9 shows the experimental prototype of the IFBB converter. The primary and secondary MOSFETs are placed on the bottom side of the PCB, in order to transfer the heat to the heat sink through an isolated gap pad material with a thermal conductivity of 4.0 W/mK.

TABLE III
IFBB CONVERTER COMPONENTS

$M_1 \sim M_4$	IRL7472L1
$M_5 \sim M_8$	AUIRF7759L2
ISO gate drivers	SI8235AB-D-IS1
Transformer	1:2, EILP43/10/28, Ferrite N87
Inductor	2.3 μ H, EILP43/10/28, Ferrite N87
Capacitors C_{in}	20 x 10 μ F 50V X7R
Capacitors C_{out}	20 x 10 μ F 100V X7S
Current sensor	ACS770LCB-100B
Switching frequency	$f_{sw} = 50$ kHz
Digital controller	TMS320F2808 DSP

Fig.9. IFBB converter prototype.

V. EXPERIMENTAL RESULTS

The experimental test is carried out with two steps: the constructed IFBB converter is tested in the laboratory firstly to verify the design validity. Then the IFBB converter is connected with a real 3.5 kW stack of alkaline electrolyzer cells in the manner of the proposed fractional power charging configuration shown in Fig. 1, and therefore the entire system test is accomplished.

A. IFBB converter test

For the experimental test of the IFBB converter, the behavior of the electrolyzer stack is simulated with an electronic load in series with a power resistor. The electronic load is configured as a constant voltage source and will set the starting point of the characteristic V-I curve shown in Fig. 3. The power resistor ($R = 0.185 \Omega$ connected in series, will provide the slope of the V-I curve as the I_{ESS} current increases. Fig. 10 shows the steady state waveforms of the IFBB converter, where v_{GS} is the gate-source voltage of the low-side switch S_4 , i_L is the inductor current, and v_{ab} and i_{trf} represent the transformer voltage and current as denoted in Fig.6. Fig. 10 (a) shows the converter operating at $V_o = 50$ V, $V_{ESS} = 38$ V, $I_{ESS} = 13$ A $V_{in} = 12$ V, $P_{ESS} = 594$ W, $P_{dc-dc} = 156$ W. In this conditions, the duty cycle D is approx. 75%. Fig. 10 (b) shows the IFBB converter waveforms at the system maximum power level i.e. the electrolyzer is charging at the maximum current. The converter operating conditions are $V_o = 50$ V, $V_{ESS} = 48$ V, $I_{ESS} = 72$ A, $V_{in} = 2$ V, $P_{ESS} = 3456$ W, $P_{dc-dc} = 144$ W and the converter's duty cycle is maximum $D = 99\%$.

As it can observed the inductor current ripple reduces as the input voltage of the converter decreases. However, the peak current on the transformer secondary side increases due to the reduced conducting time of the secondary MOSFETs. Fig. 11 shows an enlarged portion of the steady state waveforms when the converter operates at maximum duty cycle (Fig. 10 (b)). As it can be observed, the voltage across the transformer does not clamp, which indicates that there is no avalanche mode operation of the MOSFETs primary side, which proves the low leakage inductance design of the transformer, thus, no snubber components are required. Fig. 12 presents a thermal image of the IFBB converter operating at the worst conditions, which are minimum input voltage and maximum input current, while the system is working at the maximum power level $P_{ESS} = 3456$ W. The thermal image shows a maximum temperature of 98.9°C . As the input voltage decreases, the converter current stress on the secondary side reduces, while it increases on the primary side, therefore, the highest temperature appears at the converter primary side.

(a)

(b)

Fig. 10. IFBB operating waveforms, from top to bottom: primary gate-to-source voltage (10 V/div); voltage across the transformer primary side (20 V/div); transformer secondary side ac current (25 A/div) Rogowski coil (20 mV/A); inductor ac current (20 A/div) Rogowski coil (100 mV/A). Time scale 5 μ s/div.

Fig. 11. Enlarged IFBB operating waveforms from top to bottom: primary gate-to-source voltage (10 V/div); voltage across the transformer primary side (20 V/div); transformer secondary side ac current (25 A/div) Rogowski coil (20 mV/A); inductor current ac (20 A/div) Rogowski coil (100 mV/A). Time scale 200 ns/div.

Fig. 12. Thermal image of the IFBB converter operating at the electrolyzer stack maximum power $P_{ESS} = 3456$ W.

Fig. 13. Block diagram of the integration test.

B. System test

For system test, the tested IFBB converter is inserted into the proposed fractional charging configuration, as shown in Fig. 13.

Fig. 14. System test setup.

The IFBB's primary side is connected in series with the ESS. This series configuration allows for the converter to control the current flow through the ESS, and consequently its power, by controlling the IFBB converter input current. If the input port V_{in} is shorted, i.e. the switches $M_1 \sim M_4$, or M_1 and M_2 , or M_3 and M_4 are always kept ON, the ESS will be directly connected in parallel with the dc bus, V_{bus} . However, if the input port V_{in} is open, i.e. the switches $M_1 \sim M_4$, or M_1 and M_3 , or M_2 and M_4 are always kept OFF, there will be no current flowing through the ESS. Finally, a real 3.5 kW stack of alkaline electrolyzer cells, as the ESS for hydrogen production and the corresponding tests are then carried out. Fig. 14 shows the system test setup, where the dc bus voltage, V_{bus} , the electrolyzer stack, and the dc-dc converter are highlighted. The converter efficiency and the system efficiency have the relationship expressed as (8) and (9).

$$\eta_{dc-dc} = \frac{P_{o\ dc-dc}}{P_{in\ dc-dc}} \cdot 100\% = \frac{P_{o\ dc-dc}}{P_{in\ dc-dc} + P_{loss}} \cdot 100\% \quad (8)$$

$$\eta_{sys} = \frac{P_{EC}}{P_{EC} + P_{loss}} \cdot 100\% \quad (9)$$

As it can be observed in Fig. 15, the highest efficiency of the system occurs at the worst conditions of the dc-dc converter (dc-dc converter input voltage $V_{in} = 2$ V, and electrolyzer current $I_{ESS} = 72$ A). It is because the IFBB converter is processing the lowest amount of power ($P_{dc-dc} = 144$ W) compared to the system output power ($P_{ESS} = 3456$ W). The highest measured system efficiency is $\eta_{sys} = 98.2\%$.

Fig. 16 (a) and (b) show a load step from 0 to 6 A, positive and negative, respectively. These waveforms correspond to the start-stop test of the converter. First, we can see that the electrolyzer current is fully controlled and it presents a critically damped response without overshoot. The settling time is approximately 5 ms for the positive current step, and 2 ms for the negative load step. Second, due to the V-I characteristics of the electrolyzer stack, the system can still operate at no current I_{ESS} , by controlling the corresponding switches $M_1 \sim M_4$ to open the IFBB converter input. Furthermore, from the start-stop test, it can also verify the effective fault protection and the converter can quickly cut off the electrolyzer current.

Fig. 15. Measured system efficiency η_{sys} .

Fig. 16. System test of load step response. (a) positive step and (b) negative step. From top to bottom: converter input voltage (10 V/div); dc-dc converter input voltage V_{in} (5 V/div); electrolyzer stack current I_{ESS} (2 A/div), inductor ac current (20 A/div), Rogowski coil (100 mV/A). Time scale 6.4 ms/div.

VI. CONCLUSION

This paper presents a fractional charging converter (FCC) configuration, which can use a 750 W dc-dc converter to

regulate an approx. 3.5 kW electrolyzer stack to generate hydrogen. The analytical comparison of dc-dc topologies in such proposed configuration was carried out. Selecting the most appropriate topology for a specific application is crucial in achieving high efficiency. Although the two analyzed converters present the same number of active switches and passive components, the CSF analysis shows a big difference of the converters' performance for the given configuration. Based on the analysis, an IFBB converter is designed and tested. Experimental results shows the converter can handle the maximum system power level with a reduction of 80% of the power rating compared to traditional load connection, which achieves a high reduction on the converter size, weight and price. However, due to the series connection, there is no galvanic isolation between the input power supply and electrolyzer stack, which may introduce other issues for some applications and thereby needs investigate in the future research work.

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