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Published in:
IEEE Transactions on Industry Applications

Link to article, DOI:
[10.1109/TIA.2019.2935929](https://doi.org/10.1109/TIA.2019.2935929)

Publication date:
2020

Document Version
Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):
Lin, Q., Cai, F., Wang, W., Chen, S., Zhang, Z., & You, S. (2020). A High Performance Online Uninterruptible Power Supply UPS System Based on Multitask Decomposition. *IEEE Transactions on Industry Applications*, 55(6), 7575 - 7585. <https://doi.org/10.1109/TIA.2019.2935929>

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A High-Performance Online Uninterruptible Power Supply (UPS) System Based on Multi-task Decomposition

Qiongbín Lin, *Member, IEEE*, Fenghuang Cai, Wu Wang, Sixiong Chen, Zhe Zhang, *Senior Member, IEEE*, Shi You, *Member, IEEE*,

Abstract—High quality online uninterruptible power supplies (UPS) are widely used in applications e.g. precision medical equipment with critical loads. This paper proposes a low-cost and high performance online UPS system. Firstly, the performance improvement of a bidirectional switch based bridgeless power factor (PFC) converter, which is regulated by a hybrid control strategy with load current feedforward is studied. Secondly, the proposed closed-loop controller integrates improved predictive current control with predictive voltage control and applies to the second-stage neutral-point-clamped (NPC) three-level inverter for low output voltage harmonics. Moreover, a push-pull dc-dc converter interfaces and boosts voltage of a 24V battery bank as the backup energy source. Considering complexity of the UPS system as well as cost reduction, we implement a multi-task decomposition method for control on a monolithic low-cost digital signal processor (DSP) embedded with Control Law Accelerator (CLA). Finally, the experimental results from a 1kVA a prototype can effectively verify validly of the theoretical analysis and design.

Index Terms—Online UPS, bidirectional switch bridgeless PFC, multi-task decomposition, three-level inverter, digital control, low cost.

I. INTRODUCTION

ONLINE uninterruptible power supplies (UPS) provide stable, reliable and high quality power to critical loads such as communication systems, data centers, medical equipment, etc. [1], [2]. Moreover, UPS has also become an effective solution to improve energy efficiency in smart buildings [3], [4]. Generally, an UPS needs to achieve high

efficiency, high power density and low cost design, and at the same time to ensure power factor correction (PFC), fast fault response and high quality output voltage. Due to the adopted line-frequency transformers, the traditional online UPS system is bulky and expensive. Therefore, using high-frequency transformers (>20 kHz) is able to reduce the volume of online UPS [5], [6], however, in such systems there are more semiconductor switches operating at high switching frequency, which decreases the overall conversion efficiency. Then the soft-switching topologies are the choices to reduce the switch losses [7]. On the other hand, non-isolated online UPS systems have no transformers meaning fewer of high-frequency switches used and therefore can solve the problems in terms of volume and efficiency associated with online UPS [8]-[14].

For efficiency improvement, volume reduction and low number of switches, various non-isolated UPS topologies have been proposed and reported [8]-[14]. A phase locked loop (PLL) based passive power filter was proposed in [8] to reduce harmonic distortion, implement PFC, and improve system efficiency. However, the passive filter is bulky and heavy. To reduce the volume of power filters, the parallel active power filter structure has been used in [9]-[10], but this structure is complicated and costly. The Z-source inverter is adopted in [11], which effectively ensures the quality of output inverter voltage when the battery voltage sags. Nevertheless, this structure increases the overall system volume due to the added Z-source network and battery bank to provide 360V dc voltage. A transformerless online UPS system consisting of a four-leg rectifier, a battery charger/discharger, and an inverter, was studied in [12]; it reduces the size, weight and cost of the system, but the needed battery voltage of 192V is still high and complicates the battery management system. Another transformerless line-interactive UPS with low ground leakage current was reported in [13], but battery bank is high and up to 180V. Thus, in [14], the battery bank voltage of 24V is used. The front-stage is a bridgeless dual Boost PFC converter, which improves efficiency of the rectifier but increases the number of power devices. The inverter is traditional single-phase full-bridge circuit, in which the employed IGBTs have high losses and

Manuscript received January 27, 2019; revised May 14, 2019; accepted July 15, 2019. This work was supported in part by the Technology Innovation Fund Support Project by the company of Kehua Hengsheng under Grant KHHS20170416.

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give high output voltage distortion because of the non-linearity introduced by their saturation voltage.

Besides UPS topologies, control algorithms of an entire UPS system need to be improved and even optimized in terms of both steady state and dynamic performance. Therefore, in order to minimize output voltage distortion in particular under nonlinear load, a multi-loop control architecture was proposed in [15], which can realize low output harmonic with a nonlinear load. In [16], the UPS system adopts two TMS320F2808 digital controllers. Based on the sliding mode function, the system uses the time slope to improve the sliding mode control and reduce output voltage harmonics. Additionally, the repetitive control is able to eliminate effects on periodic signals, and thereby the method of shortening the repetitive control delay to improve inverters' dynamic and static performance has been used in [17]- [18]. In [19]-[20], some modified repetitive control schemes were used to improve the control performance and simplify calculation. There are also other control strategies used in UPS including proportional resonance, improved sinusoidal pulse-width modulation (SPWM), improved passivity-based control method [21], Lyapunov-function-based control strategy [22], SPWM-based D- Σ Digital Control [23], and dc-link voltage protection control method for modular UPS systems [24], etc. However, most of the aforementioned control strategies are implemented for every part of UPS with a serial software architecture. Then using complex control strategy or mathematical calculation in the UPS overall system will impose a high processing burden on the master controlling chip and may cause UPS system instability. In order to overcome such issues, a distributed UPS system using distributed multiprocessor control boards has been discussed in [25], but this method is complicated and costly. On the other hand, the traditional methods use single high performance digital signal processor (DSP) or multi DSPs to implement these complex system control and mathematical logic operations, resulting in a simple structure but high cost.

In order to improve power density and efficiency of an online UPS system, this paper proposes a novel single-phase online UPS topology. The rectifier in this topology is a single-phase bridgeless PFC with bidirectional switches, as shown in Fig. 1. In comparison to traditional diode rectifier bridge PFC, VIENNA rectifier [26] and bridge-less dual Boost PFC [27], it has several advantages such as only one driving circuit needed, less devices, simple control, and high efficiency. The dc-dc converter, interfacing the battery bank and dc bus, adopts push-pull boost circuit and uses 24V battery bank. The single-phase neutral point clamped (NPC) inverter has three-level output voltage, which not only improves output waveform quality but efficiency [28]. In order to implement complex control strategies in a low-cost, low-speed DSP with control law accelerator (CLA), a control method for multi-task decomposition is proposed and therefore the tasks can process in parallel.

This paper is organized as follows. After this introduction,

Section II introduces the proposed topology as well as its operation principles; Section III presents the control method for the whole UPS system; Section IV provides experimental results to verify the theoretical analysis; finally, Section V gives the conclusion.

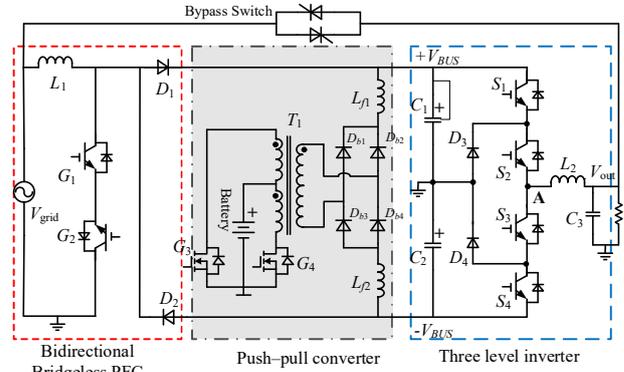


Fig. 1. Circuit diagram of the proposed online UPS system

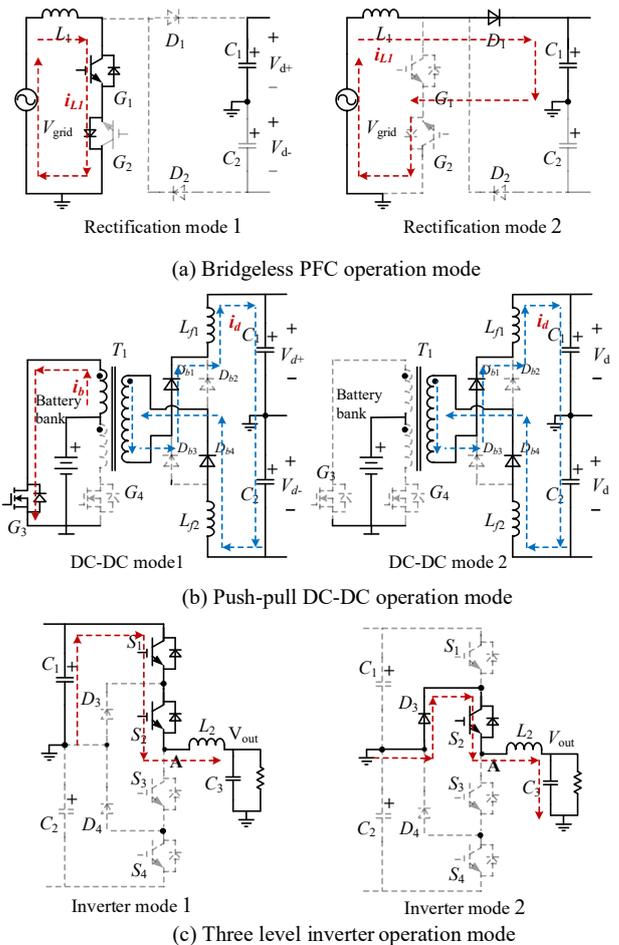


Fig. 2. Operating modes of UPS

II. TOPOLOGY AND ITS OPERATION PRINCIPLES

A. The proposed topology

Fig.1 shows the proposed online UPS topology, which is non-isolated in the grid-connected mode and galvanic isolated in battery mode. Under the grid-connected mode, the bridgeless rectifier with switches G_1 and G_2 achieves power factor correction and at the same time provides a stable dc bus voltage up to $\pm 360V$, and then deliver high quality power to the load through the NPC inverter. When the power grid fails, the battery supports the dc bus voltage through isolated push-pull dc-dc converter. Fig.2 shows the operating modes of the various circuit sections of proposed online UPS system.

B. Bridgeless PFC with bidirectional switch

Assuming that the inductor L_1 operates in continuous conduction mode (CCM), as shown in Fig. 2(a), Rectification Mode 1 and 2 are the operating modes of the circuit during the positive half cycle of the grid. Due to symmetry, the operation principles are the same in the negative half cycle.

Rectification Mode 1: The circuit works in boost inductor charging mode. G_1 conducts high frequency operation with conduction duty cycle of d_{g1} . IGBT G_2 anti-parallel diode conducts. The grid voltage v_g applies to inductor L_1 , and the inductor L_1 starts to charge. The inductor current ripple is calculated by

$$\Delta i_{L1} = \frac{v_g}{L_1} d_{g1} T_1 \quad (1)$$

where T_1 is the switching period of PFC converter.

Rectification Mode 2: The circuit works in boost inductor discharging mode. IGBT G_1 is open and diode D_1 conducts the freewheeling current. The difference between v_g and output dc voltage $V_d = V_{bus}/2$ is inversely applied to inductor L_1 and the current of inductor i_{L1} decreases linearly. Then,

$$\Delta i_{L1} = \frac{V_d - v_g}{L_1} (1 - d_{g1}) T_1 \quad (2)$$

Equalizing (1) and (2) obtains

$$V_d = \frac{v_g}{1 - d_{g1}} \quad (3)$$

In the negative half cycle similarly we get

$$V_d = \frac{v_g}{1 - d_{g2}} \quad (4)$$

where d_{g2} is the duty cycle of IGBT G_2 .

Apparently, the achieved voltage gain is the same as that in the conventional Boost PFC.

C. Isolated push-pull dc-dc converter

When there is a grid power failure and the PFC rectifier stops working, the battery provides dc bus voltage up to $\pm 360V$ through the push-pull dc-dc converter with a high frequency transformer. As illustrated in Fig.2 (b), during dc Mode 1, MOSFET G_3 is on and G_4 is off, and the rectifier diodes D_{b1} and D_{b3} turn on, the output voltage is stable

through L_{f1} , L_{f2} and C_1 and C_2 .

Assuming that the conduction duty cycle of the switch G_3 is d_{g3} , then, $d_{g3} = \frac{T_{on}}{2T_s}$. The battery bank voltage is V_b , the

center tap transformer is vertically symmetrical and the turns ratio is 1. Assuming turns ratio is $N_1:N_2$, Where N_1 is the number of turns in primary winding and N_2 is the number of turns in secondary winding. The output voltage is

$$2V_d = \frac{N_2}{N_1} d_{g3} \cdot V_b \quad (5)$$

D. Single-phase NPC inverter

The most critical part of the online UPS is the inverter that supplies the voltage to the load. The working principle of the NPC inverter is shown in Fig. 2(c). When the inverter is in the positive half cycle, S_1 operates at a high frequency, S_2 turns on, and S_3 , S_4 do not participate in the operation. When the inverter is in the negative half cycle, the action of switches is reversed. Here, only the operation principle in the positive half-cycle is analyzed since the NPC inverter works symmetrically in the negative half-cycle.

Inverter Mode 1: S_1 and S_2 turn on, the inverter energy is provided by the positive bus capacitor C_1 , and the inductor current rises linearly under the combined action of positive bus voltage and output voltage

$$\Delta i_{L2} = \frac{V_d - v_{inv}}{L_2} d_{s1} T_2 \quad (6)$$

where v_{inv} is the inverter output voltage, i_{L2} is the inverter inductor current, and d_{s1} is the duty cycle of the switch S_1 .

Inverter Mode 2: S_1 turns off, S_2 turns on, and the inverter voltage to the load is supplied by the energy store at output filter. The inductor current drops linearly under the action of output voltage

$$\Delta i_{L2} = \frac{v_{inv}}{L_2} (1 - d_{s1}) T_2 \quad (7)$$

The relationship between the duty cycle and the bus voltage and the inverter voltage can be obtained from (6) and (7).

$$v_{inv} = d_{s1} V_d \quad (8)$$

III. SYSTEM CONTROL TECHNOLOGY

A. Multi-task decomposition

According to the relationship between the input-output voltage and the duty ratio, the PWM driving signal required by each controller can be obtained. Prior to this, the DSP needs to be decomposed modularly to make it suitable for collaborative control between the various parts of the online UPS system. The decomposition of each module is shown in Fig.3.

Where the CLA is responsible for the subroutines of the PFC converter and the push-pull converter, and both of the converters have switching frequency of 40 kHz. In addition to executing the 20kHz switching frequency for the NPC

inverter, the main core also needs to capture, sampling and interrupt the procedures, etc. This design is difficult to achieve if the main frequency of single-core microcontroller is only 60MHz. Therefore, this design uses the "pseudo-dual core" task-parallel architecture to achieve the CLA "multiplier" effect. The CLA triggering mechanism of the PFC and dc-dc converter in Fig. 3 is triggered periodically by PWM1 and PWM2, respectively. The grid-connected state and the battery mode in the UPS work independently, so the two subroutines in CLA had no interruption of nesting.

Fig.4 shows the block diagram of specific control strategy of each module. Where the rectified PFC converter is controlled by combining the proportional integral (PI) voltage outer loop and deadbeat mixed conduction mode (MCM) current inner loop. At the same time, the load current feed forward control is added to improve the dynamic and static performance of the PFC. The push-pull dc-dc converter uses traditional voltage and current double loop PI control, so the detailed controller design is no given here. In order to improve the dynamic and static performance of the inverter as well as reduce the waveform distortion with nonlinear load, the current inner loop adopts predictive control based on the voltage PI outer loop to improve the dynamic response speed of the system through the inductor current prediction.

B. PFC control

The outer voltage loop of the bridgeless PFC is realized by PI control, and for the inner current loop, deadbeat control is used. In CCM, we have

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = v_g(n) & (t_n < t < t_n + T_{s1}d_{PFCn}) \\ L_1 \frac{di_{L1}}{dt} = v_g(n) - V_d & (t_n + T_{s1}d_{PFCn} < t < t_{n+1}) \end{cases} \quad (9)$$

where n is the n^{th} switch period of a power frequency cycle and $v_g(n)$ is the corresponding voltage of power grid. T_{s1} and d_{PFC} are the switching period and duty cycle of the PFC converter, respectively.

Given that the grid voltage as a constant value during a single switching cycle, the duty cycle expression of CCM is

$$d_{PFC}[n] = \frac{(i_{L1}[n+1] - i_{L1}[n])L_1}{T_{s1}V_d} + \frac{V_d - v_g[n]}{V_d} = d_i + d_{ccm} \quad (10)$$

where,

$$d_{ccm} = \frac{V_d - v_g[n]}{V_d} \quad (11)$$

$$d_i = \frac{(i_{L1}[n+1] - i_{L1}[n])L_1}{T_{s1}V_d} \quad (12)$$

d_{ccm} is a voltage-dependent steady-state open-loop term, and d_i is a current-dependent sinusoidal correction term. The conventional PI controller controls the duty cycle d_i to make the output sinusoidal.

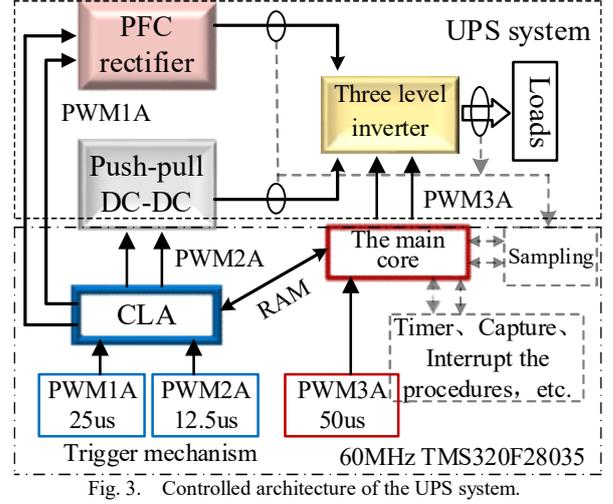


Fig. 3. Controlled architecture of the UPS system.

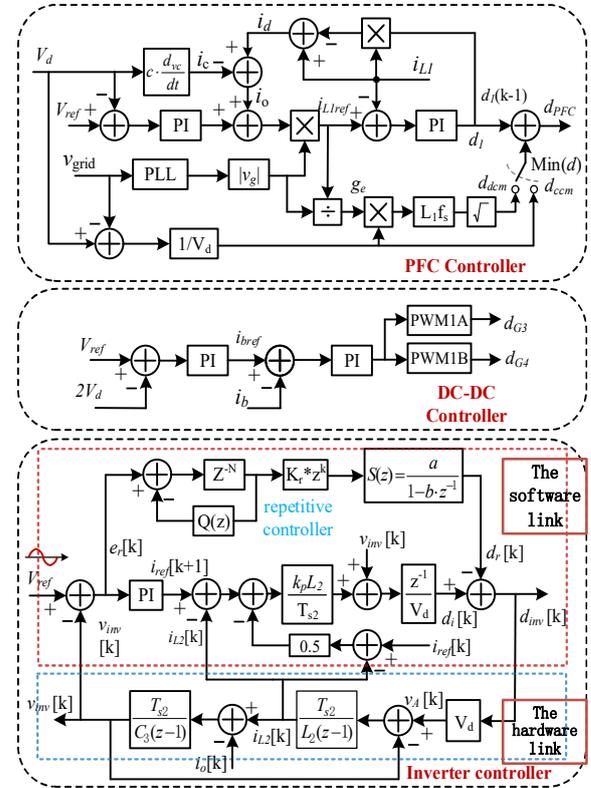


Fig. 4. Control strategy of proposed UPS.

Due to the sinusoidal ac output current, there will be discontinuous current mode (DCM) or the mixed current mode (MCM) i.e. CCM and DCM coexisting, depending on the load. Therefore, continuous current mode operation no longer holds and the traditional control method deteriorates the performance of the prototype. Therefore, further analysis of PFC control under DCM and MCM is required. The duty cycle of the steady-state open-loop term can be obtained as follows

$$d_{dcm} = \sqrt{2L_1 f_{s1} g_e d_{ccm}} \quad (13)$$

where d_{dcm} is the duty ratio of PFC inductor in DCM, d_{ccm} is the duty ratio in CCM, $g_e = \langle i_{L1} \rangle / v_g$, and the input power $P_{in} = g_e * v_g^2$ when the PFC current completely tracks the input voltage. Analyze the steady-state open-loop duty cycle operating in critical mode to select a suitable steady-state open-loop term. Using the CCM steady-state open-loop term d_i in (11) and DCM steady-state open-loop term d_{dcm} in (13), the duty ratio d_{bcm} of the steady-state open-loop term of the critical mode can be obtained as

$$d_{bcm} = 2L_1 f_{s1} g_e \quad (14)$$

According to (11), the minimum value of d_i at the peak grid voltage is

$$d_{ccm.min} = 1 - \frac{\sqrt{2}V_g}{V_d} \quad (15)$$

where V_g is the root meaning square value of the grid voltage.

When $d_{ccm.min}$ is larger than (15), the PFC works in CCM, otherwise it works in DCM. Combining (14), (15) and $g_e = P_{in} / v_g^2$, g_e needs to satisfy (16) when the system is completely discontinuous or completely continuous.

$$\begin{cases} g_e < \frac{1}{2L_1 f_{s1}} - \frac{\sqrt{2}V_g}{2L_1 f_{s1} V_d} & \text{DCM} \\ g_e \geq \frac{1}{2L_1 f_{s1}} & \text{CCM} \end{cases} \quad (16)$$

The MCM control mode of the PFC converter determines the duty cycle steady-state open-loop term to select d_{ccm} or d_{dcm} according to g_e . In the PFC circuit of the online UPS, there is a double-line-frequency ripple, 100Hz or 120Hz, in the dc bus voltage during the grid-connected mode. The bandwidth of the voltage loop is usually set low to attenuate such low frequency ripple; however, the PFC dynamic performance suffers. Therefore, load current feed forward is introduced in the current dead-beat MCM controller to the PFC. Applying Kirchhoff's Current Law (KCL), the inverter load current i_o is the difference between the diode output current i_d and the filter capacitor output current i_c . We get

$$i_o = i_d - i_c = (1-D)i_{L2} - C_3 \frac{dv_c}{dt} \quad (17)$$

After discretizing (17), the instantaneous value expression of the output current of the dc bus with load can be obtained as

$$i_o(k) = (1-d_{PFC}[k-1])i_{L1}(k) - C_3 \frac{v_d[k] - v_d[k-1]}{T_s} \quad (18)$$

The PFC controller in Fig. 4 can be obtained by putting the above load current as a feed forward term into the PFC current deadbeat MCM control.

C. Three level inverter control

The inverter adopts PI control and repetitive control in the voltage outer loop; improved predictive control is used in the inner current loop, and the predictive control directly gives the duty cycle of the next switching cycle according to the inductor current reference so that improve the dynamic

performance of the inverter.

When the inverter is operating at steady state, the changes of the bridge arm point A and v_{L2} of the filter inductor L_2 during the the switching period of $[k, k+1]$ are

$$v_{L2}[k] = \begin{cases} v_{inv}[k] + (i_{L2}[k+1] - i_{L2}[k]) \frac{L_2}{T_{s2}} \\ V_d[k] \times d_{inv}[k] \end{cases} \quad (19)$$

where v_{inv} is inverter voltage, L_2 is inverter filter inductance, i_{L2} is inductor current, and d_{inv} is inverter duty cycle. The inner loop control target is the value of the inductor current at $[k+1]$, which is the value of the sampled value $i_{L2}[k+1]$ tracking reference current value $i_{ref}[k+1]$.

The output duty cycle of the inner loop controller is expressed as

$$d[k] = \frac{v_{inv}[k] + (i_{ref}[k+1] - i_{L2}[k]) \frac{k_{ip} L_2}{T_s}}{V_d[k]} \quad (20)$$

The input-to-output transfer function of the current loop can be derived by combining (20) and LC type filters

$$\frac{i_{L2}(z)}{i_{ref}(z)} = \frac{1}{\frac{L_2}{T_{s2} k_p} (z-1) + 1} \quad (21)$$

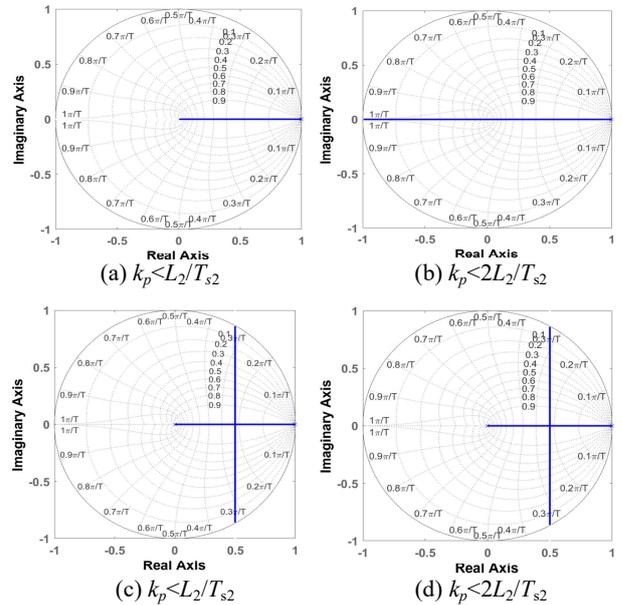


Fig. 5. Root locus of the current loop transfer function with k_p transform ((a) and (b) for (21), (c) for (22), (d) for (23))

The inverter circuit parameters of T_{s2} and inductor L_2 are selected as 50 μ s and 1.8 mH respectively without considering the system delay. Fig. 5(a) and Fig. 5(b) are graphs showing the variation of the zero-pole of (21) with the coefficient k_p . The necessary and sufficient condition for the system to be stable in the Z domain is that its poles are distributed in the unit circle of the Z domain. In Fig.5 (a), when the proportional coefficient $k_p < L_2/T_{s2}$, the system with

the pole in the right half of the real axis will have low-pass output characteristic. When $L_2/T_{s2} < k_p < 2L_2/T_{s2}$, the system with the pole in the left half of the real axis will have high-pass output characteristic. Thus, the proportional coefficient k_p of the predictive controller must be less than L_2/T_{s2} .

Since the actual on-line UPS system has control delay, the duty cycle $d[k]$ in (20) needs to add a delay zero-order keeper Z^{-1} before outputting. After adding the zero-order keeper in (21), we get

$$\frac{i_{L2}(z)}{i_{ref}(z)} = \frac{1}{\frac{L_2}{T_{s2}k_p}z(z-1)+1} \quad (22)$$

Fig. 5(c) shows the variation of the zero-pole point of (22) with k_p . Since the system will not be stable when $k_p > L_2/T_{s2}$, thus, in order to satisfy both the stability and low-pass output characteristics of the system, the proportional coefficient must be satisfied $k_p < L_2/T_{s2}$, and its stability margin is L_2/T_{s2} . The purpose of predictive control is to make the error be zero in the next cycle. Too small stability margin will result in insufficient stability margin and poor dynamic performance of the online UPS system. However, it is difficult to reduce the control error to zero due to the parameter uncertainty of system in practical use.

In order to overcome this problem, an improved predictive current control strategy that can automatically convert the current error into zero is proposed combined with [29], which doubles the stability margin of the system. The improved design of the predictive current inner loop is given by

$$d_i[k] = \frac{v_{inv}[k] + (i_{ref}[k+1] - i_{L2}[k] - 0.5 \times e_i[k]) \frac{k_p L_2}{T_{s2}}}{V_d[k]} \quad (23)$$

where $e_i[k]$ is the current error.

Fig. 4 shows the control structure of the improved inverter current loop, and Fig. 5(d) shows the corresponding closed-loop root locus. The predictive current can give a control duty ratio, according to the predictive current change in the next cycle, to improve the dynamic and static performance of the UPS inverter output voltage. Since the traditional voltage PI control will cause the voltage waveform distortion when the online UPS has a non-linear load, a method of directly inserting repetitive controller to solve the problem is adopted in [17], [30]. Combined with the repetitive controller, the inner-loop predictive current control proposed in this paper constructs the block diagram of control structure of the inverter link shown in Fig.4, where z^{-N} is the delay unit, z^k is the time advance unit, k_r is the controller gain, $S(z)$ is compensator, and $Q(z)$ is the low-pass filter function. Similar to the methods given in [29], we can get the repetitive controller parameters. Then, the design of the outer loop voltage PI and repetitive control can be completed. The reference generated by the voltage loop is given a corresponding predictive current inner loop to form an inverter control duty cycle.

IV. EXPERIMENTAL RESULTS

To verify the performance of the proposed UPS system, a laboratory prototype with an output power of 1kVA has been implemented with the specifications shown in Table I. The parameters of this prototype are given in Table II. And the DSP in the prototype uses TMS320F28035.

TABLE I

SYSTEM SPECIFICATION			
Specification	Value	Specification	Value
Rated Power	1kVA	Rated Efficiency	Grid mode: >90%
Input voltage	160V-242V	Output voltage	220V ±1V
f_{in}	50Hz/60Hz	f_{out}	$=f_{in}$
PF _{in}	>0.99	PF _{out}	0.7-1
Input THDi	<5%	Output THDu	<3%

TABLE II
PARAMETERS OF EXPERIMENTAL PROTOTYPE

Symbol	Value	Parameters
f_{s1}	40kHz	PFC switching frequency
f_{s2}	40kHz	DC-DC switching frequency
f_{s3}	20kHz	Inverter switching frequency
v_g	160V _{rms} ~240V _{rms}	Grid input voltage
V_d	±360V	DC bus voltage
V_{inv}	220V _{rms}	Inverter output voltage
P_o	1000VA	Inverter output power
L_1	1.2mH	PFC boost inductor
L_2	1.8mH	Inverter filter inductor
C_1, C_2	700uF	DC bus capacitor
C_3	4.7uF	Inverter filter capacitor
G_1, G_2	IKW15N120H3	PFC switch IGBT
D_1, D_2	RHRP8120	PFC freewheeling Diode
S_1, S_2	STGB14NC60KD	Inverter switch IGBT
D_3, D_4	MUR1560	NPC freewheeling Diode

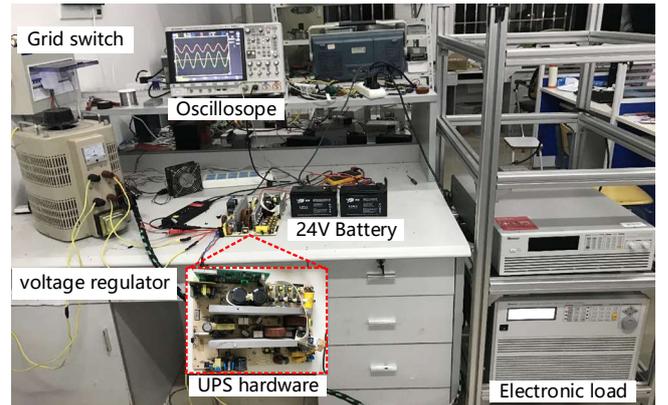
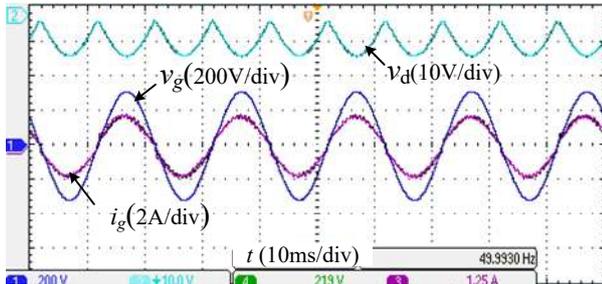


Fig. 6. Experimental setup.

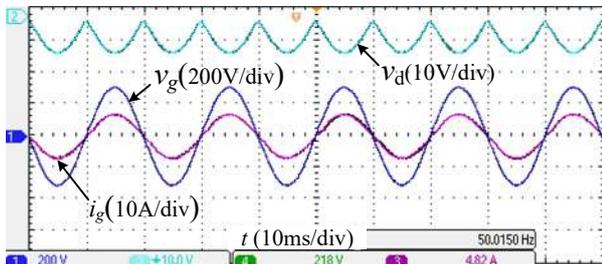
The constructed prototype of proposed UPS and its experiment test platform are shown in Fig. 6. It is worth to mention that it will have a very high voltage spikes across the devices G_3 and G_4 in the push-pull dc-dc converter shown in Fig. 2(b) due to the leakage inductance of the center tapped transformer windings, if there is no any absorb/snubber circuit. Therefore, RC absorb circuits are used in this experimental

hardware. Then, the following experimental tests are carried out.

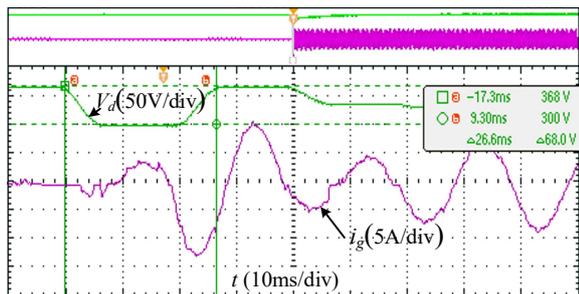
A. Grid-connected mode



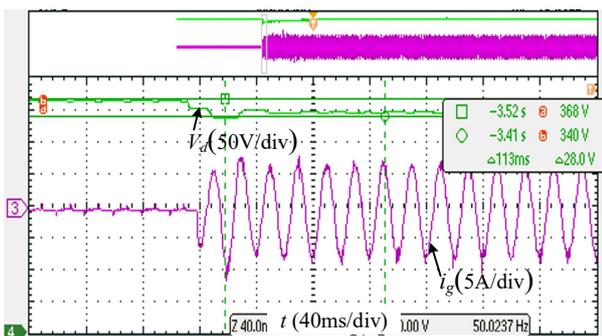
(a) Output power 250W



(b) Output power 1050W



(c) No load current feedforward sudden load



(d) Load current feedforward sudden load

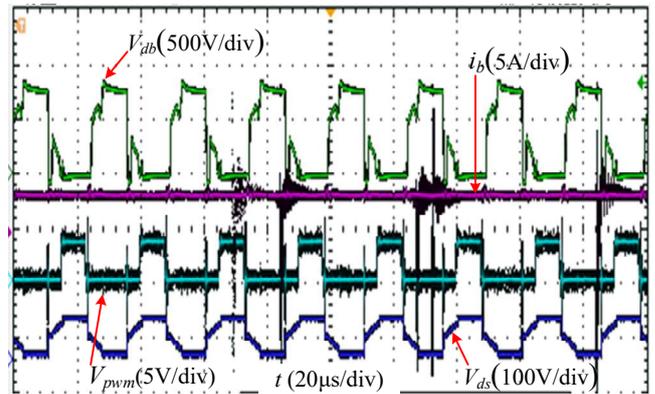
Fig. 7. Experiments of the proposed PFC converter.

Fig.7 shows measured waveforms from the PFC converter and the cascaded NPC inverter with the resistive load. Where v_d is the variation waveform of driving voltage duty cycle, v_g and i_g are the grid voltage and current, respectively. Fig. 7(a) and Fig. 7(b) show the PFC waveform at 25% of full load and rated load 1kw when the grid input voltage is 220Vrms; Fig.

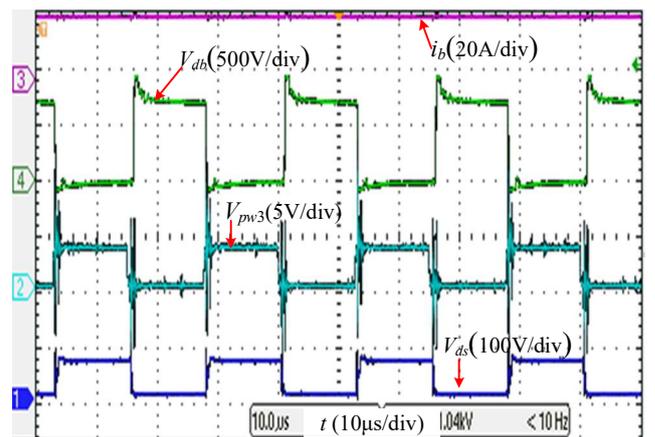
7(c) shows that sudden load causes the dc bus voltage to drop of approximately 9.5% when no load current feed forward. The experimental waveform after adding the load current feed forward control as shown in Fig. 7(d), and the bus voltage drops only 3.9%.

B. Battery mode

The experimental waveform of the battery to maintain the stability of dc bus voltage is shown in Fig. 8. Where V_{ds} is the drain to source voltage of the switch G_3 . V_{pwm} is the driving signal of G_3 , and it is inverse phase with the gate voltage of V_{G3} due to the isolated driving circuit with optocouplers. i_b is the battery output current, and V_{db} is the voltage of the secondary side rectifier diode D_{b2} . The voltage and current waveforms of each key point when the push-pull output power is 100W as shown in Fig. 8(a), and the waveform corresponding to the output power at 700 W as shown in Fig. 8(b).



(a) DC-DC output power 100W



(b) DC-DC output power 700W

Fig. 8. Experiments of DC-DC converter.

When the power supply is normal, the experimental waveforms of the dc bus voltage, which is supplied by the PFC rectifier and loaded by the inverter, is as shown in Fig. 9. Where V_{GS4} is the driving voltage of the switch S_4 , V_A is the voltage of the midpoint of the bridge arm to the negative bus,

the inverter voltage is v_{inv} , and the load current is i_o .

Under light load condition, the experimental waveform of inverter output voltage, the waveforms of the corresponding driving signal and the bridge point A is as shown in Fig. 9(a). Fig. 9(b) and Fig. 9(c) show the output voltage and current at light load and full load, respectively. The distortion of the inverter voltage waveform when the voltage PI loop with nonlinear load as shown in Fig. 9(d). The inverter voltage waveform when the repetitive control voltage loop is combined with the predictive current inner loop under a nonlinear load as shown in Fig. 9(e).

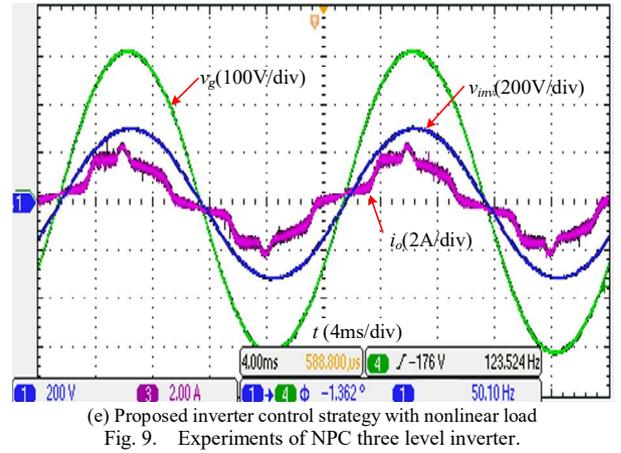
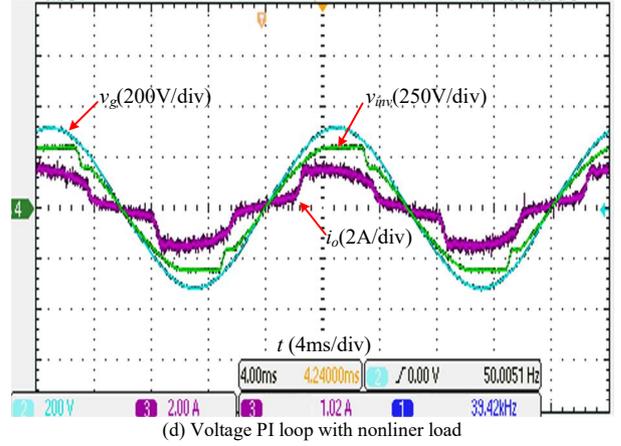
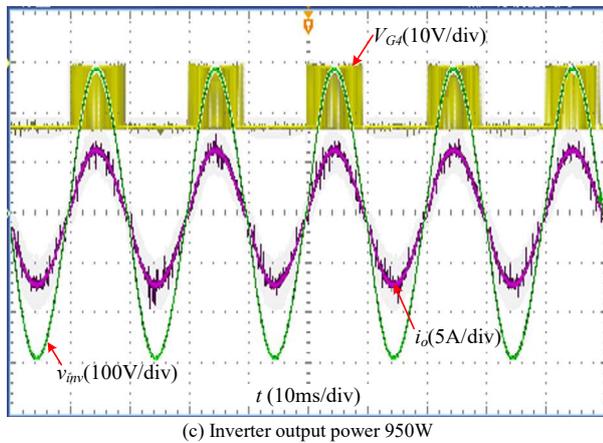
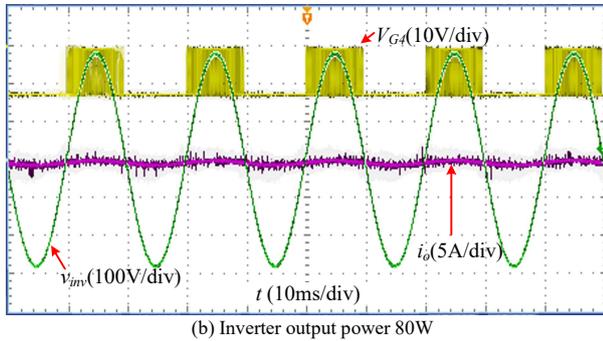
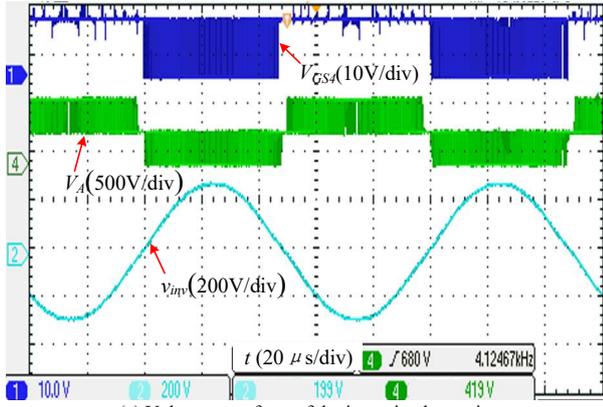
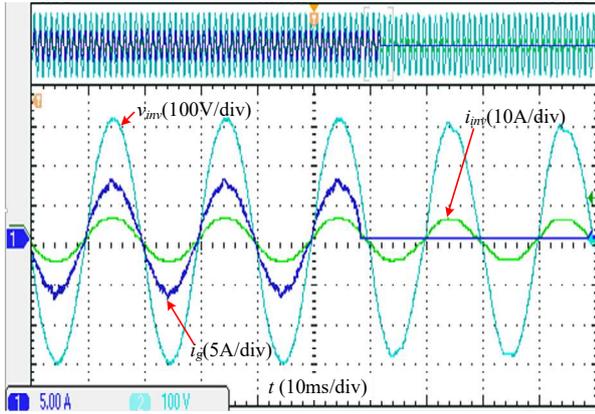


Fig. 9. Experiments of NPC three level inverter.

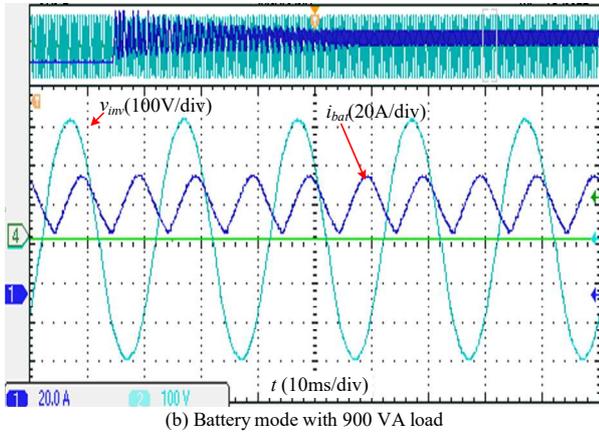
C. Transition from grid-connected mode to battery mode

When there is a power failure, the online UPS needs to be powered by the battery bank to ensure safe and reliable operation of the equipment. Fig. 10 shows the experimental waveform of the power supply from the battery mode when the power failure occurs and the PFC rectifier does not work. In Fig. 10 (a), it can be seen that when there is no power from the utility grid, the battery provides the dc bus voltage to ensure the stability of the UPS output inverter voltage. The corresponding experimental waveforms of the inverter voltage and battery current in this mode are shown in Fig. 10(b).

The measured efficiencies and total harmonic distortion (THD) are presented in Fig. 11. The efficiency test of the invert output with resistive load is shown in Fig. 11(a). The peak value of the two-stage conversion efficiency of the grid-connected state and the battery mode is 92% and 90.8%, respectively. As can be seen from Fig. 11(b), the commercial grid side PFC grid-connected current THDi is 3.4% at full load, and the invert output voltage THDu with resistive load is 1.7% at the full load



(a) Transition from grid mode to battery mode



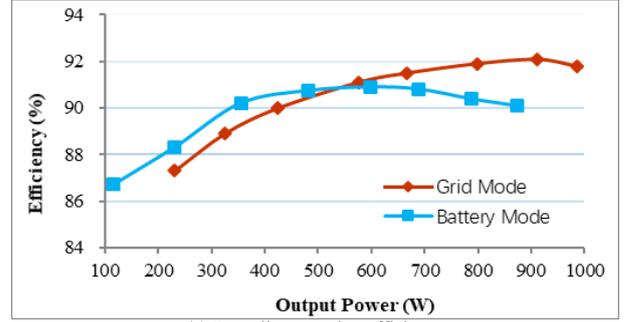
(b) Battery mode with 900 VA load

Fig. 10. Experiments of grid-connected mode and battery mode.

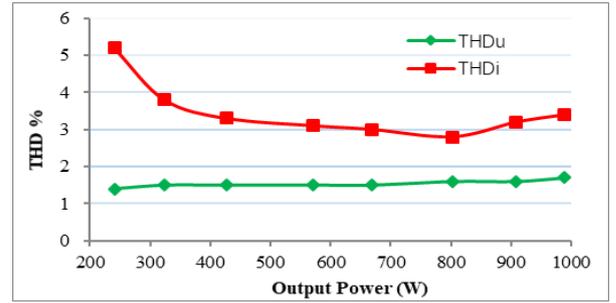
Table III shows the performance comparison of different UPS structures to compare the performance of the proposed UPS prototype. Online UPS develops towards high frequency and power density, traditional methods use multi chips DSP to work together or single chip high performance DSP to realize the high frequency of the UPS. In the proposed experimental prototype. If the semiconductor devices with low conduction and switching loss are used for instance wide bandgap devices, the efficiency of the whole system can be further improved.

TABLE III
COMPARISON OF THE PROPOSED UPS SYSTEM

Types of UPS	Efficiency	Power Ratings	Battery bank	Size	Master chip	Switching frequency
110V/220V online UPS ^[5]	86%	2.6kVA	108V	big	AC-DC\UC3854B DC-AC\PIC16F870 DC-DC\unknown	50kHz
Z-source inverter based UPS(battery mode) ^[12]	95%	3kVA	360V	medium	Only one DSP in battery mode	10kHz
Little battery bank online UPS ^[14]	92%	1kVA	24V	small	TMS320F28335 (150MHz)	AC-DC 30kHz DC-DC 30kHz DC-AC 20kHz
UPS proposed in this paper	92%	1kVA	24V	small	TMS320F28035 (60MHz)	AC-DC 40kHz DC-DC 40kHz DC-AC 20kHz



(a) Overall conversion efficiency



(b) Measured THD curve of input ac current and output ac voltage

Fig. 11. Test results of the prototype

V. CONCLUSION

A low-cost single-phase online UPS topology is proposed and researched in this paper. A novel single-phase bridgeless boost PFC circuit with a bidirectional switch has been used, and the dynamic and the static performance of the PFC has also been improved by the MCM current deadbeat control with the load current feed forward. By the voltage loop PI + repetitive control combined with the predictive current control strategy, THDu of ac output voltage is lower than 2% over the entire load range. A multi-task decomposition method for implementation of "multiplier", which is completed by the way of task parallelism, and overall control of the online UPS system on a monolithic low cost DSP embedded with CLA. This provides an effective solution for designing low cost, the high frequency, high

power density and high complex power electronic systems. It is worth to mention that the bidirectional switch rectifier containing two IGBTs can be replaced by one GaN bidirectional switch with lower power loss, when the price of high voltage GaN device decline in future. Based on the proposed online UPS and its control strategy with multi-task decomposition, the system efficiency will be higher by using SiC diodes and SiC MOSFETs in inverter.

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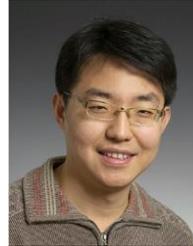


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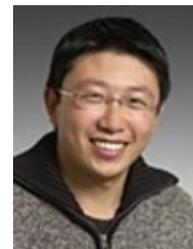


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