A power converter embodied in a semiconductor substrate member

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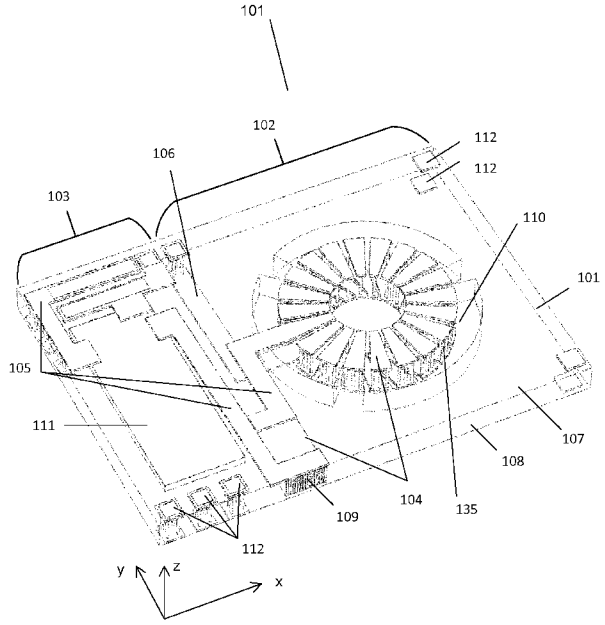

Fig. 1

(57) **Abstract:** A power converter, such as a DC-DC converter or a power amplifier, embodied on a semiconductor substrate member (101), comprising: a first region (102) with a passive electrical component (104) with a first electrically conductive layer pattern (105) of an electrically conductive material and a second electrically conductive layer pattern (106) of an electrically conductive material deposited on respective sides (107, 108) of the semiconductor substrate member; wherein a trench (109) or through-hole (110) is formed (by etching) in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and electrically connected to one or both of the first conductive layer pattern (105)andthe second conductive layer pattern (106); and a second region (103) with an active semiconductor component (111) integrated with the semiconductor substrate (101) by being fabricated by a semiconductor fabrication process. There is also provided a power

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supply, such as a DC-DC converter, embedded the semiconductor substrate member.

A power converter embodied in a semiconductor substrate member

Semiconductor substrate components are widely used to closely integrate a few to millions of semiconductor components such as transistors, diodes, resistors, capacitors or even inductors to form much more complex circuits like central processing units, CPUs, microcontrollers and a wide range of other devices like modems for wired or wireless communication.

However, oftentimes it is necessary to electrically connect external passive components such as inductors and capacitors to the semiconductor components. In connection therewith, it is observed that there is an unmet demand for further closely integrating electrical circuits.

A special technical field, where there is such an unmet demand for closely integrating electrical circuits, is the field of power supply units, such as DC-to-DC converter units, which are typically based on switched-mode power conversion.

Typical requirements for a power supply unit, in general, are: low cost, light weight, high degree of reliability, efficient power conversation, and small size. Further typical requirements are modularity and being "easy to use".

With the earliest switched-mode power converters, it became clear that higher switching frequencies allow smaller inductors and capacitors. This in turn should lead to smaller, lighter, and less costly systems. Smaller inductors and capacitors generally contribute to higher power densities. Power density may be defined as electrical power per volume unit, such as [W/mm^3], which represents rated electrical power input to or output from a power converter divided by the cubic space of the power converter.

However, using a high switching frequency is not enough to achieve higher power densities. Also, a high switching frequency may come at the cost of decreased efficiency of the switched-mode power converter since parasitic

components play an increasing role with increasing switching frequency. New devices need to be developed to achieve a goal such as higher power density.

In general, it should be appreciated that a semiconductor substrate member is a piece of substrate which may have embedded therein, by a semiconductor manufacturing process, one or more semiconductor components.

In contrast thereto, semiconductor substrate member may carry one or more components attached to the semiconductor substrate member e.g. by soldering or wire-bonding or another bonding technique. This is typically performed by (during) montage or mounting, such as surface mounting.

Also, it should be appreciated that a semiconductor substrate member may be attached to one or more other semiconductor substrate members e.g. in a stack. Further, a semiconductor substrate member may be attached to a printed circuit board, PCB; which may have one or more metal layers supported by layers of e.g. a glass-fibre reinforced epoxy material.

Generally, it is known that wire-bonding connections introduces parasitic inductances and resistances and behaves as antennas transmitting electromagnetic radiation which easily causes problems related to electromagnetic interference, EMI, especially at (high) switching frequencies.

Generally, stray electromagnetic fields are known to cause problematic Electromagnetic Interference, EMI. Especially, switched circuits, such as switched power supplies like DC-to-DC converters and switched power amplifiers like class-D power amplifiers, are prone to cause EMI problems.

Generally, it is known that so-called flip-chipping, which is a technique used for surface mounting semiconductor substrate members to e.g. printed circuit boards, has its limitations in terms of stacking components since a semiconductor substrate member for flip-chipping has only one side available for mounting.

Generally, in the field of power converters circuit architectures fully or partially implemented in a silicon substrate as a small-sized module, it is known that the term PSiP designates “Power Supply in a Package” and the term PwrSoC designates “Power Supply on a Chip”.

RELATED PRIOR ART

US 8,907,447 discloses an inductor integrated in a semiconductor substrate for use in a DC-DC converter. Such an inductor is sometimes referred to as a power inductor in silicon. In an embodiment, the inductor has a magnetic core of magnetic material embedded in a silicon substrate and a conductive winding. The inductor is a spiral inductor, or a toroidal inductor integrated in the substrate. A cap layer of magnetic material is disposed on at least one side of the silicon substrate to increase the inductance of the inductor. It is also described that the DC-DC converter includes an integrated circuit mounted on top of the cap layer of the power inductor in silicon. However, despite of having a small size, there is still a need for more integration and improved efficiency of such DC-DC converters. Also, The process used for manufacturing the inductors is not compatible with semiconductor processes which makes it harder to integrate active devices and other passive devices in the same substrate for tighter integration.

KR 10-0438892 discloses a one-chip module package by forming an integrated circuit and a thin film inductor in the same semiconductor substrate. A first and a second well region are formed in a semiconductor substrate. A first and a second MOS (Metal Oxide Semiconductor) transistor are formed on the first and second well region, respectively. A plurality of metal layer patterns are electrically connected between the first and second MOS transistor and impurity regions. A protecting isolation layer is located on the resultant structure for separating the metal layer patterns. A lower core layer pattern is formed on the predetermined portion of the protecting isolation layer. The first polyimide layer, a metal coil layer, the second polyimide layer, an upper core

layer pattern, and the third polyimide layer are sequentially formed on the resultant structure.

Most of the prior art on integrated power supplies use either on-silicon inductors or in-silicon inductors fabricated by 2D semiconductor fabrication technologies. 2D semiconductor fabrication technologies are limited to planar inductor geometries, such as circular spirals, rectangular spirals, and elongated spirals (so-called racetrack inductors) - all of which induces strong stray electromagnetic fields perpendicular to the inductor plane. This is a problem towards closer integration of components since the stray electromagnetic fields, perpendicular to the inductor plane, interferes with other components, such as active semiconductor devices, integrated in proximity of the inductor, whereby electromagnetic interference (EMI) is likely to become an issue.

Thus, there is still a need for a small-size one-chip module package which enables tight integration and reduced stray electromagnetic fields.

SUMMARY

It is realized that a fully functional power converter, such as a DC-to-DC converter can be embodied on a single semiconductor substrate member with a thickness of less than a millimetre including all active and passive components needed. There is provided:

A power converter embodied in a semiconductor substrate as set out below. In some embodiments the power converter is a DC-DC converter. In some embodiments the power converter is a power amplifier e.g. an audio power amplifier.

There is also provided a semiconductor substrate member, comprising:

- a first region with a passive electrical component with a first electrically conductive layer pattern of an electrically conductive material and a second electrically conductive layer pattern of an electrically conductive material

deposited on respective sides of the semiconductor substrate member; wherein a trench or a through-hole is formed in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and electrically connected to one or both of the first conductive layer pattern and the second conductive layer pattern; and

- a second region with an active semiconductor component embedded in the semiconductor substrate member by a semiconductor fabrication process.

Such a semiconductor substrate member enables the manufacture of thin power supplies which are suitable for products which require very tight integration of its components, such as in mobile devices e.g. smart-phones, smart-watches etc. Oftentimes, such products require a certain degree of Electromagnetic Compatibility, EMC, to ensure proper functioning of advanced circuitry inside the product.

Such a semiconductor substrate member enables better inductor topologies such toroidal inductors and solenoid inductors, compared to spiral inductors. This may be attributed to the geometry enabling an improved quality factor (related to storing of energy to losses ratio) of the inductor.

Such a semiconductor substrate member can be made much smaller that corresponding components on a Printed Circuit Board and with much smaller tolerances, which in turn reduces parasitic elements and hence enables use of higher switching frequencies e.g. in a power supply module such as DC-DC converter.

Especially, it is possible to reduce electromagnetic field radiation from the semiconductor substrate member. The passive components have a 3D, three-dimensional, configuration extending not only as electrical paths at the surface of the semiconductor substrate member in one or both of a horizontal top and bottom plane, but also with electrical paths through the semiconductor substrate member in a vertical direction. Thus, forming a 3D, three-

dimensional, configuration. This enables to a higher degree, than for planar passive components, to keep electromagnetic fields, at least where they are strongest, inside the volume of the semiconductor substrate member.

The active semiconductor component embedded in the semiconductor substrate member may be fabricated e.g. by a Silicon, Gallium-nitride, or Gallium-arsenide semiconductor fabrication process. The semiconductor fabrication process may be a conventional semiconductor manufacturing process where a semiconductor wafer is used as a starting material for the manufacturing process. The process may involve etching, deposition of implants such as a so-called dopant like Boron and Phosphorus to form active devices like transistors and diodes, and deposition of metal one or more layers to form interconnects among the active components. The result of the process is a processed wafer with active components.

The processed wafer with active components is passivated by one or more protective layers to protect the active components from post processing steps.

Post processing steps are applied to form the passive components. Post processing steps may include etching to form trenches and through-holes and deposition to apply one or more metal layers to form the passive components. The one or more metal layers are formed e.g. at the through-holes to form through-substrate vias (TSVs) and/or at the one or more trenches and/or between the passive component and the one or more active components to form the electrically conductive layer pattern and/or at pads for soldering or wire-bonding to attach additional component members. One or more steps of post processing is to establish electrical connection between the passive components and the active components by deposition of a metal layer; this may include removing the protective layer fully or partially to enable electrical connection with the active components. The result of post processing is the semiconductor substrate member. The semiconductor substrate member may

implement a power supply, a power amplifier or another integrated circuit comprising active and passive components.

Following post-processing, the semiconductor substrate member is manufactured and may be subject to assembly steps e.g. for being attached to a so-called lead-frame and/or a PCB and/or for having component members, such as SMD components attached to it by soldering. Also, component members may be attached by wire-bonding.

Manufacturing of a semiconductor substrate member with a structure as set out in the claims and generally described herein can be performed with a conventional semiconductor manufacturing process method and a method for manufacturing a hollow MEMS structure e.g. as described in WO 201 7/1 0821 8-A1 assigned on its face to Danmarks Tekniske Universitet.

The thickness of the semiconductor substrate member may be e.g. about 280 urn, 350 urn, 500, 1100 urn. The member may have a rectangular shape and be e.g. 6 by 9 mm or larger or smaller. The member may also have another shape e.g. circular or oval.

The first region and the second region may abut one another e.g. at a transverse or longitudinal border across the semiconductor substrate member. The first region and the second region may be spatially non-overlapping. The first region and the second region may have any shape and may have a mutually spatially complementary shape.

Depositing comprises one or more of electro-deposition, sputtering, evaporation, atomic layer deposition.

The semiconductor components may be in accordance with complementary metal-oxide-semiconductor (CMOS) technology. The power supply may be implemented as a so-called interposer, which may be arranged between an application printed circuit board (PCB) and an integrated circuit (IC). The

interposer may establish conductive vias or paths between the PCB and the 1C.

Further embodiments are described in the detailed description.

There is also provided a stack of components comprising one or more semiconductor substrate members as set out herein, wherein at least one semiconductor substrate member comprises pad portions on a top side and pad portions on a bottom side.

A stack of components may comprise: a first semiconductor substrate member and a second semiconductor substrate member. A stack of components may additionally comprise one or more of: a PCB, one or more further semiconductor substrate members, and more or more discrete components such as passive components and/or active components. The components may be surface-mount components. The components in the stack may be attached to each other at the pad portions by soldering or gluing.

There is also provided a DC-DC converter comprising a semiconductor substrate as described herein.

The DC-DC converter may have a configuration selected from the group of: Buck-converters, boost converters, and fly-back converters. The converters may be step-up or step-down converters. The converter may be a resonant converter. The DC-DC converter may be configured for voltages up to 10 volts or higher, e.g. 48 volts. The DC-DC converter may be configured to power levels of up to 20-30 Watts or higher.

BRIEF DESCRIPTION OF THE FIGURES

A more detailed description follows below with reference to the drawing, in which:

fig. 1 shows a perspective view of a semiconductor substrate member with a first region with a passive electrical component and a second region with an active semiconductor component integrated with the semiconductor substrate member;

fig. 2 shows a perspective view of the semiconductor substrate member of fig. 1 with additional component members mounted on one side of the semiconductor substrate member;

fig. 3 shows a perspective view of a solenoid inductor embedded in the semiconductor substrate member;

fig. 4 shows a perspective view of a winding of an inductor embedded in the semiconductor substrate member;

fig. 5 shows a perspective view of a first coil and a second coil of an inductive transformer or a coupled inductor with coupled coils which can be embedded in the semiconductor substrate member;

fig. 6 shows a perspective view of the toroidal inductor embedded in the semiconductor substrate member and having a inductor core which has an array of deep trenches.

fig. 7 shows a cross-sectional view of the inductor core which has an array of deep trenches;

fig. 8 shows a cross-sectional view of a trench, of an inductor core, filled with a magnetic material;

fig. 9 shows a cross-sectional view of a trench, in an inductor core, filled with a magnetic material or magnetic particles suspended in epoxy;

fig. 10 shows a cross-sectional view of a trench, in an inductor core, laminated with a first layer of a magnetic material and a second layer of a non-magnetic material;

fig. 11 shows a perspective view of the capacitor embedded in the semiconductor substrate member and cross-sectional views, A-A and B-B thereof;

fig. 12 shows a cross-sectional view of another capacitor, which can be embedded in the semiconductor substrate member; and

fig. 13 shows cross-sectional view of yet another capacitor, which can be embedded in the semiconductor substrate member.

DETAILED DESCRIPTION

In some embodiments, the semiconductor substrate member is embodied as power supply in a package, PSiP, embodied as a micro-fabricated 3D passive interposer. The micro-fabricated 3D passive interposer may have a size less than about 40 by 40 by 1 mm, e.g. about 4 by 8 by 0.3 mm, and comprise 3D toroidal inductor with through-substrate vias, TSVs, and through-substrate vias establishing interconnects from one side of the micro-fabricated 3D passive interposer to the other. The power supply in a package may comprise a Buck converter or a Class DE resonant converter. The power supply in a package may comprise active components, such as one or more Field Effect Transistors, FETs, one or more gate drivers, and capacitors. The power supply in a package may operate in accordance with zero-voltage switching (ZVS), e.g. in accordance quasi-square wave (QSW) mode, to convert a first DC voltage, e.g. about 5 VD, to a second DC voltage e.g. about 3.3 VDC. The power supply in a package may operate at a switching frequency above 5 MHz e.g. at about 22 MHz. The power supply in a package may comprise a 3D air-core toroidal inductor e.g. of about 50-nH. However, the claims are not limited thereto. A Buck-type converter, power supply in a package, was successfully tested with an output current from 0 to 300 mA and an input voltage from 3.5 to 8.5 V. A peak efficiency of 83.0 % at 300 mA output current was measured and a 1.15 Watts was delivered to a load.

In some embodiments one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern extends across at least some of second region to electrically connect the active semiconductor component with the passive electrical component.

In this way the path of the electrical connection between the active component and the passive component can be made shorter and less prone to generating electromagnetic interference, EMI. Also parasitic elements can be reduced.

Then interconnection between the active component and the passive component doesn't have to go via the PCB. This in turn reduces electromagnetic field radiation. Also, costs related to assembling may be reduced.

It should be noted that the one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern extends in parallel horizontal planes e.g. at opposite (top and bottom) sides of the semiconductor substrate member. However, one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern may follow topography, such as a submicron-topography of the semiconductor substrate member.

In some embodiments the one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern comprises a pad portion which is exposed for electrical connection by soldering, wire bonding or flip-chip bonding.

Thereby, the semiconductor substrate member is configured for use as an combined active-passive interposer. The pad portion enables interconnection with other components and/or a PCB by soldering or wire-bonding. In some embodiments the semiconductor substrate member comprises pad portions on both a top side and a bottom side which enables stacking of multiple semiconductor substrate members.

Soldering may comprise using a solder paste or solder ball to electrically connect by heating to melt the solder.

Wire-bonding may comprise attaching a wire to the pad portion by applying sufficient pressure and/or heat e.g. by ultrasound. The wire for wire-bonding may comprise a metal such as gold, aluminium, or copper as it is known in the art.

Flip-chip bonding may comprise attaching a substrate to a PCB or another substrate by forming a ball or pillar of metal and gluing with an electrically conductive glue the ball or pillar to the substrate and the PCB or the other substrate.

In some embodiments one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern comprises a portion, extending from or to the pad portion, which is covered by an isolation layer. The isolation layer may be e.g. silicon oxide (Si02), aluminium oxide (AI203), or silicon nitride (Si3N4). The isolation layer may be applied using methods known in the art.

In some embodiments the semiconductor substrate member comprises an inductor formed in the first region with an inductor winding of the inductor comprising:

- a first winding portion formed in the first electrically conductive layer pattern,

- a second winding portion formed by a first through-substrate-via,

- a third winding portion formed in the second electrically conductive layer pattern, and

- a fourth winding portion formed by a second through-substrate-via;

wherein the first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

Thereby a 3D inductor is formed. Such a 3D inductor may emit a significantly reduced electromagnetic field in a direction normal to the top and bottom surface of the semiconductor substrate member compared to a planar, e.g. spiral-shaped, inductor. Instead, the claimed inductor may have an electromagnetic field which is concentrated inside the volume of the semiconductor substrate member.

In some embodiments the inductor is a solenoid inductor or a toroidal inductor.

In some embodiments an inductor winding circumscribes an inductor core, comprising a material selected from the group of: air, silicon, magnetic materials, epoxy or a combination thereof.

In some embodiments an inductor winding circumscribes an inductor core, comprising magnetic particles suspended in epoxy. The epoxy material establishes spacing between the magnetic particles, thereby reducing eddy current loss. Thereby it is possible to strike a trade-off between an inductor with an air core known to have low loss, low inductance and a magnetic core known to have high loss, high inductance.

In some embodiments an inductor winding circumscribes an inductor core which has an array of deep trenches filled with or laminated with a magnetic material or magnetic particles suspended in epoxy. The array may comprise one or more rows of deep trenches. A core may comprise an array with e.g. 10 to 500 deep trenches.

In some embodiments an inductor winding circumscribes an inductor core which has an array of deep trenches laminated with a first layer of a magnetic material and a second layer of a non-magnetic material. Thereby, the non-magnetic layer reduces eddy current loss since magnetic layers are separated by the non-magnetic layer. Thereby it is possible to strike a trade-off between an inductor with an air core known to have low loss, low inductance and a magnetic core known to have high loss, high inductance. Thereby vertical laminar layers are established.

In some aspects, the semiconductor substrate member comprises a layer or patch of an electrically non-conductive material (dielectric) at least covering some openings of the deep trenches when the trenches are laminated. In some aspects the layers are deposited by electro-deposition or atomic layer deposition.

In some embodiments the inductor comprises a first coil and a second coil circumscribing a common inductor core, wherein windings of the first coil and windings of the second coil are formed by the first electrically conductive layer pattern and the second electrically conductive layer pattern and through-substrate vias. It should be noted that “windings” are windings of an inductor formed by depositing an electrically conductive material, rather than by winding a thread about the core.

A "through-substrate via" is a via formed by firstly etching a hole through the semiconductor substrate member and then depositing an electrically conductive material to establish electrical connection from one side of the semiconductor substrate member to the opposite side e.g. extending between pads at the opposite sides. The electrically conductive material should be electrically isolated from the substrate material.

In some embodiments the semiconductor substrate member comprises a capacitor formed by:

- a first capacitor member which comprises a conductive material deposited in first deep trenches extending from a first side of the semiconductor substrate; and

- a second capacitor member which comprises a conductive material deposited in second deep trenches extending from a second side of the semiconductor substrate.

The conductive material deposited in the deep trenches extending from the first side of the semiconductor substrate is electrically connected to the first

electrically conductive layer pattern, and the conductive material deposited in the deep trenches extending from the second side of the semiconductor substrate is electrically connected to the second electrically conductive layer pattern.

Reverting to the detailed description:

Fig. 1 shows a perspective view of a semiconductor substrate member with a first region with a passive electrical component and a second region with an active semiconductor component integrated with the semiconductor substrate member. The semiconductor substrate member 101 has a substantially plate-shaped form. For convenience the size of the semiconductor substrate member 101 may be designated by a length along an x-axis, a width along a y-axis, and a height along a z-axis, as shown. Also, for convenience, the length and width are defined in a horizontal plane and the height in a vertical direction. Further, for convenience, a top side refers to one side 107 of the semiconductor substrate member (e.g. the one facing upwards in the figure) and a bottom side refers to the opposite side 108 of the semiconductor substrate member (e.g. the one facing downwards in the figure).

The semiconductor substrate member 101 has a first region 102 and a second region 103 which may be both defined in the horizontal plane. The regions may be associated with respective end-portions of the semiconductor substrate member or with another geometrical definition. The semiconductor substrate member may have a rectangular shape, a polygonal shape, a circular or oval shape or a combination thereof. Also, the first region 102 and the second region 103 may have a rectangular shape, a polygonal shape, a circular or oval shape or a combination thereof.

One or more passive electrical components 104, e.g. selected from the group of inductors, capacitors and resistors, may be accommodated within the first region 102.

One or more active semiconductor components 111 may be integrated within a second region 103 of the semiconductor substrate member 101 by being fabricated by a semiconductor fabrication process. The active semiconductor components may be selected from the group of transistors, diodes or any devices fabricated by a conventional semiconductor fabrication process. As it is known in the art, the semiconductor fabrication process may restrict transistors and diodes within the certain types e.g. CMOS types or bipolar types. It should be noted that the one or more active semiconductor components 111 are depicted as a rectangular 3D space, however, as it is known within the field of semiconductors, multiple semiconductor components - such as arrays of semiconductor components may be arranged and electrically interconnected in such a 3D space, irrespective of its shape.

One or more first electrically conductive layer patterns 105 of an electrically conductive material and one or more second electrically conductive layer patterns 106 of an electrically conductive material may be deposited on respective sides 107, 108 of the semiconductor substrate member 101. The one or more first electrically conductive layer patterns 105 and the one or more second electrically conductive layer patterns 106 serves to electrically connect one or more passive components within the first region with one or more active components within the second region. Additionally, or alternatively, the electrically conductive layer patterns 106, 107 form at least portions of the one or more passive components. The portions of the one or more passive components may be one or more of e.g. portions of inductor windings and portions of capacitor plates. In this respect the term 'windings' should be construed as being a winding of an inductor which is not "winded" as a thread, but rather a structure of an inductor. Further, the term 'capacitor plates' or simply 'plates' should be construed as serving the function of a capacitor plate, rather than necessarily having a plate-shape.

The semiconductor substrate member 101 has one or more, such as multiple, trenches 109 or through-holes 110 etched into, such as through, the

semiconductor substrate member 101. The trenches 109 or through-holes 110 are formed by an etching process, removing semiconductor material from the semiconductor substrate member within the first region and/or within the second region. An isolation layer 113 may be deposited to electrically isolate the semiconductor material from the conductive material. The isolation layer 113 may be deposited during or after the conductive material is deposited. An electrically conductive material may be deposited at selected areas at least on the bottom portion, on a sidewall, or completely fill the through-hole to electrical connect to one or both of the first conductive layer pattern 105 and the second conductive layer pattern 106.

In some embodiments, the trenches 109 or though-holes 110 is passivated using an isolation layer 113 without deposition of a conductive layer. In some embodiments, the semiconductor substrate member is configured as a power converter e.g. a DC-DC converter and/or a power amplifier e.g. an audio power amplifier.

Subsequently, electrically conductive material is deposited at least on a bottom portion of a trench or on a sidewall of the through-hole to electrically connect to one or both of the first conductive layer pattern 105 and the second conductive layer pattern 106.

In this way, one or more passive components can be formed and electrically connected to the one or more active components.

It should be known that one or more pad portions 112 may be arranged on a bottom side and/or on a top side of the semiconductor substrate member to connect to the first electrically conductive layer pattern and/or second electrically conductive layer pattern and/or to provide for mechanical support e.g. by soldering to another member such as a PCB.

An isolation layer 113 is deposited to electrically isolate the one or more conductive layers from the semiconductor material.

In some embodiments the semiconductor substrate member 101 has a size of approximately 4-by-8 mm and thickness of about 280 pm. However, the semiconductor substrate member 101 may be larger or smaller than that e.g. up to 40-by40 mm and with thickness of about 200 pm to1 100 pm.

Fig. 2 shows a perspective view of the semiconductor substrate member of fig. 1 with additional component members mounted on one side of the semiconductor substrate member. Here, it is shown that the semiconductor substrate member 101 accommodates stacked, passive electrical components 133. The stacked, passive electrical components 133 may be attached to the semiconductor substrate member by surface-mount soldering. It should be noted however, that the semiconductor substrate member 101 may accommodate stacked, active electrical components.

It should be noted that the stacked, passive electrical components 133 or the stacked, active electrical components may be denoted discrete components in the sense that they are not integrated in the semiconductor substrate member.

It should be noted that the discrete components can be arranged anywhere on the semiconductor substrate member when attached at pad portions to connect to circuitry integrated with the semiconductor substrate member.

Fig. 3 shows a perspective view of a solenoid inductor embedded in the semiconductor substrate member. The solenoid inductor 124 may be used as an alternative or in addition to the toroidal inductor. It should be noted that the semiconductor substrate member is shown only partially, not including the first region 102 which accommodates the one or more active semiconductor components.

The solenoid inductor 124 is electrically connected with one or both first electrically conductive layer pattern 105 and the second electrically conductive layer pattern 106 (not shown here). Thereby a 3D solenoid inductor is provided in the semiconductor substrate member 101.

Fig. 4 shows a perspective view of a winding of an inductor embedded in the semiconductor substrate member. The winding 144 may be a winding of a solenoid inductor or a toroidal inductor. Multiple windings 144 are arranged next to each other and are electrically connected to form an inductor as it is known in the art.

The winding 144 comprises a first winding portion 114 formed in the first electrically conductive layer pattern, a second winding portion 115 formed by a first through-substrate-via, a third winding portion 116 formed in the second electrically conductive layer pattern, and a fourth winding portion 117 formed by a second through-substrate-via. The first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

In particular, it should be noted that one or both of the second winding portion 115 and the fourth winding portion 117 may comprise one or more first through substrate vias, TSVs. The through substrate vias may have e.g. a substantially circular cross-section or have a substantially rectangular cross-section. The latter example can be described as a "vertical wall" rather than cylinders as shown.

Fig. 5 shows a perspective view of a first coil and a second coil of an inductive transformer with coupled coils which can be embedded in the semiconductor substrate member. The inductive transformer is configured as a toroidal inductive transformer and comprises a first coil 126 and a second coil 127 circumscribing a common inductor core. The first coil 126 is shown with relatively "wider" windings than the second coil 127, which has relatively "narrower" windings than the first coil 126. The first coil 126 and the second coil 127 are electrically isolated from each other. The windings "cross" each other at respective sides of the semiconductor substrate member, but not at the same side. Thus, with reference to the winding 144, for the first coil 126, a first winding portion 114 formed in the first electrically conductive layer pattern, "crosses" a respective third winding portion 116 of the second coil 127. One or

both of the width and thickness of a winding of a respective coil, may be configured to carry a respective desired amount of electrical current.

Fig. 6 shows a perspective view of the toroidal inductor embedded in the semiconductor substrate member and having an inductor core which has an array of deep trenches. For illustration purposes the semiconductor substrate member is partially cut away to better show the inductor core, which has an array of deep trenches 119.

As shown the deep trenches 119 are arranged as concentric, curved "vertical walls" to collectively substantially fit the space available within the core of the toroidal inductor or transformer as the case may be. The curved "vertical walls" are spaced apart in a direction normal to the wall. The walls may be divided into angular sections.

Fig. 7 shows a cross-sectional view of the inductor core which has an array of deep trenches. The cross-sectional view is also a cross-section of a portion of the semiconductor substrate member 101. The uppermost portion shown is an isolation layer 113, which isolates an electrically conductive material deposited in the deep trenches 119 in the inductor core from one or more first electrically conductive layer patterns (not shown here) and from the semiconductor substrate 101.

Fig. 8 shows a cross-sectional view of a trench, of an inductor core, filled with a magnetic material. The magnetic material is deposited in a deep trench laminated with an isolation layer 113 which isolates an electrically conductive material deposited in the deep trenches 119 in the inductor core from one or more first electrically conductive layer patterns (not shown here) and from the semiconductor substrate 101.

Fig. 9 shows a cross-sectional view of a trench, in an inductor core, filled with a magnetic material or magnetic particles suspended in an epoxy material. The magnetic material or magnetic particles suspended in an epoxy material is designated by reference numeral 120.

Fig. 10 shows a cross-sectional view of a trench, in an inductor core, laminated with a first layer of a magnetic material and a second layer of a non-magnetic material. The first layer 122 of a magnetic material is arranged alternately with a second layer 123 of a non-magnetic material. The layers may continue substantially horizontally at the bottom of the trench to connect vertical layers at the side or sides of the trench - alternatively, the vertical layers may terminate at the bottom of the trench with end portions of the vertical layers abutting a bottom portion of the trench.

Fig. 11 shows a perspective view of the capacitor embedded in the semiconductor substrate member and cross-sectional views, A-A and B-B thereof. The capacitor has a first terminal 136 and a second terminal 137. The first terminal 136 and the second terminal 137 faces the same side of the semiconductor substrate member 101, but could also face opposing sides.

The "capacitor plates" are implemented as deep trenches wherein an electrical conductive material is deposited to form an array of parallel "vertical walls" or "lamella" alternately electrically connected to the first terminal 136 and the second terminal 137 and alternately electrically isolated from the first terminal 136 and the second terminal 137. Otherwise, the parallel "vertical walls" are electrically isolated from each other.

Cross-sectional view, A-A, shows that the first electrically conductive layer pattern 105, of which a portion may form a portion of the first capacitor member 129, is arranged between isolation layers 113. One or more of the isolation layers may extend along sides and bottom of the deep trenches and across the semiconductor substrate member between the deep trenches e.g. to form a substantially coherent layer. The first electrically conductive layer pattern 105, of which a portion may form a portion of the first capacitor member 129, may be deposited to form capacitor plates and to mutually connect the capacitor plates. Atop the first electrically conductive layer pattern 105, another one or more of the isolation layers may be deposited. One or more portions of

the isolation layers may be removed e.g. by etching to expose electrical connection to the first electrically conductive layer pattern 105 e.g. as shown at pad portion 112 at the top-side.

Correspondingly, at the bottom side, the second electrically conductive layer pattern 106, one or more portions of the isolation layers may be removed e.g. by etching to expose electrical connection to the second electrically conductive layer pattern 106 e.g. as shown at pad portion 112 at the bottom side.

Cross-sectional view, B-B, shows essentially the same structure as shown in cross-sectional view, A-A. It can be inferred that the capacitor plates connected to respective capacitor terminals do not fully overlap, but rather are displaced relative to each other longitudinally. However, various configurations of the capacitor plates are foreseeable, e.g. comprising that the capacitor plates fully overlap in a longitudinal direction.

The isolation layers 113 also provides electrical isolation between the capacitor plates and the semiconductor substrate.

Fig. 12 shows a cross-sectional view of another capacitor, which can be embedded in the semiconductor substrate member. This configuration of a capacitor is suitable for implementing capacitors with relatively narrow trenches, which may be difficult to reliably made deep in the sense that they extend through the full depth (thickness) of the semiconductor substrate. An unfilled trench 139 may reduce the thickness of the substrate at the area where the capacitor is embedded.

As shown, the wide and unfilled trench 139 is formed in the substrate from the top-side of the semiconductor substrate member. Inside the trench is deposited a portion of the first capacitor member 129 as a layer of conductive material, which electrically is connected to the first electrically conductive layer pattern 105.

The capacitor is formed by realizing non-overlapping deep trenches from both top and bottom side of the substrate. Isolating layer 113 is applied on the top side bottom side and inside the trenches. Conductive layer from top 105 is deposited to for the first plate of the capacitor 131. The second plate of the capacitor 132 is realized by depositing a conductive layer 106 on the back side of the substrate. Another Isolation layer 113 may be deposited on top and bottom of the substrate. Pads or pad openings 112 may be realized by etching the isolation layer for external connections.

The deep trenches are laminated with an isolation layer 138 to isolate capacitor plates of different polarity from each other and serves as the dielectric material of the capacitor. The isolation layer 138 may be made from a material that has a different dielectric constant than the material of the isolation layer 113. The material of the isolation layer 138 may have a dielectric constant larger than e.g. 12 and to about 150 or up to about 200 or higher. The material of the isolation layer 138 may be a ceramic e.g. titanium-oxide, which has may have a dielectric constant in the range of 86 to 173. The material of the isolation layer 113 may be for example silicon-oxide or Aluminium-oxide.

Fig. 13 shows cross-sectional view of yet another capacitor, which can be embedded in the semiconductor substrate member. The capacitor is formed by realizing non-overlapping deep trenches from both top and bottom side of the substrate. Isolating layer 113 is applied on the top side bottom side and inside the trenches. Conductive layer from top 105 is deposited to for the first plate of the capacitor 131. The second plate of the capacitor 132 is realized by depositing a conductive layer 106 on the back side of the substrate. Another Isolation layer 113 may be deposited on top and bottom of the substrate. Pads or pad openings 112 may be realized by etching the isolation layer for external connections.

A prototype of the device integrates two 40 V gallium-nitride field effect transistors (GaNFETs) driven by a high frequency half bridge gate driver and

an in-silicon inductor in addition to input and output capacitors. The in-silicon inductor could be fabricated with a nonmagnetic-core (e.g. air core, non-conducting thermal conducting polymers) or integrated magnetic core (e.g. composite core by screen-printing, electroplated solid/laminated core). All the mounted components are commercially available. The prototype device is configured as a zero-voltage switching buck converter power stage.

The proposed converter uses a CMOS compatible process to construct 3D passive components without affecting the active part of the silicon die. As an added value, the top side of the silicon die can be used to integrate the components which are not compatible with integrated circuits processing like Gallium nitride FETs, Ceramic capacitors, etc. The mounted components are connected to the silicon devices using through silicon vias (TSVs) and/or conductive layers. The toroidal core can be fabricated with a wide range of core materials: air, silicon, non-conducting thermal polymers, composite core (micro or nanoscale magnetic powders mixed in a non-conducting thermal polymer), micro-fabricated magnetic material (magnetic thin films, lamination thin films, deep-trench magnetic).

The proposed converter allows the lowest profile converters (basically silicon wafer thickness if no stacked components are used). Lower noise converters are possible with technology due to shorter current loops and compact size.

CLAIMS

1. A power converter comprising a semiconductor substrate member (101), comprising:

- a first region (102) with a passive electrical component (104) with a first electrically conductive layer pattern (105) of an electrically conductive material and a second electrically conductive layer pattern (106) of an electrically conductive material deposited on respective sides (107, 108) of the semiconductor substrate member; wherein a trench (109) or through-hole (110) is formed in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and electrically connected to one or both of the first conductive layer pattern (105) and the second conductive layer pattern (106); and

- a second region (103) with an active semiconductor component (111) embedded in the semiconductor substrate member (101) by a semiconductor fabrication process.

2. A power converter according to claim 1, wherein one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) extends across at least some of second region (103) to electrically connect the active semiconductor component (111) with the passive electrical component (104).

3. A power converter according to claim 1 or 2, wherein the one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) comprises a pad portion (112) which is exposed for electrical connection by soldering, wire bonding or flip-chip bonding.

4. A power converter according to any of the preceding claims, wherein one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) comprises a portion, extending from or to the pad portion (112), which is covered by an isolation layer (113).

5. A power converter according to any of the preceding claims, comprising an inductor (124; 125) formed in the first region with an inductor winding of the inductor comprising:

- a first winding portion (114) formed in the first electrically conductive layer pattern,

- a second winding portion (115) formed by a first through-substrate-via,

- a third winding portion (116) formed in the second electrically conductive layer pattern, and

- a fourth winding portion (117) formed by a second through-substrate-via;

wherein the first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

6. A power converter according to claim 5, wherein the inductor is a solenoid inductor (124) or a toroidal inductor (125).

7. A power converter according to claim 5 or 6, wherein an inductor winding circumscribes an inductor core (118), comprising a material selected from the group of: air, silicon, magnetic materials, epoxy or a combination thereof.

8. A power converter according to any of claims 5-7, wherein an inductor winding circumscribes an inductor core (118), comprising magnetic particles suspended in epoxy.

9. A power converter according to any of claims 5-8, wherein an inductor winding circumscribes an inductor core (118) which has an array of deep trenches (119;120;121) filled with or laminated with a magnetic material or magnetic particles suspended in epoxy.

10. A power converter according to any of claims 5-9, wherein an inductor winding circumscribes an inductor core (118) which has an array of deep trenches (121) laminated with a first layer (122) of a magnetic material and a second layer (123) of a non-magnetic material.

11. A power converter according to any of claims 5-10, wherein the inductor comprises a first coil (126) and a second coil (127) circumscribing a common inductor core, wherein windings of the first coil and windings of the second coil are formed by the first electrically conductive layer pattern and the second electrically conductive layer pattern and through-substrate vias.

12. A power converter according to any of the preceding claims, comprising a capacitor (128) formed by:

- a first capacitor member (129) which comprises a conductive material deposited in first deep trenches (131) extending from a first side of the semiconductor substrate; and

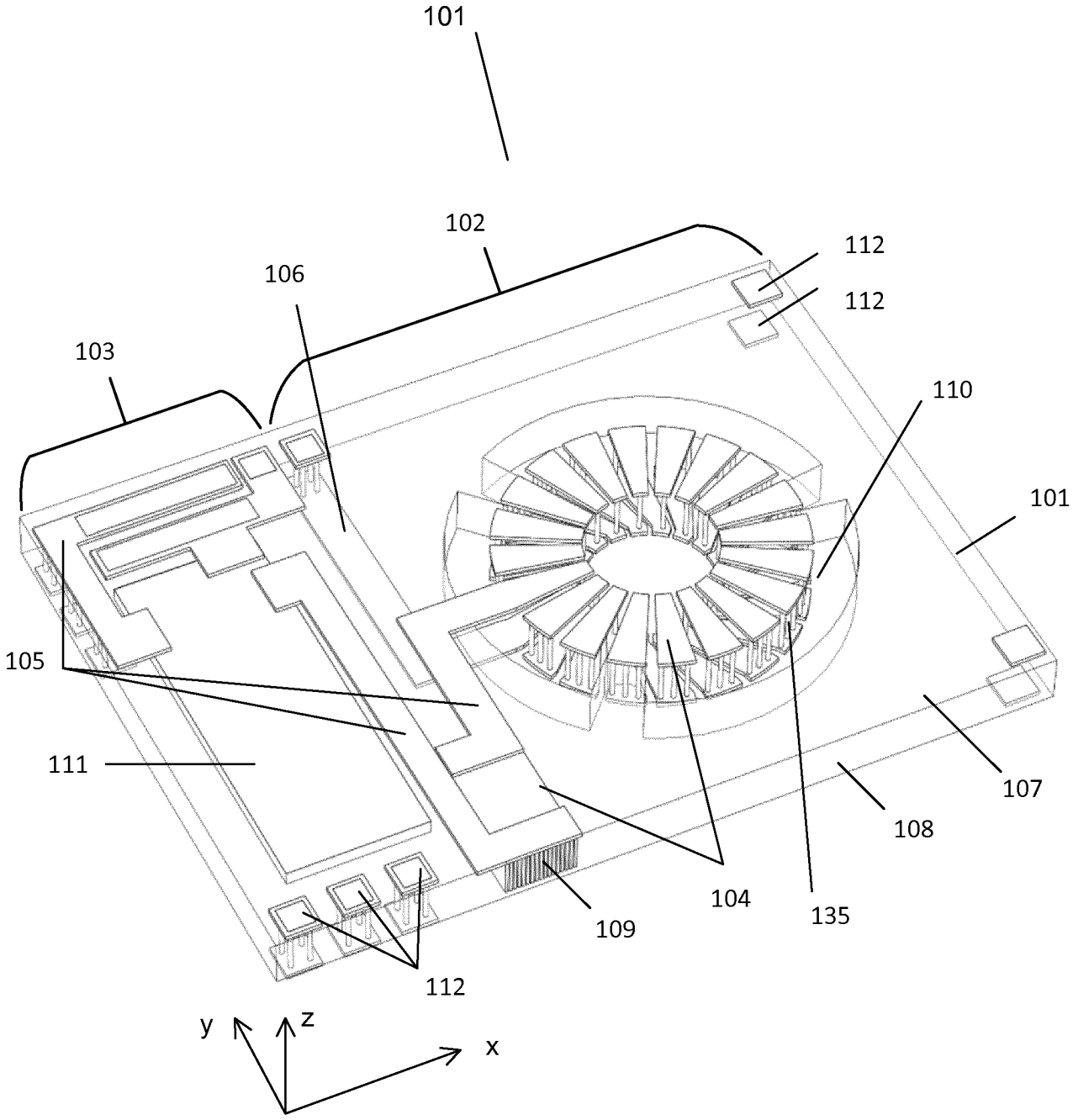
- a second capacitor member (130) which comprises a conductive material deposited in second deep trenches (132) extending from a second side of the semiconductor substrate.

13. A power converter according to any of the preceding claims, wherein the power converter is embodied in a single semiconductor substrate piece by a semiconductor manufacturing process.

14. A stack of components comprising one or more semiconductor substrate members according to any of the preceding claims, wherein at least one semiconductor substrate member comprises pad portions (112) on a top side and pad portions (112) on a bottom side.

15. A DC-DC converter according to any of claims 1-13.

16. A power amplifier, such as an audio power amplifier, according to any of claims 1-14.


101
102
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107
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y
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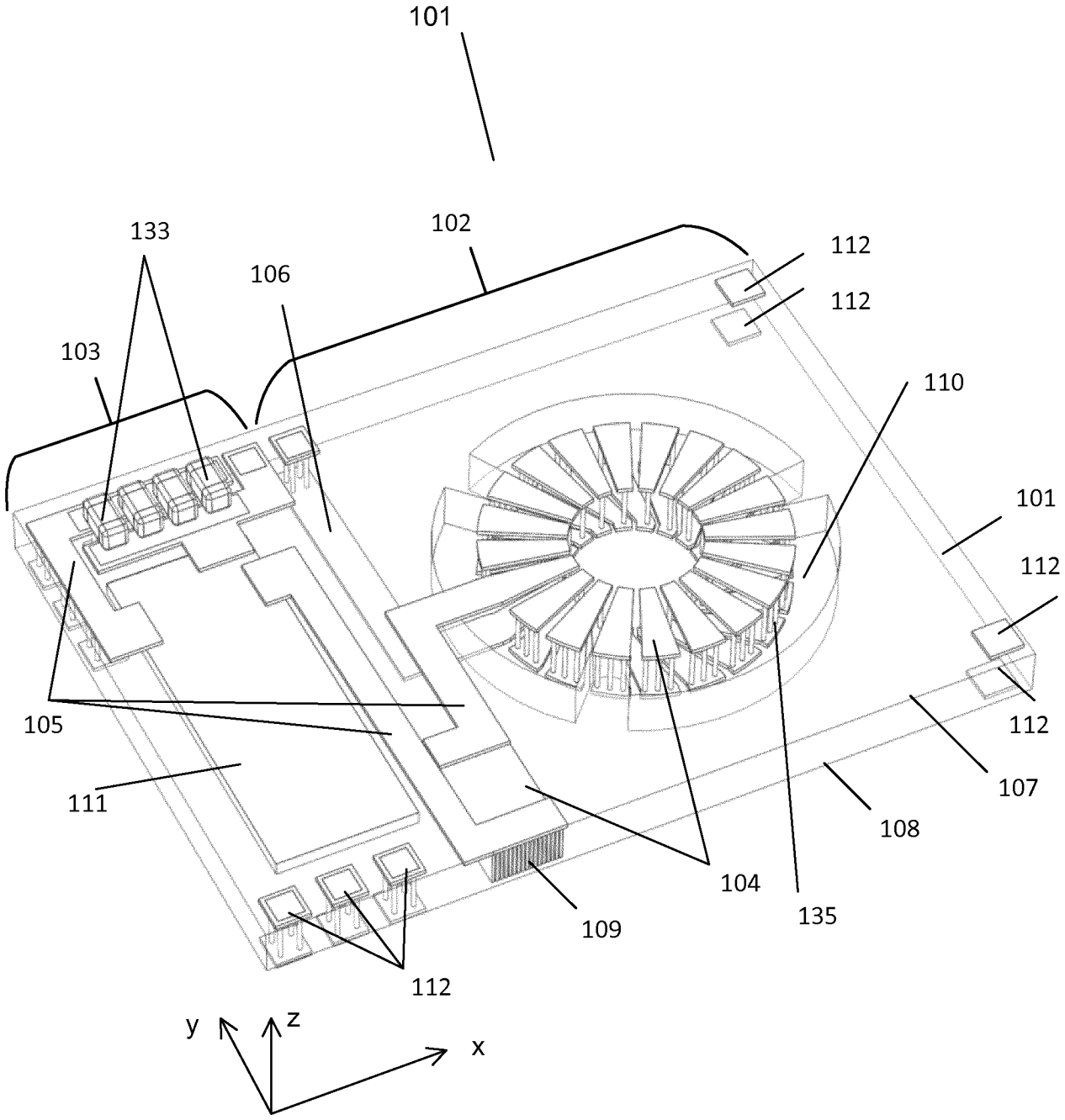
x

Fig. 1


101
133
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112
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Fig. 2

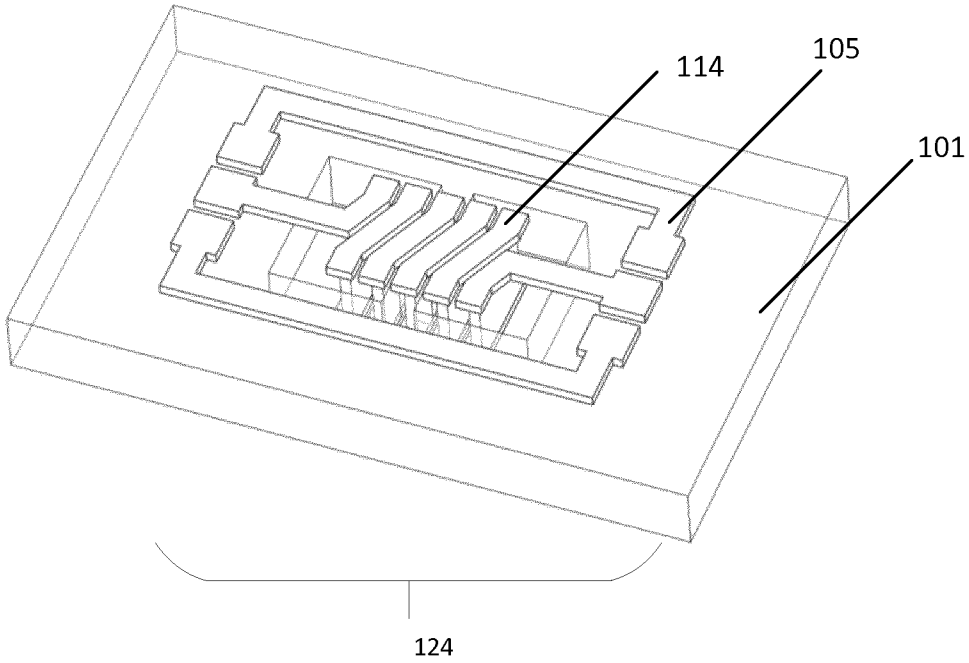


Fig. 3

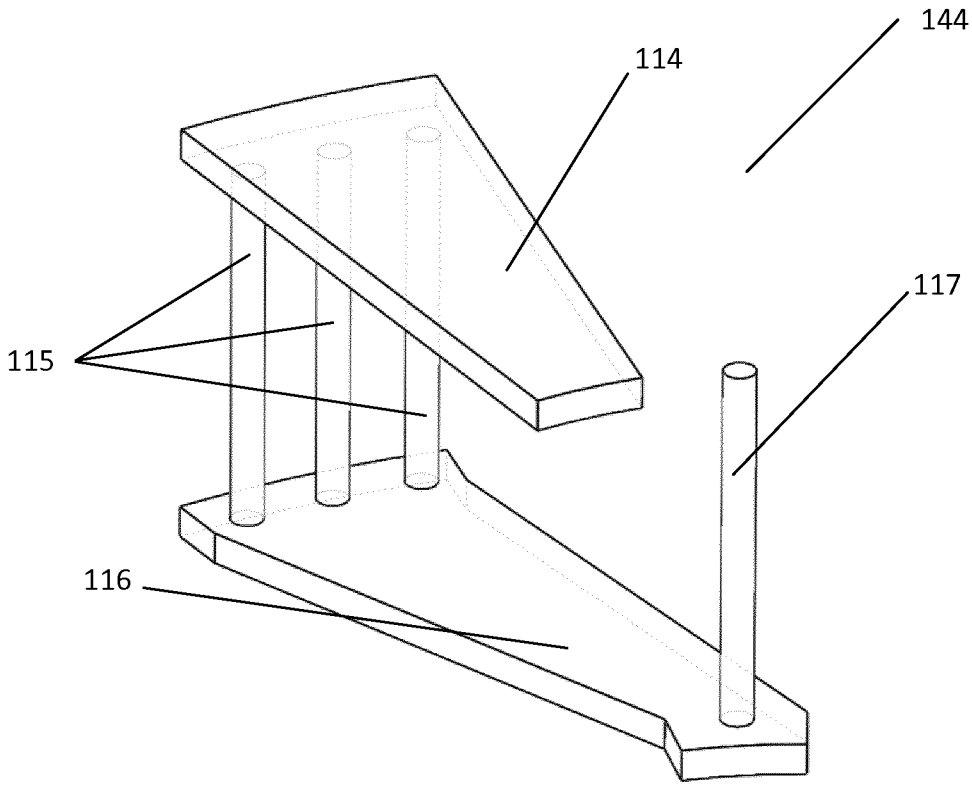


Fig. 4

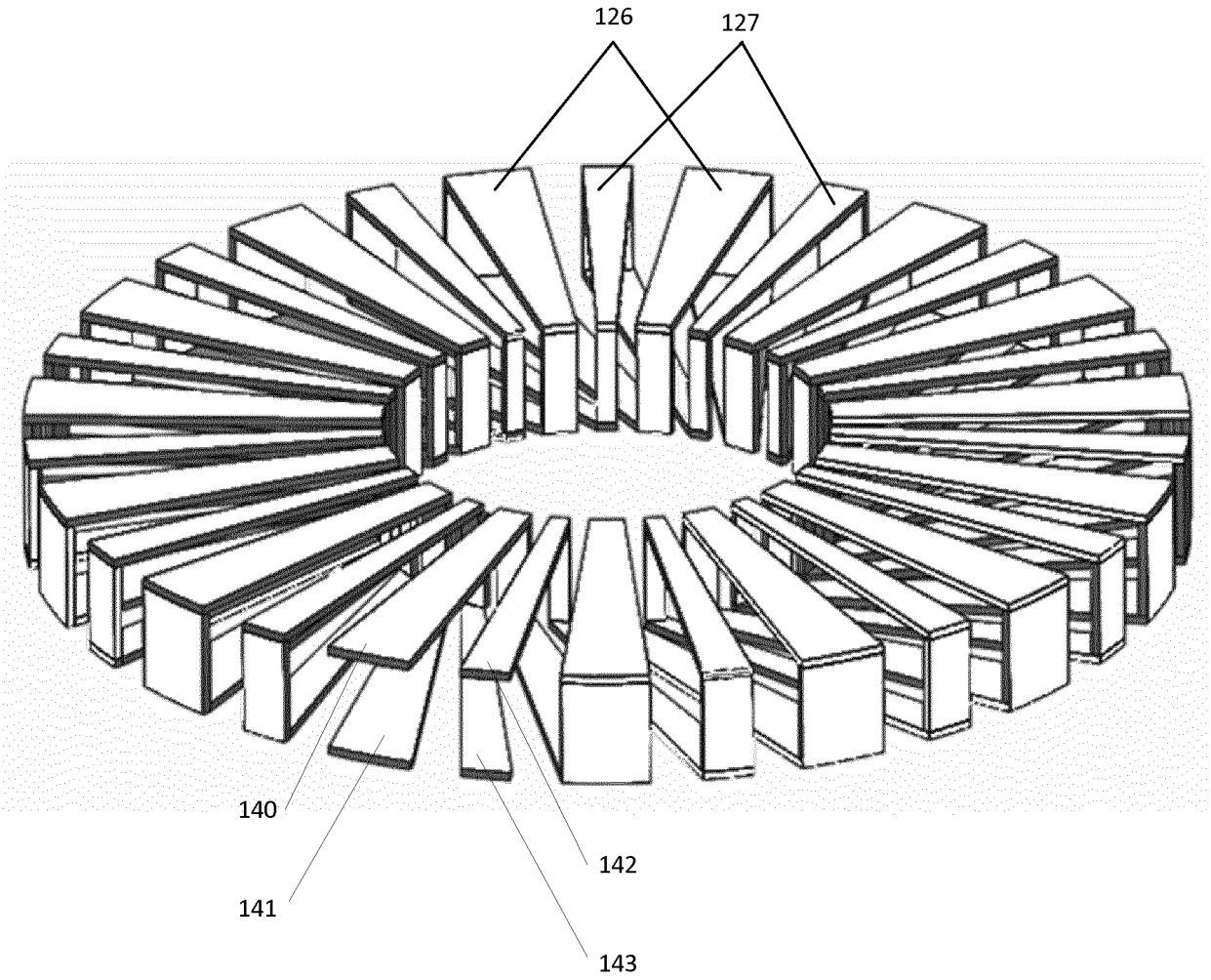


Fig. 5

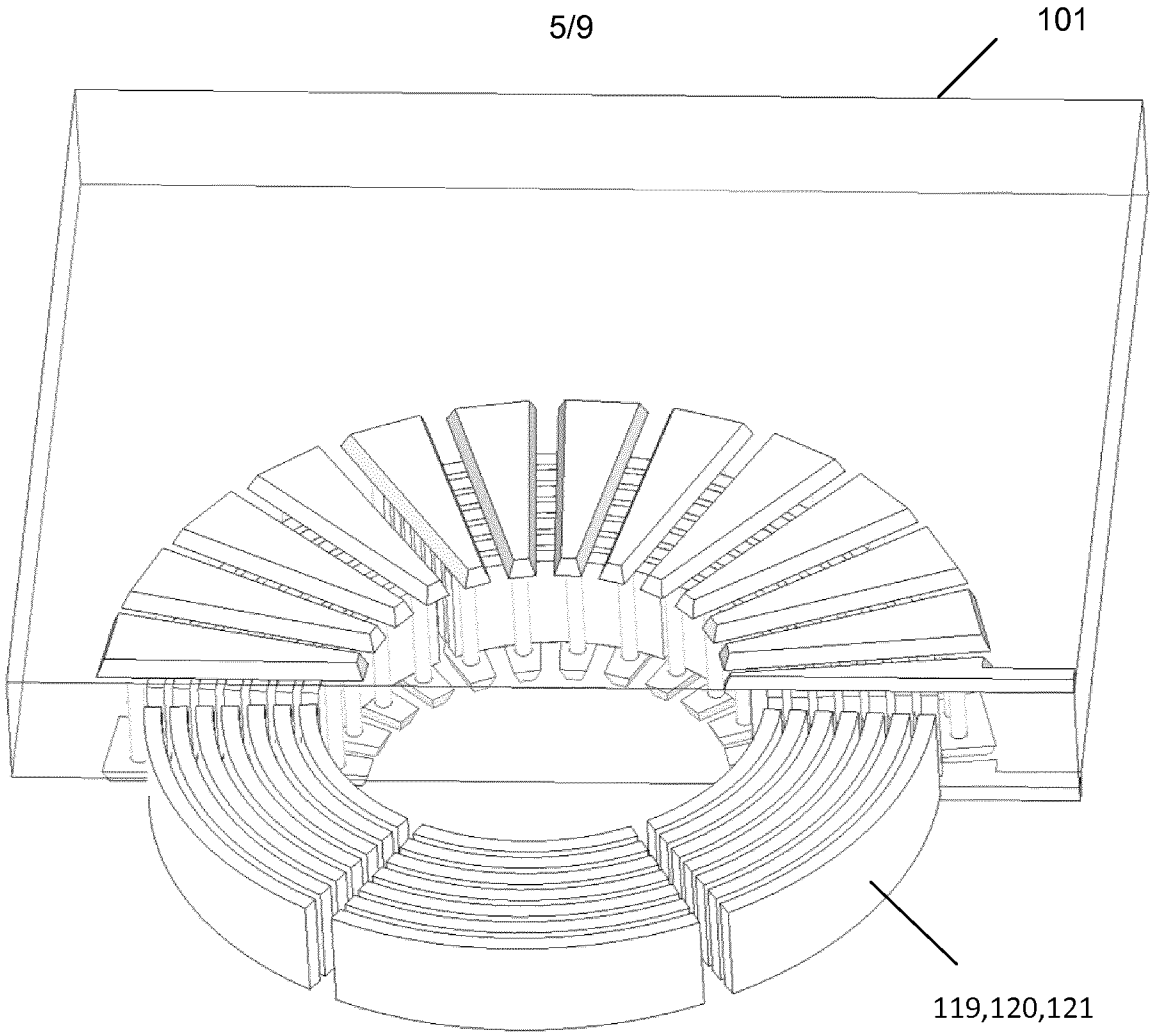


Fig. 6

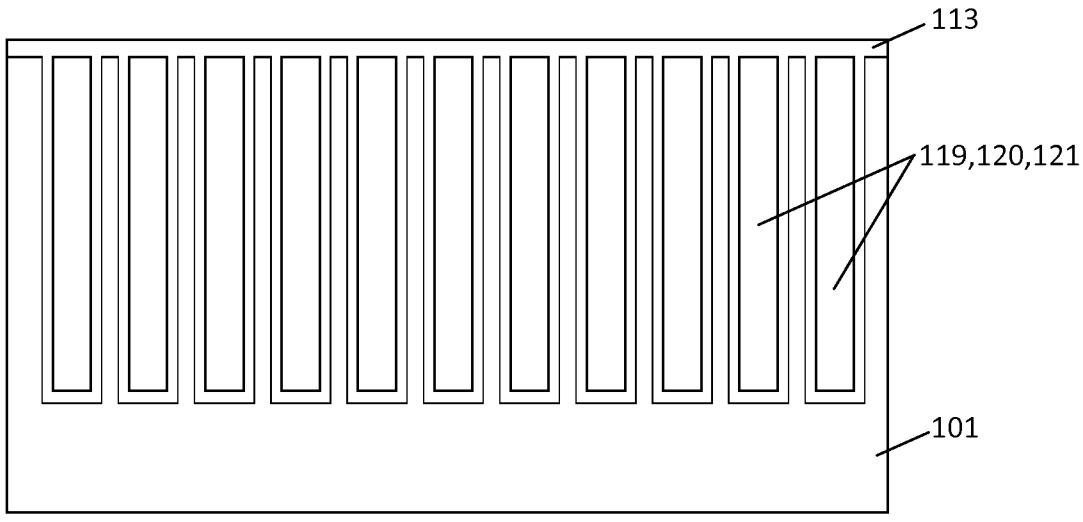


Fig. 7

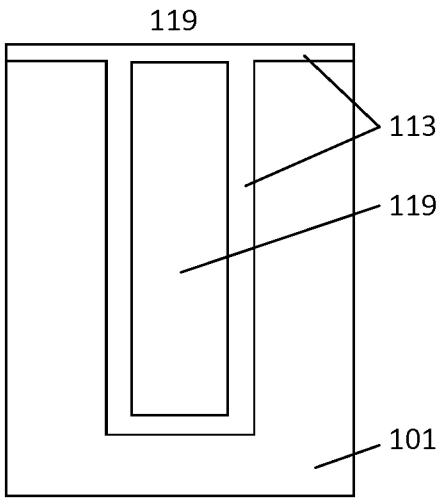


Fig. 8

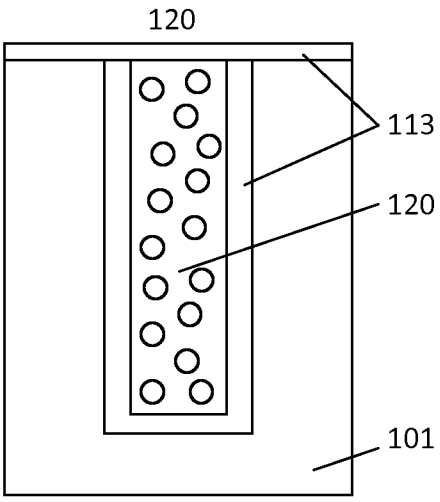


Fig. 9

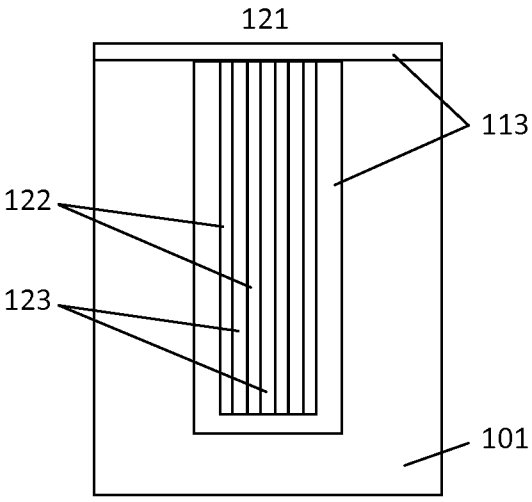
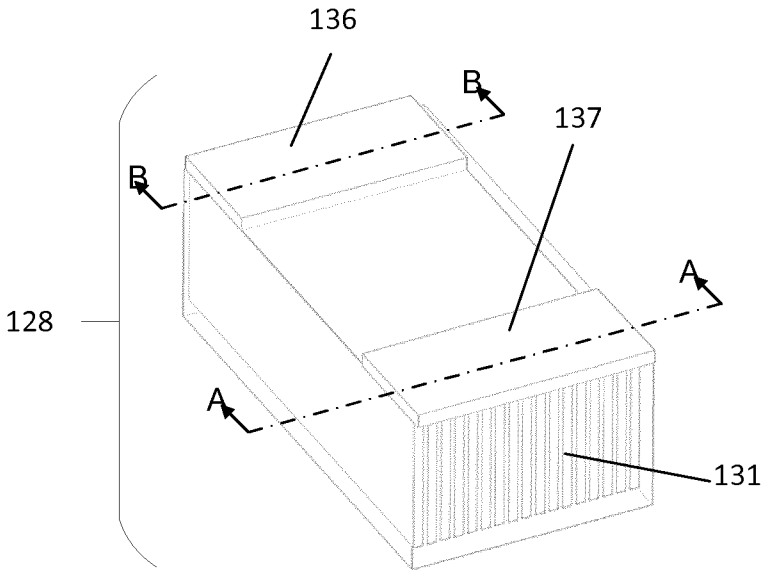
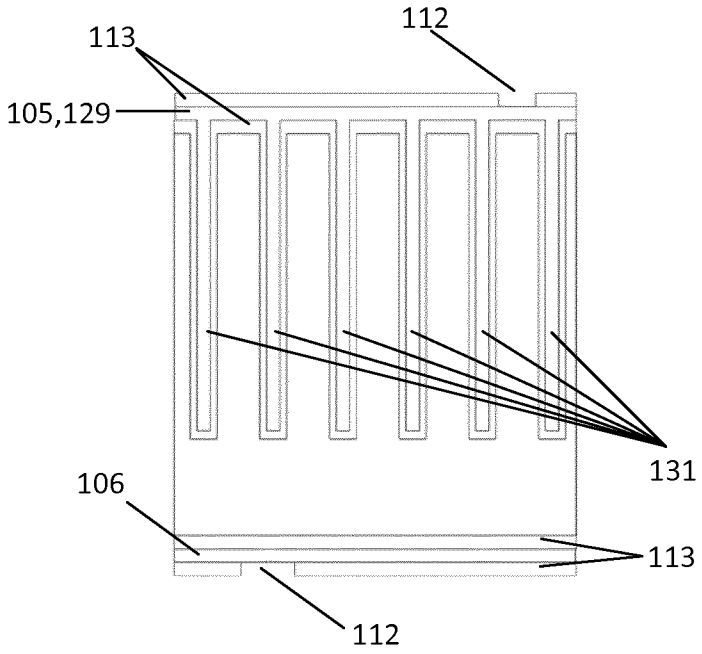
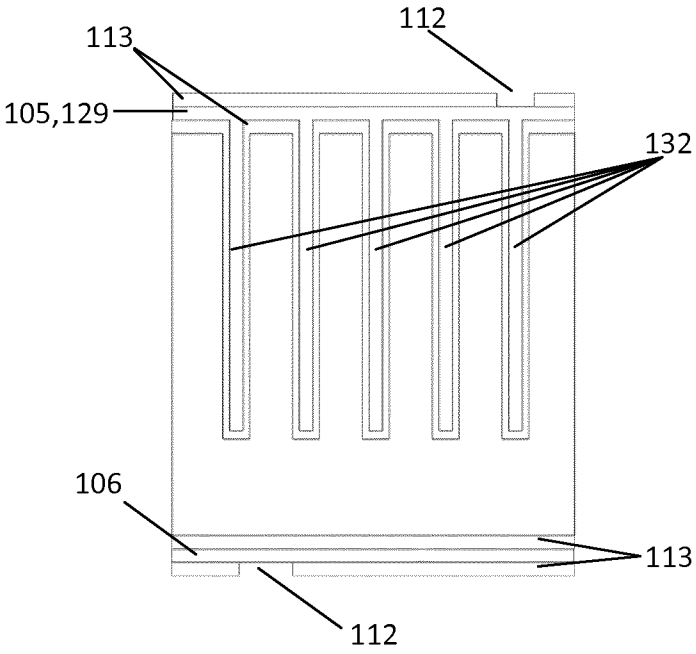


Fig. 10





Section A-A



Section B-B

Fig. 11

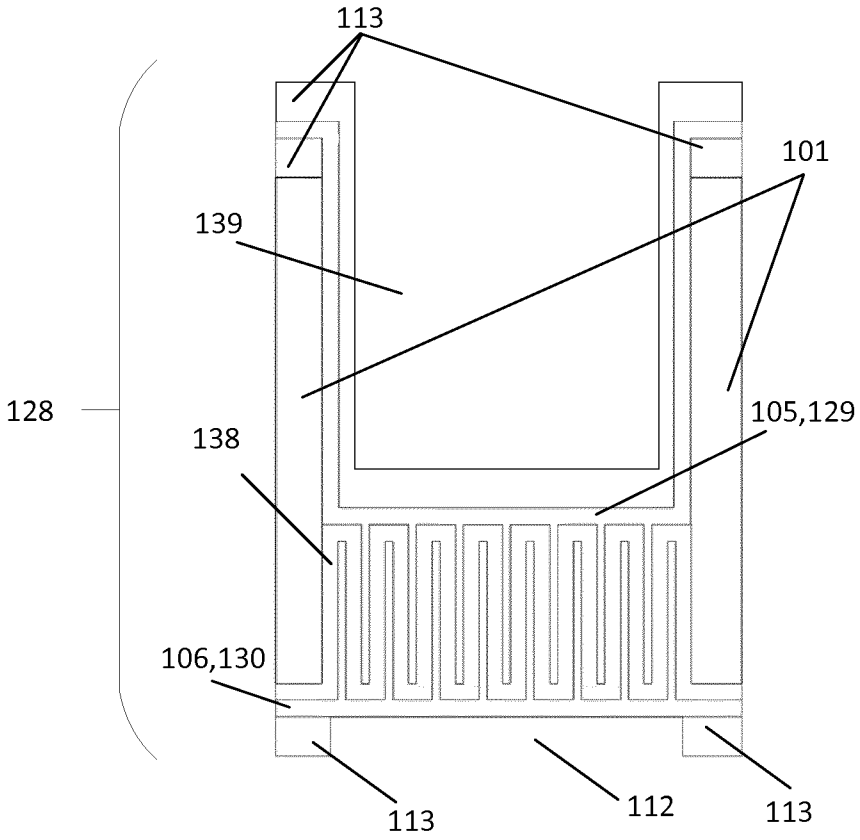


Fig. 12

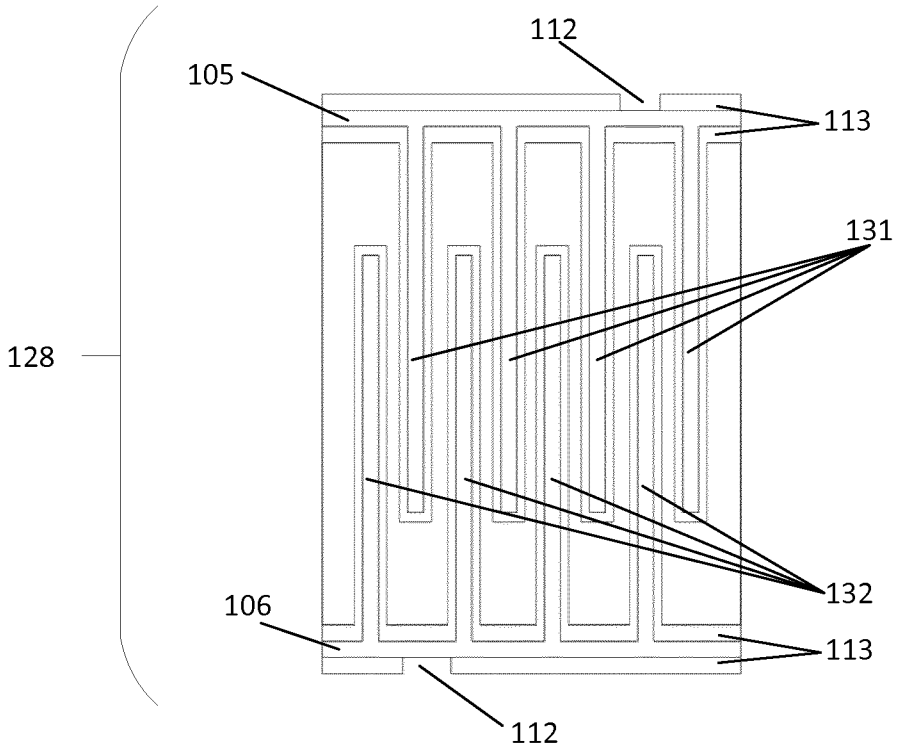


Fig. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/053302

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01F27/28 H01F27/255 H01F17/02 H01F17/04 H01F17/06
H01F17/00 H01F27/34 H01L23/52 H01L27/08 H01L49/02
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01F H01L H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2011/285302 A1 (CHOUTOV DMITRI A [US] ET AL) 24 November 2011 (2011-11-24) paragraphs [0007], [0012] - [0016], [0028], [0030], [0033] - [0038], [0041], [0042], [0045], [0046] -----	1-7, 13-15 16
X A	US 2015/303888 A1 (YEN HSIAO-TSUNG [TW] ET AL) 22 October 2015 (2015-10-22) abstract paragraphs [0009], [0030] - [0036], [0039] - [0042], [0056], [0060], [0078], [0086] -----	1-4,6,14 7,13,15, 16
A	US 2013/187255 A1 (WANG MINGLIANG [US] ET AL) 25 July 2013 (2013-07-25) paragraphs [0016] - [0020], [0022], [0026] - [0029], [0031] - [0033] -----	1-7, 13-16

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 March 2019	23/05/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gols, Jan

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Lê Thanh et al.: "3D MEMS Air-core Inductor in a Very High Frequency Switched-Mode Power Converter", Abstract from 43rd International conference on Micro and Nano Engineering, 22 September 2016 (2016-09-22), XP055492663, ISBN: 978-0-494-76162-5 Retrieved from the Internet: URL:http://orbit.dtu.dk/files/140796541/Conf_MNE2017.pdf [retrieved on 2018-07-16] the whole document	1-7, 13-16
A	HOA THANH LE ET AL: "Fabrication of 3D air-core MEMS inductors for very-high-frequency power conversions", MICROSYSTEMS & NANOENGINEERING, vol. 4, 29 January 2018 (2018-01-29), page 17082, XP055492672, DOI: 10.1038/micronano.2017.82 figures 1-6,8	1-7, 13-16
Y	EP 2 479 890 A1 (HARMAN INT IND [US]) 25 July 2012 (2012-07-25)	16
A	paragraphs [0001], [0008], [0022], [0023], [0046]	1-7, 13-15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2019/053302

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-7, 13-16

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2019/053302

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011285302 A1	24-11-2011	US 2011285302 A1	24-11-2011
		US 2011285312 A1	24-11-2011
		WO 2011146427 A2	24-11-2011
US 2015303888 A1	22-10-2015	TW 201541598 A	01-11-2015
		US 2015303888 A1	22-10-2015
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		US 2013187255 A1	25-07-2013
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		CN 102611401 A	25-07-2012
		EP 2479890 A1	25-07-2012
		JP 5444321 B2	19-03-2014
		JP 2012151838 A	09-08-2012
		KR 20120084269 A	27-07-2012
		US 2012182069 A1	19-07-2012

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7, 13-16

   A semiconductor substrate member comprising an inductor.

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2. claims: 8-10

   A semiconductor substrate member comprising magnetic particles suspended in epoxy.

   ---

3. claim: 11

   A semiconductor substrate member comprising a first coil and a second coil circumscribing a common inductor core, wherein windings of the first coil and windings of the second coil are formed by the first electrically conductive layer pattern and the second electrically conductive layer pattern and through-substrate vias.

   ---

4. claim: 12

   A semiconductor substrate member comprising a first capacitor member which comprises a conductive material deposited in first deep trenches extending from a first side of the semiconductor substrate; and a second capacitor member which comprises a conductive material deposited in second deep trenches extending from a second side of the semiconductor substrate.
