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A 36 nW trimless voltage reference with low sensitivity to PVT variations

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Abstract—In this paper a trimless ultra-low-power voltage reference with low sensitivity to process, voltage and temperature (PVT) is presented. The design uses a cascaded proportional to absolute temperature (PTAT) voltage generator to produce a voltage independent of process and line variations. The voltage is compensated in temperature by using a temperature-dependent current-load that changes the bias point of the voltage generator. The voltage reference is simulated over PVT in a 28 nm FD-SOI process and a mean value of 386 mV with absolute accuracy of $\pm 3.8\%$ is found. Spread across process corners is 4.7% ($3\sigma/\mu$). Power consumption is 36 nW at 25°C and 0.8 V. Line sensitivity is better than $0.14\%/V$ and the worst temperature coefficient (T.C.) from 0°C to 60°C is $91.8\text{ ppm}/^\circ\text{C}$.

I. INTRODUCTION

The development of the Internet of Things, medical devices and sensors has been pushing the boundary of low-power and low-voltage integrated circuits. A crucial component of any integrated solution is a voltage reference and with the need for low power supply the conventional bandgap reference is no longer feasible [1]. This has attracted CMOS-based solutions that use adapted bandgap circuits such as [1] and [2] or use MOSFETs in weak inversion [3]–[6].

In general, CMOS based references suffer from process variations, especially due to the spread of the threshold voltage. This has classically been dealt with through trimming circuits, as is used in [4] and [5]. However, trimming often requires an additional manufacturing step, which increases the cost. It also assumes that the neighbouring circuits used for the trimming itself are functioning properly, which may not be a valid assumption depending on their starting conditions.

The authors in [1] presented a reverse bandgap reference with high accuracy but it utilizes a large area and the control scheme increases the complexity of the design.

In [5] a low-power reference with low sensitivity to PVT based on the averaging of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltages was presented. The reference has $\pm 2.1\%$ ($3\sigma/\mu$) accuracy without trimming, however, the averaging circuit used requires an off-chip capacitor, which is often not an available choice for space restricted circuits.

In this paper an ultra-low-power voltage reference based on MOSFETs in weak inversion and robust to PVT variations without trimming is presented. Process variations are minimized by using a PTAT voltage generator insensitive to threshold voltage spread. Temperature compensation is

achieved by introducing a temperature-dependent current on the output of the voltage generator, counteracting the PTAT behavior. The circuit is biased by a reference current which is stable across the power supply range, minimizing the effect of line variations. The reference operates from 0.8 V, does not use external components and occupies a low area. Section II details the operation principle of the circuit. Section III shows simulation results and Section V concludes the work.

II. OPERATION PRINCIPLE

The proposed voltage reference is shown in Fig. 1. The circuit is composed of a current reference, a PTAT voltage generator and an output stage that compensates the voltage reference over temperature and resistor variations. With the exception of the PMOS current mirrors $M_{P1} - M_{P6}$, which are in strong inversion, all transistors operate in weak inversion. The bulk of the NMOS transistors are connected to ground and of the PMOS transistors to their sources.

The drain current I_D of a MOSFET in weak inversion has an exponential relation to its gate voltage. From the EKV model it can be approximated as [7]:

$$\begin{aligned} I_D &= \\ K I_{D0} \exp\left(\frac{V_G - V_T}{\eta U_T}\right) \left(\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right)\right) \\ I_{D0} &= 2\eta\mu C_{ox} U_T^2 \\ U_T &= \frac{k_B}{q} T \end{aligned} \quad (1)$$

Where V_G , V_D and V_S are, respectively, the gate, drain and source voltages referred to the bulk, K is the transistor aspect ratio (W/L), I_{D0} is defined as a process parameter, μ the carrier mobility, C_{ox} the unit oxide capacitance, V_T the threshold voltage, η the slope factor, U_T the thermal voltage, k_B the Boltzmann constant, q the elementary charge and T temperature.

For $V_D > 4U_T$, the transistor is assumed to be saturated and the drain current dependence on V_D can be neglected. In this case, the gate voltage is

$$V_G = V_T + \eta U_T \ln\left(\frac{I_D}{I_{D0} K \exp(-V_S/U_T)}\right) \quad (2)$$

Fig. 1. Schematic of the voltage reference circuit proposed.

A. Current reference

The current reference has the purpose of biasing the transistors in the circuit and making it robust to power supply variations. As will become clear in section II-C, the absolute value of the reference current is not crucial, but it is important that its behavior over temperature and process corners is predictable.

The core of the current reference is composed of M_{B1} , M_{B2} and R_1 (Fig 1). The voltage across R_1 , V_{R1} , can be calculated by using the relation $V_{G,B1} = V_{G,B2}$. From (2) and noticing that $V_{S,B1} = 0$ and $V_{S,B2} = V_{R1}$,

$$\begin{aligned} V_{T,B1} + \eta U_T \ln \left(\frac{I_{D,B1}}{I_{D0} K_{B1}} \right) = \\ V_{T,B2} + \eta U_T \ln \left(\frac{I_{D,B2}}{I_{D0} K_{B2} \exp(-V_{R1}/U_T)} \right) \end{aligned} \quad (3)$$

To minimize threshold voltage mismatch due to geometrically different devices [8], the transistors are designed with the same aspect ratio and number of fingers. To achieve a different effective ratio between the two, a different number of devices in parallel is chosen for each. For a small value of $V_{S,B2}$, $V_{T,B1} \approx V_{T,B2}$ and V_{R1} can be derived from (3). Making $I_{REF} = V_{R1}/R_1$,

$$I_{REF} = \frac{U_T}{R_1} \ln \left(\frac{K_{P1} K_{B2}}{K_{P2} K_{B1}} \right) \quad (4)$$

The result in (4) shows that the reference current is proportional to U_T , and thus to temperature, but is independent of power supply variations and MOSFET corners. It is, however, subject to resistor variations, which will be discussed later in the design.

B. PTAT voltage generator

Fig. 2a shows two MOSFET in series on a diode-connected configuration where their bulks are connected to ground. By biasing M_1 and M_2 in weak inversion, a voltage proportional to the thermal voltage U_T can be generated [9]. Assuming that the transistors are matched, V_{PTAT} can be derived from (1) by making $V_{G,1} = V_{G,2}$,

$$V_{PTAT} = U_T \ln \left(\frac{I_{D,1} K_2}{I_{D,2} K_1} + 1 \right) \quad (5)$$

If the circuit has no output current, $I_{D,1} = I_{D,2}$ and the current ratio can be cancelled.

It is also possible to increase the generated voltage by cascading the circuit, as shown in Fig. 2b. In this case, the output voltage of n stages, $V_{PTAT}(n)$, is the sum of the voltages of each stage. If the ratio between the odd and even-numbered transistors is such that $I_{odd} K_{even} / I_{even} K_{odd} \gg 1$, the output voltage is given by (6).

$$\begin{aligned} V_{PTAT}(n) = \\ U_T \ln \left(\frac{I_{D,1} I_{D,3} \dots I_{D,(2n-1)}}{I_{D,2} I_{D,4} \dots I_{D,(2n)}} \frac{K_2 K_4 \dots K_{2n}}{K_1 K_3 \dots K_{2n-1}} \right) \end{aligned} \quad (6)$$

Fig. 2. PTAT voltage generator.

C. Output compensation

A closer look at (6) suggests that it should be possible to compensate the temperature dependence of the PTAT voltage generator if the term inside the logarithm had a complementary relation to temperature. If this relation were in the form of an exponential function of the inverse of temperature, as shown in (7), where C is a positive constant, it would be cancelled out entirely. Substituting (7) in (6) leads to (8).

$$\frac{I_{D,1} I_{D,3} \dots I_{D,(2n-1)}}{I_{D,2} I_{D,4} \dots I_{D,(2n)}} \frac{K_2 K_4 \dots K_{(2n)}}{K_1 K_3 \dots K_{(2n-1)}} = \exp \frac{C}{U_T} \quad (7)$$

$$V_{PTAT}(n) = C \quad (8)$$

One way to achieve this is to load the output of the voltage generator $V_{PTAT}(n)$ with a temperature-dependent compensating current, I_{COMP} . This way it is possible to control the odd-numbered currents and the current ratio in (7). If the currents $I_1, I_2, \dots, I_n$ are proportional to the reference current I_{REF} (4), there are a few observations to be made about I_{COMP} . First, it cannot be a multiple of I_{REF} as the current ratio would then be constant in temperature. Second,

since I_{REF} depends on R_1 , it follows that I_{COMP} also needs to compensate for resistor process variations.

To generate I_{COMP} the output compensation circuit of Fig. 3 is proposed. In its core, it is the same topology as the one used for the current reference, however, M_{C2} is biased so that $V_{D,C2} < 4U_T$. In this way, the drain current dependence on the drain-bulk voltage can be used and $V_{G,C2}$ is given by (9). It can then be shown that I_{COMP} is defined by (10).

Fig. 3. Output compensation subcircuit

$$V_{G,C2} = V_T + \eta U_T \ln \left(\frac{I_{D,C2}}{I_{D0} K_{C2} \left(\exp \left(-\frac{V_{S,C2}}{U_T} \right) - \exp \left(-\frac{V_{D,C2}}{U_T} \right) \right)} \right) \quad (9)$$

$$I_{COMP} = \frac{2U_T}{R_2} \ln \left(\frac{K_{C2} K_{C3}}{K_{C1} K_{C4} + K_{C2} K_{C3} \exp \left(-\frac{V_{D,C2}}{U_T} \right)} \right) \quad (10)$$

To understand how I_{COMP} compensates $V_{PTAT}(n)$ in temperature, consider the specific case where the voltage generator only has one stage ($n = 1$) and $I_1 = I_{REF}$. Combining (5), (4) and (10) results in an expression for $V_{PTAT}(1)$, shown in (11a) and (11b).

$$V_{PTAT}(1) = U_T \ln \left(\frac{K_2}{K_1} \left(\frac{I_{REF} - I_{COMP}}{I_{REF}} \right) \right) = \quad (11a)$$

$$U_T \ln \left[\frac{K_2}{K_1} \left(1 + \frac{2R_1}{R_2} \frac{\ln \left(\frac{K_{C1} K_{C4}}{K_{C2} K_{C3}} + \exp \left(-\frac{V_{D,C2}}{U_T} \right) \right)}{\ln \left(\frac{K_{B2} K_{P1}}{K_{B1} K_{P2}} \right)} \right) \right] \quad (11b)$$

Equation (11b) is not fully simplified as $V_{D,C2}$ depends on the output voltage itself as well as the gate-bulk voltage of M_{C4} , as shown in (12). The analysis including these considerations does not result in an intuitive understanding of the system and an explicit solution is overly complicated. However, the design can be made by understanding what contributes to compensating the voltage reference in corners and temperature.

$$\begin{aligned} V_{D,C2} &= V_{PTAT}(1) - V_{G,C4} \\ &= V_{PTAT}(1) - \left(V_T + \eta U_T \ln \left(\frac{I_{COMP}}{2I_{D0} K_{C4}} \right) \right) \end{aligned} \quad (12)$$

TABLE I
PARAMETERS OF THE PROPOSED VOLTAGE REFERENCE.

Component	W/L (μm/μm)	Component	W/L (μm/μm)
M_1	0.7/0.7	M_{B2}	10/1, m = 3
M_2	14/0.7	M_{B3}	20/1
M_3	0.7/0.7	M_{B4}	20/1
M_4	14/0.7	M_{P1}	0.8/2
M_5	0.7/0.7	M_{P2}	0.8/2
M_6	14/0.7	M_{P3}	0.2/2
M_7	0.7/0.7	M_{P4}	0.2/2
M_8	14/0.7, m = 4	M_{P5}	0.2/2
M_{C3}	40/0.3	M_{P6}	0.4/2
M_{C4}	40/0.3		
M_{C1}	1/0.5, m = 10	Component	Resistance (Ω)
M_{C2}	1/0.5, m = 14	R_1	800k
M_{B1}	10/1, m = 2	R_2	2.5M

By sizing M_{C4} , it is possible to choose $V_{G,C4}$ so that $V_{D,C2} < 4U_T$. Furthermore, considering that V_T decreases with temperature [8] and that it dominates the variations of (12), $V_{D,C2}$ itself is PTAT. This causes the term inside the logarithm of (11a) to decrease with temperature, which was the objective of using I_{COMP} . The circuit does not directly match the proposal of (8) but it provides a compensation in temperature that can be adjusted by changing the bias point of $V_{D,C2}$, the currents I_{REF} and I_{COMP} as well as the number of stages of the PTAT voltage generator. The circuit is also fairly robust to resistor variations as long as the ratio between R_1 and R_2 is maintained. It can be noted, however, that $V_{D,C2}$ also has a minor dependence on R_2 .

D. Proposed voltage reference

The concept was implemented in a 28 nm FD-SOI process using a 4-stage PTAT voltage generator as shown in Fig. 1. The number of stages was chosen to provide enough bias voltage for the output compensation subcircuit while also leaving enough room for the PTAT generator and the PMOS current mirrors in the lowest power supply. The components' parameters are listed on Table I and V_{REF} is derived from (6) for $n = 4$, as shown in (13). The odd-numbered currents in the equation depend on I_{COMP} .

$$V_{REF} = U_T \ln \left(\frac{I_{D,1} I_{D,3} I_{D,5} I_{D,7} K_{ratio}}{I_{REF}^4} \right) \quad (13)$$

$$K_{ratio} = \frac{K_{P2}^4}{K_{P3} K_{P4} K_{P5} K_{P6}} \frac{K_2 K_4 K_6 K_8}{K_1 K_3 K_5 K_7} \quad (14)$$

Figs. 4 and 5 show how the resistor values can be used to change the current ratios of (13) and adjust V_{REF} 's compensation over temperature. By making R_1 smaller, I_{REF} gets larger, effectively decreasing the compensation factor over temperature and resulting in a PTAT behavior. In an analogous way, by increasing R_1 , the voltage reference shows a CTAT behavior. The opposite is true for R_2 and I_{COMP} , since the larger I_{COMP} the smaller the term inside the logarithm of (13).

Fig. 4. Voltage reference variation with R_1 over temperature in the typical corner (TT).

Fig. 5. Voltage reference variation with R_2 over temperature in the typical corner (TT).

III. SIMULATION RESULTS

The reference voltage was simulated over temperature and power supply as shown in Figs. 6 and 7. Table II shows the specifications of the corners selected. The MOSFET corners FFA, FSA, SFA and SSA are corners provided by the process used that have a higher spread than the traditional corners FF, FS, SF and SS. The resistor and, in the case of the simulation over temperature, power supply values were chosen to match the worst case scenario of the MOSFET corners.

For Fig. 6, the worst spread in terms of absolute value is $\pm 3.8\%$ which occurs between SSA at 60°C and FFA at 60°C . The T.C. varies from $20.6\text{ ppm}/^\circ\text{C}$ on the typical case to $91.8\text{ ppm}/^\circ\text{C}$ in the SSA corner. The line sensitivity of the reference voltage can be seen in Fig. 7 where the simulation was made at 25°C and a worst variation of $0.14\%/V$ was obtained for the SFA corner. Power consumption on the typical corner at 25°C and 0.8 V is 36 nW . For the worst corner at 60°C and 1.8 V the consumption is 111 nW .

Finally, Monte Carlo simulations including global (die-to-die) and local (inter-die, i.e. mismatch) variations were made at 25°C and a supply of 1.25 V . The results are shown in Fig. 8, where a spread of 4.7% ($3\sigma/\mu$) was achieved.

TABLE II
CORNER SPECIFICATIONS FOR FIGS. 6 AND 7

MOSFET Corner	Resistor	$V_{DD}(\text{V})$ (only Fig. 6)
FFA	max	0.8
FSA	min	1.8
SFA	max	0.8
SSA	min	1.8
TT	typical	1.25

Fig. 6. Voltage reference as a function of temperature across PVT variations.

Fig. 7. Voltage reference as a function of power supply across PVT variations.

Fig. 8. Monte Carlo simulation results for 800 samples with global and local variations at 25°C and $V_{DD} = 1.25\text{ V}$.

TABLE III
COMPARISON TO RELATED LOW-POWER VOLTAGE REFERENCES

	This Work	V. Ivanov et al 2012 [1]	K. Ueno et al 2009 [3]	Y. Osaki (subbandgap) 2013 [2]	Y. Wang et al 2015 [4]	N. Modak et al 2015 [5]	A. C. de Oliveira 2017 [6]
Technology	28 nm FD-SOI	0.13 μm	0.35 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Temperature [$^{\circ}\text{C}$]	0 - 60	-20 - 85	-20 - 80	-40 - 120	-40 - 125	-25 - 100	0 - 125
Supply Voltage [V]	0.8 - 1.8	0.75 (min)	1.4 - 3	0.7 - 1.8	0.45 - 1.8	0.8 - 1.8	0.45 - 3.3
Power Consumption [nW]	36 @ 0.8 V	170	300 @ 1.4 V	52.5	14.6	120 @ 0.8 V 300 @ 1.8 V	0.093
Voltage reference [mV]	386	256	745	548	118.46	231.5	248
Accuracy untrimmed ($3\sigma/\mu$) [%]	4.7	11.7	21.4	4.83	11.4	2.1	21.8
Accuracy trimmed ($3\sigma/\mu$) [%]	-	1.9	-	-	1.8	-	-
T.C. [ppm/ $^{\circ}\text{C}$]	20.6 - 91.8	40 (typical)	7 - 45	114	25 - 250	7 - 45	7
Line Sensitivity [%/V]	0.14	-	0.002	-	1.01	0.18	0.217
Area [mm^2]	0.002 (estimated)	0.07	0.055	0.0246	0.012	0.023	0.002

IV. DISCUSSION

Table III shows the performance comparison to related low-power voltage references. In order to correlate the proposed voltage reference's robustness to process variations, accuracy was defined as the deviation $3\sigma/\mu$ obtained from Monte Carlo simulations considering global and local variations, except for [4] where deviation in measured samples is shown instead. The untrimmed accuracy of the voltage reference is among the best reported. Area, albeit estimated, is comparably small. Power consumption is also among the lowest, making the reference desirable for low-power and low-area applications.

V. CONCLUSION

A low-voltage ultra-low-power trimless voltage reference was presented and simulated in a 28 nm FD-SOI process. To reduce the circuit's sensitivity to PVT variations, the design is based on compensating a process insensitive PTAT voltage generator in temperature. This is done by using a temperature-dependent compensating current to bias the output of the voltage generator. The compensating current is adjusted by using the drain current dependence on the drain and source voltages of a MOSFET in weak inversion. Simulated results show an absolute accuracy over PVT of 3.8% and a spread of 4.7% ($3\sigma/\mu$) over global and local process variations.

REFERENCES

- [1] V. Ivanov, R. Brederlow, and J. Gerber, "An ultra low power bandgap operational at supply from 0.75 V," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1515–1523, July 2012.
- [2] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, June 2013.
- [3] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15 ppm/ $^{\circ}\text{C}$, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold mosfets," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, July 2009.
- [4] Y. Wang, Z. Zhu, J. Yao, and Y. Yang, "A 0.45-V, 14.6-nW CMOS subthreshold voltage reference with no resistors and no BJTs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 7, pp. 621–625, July 2015.
- [5] N. Modak, B. Chatterjee, A. Anvesha, and M. S. Baghini, "A 120 nW, tunable, PVT invariant voltage reference with 80 dB supply noise rejection," in *2015 IEEE International Symposium on Nanoelectronic and Information Systems*, Dec 2015, pp. 181–184.
- [6] A. C. de Oliveira, D. Cordova, H. D. Klimach, and S. Bampi, "A 0.45 V, 93 pW temperature-compensated CMOS voltage reference," in *2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS)*, Feb 2017, pp. 1–4.
- [7] C. Enz and E. Vittoz, "Charge-based MOS transistor modeling : The EKV model for low-power and RF IC design," August 2006.
- [8] N. H. E. Weste and D. Harris, "CMOS VLSI design a circuits and systems perspective," 2005.
- [9] E. A. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 3, pp. 573–579, June 1979.