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Analysis and Optimal Design of High Frequency and High Efficiency Asymmetrical Half-Bridge Flyback Converters

Mingxiao Li, Student Member, IEEE, Ziwei Ouyang, Senior Member, IEEE and Michael A.E. Andersen, Member, IEEE

Abstract—The asymmetrical half-bridge (AHB) flyback converter is capable to achieve zero voltage switching (ZVS) and has lower voltage stress compared to the active clamp flyback converter (ACF). This topology gives much margin for components selection and transformer turns ratio design. It is well adapted to voltage step-down applications. However, the optimal design for AHB flyback converter taking current dip effect causing by components parasitic capacitances, and each component effect to power loss into consideration has never been explored. This paper gives detailed operation and mathematical analyses of this effect. The optimal design procedure with the consideration of each circuit parameter is presented in this paper. The transformer benefits low power loss from interleaving winding layout. A 56W/inch³ 1MHz 65W prototype with 100V-250V input is built to verify the feasibility of the converter. Experimental results show the peak efficiency 96.5% is achieved with 127V input and the whole system efficiency under the entire input voltage range is above 93%.

Index Term—AHB flyback converter, high efficiency, voltage step down applications

I. INTRODUCTION

With the increasing demand for size reduction and high power density, high frequency operation provides a way to achieve these goals. The emerging gallium nitride (GaN) devices open the door for Megahertz (MHz) range switching frequency operation. GaN devices show better performance than silicon MOSFETs under a similar voltage and current ratings, such as smaller output capacitance, lower gate charge and smaller package. Thus GaN devices can be applied to a considerably high frequency converters design [1]-[6].

Among many DC/DC converters, flyback converters have been widely used in many applications, such as switching mode power supplies, adaptors for tablets and smartphones, PV systems, etc. However, traditional flyback converter operating at hard switching mode cannot reach high efficiency at high frequency. Both voltage and current stress are very high due to the energy stored in transformer leakage inductance. The conventional passive clamping method helps reduce the leakage energy by using the clamp resistor. This reduces the switch voltage stress, but the efficiency is not improved. Active clamp flyback converters have been proposed in [6]-[8] to fully utilize the leakage energy to achieve soft-switching. It has been proved to achieve high efficiency at high frequency. Many publications have done excellent works on ACF design [9]-[17]. However, the high voltage stress for ACF is still a problem. It poses obstacles to components selection and transformer design.

The AHB flyback converter has lower voltage stress compared to ACF and is also capable to achieve soft-switching, which is gaining popularity. It can achieve strong output voltage regulation through PWM control, which is the same with ACF. On the other hand, LLC is not suitable to be used in the applications with a wide input voltage range, whose regulation capability relies on the small inductance ratio of magnetizing inductance to resonant inductance. A large resonant inductor is required, leading to small power density and low efficiency. This topology is not considered in this paper.

Many publications have done excellent analyses on AHB flyback converter. It can be regarded as a buck converter with a transformer [18]-[23]. Thus it is well adapted to voltage step-down applications. The switching loss is reduced and a larger margin for components selection and turns ratio design are given. Detailed operating principles can be found in [18][20][22]. The hybrid-switching technique is proposed in [23] to achieve ZVS for primary switches and ZCS for the secondary rectifier. However, ZCS realization relies on the resonance between the resonant inductor and resonant capacitor. It leads to high primary and secondary RMS current. Detailed analysis can be found in this paper. Literature [24] gives conventional analysis and design procedure for AHB flyback converter, but the current dip effect is not considered. It affects primary and secondary RMS current.

To obtain soft-switching properties, capacitances of switches are always taken into consideration, as many publications have explored [19][20][24][25]. However, the current dip effect due to the current shared by the primary and secondary capacitances has never been mentioned or investigated in optimal design procedure for AHB flyback converters. At Mega Hz operation, they are of great importance to design a high performance converter. This paper gives detailed analyses of the current dip effect due to the current shared by the primary and secondary capacitances, which affects both primary and secondary RMS current and further power loss. This effect can be used to select primary and secondary switches. The flux cancellation in the transformer is first mentioned in this paper. The AHB flyback converter benefits low winding loss from interleaving winding layout. Additionally, the impact of the resonant capacitor on primary and secondary RMS current and the optimal magnetizing inductance design with the consideration of power loss are investigated. An optimal design procedure is given and iterations are then conducted to select the turn ratio with minimum power loss. The half-turn winding paralleled concept proposed in [26] is adopted to minimize the transformer AC resistance.

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This paper is organized as follows: Section II gives the detailed operating principle and analyses of the current dip effect along with mathematical equations and waveforms. A comparison of the traditional ACF and the AHB flyback converter is also illustrated. The optimal design procedure is described in Section III. A 56W/inch\(^3\) 1MHz 65W with peak efficiency 96.5% prototype is demonstrated in Section IV. Section V concludes this paper.

II. ANALYSES OF THE AHB FLYBACK CONVERTER

Two configurations of the AHB flyback converter are illustrated in Fig.1 (a) and Fig.1 (b), respectively. \(Q_1\) and \(Q_2\) form a half-bridge configuration. The switch node is connected to the transformer and the resonant capacitor. The switch \(Q_1\) toggles complementarily concerning \(Q_2\). Thus the voltage stress on \(Q_1\) and \(Q_2\) is always clamped by the input voltage, regardless of the transformer turns ratio and output voltage. Waveforms of the proposed converter operating close to the CCM/DCM mode boundary is shown in Fig.2. Since the operating principles of these two configurations are identical, only the Fig.1(a) is analyzed. Both steady-state and operating principles analyses of this topology are discussed in this section.

A. Steady-state analyses

To analyze this circuit, the following assumptions are made:

- The output voltage \(V_o\) is a constant value.
- The resonant inductance \(L_r\) is much smaller than the magnetizing inductance \(L_m\).
- Conduction power losses of all switches are neglected.
- The resonant capacitor \(C_r\) can be taken as a constant voltage source.
- The conduction times for \(Q_1\) and \(Q_2\) are \((1-D)T_s\) and \(DT_s\), respectively, where \(D\) is the duty cycle for \(Q_2\) and \(T_s\) is the switching period. Dead time is neglect in the steady-state analysis.

Based on the assumptions mentioned above, the voltage transfer ratio \(V_o/V_{in}\) and the voltage across the resonant capacitor \(V_{cr}\) can be obtained when voltage second balance is applied to magnetizing inductance \(L_m\). When the bottom switch \(Q_2\) turns on, the voltage across the transformer primary winding is \(V_{in}-V_{cr}\) and \(Q_1\) is clamped by the input voltage \(V_{in}\). In the next time interval, \(Q_2\) turns off while \(Q_1\) turns on. The voltage applied to the transformer primary winding becomes \(-V_{cr}\). \(Q_2\) is clamped by the input voltage \(V_{in}\). Apply voltage second balance on magnetizing inductance and the voltage across the resonant capacitor can be expressed by

\[
D\left(V_{in} - V_{cr}\right) = V_{cr} \left(1 - D\right)
\]

\[
V_{cr} = V_{in}D
\]  

The converter is operating close to the CCM/DCM boundary with the relatively small magnetizing current. It has a negligible effect on (1). The voltage-second-balance law can still be used. The same approximation can be found in [14][24][25].

\(nV_o\) is applied to magnetizing inductance during the period when \(Q_1\) is on. If \(L_r\) cannot be ignored, \(V_{cr}\) should be expressed by

\[
V_{cr} = nV_o \left(1 + \frac{L_r}{L_m}\right)
\]

Based on the given assumption, \(L_r\) is much smaller than the magnetizing inductance \(L_m\). Thus \(V_{cr}\) is very close to the reflected output voltage \(nV_o\). The same approximation can be found in [14][24][25]. The voltage transfer ratio can be found in (2)

\[
D\left(V_{in} - V_{cr}\right) = nV_o \left(1 - D\right)
\]

\[
\frac{V}{V_{in}} = \frac{D}{n} \left(1 - D\right)
\]  

Then the voltage across secondary synchronous rectifier (SR) when \(Q_2\) turns on, \(V_{SR}\) can be found to be

\[
V_{SR} = \frac{V_o}{n}
\]

| TABLE I | COMPARISON BETWEEN TRADITIONAL ACF AND AHB FLYBACK |
| --- | --- | --- |
| | \(V_{SR}/V_{in}\) | \(V_{SR}/V_{in}\) | \(D/n(1-D)\) |
| ACF | \(V_{SR}/V_{in}\) | \(V_{SR}/V_{in}\) | \(D/n(1-D)\) |
| AHB Flyback | \(V_o\) | \(V_o/n\) | \(D/n\) |
The comparison between ACF and AHB flyback converter is shown in TABLE I. The voltage stresses for both primary and secondary switches are reduced, which offers much margin to select primary and secondary components and transformer turns ratio. It is also worthwhile to point out that the voltage stress for the primary main switch of ACF is higher than \( V_{in} + n V_o \) due to the voltage across the leakage inductance. On the other hand, that for the AHB flyback converter is always clamped by the input voltage \( V_{in} \). This provides a safe selection for primary switches. More importantly, since there is no 1-D in the denominator of the voltage transfer ratio for the AHB flyback converter, it is more preferable to be used in voltage step down cases. In another word, the traditional ACF converter can be regarded as a buck-boost converter, while the AHB flyback converter functions as a buck converter. Its capability to step the voltage down is higher than the traditional ACF. With all mentioned merits, it is more preferable for voltage step down applications.

**B. Operating principles analyses**

Stage 1 \( (t_1 < t < t_2) \): \( Q_1 \) ZVS turns on at \( t_1 \) and then the drain-to-source voltage of \( Q_1 \), \( V_{d1} \) is clamped by input voltage \( V_{in} \). The secondary rectifier is blocked. The energy is stored in the transformer. The magnetizing current \( i_m \) increases linearly together with the resonant current \( i_{Lr} \) and can be expressed by

\[
i_{Lr}(t) = i_{Lr}(t_1) + \frac{V_{in} - V_{Cr}}{L_m + L_m} t
\]

This time interval ends when \( Q_2 \) turns off at \( t_2 \).

Stage 2 \( (t_2 < t < t_1) \): A current dip happens to the resonant current \( i_{Lr} \) during the transient period after \( Q_2 \) turns off at time \( t_2 \), which can be observed from Fig.2. It affects both primary and secondary RMS current. Detailed analysis of this effect will be given in the following description.

**Fig.3** Equivalent resonance circuit

Resonance occurs among \( L_m \), output capacitances \( C_{oss} \) of primary switches and secondary rectifier output capacitance \( C_{sj} \). The equivalent circuit is shown in Fig.3. \( C_{ps} \) is \( C_{sj} \) referred to the primary side. Assume the magnetizing current \( i_m \) maintains the peak value \( I_{Lm \_max} \) during this transient period, which can be calculated by

\[
I_{Lm \_max} = I_{Lm \_avg} + \frac{n V_o (1 - D)}{2 L_m} \tag{5}
\]

\[
I_{Lm \_avg} = I_{Lr \_avg} + I_{r \_avg} = \frac{I_o}{n} \tag{6}
\]

where \( t_d \) is the dead time as shown in Fig.2. Only the dead time between \( t_d \) to \( t_1 \) is considered because it takes longer time than that from \( t_2 \) to \( t_1 \) for the small reverse magnetizing current to charge and discharge the parasitic capacitances; \( I_o \) is the output current. The average resonant current \( I_{Lr \_avg} \) is zero when the law of charge balance is applied to the resonant capacitor.

Then the resonant current \( i_{Lr} \) can be solved by [14]

\[
i_{Lr}(t) = I_{Lm \_max} \frac{2 C_{ps}}{2 C_{ps} + C_{m} + C_{ps}} + I_{Lm \_max} \frac{C_{m}}{2 C_{ps} + C_{ps}} \cos(\omega_r t) \tag{7}
\]

where

\[
\omega_r = \sqrt{\frac{2 C_{ps} C_m}{2 C_{ps} + C_{ps}}} \tag{8}
\]

Due to the large peak magnetizing current \( I_{Lm \_max} \), \( Q_1 \) is usually fully discharged within one resonance period. The maximum current dip when the resonance is longer than half period can be obtained by

\[
I_{dip \_max} = I_{Lm \_max} \frac{2 C_{ps}}{2 C_{ps} + C_{ps}} \tag{9}
\]

Equation (9) illustrates that the resonant current dip is due to the current shared by the primary and secondary capacitances. The maximum current dip is determined by the ratio \( C_{ps} / C_{oss} \).

If the resonance is shorter than the half period, the current dip is lower. Actually, the resonance stops when \( C_{oss} \) of \( Q_1 \) is fully discharged or \( C_{ps} \) of the secondary rectifier is fully discharged. The expressions for \( V_{d1} \) and \( V_{SR} \) are given as follows:

\[
V_{d1}(t) = V_n - \frac{I_{Lm \_max} t}{2 C_{ps} + C_{ps}} - \frac{I_{Lm \_max} C_{ps}}{2 C_{ps} + C_{ps}} \sin(\omega_r t) \tag{10}
\]

\[
n V_{SR}(t) = V_n - \frac{I_{Lm \_max} t}{2 C_{ps} + C_{ps}} - \frac{I_{Lm \_max} C_{ps}}{2 C_{ps} + C_{ps}} \sin(\omega_r t) \tag{11}
\]

**Fig.4** \( V_{d1} \) and \( V_{SR} \) waveforms during ZVS transition period when (a) \( C_{oss} = 8 \mu F \) and \( C_{sr} = 200 \mu F \); (b) \( C_{oss} = 17 \mu F \) and \( C_{sr} = 400 \mu F \)

**Fig.5** Equivalent circuit of \( L \) and \( C \) resonant process
Large $C_{osx}$ and $C_{ps}$ give longer resonance, which is longer than half resonance period. In this case, $V_{st}$ drops to zero first. By contrast, small $C_{osx}$ and $C_{ps}$ give short resonance, which is shorter than half resonance period and $V_{st}$ will drops to zero first. This phenomenon is shown in Fig.4. If the resonance is much smaller than the half resonance period $T_0$, $\sin(\omega_0 t)$ can be replaced by $\omega_0 t$. $V_{st}$ decreases to zero linearly. Thus it will not join in the resonance and the resonance current expressions can be solved by

$$i_{Lr}(t) = I_{Lr, max} - \frac{V_{in} + V_C}{L_r + V_C} \sin(\omega_0 t)$$  \hspace{1cm} (12)

$$Z_{r \a} = \sqrt{L_r / C_p} \omega_0 = 1 / \sqrt{L_r C_p}$$  \hspace{1cm} (13)

The maximum current dip becomes

$$I_{dp, max} = \frac{V_{in} + V_C}{\frac{1}{1 + L_r / L_m} Z_{r \a}}$$  \hspace{1cm} (14)

Equation (14) shows when the resonance is less than half resonance period, the ratio of $L_r / C_p$ will affect the maximum current dip. Since the magnetizing inductance $L_m$ is much larger than $L_r$, $I_{dp, max}$ depends on $Z_{r \a}$.

Stage 3 ($t_3 < t < t_4$): After the current dip happens to $i_{Lr}$, $Q_2$ and secondary rectifier start to conduct current. The resonant current is transferred to the secondary side. The magnetizing inductance is clamped by $nV_o$. The resonant process of $L_r$ and $C_p$ is the same with traditional active clamp flyback converter, but the initial conditions are different. The equivalent resonant circuit is shown in Fig.5 and the expressions for magnetizing current $I_{Lm}$ and resonant current $i_{Lr}$ during this time interval are as follows

$$I_{Lm}(t) = I_{Lm, max} - \frac{nV_o}{L_m} t$$  \hspace{1cm} (15)

$$i_{Lr}(t) = I_{Lr, ini} \cos(\omega_0 t) + \left( \frac{V_{in} - V_{Cr, ini}}{Z} \right) \frac{\sin(\omega_0 t)}{Z}$$  \hspace{1cm} (16)

$$V_{Cr, ini} = nV_o + \frac{I_{Lm, max} + I_{Lm, avg}}{2C_r} DT$$  \hspace{1cm} (17)

$$I_{Lm, max} = I_{Lm, avg} = \frac{nV_o (1 - D) (T_s - t_{4d})}{2L_m}$$  \hspace{1cm} (18)

$$\omega_0 = 1 / \sqrt{L_r C_p} \ Z_{r \a} = \frac{L_r}{\sqrt{C_p}}$$  \hspace{1cm} (19)

where $V_{Cr, ini}$ is the initial voltage across the resonant capacitor before the resonance starts and can be estimated based on the charge balance; $I_{Lm, min}$ is the minimum magnetizing current; $I_{Lr, ini}$ is the resonant current after the current dip. It can be expressed by

$$I_{Lr, ini} = I_{Lr, max} \frac{2C_{osx} - C_{ps}}{2C_{osx} + C_{ps}}$$  \hspace{1cm} (20)

or

$$I_{Lr, ini} = I_{Lr, max} - \frac{V_{in} - V_C}{L_r + V_C} \frac{V_{in} + V_C}{Z_{r \a}}$$  \hspace{1cm} (21)

depending on the resonance longer or shorter than the half resonance period.

Stage 4 ($t_4 < t < t_5$): The current dip also occurs during this ZVS transition period after $Q_2$ turns off. The equivalent resonant circuit is also the same with the previous ZVS transition period as shown in Fig.3, while the initial conditions are different. The similar expression for resonant current $i_{Lr}$ is shown as follows:

$$i_{Lr}(t) = I_{Lr, ini} \cos(\omega_0 t) + \left( \frac{nV_o - V_{Cr, ini}}{Z} \right) \frac{\sin(\omega_0 t)}{Z}$$  \hspace{1cm} (22)

$$V_{ds2}(t) = \frac{V_{in} + I_{Lm, min} / 2C_{osx} + C_{ps} + I_{Lm, min} C_{ps}}{2C_{osx} + C_{ps} \omega_0^2 2C_{osx}} \sin(\omega_0 t)$$  \hspace{1cm} (23)

A simulation is conducted to illustrate this phenomenon. As shown in Fig.6, the blue curve with low $C_{ps}$ is decreasing faster and turns off earlier than the red curve with high $C_{ps}$. In high frequency converter design, dead time control is of great importance. It is desirable to have a very short ZVS transition period to minimize the circulation power loss.

![Fig.6 Drain-to-source voltage for Q2 during ZVS transition time](image)

Additionally, due to the small $I_{Lm, min}$, it takes several resonant periods to fully discharge $Q_2$. This can also be observed in Fig.6. On the other hand, the magnetizing current $I_{Lm, max}$ is much larger than $I_{Lm, min}$. During the ZVS transition after $Q_2$ turns off, $Q_2$ is usually fully discharged within one resonant period. The decreasing rate of $V_{ds2}$ is almost linear. Therefore, only the dead time from $t_4$ to $t_5$ is considered.

This period ends when $Q_2$ is fully discharged and realizes ZVS turn on. $Q_2$ will be clamped by the input voltage.

### TABLE II

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>QUANTITY</th>
<th>RANGE</th>
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<tbody>
<tr>
<td>$V_{st}(V)$</td>
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</tr>
<tr>
<td>$V_{st}(V)$</td>
<td>19.3</td>
<td></td>
</tr>
<tr>
<td>$P_{st}(W)$</td>
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<td></td>
</tr>
<tr>
<td>$f_c$</td>
<td>1 MHz</td>
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</tr>
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### III. OPTIMAL DESIGN PROCEDURE

The specification is shown in TABLE II. Since the voltage stress for primary devices is reduced to input voltage $V_{in}$ for the proposed topology, both switches and turns ratio selection have a larger margin than traditional ACF. In this design, the converter is designed to operate at discontinuous conduction mode (DCM). The negative $i_{Lm}$ helps ZVS
operation. The resonant inductance $L_r$ is integrated into the transformer by using its leakage inductance. The optimal design procedure will be given in this section.

**A. Considerations of transformer power loss**

Transformer power loss consists of core loss and winding loss. Core loss increases significantly at high frequency. The core material ML91S from Hitachi shows good performance at 1MHz [34] and is selected for the core material.

Flux cancellation for the traditional ACF is pointed out in [15], as shown in Fig. 7 (a). The negative primary current helps the flux cancellation in the transformer and winding loss will be reduced compared to the traditional flyback converter. Actually, this is because the resonant capacitor has to satisfy the law of current-second-balance during the resonant period. The shaded area I should be exactly the same with area II as shown in Fig. 7(a). On the other hand, the resonant inductance should be designed to provide enough negative magnetizing current. The ZVS realization can be described by the charge equation. Similarly, combine (4) and (26), the RMS current on $Q_2$, $I_{ds2_{rms}}$ is derived. The resonant current RMS value $I_{L_r_{rms}}$ can be calculated by

$$I_{L_r_{rms}} = \sqrt{\frac{1}{t_4-t_3} \int_{t_3}^{t_4} i(t)^2 dt}$$

The secondary current $i_s$ is the difference of the magnetizing current to resonant current from $t_3$ to $t_4$, which can be expressed by

$$i_s(t) = i_{L_m}(t) - i_{L_r}(t) \ (t_3 < t < t_4)$$

Combine (5),(6),(15) to (21) and (28), the secondary RMS current $I_{L_r_{rms}}$ is derived. The impact of magnetizing inductance on primary and secondary RMS current is summarized in Fig. 8. It can be concluded that the magnetizing inductance should be maximized as possible to reduce power loss. Meanwhile, it should be smaller enough to discharge all parasitic capacitances during dead time. The optimal magnetizing inductance and corresponding dead time can then be determined from Fig. 9 referring to (25).

**B. Magnetizing inductance design**

In order to achieve ZVS turn-on for $Q_1$, the magnetizing inductance should be designed to provide enough negative current. The ZVS realization can be described by the charge balance

$$I_{L_m_{min}} t_d = 2C_{ps} V_{in} + C_{ps} V_n + C_v V_{in}$$

(24)

where $C_v$ is the transformer parasitic capacitance referred to the primary side. Combine (6), (18) and (24), the magnetizing inductance can be derived in (25). The optimal magnetizing inductance can be designed from the analysis of RMS current.

$$L_m = \frac{n^2 V_n (1-D)(T_s - t_f)}{4nC_{ps} + 2C_{ps} + 2nC_v} V_n + 2I_{L_r} t_d$$

(25)

**C. Primary and secondary RMS current**

The RMS current should be calculated first to estimate the power loss. The definition equation of RMS is

$$I_{rms} = \frac{1}{T_s} \int_{t_1}^{t_2} i(t)^2 dt$$

(26)

Combine (16), (17) and (26), the RMS current on $Q_1$, $I_{ds1_{rms}}$ can be described. Maple is used to solving the bulky equation. Similarly, combine (4) and (26), the RMS current on $Q_2$, $I_{ds2_{rms}}$ is derived. The resonant current RMS value $I_{L_r_{rms}}$ can be calculated by

$$I_{L_r_{rms}} = \sqrt{I_{ds1_{rms}}^2 + I_{ds2_{rms}}^2}$$

The secondary current $i_s$ is the difference of the magnetizing current to resonant current from $t_3$ to $t_4$, which can be expressed by

$$i_s(t) = i_{L_m}(t) - i_{L_r}(t) \ (t_3 < t < t_4)$$

(28)

Combine (5),(6),(15) to (21) and (28), the secondary RMS current $I_{L_r_{rms}}$ is derived. The impact of magnetizing inductance on primary and secondary RMS current is summarized in Fig. 8. It can be concluded that the magnetizing inductance should be maximized as possible to reduce power loss. Meanwhile, it should be smaller enough to discharge all parasitic capacitances during dead time. The optimal magnetizing inductance and corresponding dead time can then be determined from Fig. 9 referring to (25).

**D. Resonant capacitor design**

The turn-off current on auxiliary switch $Q_1$ and secondary rectifier is small if the resonant current $i_{L_r}$ is close to the magnetizing current $i_{L_m}$ at the end of resonance. In this case, a small $C_r$ is desirable to obtain the low turn-off current through the high side $Q_2$ and secondary rectifier. However, both primary and secondary RMS current increase with the smaller $C_r$, as shown in Fig. 10. On the other hand, the larger $C_r$ means smaller RMS current while larger turn-off current on auxiliary switch $Q_1$ and secondary rectifier. The AHB flyback converter has significantly reduced the voltage stress on active components. Thus the turn-off loss is greatly reduced. The large $C_r$ is desirable to minimize conduction.
loss after iteration.

An iteration is needed for the optimal design.

### TABLE III

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>Value</th>
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<tr>
<td>Primary devices</td>
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<tr>
<td>Secondary rectifier</td>
<td>EPC2033</td>
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<tr>
<td>Magnetizing inductance</td>
<td>11uH</td>
</tr>
<tr>
<td>Resonant inductance</td>
<td>195uH</td>
</tr>
<tr>
<td>Resonant capacitance</td>
<td>430nF</td>
</tr>
<tr>
<td>Magnetic core</td>
<td>EI22/6/16-ML91S</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>6:2</td>
</tr>
</tbody>
</table>

---

**Fig.11** Primary and secondary RMS current under different \( \frac{C_{ps}}{C_{oss}} \) when \( V_{in}=127V, \ n=1:3:1 \)

**Fig.12** \( \frac{C_{ps}}{C_{oss}} \) impact on converter total power loss

**E. Current dip effect**

The impact of the current dip causing by the current divider effect of primary and secondary output capacitance is investigated and summarized in Fig.11. \( 2C_{oss}+C_{ps} \) is kept constant to ensure the same negative magnetizing current. Larger \( \frac{C_{ps}}{C_{oss}} \) contributes to higher \( I_{srms} \). On the other hand, \( I_{lrms} \) is decreasing to a certain value and then increasing. Therefore, the secondary SR should be selected taking into consideration the whole converter power loss. The relationship of converter total power loss \( P_{total} \) and \( \frac{C_{ps}}{C_{oss}} \) is shown in Fig.12. \( \frac{C_{ps}}{C_{oss}} \) between 2 and 4 achieves minimal loss. This can be used to select primary and secondary switches. Given that switches of specific characteristics change slightly in different devices of the same part number, the primary and secondary switches are selected referring to information in the datasheet.

**Fig.13** Total power loss under different turns ratio

**F. Turns ratio selection**

The turns ratio selection is of great importance to design a high efficiency converter. It has several impacts on the converter design. For ACF converters, both primary and secondary switches selections are relating to the turns ratio, as shown in TABLE I. However, for the AHB flyback converter, the voltage stress for the primary switches is \( V_{in} \), which has no relation with the turns ratio. Moreover, the turns ratio selection also affects both primary and secondary RMS current [15] and transformer core loss. In other words, the converter total power loss is affected by the turns ratio.

**Fig.14** Optimal design flow chart

Based on the design procedure as mentioned above, a flow chart is made to obtain the optimal design, as shown in Fig.14. Iterations for the optimal turns ratio selection are performed and the corresponding power loss when \( V_{in}=100V \) is shown in Fig.13. 6:2 yields the minimum power loss and is determined for the transformer design. Finally, the circuit parameters are listed in TABLE III. GaN devices 650V GS66502B from GaN system are selected for primary switches due to the lower output capacitance compared to 350V EPC2050. GaN devices with lower voltage ratings, for example, 300V, can be selected when they are available in the market. EPC2033 is used for secondary SR. The ratio of \( \frac{C_{ps}}{C_{oss}} \) is 2:87.

To operate at MHz frequency, planar transformers illustrate better performance than conventional transformers [26]-[32]. Secondary windings are connected in parallel to further reduce winding loss. A half-turn paralleled winding practice is first proposed in [26]. The paralleled winding structure along with the magnetomotive force (MMF) distribution is shown in Fig.15. The number of layers \( m_p \) for primary windings and \( m_s \) for secondary windings can be derived from the MMF distribution, which is 0.5 and 1, respectively. The current distribution conducted by 2-D FEA simulation at 1 MHz shown in Fig.16. Air gaps are created on all three legs of the magnetic core E22/6/16. The current distribution for secondary windings S1_1 located on the top and S2_2 located on the bottom are identical, while they are a little bit lower than the current distribution for S1_2 and S2_1 in the middle having the same current distribution. The secondary current can be taken as uniformly distributed in this paralleled winding structure. Thus this winding structure contributes to a low AC winding loss.
IV. EXPERIMENT VERIFICATION

A 1MHz, 65W, 19.3V prototype is built to verify the feasibility of the converter, as shown in Fig.17. GaN devices are used for both primary and secondary switches. Fig.18 shows the measured drain-to-source voltage waveform of $Q_2$ and the resonant current waveform when input DC voltage is 127V. ZVS for $Q_2$ is achieved despite the decreasing rate is affected by the resonance that happens to $i_{Lr}$. As discussed in Section II, $i_{Lr}$ ringing amplitude is affected by $C_{ps}/C_{oss}$. High $C_{ps}/C_{oss}$ may lead $i_{Lr}$ to be positive, which affects the $V_{ds1}$ decreasing rate. The current dip effect during ZVS transition time can be easily observed from Fig.18 (b) with an external 330pF film capacitor connected in parallel with the secondary rectifier. The ZVS transition time becomes obviously longer than the converter without external $C_{sj}$.

Efficiency curves under whole input voltage range at full load condition are shown in Fig.19. The output current $I_o$ was measured by the multi-meter Keysight 34465A. The output voltage $V_{out}$, input voltage $V_{in}$ and input current $I_{in}$ are measured by three multimeters Agilent 34410A, respectively. The 96.5% peak efficiency is achieved when the input voltage is 127V for the converter without external $C_{oj}$. This proves the effectiveness of previous analysis in Section II.

Table IV Efficiency Comparison

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref.[35]</td>
<td>200kHz</td>
</tr>
<tr>
<td>Ref.[36]</td>
<td>200kHz</td>
</tr>
<tr>
<td>Ref.[37]</td>
<td>1MHz</td>
</tr>
<tr>
<td>Ref.[33]</td>
<td>1MHz</td>
</tr>
<tr>
<td>This paper</td>
<td>1MHz</td>
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</tbody>
</table>

The built prototype verifies the effectiveness of the optimal design procedure. It benefits from the better high frequency performance core material and interleaved winding layout. Taking the impact of the current dip effect into consideration, primary and secondary switches are selected to minimize the power loss. Together with the optimal design of magnetizing inductance, resonant capacitor and turn ratio selection, a high performance converter is built.

The uncertainty analysis is done to justify the measured peak efficiency. Type A, Type B and combined standard uncertainty are summarized in TABLE V. It should be noted here that the confidence level is not given in datasheet of the measurement. 95% confidence level is assumed and the coverage factor is selected to be 2.

The built prototype verifies the effectiveness of the optimal design procedure. It benefits from the better high frequency performance core material and interleaved winding layout. Taking the impact of the current dip effect into consideration, primary and secondary switches are selected to minimize the power loss. Together with the optimal design of magnetizing inductance, resonant capacitor and turn ratio selection, a high performance converter is built.
flyback converter. capacitor, primary and secondary switches selection and inductance design with the consideration of dead time is magnetizing inductance. The optimal magnetizing Hz operation, the dead time is of great importance to design be used to select primary and secondary switches. At Mega effect affects primary and secondary RMS current. This can selected for primary switches when they are available in the market.

The detailed analysis of the circuit is presented, including both steady-state and transient analyses. The current divider effect affects primary and secondary RMS current. This can be used to select primary and secondary switches. At Mega Hz operation, the dead time is of great importance to design magnetizing inductance. The optimal magnetizing inductance design with the consideration of dead time is investigated. The design procedure, including the resonant capacitor, primary and secondary switches selection and turns ratio design contributes to a high efficiency AHB flyback converter.

Finally, a 56W/inch³ 1MHz 65W prototype is built to verify the feasibility of the proposed converter. It achieves 96.5% peak efficiency at 127V. The whole system efficiency under the entire input voltage range is above 93%.

V. Conclusion

This paper gives detailed analyses of the AHB flyback converter. It can be regarded as a buck converter with a transformer. Thus this converter is well adapted to voltage step-down applications. Larger margin is given for components selection and turns ratio design. GaN devices with lower voltage ratings, for example, 300V, can be selected for primary switches when they are available in the market.

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References


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