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Synchronous Rectifier for High-Frequency Switch Mode Power Supplies using Phase Locked Loops

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Abstract—To meet the ever increasing demands for small lightweight consumer chargers, solutions to achieve higher switching frequencies are required. In this paper we show that it is essential to implement a synchronous rectifier for furthering advancements in power density. The shortcomings of diodes are illustrated, their main disadvantage being their large power losses ranging from 600 mW to 2500 mW. We propose a synchronous rectifier based on a Phase Locked Loop (PLL). An application specific integrated circuit containing a PLL designed for a synchronous rectifier was taped out in a 0.18 μm CMOS process. The PLL has an area of 0.05 mm^2 , and the total area containing two level shifters and gate drivers is 0.21 mm^2 . Two main issues with the PLL based synchronous rectifier are identified, the locking time and the RMS jitter. The designed PLL achieves a sufficient phase noise performance, of 8 ns RMS jitter, which from simulations have been shown to have a minimal impact on the efficiency. The locking time of the PLL is measured to 8 μs . The resulting synchronous rectifier prototype showed a possible efficiency improvement of up to 1.8 %, removing $\frac{1}{8}$ of the total power loss, compared to a purely passive rectifier.

I. INTRODUCTION

Consumer electronics are consistently aiming towards more compact designs. The demand for higher power density is increasing. Therefore methods of increasing efficiency and minimize energy storing components are essential. The most common way to reduce the size of the passive components, is by increasing the frequency. In recent years there has been a lot of development in the increase of switching frequency [1]–[4]. This led to the maturation of DC/DC High- (3 MHz to 30 MHz) and Very High Frequency (30 MHz to 300 MHz) (RF) Switch Mode Power Supplies (SMPS). Generally a RF-SMPS can be considered in two parts, an inverter and a rectifier. The inverter stage converts DC voltage to an RF sinusoidal current. The rectifier stage then rectifies this current back to a DC voltage. To achieve high efficiency these topologies utilize Zero-Voltage Switching (ZVS) and Zero-Current Switching (ZCS).

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A challenge of the RF-SMPS is driving the MOSFET at higher frequencies. Research developed self-oscillating gate drives for both single switch [5] and half-bridge configurations [6]. Additionally, single-switch self-oscillating active rectifiers have been demonstrated in [7], [8]. These gate drives all utilizes passive components and the intrinsic capacitances of the MOSFET to generate multi-MHz gate signals, achieving ZVS. However, due to component tolerances the exact frequency and phase of the inverters is not known, especially over a product range. This complicates the design of any synchronous rectifier.

The rectifier stage is often designed using diodes in either a half-bridge Class DE configuration [9]–[11], or using a resonant topology, such as the Class E [12], [13]. Diodes provides the benefit of working passively, and thus very well with the aforementioned self-oscillating inverters. However, diodes are inherently lossy, especially at low voltage applications. Furthermore, as we will show, diodes are often limited by their junction temperature, rendering them unusable in e.g. a high power-density converter. It is thus desired to design a Synchronous active Rectifier (SR), achieving ZVS, using GaN- or MOSFETs instead.

A SR can be implemented with so-called active-diodes [14], [15]. The active-diode is a MOSFET in parallel with a diode. A comparator will trigger the MOSFET to turn on at ZVS, and turn off, as the current reverses. The disadvantage to this topology is the requirement for very fast comparison between signals, level shifting and charging of the gate of the MOSFET, often taking ≥ 10 ns.

This work introduces a SR that is capable of achieving ZVS by utilizing a Phase Locked Loop (PLL) for synchronization. A SR can both improve the efficiency as well as mitigate the need for diodes altogether. Their applications, a part from in resonant power converters, are wireless power transfer [16], [17], PFC rectifiers [18] and more. PLLs are widely applied in telecommunications field as frequency generation sources, as well as for pulse-width-modulation in power amplifiers [19], [20]. PLLs have been introduced in grid-connected converters, to optimize grid synchronization [21], [22]. Very few works have used PLLs in RF-SMPSs. In [23] a digital PLL is briefly introduced in a synchronous rectifier for wireless charging, leaving out the details of the PLL itself. The details in the design of the analog PLL, and its influence in a synchronous rectifier will be thoroughly discussed in this work. The PLL can mitigate the requirements for fast level shifting and com-

parison, if these are included in the loop. We have designed an Application Specific Integrated Circuit (ASIC) for this purpose.

The designed ASIC will be implemented in a USB-C charger prototype. With the next generation of USB, convenience has been a focus. A consumer can expect any USB-C charger of a certain power level to deliver a specific voltage and current output, requested by their devices. The USB-C power delivery protocol [24] specifies output voltages of 5 V, 9 V, 12 V, 15 V and 20 V, and up to 5 A output. The output voltages will be the specifications, aimed for in the designed power converter.

The paper is structured as follows: In section II we introduce the passive rectifier, and analysis of the diodes currently available on the market. In sec. III the proposed synchronous rectifier based on the PLL is introduced. In section IV we will go through the building blocks of the PLL, and present how they are designed in the ASIC. The effect of jitter in a PLL synchronized rectifier will be presented in this section as well. In section V we will show the results of the power converter prototype designed with the SR presented. The challenges of PLL SR will be thoroughly discussed. It will all be summarized in the conclusion in section VI.

II. RADIO FREQUENCY RECTIFIERS

In many RF-SMPS the design is split in two, with an inverter and a rectifier, as described in the introduction. The design of the inverter will not be discussed in this paper. Details on designing this part can be found in [4], among others. In this paper the focus will be on the RF rectifier, and for the illustrative purpose, the inverter will be seen as an ideal sinusoidal current, I_{in} shown in Fig. 1.

Several topologies are of interest when designing a rectifier. Two classes of interchangeable rectifiers exist; Class E and Class DE. The Class E rectifier is a single-switch rectifier, where the rectifier input impedance is made resistive at the switching frequency of the inverter stage. The inherent downside in this topology is the voltage across the rectifying elements, often 3-4 times the output voltage. It does not have a high side switch, and generally is a simpler implementation. The increased voltage stresses, however, are undesirable for any higher voltage output application [25]. The Class DE rectifiers are often described as either voltage or current driven. For this application the current driven rectifiers are of interest. They are usually split in three [15]. In Fig. 1 the three topologies are shown.

All the presented topologies will ZVS, as the diodes will switch passively at the required instance. The shunt capacitances, C_1 and C_2 , will influence the duty cycle, D_d , of the individual power devices. C_1 and C_2 is the accumulated capacitance of the the intrinsic junction capacitances as well as any added external capacitances. From [11], the optimal output power capabilities of both of the half-bridge topologies is achieved at a diode duty cycle of $D_d = 0.25$. In this instance the capacitances will have to fulfill (1).

$$P_{OUT} = \frac{I_{OUT}^2}{f_{sw} (C_1 + C_2)} \quad (1)$$

(a) Class DE Half-Bridge Rectifier [10]

(b) Class DE Half-Wave Low dV/dt Rectifier [9]

(c) Class DE Full-Bridge Rectifier [25]

Fig. 1: Class DE Rectifiers. Inverter is modeled as an ideal sinusoidal current source.

From (1) it can be seen that for larger switching frequencies, f_{sw} , the required capacitances reduces. When the frequency increases significantly, the intrinsic capacitance of the diodes and FETs will become too large to have the required duty cycle $D_d = 0.25$. The duty cycle would reduce, and this increases the peak currents in the diodes. As an example the required capacitance at 30 MHz and an output of 60 W and 3 A is 2.5 nF. This is generally significantly higher than the intrinsic capacitances of the diodes.

The primary reason for designing the full bridge rectifier is to reduce the stresses of the components. The rectifier conducts both half waves of the sinusoidal input current and the resulting load on the inverter is almost increased by 4. This effectively halves the required peak output current of the inverter for the same output voltage, and significantly reduces the component stress, as discussed in [15]. The duty cycle of the power devices is desired to be as close to $D_d = 0.5$ to achieve these benefit. This is achieved with the lowest possible junction capacitance. The full bridge rectifier will be implemented in the prototype.

A. Diode Power Loss Estimation

The topologies presented in Fig. 1 all function passively but the diodes will have a relative higher power loss than a GaN- or MOSFET. If designing for higher power density, smaller packages for the diodes are required. The trade-offs of smaller packages is a higher thermal resistance to ambient i.e. less power can be lost in the diodes. Furthermore, forward voltages are often around 500 mV, which makes them undesirable for low voltage application, e.g. at an output of 5 V, double the

forward voltage (1 V) will be dropped across the diodes. For the given USB-C application, especially the 20 V output yields undesirable results.

The power losses of 70 commercially available diodes are estimated. The results of this analysis can be seen in Fig. 2. The diodes have all been selected according to the specifications listed in table I. The blocking voltage, V_{rr} , should be high enough to work in the USB-C application. The junction capacitances of all the available diodes are less than 2.5 nF.

TABLE I: Diodes Specifications

	Minimum	Maximum
V_{rr}	20 V	100 V
I_{avg}	3 A	10 A
Mounting Type	SMD	

The power loss estimation was split in two parts - conduction loss and reverse loss. The conduction loss is primarily the loss generated from the current conduction and the forward voltage drop, as in (2). I_{avg} is the average current of the sinusoidal input current with amplitude I_m , multiplied by the duty-cycle, D_d , of the diode, i.e. 0.5.

$$P_{cond} = V_f \cdot I_{avg} = V_f \cdot \frac{2}{\pi} I_m D_d \quad (2)$$

The reverse loss is two fold; reverse recovery loss and leakage loss. While most of the presented diodes are Schottky diodes, that are said to switch instantaneously, the reality is often a few nanoseconds of reverse recovery loss, primarily caused by the charging of the junction capacitance [26], [27]. Secondly, Schottky diodes experience higher leakage currents than regular PN junction diodes. This leakage current increase exponentially with the junction temperature, and Schottky diodes are vulnerable to thermal runaway.

The reverse recovery time, T_{rr} , is estimated using (3). The current in the reverse recovery period is estimated to be symmetrically triangular shaped. The first half of the triangular current will have the slope, SL_I , of the sinusoidal current at zero crossing. Equally, the current will return to the leakage current with the same but opposite slope in the last half of T_{rr} . The reverse recovery time can be estimated from the output voltage, V_{out} , the effective junction capacitance C_j , and the integrated current. The effective capacitance is taking into account the voltage dependencies of the junction capacitance.

$$T_{rr} = 2 \cdot \frac{\sqrt{SL_I C_j V_{out}}}{SL_I}, \quad SL_I = I_m 2\pi f_{sw} \quad (3)$$

The reverse loss is then given in (4). To have a safety margin to thermal runaway the leakage current, I_{rr} , is taken at the highest temperature, and blocking voltage.

$$P_{rev} = \frac{1}{2} T_{rr} I_{rr,pk} V_{out} f_{sw} + (1 - D_d - T_{rr} f_{sw}) I_{rr} V_{out} \quad (4)$$

It is evident from (4) that the reverse losses increases both with frequency and output voltage. As the average current in the diodes will be equal in all the USB-C output case, the

worst case losses will be experienced at an output of 20 V and 3 A.

The losses in a single diode is shown in Fig. 2. The power loss is estimated for a diode in a full-bridge rectifier, switching at 1 MHz, with an output of 20 V and 3 A. The diodes area on a printed circuit board (PCB) have been estimated from the footprint specified for the specific thermal resistance to ambient. The junction temperature has been estimated from an ambient temperature of 25 °C

Fig. 2: Single Diode Power losses vs. Required PCB Area. Junction temperature estimated from thermal resistance to ambient. Several diodes exceeds their thermal limit.

The analyzed diodes loose between 600 mW and 2300 mW. The junction temperature for several of the diodes are above their thermal limit, with no diodes performing under 80 °C. Furthermore, it would require PCB areas of 80 mm² to 100 mm² or larger heat sinks to keep the diodes at these temperatures. Finally, the ambient temperature is set to 25 °C, which is unrealistic for a high power density converter.

In comparison using (5) and (6) the gate losses, P_{gate} and conduction losses P_{cond} , of EPCs EPC2014 GaNFET is estimated. The switching losses are assumed negligible as the devices would be operated at ZVS.

$$P_{gate} = Q_g V_{gs} f_{sw} \quad (5)$$

$$P_{cond} = R_{ds,on} I_{RMS}^2 \quad (6)$$

Where Q_g is the gate-charge, V_{gs} is the gate-source threshold voltage on the GaNFET, f_{sw} is the switching frequency, $R_{ds,on}$ is the on resistance of the GaNFET and I_{RMS} is the RMS current in the GaNFET. $R_{ds,on}$ and Q_g can be found in the data sheet. The total estimated losses of a single EPC2014 in the described full-bridge rectifier is 106.2 mW. The comparison is shown in Fig. 2. A synchronous full-bridge rectifier designed with EPC2014, could potentially loose less power than a single diode. It is evidently necessary to implement an SR if designing for high power density.

III. SYNCHRONOUS RECTIFIER PROPOSAL

The main challenge when designing a SR for a HF or VHF inverter will be the timing of the gate signals. There are two inherent problems with the discussed topologies. First, the switching frequency and phase of the RF-SMPS are changing with component tolerance and load due to the nature of the self-oscillating gate drive. Secondly, the delays through

Fig. 3: Proposed SR with timing diagram.

comparators, level shifters and gate drivers can be ≥ 10 ns, which will have to be mitigated to achieve higher efficiency. We propose the use of a PLL to synchronize the switching of the rectifier with the input current from the inverter. The concept is shown in Fig. 3.

The PLL works by the heterodyne principle. The reference frequency and feedback frequency is compared through a phase-detector. The phase difference is passed through a low pass filter, and fed to a voltage-controlled oscillator. The negative feedback loop will ensure zero phase difference, and the output of the PLL will match in frequency and phase to the input current. The PLL output signal can then be controlled, such that the high and low side GaN- or MOSFET are turned on and off properly. The advantage of this proposal is the inclusion of the level shifter and gate driver in the loop as well as any comparators used. This mitigates all delays experienced in these blocks, allowing for higher switching frequencies. The trigger levels of V_{ref1} and V_{ref2} is selected such that PLL will synchronize the turn on of G_{HS} to when V_{sw} reaches the output voltage, achieving ZVS. In the following the design procedure for a PLL is detailed.

IV. IMPLEMENTATION OF THE PLL

The basic blocks of a PLL is shown in Fig. 4. Four blocks make up its general function. They are a Phase Detector (PD), a Low-Pass Filter (LP), a Voltage Controlled Oscillator (VCO) and finally the feedback path (FB). The FB path can be used to create a output frequency greater than the input frequency. In the SR the feedback factor is unity as it is used to replicate the input frequency.

A PLL has many design parameters. When implementing a PLL in an SR the two parameters of main concern are phase noise and locking time. Phase noise, often called jitter, is defined as a rising or falling edges deviation from its ideal

Fig. 4: Concept of a PLL

position in time. In a SR designed to achieve ZVS any jitter of the gate signals can impact the efficiency of a power converter. Locking time is the time from the input frequency of the PLL changes, to the PLL has the same output frequency. During this time, the PLL output cannot switch the power devices, as it can cause undesirable effect such as shorting of the output.

The designed PLL is an analog charge-pump PLL based on the design procedure from [28]. In the following, the elements are discussed in details. The primary focus of the analysis will be their respective noise contributions, and will be concluded with the estimated RMS jitter of the designed PLL.

A. Phase Detector and Charge Pump

The phase detector is an extended range detector consisting of two flip flops, which resets the output when two rising edges arrives. It provides the charge pump with a signal corresponding to the phase difference. It is implemented with a delay, T_d , in the reset path, to eliminate the dead zone problem (i.e. lack of frequency tracking when the input and output phases are close). The charge pump is implemented as switched current sources. The principle block-diagram is shown in Fig. 5. While other more complex implementations

can improve the over all performance of the PLL this is not necessary to perform well enough for a RF-SMPS.

Fig. 5: The extended range phase detector and Charge Pump

In the jitter analysis the noise of the charge pump is assumed to be the primary influence. Because of the dead zone solution the noise contribution from the phase detector is assumed to be negligible.

B. Low Pass Filter

The low pass filter is a 3rd order RC-network, which filters the output current of the charge pump to the control voltage of the VCO. The choice and design of the low pass filter is critical to ensure stability in the PLL. The 3rd order filter provides the largest suppression of spurious tones, generated by any ripple on the VCO, i.e. more jitter. A disadvantage of this is the added settling time to acquire a lock on the PLL frequency. The RC-network is shown in Fig. 6. The only noise sources in the filter are the resistors.

Fig. 6: 3rd order Low Pass Filter in the PLL loop.

The transfer function for the filter can be found in [29]. The 4th order PLL design procedure is given in [28]. The loop filter is implemented off-chip to give a broader range of possible designs in the SR.

C. Voltage Controlled oscillator

The voltage controlled oscillator is implemented as a single-ended current-starved ring oscillator, as shown in Fig. 7. The bias voltages, $V_{bias,n}$ and $V_{bias,p}$ is generated from a voltage controlled current mirror.

The VCO is the most critical part in terms of phase noise. The ring oscillator is chosen for its broad tuning range. It will not have state-of-the-art phase noise performance, but for implementation in this SR, the current-starved oscillator has sufficiently low phase noise.

Fig. 7: Voltage Controlled Oscillator. Sizes shown are in μm

The open-loop period jitter of the oscillator is measured and shown in Fig. 8 together with a simulation of the phase noise ($X(\omega)$). The period jitter (ϕ_N) relation to the phase noise is given in [30], and repeated in (7).

$$\phi_N^2 = \int_0^\infty |X(\omega)|^2 4 \sin^2\left(\frac{\omega}{2}\right) d\omega \quad (7)$$

In Fig. 8 the period jitter flattens at about 90 ps, at a frequency of 10 MHz. As the VCO is the dominant noise source in the PLL, the open-loop period jitter is an estimate of the experienced RMS jitter in the PLL.

Fig. 8: Period Jitter of the Open-Loop Oscillator vs. Output Frequency, F_{out}

D. Jitter analysis

To analyze the phase noise of the PLL, the model shown in Fig. 9 is used. The noise spectral densities (NSD) are denoted $S_{i,cp}$ for the charge pump current noise, $S_{v,LF}$ for the loop filter voltage noise and $S_{\Phi,VCO}$ for the phase noise of the oscillator. They are all obtained from simulations. The input phase noise as well as the phase noise of the phase detector are negligible.

The individual transfer functions of the noise sources are derived. The important parameters are the charge pump current i_{CP} , loop filter current-to-voltage transfer function $LF(s)$ and the frequency-per-volt gain of the oscillator K_{VCO} . The gain of the phase detector is $\frac{1}{2\pi}$ and included together with the charge pump current.

Fig. 9: Noise model used to estimate the phase noise of the PLL

The resulting simulated Single Side Band noise, SSB , for the PLL at 1 MHz is shown in Fig. 10. The SSB for the individual source is obtained by multiplying the individual NSD with the magnitude of their respective transfer functions squared. The resulting contributions are denoted SSB_{CP} from the charge pump, SSB_{LF} from the loop filter and SSB_{VCO} from the VCO. The total phase noise, SSB_{tot} is the sum of the individual contributions. The individual noise contributions are plotted as well. The noise of the VCO is the primary noise source in the PLL.

Fig. 10: Simulated Single Side Band Noise Power Spectrum, SSB , for the blocks in the PLL. $F_{out} = 1\text{MHz}$.

The RMS jitter, $\sigma_{\Delta T}$, is found by integrating the SSB . The lower end of the SSB is often dominated by flicker noise in the system. However, for a RF-SMPS burst mode regulation is often introduced. Burst mode regulation runs the converter for a portion of a burst period, D_{bs} . The PLL will thus not run longer than D_{bs} , and the lower integration limit can be set by half the burst mode frequency F_{bs} . The noise at the lower frequencies of the SSB can be ignored. The upper limit is set by half the output frequency, F_{out} . The equation is given in (8).

$$\sigma_{\Delta T} = \frac{1}{2\pi F_{out}} \sqrt{\int_{F_{bs}/2}^{F_{out}/2} S_{TOT}(f) df} \quad (8)$$

The estimated RMS jitter of the PLL operating at 1 MHz is 8 ns. Operating at 1 MHz is at the lower limit of the PLL. If the frequency is increased the jitter normalized to its period would be reduced.

E. Jitter in a Synchronous Rectifier

The SR is designed to switch at ZVS. If the output of the PLL has jitter, the resulting switching will not be exactly at zero voltage. This will result in a drop in efficiency among other effect. In [31] it was shown that for a Class E converter, with a 4% period jitter, would result in 1% efficiency drop.

A SPICE model of a full bridge synchronous rectifier, switching at 1 MHz is built. The SR is built with SPICE models available for the GaNFET EPC2014 from EPC, and PMEG3030ER from Nexperia. LMG1205, an integrated level shifter and gate driver circuit from Texas Instruments, is implemented to produce the required high side signals. Python is used to generate a Gaussian distributed jittery signal, with a desired RMS jitter. The jitter can be assumed to be Gaussianly distributed, as its primary sources will be thermal and flat noise. The flicker noise for the given CMOS technology is below the frequency of interest. The results can be seen in Fig. 11. In Fig. 11a the efficiency of the SR is shown and in Fig. 11b the currents in the respective power devices are shown.

The simulations are done with 4 different output specifications of a USB-C charger, 5 V, 9 V, 12 V and 20 V, and 3 A. The efficiency drops $\approx 10\%$ at an RMS jitter of 10 ns. In Fig. 11b the average current in the GaNFETs is seen to drop off, with the same rate as the efficiency. The RMS current in the diodes are increasing with jitter, as they will conduct during the jittery part of the period. Based on simulations, the jitter of the PLL of 8 ns will impact the efficiency by approximately 4%.

F. ASIC

The presented PLL with gate driver and level shifter has been taped-out in a $0.18\mu\text{m}$ CMOS process. The area of the total system is 0.21mm^2 , neglecting area required for pads etc. The area of the PLL is 0.05mm^2 . A photo of the die can be seen in Fig. 12.

G. Power Stage Implementation

When starting up the converter, or utilizing burst mode control, it is important to disconnect the switching of the power devices in the rectifying stage during the locking time of the PLL. Even if the PLL is biased to operate at the switching frequency, the output phase will not be correct, and the PLL will need to swing in, in order to achieve the correct phase. If the rectifying stage was switched during the phase-locking period, it will have undesirable consequences such as shorting of the output.

Fig. 11: Impact of Jitter in a Synchronous Full-Bridge Rectifier switching at 1 MHz. Simulated using LTSpice and Python.

Fig. 12: Die photo of the taped-out PLL

The solution is to implement an and-gate before the level shifter and gate driver, such that the output can be turned

off. The control signal, SR Power Enable, is derived from an internal LOCK signal from the ASIC. The inherent problem will be that the level shifter and gate drivers is not included in the PLL loop, and their respective delay time will influence the SR. Switching the power converter at 1 MHz the impact will be negligible. A schematic of the solution can be seen in Fig. 13.

Fig. 13: Schematic of PLL implementation in a SR.

As this solution was not implemented on the ASIC, the prototype is build with discrete logic gates, level shifters, and gate drivers.

V. EXPERIMENTAL RESULTS

The taped-out IC was packaged in a QFN64 6 mm × 6 mm package. A half-bridge synchronous rectifier was implemented on a 10 cm × 10 cm PCB, for testing with a 1 MHz self-oscillating Class DE rectifier, designed by Nordic Power Converter (NPC). The half-bridge is implemented as one of the legs of a full bridge rectifier. The full bridge rectifier is required in order to have a proper load matching between the inverter and synchronous rectifier. The half-bridge rectifier PCB can be seen in Fig. 14.

Fig. 14: Implemented Half-Bridge Synchronous Rectifier.

The loop filter of the PLL is implemented with off chip components, to allow for changing of the loop dynamics. The synchronous half-bridge active rectifier is implement with EPC2014 GaNFETs from EPC and PMEG3030 Schottky diodes from Nexperia. The parallel diodes is implemented to insure the passive functionality the Class DE rectifier. The GaNFETs do not have a body diode and their reverse conduction behavior is not well defined. Previous work have shown that they emulate the effect of a body-diode with a forward voltage drop close to their threshold voltage [32], [33].

It is important to design the loop filter tightly to minimize the overshoot, and locking time of the PLL. To show this, two designs is carried out. The loop filter values can be seen in table II. They are designed following the method described in [28].

TABLE II: Loop Filter Design

	Loop 1	Loop 2
PM	50°	50°
f_c	33 kHz	100 kHz
R_0	289Ω	866Ω
C_0	45 nF	5 nF
C_A	3.5 nF	390 pF
R_X	126Ω	374Ω
C_X	3.5 nF	390 pF

Fig. 15: Locking time in the SR. The phase difference, ΔT_{re} , is plotted vs. time.

In Fig. 15 the phase difference between the PLL during locking time is plotted. The results are achieved measuring the input to the ASIC PLL on the PCB shown in Fig. 14. The PLL needs at least $8 \mu s$ of locking time. To decrease the locking time, the bandwidth of the system, f_c , would have to be increased. However, the PLL is a sampled system, and f_c need to be kept a decade or less below the output frequency. It is thus not possible to reduce the locking time further.

In Fig. 16 the PLL is applied in the burst-mode regulated resonant power converter. During the locking phase of the PLL, the frequency output is varying. When the PLL is locked, the active rectifier is enabled through the method described in Fig. 13. Hereafter, the switch node voltage drops

roughly 300 mV, corresponding to the forward voltage of the PMEG3030 diode.

Fig. 16: Oscilloscope comparing the switch node, V_{sw} between Synchronous and Passive Rectification. **Blue:** Active Switch Node, V_{sw} , **Green:** Gatesignal for high side GaNFET fate, **Red:** Passive Switch Node. Output voltage and power is 9V and 13.5W respectively.

In Fig. 17 the thermal images of the synchronous half-bridge rectifier can be seen operating at 1 MHz, and with an output voltage of 12 V and current of 1.9 A. In Fig. 17a the diodes in the half-bridge can be seen heating up, to approximately $50^\circ C$. When the PLL synchronizes the GaNFETs, the resulting thermal image in Fig. 17b is seen to have no significant heating.

In Fig. 18 the efficiency vs. the output scenarios has been plotted. The efficiency is improved in most of the output cases.

At 9 V the converter efficiency is improved by 0.9 %. As this implementation is only one leg of a full bridge rectifier, the overall efficiency improvement can be expected to be 1.8 %. Effectively removing $1/8$ of the total losses.

The self-oscillating resonant converter needs a certain output power level, to keep oscillating. At the lowest output voltage, 5 V the self-oscillating gate drive cannot sustain operation. This results in the low output power and efficiency.

Furthermore, as mentioned, the resonant converter output power is controlled using burst mode control with a frequency of 25 kHz. Due to the nature of the PLL, switching of the synchronous rectifier cannot start before lock has been achieved. At higher output levels, the on-time of the converter reduces, while the locking time is constant. This reduces the efficiency achieved by the converter. Furthermore the increased voltage of the sensing node, at higher output voltage, and the fixed threshold of the sense/FB comparator, results in a small shift in the timing. The outcome is that the gate's are not driven perfectly synchronized and at 20 V it even results in a slight decrease in efficiency.

Fig. 17: Comparison of Thermal Images. The rectifier is in the area marked HB. In Fig. 17a the diodes are visibly heating up (approx. 50 °C), compared to Fig. 17b, where no significant heating can be seen. The pictures are captured at an output of 12 V, 1.9 A.

A. Challenges in a PLL based Synchronous Rectifier

In Fig. 19 an oscilloscope plot of the SR can be seen. In green, the switch node of the half-bridge rectifier and in blue the burst mode PWM is shown. To mitigate the effect of the burst mode control, the charge pump in the PLL is disabled in the converter off period. This keeps the output frequency almost constant during the off-period, allowing for faster locking. This can be seen in the teal waveform. The purple waveform is the enable signal shown in Fig. 13.

The PLL output frequency is seen to be close to constant when the power converter is off. However, the open loop of the oscillator accumulates the phase noise, and the output phase is drifting. When the power converter is turned on again, the PLL corrects the phase of the oscillator. As the charge pump PLL resembles a sample system, the phase-locking requires several rising edges before locking is achieved. As shown in Fig. 15, the locking time cannot be minimized further without comprising the loop stability.

The burst mode regulation adopted in the resonant power converter is not otherwise affected by the locking time. The

Fig. 18: Output Profiles of Resonant Converter. The difference in efficiency between the active and the passive rectifier, $\eta_{act} - \eta_{passv}$, is shown in the bottom axis.

Fig. 19: Oscilloscope of Synchronous Rectifier. Blue: Burst-mode PWM, Green: Switch Node, Red: Highside GaNFET gate, Purple: SR Enable signal.

locking time is limiting the achievable efficiency improvement.

VI. CONCLUSION

To meet the ever increasing demands for small light weight consumer chargers, solutions to achieve higher switching frequencies are required. In this paper we have shown that it is essential to implement a synchronous rectifier for furthering the advancements in power density. The shortcomings of diodes have been illustrated, their main disadvantage being their large power losses ranging from 600 mW to 2500 mW. The phase locked loop is a solution to achieve a zero-voltage switching synchronous rectifier. An ASIC containing a PLL designed for a synchronous rectifier was taped out in a 0.18 μm CMOS process. The PLL has an area of 0.05 mm^2 , and the total area containing two level shifters and gate drivers is 0.21 mm^2 . Two main issues with the PLL based SR was identified, the locking time and the RMS jitter. The designed PLL achieves a sufficient phase noise performance, of 8 ns RMS jitter, which from simulations have been shown to have

a minimal impact on the efficiency. The locking time of the PLL is measured to 8 μ s. The resulting synchronous rectifier prototype showed a possible efficiency improvement of up to 1.8 %. This corresponds to removing $1/8$ of the total power lost. While the PLL-based synchronous rectifier showed valuable benefits, the inherent locking time also limits the possibilities for regulation of radio-frequency switch mode power supplies. Future solutions must minimize any required start-up time, to further improve the synchronous rectifier.

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