Monolithic CZTS-on-Silicon Tandem Solar Cells: Prospects and Challenges


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SUMMARY

We have systematically investigated the possible detrimental effects of monolithic integration of Cu2ZnSnS4 (CZTS) on a Tunnelling Oxide Passivated Contact (TOPCon) silicon cell, as promising representatives for a cheap, stable and earth abundant tandem solar cell. We have studied the role of TiN, as the barrier layer in between the two absorbers, and discuss the implications on the performance of the tandem device. Measurements of minority carrier lifetime revealed that Cu diffusion from CZTS into silicon is not as severe as diffusion from pure Cu. Moreover, a promising implied \( V_{oc} \) (i-\( V_{oc} \)) above 700 mV for Si was measured after the high-temperature CZTS synthesis on Si, despite a 40% percent decrease from initial effective lifetime. Further investigations are required to understand the role of TiN as the barrier layer, because even though the decrease in lifetime seems to be independent of TiN thickness, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) measurements show an effective blocking of diffusing species, when TiN is present as a barrier layer. Further SIMS and Deep-level Transient Spectroscopy (DLTS) characterizations on silicon, where both TiN and CZTS are removed, are planned for more precise measurement of trace elements. Ultimately, asymmetrically passivated TOPCon device wafers with i-\( V_{oc} \) above 710 mV were prepared for the fabrication of monolithic tandem devices with different barrier configurations.

1. INTRODUCTION

Silicon-based tandem solar cells have drawn growing attention, due to the possibility of increasing the overall efficiency of the well-established silicon technology beyond the theoretical and practical limits of single-junction cells [1]. Cu2ZnSnS4 (CZTS) [2], or other similar high-band gap chalcogenides such as Cu2Ge(S,Se)4 [3] and Cu2ZnGeS4 [4], are promising materials for the top cell, since they use abundant, eco-friendly elements and are highly stable. Even though large efforts were made to develop high band gap chalcogenides, the current knowledge on the feasibility of their monolithic integration with silicon and possible interactions of the two absorbers is still limited. The fabrication of chalcogenides usually involves at least one high temperature anneal (>500 °C) of metallic precursors in a reactive ambient (e.g., S or H2S), which can lead to in-diffusion of detrimental metallic elements (Cu in particular) into the bottom silicon cell. As a result, the photovoltaic properties of the Si cell can degrade significantly. Therefore, development of protective intermediate diffusion-barrier layer(s), that do not compromise carrier transport and near-infrared photon transmission, is of crucial importance.

In this research, we use CZTS as a representative of the chalcogenide family for the top cell, and TOPCon structure as a potential technology for the bottom Si cell, owing to its excellent charge carrier selectivity and high temperature resilience [5]. Additionally, we utilize Ti-based inter layers, such as TiN and TiO2, to serve both as a diffusion barrier and a recombination layer. In this respect, after developing in-house TOPCon structures featuring implied \( V_{oc} \) above 700 mV, we investigated possible effects of the CZTS fabrication process on the bottom silicon cell, and studied the role of different barrier layers to mitigate these effects. In addition, based on the preliminary findings, we will fabricate and characterize monolithic tandem devices.
2. MATERIALS AND METHODS

2.1. Silicon TOPCon structure

Double-side polished 100 nm diameter, 1 Ω cm, 350 μm thick, (100) n-type Cz-Si wafers were used. Two types of samples were fabricated: 1) Lifetime samples, with symmetrical passivation stacks of highly doped n-type poly silicon/tunnelling oxide (n-polySi/TO) on both sides. 2) Device samples, with asymmetrical passivation stacks of n-polySi/TO on the front side and p-polySi/TO on the rear side.

The fabrication process is as follows. After RCA clean of the wafers, ~1.2 nm tunnelling silicon oxide was grown by chemical oxidation in 65 % wt HNO₃ solution at 95 ºC. Subsequently, ~40 nm polySi layers were deposited using Low Pressure Chemical Vapour Deposition (LPCVD) at 620 ºC, with SiH₄, B₂H₆, and PH₃ as precursors for p- and n-polySi layers, respectively. The samples were then annealed in N₂ at 850 ºC for 20 min for further crystallization and dopant activation.

2.2. Barrier Layers and CZTS

Thin TiN barrier layers (<25 nm) were deposited by Plasma Enhanced Atomic Layer Deposition (PEALD) using TiCl₄ and NH₃ precursors at 500 ºC to protect the passivated wafers against CZTS diffusion. Subsequently, ~300 nm CZTS precursors were co-sputtered from Cu, ZnS, and SnS targets, and annealed in sulphur atmosphere at dwell temperature of 575 ºC for 30 min. CZTS and TiN layers were then removed in a mixture of H₂O₂:4H₂SO₄ (piranha solution) for lifetime measurements.

2.3. Characterization

Effective minority carrier lifetime of Si was measured by microwave detected photodiocdactance method in steady-state configuration and 1-sun illumination using MDP lifetime scanner from Freiberg Instruments. The in-diffusion profiles of the metallic species were measured using ToF-SIMS.

To evaluate the effect of CZTS synthesis on the silicon cell, 10 lifetime samples were prepared with symmetrical n-Poly/TO passivation on both sides. The as-passivated lifetime values are shown in FIG. 1a. The experiment was designed as follows:

- CZTS material was synthesized on lifetime samples coated with 0, 10, and 25 nm of TiN as the barrier layer, referred to as Si/NoTiN/CZTS or Si/(TiN)/CZTS, respectively.
- Lifetime samples coated with 0 and 25 nm TiN were annealed at 575 ºC in a sulphur atmosphere without any CZTS to observe the influence of the annealing atmosphere separately, referred to as Si/(TiN)/sulphur.
- Lifetime samples coated with 25 nm of TiN and 100 nm of Cu were prepared and annealed in vacuum at 575 ºC to compare Cu diffusion from CZTS to that from a pure Cu layer, referred to as Si/TiN/Cu.

3. RESULTS

The effect of CZTS growth conditions on passivated Si is summarized in FIG.1b. A ∼40% decrease in lifetime can be observed in all Si/(TiN)/CZTS samples, and the lifetime seems to be independent of the TiN thickness. Nonetheless, we observed a severe delamination of CZTS in Si/NoTiN/CZTS sample after the annealing. Although no CZTS was present in Si/(TiN)/sulphur samples, the lifetime has reduced by ∼50%, which suggests the role of sulphur as a contaminating species. Moreover, the Si/TiN/Cu reference sample shows a 80% decrease in lifetime after the annealing. This implies that the Cu in a CZTS matrix tends to
diffuse to a lesser extent in Si as compared to metallic Cu, despite the fact that pure Cu exists in CZTS as one of the main precursors. Ultimately, despite the 40% decrease in lifetime for Si/(TiN)/CZTS samples, the absolute final lifetime is still ~1.6 ms, which corresponds to an implied $V_{oc}$ above 700 mV. This encouraging result indicates that the performance of the bottom silicon cell may not necessarily be compromised as a result of the CZTS synthesis.

The TOF-SIMS depth profile results show that elements from CZTS can diffuse into the silicon layer when no TiN barrier is present, as revealed by the smeared interface between the CZTS and Si layers (Fig. 2 a). On the other hand, the sample with 25 nm of TiN could effectively suppress the in-diffusion into the silicon substrate (Fig. 2 b). This is not too well-aligned with our previous findings in FIG 1.b. Thus, further investigations using SIMS and DLTS, where both CZTS and TiN are removed prior to measurements, are planned to further study the observed trends.

Finally, 10 asymmetrically passivated device wafers were prepared, and the measured $i-V_{oc}$ depicted in FIG 1c. These samples will be used to fabricate monolithic tandem devices with different barrier configurations, to confirm the observations also at the device level.

4. REFERENCES