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Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications

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***Abstract*—Resonant converter topologies have the ability to eliminate switching losses through zero-voltage switching, making them well-suited for switching operation in the MHz frequency range. However, these types of converters are traditionally very sensitive to changes in input voltage and power level, making them unsuitable as power factor correcting AC-DC converters. This paper present a throughout analysis of the operation of a class DE converter in order to derive a set of conditions, under which it can achieve constant input impedance over a wide input voltage range (60-325 V DC) with constant output voltage (450 V DC) and thus be operated as a PFC converter, while maintaining zero voltage switching across the full range. The operation is experimentally verified under DC-DC operation for different power levels at a series of input voltages within the specified range. The implemented prototype achieves conversion efficiencies of up to 94 % and handles up to 105 W of power at switching frequencies of 2 MHz and above, while achieving constant input impedance over the full input voltage range, enabling its use as a power factor correcting converter.**

***Index Terms*—AC-DC power conversion, power factor correction, resonant converters, zero voltage switching, wide-bandgap semiconductors**

I. Introduction

The recent years have seen many advances in the field of power converters operating at switching frequencies in the high frequency (HF, 3-30 MHz), or very high frequency (VHF, 30-300 Mhz) ranges [1]–[4]. By the use of resonant converter topologies [5], the converter switching losses are mostly eliminated, allowing converters to be operated at much higher frequencies than previously feasible, greatly reducing the size and cost of passive energy storage components [6], [7]. Popular resonant converter topologies include the Class E [8], [9], Class DE [10], [11] and Class Φ_2 converters [12].
Through the use of self-oscillating passive gate drivers [13], the need for active gate drivers is eliminated, enabling power converters operating in the range of 30 MHz [14], [15] or even 100 MHz [16]. With the emergence of wide bandgap technologies such as Gallium Nitride (GaN) transistors, this development is further enabled by the improved figures of merit of new switching devices [17], [18], and previous publications have demonstrated active-driven GaN-based switch-mode converters operating at switching frequencies of 10 MHz [19] and even 100 MHz [20].
While resonant converter topologies have enabled increased switching frequencies compared to traditional hard-switched topologies, their control is complicated. Through their ability to operate with zero-voltage switching (ZVS), they can achieve high efficiency under the right operating conditions, but they are very sensitive to changes in loading conditions [21], [22]. As the diode-based rectifiers used in resonant converter topologies are inherently non-linear in their input impedance, this means that these topologies are very sensitive to changes in voltage and power levels, giving them a low dynamic range and making them a less obvious choice for AC/DC applications as power factor correctional (PFC) converters.
Methods compensating for these non-linearities in order to achieve zero-voltage switching over a wider voltage range has previously been described for the class E converter [23]–[26] and LLC converters [27].
Other work describing soft-switching PFC converters with resonant and non-resonant converter topologies include [28]–[34]. In order to function as a PFC converter, a converter must draw an input current proportional to its instantaneous input voltage - meaning that the input impedance of the converter must emulate a constant resistor, R_{in}, over a desired voltage range and that the input power must be defined by (1) in this range.

$$P_{in} = \frac{V_{in}^2}{R_{in}} \tag{1}$$

This paper presents a throughout analysis of the operation of a class DE converter, in order to derive a set of conditions required for the converter to achieve constant input impedance

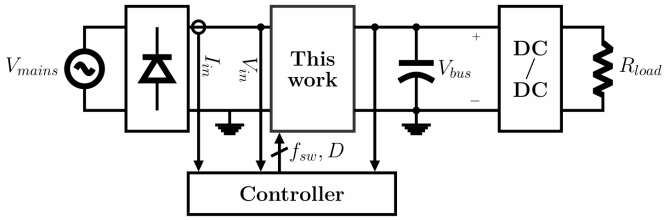

Fig. 1: The presented converter as part of 2-stage AC/DC power supply

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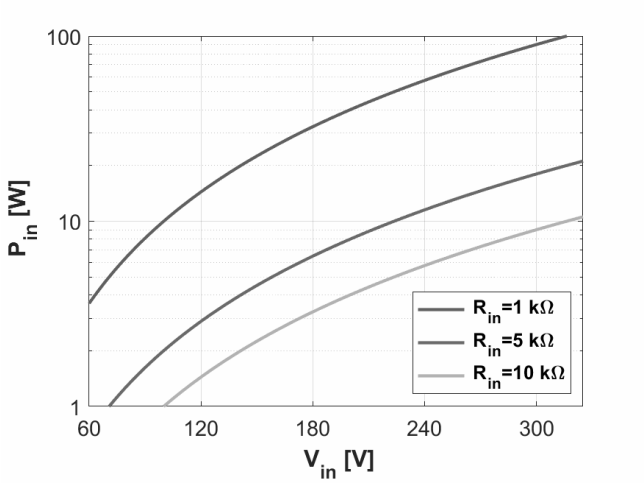


Fig. 2: Input power vs. input voltage for three different impedance levels.

and zero voltage switching over a desired voltage range. This enables the class DE converter to be used as a PFC converter in a system as the one shown in fig. 1. Through careful control of frequency and duty cycle, it is shown that is it possible to use the topology as a PFC converter without the need for any additional components. Open-loop DC-DC operation is demonstrated for a series of operating points with varying input voltage and power levels. The specifications of the lab prototype is shown in table I and the relation between input voltage and power for three different values of input resistance is shown in fig. 2.

Quantity	Symbol	Value
Input voltage	V_{in}	60 V - 325 V
Output voltage	V_o	450 V_{DC}
Input resistance	R_{in}	$1000 - 10,000\ \Omega$

TABLE I: Prototype specifications.

II. Topology analysis

The converter is designed as a class DE resonant converter consisting of a class DE inverter [10], [11] and a class DE rectifier [10], [35] connected through a series resonant tank as shown in fig. 3. Compared to other resonant converter topologies, the class DE converter has the benefits of lower voltage stresses on the semiconductor devices, and that it incorporates only a single magnetic component. As magnetic components are often bulky, this allows for a more compact design. The primary disadvantage of the topology is the floating high-side switch on the inverter side, which complicates the driving of the switches.

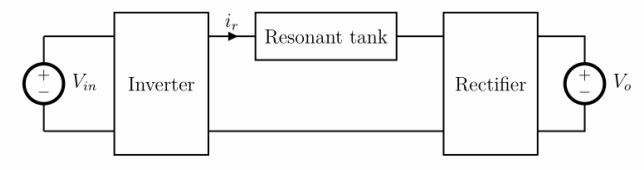


Fig. 3: Block diagram of resonant converter

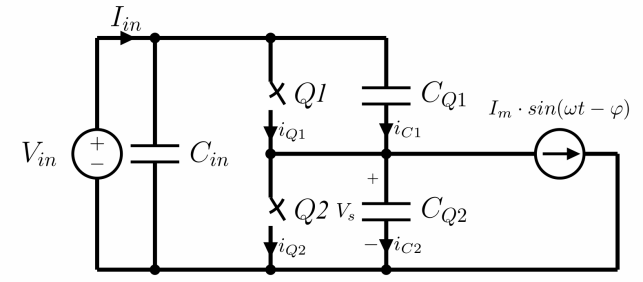


Fig. 4: Class DE inverter schematic

By performing a throughout mathematical analysis of the ideal converter operation, the conditions that must be met for the converter to function in the desired voltage and power range are determined. By first analyzing the operation of inverter and rectifier separately, the conditions can be determined by assuming conservation of power.

Both circuits have been analyzed in detail in previous literature [11], [36]. However, as the intended converter application in this work is power factor correction, the following analysis will be more focused on quantities related to this application, with most operational parameters being referred to the input voltage and resistance, rather than output power. Furthermore, this analysis sacrifices the traditional requirement of zero-$\frac{dv}{dt}$ switching in the inverter in exchange for the option to achieve constant input resistance over a wide input range.

A. Inverter analysis

The mathematical analysis starts with the inverter circuit, in order to determine its required load impedance, which is later needed for impedance matching of the rectifier.
The class DE inverter (fig. 4) consists of a transistor half-bridge with shunt capacitors across the transistors. During analysis the two switches are assumed to be driven with an equal duty cycle, D_i, and 180 degrees of phase shift between them while the inverter output current is a pure sine wave at the switching frequency. Traditionally the inverter is designed for the resonant current to be in phase with the driving signal for the high-side switch in order to achieve zero-$\frac{dv}{dt}$ switching. However, this design introduces a phase lag, φ, in order to give an additional degree of freedom. Throughout analysis, the parameter C_s is introduced as an expression for the total capacitance on the switch node, i.e. the sum of capacitors C_{Q1} and C_{Q2}, where I_m is the resonant current amplitude and ω_{sw} is the switching frequency in radians per second.
The inverter has four states of operation as described in table II: one conducting state for each switch (states 1 and 3) and two charge/discharge states for the shunt capacitors (states 2 and 4), in order to achieve zero voltage switching.

State	Conducting switch	i_{Q1}	$i_{C2} - i_{C1}$
1	Q1	$I_m \cdot sin\left(\omega_{sw} t - \varphi\right)$	0
2	-	0	$-I_m \cdot sin\left(\omega_{sw} t - \varphi\right)$
3	Q2	0	0
4	-	0	$-I_m \cdot sin\left(\omega_{sw} t - \varphi\right)$

TABLE II: Operating states of class DE inverter.

The DC input current of the inverter, I_{in}, is found by calculating the average current drawn from the input voltage source, V_{in}, over a full switching cycle. In steady state operation, the average current through capacitors C_{in} and C_{Q1} will be zero, and the DC input current will be equal to the average value of the current in the high side switch, $Q1$. An expression for the DC input current, I_{in}, is found by calculating the average value of i_{Q1} over a full switching cycle. As this switch is only conducting in state 1, the switch current only needs to be integrated over this state.

$$I_{in} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{Q1} dt \tag{2}$$

$$= \frac{I_m}{T_{sw}} \int_0^{D_i \cdot T_{sw}} sin\left(\omega_{sw} t - \varphi\right) dt \Leftrightarrow$$

$$I_{in} = \frac{I_m}{2\pi} \cdot \left(cos(\varphi) - cos(2\pi D_i - \varphi)\right) \tag{3}$$

The voltage at the switch node, V_s, is equal to either the input voltage or zero when switches *Q1* and *Q2* are turned on in states 1 and 3, respectively. During the dead-time in states 2 and 4, the resonant current charges and discharges the voltage across capacitors C_1 and C_2.

$$V_s(t) = \begin{cases} V_{in} & \texttt{in state 1} \\ V_{in} - \frac{I_m}{C_s} \int_{D_i T_{sw}}^{t} sin(\omega_{sw} t - \varphi) dt & \texttt{in state 2} \\ 0 & \texttt{in state 3} \\ -\frac{I_m}{C_s} \int_{\frac{T_{sw}}{2} + D_i T_{sw}}^{t} sin(\omega_{sw} t - \varphi) dt & \texttt{in state 4} \end{cases} \tag{4}$$

An expression for the input voltage is found by determining the state 4 value of V_s at time $t = T_{sw}$. Assuming ZVS, the value at this time should be equal to V_{in}:

$$V_{in} = V_s(T_{sw}) = \frac{I_m}{\omega_{sw} C_s} \cdot \left(cos(\varphi) + cos(2\pi D_i - \varphi)\right) \tag{5}$$

Combining (4) and (5) gives a simpler expression for the switch node voltage.

$$V_s(t) = \begin{cases} V_{in} & \texttt{in state 1} \\ V_{in} \cdot \frac{cos(\omega_{sw} t - \varphi) + cos(\varphi)}{cos(2\pi D_i - \varphi) + cos(\varphi)} & \texttt{in state 2} \\ 0 & \texttt{in state 3} \\ V_{in} \cdot \frac{cos(\omega_{sw} t - \varphi) + cos(2\pi D_i - \varphi)}{cos(2\pi D_i - \varphi) + cos(\varphi)} & \texttt{in state 4} \end{cases} \tag{6}$$

Fig. 5 shows normalised waveforms for V_s, i_r (resonant current) and i_{Q1}. Combining and rewriting (3) and (5) gives expressions that can be used to find φ and D_i for a given set of parameters:

$$cos(\varphi) = \frac{\pi f_{sw} C_s V_{in} + \pi I_{in}}{I_m} \tag{7}$$

$$cos(2\pi D_i - \varphi) = \frac{\pi f_{sw} C s V_{in} - \pi I_{in}}{I_m} \tag{8}$$

Lastly, the required impedance at the inverter output is determined, in order to achieve the desired resonant current amplitude and phase. This is done through a first harmonic analysis of the switch-node voltage $V_s(t)$, which is considered in two parts - an active part in phase with the resonant current, labelled $V_{s,R}$, and a reactive part leading the resonant current by 90 degrees, labelled $V_{s,X}$. The active and reactive components of the switch-node voltage (6) are determined from Fourier analysis:

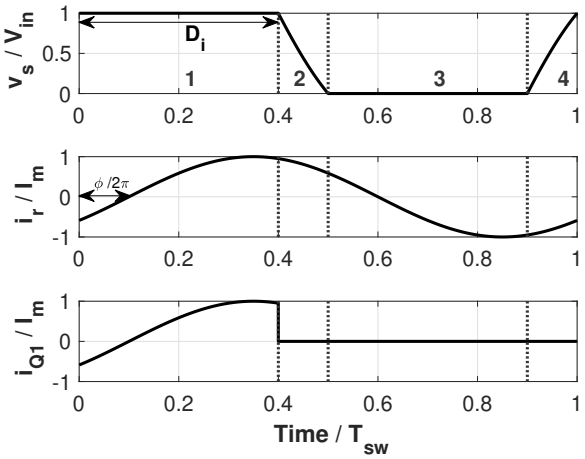


Fig. 5: Class DE inverter waveforms, for $D_i = 40\ \%$ and $\varphi = \frac{\pi}{5}$

$$V_{s,R} = \frac{2}{T_{sw}} \cdot \int_0^{T_{sw}} V_s(t) \cdot sin(\omega_{sw} \cdot t - \varphi) dt \tag{9}$$

$$= \frac{V_{in}}{\pi} \cdot \left(cos(\varphi) - cos(2\pi D_i - \varphi)\right)$$

$$V_{s,X} = \frac{2}{T_{sw}} \cdot \int_0^{T_{sw}} V_s(t) \cdot cos(\omega_{sw} \cdot t - \varphi) dt \Leftrightarrow \tag{10}$$

$$V_{s,X} = \frac{V_{in}}{2\pi} \cdot \left(\frac{K_1 + K_2 + \pi - 2\pi D_i}{cos(\varphi) + cos(2\pi D_i - \varphi)}\right) \tag{11}$$

where the expressions K_1 and K_2 are functions of φ and D_i:

$$K_1 = sin(\varphi) \cdot cos(\varphi) \tag{12}$$

$$K_2 = sin(2\pi D_i - \varphi) \cdot cos(2\pi D_i - \varphi) \tag{13}$$

The required active and reactive load impedances, R_{inv} and X_{inv} respectively, are calculated by dividing the voltage components by the resonant current amplitude I_m. Through (3), the impedances can be expressed in terms of input voltage and current, as well as φ and D_i.

$$R_{inv} = \frac{V_{s,R}}{I_m} = \frac{V_{in}}{2\pi^2 I_{in}} \cdot \left(cos(\varphi) - cos(2\pi D_i - \varphi)\right)^2 \tag{14}$$

$$X_{inv} = \frac{V_{s,X}}{I_m} = \frac{V_{in}}{4 \cdot \pi^2 \cdot I_{in}} \cdot (K_1 + K_2 + \pi - 2\pi D_i) \cdot K_3 \tag{15}$$

where the expressions K_3 is a function of φ and D_i:

$$K_3 = \frac{cos(\varphi) - cos(2\pi D_i - \varphi)}{cos(\varphi) + cos(2\pi D_i - \varphi)} \tag{16}$$

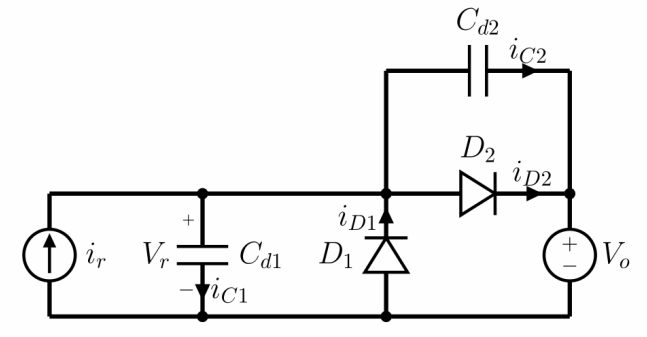


Fig. 6: Class DE rectifier schematic

B. Rectifier analysis

A similar analysis is applied to the class DE rectifier. The class DE rectifier (fig. 6) consists of a diode half bridge with shunt capacitors connected across the diodes. The shunt capacitors include any parasitic capacitance of the diodes, as well as any externally added capacitance. By assuming a constant output voltage and a purely sinusoidal input current, the rectifier can be analysed with equal diode conduction duty cycles, denoted D_r. The sinusoidal input current source represents an ideal resonant inverter, and is replaced by a class DE inverter in the full converter.

Previous work [36] has analyzed the topology in detail with its output power described as functions of input current amplitude and diode duty cycle, but in this case it is more desirable to calculate the required current amplitude as a function of power and switching frequency, as the primary quantity of interest for PFC applications is the input current, or input impedance, of the full converter.
The input current i_r is a perfect sine wave with amplitude I_m, $i_r = I_m \cdot sin(\omega_{sw} t)$, and the rectifier operation can be divided into 4 different states, as shown in table III. Each diode conducts for a duty cycle D_r, while the shunt capacitors charge and discharge in the remaining time. As the net average current through the shunt capacitors over a switching cycle is zero, any charge carried to the output is flowing through the diode $D2$.

Fig. 7 shows waveforms for input current and voltage, as well as the current through the high-side diode, $D2$.
The amplitude of the resonant current, I_m can be expressed as a function of output voltage, output current, switching frequency and the sum of the two shunt capacitors, denoted C_r, by looking at the charge transfer for the positive half cycle of the resonant current, states A and B.
In state A, before the diode $D2$ starts conducting, the resonant current transfers the amount of charge needed to raise the

State	Conducting diode	i_{D2}	$i_{C1} + i_{C2}$
A	-	0	i_r
B	D2	i_r	0
C	-	0	i_r
D	D1	0	0

TABLE III: Operating states of class DE rectifier.

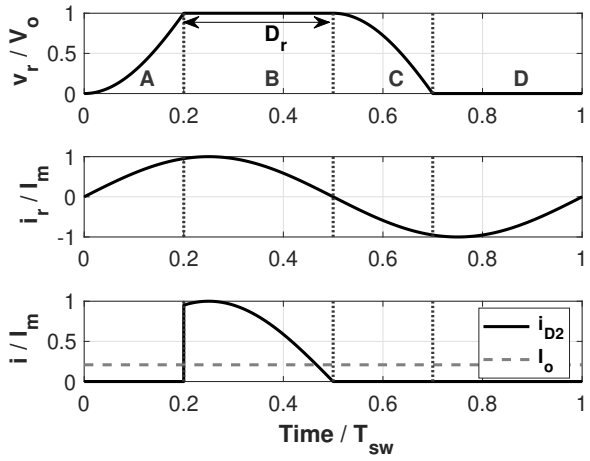


Fig. 7: Class DE rectifier waveforms, for $D_r = 30\%$

voltage v_r to the level of the output voltage V_o. The shunt capacitors store this charge during diode conduction in state B.

$$\int_0^{T_{sw}\cdot\left(\frac{1}{2}-D_r\right)} I_m \cdot sin(\omega_{sw} t) dt = C_r \cdot V_o \tag{17}$$

In state B, the diode $D2$ is conducting and the resonant current transfers an amount of charge to the rectifier output. This charge is equal to the average output current multiplied by the switching period, T_{sw}.

$$\int_{T_{sw}\cdot\left(\frac{1}{2}-D_r\right)}^{T_{sw}\cdot\frac{1}{2}} I_m \cdot sin(\omega_{sw} t) dt = I_o \cdot T_{sw} = \frac{2 \cdot \pi \cdot I_o}{\omega_{sw}} \tag{18}$$

Combining (17) and (18), an expression for the required resonant current amplitude as a function of V_o, I_o, C_r and the switching frequency is obtained:

$$\int_0^{\frac{T_{sw}}{2}} I_m \cdot sin(\omega_{sw} t) dt = \frac{2 \cdot I_m}{\omega_{sw}} \Leftrightarrow \tag{19}$$

$$\frac{2 \cdot I_m}{\omega_{sw}} = C_r \cdot V_o + \frac{2 \cdot \pi \cdot I_o}{\omega_{sw}} \Leftrightarrow \tag{20}$$

$$I_m = \pi \cdot f_{sw} \cdot C_r \cdot V_o + \pi \cdot I_o \tag{21}$$

At the switching frequency, the input impedance of the rectifier resembles an RC-series circuit, with resistance R_{rect} and capacitance C_{rect} depending on the output power.
The equivalent input resistance of the rectifier for a given output current can be determined from (21) by assuming 100% efficiency.

$$R_{rect} \cdot \frac{I_m^2}{2} = I_o \cdot V_o \Leftrightarrow \tag{22}$$

$$R_{rect} = \frac{2 \cdot I_o \cdot V_o}{I_m^2} = \frac{2 \cdot I_o \cdot V_o}{\left(\pi \cdot f_{sw} \cdot C_r \cdot V_o + \pi \cdot I_o\right)^2} \tag{23}$$

The equivalent input capacitance can be determined using fourier analysis, and a general expression dependent on the diode duty cycle was derived in [36].

$$C_{rect} = \frac{\pi \cdot C_r}{\pi \cdot (1 - 2D_r) + K_r} \tag{24}$$

Where K_r is a function of diode duty cycle:

$$K_r = sin(2\pi D_r) \cdot cos(2\pi D_r) \tag{25}$$

The duty cycle is described as a function of the other parameters by re-evaluating (17) and combining with (21):

$$\int_0^{T_{sw}\cdot\left(\frac{1}{2}-D_r\right)} sin(\omega_{sw}t)dt = \frac{C_r \cdot V_o}{I_m} = \frac{1+cos(2\pi D_r)}{\omega_{sw}} \Leftrightarrow \tag{26}$$

$$D_r = \frac{1}{2\pi} \cdot cos^{-1}\left(\frac{f_{sw}\cdot C_r \cdot V_o - I_o}{f_{sw}\cdot C_r \cdot V_o + I_o}\right) \tag{27}$$

Equations (23), (24) and (27) express the equivalent input resistance and capacitance of the class DE rectifier for any combination of V_o, I_o, C_r and f_{sw}.

C. Full converter

The class DE rectifier is connected to the output of the class DE inverter through a series resonant tank, sized to meet the reactance requirement of the inverter.
With the two circuits connected, the current sources in fig. 4 and 6 are replaced by the other half-circuit and the resonant tank, with the inverter output current being equal to the rectifier input current.
By inserting (21) into (7), an expression for the phase angle, φ, can be written:

$$cos(\varphi) = \frac{\pi f_{sw} C_s V_{in} + \pi I_{in}}{\pi f_{sw} C_r V_o + \pi I_o} \tag{28}$$

For the topology to function as a PFC converter, it must achieve a constant input impedance R_{in} over the full input voltage range, in order to ensure a proportional relationship between the input voltage and current. The input current can be expressed in terms of input voltage and resistance:

$$I_{in} = \frac{V_{in}}{R_{in}} \tag{29}$$

Since the resonant topology has negligible switching losses, considering ZVS operation, the losses in the converter are assumed to be dominated by the losses in the resonant tank. With an efficiency η_{res} in the resonant circuit, the output current can be expressed as:

$$I_o = \eta_{res} \cdot \frac{V_{in} I_{in}}{V_o} = \eta_{res} \cdot \frac{V_{in}^2}{V_o \cdot R_{in}} \tag{30}$$

Where η_{res} is determined by the ratio of the rectifier input resistance and the equivalent series resistance (ESR) of the resonant tank:

$$\eta_{res} = \frac{R_{rect}}{R_{rect} + ESR} \tag{31}$$

The ESR of the resonant tank includes ESR of the resonant capacitor as well as winding and core losses in the resonant inductor.
Equation (28) can now be rewritten.

$$cos(\varphi) = \frac{f_{sw} C_s R_{in} V_{in} V_o + V_{in} V_o}{f_{sw} C_r R_{in} V_o^2 + \eta_{res} \cdot V_{in}^2} \tag{32}$$

In order for φ to be a real number, it is required that $cos(\varphi) \leq 1$. By rearranging (32), a constraint for the converter operation can be written:

$$f_{sw} \cdot R_{in} \geq \frac{V_{in} V_o - \eta_{res} \cdot V_{in}^2}{V_o \cdot (C_r V_o - C_s V_{in})} \tag{33}$$

For a given set of voltages and capacitances this gives a minimum achievable input resistance for a specific switching frequency. An increase in η_{res} will reduce the minimum input resistance.
Equations (21), (29) and (30) are inserted into (8) in order to determine the inverter duty cycle:

$$cos(2\pi D_i - \varphi) = \frac{f_{sw} C_s R_{in} V_{in} V_o - V_{in} V_o}{f_{sw} C_r R_{in} V_o^2 + \eta_{res} \cdot V_{in}^2} \tag{34}$$

Combining (32) and (34) makes it possible to reduce (16).

$$K3 = \frac{1}{f_{sw} C_s R_{in}} \tag{35}$$

Inserting (35) and (29) into (15) gives a simpler expression for the required load reactance seen from the inverter side.

$$X_{inv} = \frac{1}{4 \cdot \pi^2 \cdot f_{sw} C_s} \cdot (K_1 + K_2 + \pi - 2\pi D_i) \tag{36}$$

Expressions for the current phase angle, φ, and inverter duty cycle, D_i, are derived from (32) and (34).

$$\varphi = cos^{-1}\left(\frac{f_{sw} C_s R_{in} V_{in} V_o + V_{in} V_o}{f_{sw} C_r R_{in} V_o^2 + \eta_{res} \cdot V_{in}^2}\right) \tag{37}$$

$$D_i = \left(cos^{-1}\left(\frac{f_{sw} C_s R_{in} V_{in} V_o - V_{in} V_o}{f_{sw} C_r R_{in} V_o^2 + \eta_{res} \cdot V_{in}^2}\right) + \varphi\right) \cdot \frac{1}{2\pi} \tag{38}$$

The expression for the rectifier diode duty cycle (27) can be rewritten using (30)

$$D_r = \frac{1}{2\pi} \cdot cos^{-1}\left(\frac{f_{sw}\cdot C_r \cdot R_{in} \cdot V_o^2 - \eta_{res} \cdot V_{in}^2}{f_{sw}\cdot C_r \cdot R_{in} \cdot V_o^2 + \eta_{res} \cdot V_{in}^2}\right) \tag{39}$$

The reactance of the resonant tank needs to cancel out the reactance of the rectifier input capacitance found in (24) and provide the required load reactance for the inverter as found in (36). For any set of input- and output voltages, input resistance, node capacitances, switching frequency and resonant tank efficiency, a required reactance can be calculated.

$$X_{tank} = X_{inv} + \frac{1}{\omega_{sw} \cdot C_{rect}} \Leftrightarrow \tag{40}$$

$$X_{tank} = \frac{K_1 + K_2 + \pi \cdot (1 - 2D_i)}{4\pi^2 f_{sw} C_s} + \frac{K_r + \pi \cdot (1 - 2D_r)}{2\pi^2 f_{sw} C_r} \tag{41}$$

The inverter and rectifier circuits of the class DE converter are connected through a series resonant tank consisting of an inductor, L_{tank}, and a capacitor C_{tank}. In order to achieve zero-voltage switching and constant input resistance, the switching frequency and duty cycle of the class DE inverter must be controlled in order to achieve a match between the required reactance determined by (41) and the reactance of the resonant tank:

$$\omega_{sw} \cdot L_{tank} - \frac{1}{\omega_{sw} \cdot C_{tank}} = X_{tank} \tag{42}$$

III. Calculation of operating point

Due to the highly nonlinear nature of (42), generic, symbolic solutions are difficult to calculate. Instead, numerical solutions are found for a specific application, based on the specifications in table I. A Class DE converter is designed to meet the specs and a series of operating points are calculated.

A. Semiconductors

The first step is to select suitable switches and diodes for the two half-bridges in the converter. For the switches in the inverter half bridge, the devices must have a voltage rating higher than the peak input voltage, 325 V, and a current ranting higher than the peak input current of converter. The peak input current is found at the maximum input voltage and lowest input resistance, $I_{in,max} = \frac{325\ V}{1000\ \Omega} = 325\ mA$. Furthermore, it is desirable to select devices with low parasitic shunt capacitance, in order to allow for fast switching of the inverter bridge.

For these reasons, the selected switches are the GS66502B GaN transistors from GaN Systems [37]. With voltage and current ratings of 650 V and 7.5 A respectively, these devices satisfy the requirements, with a parasitic shunt capacitance, C_{oss}, in the range of tens of pF. In order to estimate the time-related effective shunt capacitance of the devices, a simulation is performed in LTSpice, using the testbench shown in fig. 8. A current source is connected to the device under test in parallel with an ideal diode connected to a voltage source with the desired test voltage. Once the voltage across the switch is charged to the level of the bias voltage, the diode will start conducting the full input current. The time when this occurs is denoted t_{charge}. By knowing the charging time, the bias voltage and the test current, the effective capacitance is calculated using (43).

$$C_Q = \frac{t_{charge} \cdot I_{test}}{V_{test}} \tag{43}$$

For the selected switch, the effective capacitance for charging from 0-325 V is found to be 54 pF. For lower voltage levels this value will be higher due to nonlinearities in the device capacitance, and this is taken into account for lower input voltages.

A graph of the time-related effective value of C_s vs. input voltage, using two GS66502B GaNFETs is shown in fig. 9. It is seen that the effective value of C_s is varying by a factor of two over the range of operation.

For the rectifier bridge, the chosen diodes are GB01SLT06 from GeneSiC Semiconductor [38]. These devices are rated for 650 V and 2.5 A, making them suitable for the design.

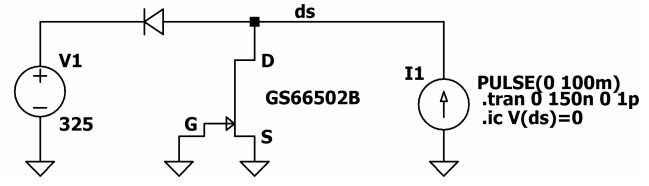


Fig. 8: LTSpice test bench for determination of switch shunt-capacitance

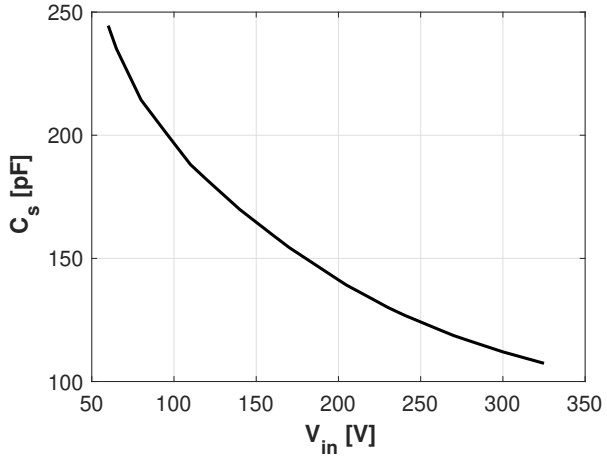


Fig. 9: Simulated values of C_s vs. input voltage using two GS66502B GaNFETs

Through simulations similar to the ones performed on the switches, the effective shunt capacitance of the diodes is found to be around 21 pF when charging from 0-450 V. As the output voltage is considered constant for all operating points, this capacitance value is assumed to be constant as well.

The simulated values for parasitic capacitances are used to calculate theoretical solutions for the switching frequency and duty cycle at different operating points. As the parasitics of the physical components may deviate from those in the simulation models, the switching frequency and duty cycle might need slight adjustments from the calculated values in order to ensure zero-voltage switching and constant input resistance of the converter. Parameter mismatches between the switching devices in the circuit are of no consequence to the converter operation, as the important parameter is the total capacitance on the switch node, C_s, and not its distribution between the devices.

B. Shunt capacitors

Rearranging (33) gives a minimum value of the rectifier shunt capacitance, C_r, based on the choice of inverter switches. This minimum value depends on the switching frequency, input voltage and efficiency of the converter, and the choice of capacitance affects the solution space of (42). As a starting point, the minimum capacitance is calculated at the peak input power (peak input voltage and minimum input resistance) and a switching frequency of 2 MHz, as this has previously been found to be the optimum frequency in terms of magnetic components sizes [39]. For this calculation the resonant tank efficiency, η_{res}, is assumed to be 95 % under the specified conditions. If the efficiency turns out to be lower than this, the switching frequency might have to be increased slightly to compensate.

$$C_r \geq \frac{V_{in}V_o - \eta_{res} \cdot V_{in}^2}{f_{sw}R_{in}V_o^2} + C_s\frac{V_{in}}{V_o} \Leftrightarrow \tag{44}$$

$$C_r \geq \frac{325\ V \cdot 450\ V - 0.95 \cdot (325\ V)^2}{2\ MHz \cdot 1\ k\Omega \cdot (450\ V)^2} + 108\ pF \cdot \frac{325\ V}{450\ V} \tag{45}$$
$$= 191\ pF$$

Since the combined parasitic capacitance of the two diodes is only 42 pF, it is evident that external capacitance is required for the converter to function under these conditions. For this reason, a external shunt capacitor, $C_{r,ext}$, of 150 pF is added, bringing the total size of C_r to 192 pF.
Decoupling capacitors are placed at the inverter input and rectifier output in order to filter out the residuals at the switching frequency.

C. Resonant tank

Knowing the capacitances C_s and C_r, the requried resonant tank reactance, X_{tank}, can be plotted as a function of the input voltage and switching frequency, as shown in fig. 10.
The resonant tank needs to be able to meet the reactance requirement at any input voltage by only adjusting the switching frequency. In order to choose a size for the resonant inductor, the input resistance of the rectifier is calculated at peak power an 2 MHz. This is done using (23) and (30):

$$R_{rect} = \frac{2\eta_{res} V_{in}^2 V_o^2 R_{in}}{\left(\pi f_{sw} C_r R_{in} V_o^2 + \pi \eta_{res} V_{in}^2\right)^2} = 130\ \Omega \tag{46}$$

According to [5], the resonant current can be assumed to have a sinusoidal shape when the loaded quality factor of the resonant tank relative to the rectifier input resistance is larger than 2.5. In this converter, the inductor is chosen to be approximately 50 percent larger than this, in order to have higher harmonic suppression in the resonant tank and make the comparison between the theory and measurements easier.

$$L_{tank} = 1.5 \cdot 2.5 \cdot \frac{R_{rect}}{\omega_{sw}} = 2.5 \cdot 1.5 \cdot \frac{130\ \Omega}{2\pi \cdot 2\ MHz} = 39\ \mu H \tag{47}$$

Based on this inductor, the resonant tank capacitor is sized to meet the reactance requirement for all input voltages. In Fig. 11 the calculated reactance requirement from (41) is plotted for a series of different input voltages over a wide frequency range. It is seen that the $40\ \mu H$ inductor in series with a 340 pF capacitor is able to meet the reactance requirement for all input levels.

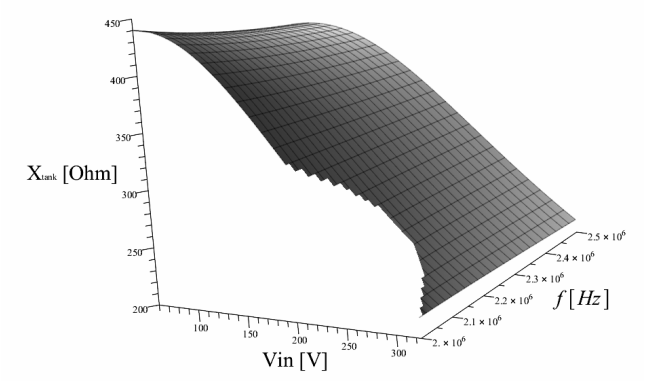


Fig. 10: Required resonant tank reactance vs. V_{in} and f_{sw}

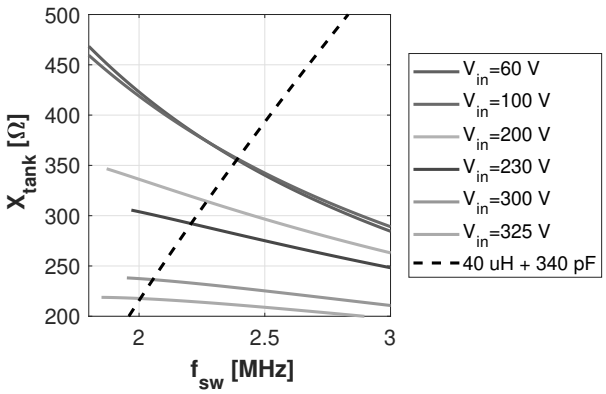


Fig. 11: Calculated values for required resonant tank reactance vs. reactance of the selected resonant tank.

Once again assuming a switching frequency of 2 MHz and a resonant tank efficiency of 95 %, the inductor current amplitude at the peak input voltage is calculated by combining (21) and (30).

$$I_{m,max} = \pi \cdot 2\ MHz \cdot 192\ pF \cdot 450\ V + \frac{0.95 \cdot \pi \cdot (325\ V)^2}{1\ k\Omega \cdot 450\ V} \tag{48}$$
$$= 1.24\ A$$

Based on the same parameters, the peak AC voltage across the resonant capacitor is calculated:

$$V_{C_{tank},max} = I_{m,max} \cdot \frac{1}{\omega_{sw} \cdot C_{tank}} \tag{49}$$
$$= \frac{1.24\ A}{2 \cdot \pi \cdot 2\ MHz \cdot 340\ pF} = 290\ V$$

In addition to this, the capacitor needs to store a DC voltage of up to V_o, resulting in a maximum voltage of around 740 V. A $40\ \mu H$ inductor with an equivalent large-signal AC series resistance of 6 Ω at 2 MHz is wound using a $40 \times 50\ \mu m$ copper litz-wire and an EFD 15/8/5 core made of Ferroxcube 3F46 material. Based on this ESR, and the rectifier input resistance calculated in (46), the expected η_{res} at peak power is calculated from (31).

$$\eta_{res} = \frac{130\ \Omega}{130\ \Omega + 6\ \Omega} = 95.6\ \% \tag{50}$$

This value is seen to be close to the assumed value of 95 %. Fig. 12 shows the circuit diagram for power stage of the implemented converter, and table IV shows a list of the selected components.

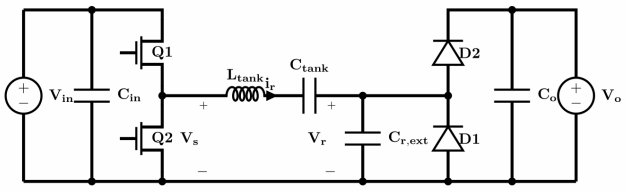


Fig. 12: Converter power stage

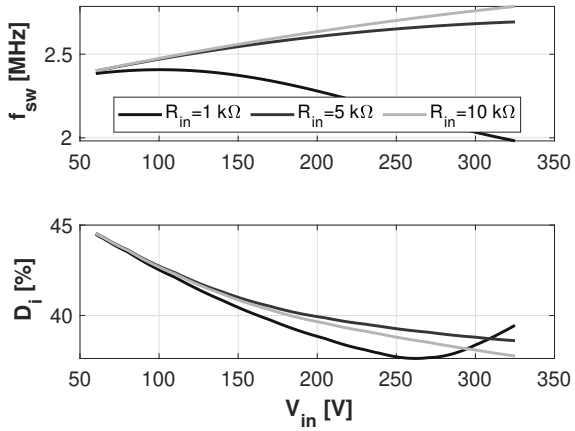


Fig. 13: Calculated switching frequency and duty cycle vs. input voltage

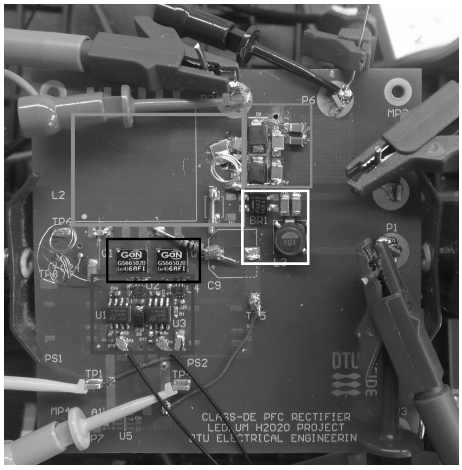


Fig. 14: Converter prototype with marked subcircuits. Gate driver (red), input filter (white), inverter (black), rectifier (green) and resonant tank[1] (cyan).

For the chosen resonant tank, the required switching frequencies and duty cycles within the input voltage range are calculated for a number of different input resistances. The calculated operating points are shown in fig. 13. It should be noted that these operating points assume a resonant tank efficiency, η_{res}, of 95%, which might not be the case under all conditions. Due to this, and any non-linearities in the resonant tank, the operating points of a physical converter will need fine-tuning in order to achieve the desired input impedance.

Component	Model / Size
Q1, Q2	GaN Systems GS66502B
D1, D2	GeneSiC GB01SLT06
C_{in}	50 nF
C_{tank}	340 pF
C_o	25 nF
$C_{r,ext}$	150 pF
L_{tank}	40 μH

TABLE IV: Selected components for the prototype.

IV. Experimental verification

A converter prototype is built (fig. 14) and tested in the laboratory. Converter operation is verified at a number of different input voltages for input resistances of 1, 5 and 10 $k\Omega$. Across the measurements, the converter output is connected to a constant voltage load of 450 V representing a large DC bus capacitor. Gate signals for the inverter switches are generated externally by a Rigol DG1062 signal generator and fed through a set of Si8610 digital isolators from silicon labs and a set of UCC27611 gate drivers from Texas Instruments. The current, voltage and power at the converter input and output is measured using a N4L PPA 5530 Precision Power Analyzer, and the input impedance of the converter is calculated from these values.
A schematic of the experimental setup including test points is shown in fig. 15.

Starting from the calculated values, the switching frequency is tuned in order to achieve the desired input impedance. A comparison between the calculated switching frequencies and the ones used in the measurements is shown in fig. 16.
Three sets of measured waveforms are shown in fig. 17. The measurements are performed at $V_{in} = 325\ V$ for 3 different input impedances. As the impedance level increase, the resonant current is seen to drop in amplitude and increase in frequency while the duty cycle of the rectifier diodes are reduced.

[1]Resonant inductor is mounted on the bottom side of the circuit board.

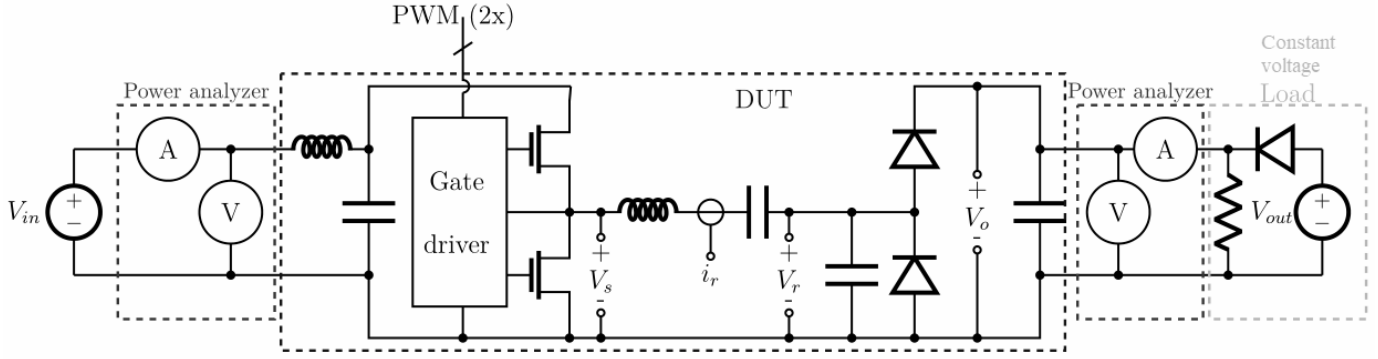


Fig. 15: Diagram of the measurement setup.

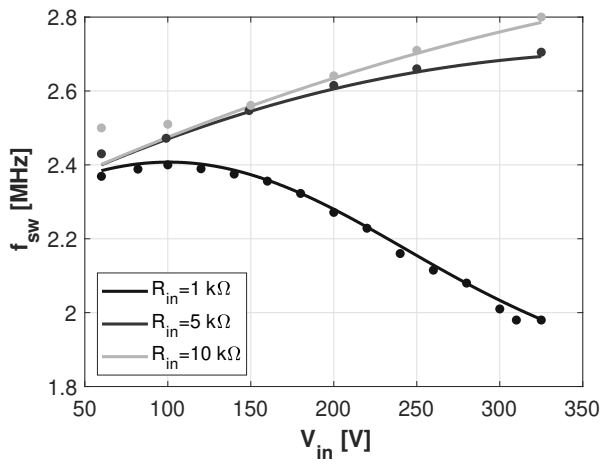
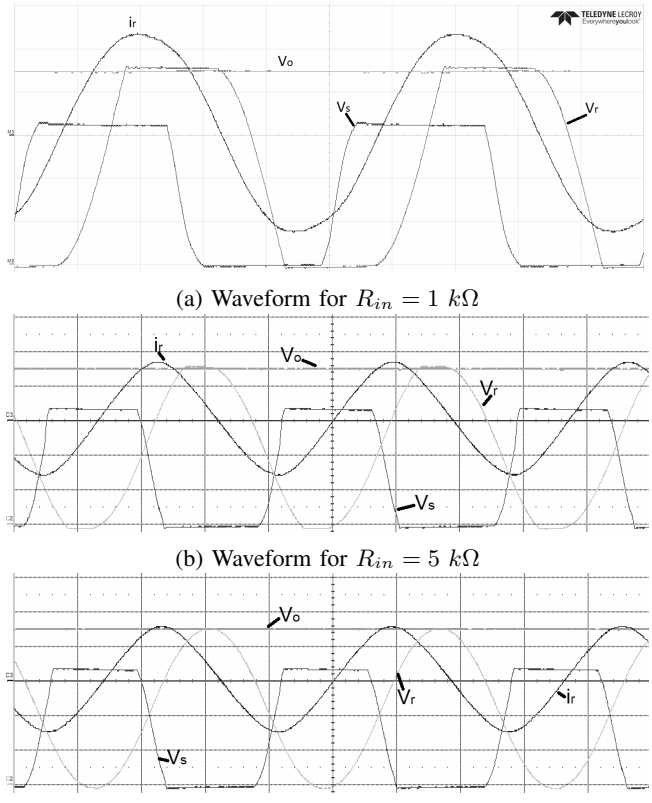


Fig. 16: Comparison of calculated (lines) and experimental (dots) switching frequencies for different input impedances.

The measured input impedances relative to the ideal values are shown in fig. 18, and is seen to be within 2 percent deviation of the target values.
From the measured values of the input impedance, an input current waveform is extrapolated for a European mains AC input voltage (fig. 19), assuming a diode rectifier bridge is placed at the converter input and that a control loop sets the



(a) Waveform for $R_{in} = 1\ k\Omega$

(b) Waveform for $R_{in} = 5\ k\Omega$

(c) Waveform for $R_{in} = 10\ k\Omega$

Fig. 17: Measured waveforms for V_s (red), V_r (green), V_o (orange) and i_r (blue) for $V_{in} = 325\ V$. Scaling is 100 V/div and 500 mA/div on the y-axis and 200 ns/div on the x-axis.

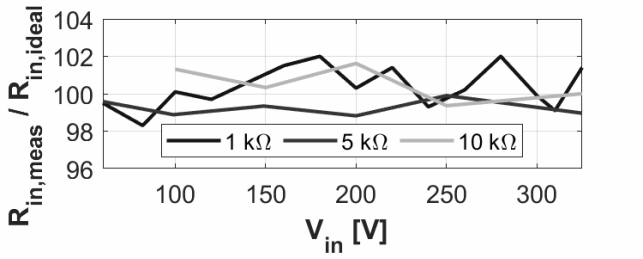


Fig. 18: Measured values for converter input resistance relative to target values.

switching frequency to the values used in the measurements, with the converter being operational when the input voltage exceeds 60 V. Using an adaptive dead-time control technique [40], the duty cycle can be adjusted accordingly such that zero-voltage switching is ensured along the line cycle. From the waveforms in fig. 19, the input current THD and power factor of the converter can be calculated for the different impedance levels. the calculated values are shown in table V. The calculated values assume an ideal input filter, which completely filters out the switching frequency and its higher harmonics while providing no attenuation or phase shift at lower frequencies. A practical filter would introduce a small phase shift in the input current and reduce the power factor of the converter, so such a filter should be designed to ensure that the power factor requirement of the converter is met.

$R_{in,taret}$	THD	Power factor
1 $k\Omega$	5.25 %	99.9 %
5 $k\Omega$	5.2 %	99.9 %
10 $k\Omega$	5.22 %	99.9 %

TABLE V: Extracted THD and Power factor values.

The efficiency of the prototype at different load levels and input voltages is measured using the power analyzer connected to the converter input and output terminals (see fig. 15).
The efficiency is defined as $\eta = \dfrac{P_{out}}{P_{in}}$, and the measured vales are shown in fig. 20. The converter is seen to achieve efficiencies of up to 94 percent at the peak output power.

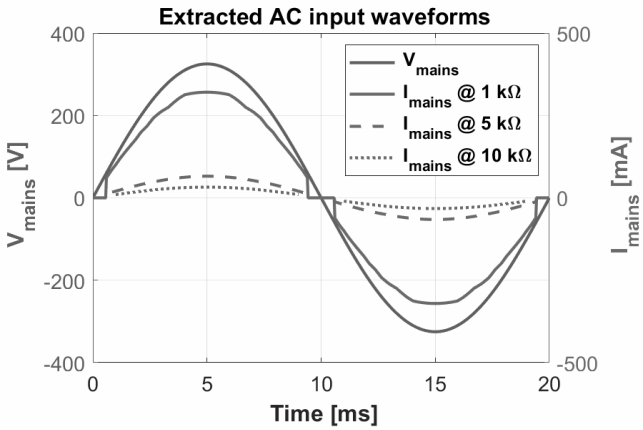


Fig. 19: Extrapolated input waveforms for european mains input.

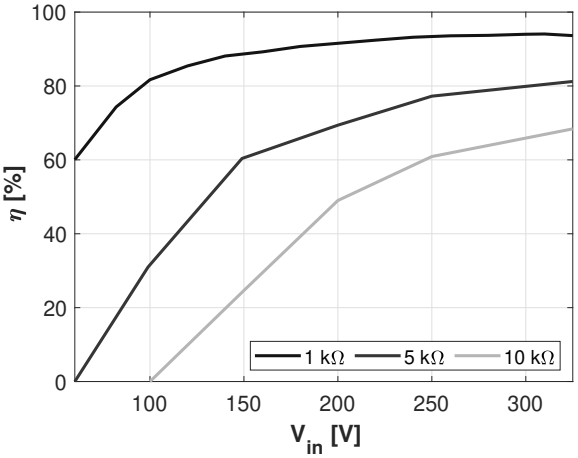


Fig. 20: Measured converter efficiency vs. input voltage for different input resistances.

V. Conclusion

Through mathematical analysis, a set of conditions has been derived for a class DE resonant converter to be operated with a constant input impedance over a wide input voltage range, enabling its use in power factor correction applications. A constructed prototype is tested at various input voltages between 60 and 325 V for input resistances of 1, 5 and 10 $k\Omega$, with measured input impedances within a few percent of the desired values.

With conversion efficiencies reaching as high as $94\ \%$, the prototype is able to convert more than 100 W of power in DC/DC operation without the need for bulky heatsinks. If implemented as an AC/DC converter with a microcontroller generating the gate-signals, the converter can function as a PFC converter with zero voltage switching and small passive components. Based on extrapolation from measured values, the converter is expected to achieve a THD as low as $5.2\ \%$ and a power factor of 0.999 before the input filter for European mains AC input.

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