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Compact High-Speed Envelope Detector Architecture for Ultra-Wideband Communications

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***Abstract*— This letter describes a Schottky diode based envelope detector architecture able to demodulate single-ended signals adopting a single balanced configuration without the use of an external balun. The proposed architecture combines the functionality of a balun and, simultaneously, the rectification of the input signal. The dual functionality of the Schottky diodes applied, leads to a compact configuration that, according to the authors' knowledge, has not ~~ever~~ been shown before. The manufactured prototype is able to demodulate error free a 2.5 Gbps amplitude shift keying (ASK) signal at 8 GHz carrier frequency, achieving a bitrate to frequency carrier ratio (*Δb*) of 31.25 %.**

***Index Terms*— Amplitude modulation; Envelope detector; Microwave detector; Schottky diode; Ultra-Wideband (UWB).**

I. Introduction

Traffic from wireless and mobile devices will account for two thirds of total IP communications by 2020 [1]. This trend will result in an increment of the number of connected wireless devices and wireless data rates, which have doubled every 18 months over the last three decades [2].

Envelope detectors (EDs) are used in ultra-wideband (UWB) wireless receivers for demodulating amplitude shift keying (ASK) signals without the need of a local oscillator (LO). EDs allow a reduction of the cost and complexity of the receiver for a penalty in terms of sensitivity [3]. They can be designed using either single-ended or balanced architecture. Single-ended EDs are limited to a maximum bitrate up to half of the carrier frequency, f_c in the best case scenario. This effect is due to the presence of a fundamental harmonic spurious at their output [3]. In practice, this value is smaller as shown in table I, where *Δb* is the bitrate normalized to the carrier frequency f_c [4].

TABLE I
State of the Art (SoTA)

Ref	f_c (GHz)	Bitrate (Gbps)	*Δb* (%)	Technology	Architecture
[5]	4-8	4	50-100	Schottky diode	Balanced
[4]	7	2.5	35.71	Schottky diode	S. ended
[6]	7	2.5	35.71	Schottky diode	S. ended
[7]	101	26	25.74	35 nm mHEMT	Balanced
[8]	108	24	22.22	50 nm mHEMT	n/a
[9]	93	20	21.51	n/a	n/a
[10]	120	10	8.33	100 nm InP HEMT	n/a
[11]	300	24	8	250 nm InP HBT	S. ended
This work	8	2.5	31.25	Schottky diode	Balanced

Balanced ED configuration is an alternative, which improves the fractional bandwidth limitation at a cost in complexity. They require a balun to convert the single-ended input signal into a differential signal and two diodes instead of the one used in single ended ED. Baluns face the challenge of achieving a broad phase balance bandwidth to allow the cancellation of the fundamental harmonic spurious generated by the Schottky diode, and hence improve *Δb*.

Moreover, a balanced configuration reduces the common mode noise at the output [3]. The drawbacks of balance detectors is the enlargement of the circuit size, due to the balun and the extra diode, and uncertainties due to the possibility of a behavior mismatch of the two diodes. Current electronic circuits have size constraints, since the devices where they are used pursue down-sizing.

This work presents a novel Schottky diode ED architecture to tackle the size disadvantage of balanced detectors, while at the same time keeping a high *Δb*. Fig. 1 shows its general architecture, which is divided in two sections: the balanced detector, that downconverts the signal; and the bias tee together with a low-pass filter (LPF). This letter focuses on the detector section.

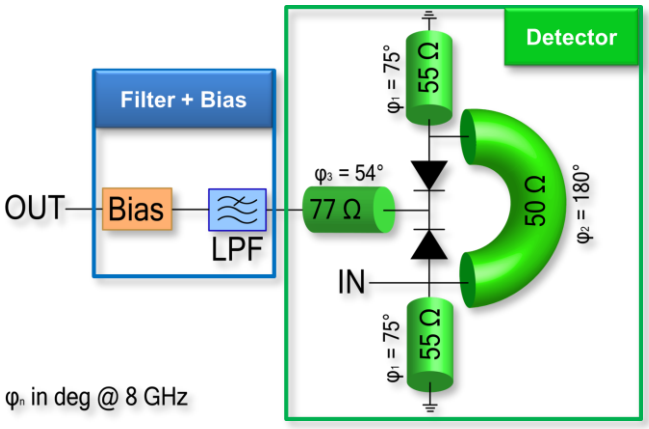


Fig. 1. Schematic of the proposed detector circuit.

The target of this ED is to demodulate an ultra-wideband 2.5 Gbps ASK signal with an f_c of 8 GHz with the same performance as previous architectures while shrinking down the circuit size. The proposed detector can be integrated in C- and X-band systems for standardized applications such as WiMAX (802.16), Wi-Fi (802.11a), satellite and radar communications, among others with bitrates above 1 Gbps. In addition, we believe that this architecture can be a key component in the future of 5G networks [12].

The proposed envelope detector is designed in microstrip technology with surface mounting devices (SMD) on a 32 mil RO4003 substrate with a 35µm top copper layer.

II. Circuit Design

Fig. 2. shows the schematic comparison between this work and the two baluns which inspired its design: a conventional rat race (Fig. 2. a) [3], [13] and the rat race which uses the high-pass compensation principle (Fig. 2. b) which consists in the substitution of the 3λ/4 transmission line from the traditional rat-race hybrid coupler by its equivalent L-C circuit. The inductors from the L-C circuit are replaced by shorted-stubs., presented in [14]. The first two circuits are rat race couplers with 4 ports: one input (port 4) and two outputs (ports 2 and 3), while the isolated port (port 1) is connected to a load.

The detector architecture proposed in this letter is composed of two Schottky diodes, two shorted-stubs and a transmission line with an electrical length of 180º at f_c= 8 GHz. It has 2 ports only: one input (port 4) which additionally has the same function as port 3 in the two other circuits, and one output. In this work, the impedance of the λ/6 transmissions lines is 50 Ω instead of 70 Ω for a standard balun to avoid an abrupt transition from the 50 Ω input transmission line where the connector is soldered. The shorted-stubs connected to ports 2 and 4 are identical to preserve the symmetry. The output delivers the demodulated signal directly, while the other two circuits need an additional balanced detector at their outputs to demodulate the signal.

The output signal is the rectified AM signal with the absence of the canceled component of the fundamental harmonic due to the balanced architecture.

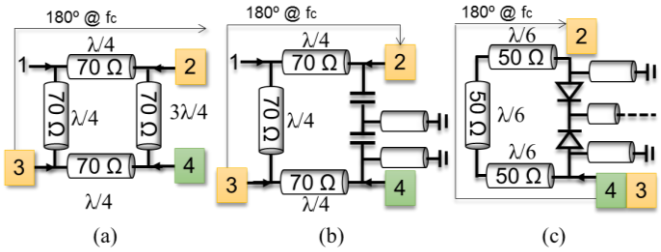


Fig. 2. Schematic of conventional rat race [3] (left); rat race with high-pass compensation [14] (middle); and this work (right).

The detector offers two key features which make it unique. First, it rectifies the input signal, while simultaneously works as a rat-race hybrid coupler inspired balun without an isolation port, since only the differential outputs are necessary in this setup. Second, the size of the balun can be shrunk using the high-pass compensation principle [14], The capacitance needed for the target operation frequency (8 GHz) is in the order of 0.1 pF. These low values can be achieved using the parasitic capacitance of the Schottky diode.

Skyworks SMS7621 diodes are chosen in this work with the features showed in table II:

TABLE II
SKYWORKS SMS7621

Is (A)	Rs (Ω)	Cj0 (pF)	Lp (nH)	Cp (pF)	Vj (V)
$4 \cdot 10^{-8}$	12	0.1	0.7	0.15	0.51

III. Simulation Approach

The detector was designed with Keysight's Advance Design System (ADS). Using the harmonic balance analysis, the frequency response of the circuit could be simulated. The purpose was measuring the output power when the system is excited with a low frequency tone (100 MHz) modulated with a high frequency carrier. The frequency response of the system allows calculating the operational bandwidth and the distortion introduced by the system. In an UWB detector, a high conversion gain is useless if the frequency response is not flat, since some frequency components of the input signal will be amplified with respect to others, deteriorating the quality of the detected signal.

Fig. 3. compares the performance in terms of phase balance bandwidth of the novel architecture introduced in this letter with a conventional manufactured rat-race hybrid coupler which uses the same microstrip technology. In both devices it is measured through an harmonic balanced simulation by comparing the phase at the input of each diode. The rat race and the architecture presented in this paper offer a phase balance bandwidth (+- 6º) of 1.52 GHz and 1.45 GHz respectively.

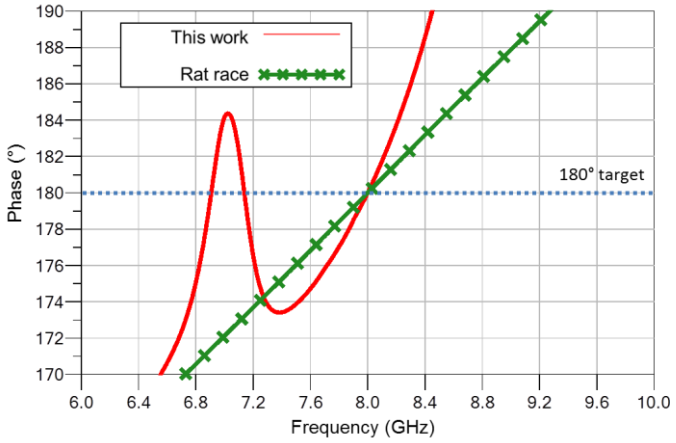


Fig. 3. Comparison of phase balance bandwidth between a rat race (green, cross) and this work (red).

The low-pass filter (LPF) is placed at the output of the detector. It is in charge of rejecting the spurious signal resulting from the second harmonic of the diodes and the portion of the first harmonic that was not cancelled by the balanced configuration. The filter is a 6th order Butterworth filter, implemented using the stepped impedance approach [3]. The cut-off frequency is 3.2 GHz, since the S_{21} of this filter has a minimum close to 8 GHz. Fig. 4. shows the S-parameters of the filter calculated by the Momentum simulation of ADS.

The bias network is implemented with SMD components. It selects the optimum point of rectification for the diodes.

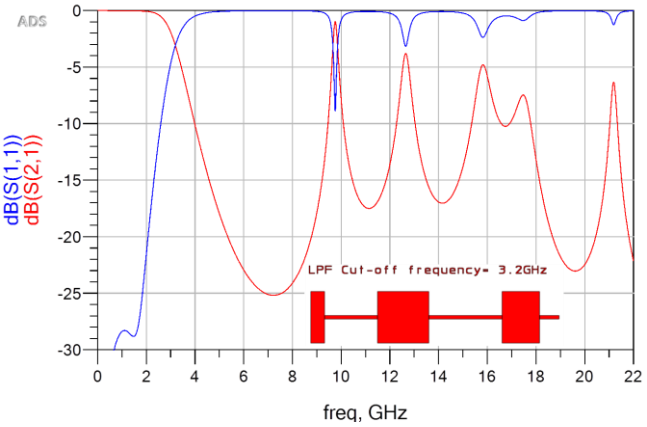


Fig. 4. S-Parameters of the low pass filter (LPF).

The simulations showed that combined with the LPF, the circuit rejects the harmonics spurious from a 2.5 Gbps ASK signals and 8 GHz carrier. The phase balance bandwidth can be improved by introducing an input matching network that adapts the impedances of the diodes along the target frequency range.

The transient analysis was used to test the demodulation performance of the circuit. Eye diagrams provided a qualitative indicator of the integrity of the signal. Simulation results confirm the capability of the detector to demodulate an ASK signal at 2.5 Gbps modulated with an 8 GHz carrier frequency.

IV. Measurements

The experiments described in this section demonstrates the functionality of the compact envelope detector by demodulating an ASK signal in real time. Fig. 5. shows the manufactured detector and Fig. 6. shows the experimental set up used during the experiment.

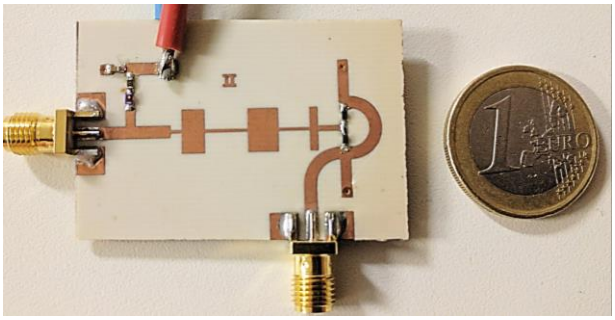


Fig. 5. Manufactured detector.

A pulse pattern generator (PPG, Anritsu MP1763B) generates a 2^{31}-1 PRBS signal NRZ coded with 0.5 Vpp and a DC offset of 0.4 V. After low-pass filtering the PRBS signal, it is mixed with a local oscillator (Rohde & Schwarz SMR 40) which sets the carrier frequency of the ASK modulated signal obtained at the output of the mixer (Avantek TFX-184L). The error detector (Anritsu MP1764C) measures the bit error rate ratio (BER) of the signal demodulated by the detector.

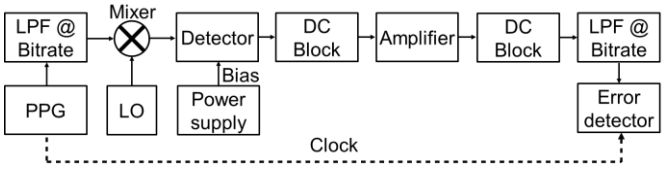


Fig. 6. Set-up used for measuring the bit error ratio, BER.

The carrier frequency of the ASK signal was swept from 7 to 9 GHz and its power from -17 to -3 dBm in steps of 1 GHz and 1 dB respectively. The bitrate of the ASK signal was set to 2.5 Gbps. The curves were not measured below -17 dBm because the input power to the error detector was below its detection threshold, not being able to measure the BER correctly.

Fig. 7. illustrates the -Log(BER) versus the ASK input power to the detector at three carrier frequencies: 7, 8 and 9 GHz.

As predicted, the best performance is achieved with an 8 GHz carrier frequency, leading to a sensitivity of -12 dBm and a Δb of 31.75 %. This value of Δb is close to the highest one found in the SoTA. Introducing forward error correction (FEC) coding [15] allows boosting the sensitivity to -20 dBm.

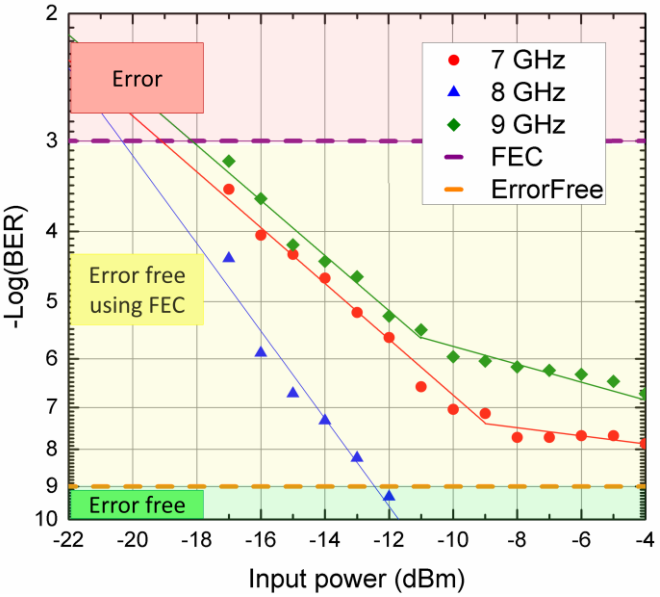
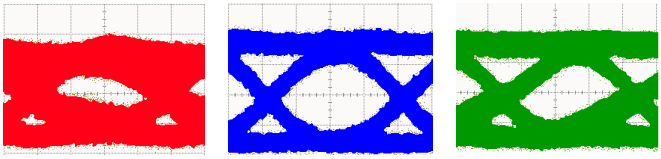


Fig. 7. BER curves versus input power at 2.5 Gbps.

Error free demodulation was not achieved at the other two carrier frequencies because of the phase balance bandwidth of the balun is 1.5 GHz centered at 8 GHz. When the carrier and the main lobe of the AM signal is outside the cancellation region, the resulting demodulated signal has a strong fundamental harmonic which cannot be successfully rejected by the LPF alone, leading to frequency components that distorts the eye diagram of the demodulated signal as shown in Fig. 8.



(a) f_c = 7 GHz. (b) f_c = 8 GHz. (c) f_c = 9 GHz.

Fig. 8. Measured eye diagrams at 2.5 Gbps. The input power is -6 dBm. 20 mV/div; 100 ps/div.

The phase balance frequency region of the balun can be shifted by tuning the shorted-stubs attending to specifications of the target application.

Finally, table III shows the reduction in terms of size of the architecture presented in this work in comparison to a single balanced detector, which uses a Rat Race as balun and was simulated in ADS Momentum in order to make an accurate size comparison when both architectures use the same diodes and substrate. According to the simulations, both present a similar performance in terms on demodulation, while the ED presented on this letter only needs one fifth of the area.

TABLE III

Size comparison of single balanced detectors (balun & detector, without filter or bias tee)

	Height (mm)	Width (mm)	Area (mm^2)	% Size
Rat race & balanced detector	29.1	21.6	628.5	100
This work	20.4	6.1	124.4	**19.8**

V. Conclusion

This letter presents a novel compact balanced envelope detector (ED) architecture. The ED is able to demodulate a single-ended signal by using the advantages of balanced detection without the aid of an external balun. It offers the same performance as balanced ED's using a Rat Race balun which uses the same planar technology, while providing a 5X shrink down factor.

A prototype was designed, fabricated and tested in the laboratory under real conditions, proving the real-time demodulation of ASK signals with bitrate up to 2.5 Gbps modulated with an 8 GHz carrier. The results lead to a bitrate to carrier frequency ratio of 31.25 %. These results show the ability of this ED to work within 5G networks. Moreover, the f_c can be easily scaled to fulfill further specifications.

Acknowledgment

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