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A Hybrid Compensation Scheme for the Gate Drive Delay in CLLC Converters

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Abstract—The CLLC converter is often used as an isolated linker between high and low voltage buses where the CLLC converter operates under the open-loop condition at resonant frequency. In such applications, CLLC converters are able to achieve high efficiency usually due to superior performance of soft switching. However, we found that the operating process of a CLLC converter under open-loop control at the resonant frequency will significantly change by the non-ideal parameters of the semiconductor switches and gate driver circuits. These impacts on the converter operation were investigated and defined as the gate drive delay. We present a comprehensive steady-state analysis for the CLLC converter that considers the gate drive delay including its operating process, mathematical model, power loss, and voltage ripple. In some cases, the gate drive delay changes the operating process of the CLLC converter. As a result, the soft switching condition changes or even loses, large circulating current exists on the secondary side, output voltage ripples become larger and so that the efficiency decreases dramatically. Therefore, a hybrid compensation scheme, consisting of an offline design procedure and an online close-loop control algorithm, is proposed to minimize resonant frequency variation due to the gate drive delay. Both the correctness of the steady-state analysis and effectiveness of the proposed hybrid compensation scheme are verified by experiment. Using the proposed compensation scheme can reduce the output voltage ripple to 1/3 of the original value and increase the efficiency of more than 10% within the whole load range.

Keywords—CLLC converter; Gate drive delay; Hybrid compensation scheme

I. INTRODUCTION

CLLC converters, as the high-efficiency high-power-density isolated bidirectional topology, have gained the attention of researchers and engineers in recent years and been widely used in uninterrupted power supply systems, dc distribution systems, vehicle-to-grid systems, more electric aircraft and reversible solid oxide fuel cell systems [1]-[8]. CLLC converters are regarded as a promising topology to bidirectional power transmission due to their excellent soft-switching characteristics [1], [2].

Traditionally, the CLLC topology is used to build general isolated bidirectional dc-dc converters (IBDC), providing both high efficiency isolated power transmission and voltage regulation. Researches in this area have mainly concentrated on parameter design, control strategy, transformer design, and topology improvement. Design considerations for the resonant tank have been discussed in [2]. Some researchers proposed a detailed 2-step procedure to design a CLLC resonant tank from a pre-designed CL LLC resonant tank [3]. A PWM control strategy was proposed to obtain a high voltage gain [9]. The phase shift control was used and analyzed for CLLC converters [10]. Control strategies combining frequency modulation and phase-shifting control were proposed to improve dynamic performance and reduce reactive power [11], [12]. A sliding mode control loop design for CLLC converters that can improve converter dynamics and achieve tight output voltage regulation was proposed [13]. Synchronous rectification methods were proposed to increase power conversion efficiency [14]-[16]. The optimal design of the conventional litz-wired transformer, planar transformer, and medium-voltage-level transformer for CLLC converters were discussed in [17]-[19]. In [20], the cancellation concept was adopted in the winding design of the planner transformer to reduce the common mode noise caused by the inter-winding capacitance. Moreover, the improved CLLC topologies to reduce the voltage ripple, narrow the frequency range, and increase efficiency were proposed in [21]-[24].

Instead of using a CLLC converter as a general IBDC, another research and application trend is to use a CLLC converter as an isolated high efficiency linker between high and low voltage dc buses, where the voltage regulation is not needed and the converter runs under open-loop control at the resonant frequency. The CLLC converter was integrated into an isolated bidirectional ac-dc converter to improve the efficiency of a dc distribution system [25]. Using a CLLC converter as a bidirectional resonant dc transformer for a hybrid ac/dc microgrid was also proposed [7]. The CLLC converter can replace the conventional bulky transformer for bus voltage matching and galvanic isolation, reducing the weight and space needed. A new multi-port bidirectional topology was proposed for the reversible solid oxide fuel cell system [8]. A multi-port CLLC converter with a shared high frequency ac bus was used to provide a fixed step-down ratio. A novel 2-stage topology for a 6.6-kW on-board charger was proposed, where the CLLC converter served as the dc/dc stage [26], [27]. This proposed topology has a 37-W/in³ power density and above 96% efficiency over the entire voltage range. Several parameter design methods were proposed for the CLLC-Type dc transformer to prevent the dispersion of resonant parameters, select the suitable switching frequency, and minimize the power loss [28]-[30].

Basically, researchers agree that a CLLC converter can achieve high efficiency naturally if it operates under the resonant frequency because of its superior performance of soft switching. However, in the above-mentioned applications, the operating process of the converter will be influenced by the non-ideal parameters of the semiconductor switches and gate
driver circuits, so that its performance suffers.

For the analysis of the CLLC converter operation, the switches used are normally assumed as ideal [1], [2]. “Ideal switches” mean that once the rising or falling edge of the PWM signals from the controller are sent, the switches can turn on or turn off instantly. For a CLLC converter under open-loop control, it means the primary and secondary switches turn on and turn off at the same time. However, in an actual prototype, propagation delays commonly exist in the driver circuit. In addition, parasitic parameters and the inherent characteristics of the semiconductor switches also influence the specific moment when switches turn on or turn off. Moreover, in practical applications, a CLLC converter is usually designed to have a high step up/down ratio. As a result, the selection of the switches and driver circuit designs for the primary and secondary sides are different, which may result in different turn-on or turn-off moments on the primary and secondary sides, even if the PWM signals are the same. Therefore, the influence of different turn-on/turn-off moments between the primary and secondary sides must be taken into account, but the related research on this topic is very limited.

In this paper, the influences of the non-ideal factors of switches and gate driver circuits are evaluated and defined as the gate drive delay. A comprehensive steady-state analysis for a CLLC converter considering gate drive delay is presented, including the operating process, mathematical model, power loss, and voltage ripple. A hybrid compensation scheme, consisting of an offline design procedure and an online close-loop control algorithm, is also proposed to minimize the negative influences of the gate drive delay. The correctness of the steady-state analysis and effectiveness of the proposed hybrid compensation scheme were verified by experiments.

This paper is organized as follows. After this introduction, in Section II, a strict definition of the gate drive delay is given and an equivalent description is proposed to simplify the following analysis. In Section III, a comprehensive steady-state analysis is proposed. The influences of the different types of gate drive delays are clarified and modeled mathematically. In Section IV, a hybrid compensation scheme is proposed and analyzed. In Section V, the experimental results are provided to verify the proposed analysis and compensation scheme. Finally, the conclusion is given in Section VI.

II. GATE DRIVE DELAY AND ITS EQUIVALENT DESCRIPTION

A. Actual turn-on and turn-off moments of switches considering non-ideal factors

Non-ideal factors in this paper mainly refer to the following.

1) Propagation delays of the driver circuit,
2) Gate resistance,
3) Input capacitance of the switches, and
4) Turn-on and turn-off delay times of the switches.

The digital isolators and driver ICs are the major source of propagation so that they determine the total propagation delay of the driver circuit. The overall effects due to the propagation delay from the digital isolator and driver integrated circuit (IC) can be summed up and modeled as the driver delay time \( t_{d,\text{driver}} \). Therefore, the gate-source voltage \( V_{gs} \) will lag behind the PWM signal by \( t_{d,\text{driver}} \) shown in Fig. 1.

![Fig. 1. Waveforms of the gate-source voltage considering the propagation delay.](image1)

The digital isolators and driver ICs are the major source of the driver circuit delay. A comprehensive analysis including the operating process, mathematical model, power loss, and voltage ripple. A hybrid compensation scheme, consisting of an offline design procedure and an online close-loop control algorithm, is also proposed to minimize the negative influences of the gate drive delay. The correctness of the steady-state analysis and effectiveness of the proposed hybrid compensation scheme were verified by experiments.

Actually, \( V_{gs} \) will not change to a high level immediately because of the existence of the input capacitance. The waveform of \( V_{gs} \) during the switching transient is a RC charging or discharging waveform determined by the time constant \( \tau = R_g C_{gs} \), where \( R_g \) and \( C_{gs} \) represent the gate resistance and input capacitance, respectively, as illustrated in Fig. 2(a). In practice, the effects of the driver delay and input capacitors are combined. As a result, the actual \( V_{gs} \) waveform is shown in Fig. 2(b).

The turn-on and turn-off transient process of power devices (such as power MOSFETs) is mainly determined by the gate threshold voltage \( V_{gs,\text{th}} \), turn-on delay time \( t_{d,\text{on}} \), rising time \( t_r \), turn-off delay time \( t_{d,\text{off}} \), and falling time \( t_f \). For simplicity, we describe the turn-on and turn-off transient process as follows: when \( V_{gs} \) increases to \( V_{gs,\text{th}} \), after \( t_{d,\text{on,all}} = t_{d,\text{on}} + t_r \), the power device turns on; when \( V_{gs} \) decreases to \( V_{gs,\text{th}} \), after \( t_{d,\text{off,all}} = t_{d,\text{off}} + t_f \), the power device turns off.

The time intervals that \( V_{gs} \) increases from 0 to \( V_{gs,\text{th}} \) and decreases from high level to \( V_{gs,\text{th}} \) are \( t_{\text{inc}} \) and \( t_{\text{dec}} \), respectively. Taking the rising moment of the PWM signal as \( t = 0 \), the turn-on moment can be calculated as:

\[
t_{\text{on}} = t_{d,\text{driver}} + t_{\text{inc}} + t_{d,\text{on,all}}.
\]

Similarly, the turn-off moment is

\[
t_{\text{off}} = t_{d,\text{driver}} + t_{\text{dec}} + t_{d,\text{off,all}}.
\]

The gray shadow in Fig. 3 shows the actual on-state interval of the switches. \( D_{\text{on}} \) is on-state duty cycle, and it can be calculated as:

\[
D_{\text{on}} = D + \frac{t_{\text{off}} - t_{\text{on}}}{T},
\]

where \( D \) and \( T \) are the duty cycle and switching period of the PWM signal, respectively.
B. Definition of the gate drive delay and proposed equivalent description

The gate drive delay in this paper is used to describe the on-state difference of the switches between the primary and secondary sides. The gate drive delay is related to three parameters:

1) $D_1$, the duty cycle of the primary side switches;
2) $D_2$, the duty cycle of the secondary side switches; and
3) $\theta$, the turn-on moment difference between the primary and secondary switches.

$\theta$ is positive when the turn-on moment of the primary side is earlier and vice versa. $\theta$ can be expressed as

$$\theta = \frac{t_{on,secondary} - t_{on,primary}}{T},$$

(4)

where $t_{on,secondary}$ and $t_{on,primary}$ are turn-on moments of primary and secondary side respectively.

In [1], [2], the non-ideal factors were ignored, so that

$$\theta = 0, D_1 = D_2.$$  (5)

If the non-ideal factors of the primary and secondary side circuits are designed to match and (5) is satisfied, the previous analysis given in [1], [2] can also be applied to CLLC converters. However, in many cases, the non-ideal factors do not match well; therefore (5) cannot hold anymore.

The definition of a gate drive delay effect is as follows: A gate drive delay effect occurs in a circuit if (5) is not satisfied.

According to the potential values of $\theta$, $D_1$, and $D_2$, there are 4 types of gate drive delays, which are denoted as Type A, Type B, Type C, and Type D, and illustrated in Fig. 4. $S_{primary}$ and $S_{secondary}$ are equivalent PWM signals of primary and secondary side.

![Fig. 4. Four types of gate drive delays and their equivalent descriptions.](image)

To simplify the analysis, an equivalent description method for the gate drive delay is proposed as follows. $\theta$, $D_1$, and $D_2$ are determined by non-ideal factors; they are uncertain, but they are constant once a prototype is built. As a result, we can still adopt the idea of “ideal switches,” but make some changes to the PWM signal, which can also guarantee an exact description of the actual working condition of the converter. Take Type A as an example: if we assume the switches are ideal, then the duty cycle of the primary and secondary PWM signal $S_{primary}$ and $S_{secondary}$ should be changes to $D_1$ and $D_2$, respectively, and $S_{primary}$ should lead to $S_{secondary}$ by $\theta$.

Other types of gate drive delays are similar to Type A. Furthermore, for the PWM signals $S_{primary}$ and $S_{secondary}$, there are four basic cases, which are illustrated in Fig. 5. Case 1 and Case 2 are related to the rising edge of the PWM signals. In Case 1, the rising edge of $S_{primary}$ lags that of $S_{secondary}$. In Case 2, the rising edge of of $S_{primary}$ leads that of $S_{secondary}$. On the other hand, Case 3 and Case 4 are related to the falling edge of the PWM signal. In Case 3, the falling edge of $S_{primary}$ lags that of $S_{secondary}$. In Case 4, the falling edge of $S_{primary}$ leads that of $S_{secondary}$.

Therefore, we can find the relationship between Types A to D and Cases 1 to 4, accordingly:

1) Type A consists of Case 2 and Case 3,
2) Type B consists of Case 1 and Case 3,
3) Type C consists of Case 2 and Case 4, and
4) Type D consists of Case 1 and Case 4.

So far, we have established an equivalent description method based on the “ideal switches” for the gate drive delay and decomposed the different types of gate drive delay into four basic cases, which form the basis of the following steady-state analysis.

III. STEADY-STATE ANALYSIS FOR THE CLLC CONVERTER CONSIDERING THE GATE DRIVE DELAY

A. Pre-descriptions and assumptions for steady-state analysis

Fig. 6 shows the topology of the CLLC converter. $S_1$ to $S_4$ are the primary side switches and $S_5$ to $S_8$ are the secondary side switches. The positive directions of the voltage and current used in the steady-state analysis are also given and the transformer turns ratio is $n$ and $n > 1$.

![Fig. 6. Topology of the CLLC converter.](image)

In this section, the discussion of the steady-state analysis mainly focuses on the proposed four basic cases since the gate drive delay is just a combination of those cases. For ease of exposition, we define the condition without the gate drive delay as the “Normal Case”. Its PWM signal is illustrated in Fig. 7, and the corresponding steady-state waveforms are illustrated in Fig. 9(a).
The following assumptions were made for the steady-state analysis:

1) All switches are “ideal switches.”

2) The range of $u_{cr2}$ can be omitted compared to $u_{cd}$, so that $u_{lm}$ is nearly clamped by $u_{cd}$ and $i_{lm}$ is a triangular wave current, where $u_{cr2}$ and $u_{lm}$ are the voltage across $C_{r2}$ and $L_m$ respectively.

3) The converter is operating at the resonant frequency.

Note that the assumption that all switches are “ideal switches” is not contradictory with the gate drive delay because the influence of non-ideal factors has already been integrated into the four basic cases.

**Fig. 7. PWM signals of the Normal Case.**

**Fig. 8. Equivalent circuits for (a) Normal Case, Case 1, Case 2, and Case 3**

**B. Operating process of the CLLC converter under the four basic cases**

We only explain the half cycle with positive $u_{cd}$, since the other half cycle is symmetrical. The equivalent circuit for the Normal Case is shown in Fig. 8(a). The operating process under the Normal Case was analyzed in detail in the literature [1], [2]. Here, we mainly focus on Cases 1 to 4.

As illustrated in Fig. 9 (a), for Case 1, the rising edges of the PWM signals of the primary side lag behind those of the secondary side by $\Delta t_1$. If we suppose the steady-state waveforms are the same as those of the Normal Case during $\Delta t_1$, then the primary-side current will be negative, so the body diodes of $S_1$ and $S_4$ will conduct and $u_{ab}$ will be positive. However, $u_{cd}$ will also be positive since the secondary-side PWM signals are the same as those in the Normal Case. As a result, the equivalent circuit in Case 1 remains unchanged. Consequently, the steady-state waveforms remain unchanged, too.

For Case 2, the PWM signals of the primary side are the same as those of the Normal Case but lead those of the secondary side by $\Delta t_2$. Similarly, if we suppose the steady-state waveforms remain unchanged, then the body diodes of $S_2$ and $S_3$ will conduct and $u_{cd}$ will be positive during $\Delta t_2$. As a result, the equivalent circuit in Case 2 is the same as that in the Normal Case, and the steady-state waveforms remain unchanged.

For Case 3, by adopting the same analysis method as above, we can know that the steady-state waveforms remain unchanged, too.

Fig. 9 (a) shows that the falling edges of the PWM signals of the primary side lead those of the secondary side by $\Delta t_3$ in Case 4. Assuming the steady-state waveforms remain unchanged...
During $\Delta t_4$, the voltage excitation of the resonant tank changes from $U_{in} - U_{out}$ to $-U_{in} - U_{out}$. As a result, the operating process of the Normal Case no longer holds in Case 4. Since $u_{AB}$ is negative while $u_{CD}$ is positive, the primary side current $i_p$ would decrease rapidly. $u_{lm}$ is clamped by $u_{CD}$, which remains unchanged so that $i_{lm}$ continues to increase. The steady-state waveforms of Case 4 are illustrated in Fig. 9 (b), and they consist of four stages.

Stage 1 $[t_0 \to t_1]$: Both H-bridges of the primary and secondary sides are in dead time, so the body diodes of $S_1, S_3, S_5$, and $S_B$ conduct, and the voltages across these switches are 0.

Stage 2 $[t_1 \to t_2]$: At the time $t_1, S_1, S_3, S_5$, and $S_B$ turn on under zero voltage switching (ZVS). From $t_1$ to $t_2$, $u_{AB}$ equals to $U_{in}$, and $u_{CD}$ equals to $U_{out}$. The operating process of the converter is similar to that of the Normal Case. The condition of $i_p > i_{lm}$ is satisfied, the polarity of secondary-side current $i_s$ is negative, and the power transfers from the primary side to the secondary side.

Stage 3 $[t_2 \to t_3]$: At the time $t_2, S_1$ and $S_5$ turn off, and $u_{AB}$ changes to $-U_{in}$. $i_p$ decreases rapidly while $i_{lm}$ increases. Since $i_s$ is still larger than $i_{lm}$, the secondary-side current $i_s$ is positive, and the power transfers from the primary side to the secondary side.

Stage 4 $[t_3 \to t_4]$: At the time $t_3$, $i_p$ equals to $i_{lm}$. The trends of $i_p$ and $i_{lm}$ are the same as those of Stage 2. During the time period of $\Delta t' = t_4 - t_3$, $i_{tr}$ is smaller than $i_{lm}$, so $i_s$ is positive. The power transfers from the secondary side to the primary side.

Two things are worth noting: one is that $\Delta t'$ is not always shorter than $\Delta t_4$, since it is possible that $i_{tr}$ decreases to $i_{lm}$ first, and $u_{AB}$ changes to $-U_{in}$ later. Whether $\Delta t'$ is smaller than $\Delta t_4$ or not depends on the value of $\Delta t_4$; the other is that, if $\Delta t_4$ is so long that the value of $i_p$ is too close to 0 or the polarity of $i_p$ changes at $t_4$, the output capacitors of the primary switches may not be fully charged. As a result, the primary switches may operate under the hard switching condition.

In summary, the main features of steady-state waveforms for Case 4 are the following.

1) The primary switches operate under ZVS or hard switching, depending on the length of $\Delta t_4$.

2) The secondary switches operate under the ZVS condition instead of the ZCS (zero current switching) condition.

3) The secondary current $i_s$ has a large circulating component.

C. Mathematical models of the four basic cases

In order to give a more comprehensive analysis of the gate drive delay, mathematical models for the proposed basic cases are needed. There are three quantitative analysis methods for the CLLC topology. First is the harmonic approximation (HFA) method [2], [14], which is the most widely used. The extended harmonic approximation (EHA) method [15] is an improved version of the HFA. However, both the HFA and EHA methods are in frequency domain. They are convenient for analyzing the gain characteristics, but are imprecise for the analysis of steady-state waveforms. An analysis method in time domain was proposed in [31], which is useful for the analysis of steady-state waveforms. This method is employed and further developed in this paper to analyze Cases 1 to 4.

We define the base value for the voltage, current, and impedance as follows:

$$x_{base} = \frac{L_{r1}}{\sqrt{C_{r1}}} = \frac{L_{r2}}{\sqrt{C_{r2}}} = \frac{U_{out}}{i_{base}} = \frac{u_{base}}{x_{base}}.$$  \hspace{1cm} (7)

The CLLC converter resonant tank is actually a 4th-order circuit. By solving its state equations, we can obtain the time domain expressions in per-unit form of the selected state variables ($i_{LM}, i_s, u_{cr1}, u_{cr2}$) for the Normal Case, as (6) shows.

Neglecting the switch and loss, $P_1, P_2, P_3, P_4$ and $M$ are undetermined coefficients, so they can be solved with the known boundary conditions and they have concise analytical expressions. The boundary conditions and expressions of $P_1, P_2, P_3, P_4,$ and $M$ are shown in (8). In (8), the items in the left bracket are the boundary conditions and the items in the right bracket are the expressions of $P_1, P_2, P_3, P_4,$ and $M$.

\[
\begin{align*}
  i_{tr}(0) &= -i_{tr}(\pi) \\
  i_s(0) &= -i_s(\pi) = 0 \\
  u_{cr1}(0) &= -u_{cr1}(\pi) \\
  u_{cr2}(0) &= -u_{cr2}(\pi) \\
  \frac{1}{\pi} & \int_0^\pi i_s(\theta) d\theta = I_o \\
  P_1 &= P_3 = -k_1 \tan \left( \frac{k_1}{2} \right) \\
  P_2 &= -\frac{\pi}{2} I_o \\
  P_3 &= 1 \\
  M &= M = 1
\end{align*}
\]

where $I_o$ is the output current.

To simplify the quantitative analysis, we suppose that Case 4 has the same operating process as that of the Normal Case but $i_s(0)$ changes, although actually, Case 4 has a different operating process during $\Delta t_4$, as noted before. Therefore, the form of the time domain expressions for Case 4 is the same as that shown in (6), but the boundary conditions change. The boundary conditions and expressions of $P_1, P_2, P_3, P_4,$ and $M$
for Case 4 are shown in (9). In (9), the items in the left bracket are the boundary conditions and the items in the right bracket are the expressions of $P_1$, $P_2$, $P_3$, $P_4$, and $M$.

We define (6) and (8) as Model I and (6) and (9) as Model II. Since the operating processes of Case 1, Case 2, and Case 3 are the same as that of the Normal Case, Model I is applicable to Cases 1-3. Model II is applicable to Case 4.

$$
\begin{align*}
    i_s(0) &= i_{s0}, \\
    u_{c1}(0) &= -u_{c2}(0), \\
    \frac{1}{\pi} \int_0^\pi i_s(\theta) d\theta &= I_o \\
    P_1 &= -k_1 \tan \left( \frac{k_1}{2\pi} \right) - i_{s0}, \\
    P_3 &= -k_1 \tan \left( \frac{k_1}{2\pi} \right), \quad (9)
\end{align*}
$$

where $i_{s0}$ is the initial value of the secondary current.

D. Power loss analysis

For Cases 1, 2, and 3, since the soft-switching features of switches remain unchanged. Additional losses come from the increase of the freewheeling time of the body diodes, which can be calculated as:

$$
\begin{align*}
    P_{loss, Case 1} &= f_s \int_{t_{case 1}}^{t_{case 1} + \Delta t_1} (V_{D,p} i_{on,p}^2 + R_{on,p} i_{on,p}^2) dt \\
    P_{loss, Case 2} &= f_s \int_{t_{case 2}}^{t_{case 2} + \Delta t_2} (V_{D,s} i_s - R_{on,s} i_s^2) dt, \quad (10) \\
    P_{loss, Case 3} &= f_s \int_{t_{case 3}}^{t_{case 3} + \Delta t_3} (V_{D,s} i_s - R_{on,s} i_s^2) dt
\end{align*}
$$

where $V_{D,p}$ and $V_{D,s}$ are the forward voltages of the primary and secondary switches, respectively, $R_{on,p}$ and $R_{on,s}$ are the on-state resistances, and $t_{case 1}$, $t_{case 2}$, and $t_{case 3}$ are the start times of Case 1, Case 2, and Case 3, respectively.

Equation (10) shows that the additional power loss in Cases 1 to 3 mainly depends on the forward voltage ($V_{D,p}$ and $V_{D,s}$), freewheeling time ($\Delta t_1$, $\Delta t_2$, and $\Delta t_3$), and average value of the freewheeling current.

Normally, the forward voltages of body diodes for different switches are very similar. For example, for the MOSFET, this value ranges from 0.5 V to 0.8 V. However, the turns ratio of the transformer in the CLLC resonant tank is often designed to be larger than 1 (usually 1 to 10 or even more) to meet the requirements of connecting high and low voltage dc buses. As a result, the secondary current may be times larger than the primary current. So that for a given freewheeling time, the additional power loss of Case 1 is the smallest. However, because the forward voltage is small and the freewheeling time is short, efficiency decrease is slight in Case 1, Case 2, and Case 3.

Gate drive loss can be calculated by (11).

$$
P_{loss\_gate} = 4f_s (C_{iss,p} V_{g,p}^2 + C_{iss,s} V_{g,s}^2), \quad (11)
$$

The gate drive loss does vary if switches change. For power switches, $V_{gs}$ is usually varies form 10-20V, $C_{iss}$ is pF to nF level, and the switching frequency is below 1MHz. The difference of the gate drive loss of different switches is small and doesn’t have significant influence on the converter efficiency.

For Case 4, turn-off loss will be larger. There are two stages during the turn off transient as illustrated in Fig. 10. The drain-source voltage raises from zero to $V_{DS}$ firstly. Then the drain current falls from $I_p$ to zero. $I_p$ means the switch current when switches begin to turn-off. $t_{ru}$ means the voltage raising time and $t_f$ means the current falling time.

$$
\begin{align*}
t_f &= \text{the Miller effect and its calculation is complex. However, }t_{ru}\text{ and }t_f\text{ are of the same order of magnitude. For simplicity, we assume }t_{ru} = 2t_f\text{ and the current and voltage during }t_{ru}\text{ and }t_f\text{ changes linearly. Therefore, the total turn-off loss can be calculated as:}
\end{align*}
$$

$$
P_{loss} = 6f_s (t_{rp} V_{DS,p} I_{DP} + t_{fs} V_{DS,s} I_{DP}), \quad (12)
$$

In Case 4, $I_{DP}$ will decrease and $I_{DS}$ will increase. $V_{DS,p}$ is about n times larger than $V_{DS,s}$ and $I_{DP}$ is about n times larger than $I_{DS}$. Seemly $P_{loss\_off}$ will basically remain unchanged. However, secondary switches are high current devices so $t_{fs}$ will be much larger than $t_{rp}$. As a result, the turn-off loss of Case 4 is larger that of Normal Case and Case 1 to Case 3.

Additionally, $i_s$ during $\Delta t'$ is a circulating current, which causes larger conduction loss. Furthermore, if $\Delta t'$ is too long, primary switches may work under the hard switching condition, causing a large amount of switching loss. With the significant increase of the conduction losses and switching losses, the efficiency of Case 4 would decrease sharply.

E. Output voltage ripple analysis under 4 basic cases

The output voltage ripple is an important index for evaluating the power quality of a converter, so it is necessary to analyze the output voltage ripple for the four basic cases.

The output voltage ripple can be calculated:

$$
\Delta u = \frac{\Delta q}{C} = \frac{1}{C} \int_{t_{start}}^{t_{stop} + \frac{T}{2}} \left( i_s \right) dt = \frac{i_s\_active + i_s\_circulating}{C}, \quad (13)
$$

where $C$ is the bus capacitance of the output side, $T$ is the switching period, and $i_s\_mean$ is the average value of the secondary current. $i_s\_active$ is the average value of the active component of $i_s$; $i_s\_circulating$ is the average value of the circulating component of $i_s$, and $t_{start}$ is any time.

When the polarities of $i_s$ and $u_cD$ are different, this part of $i_s$ is defined as the active component and vice versa.

The average value of the active component of $i_s$ is determined by the load conditions, which are given in the following equation.

$$
i_s\_active = \frac{P_o}{U_o}, \quad (14)
$$

where $P_o$ and $U_o$ are the output power and output voltage, respectively.

In Cases 1 to 3, there is no circulating component in $i_s$, so that $i_s\_circulating$ is 0. However, in Case 4, $i_s\_circulating$ is not 0. Therefore, we can know that:
The output voltage ripples of Cases 1 to 3 are the same as that of the Normal Case, but smaller than that of Case 4. For Case 4, the longer $\Delta t_4$ is, the bigger $i_{\text{circulating}}$ is. As a result, the output voltage ripple will be larger.

Based on above analysis of the four basic cases, the influence of the different types of gate drive delays can be summarized as shown in Table I.

<table>
<thead>
<tr>
<th>Component part</th>
<th>Type A</th>
<th>Type B</th>
<th>Type C</th>
<th>Type D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applied Model</td>
<td>Model I</td>
<td>Model I</td>
<td>Model I</td>
<td>Model II</td>
</tr>
<tr>
<td>Soft switching condition</td>
<td>Primary</td>
<td>ZVS</td>
<td>ZVS</td>
<td>ZVS</td>
</tr>
<tr>
<td></td>
<td>Secondary</td>
<td>ZCS</td>
<td>ZCS</td>
<td>ZVS</td>
</tr>
<tr>
<td>Circulating component of $i_g$</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Efficiency decrease</td>
<td>Slight</td>
<td>Slight</td>
<td>Obvious</td>
<td>Obvious</td>
</tr>
<tr>
<td>Output voltage ripple</td>
<td>Small</td>
<td>Small</td>
<td>Large</td>
<td>Large</td>
</tr>
</tbody>
</table>

\[ \Delta u_{\text{Case 4}} > \Delta u_{\text{Case 1,2,3}} = \Delta u_{\text{Normal Case}}. \]  

The proposed design procedure consists of three steps.

1. \textit{Make a list of the switch models to be selected.}
   First, determine the voltage and current level of the primary and secondary switches according to the required voltages of the primary and secondary dc buses and the rated power.

2. \textit{Select components of the driver circuit.}
   “Components” here mainly refer to the digital isolator and driver IC, which are the main sources of the propagation delay. The selection principle is to make the propagation delay of the primary and secondary sides as the same as possible. If conditions permit, choosing the same models for the isolator and driver IC for the primary and secondary sides is recommended.

3. \textit{Choose the final models of the switches for the primary and secondary sides.}
   The subscript “p” refers to variables related to the primary side and the subscript “s” refers to variables related to the secondary side.

We denote that:

\[
\begin{align*}
\Delta t_{\text{inc}} &= t_{\text{inc,p}} - t_{\text{inc,s}}, \\
\Delta t_{\text{d,om,ailt}} &= t_{\text{d,om,ailt,p}} - t_{\text{d,om,ailt,s}}.
\end{align*}
\]

Then (4) can be rewritten as:

\[
\theta = \frac{\Delta t_{\text{d,driver}} - (\Delta t_{\text{inc}} + \Delta t_{\text{d,om,ailt}})}{T}.
\]

In order to make \( \theta \) equal to 0, we need guarantee \( \Delta t_{\text{inc}} + \Delta t_{\text{d,om,ailt}} = \Delta t_{\text{d,driver}} \). \( \Delta t_{\text{d,driver}} \) and \( \Delta t_{\text{d,om,ailt}} \) are constant. These values can be obtained directly from the datasheet. The calculation of \( \Delta t_{\text{inc}} \) is more complex, and its expression can be derived through the $RC$ charging equation:

\[
\Delta t_{\text{inc}} = R_{gs,0}C_{gss} \int \left( \frac{V_{gs}}{V_{gs,p}} - \frac{V_{gs}}{V_{gs,s}} \right) dt.
\]

The input capacitance $C_{gss}$ and gate threshold voltage $V_{gsth}$ can be found in the datasheets of switches. $V_{gs,p}$ and $V_{gs,s}$ are the output voltages of the driver circuit and are also provided in

A. \textit{Offline design procedure}

B. \textit{Online design procedure}

C. \textit{Redesign procedure}
the datasheet of the driver IC. The recommended value for \( R_g \)
can be found in the reference design of the selected driver ICs and switches. Further, we can also adjust the value of \( R_g \) to
tune the length of \( \Delta t_{inc} \). According to (19), larger \( R_{g,p} \) and
smaller \( R_{g,s} \) lead to a longer \( \Delta t_{inc} \) and vice versa.

The steps for choosing the final models are as follows:

1. Calculate \( \Delta t_{inc} + \Delta t_{d,om,all} \) for all the models in the list
   mentioned in Step 1,

2. Choose a pair of primary and secondary switches whose
   \( \Delta t_{inc} + \Delta t_{d,om,all} \) is closest to \( \Delta t_{d,driver} \) as calculated by (16),
   and

3. Fine-tune \( \Delta t_{inc} \) by adjusting the values of \( R_{g,p} \) and \( R_{g,s} \)
to make \( \theta \) closer to \( \theta \).

B. Online close-loop control algorithm

By adopting the proposed design procedure, the influences of
the gate drive delay can be minimized in most situations.
However, this design procedure has its own limitations.

In theory, it is possible to make \( \theta \) equal to \( 0 \) by adjusting the
gate resistance, but it cannot always be guaranteed because the
gate resistance should not be larger or smaller than its recommended value too much. If the gate resistance is too small,
the waveform of \( V_{gs} \) may rise or fall so fast that it causes a
larger \( \frac{dV}{dt} \) and \( \frac{dI}{dt} \). If the gate resistance is too large, the
waveform of \( V_{gs} \) may rise or fall so slowly that the switches
stay in the variable resistance area too long during the
switching transient, causing an extra switching loss. Additionally, this design procedure cannot guarantee \( D_1 = D_2 \),
because it aims to reduce \( \theta \) as much as possible.

As a result, a close-loop compensation algorithm is proposed
to further reduce the influence of the gate drive delay.

As analyzed in Section III, Type C and Type D have
the longest gate drive delays. Therefore, the principle of the
close-loop compensation algorithm is to avoid Type C and
Type D and at the same time eliminate the impacts on Type A
and Type B.

The negative effects of Type C and Type D are mainly
caused by Case 4. Since the feature of Case 4 is that the primary
switches turn off before the secondary switches, an effective
way to avoid Case 4 is to change the phase shift between the
primary and secondary PWM signals to guarantee that the
primary switches turn off no earlier than the secondary
switches.

This raises the following question: what is the specific value of
the phase shift?

In theory, the phase shift \( \theta_{shift} \) can be calculated as:

\[
\theta_{shift} = \frac{-\Delta t_s}{T} = D_1 - D_2 - \theta. \tag{20}
\]

However, the exact values of \( \theta, D_1, \) and \( D_2 \) can only be
measured experimentally instead of theoretical calculation
because of the dispersion of the non-ideal parameters. Measuring \( \theta_{shift} \)
manually for every prototype is unacceptable due to its time cost. This is the reason why we need a close-loop
algorithm in order to implement the compensation automatically.

A detailed step-by-step flowchart of the proposed close-loop
compensation algorithm is illustrated in Fig. 12 and algorithm
cycle consists of three steps.

Step 1: Sampling

Output voltage \( U_{out} \), output current \( I_o \), and the maximum
value of the primary current \( I_{p,max,measure} \) are sampled.

Step 2: Estimation of \( I_{p,max,ref} \)

\( I_{p,max,ref} \) represents the value of \( I_{p,max} \) under the sampled
\( U_{out} \) and \( I_o \) when the converter is under the condition of
the Normal Case. \( I_{p,max,ref} \) is estimated through \( U_{out} \) and \( I_o \).
With the established mathematical model, i.e. (6) and (8), of
the Normal Case, the expression of \( i_p \) can be derived. Denote the
function of \( i_p \) as \( i(p, \phi, U_{out}, I_o) \).

We proposed a fast estimation algorithm to calculate
\( I_{p,max,ref} \). Firstly, we need to estimate \( \phi_{max} \) and the moment
when \( i_p \) reaches its maximum value. \( \phi_{max} \) is the root of (21).

\[
i_p(\phi_{max}, U_{out}, I_o) = \frac{d i}{d \phi} |_{\phi_{max}} = 0 \tag{21}
\]

We choose the Newton-Raphson method [32] to solve \( \phi_{max} \).
First, we need to set the value of \( \phi_0 \), which is the initial
estimated value of \( \phi_{max} \). If the algorithm runs for the first cycle,
we set \( \phi_0 = \pi/2 \), because \( \phi_{max} \) is near \( \pi/2 \). Second, we need

![Fig. 12. Step-by-step flowchart of the proposed close-loop compensation algorithm.](image-url)

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to calculate $\phi_{n+1}$ by (22).

$$\phi_{n+1} = \phi_n - \frac{\Delta P_f(\phi_n, U_{out}, I_0)}{\Delta P_f(\phi_n, U_{out}, I_0)}$$

(22)

$\phi_{n+1}$ is the estimated value of $\phi_{max}$ in the current algorithm cycle. $\phi_n$ is the estimated value of $\phi_{max}$ in the last algorithm cycle. $\phi_n$ equals to $\phi_0$ when the algorithm runs for the first cycle. Third, we need to calculate $I_{p,max,ref}$ by (23).

$$I_{p,max,ref} = I_p(\phi_{n+1}, U_{out}, I_0)$$

(23)

The time consumption for the estimation of $I_{p,max,ref}$ is minimized because only one iteration is needed in each cycle. Fig. 13 shows the simulation results of the proposed estimation algorithm. $I_p$ changes from 0.2 to 0.4 at the 5th iteration and the estimated $I_{p,max}$ equals the actual value of $I_{p,max}$ after three iterations. The result shows that proposed estimation algorithm is able to track the actual current values.

![Fig. 13. Simulation results of the proposed fast estimation algorithm.](image)

**Step 3: Update $\theta_{shift}$**

First, we need to calculate $\Delta I_{p,max}$.

$$\Delta I_{p,max} = I_{p,max,ref} - I_{p,max,measured}$$

(24)

Second, we need to identify the status of the close-loop compensation algorithm. The algorithm has two status i.e. PART I and PART II, depending on the judgement if the gate drive delay has been fully compensated.

If the algorithm status is PART I and $\Delta I_{p,max} < \eta_1 I_{p,max,ref}$ is not satisfied. A PI controller is used to update $\theta_{shift}$. If $\Delta I_{p,max} < \eta_1 I_{p,max,ref}$ is satisfied, the algorithm will judge the gate drive delay is fully compensated. The algorithm status will be set to PART II, and a small adjustment will be added to $\theta_{shift}$ ($\theta_{shift} = \theta_{shift,pre} + \Delta \theta$). $\eta_1$ determines the compensation accuracy and $\Delta \theta$ can further increase compensation accuracy.

If the algorithm status is PART II and $\Delta I_{p,max} > \eta_2 I_{p,max,ref}$ is not satisfied. $\theta_{shift}$ will not change. If $\Delta I_{p,max} > \eta_2 I_{p,max,ref}$ is not satisfied, the algorithm will judge that the gate drive delay is not fully compensated. The algorithm status will be set to PART I to compensate the existing gate drive delay. $\eta_2$ need be larger than $\eta_1$.

The principle of hysteresis comparison is adopted to raise the anti-interference capability of the proposed compensation algorithm: If the algorithm status is PART I, the criterion of the existence of gate drive delay is $\Delta I_{p,max} < \eta_1 I_{p,max,ref}$, on the other hand, if the status is PART II, the criterion is $\Delta I_{p,max} > \eta_2 I_{p,max,ref}$. The margin for disturbance is $\eta_2 I_{p,max,ref} - \eta_1 I_{p,max,ref}$.

**C. Selection of the feedback variable for the close-loop compensation**

The maximum value of the primary current $i_{p,max}$ was chosen as the feedback variable for the following two reasons.

1) $i_{p,max}$ is negatively associated with $\theta_{shift}$.

We can calculate the relationship between $i_{a0}$ and the maximum value of the primary current $i_{p,max}$ under different $k$ values with the established mathematical model of Case 4, as illustrated in Fig. 14.

![Fig. 14. Three-dimensional $i_{p,max}$ contour over $k$ and $i_{a0}$.](image)

Fig. 14 shows that $i_{p,max}$ is positively associated with $i_{a0}$ under different $k$ values. According to the steady-state analysis for Case 4 in Section III, the longer $\Delta t_4$, the smaller $i_{a0}$. According to (16), the longer $\Delta t_4$, the larger $\theta_{shift}$ is.

As a result, $i_{p,max}$ is negatively associated with $\theta_{shift}$. Such a monotonic relationship between $i_{p,max}$ and $\theta_{shift}$ makes $i_{p,max}$ suitable to be used as a feedback variable in the close-loop control.

2) $i_{p,max}$ is a more suitable feedback variable than other characteristic variables.

Using the mathematical model of Case 4, we found some other characteristic variables that also have a monotonic relationship with $\theta_{shift}$: Those characteristic variables are listed in Table II.

<table>
<thead>
<tr>
<th>Characteristic variable</th>
<th>Relationship</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero crossing time of primary current $t_{zero,p}$</td>
<td>↓</td>
</tr>
<tr>
<td>Initial Value of primary current $i_{a0}$</td>
<td>↑</td>
</tr>
<tr>
<td>Maximum value of secondary current $i_{s,max}$</td>
<td>↓</td>
</tr>
<tr>
<td>Zero crossing time of secondary current $t_{zero,s}$</td>
<td>↑</td>
</tr>
<tr>
<td>Initial Value of secondary current $i_{a0}$</td>
<td>↓</td>
</tr>
</tbody>
</table>

Note: ↑ means the corresponding variable has a positive correlation relationship with $\theta_{shift}$ and vice versa.

In order to get the exact value of zero crossing time, a high bandwidth current sensor is essential to guarantee the delay time is low enough. The switching frequency of CLLC converters is usually several hundreds of kHz, which means the corresponding current sensors need high bandwidth and will be too expensive to use in practical applications.
For the sampling of the initial value of the primary or secondary current, the electromagnetic interference during the switching transient is the main restricting factor. The sensors and signal processing circuits are sensitive to the high $di/dt$ and $dv/dt$ caused by the switching operation. The suppression of the interference will lead to extra costs for the sensors and corresponding signal processing circuits.

Instead, the reaching time of the maximum value is out of switching transient so that $i_{p,max}$ or $i_{s,max}$ can be sampled without being disturbed. The sampling of $i_{p,max}$ or $i_{s,max}$ does not require a very short delay time of the current sensor so a cheaper sensor can be used. Therefore, $i_{p,max}$ and $i_{s,max}$ are both suitable. In this paper, we chose $i_{p,max}$ as the feedback variable, but $i_{s,max}$ can also be chosen. The proposed fast estimation algorithm can also be applied for $i_{s,max}$.

V. EXPERIMENTAL VERIFICATION

A laboratory prototype was designed, built, and tested to demonstrate the proposed hybrid compensation scheme. The corresponding experimental results are given and analyzed in this section. The prototype is shown in Fig.15, and its parameters are listed in Table III. In the experiment, the tested input voltage is 200V, the load resistance for 25%, 50%, 75%, 100% load is 6.4Ω, 3.2Ω, 2.13Ω, 1.6Ω respectively.

Theoretical values of $\theta$, $D_1$, and $D_2$ in the original design were calculated using (1)-(4) and (16)-(19), and they were 0.0277, 0.5018, and 0.5082, respectively. Their relationship is

$$\theta > 0, \quad D_1 - D_2 < \theta.$$  
(25)

From (5) and Fig. 4 we can know that a Type D gate drive delay exists. The steady-state waveforms of the original design are illustrated in Fig. 16(a) and Fig. 17(a). They are the waveforms of Type D, and are consistent with the calculations above.

In Fig.16 (a), at the beginning of $\Delta t_4$, $u_{AB}$ falls while $u_{CD}$ remains positive. During $\Delta t_4$, $i_p$ decreases rapidly while $i_{lm}$ increases following the shape of a triangular wave. Since $\Delta t_4$ is very long, the initial value of $i_p$ is so small that the output capacitor of the primary switches cannot be fully charged. As a result, voltage $u_{AB}$ is an oscillation waveform during $\Delta t_4$ and the dead time. Switches on the primary side work under hard switching. On the secondary side, there is a large circulating component in $i_s$ and the secondary side switches work under the ZVS instead of the ZCS. Because of the change in the operating process, the efficiency is only 84.79%. The measured efficiency data and steady state waveforms match the theoretical analysis well.

The proposed hybrid compensation scheme is applied to the original design to reduce the gate drive delay. First, we implemented the offline compensation and got the improved design. The comparison of values of $\theta$, $D_1$, and $D_2$ between the original and the improved design is shown in Table IV.

In the improved design, $\theta$ is much closer to 0 and $D_1$ is much closer to $D_2$. According to formula (5), the gate drive delay in the improved design is reduced compared to the original design.
The steady-state waveforms after the offline compensation, i.e. the waveforms of the improved design, are illustrated in Fig. 17 (b).

Fig. 17 (b) shows that the initial value of $i_p$ increases. The output capacitors of the primary switches are fully charged as a result ZVS is achieved. The secondary switches still work under ZVS but the circulating component of $i_s$ is obviously suppressed. The efficiency of the improved design is increased to 92.61%.

Second, we implemented the online compensation on the improved design. The dynamic waveforms of $i_p$ and $i_s$ are illustrated in Fig.17(d). After online compensation, the maximum value of $i_p$ increased and that of $i_s$ decreased. The steady-state waveforms after the online compensation are illustrated in Fig.17(c). The initial value of $i_p$ increases further and is equal to that of $i_{L_m}$. The circulating component of $i_s$ is reduced to 0 so that the secondary switches work under ZCS. The Type D of gate drive delay are totally compensated and the efficiency increased to 94.99%.

The mathematical models proposed in Section III are also verified. In Fig.16 (a) and Fig.17 (a)-(c). The dashed line waveforms are theoretical waveforms calculated by the proposed mathematical models. The theoretical waveforms match well with the measured waveforms. The proposed mathematical models have a high accuracy.

The waveforms of output voltage ripple are illustrated in Fig. 16 (b). The voltage ripple of the original design is 240 mV. After the offline compensation, the value is 167 mV. After online compensation, the voltage ripple is further reduced to 88 mV. Output voltage ripple is reduced with the reduction of gate drive delay.

![Efficiency Comparison](image-url)  
Fig. 18. Full load range efficiency comparison of the original design, offline compensation, and online compensation.

A full load range efficiency comparison between the original design, offline compensation, and online compensation is illustrated in Fig. 18. From the curve labeled with “original design” to the curve labeled with “offline compensation”, the offline part of the proposed compensation scheme is implemented. The physical gate drive delay is reduced. From the curve labeled with “offline compensation” to the curve labeled with “online compensation”, the online part of the proposed compensation scheme is implemented. The remaining gate drive delay is compensated. From Fig. 18 we can know that, with the reduction of gate drive delay, the efficiency increases with full load range.
VI. CONCLUSION

A CLLC converter is often used as an isolated linker between high and low voltage buses where the CLLC converter operates under the open-loop condition at the resonant frequency. In this kind of applications, the high efficiency feature of CLLC converters is usually thought as common sense.

However, in this paper it is pointed out that the operating process of the CLLC converter under the open-loop control at the resonant frequency could also be significantly influenced by the gate drive delay. A comprehensive steady-state analysis of the influences caused by the gate drive delay is presented and a hybrid compensation scheme is proposed. Experimental verifications have been conducted. Based on the above works, the following conclusions can be obtained:

1. The proposed mathematical models for the gate drive delay are of high accuracy, which has been demonstrated by the theoretical analysis and experimental tests. They can precisely describe the influences of gate drive delay in CLLC converters. From the analysis it can be found, the parameter matching between primary and secondary side switches as well as the driver circuit is a decisive factor of the performance of CLLC converters.

2. The negative influences of the gate drive delay can be restrained by the proposed hybrid compensation scheme effectively. Essentially, the soft-switching conditions of CLLC converters are ensured by using the proposed hybrid compensation scheme, hence, the efficiency has been enhanced.

References


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