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Chang, Bingdong

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Bingdong Chang

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Bingdong Chang[a)]

AFFILIATIONS

DTU Nanolab, Technical University of Denmark, Ørsteds Plads, Building 347, 2800 Kgs. Lyngby, Denmark

[a)]**Electronic mail:** bincha@dtu.dk

ABSTRACT

Self-aligned double patterning (SADP), or spacer lithography, is a widely used technique in the semiconductor industry for high-throughput nanoscale pattern definition and thus is of great significance for very-large-scale integration, large-area photonic device fabrications, and other applications. In a standard SADP flow, chemical vapor deposition or atomic layer deposition is used to deposit a conformal spacer layer, which is typically a dielectric material. The spacer composition and film quality will influence downstream critical dimension control. However, samples have to go through multiple processing environments, and fabrication complexity is thus increased. In this work, an *in situ* SADP process is proposed, with all the fabrication steps being integrated into a single process inside a commercially available plasma etching equipment. The spacer layer is a plasma-deposited fluorocarbon film, which has a uniform step coverage and a good etch selectivity to silicon. Various nanostructures have been fabricated to prove the capability of this technique. With its high integrity and technical convenience, this method can be promising to improve the throughput and efficiency of nanofabrication in the semiconductor industry, microelectromechanical systems, and photonic engineering.

I. INTRODUCTION

Driven by the ever-increasing need for industrial production and academic research, technical limits are being pushed forward in the semiconductor industry for higher-resolution manufacturing with structural dimensions of fewer nanometers or even toward the atomic scale.[1] Lithography, as the fabrication technique with a critical influence on the final structure dimensions, has been studied and developed extensively in the last few years. While charged particle lithography (such as electron beam lithography and ion beam lithography) is suffering from relatively low throughput and mostly being used for small-scale prototype fabrications,[2] extreme ultraviolet (EUV) lithography has shown its superiorities over traditional optical lithography in recent years, offering possibilities for volume production with a half-pitch size of 13 nm.[3] However, due to the high economical cost of EUV lithography equipment, most of the semiconductor industry still rely on traditional optical lithography, and multiple patterning techniques are employed to enhance the pattern density and overcome the diffraction limit. Self-aligned double patterning (SADP) or spacer lithography is a widely used multiple patterning method.[4] Briefly speaking, spacer layers are first formed by deposition or reaction on the transferred features from lithography patterns and then etched back afterward so that the rest of the spacer on the sidewall of the features can serve as masks for the second etching step; therefore, structure density can be doubled or even quadrupled by repeating the procedure. Since high-resolution patterning with dense pitch sizes can be achieved with a reasonable economic cost, SADP has been widely used in the semiconductor industry for memory and logic device manufacturing.[3] Beside, the technique has also shown its advantages in other fields like photonic engineering and microelectromechanical systems, e.g., microfluidic channels[5] and large area photonic devices such as wire grating polarizers.[6–8]

The standard SADP process, however, has to involve multiple fabrication techniques. Specifically, chemical vapor deposition (CVD) is normally employed for a conformal deposition of the spacer layer, which is typically a dielectric material such as silicon nitride.[9,10] With a uniform step coverage and accurate thickness control of the spacer layer, atomic layer deposition (ALD) has shown its advantages for SADP processing,[11,12] while highly purified precursors and the slow deposition rate can set limitations for certain applications. Apart from these techniques, thermal oxidation[13] and direct coating of organic spacer films[14] are also alternative options to

reduce equipment costs. A common drawback among the above-mentioned techniques, however, is that different processing equipment are required for SADP process, and samples have to be transferred through various processing environments, thus increasing the manufacturing complexity and limiting the yield. Besides, some of the spacer deposition processes can introduce high temperatures or a wet environment, which is not favorable for samples sensitive to thermal stress or capillary forces.

In this paper, a novel SADP process is proposed for a higher level of process integrity. Instead of involving additional equipment for thin film formation, the whole procedure is performed inside a commercially available plasma etching system, including (1) first pattern transfer after lithography, (2) spacer deposition, (3) spacer etching back, and (4) second pattern transfer. The novelty of this technique resides in using a fluorocarbon (FC) film as the spacer layer, which is deposited *in situ* inside the plasma etch chamber by perfluorocyclobutane (C_4F_8)-based plasma. The deposition mechanism is discussed and the film quality is characterized. Moreover, optical emission interferometry (OEI) is applied to monitor the FC film thickness during the deposition process, making the process more controllable. To demonstrate the capability of this technique, high aspect ratio (HAR) silicon nanostructures have been fabricated, with the initial patterns defined by both ultraviolet (UV) lithography and high-resolution electron beam lithography. Compared with standard SADP techniques, this method offers the possibility of an *in situ* process with less fabrication complexity, which is likely to lead to an increase in volume production yield in the semiconductor industry. Additionally, it can provide a low cost method to improve pattern resolution and density in facilities with limited access to advanced lithography techniques.

II. EXPERIMENT

A. Fabrication details

All the patterns in this work were defined by either maskless UV lithography or electron beam lithography, and 4-in. silicon wafers (single side polished, ⟨100⟩ crystalline orientation) were used as substrates. For microscale patterning, a direct writing system (MLA100, Heidelberg Instrument) was employed, which is equipped with a 365 nm LED light source, and the resist was negative tone photoresist AZ nLOF 2020 (MicroChemicals) with a thickness of 1.5 μm. For nanoscale patterning, a 100 kV electron beam writing system (JEOL JBX-9500FC, JEOL) was used, with 85 nm-thick positive tone electron beam-sensitive resist AR-P 6200.04 (ALLRESIST GmbH).

After pattern definition with lithography, all the fabrication steps in the SADP process were performed with a dual-coil inductively coupled plasma (ICP) etching system (DRIE Pegasus, SPTS), which is a widely used equipment for silicon-based prototype productions. The system is equipped with a 13.56 MHz RF coil generator synchronized with a 13.56 MHz RF platen electrode for independent control of plasma generation and ion acceleration; switched process is available with SF_6 gas for etching and C_4F_8 gas for passivation. The chuck and funnel are designed to handle 4-in. wafers. The detailed parameter settings are listed in Table I. A descum step with oxygen plasma was first applied to clean the resist residues after lithography. For the first pattern transfer, a three-step switched plasma etching process was performed with a coil power of 500 W (the recipe named as DREM 0.5 kW). The structures were then cleaned with oxygen plasma etching, before C_4F_8 plasma was applied for deposition of the FC thin film. To etch back the FC spacer layer, oxygen plasma etching is used again, before the second pattern transfer, which utilizes the spacer sidewalls as a mask can proceed. It can be seen in Table I that the parameter setting in the second etching step (recipe named as DREM 1 kW) is different compared with DREM 0.5 kW in the first etching step, but practically there are no limitations on the choice of etching recipes in the second pattern transfer step, since the patterns are already defined by FC spacers. The principle of the switched etching process (named as DREM process) has been introduced in previous studies by the author.[15] Briefly speaking, DREM process is a modified Bosch process, with three steps well defined in each sequence, including FC passivation (Deposit), FC removal with low-pressure argon plasma (Remove), and silicon etching with SF_6 plasma (Etch). Compared with the traditional Bosch process, DREM process has the advantage of good etching directionality and high etching selectivity and thus is favorable for etching high aspect ratio structures,[15] 3D periodic structures,[16,17] and even tilted structures.[18,19]

TABLE I. Overview of parameter settings of the *in situ* SADP process (the platen chiller temperature is 0 °C during the entire process).

			Parameter settings						
	Process step		Time (s)	Coil power (W)	Platen power (W)	Pressure (mTorr)	SF_6 (SCCM)	C_4F_8 (SCCM)	Ar (SCCM)	O_2 (SCCM)
1	Descum		90	500	20	5	0	0	0	100
2	First etch (DREM 0.5 kW)	Deposit	3.2	500	0	10	10	25	100	0
		Remove	1.0	500	40	1.8	10	5	75	0
		Etch	1.5	500	0	10	30	5	100	0
3	Resist strip		600	2500	25	5	0	0	0	200
4	FC deposition		30	1000	20	10	0	200	0	0
5	FC etch back		165	2500	25	5	0	0	0	200
6	Second etch (DREM 1 kW)	Deposit	3.2	1000	0	11	15	40	100	0
		Remove	1.0	1000	40	2	15	5	75	0
		Etch	1.7	1000	0	11	40	5	100	0

The thickness of the FC film during deposition was measured *in situ* by OEI with an optical end point detection system (Verity Instruments) and verified with a spectroscopic ellipsometry system (VASE, J. A. Woolam Co., Inc.). To characterize the surface roughness and morphology of the plasma-deposited FC film, an atomic force microscope (AFM) was used with the tapping mode (ICON PT, Bruckers) and a scanning electron microscope (SEM) was also employed for structure inspections (Supra V60, Zeiss).

B. SADP mechanism

Figure 1(a) shows a schematic illustration of the process flow (from a cross-sectional view). The process starts with pattern definition using standard lithography techniques, and photoresist patterns are generated with the linewidth of W_1 and pitch of P_1 (here we consider a simple design of patterns with periodic line arrays). Afterward, plasma etching is performed to define the mandrels (or cores). Without retrieving the sample from the plasma etching equipment, the resist is striped off by an oxygen plasma etching process, and an FC spacer layer is deposited directly with the C_4F_8 plasma deposition process.

It should be noticed that the FC deposition inside the ICP etching equipment is like a plasma-enhanced chemical vapor deposition process and thus a conformal step coverage is limited by the ion incoming angles and radical transport into the micro- and nanostructures; therefore, the FC layer thickness on the sidewall

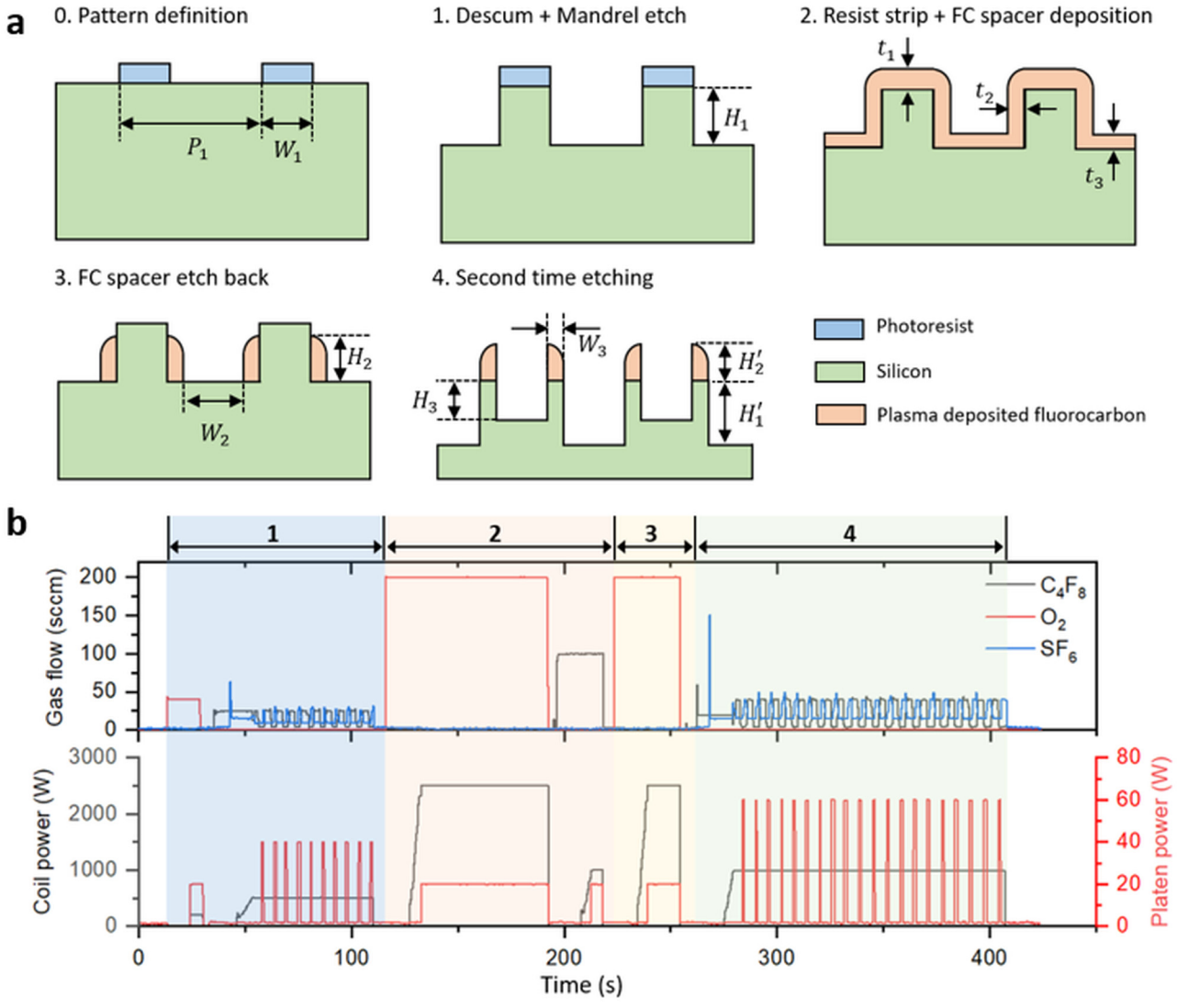

FIG. 1. (a) Schematic illustration of process flow of SADP process with FC as the spacer layer; (b) *In situ* monitoring of key parameters during the whole SADP process.

(t_2) is generally smaller compared with the thickness on top (t_1) and the bottom of the structures (t_3). In order to proceed to the second pattern transfer step, the height of the mandrel (H_1) has to be larger than the FC layer on the bottom of structures (t_3). In order to assist the ion and radical transport onto the structured surface, a DC bias is applied on the platen electrode with a relatively low pressure during the FC deposition, which can also lead to a smooth FC film.[20,21]

In the third step, an oxygen plasma etching process was performed again to remove the FC layer from both top and bottom of the structures; thus, FC masks are formed on the sidewall with a reduced height of H_2. It can be seen that mandrels with a large height H_1 can give a thick FC mask, which is favorable for deep etching in the second pattern transfer step; however, it will also lead to a nonuniform deposition of FC on the sidewall of the mandrels, and the mechanical stability of the FC mask will also be compromised,; thus, the aspect ratio of the mandrel (H_1/W_1) is below 2 for all the structures in this work.

The process continues with the second pattern transfer, where the DREM process is performed again with FC masks, and silicon is etched both on top and bottom of the mandrels. The structures fabricated after the second patterning step have a reduced critical dimension (CD) of W_3 compared with W_1 in original patterns and an aspect ratio defined by H_3/W_3; additionally, the spatial frequency is doubled from $1/P_1$ to $2/P_1$. Since the DREM process has advantages of good directionality and small sidewall roughness, a well-defined profile and small sidewall roughness can be achieved on the FC masks, which is favorable for the second pattern transfer.

Since all the fabrication steps have been integrated into a single process as introduced above, some important parameters can be monitored *in situ* during the whole procedure, which is convenient for process development and quality control. Figure 1(b) shows the evolution of some important parameters during the entire SADP process, including gas flow ratios of SF_6, C_4F_8, and O_2, and forward powers on both coil and platen electrodes. As per the parameter settings shown in Table I, 10 cycles of "DREM 0.5 kW" are performed during the mandrel definition and 20 cycles of "DREM 1 kW" are performed in the second pattern transfer; the switched signals can be clearly seen on the gas flows and platen forward power. This straightforward monitoring of the SADP processes can be quite difficult with traditional methods, where multiple fabrication equipment are involved.

III. RESULTS AND DISCUSSION

A. FC deposition and OEI studies

As can be seen from discussions above, a crucial step in the SADP process is the FC deposition step, which can directly influence the CD and quality of final structures. Normally, FC is used as inhibition species during a Bosch etching process, while the performance of an FC film as an etching mask has yet to be explored. In order to better understand FC deposition processes inside the plasma etching system, a discussion will be given in this section on the FC deposition mechanism; specifically, the deposition rate of the FC thin film will be compared for different parameter settings. For an accurate and convenient measurement of the FC deposition rate, OEI analysis has been performed, which is a standard technique in plasma diagnostics and real-time process monitoring.[22,23] Briefly speaking, OEI is a technical variation of optical emission spectroscopy, which can identify ionic species inside the chamber by detecting photon generations from de-excited electrons in a wide optical spectrum. Instead of monitoring the whole spectral range, the time evolution of emission intensities in specific wavelengths are traced in OEI, with a focal point on the surface of the wafer and a spot size of a few millimeters. When the wafer surface is covered by a thin film with time-varying thickness, interference patterns can be observed and the change in thickness can be calculated accurately.

Figure 2(a) shows an optical emission spectrum of the C_4F_8 plasma, with coil power of 3 kW, pressure of 20 mTorr, and C_4F_8 gas flow of 400 SCCM. For considerations of signal-to-noise ratio and temporal resolutions, spectral intensity at a wavelength of 440.1 nm was chosen for OEI monitoring, when FC thin films were deposited on pristine silicon wafers. Time evolution of emission intensities in the whole spectral range (200–800 nm) can be seen in Fig. 2(b), where periodic patterns indicate an increasing thickness of the FC thin film during a deposition time of 100 s. Since a higher sticking coefficient for FC radicals can be achieved with a lower chiller temperature, the period of the interferometric patterns at −19 °C chiller temperature is observed to be smaller compared with 20 °C.

By employing OEI, the deposition rate of FC thin films can be measured conveniently and accurately with various parameter settings, including chiller temperature, coil power, platen power, and processing pressure. First, a higher coil power generally gives a higher deposition rate [Fig. 2(c)]; this can be explained by an increasing dissociation level of deposition species, which can lead to a higher density of ions and radicals to participate in the FC growth process. Second, deposition rate at a lower chiller temperature at −19 °C are observed to be three to five times larger compared with the deposition rates at 20 °C. This coil power and temperature dependency of deposition rate agree with previous studies.[21,24] With a larger platen power, the deposition rate will increase and achieve a maximum at around 50 W as seen in Fig. 2(d); this is possibly due to more significant ion bombardments at a higher kinetic energy level, and the sputtering on FC surface will limit the deposition process. The pressure dependency of the FC deposition rate was also studied by manually controlling the valve position [Fig. 2(e)], and a higher deposition rate is achieved with a higher pressure, which is assumed to be caused by a longer lifetime of radicals inside the processing chamber. In the SADP process for high-resolution patterning, a controllable FC deposition is necessary; thus, a lower deposition rate can be favorable. In this work, the FC deposition step was performed with 1 kW coil power, 20 W platen power, 200 SCCM C_4F_8, 10 mTorr processing pressure, and a chiller temperature of 0 °C.

B. FC thin film characterization

For mass production in the semiconductor industry, minimizing both across-wafer uniformity and wafer-to-wafer uniformity is crucial for robust fabrication processes. While the latter indicates process repeatability, which can be improved by methods like chamber preconditioning, the former is more dependent on the equipment design, which can set intrinsic technical limitations on the throughput

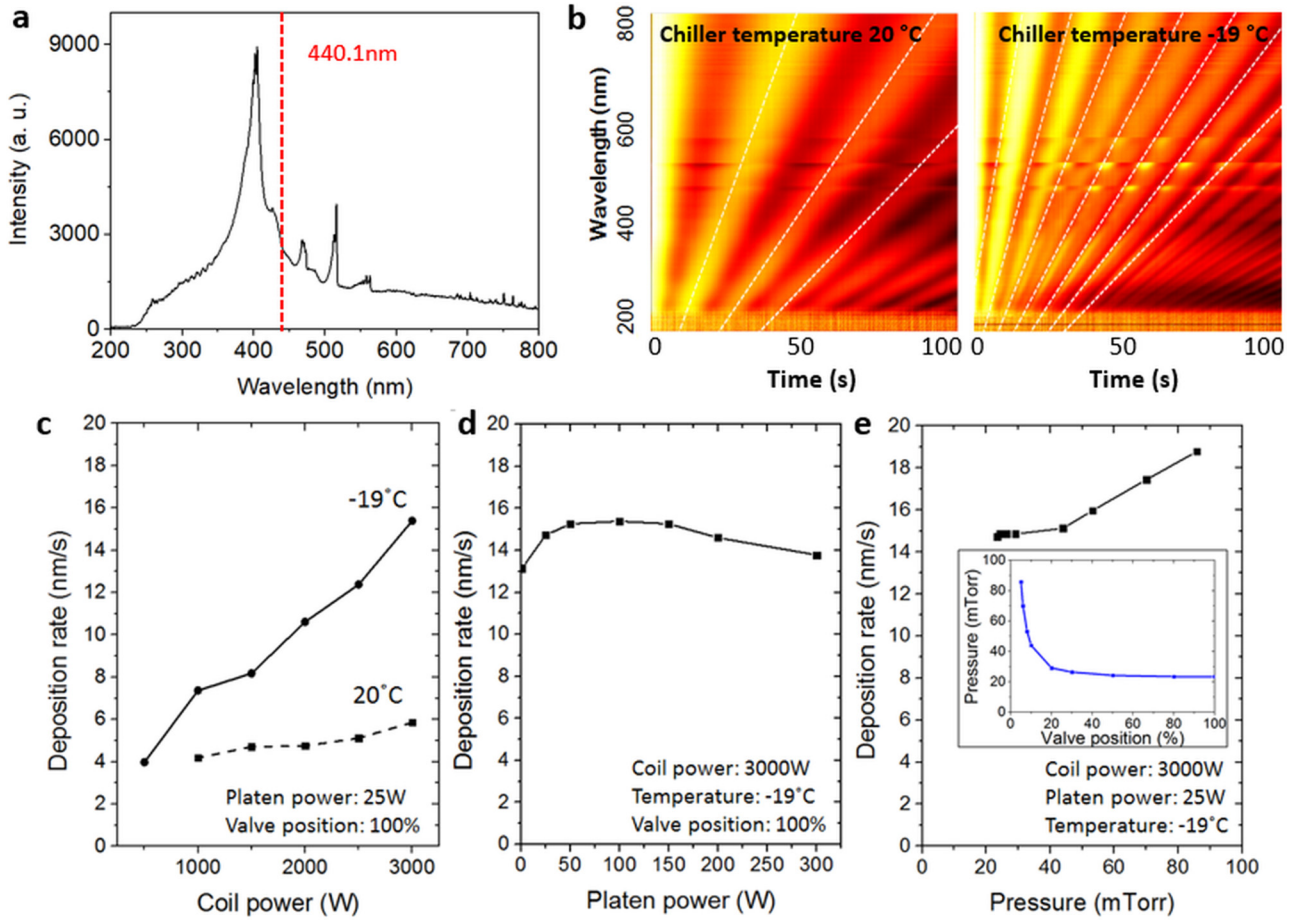

FIG. 2. Using OEI to study FC deposition as a spacer layer: (a) A typical optical emission spectrum of C_4F_8 plasma; (b) time evolution of optical emission spectrum on the whole wavelength range between 200 and 800 nm, with two different chiller temperatures of 20 and −19 °C. Deposition rates of FC measured with various parameter settings of (c) coil powers and chiller temperatures, (d) platen power, and (e) processing pressures.

and yield of production. Since FC spacer deposition is the essential step, during which CD is defined for the final structures, the deposition of FC should be ideally uniform across the whole wafer. Figure 3(a) shows the thickness of the FC layer measured on a 4-in. wafer, and the set point for FC thickness is 40 nm. After deposition, the thickness was measured and mapped with ellipsometry on 76 different positions across the wafer. The thickness measured in the center point is 43 nm, and a good deposition uniformity can be achieved inside the region with a distance of less than 2 cm from the center, where the average deposition thickness is 46.6 nm and the coefficient of variance is around 3.3%, which is acceptable for small-scale prototype productions. However, for a larger region with distance more than 2 cm from the center, the variation of FC thickness is significant. While a bell-shape distribution of FC thickness can be noticed in the center region, the deposition also seems to be more efficient on the edge of the wafer. This nonuniformity is supposed to be caused by the depletion of deposition species and nonuniform cooling efficiency on different positions of the wafer. Due to the chuck design of the specific etching equipment being used in this work, the center of the wafer is cooled down more efficiently compared with the periphery of the wafer; thus, the sticking coefficient is higher for deposition species, giving a thicker FC layer.[25] However, on the edge of the wafer, the depletion of deposition species is less significant, which will also lead to a thicker deposited FC layer. This variation of FC thickness across the wafer implies a nonuniform deposition of the FC spacer layer for the SADP process; thus, the across-wafer CD uniformity will be limited. An improved FC deposition uniformity can be expected with a lower chiller temperature and a chuck design dedicated for larger wafer sizes.

Another important issue to address is the quality of the deposited FC thin films, especially the surface roughness, which will have a strong influence on both line edge roughness and linewidth roughness of the final structures. An SEM image from a cross-sectional view is shown in Fig. 3(b), illustrating a uniform coverage of a 160 nm-thick FC film on a silicon substrate without observable

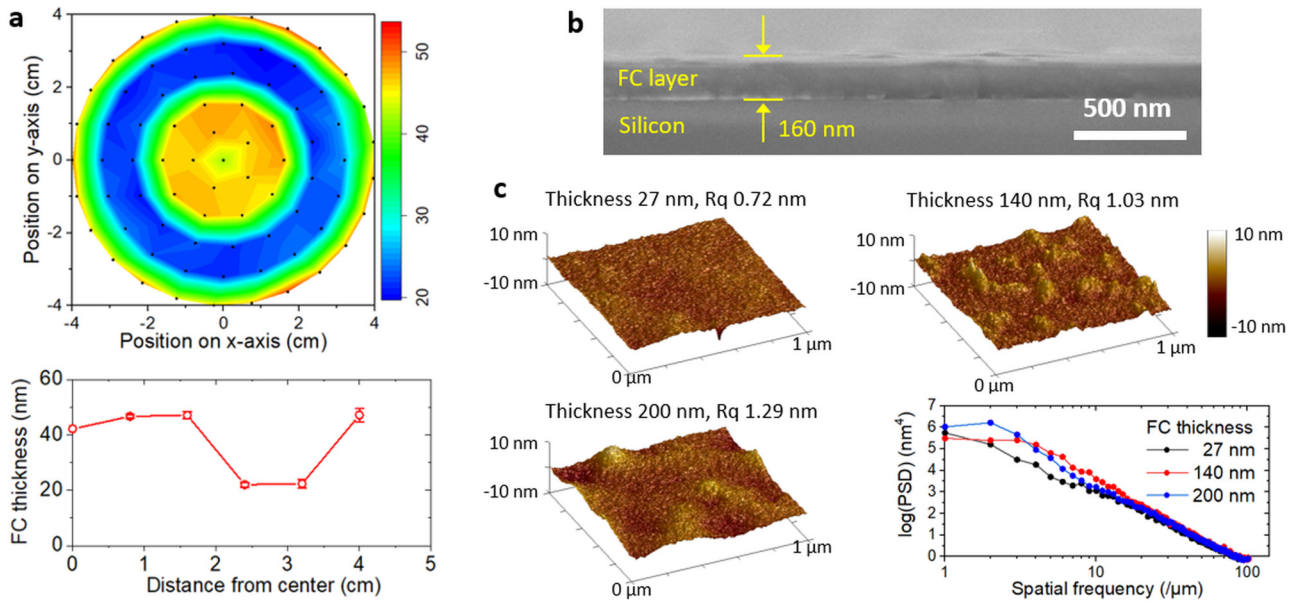

FIG. 3. Characterization of plasma-deposited FC thin film. (a) Measured deposition uniformity on a 4-in. wafer; (b) SEM image of the deposited FC film on a pristine silicon wafer; (c) Surface morphology of the FC thin film measured by AFM, showing surface roughness for different deposition thicknesses; power spectrum density is also plotted to illustrate the evolution of FC film surface morphology with an increased deposition thickness.

grains or aggregates. AFM was also performed on FC film surfaces within a square region with a size of 1 by 1 μm^2, with different FC thickness of 27, 140, and 200 nm. A surface morphology with aggregates can be noticed for a thicker FC layer, which could be explained by radical impinging and diffusion on the silicon surface.[26] For a FC film with thickness of 27 nm, surface roughness (characterized by root mean squared roughness, RMS or R_q) is 0.72 nm, which is comparable with previous studies on a continuous wave FC deposition.[27] For a thicker FC layer, the surface roughness increases, which is a well-known phenomenon for CVD processes. The evolution of surface roughness with FC film thickness is plotted with a 2D power spectrum density as in Fig. 3(c). When the FC thickness increases, the amplitude of roughness increases and is shifted to a lower spatial frequency range, implying the formation of aggregates. Considering that the FC film thickness has a coefficient of variance below 3%, the quality of the FC film should be sufficient for the second pattern transfer with a good geometry control.

C. Fabrication results

Figure 4 shows the application of our *in situ* SADP process for patterns initially defined by standard UV lithography, which should normally give a spatial resolution of above 1 μm due to the optical diffraction limit. Figure 4(a) contains SEM images showing the profile of the structures during different steps of the SADP process. The original linewidth of the patterns was 3.4 μm after the first pattern transfer step. After FC spacer deposition and etch back, FC masks are defined on the sidewall of the mandrels with a linewidth of 330 nm and a height of 1.59 μm, which can be transferred into silicon during the second pattern transfer step. Since FC films can be used as a hard mask with good etching selectivity (around 9 to silicon with the recipe DREM 0.5 kW), HAR silicon nanostructures can be created after the second pattern transfer. Besides, by tuning the FC deposition time, silicon structures with high spatial resolution can be fabricated. Figure 4(b) shows a HAR silicon nanofin structure with a linewidth of 30 nm and a height of 600 nm. Compared with the original patterns after the first etching step, the linewidth is reduced by 100 times, which is normally only possible with high-resolution patterning techniques such as electron beam lithography or ion beam lithography. HAR grating structures are shown in Fig. 4(c), with a linewidth of 160 nm and a height of 6 μm (giving an aspect ratio of 37.5). To demonstrate the flexibility of this technique for complicated patterns, concentric circular grating structures are fabricated as shown in Fig. 4(d), and the linewidth of the gratings is 110 nm with an aspect ratio of 39.

To demonstrate the size scalability of the *in situ* SADP process, electron beam lithography was used for the first pattern definition step. In Fig. 5(a) are SEM images of structure profiles during different process steps, from which we can see that the initial linewidth of the structures is 70 nm with a pitch of 300 nm. After FC spacer deposition and etch back, patterns were transferred into silicon structures, giving a reduced linewidth of 35 nm and height of 520 nm [as can be seen in Figs. 5(a) and 5(b)]. Since the pattern density is doubled after the second etching step, this method can be used to increase the throughput of electron beam lithography, which is normally limited by the long exposure time. At the same time, the spatial resolution can also be improved in a

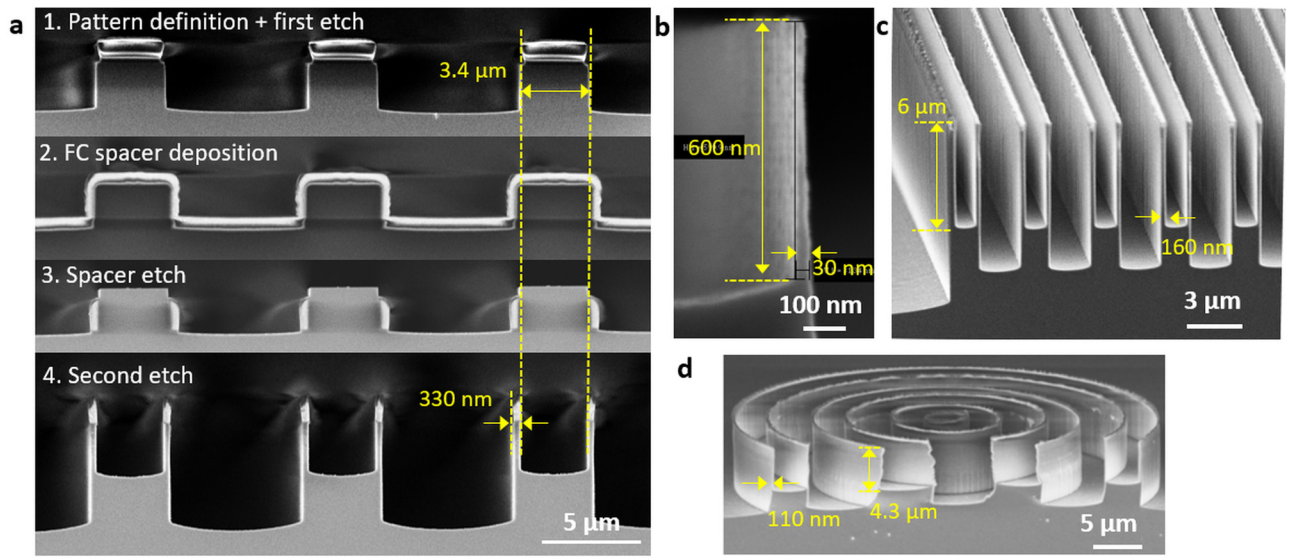

FIG. 4. Using an *in situ* SADP process with FC as the spacer to downscale microstructures fabricated with UV lithography: (a) SEM images from a cross-sectional view showing the profiles of structures during the SADP process; (b) a HAR nanofin structure; (c) a tilted view of fabricated nanogratings; (d) a tilted view of concentric circular gratings.

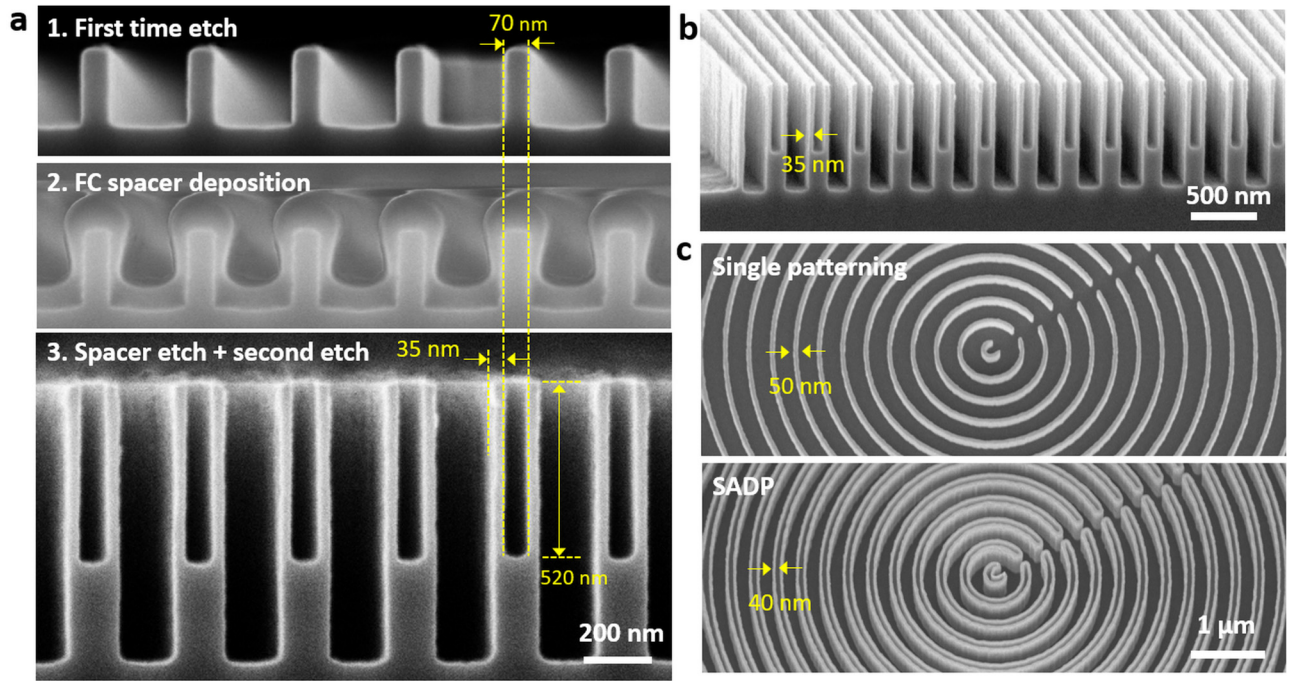

FIG. 5. Using an *in situ* SADP process to downscale nanostructures fabricated with electron beam lithography: (a) SEM images from a cross-sectional view showing the profiles of structures during the SADP process; (b) fabricated nanogratings with doubled pattern density; (c) SEM images from a tilted view showing concentric circular gratings fabricated with single patterning (above) and SADP (below).

controllable way, which is favorable for fabricating large-area subwavelength grating structures.[28] Concentric circular gratings were also fabricated with both single patterning and double patterning for comparison, and SEM images are shown in Fig. 5(c). The structures with double patterning are well defined with a reduced linewidth of 40 nm and smooth line edges, implying a good flexibility and size scalability of this technique. It has to be addressed that for structures with small pitch sizes, conformality of the FC spacer layer is degraded, which can be observed in Fig. 5(a), where the thickness of the deposited FC film varies from top to bottom of the structures along the sidewall, while for structures with large pitch sizes, the conformality is significantly better as can be seen in Fig. 4(a). As mentioned earlier, this difference is supposed to be caused by the ion incoming angles and limited radical transport, which is especially significant for dense nanostructures. For advanced memory and logic devices, it is crucial to have high-quality nanostructures with small pitch sizes; thus, the conformality of the FC spacer layer has to be further improved. A possible solution is to reduce the kinetic energy of the ion flux and increase the processing pressure; thus the FC deposition process can become more isotropic for a uniform step coverage.

From the fabrication results, we can see that since a bulk silicon substrate is being used, the etch depth H_1' is larger than the height of the final structures H_3 [as illustrated in Fig. 1(a)]. For a uniform structure depth after the SADP process, an etch stop layer (e.g., silicon oxide or silicon nitride) can be deposited under the silicon device layer, while the whole process can still be performed inside the same equipment. A demonstration of this concept will not be discussed in this paper. It should also be mentioned that this technique can in principle be transferred onto other etching systems, as long as C_4F_8 gas and Bosch-like process parameters are available. However, in order to process wafers with larger sizes, it is recommended to use high volume manufacturing etching tools designed for handling larger substrates to achieve better structure uniformity across the wafer.

IV. SUMMARY AND CONCLUSIONS

In conclusion, an *in situ* SADP process has been proposed, with all fabrication steps integrated and monitored during a single procedure. By using plasma-deposited FC as a spacer layer, additional fabrication techniques (such as CVD or ALD) can be avoided, and the entire SADP process can take place inside a commercially available plasma etching equipment. The FC deposition process was studied and the quality of the FC film was characterized. The *in situ* SADP process was performed with initial patterns defined by both UV lithography and electron beam lithography, demonstrating an improvement of resolution limit and spatial frequency doubling, and a HAR nanostructure can be fabricated with good quality. Compared with standard SADP processes, this fabrication technique is remarkably simplified, easily monitored, and is not dependent on expensive facilities for high-resolution lithography and thin film depositions. Potential applications are expected for large-area patterning of high-resolution nanostructures, which is of great significance in the semiconductor industry and large-scale photonic devices.

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