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A 280-GHz Self-Mixing Balanced Frequency Tripler in SiGe BiCMOS Technology

Arsen Turhaner, Yunfeng Dong, *Member, IEEE*, Vitaliy Zhurbenko, *Member, IEEE*, and Tom Keinicke Johansen, *Member, IEEE*

***Abstract*— In this letter, a self-mixing balanced frequency tripler is presented. It comprises a push–push frequency doubling stage followed by a single balanced mixing stage sharing the input power via coupled lines. The chip is fabricated using the SG13G2 (130-nm SiGe BiCMOS) technology of Innovations for High Performance Microelectronics (IHP). A measured output power of 3 dBm is achieved at 280 GHz with a dc-to-RF efficiency of 2.19%.**

***Index Terms*— Frequency tripler, mm-wave circuits, SiGe BiCMOS, subharmonic mixer.**

I. Introduction

OVER the past few years, research on the exploitation of the terahertz gap (0.1–10 THz) for emerging applications such as short-range wideband communication, high-resolution radar and imaging, spectroscopy and material characterization has gained momentum. The inherent challenge on designing an on-chip source operating in the terahertz gap is to produce enough power as the transistor sizes are continuously scaled down to increase f_{T} and f_{max}. Therefore, especially for sources operating above 200 GHz, frequency multiplication stages are inevitable [1]. Thus, most of the reported systems operating in the terahertz gap exploit frequency multiplication [2]–[5].

In this letter, a 280 GHz frequency tripler is introduced. It is intended to be used in a signal source of an imaging system similar to the one described in [6], which provides −13 dBm of output power at 490–645 GHz. Therefore, a frequency doubler with a mediocre conversion loss below 16 dB placed after the proposed tripler is sufficient to reach a similar performance. The proposed tripler comprises a push–push frequency doubling stage and a mixing stage similar to those in [7]–[9]. It operates at a much higher frequency, hence, the power distribution also becomes an issue which is handled by coupled lines. The advantage of using the self-mixing design approach compared to the traditional frequency triplers as demonstrated in [10] is that it relies on the strength of the first- and the second-order nonlinearities instead of the third-order nonlinearity.

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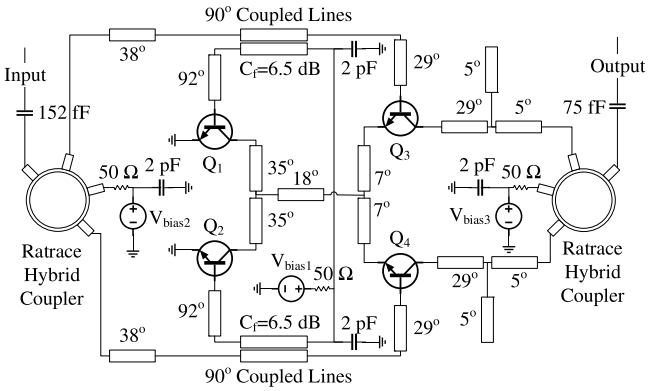

Fig. 1. Full schematic of the frequency tripler. The characteristic impedance of the transmission lines is 50 Ω and the electrical lengths are given at 93.3 GHz.

The letter is organized as follows. In Section II, the circuit design is presented. In Section III, the simulation and the measurement results are given along with the discussion. Finally, Section IV concludes the letter.

II. Circuit Design

The circuit topology is shown in Fig. 1. Transistors Q_1 and Q_2 belong to the push–push frequency doubling stage whereas Q_3 and Q_4 perform single balanced mixing. Coupled lines are used to divide the input power between these two stages. For a differential system, the ratrace hybrid couplers are not needed and the topology can be very compact.

In the proposed design, all the transistors have ten emitter fingers to increase the current driving capability. Base bias voltage is chosen for the frequency doubling stage to have a reduced angle of conduction. This boosts the second harmonic generation. The signal from the thru ports of the coupled lines must be powerful enough to commutate the current flowing in the mixing stage transistors. The elements of the matching networks are optimized considering the output power and the routing in the layout.

A. Balun Design

The balun has to have a low loss at the frequency of operation in order to reduce the RF input power level requirement and preserve the output power. Considering the design frequency, two balun structures become prominent: 1) ratrace hybrid coupler and 2) Marchand balun. Electromagnetic (EM) simulations of both structures are compared

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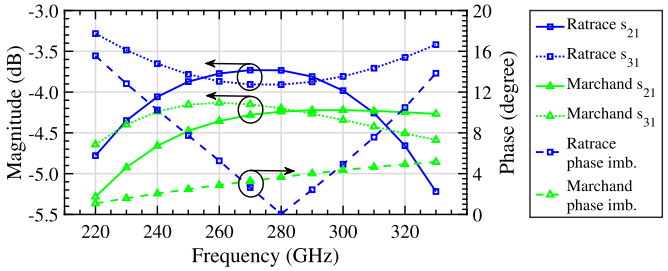

Fig. 2. Insertion loss and phase imbalance.

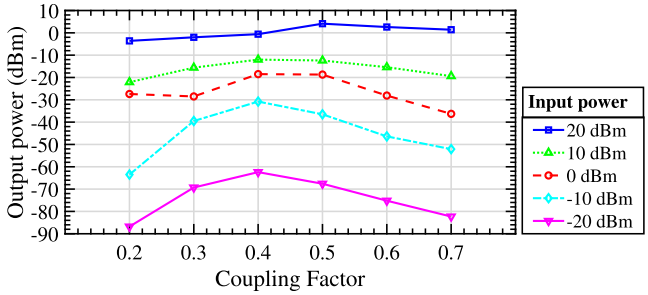

Fig. 3. Simulated output power versus the coupling factor.

across 220–330 GHz using Keysight Advanced Design System (ADS) on optimized layouts based on the layer stack of the SG13G2 technology.

The simulation results for the balun structures are given in Fig. 2. For the ratrace hybrid coupler, it can be deduced that the loss is less than 1 dB for a 20% bandwidth at around 270 GHz. The amplitude imbalance is less than 1 dB for a 30% bandwidth at around 270 GHz. The phase imbalance is quite low around the targeted center frequency of the design. For the Marchand balun, the loss is higher, however, the amplitude and the phase imbalances are quite low. The EM simulation results show that both structures are well matched for the full band with a return loss of more than 15 and 10 dB for the ratrace hybrid coupler and the Marchand balun, respectively. The output ports, however, are matched in the ratrace hybrid coupler but not in the Marchand balun. The ratrace hybrid coupler is chosen because of its low loss, good match, and sufficiently low imbalance in the frequency band of interest.

B. Optimization of the Third Harmonic Generation

Assuming the RF signal driving the mixing stage is powerful enough to commutate the collector current, the third harmonic component of the output current depends on the dc bias and the RF signal introduced to the base of the frequency doubling stage transistors, and the phase difference, ϕ, between the signals reaching the base of the frequency doubling stage transistors and the mixing stage transistors. If the electrical lengths of the interstage matching network are neglected, it can be shown that the output power is maximized when $\phi = (2k+1)\cdot 90°$, where k is an integer. The transmission line lengths are chosen to provide a phase difference of 270° at 93.3 GHz taking into account the parasitics of via interconnects and the capacitive loading of the input of the transistors.

Another important parameter is the coupling factor which affects the power division between the stages. Enhancing the coupling factor and hence, increasing the RF input power introduced to the frequency doubling stage, improves the output power as long as there is enough power to drive the mixing stage. This relation can also be seen in Fig. 3. For the figure, the base bias voltages are optimized for a coupling factor of 0.45 and otherwise kept fixed. As is seen, as the input power increases, a higher coupling factor is favored.

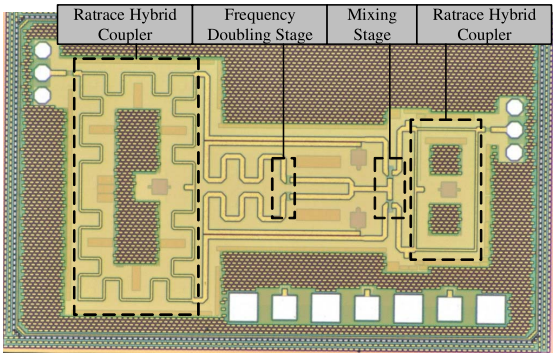

Fig. 4. Chip photograph of the frequency tripler with the indicated building blocks. The chip size is 0.8 × 1.3 mm^2.

III. Measurement Results

The fabricated chip is measured on-wafer using 50-μm pitch Picoprobes from GGB Industries in a ground-signal-ground (GSG) configuration. In order to generate the input signal, a customized source is used with an adjustable attenuator. This is a narrowband source (92–96 GHz) with a high output power [11]. For the full band measurements, an AFM6-110, ×6 frequency multiplier, and a W-MPA power amplifier both from Radiometer Physics GmbH are driven from an Anritsu MG3694A signal generator. The W-MPA has a lower output power than the customized source has. On the receiver side, a PM5 Erickson power meter from Virginia Diodes, Inc., (VDI) is used. In order to verify the results and measure the suppression of the unwanted harmonics, measurements are repeated using harmonic mixers (11970W model from Keysight, M05HWD and M03HWD models from OML with DPL26 diplexer). The sources are calibrated using the power meter. Sufficient time is allowed for the power meter to settle for each measurement. For the full band measurement, the source with the ×6 frequency multiplier and the W-MPA is also calibrated using the 11970W harmonic mixer for verification. The photograph of the chip is shown in Fig. 4. The chip size is 0.8 × 1.3 mm^2.

The first experiment is to characterize the behavior of the output power at the center frequency of 280 GHz with respect to V_{bias1} (refer to Fig. 1). For this purpose, the narrowband customized source is used [11]. The V_{bias2} is optimized for each measurement and the collector voltage is kept constant at 3.2 V. The results of the characterization is given in Fig. 5 in which the input power level is incrementally increased. The collector current depends on the RF input power level and the V_{bias1}. When the V_{bias1} is less than 0.5 V with an RF input power of less than 13 dBm, the dc current is below 1 mA. It increases to approximately 15 mA when more than 15 dBm of RF input power is used with a dc bias of more than 0.75 V. It can be concluded from Fig. 5 that for the low input power, the curves have a class B operation characteristic, and as the input power increases, they show the characteristic of an over-driven class A operation for the frequency doubling stage. In this highly nonlinear mode of operation, the output power is boosted by the harmonic generation.

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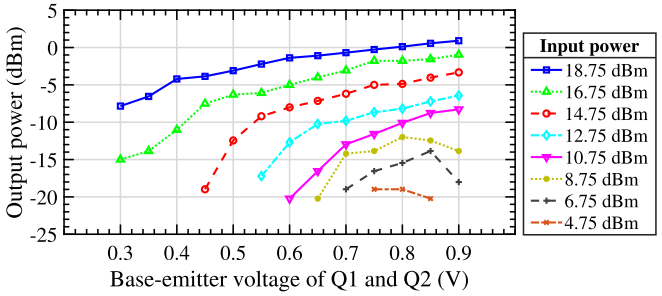

Fig. 5. Measured output power versus the base–emitter voltage of the transistors Q_1 and Q_2 for incrementally increased input power levels.

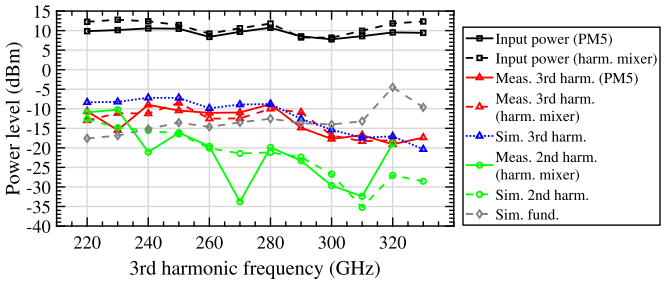

Fig. 6. Full band measurement of the output power and its comparison to the simulation results.

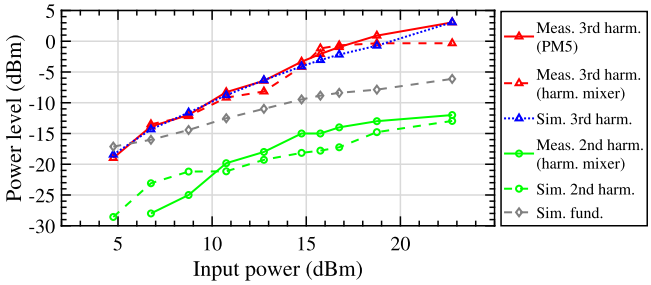

Fig. 7. Measured output power and its comparison to the simulation results at 280 GHz.

The second experiment is to characterize the behavior of the output power for the full band (220–330 GHz). For this purpose, the source with the ×6 frequency multiplier and the W-MPA is used. Base biases are adjusted to maximize the output power at each frequency. The collector voltage is kept constant at 3.2 V. The results are given in Fig. 6. The PM5 data agrees well with the harmonic mixer data. In general, a good agreement between the simulations and measurements is observed. Discrepancies between the measured second harmonic and the simulation are probably due to having a mismatch at the second and the third harmonics during the measurements with the M05HWD harmonic mixer and a 140–220 GHz probe. Minimum 10 dB of a second harmonic suppression is obtained around the frequency of interest. Due to the lack of a second *W*-band probe, the fundamental signal suppression could not be measured, therefore, simulation results are given instead. As the fundamental signal is also a product of mixing, it appears in the spectrum. However, it is far away from the third harmonic; thus, it can be easily suppressed by an external filter. In addition, as the input power increases, the fundamental signal suppression improves as it is seen in the following experiment.

The third experiment is conducted to obtain the saturated output power at 280 GHz. The results are given in Fig. 7.

TABLE I

PERFORMANCE COMPARISON TO THE STATE-OF-THE-ART

Technology	Freq. (GHz)	Topology	$P_{out,peak}$ (dBm)	P_{DC} (mW)	η_{dc}*	P_{in} (dBm)	Ref #
130 nm SiGe BiCMOS	325	Amp. + Doubler	-3	420	0.12%	-7	[12]
130 nm SiGe BiCMOS	220	Amp. + Doubler	-1	630	0.13%	0	[12]
90 nm SiGe BiCMOS	215	Amp. + 4-Way Comb. Doublers	8	2700	0.23%	12.7	[13]
130 nm SiGe BiCMOS	204	2-Way PA + Doubler	6.5	394	1.13%	2	[14]
55 nm SiGe BiCMOS	240	VCO + Amp. + Doubler w/Divider	7.2	386	1.36%	-	[15]
130 nm SiGe BiCMOS	284	x4 + PA	2.5	384	0.46%	0	[16]
130 nm SiGe BiCMOS	270	Amp. + Doubler	-0.5	429	0.21%	-14	[17]
130 nm SiGe BiCMOS	235	x8 + Amp. + 4-Way PA	13.5**	990	2.30%**	-6	[18]
130 nm SiGe BiCMOS	280	Tripler	3	91.2	2.19%	22.75	This work

* dc-to-RF efficiency as defined in [10]
** With de-embedding input and output baluns and pads

For this measurement, the narrowband customized source is used again [11]. Base biases are adjusted to maximize the third harmonic power at each input power level. The results are not compensated for any ratrace hybrid coupler and RF pad loss. The graph shows good agreement between the simulation and the PM5 measurement of the third harmonic output power. The harmonic mixer data also agrees well with the PM5 data for the input power levels of less than 17 dBm. Due to the lack of an attenuator at 280 GHz, the harmonic mixer goes into compression and does not give reliable results in the range of highest output powers. The output power of 3 dBm is achieved with a dc power consumption of only 91.2 mW measured under continuous wave (CW) operation. This translates into a dc-to-RF efficiency of 2.19%. In order to reach this value, the collector voltage is pushed up to 3.8 V with a collector current of 24 mA. It is also seen in Fig. 7 that the fundamental signal suppression and the second harmonic suppression of 9 and 15 dB are achieved, respectively, when sufficient input power is used.

The comparison of this work to the state-of-the-art for SiGe BiCMOS based designs from the literature is given in Table I. This work has the simplest topology, and hence, the lowest dc power consumption, and one of the highest dc-to-RF efficiencies. In addition, the measured peak power of 3 dBm is competitive considering the frequency of operation. The required input power is high, but this is due to being a topology demonstration without any preamplification.

IV. CONCLUSION

A frequency tripler with a novel topology is demonstrated. The measured output power of 3 dBm is the state-of-the-art at this frequency for active SiGe BiCMOS-based on-chip sources. The topology enables a differential design with a compact layout and achieves a high dc-to-RF efficiency.

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