Doping Technologies for Lateral Junctions in Photonic Crystal Membranes

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Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

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Doping Technologies for Lateral Junctions in Photonic Crystal Membranes

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PhD Thesis

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April 2020

Abstract

Development of optical short-range data interconnects for photonic network-on-chip applications brings the prospect of overcoming the problems related to power consumption and transmission speed of electrical counterparts. Photonic crystals constitute a highly flexible platform with rich physical phenomena, which allow miniaturization and tight integration of a wide range of devices. The focus of this work is on indium phosphide (InP) photonic crystal membranes bonded to silicon (Si) for the realization of lasers and all-optical switches based on Fano resonance. The important component is a lateral p-i-n junction in InP membrane, which is required for electrical pumping of the lasers, as well as for carrier sweep-out from the Fano switches. For this purpose, doping technologies for InP have been investigated.

The main part of this work has been dedicated to the extensive development and optimization of the fabrication procedure for the experimental realization of lasers and Fano switches with the lateral p-i-n junction. Various fabrication issues and the ways to solve them are described. Direct bonding of InP to Si substrate is implemented to take advantage of mature silicon industry. For n-type doping, silicon ion implantation is investigated. Optimal ion energy, dose and activation temperature are investigated, with the consideration of the effect on active material properties. The possible drawback of undesired overall p-doping and the way to avoid it are addressed. For p-type doping, zinc thermal diffusion is analyzed. A thorough study of various diffusion parameters affecting the electrical properties of p-InP is presented. The problem of diffusion-induced surface deterioration in special cases is identified and solved. Lateral redistribution for both silicon and zinc is characterized.

Light emission under electrical injection has been observed, however, no lasing has been achieved due to fabrication obstacles. In the case of Fano switches, wavelength conversion has been successfully performed, with a hint on the possibility of enhancement of modulation bandwidth due to carrier sweep-out from the Fano cavity. Future opportunities for devices performance improvement are discussed.

Resumé (in Danish)

Udvikling af optiske kort-distance data forbindelser til andvende i fotoniske network-on-chip løsninger har udsigt til at overkomme udfodringerne som er forbundet til energi forbrug og transmissions hastighed af elektriske komponenter. Fotoniske krystaler udgøre og fleksibel platform med bred vift af fysiske fænomener, hvilket baner vej for at mindske størrelsen og tæt integration af stort udvalg af componenter. Fokus med denne arbejde er at gøre brug af indiumphosphid (InP) fotoniske krystal membraner bundet til silicium (Si) for a realisere laser og optiske omskifter baseret på Fano resonans. Den vigtigt komponent er lateral p-i-n overgang i InP membran, som er påkrævet for elektrisk stimulering af laser og samtidligt at udvandre ladninger fra Fano omskifter. Til denne formål doping teknologier for InP er blevet undersøgt.

Hoved fokus ved dette arbejde har været dedikeret til intensiv udvikling og optimering af fabrikations fremgangsmåder til opnåelse af Fano omskifter med lateral p-i-n overgang. Flere vanskeligheder i forbindelse med fabrikation og løsninger til disse er beskrevet. Direkte bonding af InP til Si substrat er implementeret og på denne måde gøre man fordelsagtigt brug af processer fra moden silicium industri. For n-type doping silicium ion implantation er undsøgt. Den optimale ion energi, dose og aktiverings temperatur er undersøgt, med betragtning af indflydelse på egenskaber af den aktive materiale. De mulige ulemper af uønsket global p-doping og hvordan man ungår dette er undersøgt. For p-type doping thermisk diffusion af zink undersøgt. En grundig undersøgelse af diffusions parameter og dens påvirkning på elektriske parameter af p-InP er presenteret. Problemet vedrørende diffusion-induceret overflade forringelse ved specifike tilfælder er identificeret og løst. Den laterale omfordeling for både silicium og zink er karakteriseret.

Lys emission under elektrisk stimulering er blevet observeret, dog var det ikke muligt at opnår lasing effekt på grund af fabrikations forhindringer. I tilfæde af Fano omskifter, konventering af bølgelængde er blevet successful opnået, med en hint af mulighed for forøgelse af båndbredde modulation på grund af udvandre ladninger fra Fano kavitet. Fremtidlige muligheder for forbedring komponenternes ydeevne er diskuteret.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy (PhD) from the Technical University of Denmark (DTU). The project has been carried out in the Nanophotonic Devices group at the Department of Photonics Engineering (DTU Fotonik) in the period from October 2016 to April 2020 under the supervision of Professor Kresten Yvind and Professor Jesper Mørk. The project has been a part of the research activities in the NAnophotonics for TErabit Communications (NATEC) center of excellence, which is financially supported by the Villum Fonden.

Acknowledgements

First and foremost, I am extremely grateful to my main supervisor Kresten Yvind for his knowledge, support and guidance throughout my entire PhD project. He was a constant source of professional expertise, wisdom and fresh ideas. I would also like to express my gratitude to my co-supervisor Jesper Mørk for his support and encouragement.

I greatly appreciate the opportunity to work together with my fellow colleagues Aurimas Sakanas, Dagmawi A. Bekele, Evangelos Dimopoulos, Kristoffer S. Mathiesen, Meng Xiong and Quentin Saudan within the framework of NATEC HERO project and beyond. Their invaluable contributions and shared ideas were indispensable for me.

My sincere thanks also goes to Luisa Ottaviano for introducing me to the cleanroom fabrication and guiding me at the initial stages of this project.

I would also like to thank Elizaveta Semenova, who, together with Kresten, was always ready to help me to solve the arising problems with the MOVPE system.

Many thanks to all Nanophotonic Devices group members for a great work environment and fruitful discussions.

My special thanks to all DTU Nanolab staff for their expertise, help and support in the cleanroom, especially Elena Khomtchenko, Evgeniy Shkondin, Jesper Hanberg, Conny Hjort, Thomas A. Anhøj, Karen Birkelund and Berit Herstrøm.

I had a great pleasure of having interesting discussions with Maksim Zalkovskij. I also want to thank him for help with translating the thesis abstract into Danish.

Last but not least, I would like to express my deepest gratitude to my wife Polina for all the love, patience and support in this challenging time.

Contents

Chapter 1

Introduction

1.1 Motivation

Nowadays information and communications technology (ICT) has become the integral part of our lives. Newly emerging areas, such as artificial intelligence, internet of things, cryptocurrency mining, are rapidly developing. Global Internet traffic continues to grow exponentially, with video streaming services contributing most. Especially large pressure is exerted on telecommunications network during extraordinary events, for example, nationwide quarantine due to the recent COVID-19 pandemic. Increase in required communication bandwidth capacity leads to large power consumption, which has already risen to environmentally significant level. It is estimated that in 2015 ICT sector was responsible for 3.6% of global electricity consumption and 1.4% of global CO_2 emissions [1], with forecasted numbers drastically rising to 51% for electricity and 23% for carbon footprint in 2030 in worst case scenario [2], although some skepticism has been expressed about the severity of this rise [1].

In the recent years, the structure of ICT sector energy consumption has been changing, with data centers electricity usage becoming significantly more important compared to personal devices consumption [3]. According to one estimate, each bit transmitted through Internet may cause $\sim 10^6$ bits communicated at all the link levels inside the data centers [4]. To make things worse, large energy consumption leads to the problem of heat dissipation. Facility cooling can amount for as much as half of total data center energy consumption [5]. Optimization of power management [6] and combining small data centers in hyperscale facilities [7] can lead to significant reduction of accompanying energy consumption, however, it cannot solve the inherent problem of energy losses related to data computation and communication on chip-to-chip and even on-chip levels.

With technology development and drastic downsizing of transistors, energy required for logical operation per bit was greatly reduced [8]. Unfortunately, the

reduction pace could not be kept up by the energy used to send data. This results in the situation where most of the energy is spent to communicate data inside electronic machine, not to compute it [9]. As a consequence, with the current level of electronic integrated circuit miniaturization, the limiting factor in further progress is the problem of heat dissipation.

Currently implemented short-range electrical interconnects suffer from significant energy consumption mostly because of large energy amount required to charge and discharge electrical wires during high frequency data transmission [10]. Potential attempts to reduce this energy are hindered by unavailability to decrease capacitance of wires while keeping the required large density of interconnects. A lot of attention is brought to the idea of replacing short-range electrical interconnects with optical ones, with the main advantage being the possibility for power consumption decrease. Other benefits include higher possible density of high-bandwidth connections, reduction of data distortion and precise signal timing [11].

1.2 Optical interconnects

Optical interconnect can be divided into three basic parts: transmitter, communication channel and receiver. In transmitter, information is converted from electrical to optical domain by either direct modulation of light source or by using constant light source output and external modulator. Communication channel is a low-loss optical waveguide which guides the light. Repeaters or amplifiers can be used to reinforce the signal, if it is significantly attenuated. The role of receiver is to convert the signal back from optical to electrical domain.

1.2.1 Evolution of optical interconnects

The rise of optical interconnects in data communication began in 1970s in long-distance range. At this time, the very first continuous wave (CW) semiconductor lasers operating at room temperature (RT) were experimentally demonstrated [12], which proved to become the required for data communication compact and efficient light sources, which output could be modulated to encode the information. At the same time, a lot of effort was put to minimize the losses of optical fibers. It was suggested that the optical losses of silica glass fibers could be significantly reduced by increasing the glass purity [13]. Further optimization of chemical glass composition, namely, doping of silica fiber core by germanium instead of titanium, allowed to achieve record low optical losses of 0.2 dB/km at 1.55 µm wavelength [14], which are close to the fundamental limit imposed by Rayleigh scattering.

The first generation of commercial optical communication employed light with 850 nm wavelength emitted by available at that moment GaAs lasers. Optical signal was then transmitted in graded-index multimode silica glass fibers and converted to electrical domain by silicon photodetectors. Even though signal losses were sig-

nificantly reduced compared to electrical coaxial cables, they were still high for silica fibers (∼3 dB/km) due to operation in near-infrared wavelength range [15]. The solution was to shift operation to longer wavelengths, where silica fibers exhibit lower losses. For that purpose new InP-based platform was developed, with InGaAsP lasers emitting at 1.3 µm [16]. The main benefit of 1.3 um wavelength is near zero chromatic dispersion in silica fibers [17]. This allowed for significant reduction of required number of signal repeaters with the same transmission distance. In push for higher bit rates, the problem arose of bit rate being limited at ∼100 Mbit/s due to modal dispersion in utilized multimode fibers. The limitation was circumvented by implementation of single-mode fibers instead of multimode ones [18].

However, even at 1.3 µm optical losses in silica fibers are still substantial. Minimum optical losses are observed at 1.55 µm wavelength (C-band), which would later become the golden standard for telecommunications. The drawback of using this wavelength is relatively large chromatic dispersion. Since the initial Fabry-Perot semiconductor lasers exhibited multiple longitudinal modes, high bit rates were not achievable due to large pulse broadening caused by different propagation velocities of different modes in the fiber. This required the development of new laser designs, namely, distributed Bragg reflector (DBR) and distributed feedback (DFB) lasers, which emit single longitudinal mode. The other approach was to reduce fiber dispersion by engineering refractive index profile of fiber core, which resulted in realization of dispersion-shifted fibers [19].

Drastic increase of information transmitted in single optical fiber is possible by implementation of various multiplexing techniques, with wavelength-division multiplexing (WDM) being the most important one. The idea behind it is to simultaneously transmit several signals from transmitters operating at slightly different frequencies. Individual channels are then combined before and separated after transmission by means of optical multiplexer and demultiplexer, respectively. The number of channels can be several hundreds, with total data bit rate exceeding 10 Tbit/s [20].

Optical time-division multiplexing (OTDM) is another promising technique, when different channels are combined in time domain [21]. Additional possibility for multiplexing is using two orthogonal polarization states (polarization-division multiplexing) [22]. Furthermore, by utilization of coherent detection scheme, measurement of both the amplitude and phase of an optical signal becomes possible, which gives the opportunity to encode information in not just wave amplitude, like in other schemes, but also in phase. This gives rise to such advanced modulation formats as, for example, quadrature amplitude modulation (QAM), when each symbol (specific value of amplitude and phase) corresponds to multiple transmitted bits [23]. Further possibilities for multiplexing include using multicore or multimode fiber for parallel transmission of bit streams in different cores or modes (space-division multiplexing, SDM) [24], and utilization of orbital angular momen-

tum (OAM) modes [25].

As a result, C-band optical links completely eclipsed electrical ones in long-distance data communication due to high bandwidth and low losses, required to efficiently transmit information over thousands of kilometers. However, the process of optics substituting electronics was not as fast in short-distance range. The reason for that is relative insignificance of low losses benefit due to small signal attenuation over short distances and lower cost of electrical wires. However, following the development of vertical-cavity surface-emitting laser (VCSEL) design and demand for high data rates, GaAs-based VCSELs operating at 850 nm with light coupled in multimode fibers became widespread high speed optical interconnects within data centers with typical link length being tens of meters [26]. Benefits of VCSELs include low fabrication cost due to possibility of wafer-level testing and creating 2D arrays, low assembly cost due to light emission in direction normal to surface and utilization of wide multimode fibers, high thermal stability and small power consumption [27]. Further optics advancement in even smaller distance range, namely, chip-to-chip and on-chip, is currently under development, with the main critical issues being low energy consumption and low cost, discussed in the following subsections.

1.2.2 Energy consumption

When we consider energy consumption of short-range optical interconnect, various components must be taken into account, including transmitter, receiver, some circuit functions, such as clocking and clock recovery. It is considered that the most challenging task is to reduce the power consumption of the transmitter, which converts electrical signals to optical ones (E/O converter). The generally recognized targets for energy per bit consumption of E/O converter in very short-range optical interconnects are 10–20 fJ/bit for chip-to-chip links and 2–10 fJ/bit for on-chip communication [10].

A lot of attention is brought to directly modulated laser (DML) as a light source in short-range optical communications, since it allows to avoid additional complexity and power consumption associated with integration of external modulator. In DML, conversion of electrical signal to optical one occurs by direct modulation of injected current. If I_{bias} and V_{bias} are bias current and bias voltage, respectively, energy cost required to transmit one bit is determined by

$$\text{Energy cost} = \frac{I_{\text{bias}} V_{\text{bias}}}{\text{BR}}\,, \tag{1.1}$$

where BR is data bit rate. As can be seen, energy cost reduction can be achieved by decreasing bias current for the same bit rate. Of course, it would also result in reduced output power, but high output power is not required for short-range optical links.

Maximum modulation bandwidth of DML is proportional to relaxation oscillation frequency f_r, which is given by

$$f_\mathrm{r} = \frac{1}{2\pi}\sqrt{\frac{\Gamma v_\mathrm{g}}{q}\frac{dg}{dN}\eta_\mathrm{i}\frac{I_\mathrm{bias}-I_\mathrm{th}}{V_\mathrm{a}}}\,, \tag{1.2}$$

where Γ is optical confinement factor, v_g is group velocity, q is elementary charge, $\frac{dg}{dN}$ is differential gain, η_i is internal quantum efficiency, I_th is threshold current and V_a is active volume [28]. If we decrease bias current, in order to maintain high bit rate, threshold current and active volume should also be decreased, which essentially means maintaining bias current and threshold current densities at the same level while decreasing active volume. Thus, reduction of laser active volume (by reducing cavity length) is crucial for achieving low energy consumption per bit [29]. Enhancing optical confinement also has influence on increasing modulation bandwidth.

When we reduce active volume by decreasing cavity length, the problem of maintaining enough gain for lasing arises. Threshold gain g_th is inversely proportional to photon lifetime τ_p and, as a consequence, cavity quality factor Q, as indicated by

$$\Gamma v_\mathrm{g} g_\mathrm{th} = \frac{1}{\tau_\mathrm{p}} = \frac{\omega}{Q}\,, \tag{1.3}$$

where ω is angular frequency. Since Q-factor decreases with reduced cavity length, special attention should be put to mirror reflectivities, which should be significantly increased in order to achieve high Q-factor values. However, photon lifetime in the cavity should not be too large in order to allow high speed modulation. Trade-off between high gain and high speed operation puts desired total cavity Q-factor value in 10^3–10^4 range [30]. At the same time, it can be seen that high optical confinement Γ is also important factor in threshold gain reduction.

Conventional in-plane DFB lasers typically have 100–200 µm long cavity and consume energy on the order of several picojoules per bit [31, 32], which is unacceptable for low power short-range optical links. However, significant enhancement of optical confinement can be achieved by implementation of InP-based membrane structure on SiO_2/Si substrate due to large difference between InP and SiO_2 refractive indices. Fabricated buried heterostructure (BH) lasers with DFB middle section and DBR mirrors, so called distributed reflector (DR) lasers, have short cavity length (down to 20 µm) and exhibit much lower power consumption compared with standard DFB lasers, with energy per bit being on the order of hundreds of femtojoules [33–35], with record value being 97 fJ/bit for 25.8 Gbit/s modulation with 75 µm long cavity [36]. However, with reduction of cavity length down from 75 µm, further decrease of energy consumption could not be achieved due to increase in grating loss [37]. Since obtained energy per bit values are many times

higher than target ∼10 fJ/bit with no foreseeable way for improvement, other laser designs should be considered.

Completely different approach is possible with VCSELs, which exhibit greatly reduced active volume compared to DFB lasers due to principally different geometry and much smaller length of vertical cavity. Reduction of active volume is achieved by decreasing the size of oxide aperture, e.g., active area. Short wavelength (850–1060 nm) VCSELs with total energy consumption on the order of ∼100 fJ/bit have been demonstrated [38–40], with record value of 77 fJ/bit for at 25 Gbit/s error-free transmission (defined by bit error rate (BER) being less than 1×10^{-12}) [41].[1] Furthermore, excellent high modulation speed of 50 Gbit/s can be achieved without drastic compromising of energy per bit (∼100 fJ/bit) [43]. Long wavelength (1.5 µm) low power VCSELs have also been demonstrated, with energy consumption in 100–200 fJ/bit range [44]. However, achieved power consumption values are still far from the target (∼10 fJ/bit). Unfortunately, further decrease of VCSELs power consumption by active area reduction is hindered by the difficulty of further oxide aperture size reduction from already very small 2–3 µm values, while maintaining devices high yield and high reliability.

Potential candidates for application in ultrashort-range optical communications could be lasers based on microring and microdisk structures, in which whispering-gallery modes circulate along the edge of the structure. There are experimental demonstrations of electrically pumped lasers with microring [45] and microdisk [46, 47] structures. However, reduction of structure size leads to significant quality factor degradation due to increasing bending and scattering losses, as well as electrical resistance increase. Heat dissipation from the structure is also an issue. Thus, in recent times interest to such laser designs for very short-range optical communications has faded away.

The most promising type of structure for realization of ultrasmall wavelength-scale cavities with high Q-factor is photonic crystal (PhC) structure, discussed in Section 2.3. Cavities can be formed in 1D and 2D PhCs, however, 2D PhC slab[2] is the most common type [48]. PhC structure for laser applications is usually formed in air suspended InP membrane to benefit from large refractive index difference between InP and air in order to achieve high Q-factor. However, such design brings the problem of large local temperature rise due to non-efficient heat dissipation, which makes RT CW operation, required for any realistic application, difficult. Implementation of active region in buried heterostructure (BH) embedded in PhC cavity for carrier and optical confinement, as well as for efficient heat dissipation,

[1] To avoid confusion, it should be clarified that there are two figures of merit for DML energy consumption: total energy per bit, defined as $P_{\mathrm{tot}}/\mathrm{BR}$, and dissipated energy per bit, defined as $(P_{\mathrm{tot}} - P_{\mathrm{opt}})/\mathrm{BR}$, where P_{tot} and P_{opt} are total consumed electrical power and optical output power, respectively, and BR is bit rate [42]. In this work total energy per bit is used, as given by Eq. (1.1), however, in VCSEL community dissipated energy per bit definition is more common.

[2] For the sake of simplicity, in the following text PhC will refer to 2D PhC, if not mentioned otherwise.

resulted in the development of lambda-scale embedded active region photonic crystal (LEAP) laser [49]. The first demonstrations confirmed the potential of PhC lasers, resulting in signal modulation at room temperature with remarkably low estimated energy consumption of 13 fJ/bit [50], which was further decreased down to 8.76 fJ/bit [51]. However, these results were obtained with optical pumping. Incorporation of lateral p-i-n junction allowed to achieve lasing under electrical injection [52], with energy consumption going from 14 fJ/bit [53] down to remarkably low 4.4 fJ/bit at 10 Gbit/s modulation [54], which was achieved by introduction of current-blocking trenches in PhC design. However, output optical power was low (2.17 µW) with wall-plug efficiency less than 5%. Consequently, either implementation of forward error correction (FEC) or development of ultrasensitive photodetectors is required in order to utilize such small optical power. Nanolasers with exceptionally low ∼1 fJ/bit energy consumption were demonstrated by reduction of PhC cavity length to sub-µm level [55], but output power was even more decreased. Nevertheless, PhC lasers have been proved to be the promising solution for ultrashort optical links due to the possibility to achieve very low power consumption in the required target limits [10].

1.2.3 On-chip integration

Apart from energy consumption, fabrication and assembly cost is also of great importance. Currently utilized electrical copper wires are extremely easy and inexpensive to fabricate, therefore, optical interconnects must be greatly improved in terms of cost with simultaneous significant performance benefits in order to become commercially viable. It is widely recognized that implementation of photonic integrated circuit (PIC) design for network-on-chip application is the future of ultrashort-range optical interconnects [56], since assembly cost is greatly diminished by eliminating the need to discretely package and assemble separate devices. In PIC, all optical components, namely, lasers, waveguides, photodetectors, (de)multiplexers, all-optical switches, would be integrated on one chip, which would require very small footprint and high operation efficiency of all components.

Photonic integrated circuits can be developed based on various platforms, which include, for instance, InP [57], InP membrane on silicon (IMOS) [58], GaAs [59], $LiNbO_3$ on insulator (LNOI) [60]. However, PICs based on silicon-on-insulator (SOI) [61] and to a lesser extent SiN_x [62] and polysilicon [63] are the most popular choices because they take advantage of rapidly developing Si photonics technology, which is projected to be the fastest growing segment of optical communications market [64]. The main motivation behind silicon photonics lies in the possibility to exploit the benefits of mature complementary metal-oxide semiconductor (CMOS) technology, which brings the well-established processing, large wafer sizes and volume throughput to photonic components, greatly reducing fabrication cost. The drawback of using silicon is the difficulty to achieve high efficiency of Si-based light sources due to Si being indirect band gap semiconductor. Therefore, the common

approach is a heterogeneous integration of active materials (mostly III-V) on silicon platform [65].

In order to be able to integrate light source in on-chip PIC, in-plane emission is essential to provide easy coupling to other devices on the same chip. This means that conventional vertically emitting VCSELs should not be considered for on-chip communications, since introduction of fiber coupling would drastically increase assembly cost. However, GaAs-based electrically pumped hybrid silicon-integrated vertical-cavity laser (VCL) with in-plane light coupling achieved by introduction of weak diffraction grating inside the cavity has been demonstrated [66]. Since operation wavelength is 850 nm, this approach is not suitable for Si waveguides due to Si absorbing below 1.1 µm, but SiN_x platform could be used instead. Long wavelength VCL integrated with Si waveguide on SOI platform has also been demonstrated under optical pumping [67]. In this case lateral coupling is achieved due to incorporation of high-contrast grating (HCG) as bottom mirror. However, electrical pumping of such devices remains a challenge.

In-plane electrically pumped long wavelength InP-based LEAP lasers, which were previously described as holding the energy consumption record on InP substrate [54], were also demonstrated in InP membrane bonded to Si substrate [68]. Later, integration of LEAP laser with Si waveguide on SOI platform was also achieved [69, 70], which brings evidence of large potential of such design. However, quite low output power, estimated to be 3–4 µW, has to be increased. Improvement of doping technologies for fabrication of lateral p-i-n junction in InP membrane can facilitate more efficient current injection and larger output power.

In other approach, RT CW operation under electrical injection was achieved in 1D PhC cavity in InP nanorib coupled to Si waveguide on SOI substrate [71]. Near 100 µW optical output power was demonstrated, which is much higher compared to LEAP laser, but dynamic modulation was not shown. The drawback of such design is large structure capacitance, which could seriously limit modulation bandwidth.

Ideally, lasers designed for ultrashort-range optical interconnects should be compatible with WDM technique in order to have the potential to provide increased network capacity in limited space. On-chip PhC lasers are good candidates for that since lasing wavelength can be adjusted by changing PhC lattice constant [72].

1.2.4 All-optical signal processing

Apart from the development of light sources for on-chip integration in PIC, significant attention is brought to the idea of performing all-optical data processing on-chip. Normally, in order to undergo data processing, optical signal has to be converted from optical domain to electrical and back to optical, which adds complexity, power consumption and latency to the system. Consequently, large benefits can be expected if we avoid O/E/O conversion by implementing all-optical switches [73]. However, it should be noted that photonics is not expected to fully substitute electronics in data processing, since electronics is very advanced in performing

accurate complex computations with buffer and memory. Photonics can be used where simple, but high speed data manipulation is required.

The basic operating principle of all-optical switches is utilization of nonlinear optical effects, which originate from the various interactions of the optical field with electrons and phonons in host material [74]. Key applications can be enabled, such as wavelength conversion, signal multiplexing, demultiplexing, multicasting, regeneration, which are required for the handling of high capacity signal modulated with different techniques [73]. In order to achieve the efficient devices with low power consumption and small footprint for on-chip integration, optical cavities are widely used due to the enhancement of light-matter interaction, with PhC nanocavities being especially interesting due to squeezing the optical field into a very small mode volume [75]. Furthermore, PhC platform allows the realization of structures exhibiting asymmetric Fano resonance, which can be exploited to enable new all-optical signal processing functionalities [76].

1.3 Thesis outline

The main goal of this work is fabrication and characterization of novel nanophotonic structures with electrical control with potential application in ultrashort-range optical communications. Two principal investigated device types are electrically pumped PhC nanolasers and all-optical PhC switches based on Fano resonance. The developed platform is InP membrane heterogeneously integrated with Si substrate, which allows to combine unique properties of III-V material with the benefits of large scale Si industry. A crucial device component in focus of this work is lateral p-i-n junction in the InP membrane, which is required for electrical pumping of the PhC nanolasers, as well as for enhancement of modulation bandwidth of the Fano switches by means of carrier sweep-out from the Fano nanocavity.

In order to realize the designed devices, the fabrication processing had to be extensively developed and optimized. The most attention was brought to doping technologies for InP for realization of lateral p-i-n junction, since post-growth doping of III-V materials is much less mature compared to Si technology.

Significant effort was put to collaborative NATEC HERO project within the framework of NATEC II Center of Excellence. Vast amount of different device types based on PhC nanolasers and Fano switches was designed and fabricated, however, characterization of the first samples was largely hindered by various unfortunate processing issues.

The structure of the thesis is comprised as follows:

Chapter 2 provides the essential theoretical background, describing the different aspects of the investigated InP-on-Si platform with the focus on laser applications. The possible methods of InP integration on Si are described, and the arguments for the Al_2O_3-assisted direct bonding are given. The concept of 2D PhC membrane is introduced, the opportunities which arise are discussed, with the focus

on efficient compact PhC lasers. The requirement of electrical pumping and the linked challenges are explained. Vertical and lateral current injection geometries are discussed, with the arguments provided for the choice of the lateral one.

Chapter 3 describes the possibilities for realization of lateral p-i-n junction in InP. The literature review of the technologies for selective area InP doping is given. Silicon ion implantation is singled out as a method for n-type InP doping, while zinc thermal diffusion is chosen for p-type InP doping. The existing reports on the doping mechanism and technology are summarized for both n- and p-type doping.

Chapter 4 focuses on the development of the fabrication process flow for the experimental realization of electrically pumped BH PhC lasers and Fano all-optical switches with carrier sweep-out. The designed device configurations are outlined. The brief summary of the whole processing sequence is followed by the elaborate description of the optimized fabrication stages. The encountered challenges and the implemented solutions are presented. In addition, electrical characterization methods are described.

Chapter 5 is dedicated to the extensive experimental investigation of Si ion implantation and Zn thermal diffusion technologies for the fabrication of lateral p-i-n junction in InP membrane bonded to Si. Various aspects affecting Si ion implantation and subsequent processing are studied, with their effect on the properties of n-InP and the surrounding material. The required trade-offs are discussed. Thorough Zn diffusion process investigation is presented, with an emphasis on electrical properties and possible Zn-induced material degradation.

Chapter 6 presents the electrical characterization of the fabricated p-i-n junctions in InP membrane, as well as the optical characterization of the fabricated BH PhC devices. Light emission is demonstrated, however, lack of lasing is noted. The reasons for not achieved lasing and the way to improve the performance are discussed.

Chapter 7 gives a short theoretical introduction of a Fano resonance in PhC structures and its application for all-optical switching. The prospect of enhancement of all-optical switching speed is outlined. The fabricated Fano switch with lateral p-i-n junction is described. Wavelength conversion experiment is discussed. A noticeable effect of carrier sweep-out from the Fano cavity under applied to p-i-n junction reverse bias is demonstrated.

Chapter 8 summarizes the main results of this work and gives an outlook on future perspectives.

In addition, *Appendix A* includes the technical details of each fabrication step implemented in NATEC HERO processing.

Chapter 2

Theoretical background on lasers

In this chapter, the rationale behind choosing the object of investigation will be given.

2.1 Material choice

2.1.1 Platform

As already discussed in Subsection 1.2.3, future short-range optical interconnects will most probably be based on a Si photonics platform due to leveraging the well-established CMOS silicon industry, which provides the possibility of large scale high yield low cost production. Nowadays most of the main components of Si photonics circuitry, such as low loss waveguides, high speed modulators and photodetectors, are advanced enough to start being commercialized [64]. However, the main challenge of Si photonics is the difficulty to achieve efficient light generation in Si-compatible material. As shown in Fig. 2.1(a), silicon is indirect bandgap semiconductor, which means that the majority of electrons and holes have different crystal momentum. Since photon momentum is negligible, in order to satisfy the condition of momentum conservation, radiative recombination is only possible via interaction with a third particle, namely, phonon. This process is inherently slow. At the same time, non-radiative processes, such as recombination at bulk and surface defects, free carrier absorption and Auger recombination, are much more likely to occur, especially under high injected carrier density, required for laser operation. This results in extremely poor internal quantum efficiency of light emission, which is typically of the order of 10^{-6} for Si [77]. On the contrary, radiative recombination is the dominating process in case of direct bandgap semiconductors, as shown in Fig. 2.1(b). For this reason, such materials, as direct bandgap III-V semiconductors, are mainly used for laser applications. However, their drawback is incompatibility with Si platform using conventional techniques.

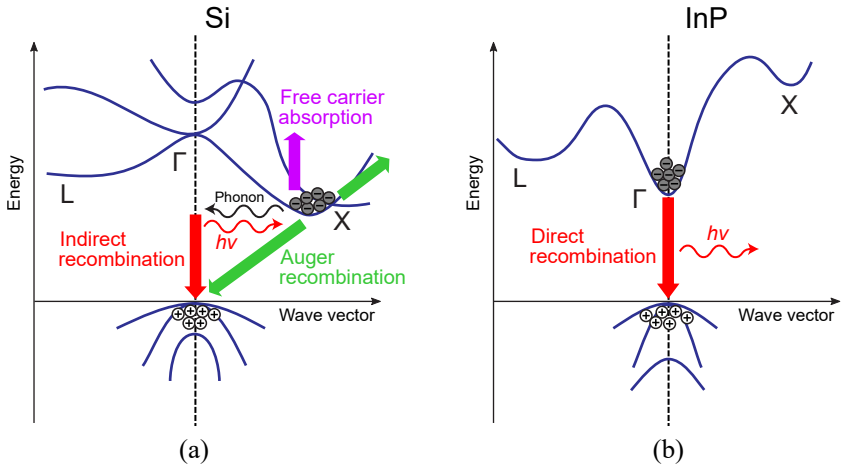


Figure 2.1: Schematic representation of band structure of (a) Si (indirect bandgap) and (b) InP (direct bandgap). Adapted from [77].

Significant effort has been made to develop Si-compatible light sources. Different approaches include using quantum confinement effect in Si nanocrystals [78], using erbium atoms as emitting centers in Er-doped Si-rich SiO_x or SiN_x [78, 79], bandgap engineering in Ge-on-Si structures [78–80]. However, all examples still suffer from very low light emission efficiency. Thus, the most practical way to achieve efficient light sources on Si is III-V integration on Si, further discussed in Section 2.2.

Two different crystalline materials can be monolithically integrated, if they share the same crystal structure and lattice constant, i.e., one can be epitaxially grown on the other. If lattice constants are not the same, the grown layer becomes strained since it adopts the substrate lattice constant. After reaching the certain critical layer thickness, strain relaxation leads to the formation of misfit dislocations, which act as non-radiative recombination and carrier scattering centers, severely degrading material quality. For instance, for this reason epitaxial growth of III-V materials on Si substrate is not an easy task, because of significant lattice mismatch between Si and III-V, as shown in Fig. 2.2.

Apart from being direct bandgap, III-V materials are advantageous due to large flexibility in choosing the bandgap of implemented materials, provided by the existence of ternary and quaternary alloys. Figure 2.2 shows the variety of III-V compounds in bandgap vs lattice constant diagram.[1] By choosing the corresponding composition of III-V compound (typically quaternary alloy) for given substrate

[1] Extensive study of band parameters of III-V semiconductors, including temperature dependence, can be found in [81].

lattice constant, it is possible to grow high quality heterostructures with predefined bandgap structure. Especially favorable situation is in case of AlGaAs/GaAs system: lattice constant of ternary $Al_xGa_{1-x}As$ alloy stays approximately the same in very broad composition range, which greatly simplifies maintaining of lattice matching. Among other things, this was the reason why the first double heterostructure lasers were demonstrated in AlGaAs/GaAs system [12, 82].

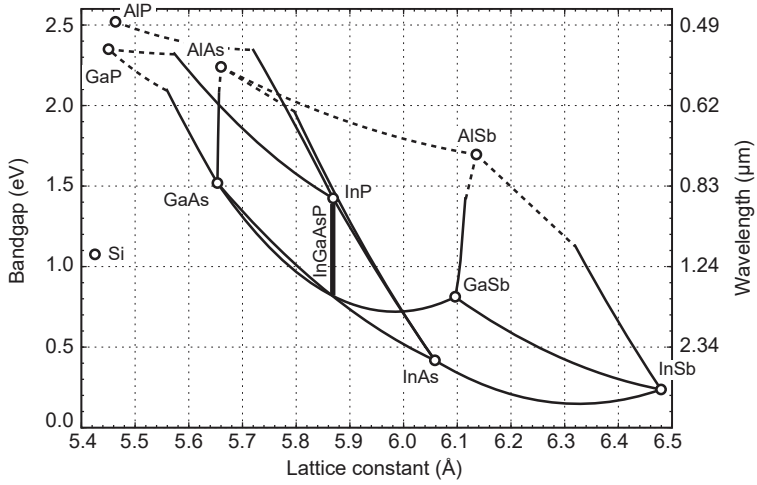


Figure 2.2: Bandgap (and corresponding wavelength) vs lattice constant of III-V semiconductors and Si at $T = 0\,\mathrm{K}$. Binary compounds are represented by points, ternary by lines, and quaternary by areas enclosed by lines. Important case of quaternary alloy InGaAsP lattice matched to InP is highlighted. Solid and dashed lines denote direct and indirect bandgap, respectively. Adapted from [28].

The most important III-V materials, which take advantage of the developed technology, are GaAs and InP. Devices based on GaAs platform mostly found their application in short-wavelength near-infrared range (0.8–1.1 µm), while InP platform is predominantly used in 1.3–1.6 µm range. However, since we aim to integrate III-V lasers on Si platform, namely, silicon-on-insulator (SOI) as the most advanced one, we need to couple light into Si waveguides, which absorb below 1.1 µm. Therefore, we utilize InP-on-Si platform.

2.1.2 Gain medium

Concerning gain material, the common approach is to utilize low-dimensional structures, such as 2D quantum wells (QWs) or 0D quantum dots (QDs), which exhibit unique density of states (DOS) properties compared to bulk material due to the re-

duction of the number of carrier translational degrees of freedom (quantum carrier confinement). Nowadays commercially used lasers based on QW gain material are the most robust and efficient due to the development of advanced epitaxial growth techniques, such as metalorganic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE), which allow the growth of very thin layers with thickness control down to monolayer level.

Quantum wells

Contrary to bulk material, which DOS has square root dependence on energy, QWs have step-like DOS function, which results in concentration of injected carriers in very narrow energy range. This leads to higher gain factor and achievement of population inversion at much lower injected current level [83, 84]. Moreover, high differential gain can be obtained in QW lasers, which gives the possibility of high speed modulation, since relaxation oscillation frequency is proportional to square root of differential gain, as shown in Eq. (1.2). Further improvement of differential gain can be achieved by implementing multiple QW structure [83], however, this comes at a cost of increased threshold current, since more material needs to be pumped.

Another advantage of QWs is the possibility to tune emission wavelength not only by composition change, but also by simply changing QW thickness due to quantization of energy levels. Furthermore, deliberate introduction of strain with opposite sign in QW and barrier layers results in increased curvature of valence band of strain-compensated QWs, which leads to less amount of holes required to reach population inversion and, thus, reduced threshold current [85].

Considering the InP platform for 1.55 µm operation, several compounds can be chosen from bandgap vs lattice constant diagram (Fig. 2.2) for well and barrier layers, such as ternary alloys InGaAs, InAlAs and quaternary alloys InGaAsP, InGaAlAs. However, the relative position of energy bands needs to be carefully considered. Combination of InGaAsP (compressively-strained well) and InGaAlAs (tensily-strained barrier) is found to provide high material gain and high differential gain due to a large conduction band discontinuity [86].

Quantum dots

Further reduction of the number of carrier degrees of freedom results in 0D QDs with δ-function-like DOS. In theory, this can provide even higher gain, lower threshold current, better temperature stability and narrower linewidth [87, 88]. However, the development of QD lasers has been hindered by the difficulty of fabrication of QDs with high density and low size variation, thus, in present-day applications QW lasers are still the most popular choice. Due to typically low areal density of QDs, in-plane optical confinement is much weaker compared to continuous QWs.

To date, the most mature QD fabrication technique is the growth of self-assembled QDs at the interface of two lattice mismatched materials in Stranski-Krastanov regime [89]. The most prominent advancement of QD lasers has been achieved with InGaAs or InAs QDs on GaAs platform with emission wavelength in 1.1–1.3 µm range [90, 91]. Longer wavelength (1.55 µm) emission of InAs QDs on InP substrate has been more difficult to achieve due to occurrence of As/P exchange [92] and relatively small lattice mismatch between InAs and InP, which results in the formation of large InAs QDs with emission wavelength >1.6 µm [93]. Nevertheless, QDs [94, 95] and QD-like so called quantum dashes [96] emitting at 1.55 µm have been demonstrated by tuning the growth conditions.

2.2 III-V integration on Si

In order to utilize the benefits provided by III-V light sources on a Si photonics platform, robust high density low cost integration technique needs to be developed. All techniques can be broadly divided into two groups: monolithic and heterogeneous.

2.2.1 Monolithic integration

Epitaxial growth of III-V materials directly on Si substrate has always been considered as the ultimate way to achieve cost-effective large scale production. However, there are fundamental challenges in such approach: large lattice constant mismatch, which leads to dislocations formation; different polarity of crystal structures, which causes anti-phase boundaries; and thermal expansion coefficient mismatch, which introduces thermal strain and cracks [97].

One way of overcoming these issues is planar growth of buffer layers, such as strained layer superlattices, for filtering out threading dislocations [98]. For elimination of anti-phase boundaries, high temperature annealing of Si substrate followed by seed and buffer layers growth can be used [99].

Another approach involves epitaxial growth on structured substrates. In this case the working principle of achieving high-quality III-V material is trapping of defects in confined growth regions. Examples include selective area growth in V-groove patterned Si substrate [100] and template-assisted selective epitaxy [101].

Most of the experimental demonstrations of III-V lasers monolithically integrated on Si [102, 103] are based on QDs as gain medium, since QDs are less sensitive to defects compared to QWs. Although significant progress has been achieved, monolithic integration is still far from being a mature technology. For this reason, heterogeneous integration is currently the most popular choice.

2.2.2 Heterogeneous integration

In principle, hybrid integration of III-V on Si could be done by standard flip-chip bonding widely used in electronic integrated circuit industry. However, this method

is unacceptable due to inherent limitations on integration density and assembly cost. Wafer bonding technology has gained a lot of popularity and is currently the most mature method for hybrid III-V on Si integration. The wide variety of wafer bonding types has been developed [104]. However, since two dissimilar materials (III-V and Si) with different thermal expansion coefficients need to be bonded, there is a requirement of relatively low bonding temperature. For application in photonics, two main techniques are widely implemented: adhesive bonding and direct molecular bonding [105].

Adhesive bonding

In case of adhesive wafer bonding, intermediate layer (typically a polymer) is used as a "glue" to hold two wafers together. Various thermoplastic, elastomeric and thermosetting polymers can be utilized for adhesive bonding, however, the requirement of stability at high temperatures during the subsequent processing leaves only thermosetting ones, with benzocyclobutene (BCB)[2] demonstrating the best performance [106]. During thermal curing, BCB undergoes polymerization with no byproducts formation, which attributes to void-free bonding [107].

Important advantage of adhesive bonding consists in relaxed requirements for surface roughness and contamination compared to direct bonding. This arises from the fact that BCB is initially applied in liquid form, thus planarizing the wafer surfaces. However, if thick (on a micrometer level) BCB layer is utilized, partial reflow during subsequent processing may occur, which is large enough to significantly affect alignment accuracy [108]. Thinning BCB layer down to $\sim$30 nm [109] probably could help to some extent, but then the advantage of high tolerance to surface contamination would be reduced. Considering also the possibility of BCB glass transition during high temperature processing[3], as well as demonstrated high alignment accuracy in case of direct bonding [108], in this work direct bonding was chosen as a method for III-V on Si integration.

Direct bonding

As the name suggests, in case of direct bonding, two wafers are brought into direct contact without any thick intermediate layer, with bonding achieved due to formation of strong covalent (molecular) bonds during subsequent annealing. For this reason, such method is sometimes called molecular bonding.

The benefits of direct bonding include high bonding strength and the absence of thick intermediate layer, which can be advantageous from device design and performance point of view. However, in order to achieve high bonding yield, stringent

[2] BCB is actually a family of related polymers. Divinylsiloxane-bis-benzocyclobutene (DVS-BCB) is commonly referred to as just BCB.

[3] Glass transition temperature depends on various parameters, thus it is usually not defined and is given as $T_g > 350\,^{\circ}\mathrm{C}$ [110].

requirements are imposed on wafer surface smoothness, flatness and cleanliness. This is due to the bonding mechanism, which relies on the short range van der Waals or hydrogen attraction forces during the initial wafer contact at room temperature. For the approach to be successful, both wafer surfaces must be in contact on the atomic level [111].

After the initial wafer contact, the formed wafer stack is annealed to convert weak van der Waals or hydrogen bonds into strong covalent bonds. In conventional approach, sometimes called fusion bonding, the required annealing temperature is very high ($> 800\,^{\circ}\mathrm{C}$) in case of both hydrophobic and hydrophilic method variations [112]. This can be tolerated in case of Si-Si bonding, however, it is totally unacceptable for dissimilar materials with different thermal expansion coefficients.

In order to lower the annealing temperature, some kind of surface activation before bonding is necessary, with the hydrophilic bonding approach being more successful for low temperature direct bonding compared to the hydrophobic one [111]. Wet chemical treatment can be used, however, better results can be achieved using oxygen plasma treatment [107, 111], with the annealing temperature lowered down to $\sim 300\,^{\circ}\mathrm{C}$. The working principle of surface activation is increasing the density of hydroxyl groups, which are responsible for establishing bonds at the interface [112, 113]. After plasma treatment, the wafer surface readily adsorbs water from air, however, a water dip is often used to enhance the surface hydration. During a pre-bonding step, –OH groups form hydrogen bonds, which are then transformed into covalent bonds following the reaction

$$\mathrm{M_1{-}OH + HO{-}M_2} \xrightarrow{T} \mathrm{M_1{-}O{-}M_2 + H_2O\,(g)}\,, \tag{2.1}$$

where $\mathrm{M_1}$, $\mathrm{M_2}$ are electropositive atoms on the bonded surfaces. The important observation is that the process is accompanied by elimination of $\mathrm{H_2O}$ molecules, which can accumulate in microbubbles and cause a large number of voids at the interface. One way to avoid the formation of voids is to etch vertical outgassing channels in Si wafer prior to bonding [114]. Gas byproduct molecules can then migrate to the closest channel and be trapped there. However, outgassing channels are not necessary if sufficiently thick amorphous dielectric layer, for example, $\mathrm{SiO_2}$, is in close proximity to the bonding interface. It can then efficiently absorb gas byproduct molecules, leading to high bonding yield [115].

An alternative approach to surface activation is the atomic layer deposition (ALD) of very thin $\mathrm{Al_2O_3}$ layer, which can have a very high density of surface –OH groups [116]. It has been shown that just the deposition of $\sim 2\,\mathrm{nm}$ ALD $\mathrm{Al_2O_3}$ prior to bonding leads to high yield low temperature bonding of heterogeneous materials [117], thus allowing to avoid the need of plasma treatment. Thus, in this work $\mathrm{Al_2O_3}$-assisted direct wafer bonding of InP and $\mathrm{SiO_2/Si}$ is implemented.

2.3 Photonic crystal membranes

The photonic crystal (PhC) platform is very powerful in terms of the possibility to realize a wide range of nanophotonic devices with small footprint and low power consumption due to enabling control of light–matter interactions through optical resonances with high quality factor and small mode volume [72, 118].

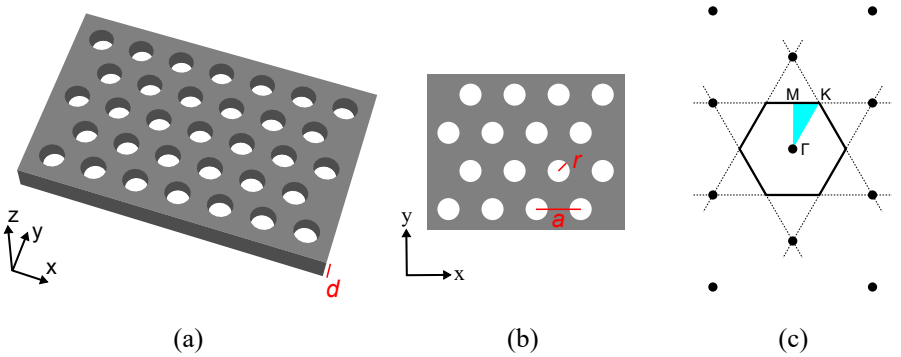
The term "photonic crystal" designates a medium with periodic dielectric function with a period of the order of the wavelength of electromagnetic waves. The backbone idea is to create a structure in which photons would behave in a way analogous to the electron behavior in conventional electronic crystals. The most important conclusion is that the periodicity of the medium gives rise to a photonic band structure with the possibility of photonic bandgap (PBG), i.e., absence of allowed propagating electromagnetic modes in certain frequency range.

The seminal work on the topic of PhCs was published in 1987 [119]. Initially the most attention was brought to the idea of 3D PhCs designed for optical wavelengths, which can provide complete PBG with prohibited propagation of light with any polarization traveling in any direction. Several types of structures have been proposed and demonstrated, such as woodpile-like and inverse opal [120]. However, PBG is very sensitive to imperfections and defects, and defect-free fabrication of 3D PhCs proved to be extremely challenging.

More feasible structure that can be successfully implemented is the PhC semiconductor slab with 2D periodicity in-plane and finite thickness in vertical direction. Two PhC slab topologies can be distinguished: rod slab and hole slab [121], with the latter gaining more interest due to more easy fabrication and the possibility to realize PhC membranes, which are suspended in air to facilitate midplane mirror symmetry and to increase refractive index contrast. In this case, 3D light confinement is achieved by in-plane bandgap guiding and index guiding through total internal reflection in vertical direction. The widest PBG can be achieved with a hexagonal arrangement of air holes in the membrane, shown in Fig. 2.3(a,b). The corresponding irreducible Brillouin zone in reciprocal space is shown in Fig. 2.3(c).

In the 2D case of a thin membrane with mirror symmetry and in-plane propagation, two principle polarization states can be identified, namely, transverse electric (TE) with electric field in x-y plane and transverse magnetic (TM) with electric field normal to x-y plane. It should be noted that pure TE and TM modes exist only at membrane midplane $z = 0$, in other cases the fields are said to be mostly polarized [121].

Figure 2.4 shows an example of PhC membrane band structure (dispersion diagram), which represents the relation of in-plane wave vector ($\mathbf{k}_{||}$) in irreducible Brillouin zone and normalized frequency of allowed modes in case of in-plane propagation ($k_z = 0$). The air hole radius r is $0.3a$, where a is PhC lattice constant. It can be seen that there is a PBG for TE-like modes, however, there is none for TM-like modes. In principle, pushing the air hole radius up to extreme values $0.4a$–$0.5a$ can lead to existence of PBG for both polarizations [121], however, membranes with



(a) (b) (c)

Figure 2.3: (a): PhC semiconductor membrane with thickness d suspended in air with hexagonal air hole arrangement. (b): 2D PhC lattice in real space with period a and air hole radius r. (c): 2D PhC lattice in reciprocal space. The first Brillouin zone and irreducible Brillouin zone are represented by hexagon and shaded region, respectively.

very thin material veins become too fragile, which makes experimental realization and exploitation of such structures impractical.

One important consequence of the finite thickness of PhC membrane compared to ideal case of infinite 2D PhC is the existence of extended modes propagating in air, i.e., leaky modes inside the light cone at frequencies $\omega \geq c|\mathbf{k}_{||}|$. Thus, PBG in PhC membrane is incomplete: it refers only to the guided modes.

The optimal membrane thickness is around half the wavelength of light in effective medium approximation. This is thick enough for the fundamental mode to be well confined, but thin enough to prevent higher-order modes from fitting within the membrane, which would drastically reduce PBG [121].

The main trend in exploitation of PhCs is the introduction of localized modes within the PBG by perturbing PhC lattice in a controllable way. The simplest case of perturbation is omitting an air hole, with other possibilities including changing air hole radius or shifting the neighboring air holes. If structure changes are applied to only one lattice site, this is called point defect. If several point defects are connected in a continuous line, they form line defects. Properly designed defects can support modes within the PBG, which are forbidden to propagate in the surrounding unperturbed PhC, thus forming an optical cavity. In order to strongly suppress vertical radiation losses, electric field distribution in the cavity can be tailored to be not abrupt at the cavity edges by shifting certain air holes [122].

Extended line defects can also be utilized as the waveguides, which are interesting due to the possibility of operation in slow light regime, when light group velocity is greatly reduced near the band edge. This can be exploited to significantly enhance nonlinear effects in passive structures [123] or to increase effective

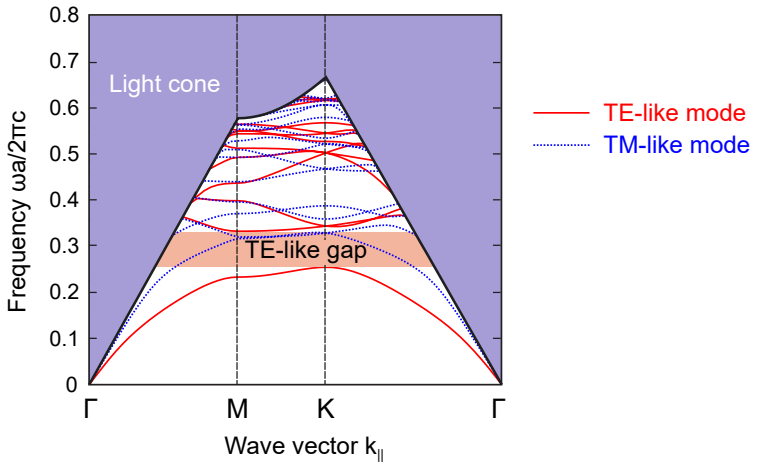


Figure 2.4: An example of band structure of PhC air hole membrane in case of dielectric constant $\varepsilon = 12$, thickness $d = 0.6a$ and air hole radius $r = 0.3a$, where a is PhC lattice constant. TE-like bandgap is highlighted. Note the absence of TM-like bandgap and the existence of leaky modes in the light cone. Adapted from [121].

spatial gain coefficient in active structures [124].

Due to the very strong light confinement provided by PBG, high quality factor Q values, exceeding 10^6, can be achieved in optimized ultrasmall cavities with effective mode volume V of the order of $(\lambda/n)^3$, where n is the medium refractive index [125]. Furthermore, if an emitter is embedded in a cavity, the existence of PBG allows to efficiently inhibit in-plane spontaneous emission, apart from emission coupled to the cavity mode, which can then be even enhanced due to the Purcell effect, since Q/V ratio is very high [126]. Therefore, such PhC cavities are very promising in application for nanolasers with low threshold and low power consumption, as discussed in Subsection 1.2.2.

2.4 Photonic crystal lasers

The first demonstration of PhC laser was reported in 1999, lasing was achieved under pulsed optical pumping at 143 K in a QW InGaAsP PhC membrane [127]. However, the main roadblock for achieving RT CW operation is a significant increase of the local temperature due to inefficient heat dissipation from the cavity. First of all, this is due to an inherent property of PhC membrane, which is suspended in air for larger refractive index contrast. Thermal properties can be improved to some extent by implementing PhC slab standing on SiO_2, but at the

price of significantly compromised vertical optical confinement [128]. Second, the thermal conductivity of the conventional membrane layer (InGaAsP) is poor. In addition, generated carriers can easily escape from the cavity, thus degrading efficiency and requiring higher input power. RT CW operation can be achieved by implementing InAs QDs [129, 130] or extremely small cavity [131]. However, the heating problem still remains, giving rise to output power saturation at relatively low input power.

All of the aforementioned lasing examples were achieved under optical pumping with an external laser, which is not viable for application in real short-range interconnects. Thus, electrical carrier injection through p-i-n junction is a critically important feature for nanolasers. However, it introduces additional difficulty in controlling the device local temperature. Heat generation occurs due to electrical resistance in n- and p-doped regions, which can be quite large in case of small cavity length. In addition, doping can cause optical losses in the system, thus degrading cavity quality factor. Moreover, special attention should be brought to the elimination of leakage currents.

Significant progress has been achieved with the idea of embedding active material in BH structure, which provides strong optical and carrier confinement [49]. It can be realized by etching a mesa through the active material layers (InGaAsP), followed by the regrowth of passive lower refractive index material with wider bandgap (InP) around the mesa. Moreover, heat dissipation from the cavity is enhanced since InGaAsP (poor thermal conductor) is substituted by InP in all the membrane except the cavity region, thus lowering the local temperature [50]. The drawback of implementing BH is an increased complexity of the fabrication process due to the difficulty to realize extremely small BH with precise position and with flat top surface after the regrowth.

2.4.1 Current injection geometry

The main challenge of electrical pumping of PhC membrane lasers is how to efficiently inject current into the very small cavity region. Considering the geometry of electrical injection, two principal variants can be distinguished: vertical and lateral current injection. In case of vertical geometry, p-i-n junction is typically formed by epitaxial growth of required combination of doped layers, whereas for lateral injection scheme, initially intrinsic[4] layers are grown, with the doping being subsequently performed in specific areas.

Vertical injection

Historically, fabrication of vertical p-i-n junction is the most widespread technique to inject current in laser active region due to the straightforward fabrication procedure: low defect layers with high doping concentration are readily attainable by

[4]By “intrinsic”, non-intentionally doped layers with very low carrier concentration are meant.

means of MOVPE or MBE growth. In fact, the initial demonstration of electrically pumped PhC laser was achieved with vertical current injection [132]. In this example threshold current and active volume were very large due to inefficient optical and carrier confinement in PhC slab. Later, the concept of current injection through the vertical post under the cavity in PhC membrane was realized, which led to substantial reduction of threshold current and operation at RT, however, only in pulsed regime [133, 134]. The idea is to utilize a particular cavity mode which can survive at the presence of the post. Introduction of the post structure also provides improved heat dissipation from the cavity compared to free standing membrane. The same approach was also applied to PhC nanobeam device (1D array of air holes in III-V nanorib) [135]. However, implementation of vertical injection significantly limits the achievable cavity Q-factor due to optical losses in doped layers. Furthermore, the presence of the post structure restricts the choice of cavity design due to the requirement of minimizing the vertical losses through the post. Moreover, efficient pumping of very small cavities becomes difficult due to lack of carrier confinement structure in lateral direction. In addition, fabrication of post structure suffers from high degree of complexity, e.g., double side processing and very precise alignment after bonding is required [136].

Vertical current injection has also been demonstrated without post structure for 1D PhC nanorib (nanobeam) laser operating at RT in CW regime [71]. Lasing has been achieved due to several factors: optimization of spatial overlap of the optical mode with the carrier recombination profile while keeping Q-factor sufficiently high by adjusting p-metal contacts position; chemical surface passivation to inhibit non-radiative recombination; encapsulation of the structure in SiO_2 for heat dissipation. High output power has been achieved (95 µW). However, threshold current is quite large (100 µA), which is explained by rather low Q-factor and large active volume, which is the roadblock for ultralow power consumption. Moreover, high speed modulation could be hindered by large capacitance of such structure.

Lateral injection

Alternative approach for carrier injection into the cavity is to employ lateral p-i-n junction [137]. Realization of lateral p-i-n junction can be achieved by butt-joint regrowth of p- and n-doped materials [137, 138]. However, since precise control of ultrasmall structures is required, fabrication process becomes highly complicated, with especial difficulty to achieve flat top surface, required for the cavity with high Q-factor [49]. For this reason, doping is usually performed by means of ion implantation or thermal diffusion.

Applicable to PhC lasers, the concept of lateral injection was first proposed in [139]. Compared to vertical injection, lateral geometry is more flexible, releasing additional spatial degree of freedom for device design and relaxing many requirements inherent to vertical geometry. For instance, the doping pattern can be defined lithographically, which gives better control over the current flow in the

plane. Arbitrary PhC cavity designs with smaller efficiently injected active volumes and higher Q-factors can then be implemented. Moreover, since doping is introduced only in the desired areas (as opposed to overall uniform doping in case of vertical geometry), the rest of the membrane can be left not doped, which leads to reduced optical losses and, as a consequence, even higher cavity Q-factor. As a result, lateral injection configuration is highly advantageous in terms of achieving low threshold current and low power consumption.

Another strength of the lateral scheme is its planar nature, which may ease the device integration in a circuit. In addition, integration of active and passive devices is facilitated by the absence of overall doping. Regarding the prospect of high speed modulation, the lateral injection scheme offers the benefit of very small junction capacitance compared to the vertical scheme due to the collinear mutual arrangement of doped layers. However, the drawback of implementing lateral geometry is the introduction of high temperature annealing steps in the process flow, which are generally undesired, especially in CMOS industry, and less spatial accuracy compared to the epitaxially grown doped layers.

The first PhC laser with lateral current injection was demonstrated with InAs QDs on a GaAs platform [140]. Ultralow threshold current less than 1 µA was achieved, however, CW operation was possible only at low temperatures (150 K). At RT the device operated only as a light emitting diode (LED), and even though high speed modulation with ultralow power consumption was demonstrated, output power, as expected for an LED, was exceptionally low [141].

The breakthrough was achieved by NTT group by embedding QW active material in BH. PhC membrane laser on InP substrate with lateral p-i-n junction was demonstrated to operate in RT CW regime with very low threshold current and power consumption [54]. Later, the same design was realized on a Si substrate [68, 70]. Since the processing includes high temperature annealing steps, III-V membrane should be quite thin (∼250 nm) due to thermal expansion coefficient mismatch with Si substrate [33], thus, lateral injection scheme can only be used, since it would be very difficult to implement vertical scheme in such thin structure. However, demonstrated devices suffer from quite low optical output power. Therefore, further progress is needed to improve the performance of such devices, including the development and optimization of doping technologies for fabrication of lateral p-i-n junction.

Chapter 3

Theoretical background on doping

In this chapter, a survey of possible doping techniques for realization of n- and p-doped regions for lateral p-i-n junction in InP is given.

In semiconductor technology, there are two primary methods to selectively introduce doping in the designed areas apart from the regrowth: ion implantation and thermal diffusion. In case of the ion implantation, basically any ions can be implanted into any material, whereas for the thermal diffusion, appropriate compound must be found for particular diffusion process details. Applied to this work, the main requirements for doping processes are high electrical conductivity of doped regions and the possibility to limit the processing temperature as much as possible. The second requirement is valid in the general case just from economic considerations, however, in our case it is especially relevant due to, first, possible effect on active material properties, and second, thermal expansion coefficient mismatch between InP membrane and Si substrate, even though the membrane is quite thin. Moreover, adequate means of surface protection during annealing in case of III-V materials (encapsulation, Group V gas overpressure) need to be implemented.

3.1 Doping for n-type InP

3.1.1 Choice of n-type impurity

Considering n-type doping in InP (and all III-V materials), several types of donor dopants can be utilized: examples are Group IV elements taking place in indium sublattice (Si, Ge, Sn) and Group VI elements (S, Se, Te) substituting phosphorus. Thermal diffusion of these dopants is completely not viable due to very low diffusivity in InP at the practical temperatures. Instead, ion implantation can be utilized.

Ion implantation is a robust way for selective area doping of semiconductor layers with the excellent control over both the amount and position of the doping. The dopant dose is controlled by the ion current and implantation duration, whereas the average depth (projected range) is controlled by the ion energy. Ion implantation is widely used in silicon industry. Among III-V materials, the most research has been performed for GaAs, however, behavior of implanted ions in GaAs and InP is quite often similar.

The energetic ions can lose their energy through interactions with either electrons or nuclei in the substrate. Electronic stopping is an inelastic process of excitation or ionization of the substrate atoms, which does not introduce lattice damage and depends only on the target properties and ion energy and not on the ion type. Electronic stopping power (defined as the ion energy loss per unit length) is found to increase as the square root of ion energy [142]. Nuclear stopping can be visualized as the elastic collisions of hard spheres (ion and target nuclei) with substantial transfer of energy, which can be enough to displace target nuclei and thus create lattice defects. Nuclear stopping power is initially relatively small at large ion energies, since fast ions may not have sufficient time to interact with the target nuclei, but later significantly increases when the ion energy becomes small [142]. Moreover, this process depends on the ion type, with much more drastic effect of nuclear stopping for the heavy ions compared to the light ions in the whole energy range.

Since the implantation process introduces lattice damage through the nuclear stopping mechanism, a subsequent annealing treatment is required to heal the crystal and restore the carrier mobility and lifetime. Furthermore, after the implantation only a part of the as-implanted ions are located in substitutional sites, where they are electrically active, thus, annealing is needed to facilitate short-range diffusion to corresponding lattice positions. As earlier mentioned, it is critically important that the annealing temperature is kept as low as possible while still providing sufficient lattice restoration and dopant activation.

For the light ions, the main energy loss mechanism is electronic stopping, with the nuclear becoming dominant only close to the final ion positions. Consequently, much less lattice disorder is induced by the light ions compared to the heavy ones, with the latter introducing significant damage over the entire projected range. For this reason, heavy elements such as Ge, Se and especially Sn, Te are disadvantageous due to the requirement of very high temperature annealing to repair significant lattice damage and activate the dopants [143]. In principle, implantation at elevated temperature ($\sim$200 °C) can be done to reduce the damage level [144], which has been shown to improve Se activation [145]. However, the effect of elevated temperature is less pronounced for InP compared to GaAs [146].

Sulphur as a light element can be used for n-type InP implantation with small degree of lattice disorder. However, it is characterized by substantial diffusivity in InP, which results in thermally unstable doping profile [147].

Another issue that should be considered is the amphoteric nature of Group IV elements (Si, Ge, Sn) in InP, since they can also occupy Group V lattice position exhibiting an acceptor behavior. For high doses, increase in amphoteric character as Sn < Si < Ge is reported based on electrical measurements of implanted n-InP [148]. Due to this, Ge implantation is typically characterized by poor activation ratios [149].

Silicon ion implantation is the most popular way to obtain n-type InP since Si impurities induce the least amount of lattice damage and thus can be implanted at RT and be activated at relatively moderate temperatures [150]. Furthermore, low Si diffusivity means thermal stability of doping profile (as opposed to S). However, at very high ion doses Si amphoteric nature starts playing a role.

3.1.2 Silicon ion implantation

The most abundant silicon isotope is ^{28}Si. However, implantation of $^{28}Si^{+}$ ions is usually avoided due to the possibility of contamination by $^{14}N_2{}^{+}$ ions, which have the same mass-to-charge ratio. For this reason, $^{29}Si^{+}$ ions are usually utilized.

The common ion implantation issue that should be mentioned is channeling, which occurs when projectile ions align with a major crystallographic direction and are guided between rows of atoms in a crystal, experiencing only electronic stopping [142]. It results in the difficulty to predict and control the implant profile, since the channeling is very sensitive to surface condition, defects and impurities in the substrate, temperature, the angular dispersion of the incident ion beam, accumulated ion dose, etc. [146] The standard procedure to minimize the channeling is to tilt and rotate the substrate relative to the ion beam, however, complete elimination of channeling is possible only in case of implantation in amorphous layers.

Ion dose

The typical values of used ion dose lie in 10^{12}–$10^{15}\,\mathrm{cm}^{-2}$ range. High doses are desired to obtain high carrier concentration in doped InP. However, electrical activation ratio decreases with increase in implanted ion dose due to several factors. First of all, even though Si is a light element, it can still cause substantial lattice damage. For Si ion implantation in InP at RT, highly disordered amorphised layers are formed if ion dose is higher than $\sim 1 \times 10^{14}\,\mathrm{cm}^{-2}$ [151–153]. The lattice is recovered during subsequent annealing, but not completely, since full recovery after ion implantation is generally hard to achieve for compound materials [146]. Since constituent elements of the target compound have different masses (and the difference is quite large in case of ^{115}In and ^{31}P in InP), after collisions with projectile ions, the lighter atoms (P) will recoil further compared to the heavier atoms (In), causing the disturbance of stoichiometry [154]. Consequently, at shallow depths an excess of In can be present while at greater depths an excess of P can exist.

Apart from the reduced Si activation due to compensation via complexes of Si with implantation-induced defects, at high doses the residual lattice disorder can degrade carrier mobility. Furthermore, increasing ion dose can also limit electrical activation due to solid solubility constraint and enhanced compensation via native defects [149].

Performing implantation at elevated temperature is especially effective for reduction of lattice damage caused by heavy ions. However, for Si it is also found to have a pronounced effect at high doses [144]. The defects created during the implantation become more mobile at elevated temperature and can immediately annihilate each other, thus avoiding the formation of extended damaged regions.

Even though Si is predominantly n-type dopant in InP, at high concentrations Si starts to show amphoteric behavior. To act as a donor, Si has to occupy an In lattice site. Therefore, Si activation depends on the availability of In vacancies during annealing. At the same time, large amount of P vacancies becomes available (either implantation-induced or thermally generated), which can be occupied by excess Si in case of high implanted dose, which leads to Si self-compensation and reduction of donor activation ratio [152]. In addition, local deviations from stoichiometric composition can also have an effect on Si activation via altered vacancy distribution [154].

Coimplantation of Si and P ions can be used to suppress Si amphoteric behavior, since in the presence of excess P relative availability of In lattice sites increases, which results in enhanced Si activation [155]. Coimplantation of Si and S is also known to enhance electron concentration [147], since Si and S occupy different lattice positions when acting as donors: Si goes to In sublattice, and S goes to P sublattice. However, the drawback of coimplantation consists in increased overall lattice damage and reduced electron mobility.

Activation annealing

The recovery of implantation-induced lattice damage in InP can occur to some extent even at RT in case of low Si ion doses [151, 156]. However, for dopant electrical activation and effective damage recovery, high temperature annealing is essential. Appreciable reordering of initially heavily damaged layers occurs already at ∼400 °C, however, Si activation becomes sizable only at ∼600 °C [157]. To maximize Si activation ratio, the substrate is typically annealed at the temperature in 750–850 °C range [158]. The most of the lattice damage is repaired at that temperatures, but the certain amount of residual defects can still persist.

Regarding the annealing technique, conventional furnace processing was initially the most widely used. However, rapid thermal annealing (RTA) later gained a lot of popularity [159] due to the opportunity to significantly reduce the annealing duration to avoid possible adverse effects (dopant diffusion, surface degradation). In general, the optimal annealing conditions with RTA consist of a higher tem-

perature, shorter duration (800–850 °C, 5–30 s) cycle than for furnace annealing (700–750 °C, 10–30 min).

However, InP starts to decompose and lose phosphorus during annealing at that high temperatures. Therefore, some kind of surface protection is required. Three possible methods can be implemented: proximity annealing, Group V (PH_3) overpressure and encapsulation [159].

In case of proximity annealing [149], the implanted wafer is placed face-to-face with another sacrificial InP wafer. This method was initially popular due to its simplicity, however, it is far from optimal due to the possibility of microscratches and baked-on contamination.

External Group V overpressure is regarded as an ideal solution [159], however, in practice it might be difficult to implement due to, for example, the need of introduction of Group V gas lines in RTA tool.

Encapsulation by deposition of protecting layer cap is a widely used technique to avoid surface degradation during annealing. Various protecting materials can be used: examples are SiN_x [147, 152], phosphosilicate glass (PSG) [145], Al_2O_3 [160], AlN [153]. The requirement for capping layer is to withstand annealing and prevent cracking, peeling and other degradation effects.

3.2 Doping for p-type InP

3.2.1 Choice of p-type impurity

Ion implantation can also be utilized for the selective area p-doping of III-V materials. Examples of acceptor impurities occupying Group III substitutional sites include Be, Mg, Zn, Cd. However, the general issue with p-doping of InP is in substantially lower carrier concentrations and poor electrical activation ratios observed for p-type impurities compared to n-type InP [150, 161]. Such behavior is in contrast with GaAs, for which the opposite trend is observed: achievable carrier concentrations are typically one order of magnitude higher for p-GaAs compared to n-GaAs. According to the amphoteric native defect model, this can be explained by the difference in relative formation energies for the compensating native point defects [162].

Another important aspect is the much higher diffusivity of p-type impurities in InP compared to n-type ones. Since ion implantation process implies high temperature annealing for dopant activation, significant redistribution and outdiffusion can occur even if RTA is implemented [146, 163].

The most popular p-type dopants for ion implantation into InP are Be and Mg due to their low masses. In order to inhibit the dopant diffusion and enhance the electrical activation, coimplantation with P can be utilized [164–166]. The idea is to increase the density of available In vacancies to enhance the acceptor occupation of substitutional sites, where dopants are electrically active, and minimize the occupation of interstitial sites, since interstitial diffusion is responsible for the high

diffusivity. However, almost similar results were obtained by coimplantation of inert Ar ions [165], which is the indication of the primary role of increased implantation-induced damage. To heal this damage, longer annealing at higher temperatures is required [166], which is disadvantageous. Moreover, in this case maximum achievable hole concentration in p-InP is only slightly larger than $10^{18}\,\mathrm{cm}^{-3}$, which is not enough to fabricate ohmic metal contacts. Typically InGaAs layer[1] with high p-type conductivity on top of p-InP is used for ohmic contacts, but in case of ion implantation, this approach then requires unnecessary processing complication and potentially even higher activation annealing temperatures.

High diffusivity of p-type impurities can be not suppressed, but exploited for doping purposes by implementing not ion implantation, but thermal diffusion at significantly lower temperatures compared to typical implant activation temperatures. The problem of implantation-induced damage is then also avoided. The drawback of doping incorporation by diffusion is the inherent limitation on the shape of the doping profile, thus, it is less flexible. However, for thin membrane application this issue is of small importance.

Among other choices, zinc thermal diffusion gained significant popularity for obtaining p-type doping in III-V materials because of Zn very rapid diffusion, high solubility and low ionization energy.

3.2.2 Zinc thermal diffusion

Mechanism

It is generally accepted that Zn diffusion in InP is governed by substitutional-interstitial mechanism [167]. The diffusion process is dominated by highly mobile Zn interstitials, which are then incorporated into substitutional In sites, where Zn is electrically active and behaves as the shallow acceptor. Thus, the hole concentration is typically assumed to be equal to substitutional Zn concentration in the absence of compensation. The diffusivity of substitutional Zn is thought to be negligible.

One possible way for a Zn interstitial to occupy a substitutional site is the dissociative mechanism (also known as the Frank–Turnbull mechanism). In such scenario a Zn interstitial $\mathrm{Zn_i}^{m+}$ takes the place of an In vacancy $\mathrm{V_{In}}$ according to the reaction equation

$$\mathrm{Zn_i}^{m+} + \mathrm{V_{In}} \rightleftarrows \mathrm{Zn_{In}}^{-} + (m{+}1)\,\mathrm{h}\,, \tag{3.1}$$

where m is the charge state of Zn interstitial, $\mathrm{Zn_{In}}^{-}$ is a substitutional Zn and h is a hole. This mechanism was long believed to be responsible for Zn diffusion in InP [168]. However, later, the kick-out mechanism was also suggested. According to it,

[1] In this work, the alloy composition lattice-matched to InP ($\mathrm{In_{0.53}Ga_{0.47}As}$) will be referred to as InGaAs, unless mentioned otherwise.

Zn interstitials displace In atoms $\mathrm{In_{In}}$ from their positions, creating In interstitials $\mathrm{In_i}$ according to the reaction equation

$$\mathrm{Zn_i}^{m+} + \mathrm{In_{In}} \rightleftarrows \mathrm{Zn_{In}}^{-} + \mathrm{In_i} + (m{+}1)\,\mathrm{h}\,. \tag{3.2}$$

When the defect equilibrium is assumed (e.g., in case of isoconcentration diffusion), the two models are indistinguishable due to the relation between In vacancies and In interstitials. However, in case of the defect non-equilibrium, the dissociative mechanism may be limited by the replenishing of In vacancies, and the kick-out mechanism may be controlled by the elimination of excess In interstitials. The kick-out model for Zn diffusion in InP was supported by the observation of interstitial-type dislocation loops [169], indication of the kick-out reaction between Zn and substitutional Fe in InP:Fe [170] and ab initio calculations [171].

The diffusivity of Zn in InP is known to be concentration dependent due to the fact that the observed diffusion front profiles are more abrupt compared to the prediction by the standard complementary error function (erfc), which is valid for the case of a constant diffusivity [142]. The dependence of Zn diffusivity D on concentration C at fixed temperature is determined by the charge state of the Zn interstitials m according to the $D \propto C^{m+1}$ relation, which gives the possibility of obtaining the value of m by fitting the experimental diffusion profiles. However, in literature there are conflicting reports on the charge state of diffusing Zn interstitials. In one work, the value of m was found to be 0 for undoped InP, but +2 for n-doped InP [172]. However, for that work the observed steep diffusion profile for n-InP could be alternatively explained by the effectively stopped interstitial diffusion due to the lack of Zn interstitials at overall Zn concentrations lower than the background donor concentration [168]. In other works, the charge state of Zn interstitials was found to be $m = 0$ [173, 174], $m = +1$ [167, 168, 170, 175] or $m = +2$ [171, 176]. The discrepancy emphasizes the significant complexity of the diffusion process in compound semiconductors, with a large number of various factors potentially playing a role. Moreover, the concentration of diffusing Zn interstitials is usually assumed to be negligible, which might be the wrong assumption in some cases. It should be noted that at extremely high Zn concentrations (10^{19}–$10^{20}\,\mathrm{cm^{-3}}$), the modeling of the diffusion mechanism is further complicated, with Zn diffusivity found to become concentration independent [177].

Technology

Several techniques can be used for post-growth InP p-doping via Zn thermal diffusion. Among them are sealed ampoule diffusion, spin-on film diffusion and open tube diffusion. The sealed ampoule technique is the oldest method [178], and was widely used in the early works with either solid Zn [169, 177, 178] or $\mathrm{Zn_3P_2}$ [167, 168] as Zn source, with the option of adding red phosphorus to provide P overpressure. However, such process suffers from poor uniformity across the wafer and

reproducibility of doping concentration and profile due to variations in Zn and P vapor pressure. Scalability for mass production is also an issue due to procedure complexity and low throughput. In addition, poor surface morphology can be a problem due to the formation of zinc phosphide during cooling down step, since Zn source is eliminated only after cooling down. Moreover, the whole system is not flexible, since only two parameters can be effectively used to influence the process: temperature and duration. Zn diffusion from spin-on Zn-doped silica films is one possible alternative [179, 180], but it also suffers from the lack of reproducibility and flexibility.

The most successful technique is the open tube diffusion, which can be performed in a conventional MOVPE reactor under flowing carrier gas and Group V gas overpressure using Zn-organic compounds (dimethylzinc (DMZn) or diethylzinc (DEZn)) as Zn source [181]. The description of the MOVPE system is given in Subsection 4.3.1. The key advantage of MOVPE-based diffusion is the ability to independently control Zn and P/As partial pressure with high precision simply by switching and adjusting the corresponding gas flows at the arbitrary temperature. Therefore, this method is highly flexible and precise in terms of controlling the diffusion conditions, with better reproducibility and uniformity across the wafer. Diffusion duration can be controlled just by switching on and off the Zn source gas flow, thus, the problem of surface degradation due to zinc phosphide formation during cooling down step is avoided. Moreover, the possibility of wafer rotation provides further improvement in the uniformity.

It has been shown that Zn diffusion in InP gives higher values of hole concentration if InGaAs capping layer is on top of InP layer [182]. This fact is quite convenient since p-InGaAs layer can also be used for high quality ohmic contacts.

The main parameters that affect the MOVPE-based Zn diffusion process are the wafer temperature, the diffusion duration, the Group V gas partial pressure and the Zn source partial pressure.

The optimal diffusion temperature for both InP and InGaAs lies in 500–550 °C range, with the maximum attainable Zn and hole concentration, as well as the diffusion depth, reached in this range. Decrease of Zn concentration at higher temperatures can be explained by increased rate of Zn desorption from the surface, which leads to significant loss of Zn to the gas stream and smaller amount of Zn available for diffusion [175, 183–186]. Decreased number of surface incorporation sites was also suggested [182]. At temperatures lower than ∼500 °C, the diffusion is hindered by the formation of parasitic layer of zinc phosphide on InP [175, 183, 185] or zinc arsenide on InGaAs [184]. Substantial Zn diffusion under Group V gas-free atmosphere at lower temperatures (380–425 °C) without the formation of the parasitic layer was successfully demonstrated for InGaAs, but not for InP [187].

The diffusion duration can be used to control the doping depth. The majority of the published results demonstrate the proportionality of the diffusion depth to the square root of the diffusion time [175, 183–185, 188, 189], which is the indication

of the reached local equilibrium and the possibility to describe the process as a diffusion from a source with a constant concentration [142]. However, in one work a linear dependence of depth with time was observed [182], which might indicate an error or the complicated diffusion process.

Group V gas overpressure during Zn diffusion is primarily required to protect the III-V surface from the thermal degradation. However, it can also affect Zn diffusion process via the influence on the equilibrium concentration of the intrinsic point defects, such as P/As and In vacancies, since incorporation and diffusion of Zn depend on the availability of substitutional and interstitial sites. In one work, increase of PH_3 partial pressure resulted in enhanced Zn incorporation in InP [190]. Contrary, in other work no effect of PH_3 partial pressure was observed [183]. In case of Zn diffusion in InGaAs, Zn concentration was found to be the same in a quite wide AsH_3 flow range, with the decline under very low and very high AsH_3 flows and deteriorated InGaAs surface under very high AsH_3 flows [184]. The authors propose the hypothesis of AsH_3-catalyzed pyrolysis of DMZn molecules in the medium AsH_3 flow range, which is hindered in high AsH_3 flow regime due to unspecified side reactions. However, at the used temperature of 525 °C, DMZn is typically considered to be completely decomposed [191]. Thus, the hypothesis of the influence on the vacancy concentrations seems to be more viable.

The increase of the Zn source (DEZn or DMZn) partial pressure leads to the increase of the diffusion depth [175, 183, 185, 186], however, the exact dependence is difficult to single out. The maximum incorporated Zn concentration increases with Zn source flow increase as well [175]. The dependence is shown to be linear for InP [185, 186], but square root for InGaAs [184], with the difference in Zn source flow ranges potentially being responsible. The hole concentration initially follows the Zn concentration, however, at high Zn source flows, Zn electrical activation substantially decreases, leading to the saturation of the hole concentration [185].

Zn activation

The saturation of the hole concentration at the relatively high Zn concentrations ($>10^{18}\,cm^{-3}$) constitutes a serious problem for obtaining p-InP with high conductivity. This issue is known to exist not only for Zn-diffused InP, but also for InP doped with Zn during the epitaxial growth. However, significant improvement of the hole concentration can be achieved by annealing under inert atmosphere at the temperature in 400–470 °C range [192]. RTA is typically used for annealing. Several explanations have been proposed in order to describe the initially low Zn electrical activity and the subsequent activation after annealing.

According to the first hypothesis, at high total Zn concentrations, the ratio of Zn atoms occupying interstitial sites becomes comparable to the ratio of Zn in substitutional sites, which leads to the reduction of Zn electrical activation. Moreover, if we assume the positive charge state of the Zn interstitials, then they have donor behavior and even compensate substitutional Zn acceptors. During the annealing,

mobile Zn interstitials outdiffuse to the surface and evaporate, which results in the decreased total Zn concentration, but the increased hole concentration. Meanwhile, substitutional Zn is almost not affected, if the annealing is not too long. Such behavior was experimentally observed, with no change in the diffusion depth [167, 183]. Another related explanation consists in Zn interstitials taking substitutional sites provided by generated In vacancies [182, 188].

The alternative hypothesis explains the observed low Zn electrical activity in InP by hydrogen passivation of Zn dopants via the formation of Zn – H complexes [182]. The hydrogen atoms can originate from either AsH_3 [193] or PH_3 [194]. During the annealing, hydrogen atoms release substitutional Zn and outdiffuse, thus giving rise to Zn electrical activation.

In addition, the neutral Zn complexes with P vacancies V_P might also be responsible for the low Zn electrical activity at high concentrations [177]. It was suggested that the formation of the stable Zn – V_P pairs can take place only in the relatively narrow temperature interval of 270–370 °C, with the dissociation occurring at higher temperatures [195]. The final concentration of such complexes is thought to depend on the time spent in that temperature range during the cooling down step from the higher temperatures. Since RTA offers faster cooling rates compared to MOVPE, this fact might contribute to the observed enhancement of Zn activation after RTA at >370 °C [195]. However, the total effect of the formation of Zn – V_P complexes is considered to be insufficient to explain the observed hole concentration saturation for Zn-doped InP [196].

3.3 Summary

To summarize, Si ion implantation and Zn thermal diffusion are the most promising methods for the selective area doping of InP and the fabrication of the lateral p-i-n junctions. However, the technology is not so well established as for silicon processing, with the significant amount of conflicting reports and missing data. The particular processing conditions, e.g., material quality, pre-treatment, the details of the utilized MOVPE system, can have an effect on the outcome. Furthermore, all of the discussed literature examples described the processing performed with InP substrates. Since InP membranes bonded to Si substrate are in the scope of this work, additional complexity is involved, especially due to the requirement of high temperature annealing steps. Thorough study of the doping technologies and the development of the fabrication procedure is thus required.

Chapter 4

Fabrication process development

The goal of this work is experimental demonstration of nanophotonic devices with electrical control. The fabrication process in a cleanroom facility is complex and time-consuming, with the outcome of different steps being interdependent. Numerous test runs with different degree of sophistication were performed at various stages. In this chapter, optimized process flow is presented, starting with brief illustrated overview and followed by detailed description of fabrication stages. Encountered problems and ways to solve them are also discussed.

Complete recipe-style process flow details can be found in Appendix A.

4.1 Fabrication overview

During this work, the exact process flow details were constantly adjusted after optimization runs, but the overall framework stayed the same. In this section, the main stages of fabrication of PhC BH InP device on Si substrate with lateral p-i-n junction are presented. For the sake of simplicity, schematic illustrations of the sample are given only for major changes, with intermediate steps involving resist and hard mask layers being omitted in most stages.

The fabrication starts with MOVPE growth of InP with embedded active material (QW or QD) on a InP substrate (Fig. 4.1a). These layers are designed to be intrinsic and are not doped intentionally. In a separate process, 1.1 µm of thermal oxide is grown on silicon wafer by wet oxidation in the furnace at 1100 °C (Fig. 4.1b). Targeted oxide thickness depends on the particular design of the final devices, e.g., to facilitate efficient light coupling in grating couplers.

The next stage is direct bonding. Very thin (∼2 nm) Al_2O_3 layer is deposited by ALD on both InP and SiO_2/Si wafers (Fig. 4.2a), which are then pressed to each other and annealed at 300 °C with applied pressure (Fig. 4.2b).

After bonding, InP substrate is selectively wet etched, which leaves only III-V epilayers on SiO_2/Si substrate (Fig. 4.3a). Then, the InGaAs etch-stop layer is

also selectively wet etched (Fig. 4.3b).

In order to create alignment marks in Si, so called pre-alignment openings are first etched through III-V and SiO_2 by a combination of dry and wet etching (Fig. 4.4a). This step is required to clear the area in Si from III-V/SiO_2 stack located above. Alignment marks are then dry etched in silicon substrate (Fig. 4.4b). Both pre-alignment openings and alignment marks patterns are defined in positive tone ultraviolet (UV) photoresist by means of contact UV lithography.

Figure 4.5(a,b) shows BH formed inside InP layer by dry etching of surrounding active III-V material and two subsequent MOVPE regrowths: selective area growth of passive InP and planarization growth of InP and InGaAs on top. E-beam lithography is used to define the BH pattern in a negative tone e-beam resist compatible with epitaxial growth.

For n-type InP doping, a deep ultraviolet (DUV) photoresist mask pattern is defined. The bottom anti-reflective coating (BARC) layer is left underneath (Fig. 4.6a). Si ion implantation is then performed in exposed BARC/InGaAs/InP layer structure at room temperature. After ion implantation, BARC and DUV photoresist layers are stripped (Fig. 4.6b).

Since p-type doping of InP is done by Zn diffusion at elevated temperatures in a MOVPE tool, a SiO_2 layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) to act as a hard mask layer. DUV lithography is then used to define pattern in DUV photoresist layer. Pattern is transferred to BARC and SiO_2 layers by two subsequent dry etching steps. DUV photoresist and BARC layers are then stripped (Fig. 4.7a). Zn diffusion is performed in MOVPE tool under AsH_3 atmosphere using DEZn as Zn source. For the Si implantation, activation step by annealing at 650 °C is incorporated in early steps of Zn diffusion recipe. After Zn diffusion, Zn impurities are activated by RTA in N_2 atmosphere. The SiO_2 hard mask is then wet etched (Fig. 4.7b).

Next, the InGaAs layer is selectively wet etched everywhere except areas designed for P metal contacts (Fig. 4.8a). InGaAs is later used as an intermediate layer between p-InP and P metal contacts due to poor performance of metal contacts directly to p-InP. Standard UV lithography with positive tone photoresist is used to define etching pattern.

Figure 4.8(b) shows PhC and current-blocking trenches etched in the InP membrane. The pattern, which also includes wire waveguides and grating couplers for some devices, is defined by e-beam exposure using positive tone e-beam resist. Prior to e-beam lithography, SiN_x is deposited by PECVD as a hard mask. After e-beam resist development, pattern is then transferred to SiN_x and InP layers by two dry etching steps.

N metal contacts (Fig. 4.9a) and P metal contacts (Fig. 4.9b) are fabricated on n-InP and p-InGaAs/p-InP, respectively, in two lift-off cycles. Metal combination for N contacts is Ni/Ge/Au, for P contacts is Ti/Pt/Au. Negative tone UV photoresist is used as mask layer. Sample is then annealed at 430 °C by RTA to alloy

the N contacts.

The final fabrication stage is membranization. The thermal SiO_2 layer underneath PhC membrane is wet etched with buffered hydrofluoric acid (BHF) with wetting agent etchant through the PhC holes (Fig. 4.10). Positive tone UV photoresist mask is used to protect the surrounding surface from wet etching, since BHF can etch titanium in P metal contacts and SiO_2 under waveguides and grating couplers.

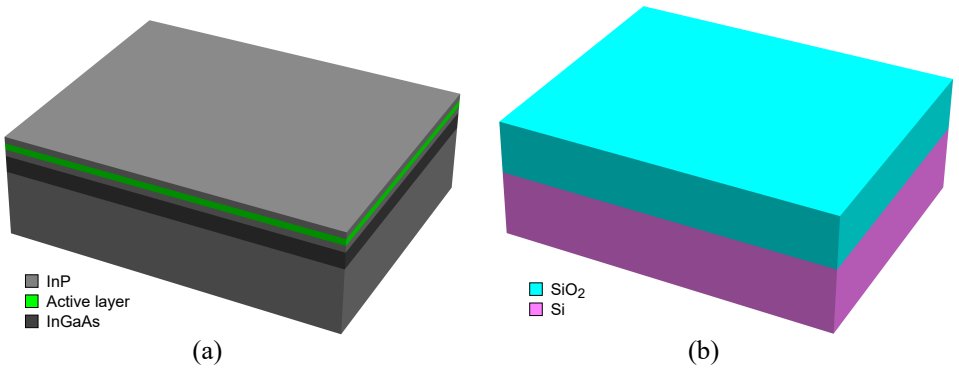


Figure 4.1: (a): InP layer with embedded active material and InGaAs etch-stop layer are grown on InP substrate by MOVPE. (b): Silicon dioxide is grown on Si substrate by thermal wet oxidation.

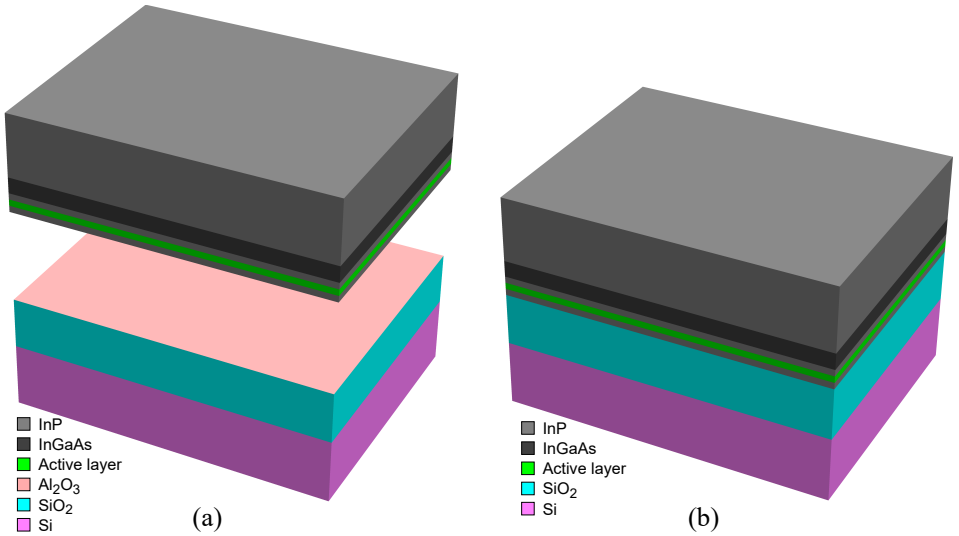


Figure 4.2: (a): Thin Al_2O_3 layer is deposited on both InP and Si wafers by ALD. InP wafer is flipped. Note that Al_2O_3 layer is shown in the schematic with zero thickness due to being very thin ($\sim$2 nm). (b): InP and Si wafers are directly bonded.

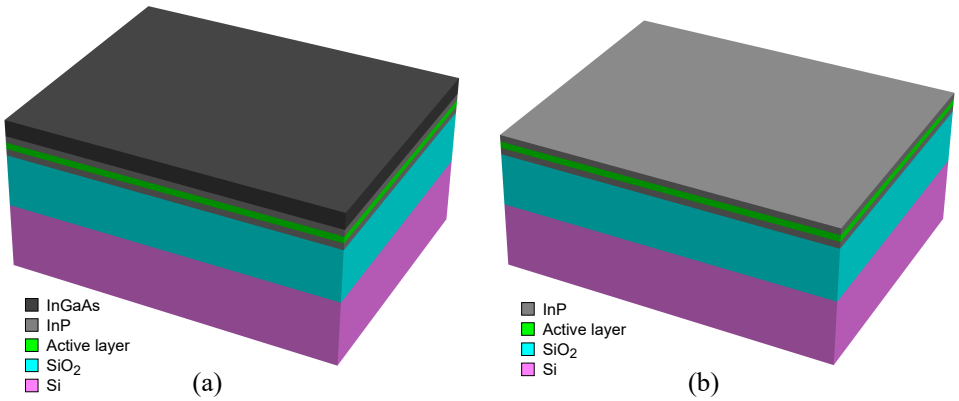


Figure 4.3: (a): InP substrate is selectively wet etched. (b): InGaAs etch-stop layer is selectively wet etched.

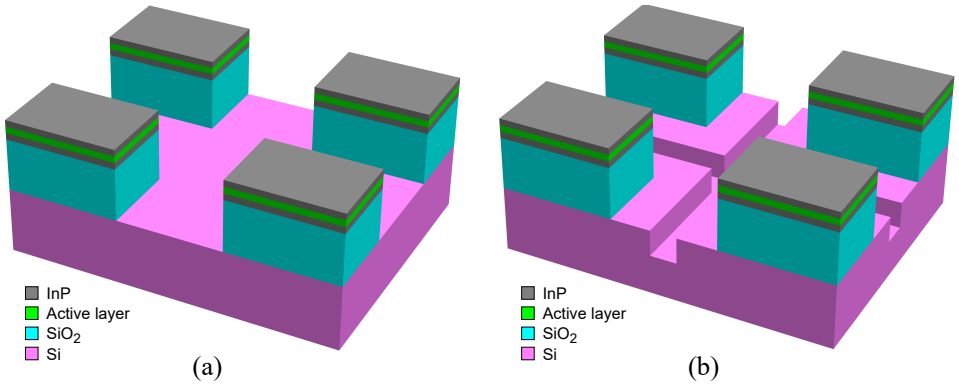


Figure 4.4: (a) Pre-alignment openings are etched in InP with active material and SiO_2. (b) Alignment marks are etched in Si.

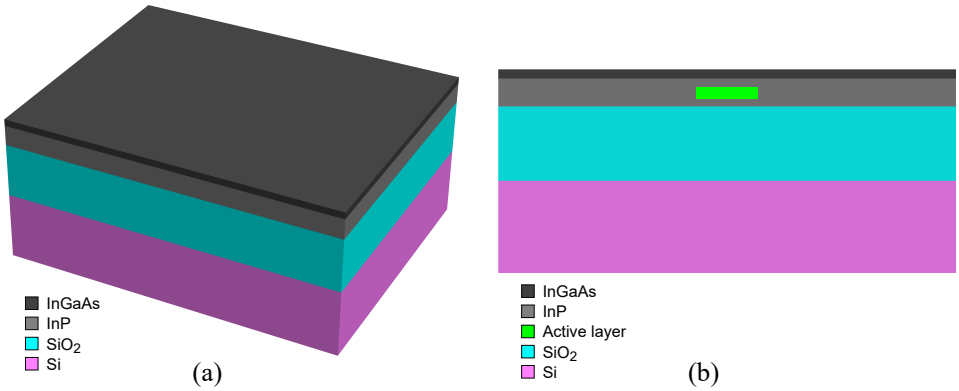


Figure 4.5: (a): BH region with active material is formed inside InP layer. InGaAs layer is grown on top. (b): Cross-section showing active region buried inside InP layer.

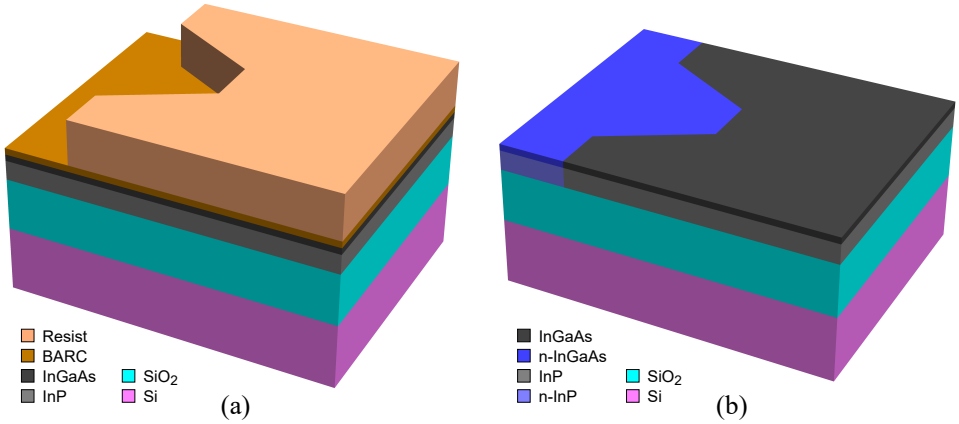


Figure 4.6: (a): DUV photoresist mask is defined for Si ion implantation. (b): DUV photoresist and BARC are stripped after Si ion implantation.

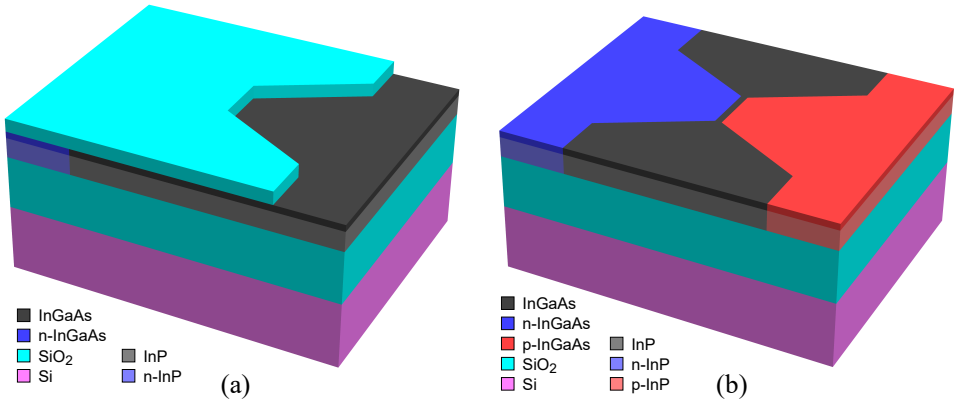


Figure 4.7: (a): SiO_2 hard mask is defined for Zn diffusion. (b): SiO_2 hard mask is stripped after Zn diffusion.

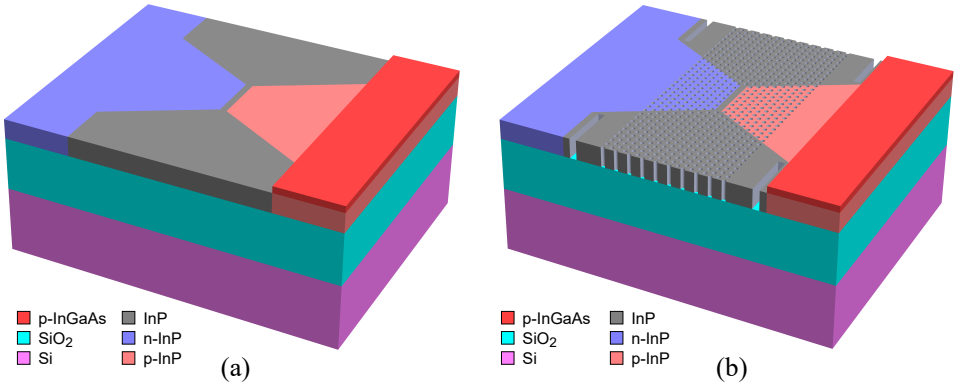


Figure 4.8: (a): InGaAs layer is selectively wet etched everywhere except regions designed for P contacts. (b): PhC pattern and current-blocking trenches are etched in InP.

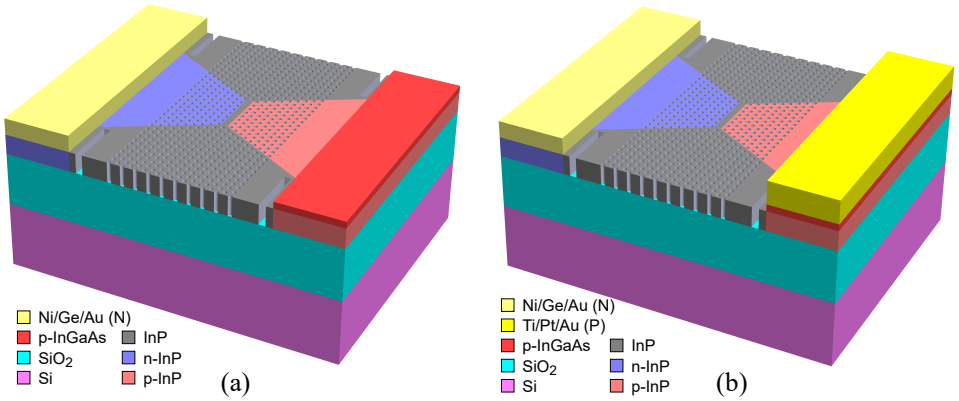


Figure 4.9: (a): N metal contact is formed by lift-off technique. (b): P metal contact is formed by lift-off technique.

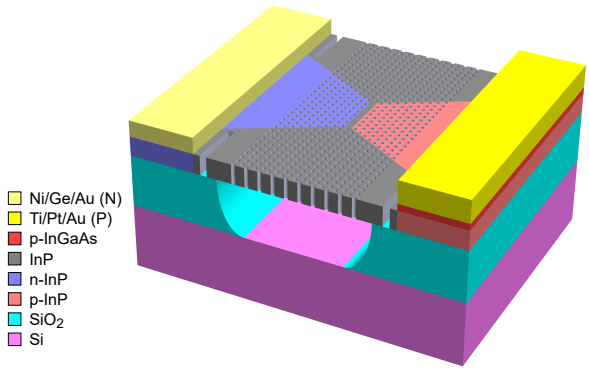


Figure 4.10: Membranization is done by wet etching of SiO_2 layer under PhC membrane.

4.2 Mask design overview

Significant effort has been put on designing the mask layout for NATEC HERO project. The idea is to combine in one process flow fabrication of huge amount of various device types. The limitations of utilized lithography methods (e-beam, DUV, UV) need to be taken into account. Since maximum possible DUV chip size, which is stepped (repeated) on wafer, is determined by DUV reticle size and is 22x22 mm in wafer scale, all design variations need to be confined in this area. In total four DUV chips fit in 2" III-V area of wafer, however, for each chip one corner happens to be outside of 2" III-V area, as shown in Fig. 4.11.[1] The DUV chip, which is shown in more detail in Fig. 4.12(top), is surrounded by 0.5 mm wide frame containing e-beam, DUV and UV alignment marks.

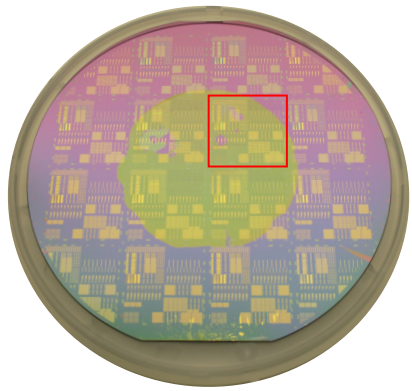


Figure 4.11: Camera image of processed NATEC HERO 2" III-V on 4" Si wafer. One DUV chip is highlighted.

The designed devices can be arranged into three groups: nanolasers, switches and test structures. An example of electrically pumped PhC BH nanolaser with line defect cavity and objective light collection is shown in Fig. 4.12(left). Other variations include nanolasers with Fano mirror cavity. For some devices thermal tuning of Fano mirror by current going through narrow doped channel (heater) is designed. Besides objective light collection, light emission into a wire waveguide with light outcoupling to a fiber through a PhC-based uniform grating coupler, as well as light collection in photodetector fabricated on-chip, are designed. Linewidth measurement configuration is included with output of two nanolasers being interfered and collected in on-chip photodetector. Varied parameters include cavity length, BH length and width, separation between BH and doped regions, PhC and grating coupler hole radii.

[1] This fact imposes the requirement of alignment marks definition not in III-V, but in Si, as further discussed in Subsection 4.3.3.

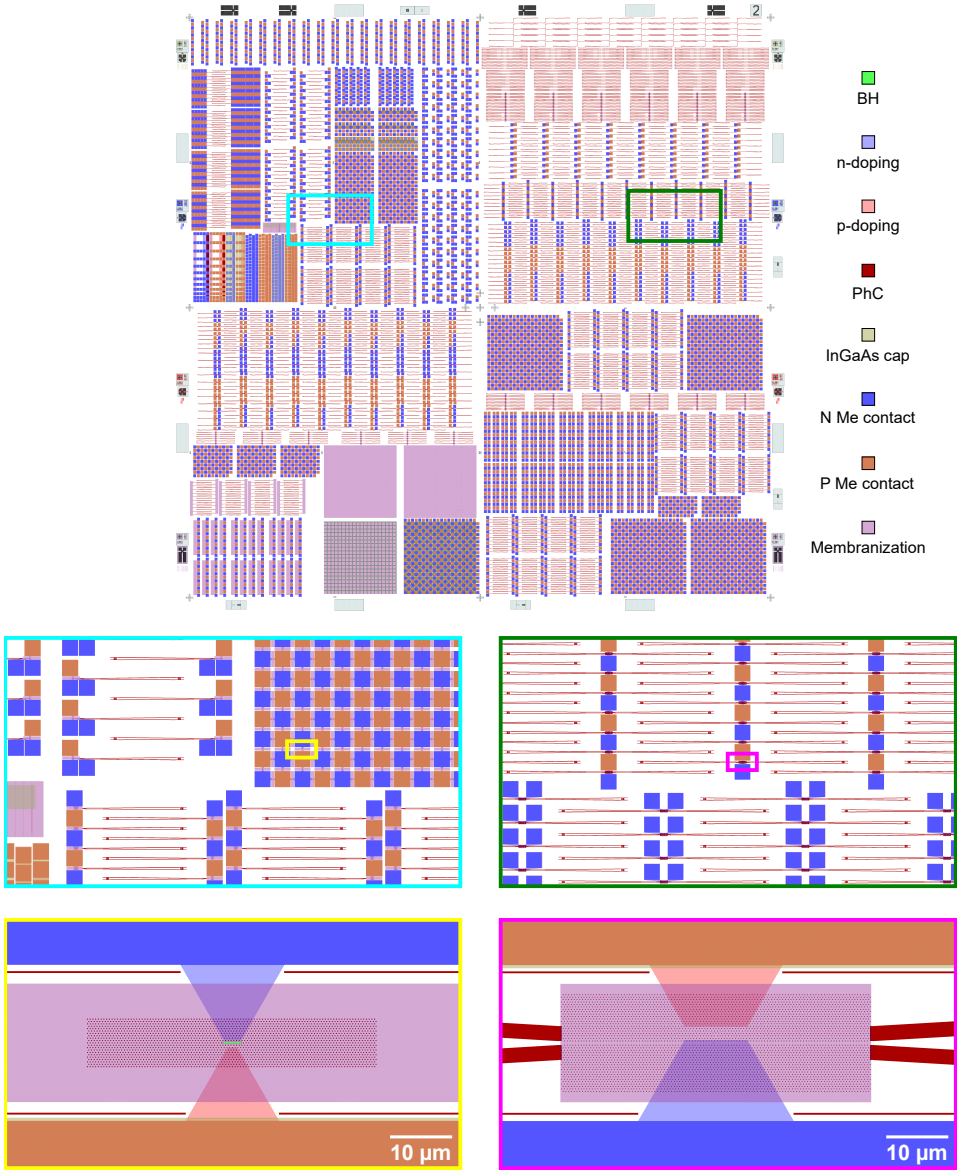


Figure 4.12: Mask design in NATEC HERO project. Top: DUV chip (22x22 mm). Bottom left: electrically pumped BH PhC nanolaser with objective light collection. Bottom right: Fano switch with carrier sweep-out.

An example of optical switch with Fano cavity and carrier sweep-out by electric field in reverse biased lateral p-i-n junction is shown in Fig. 4.12(right). Other design variations include switches with thermal tuning of Fano cavity by heater, as well as with two tuned Fano cavities. Varied parameters are separation between Fano cavity and doped regions, heater doping type, position and length, PhC and grating coupler hole radii.

Test structures include transmission line method (TLM) structure arrays for sheet resistance and contact resistance measurement, TLM-like structures for estimation of lateral dopant redistribution, PhC and wire waveguides with grating couplers, test structures for gain measurement using segmented contact method.

Unfortunately, the first iteration of NATEC HERO sample processing was hindered with arising problems such as p-doped region surface degradation and instability of InP dry etching, so only fraction of designed devices could be tested. However, processing has been improved, and there are high expectations for the next HERO samples.

4.3 Fabrication details

In this section, the detailed description of active samples processing is given. In case of all-passive (Fano switches) and doping test samples, some steps are different or skipped, which is mentioned where applicable.

4.3.1 Epitaxial growth

The initial step of every sample processing done in this work is epitaxial growth of required III-V layer combination on 2" (100)-oriented InP substrate, which is performed in metalorganic vapor phase epitaxy (MOVPE)[2] Emcore Discovery D125 turbodisk system. Since MOVPE plays important role throughout this work during not only initial growth, but also BH regrowth and Zn diffusion, the brief explanation of MOVPE working principle is given.

Figure 4.13 shows the schematic representation of MOVPE system used in this work. During the process, the wafer is located on a heated rotating carrier, which can be changed to fit up to 4" wafer size. The temperature is controlled by emissivity compensated pyrometer. In case of not ideal wafer surface quality, and also in temperature range under 500 °C, a pair of thermocouples is used instead.

Reactive gases are supplied to the reactor chamber by Group III (alkyle), Group V (hydride) and carrier (H_2) gas lines through inlets on the top of the chamber. Reactive species then undergo gas phase and surface reactions and give rise to crystal growth (or diffusion). The exhaust is then pumped to the scrubber

[2]In literature MOVPE is also frequently named as MOCVD (metalorganic chemical vapor deposition). Other names include OMVPE (organometallic vapor phase epitaxy) and OMCVD (organometallic chemical vapor deposition).

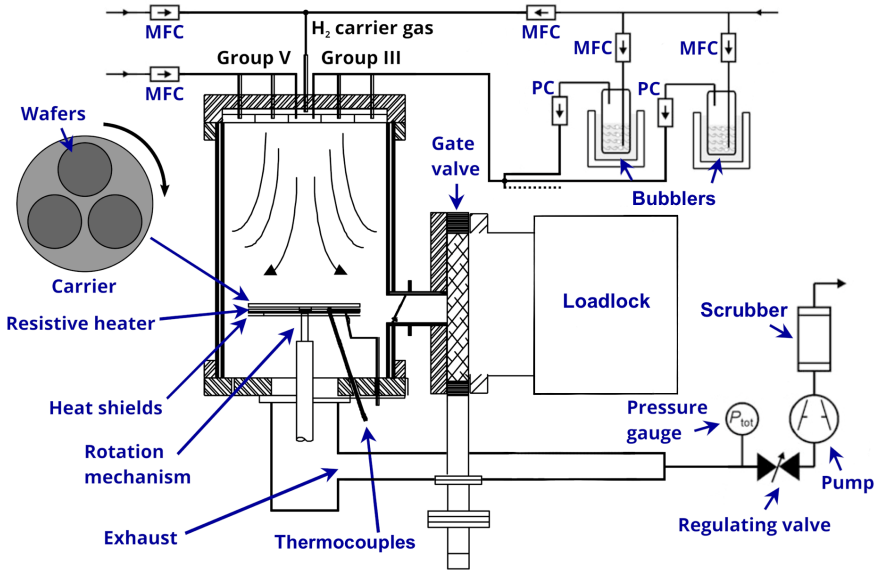


Figure 4.13: Schematic of MOVPE system with vertical rotating disk reactor. MFC stands for mass flow controller, PC for pressure controller. Gas lines are simplified, e.g., dilution schemes are not shown. Adapted from [197].

system where it is filtered from toxic gases. The growth rate is determined, on the one hand, by gas phase mass transport to the surface, and on the other hand, by kinetics of species incorporation at or near the surface. The detailed study of MOVPE complex process dynamics can be found in [198].

Group III gases originate from so called bubblers, where H_2, being a carrier gas, is passed through the reservoir with the corresponding metalorganic compound and is enriched with alkyle vapor. Reservoir temperature has drastic effect on vapor pressure and needs to be controlled. Specifically, malfunction of Zn source thermostatic bath, which was not identified for some time due to seemingly right sensor reading and overall variety of possible problems, resulted in several failed Zn diffusion test batches. Alkyle compounds used in this work are trimethylindium (TMIn, solid, 18 °C), trimethylgallium (TMGa, liquid, −5 °C), trimethylaluminum (TMAl, liquid, 18 °C) and diethylzinc (DEZn, liquid, 18 °C)[3]. Group V precursors are PH_3 and AsH_3, which are gases at normal conditions and do not require bubbler configuration.

[3]Even though DEZn is Group II compound, in MOVPE schematic it is commonly referred as Group III gas.

Different epitaxial layer combinations are grown for various applications. In case of the samples with active material[4], compressively strained InGaAsP quantum wells with tensely strained InAlGaAs barrier are sandwiched between InP layers, which are separated from the substrate by InGaAs etch stop layer, as shown in Fig. 4.1(a). In case of all-passive samples for Fano switches and doping tests, active layer is omitted, instead, there is additional InGaAs layer with corresponding InP etch stop layer. This InGaAs layer, needed for the purposes, discussed in Chapter 5, is later grown during BH regrowth step in case of active samples, but since the whole BH definition stage is omitted for all-passive samples, InGaAs is grown during the initial growth.

The growth of InP and lattice matched InGaAs is carried out at 610 °C in mass transport limited regime under large Group V gas overpressure, so the growth rate and layer compositon can be controlled by adjustment of Group III gas flows.

4.3.2 Direct wafer bonding

As discussed in Section 2.1, integration of III-V material on Si platform is crucial for implementation of active photonic devices in CMOS-compatible chip, which can then benefit from mature large scale silicon industry. In this work, direct wafer bonding process, which is described below, is utilized.

After epitaxial growth, III-V wafer is directly bonded to SiO_2/Si substrate. Prior to bonding, in a separate process thick (1.1 µm) thermal oxide layer is grown on a silicon wafer by wet oxidation at 1100 °C. The silica layer is required for several reasons. It is used as a sacrificial layer etched during the membranization stage to form a free-standing InP photonic crystal membrane. Also, its presence guarantees absence of leakage currents through the substrate during device electrical operation. Furthermore, in the future iteration of device design with light coupling into an underlying Si platform it can be possible to use SiO_2 as an intermediate optical-coupling layer between III-V and Si, as shown in [199, 200].

The direct bonding process requires smooth interfaces and, because of that, it is extremely sensitive to particle contamination. Extra care is taken during wafer handling at this stage, and wafer processing before bonding is minimized as much as possible.

Direct bonding includes the following steps. In the first step a thin (∼2 nm) layer of Al_2O_3 is deposited on both InP and Si wafers by ALD at 250 °C. Al_2O_3 is used as an intermediate bonding layer, because it is characterized by large density of −OH groups [116], which give rise to large number of covalent bonds in the interface, which are responsible for high bonding strength in direct bonding process [112, 113]. After ALD, the InP wafer is flipped and gently pressed against the Si wafer at room temperature. At this step, wafers become pre-bonded to each other. Thirdly, the formed wafer stack is annealed at 300 °C for 1 hour in vacuum with

[4]Growth of samples with active material was performed by Aurimas Sakanas.

applied 2 kN force in a special wafer bonder tool. This is done to further increase bonding strength [117].

After wafer bonding, the InP substrate is removed by wet etching in concentrated HCl for ∼1 hour, leaving only III-V epilayers on SiO_2/Si substrate. Then, the InGaAs etch-stop layer is selectively wet etched by $1H_2SO_4(96\%) : 8H_2O_2(31\%) : 8H_2O$ solution[5]. In case of all-passive samples, which have InGaAs layer for P contacts grown in initial growth, additional InP etch-stop layer is also selectively wet etched by $1HCl(37\%) : 4H_3PO_4(85\%)$ solution [201].

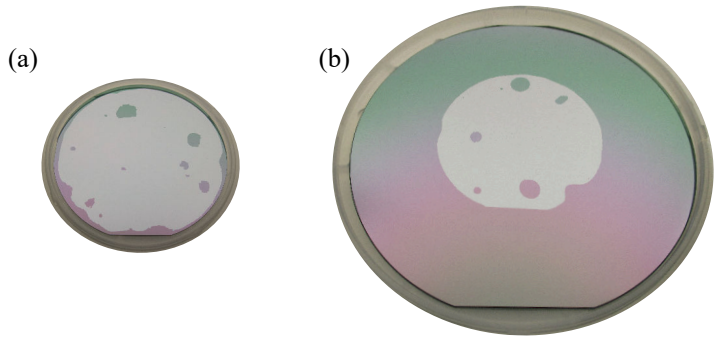
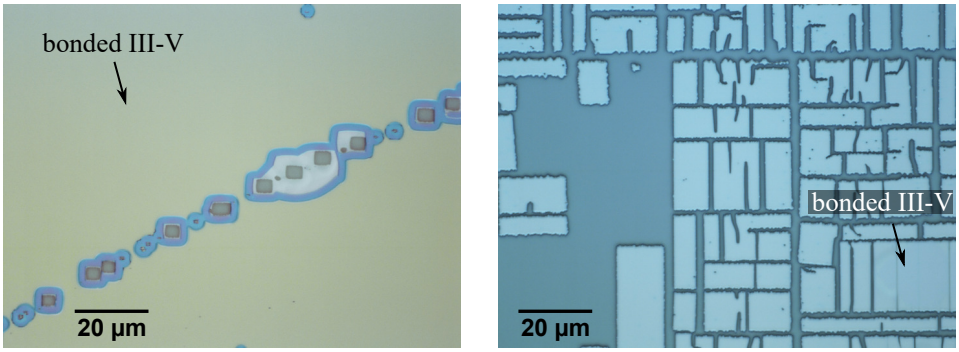


Figure 4.14: Camera images of the samples after substrate and etch-stop removal. (a): 2" InP bonded to 2" Si. (b) 2" InP bonded to 4" Si. Good surface area yield is achieved.

Early experiments were done with 2" InP bonded to 2" SiO_2/Si substrate (see Fig. 4.14a). After transition from UV to DUV lithography for mask patterning at doped region definition stages, bonding to 4" SiO_2/Si substrate was developed (see Fig. 4.14b) in order to fulfill the limitations imposed by DUV stepper tool. Moreover, e-beam alignment is expected to be more accurate on large 4" samples compared to 2" or chip-sized samples [197].

As can be seen in Fig. 4.14, bonded area yield is large, however, it is not 100%. Macroscopic bonding defects (voids) can be seen, which are caused by particles residing on wafer interfaces during bonding. Furthermore, in case of not perfectly lattice matched III-V epilayers, the accumulated stress can result in microscopic void formation, as shown in Fig. 4.15.

[5]In the following text, in case of omitted concentration values, concentrated chemical substances are meant, if not mentioned otherwise.



(a) (b)

Figure 4.15: Optical microscope images of III-V epilayers bonded to Si after substrate removal in case of (a) moderate lattice mismatch for InGaAs etch-stop layer and (b) severe lattice mismatch. Defects are aligned along crystallographic directions.

4.3.3 Alignment marks

When the processing involves several lithography steps, proper alignment of different patterns relative to each other is important. Requirements for the alignment can vary depending on a particular situation. In our case, alignment of some stages (InGaAs etching, N and P metal contacts, membranization) is not too critical, which, together with large size of patterned structures, allows the use of ordinary UV lithography with ∼1 µm alignment accuracy at that stages. However, the BH gain region position needs to be accurately located in PhC cavity with misalignment being at least less than 100 nm to ensure efficient laser operation. Doped regions position relative to BH is also very important in order to inject carriers only in the gain material region to reduce threshold current and to increase modulation speed by reduction of ambipolar diffusion time. Taking this into account, patterning of doped areas is done with DUV lithography since feature size can be relatively large, but BH and PhC patterns are defined with e-beam lithography due to feature size being on the order of 100 nm. Furthermore, strict alignment requirements impose constraints on the quality of alignment marks.

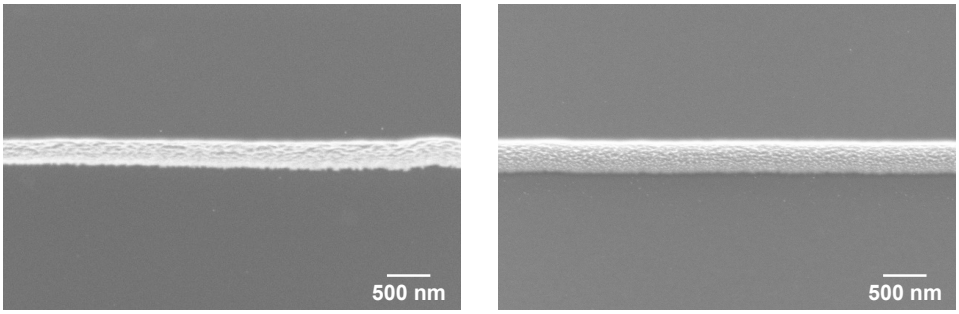
In early runs alignment marks were etched in the InP layer. This approach had the advantages of high contrast between InP and underlying SiO_2 during mark detection in e-beam lithography, and simple process flow. However, due to not 100% bonding yield, some alignment marks could happen to be located in not bonded region with no InP material. Due to that, considerable amount of backup alignment marks was included in mask design, which reduced useful wafer area. Moreover, in case of the latest mask design (see Section 4.2), some alignment

marks have to be located outside of bonded InP area, thus making etching in InP impossible. In order to overcome this problem, the strategy of first, etching of pre-alignment openings in top InP and SiO_2 layers, and second, actual alignment marks etching in Si inside pre-alignment openings, is implemented. In principle, alignment marks could also be etched in SiO_2, but then they would degrade during subsequent processing at BHF wet etching steps. Another possibility is alignment marks definition in Si prior to bonding, but since direct bonding process is highly sensitive to any kind of contamination, all wafer processing and handling prior to bonding is minimized as much as possible.

Pre-alignment openings require only approximate position and dimension control, so they can be wet etched in III-V layer using a combination of $1HCl : 4H_3PO_4$ and $1H_2SO_4 : 8H_2O_2 : 8H_2O$ with hard baked positive photoresist AZ 5214E (Microchemicals) mask, defined by UV lithography. Inductively coupled plasma (ICP) etching using HBr chemistry at 120 °C was also tried as more simple one step process, but the etch rate of QW layers was too low. Increasing etching temperature would overcome this problem, but that would require pattern transfer from photoresist to a hard mask, unnecessarily complicating the process flow. After III-V etching, most of the 1.1 µm SiO_2 is etched by ICP with CF_4/H_2 chemistry, and the remaining ∼0.1 µm is wet etched by BHF to ensure not to degrade the Si surface.

Alignment marks, used in this work, have critical dimension 2 µm, so they can be defined using ordinary UV lithography. Since the alignment mark position search in both e-beam writer and DUV stepper occurs by alignment mark edges detection, absolute dimensions are insignificant, with the position of alignment marks relative to each other being important. However, most common photomask material soda lime glass in this case is unfavorable due to large thermal expansion coefficient ($8.2 \times 10^{-6}\,K^{-1}$) [202], which would result in ∼40 nm deviation from the design across 2" just because of 0.1 °C variation. Quartz with one order of magnitude lower thermal expansion coefficient is used instead.

Alignment marks are etched in the Si substrate with SF_6/O_2 chemistry in a ICP dry etching tool with AZ 5214E photoresist mask. Even though anisotropic Si dry etching is a well-established process [203], it had to be optimized due to prohibition of III-V samples processing in Si-dedicated equipment according to cross-contamination rules in DTU Nanolab facility. Scanning electron microscope (SEM) images of alignment mark sidewalls (Figure 4.16) show the result of Si etching optimization in III-V-dedicated ICP tool. The optimized etching recipe can be found in Appendix A.



(a) (b)

Figure 4.16: SEM images of alignment mark sidewalls in case of (a) not optimized and (b) optimized Si ICP dry etching.

4.3.4 Buried heterostructure

In order to achieve high optical mode and carrier confinement, the buried heterostructure (BH) approach is implemented[6]. After short treatment in BHF for proper resist adhesion, high resolution negative tone e-beam resist hydrogen silsesquioxane (HSQ) is spin coated and baked on the wafer. Then, the BH pattern is defined in the HSQ layer by e-beam exposure and resist development in AZ 400K developer. The next step is ICP dry etching of InP and active layers in unmasked area with HBr chemistry at 180 °C. A thin bottom layer of InP is left unetched to facilitate subsequent regrowth. Then, selective area growth of InP is done by MOVPE, thereby substituting previously dry etched active layers by passive InP in unmasked area. No growth takes place in glass-like exposed HSQ covered regions. After a HSQ mask strip by BHF wet etching, the second MOVPE growth is done on entire surface to planarize the surface, to bring the InP membrane thickness up to designed 250 nm value and to add InGaAs layer needed for subsequent doping processes. In case of all-passive samples, the whole BH definition stage is skipped.

Special attention is brought to the problem of alignment marks conservation during MOVPE regrowth steps, since they can be affected by the InP grown on top. Alignment marks, which are etched in Si, are covered using exposed HSQ to inhibit possible III-V growth on Si. This protection almost works in case of alignment marks, located inside the bonded wafer area, e.g., surrounded by an InP surface. SEM images in Fig. 4.17 show that in this case alignment marks are mostly free from III-V, with only some InP crystallites located on alignment marks edges. The fact of InP growth on the edges gives evidence of not good enough step coverage by HSQ due to insufficient thickness (HSQ is only 350 nm thick compared

[6]BH e-beam lithography, dry etching and two MOVPE regrowth steps were developed and performed by Aurimas Sakanas. Detailed discussion can be found in [197].

to 1 µm deep alignment marks).

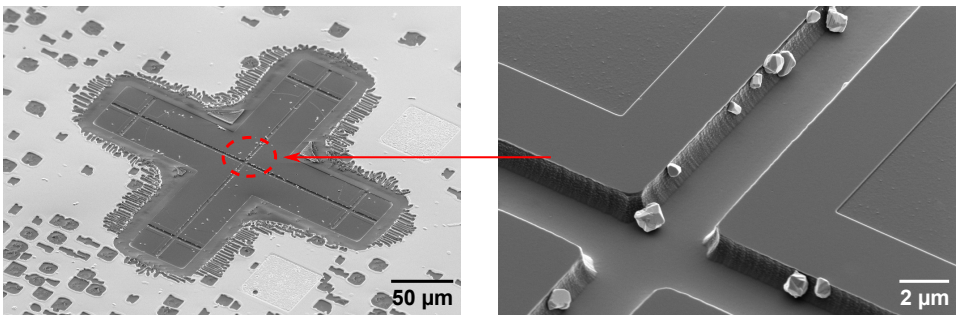


Figure 4.17: SEM images of alignment mark in **bonded** wafer area (surrounded by InP) after BH definition stage.

However, the problem of bad step coverage becomes much more pronounced as seen from the huge amount of III-V material grown on top of alignment mark located outside of bonded area, e.g., surrounded by SiO_2 (see Fig. 4.18). Drastic difference from the case of the mark in bonded area can be explained by the absence of III-V growth on surrounding not bonded SiO_2 surface together with the migration of source species from SiO_2 to not perfectly covered Si edges.

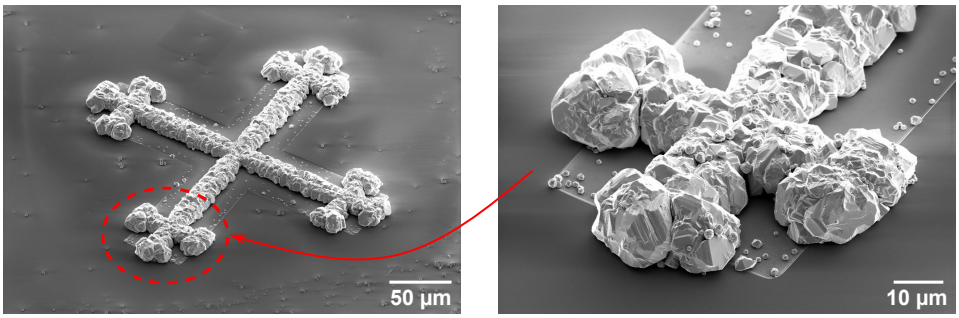


Figure 4.18: SEM images of alignment mark in **not bonded** wafer area (surrounded by SiO_2) after BH definition stage.

Since there is no freedom to increase HSQ thickness, which should be kept small to ensure high resolution of BH pattern, III-V material grown on top of alignment marks is removed by prolonged (∼30 min) wet etching using InGaAs-etching $1H_2SO_4 : 8H_2O_2 : 8H_2O$ and InP-etching $1HCl : 4H_3PO_4$ solutions. The useful III-V area is protected during wet etching by thick (4.2 µm) AZ 5214E photoresist layer, which is patterned using the photomask from pre-alignment openings definition step. To increase photoresist durability against wet etchant attack, it is

hard baked at 130 °C. The resulting cleaned alignment marks after stripping of photoresist are shown in SEM images in Fig. 4.19.

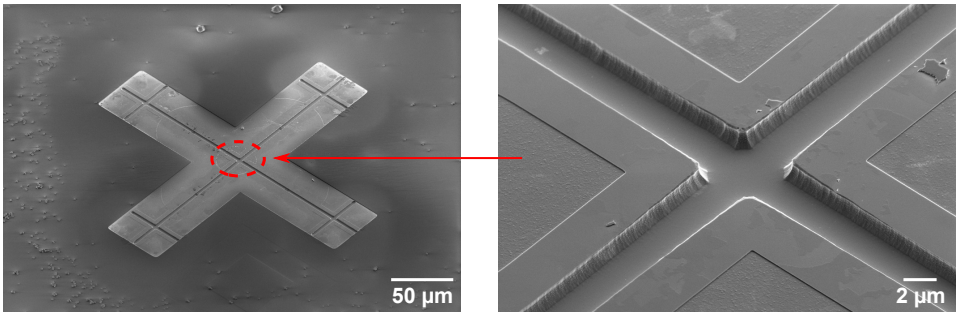


Figure 4.19: SEM images of alignment mark in **not bonded** wafer area (surrounded by SiO_2) after cleaning step.

4.3.5 Doping and InGaAs removal

In order to achieve high alignment accuracy of the p-i-n junction position required for efficient carrier injection, ordinary UV lithography cannot be used since routine ∼1 µm alignment error is too large. By implementation of Vernier scales as alignment marks, accuracy can be improved down to ∼0.25 µm [204], but still this is a large value. Moreover, UV lithography has an inherent resolution limitation of ∼1 µm, which for some design variations is not enough. For example, in case of devices with thermo-optical tuning, the width of doped channels (heaters) should be less than 1 µm, including the effect of lateral dopant redistribution. E-beam lithography could be used for doped regions definition, but it is very expensive and time consuming in case of large area definition, even at the maximum possible beam current. DUV lithography is the optimal and robust method to define doped regions since it can provide alignment accuracy better than 50 nm and resolve fine features down to 300 nm. But there is a limitation of wafer size that can be used in DUV stepper tool used in this work (Canon FPA-3000 EX4): it is designed for 6” and 8” wafer handling with the possibility of 4” wafer use in special adapter. In this work 4” Si substrate size is used because of limitation on maximum wafer size imposed by MOVPE tool used for BH regrowths and Zn diffusion.

DUV lithography cycle involves the following steps. First, 65 nm of conformal BARC DUV42S-6 (Brewer Science) and 750 nm of chemically amplified positive tone DUV photoresist JSR-M35G (JSR) are spin coated and soft baked on the wafer. The BARC layer is required to inhibit substrate reflectance and thin film light interference due to high sensitivity of chemically amplified photoresist to those effects. Second, the wafer is aligned on the DUV stepper stage using coarse and fine

alignment marks. Chips with 22x22 mm size are exposed one by one with a KrF (248 nm) excimer laser through the reticle and 5:1 projection optics. DUV exposure is then followed by post-exposure bake (PEB) step at 130 °C, which is required for acid-catalyzed activation of the exposed photoresist [205], and development in 2.38% water-based tetramethylammonium hydroxide (TMAH).

Doped regions in InGaAs/InP are then formed by Si ion implantation for n-type and Zn diffusion for p-type. In the mask designs offsets are made to compensate for lateral redistribution of corresponding dopants. Detailed description of doping processes and challenges related to them is given in Chapter 5.

After doping, InGaAs layer is selectively wet etched using $1H_2SO_4 : 8H_2O_2 : 8H_2O$ solution in all sample surface except for pads for the future P-type metal contacts. Mask design is adjusted to account for resist layer undercut occurring during wet etching. Mask is defined with UV lithography. First, the wafer is primed by immersion in SurPass 3000 adhesion promoter (DisChem). Then, 1.5 µm thick positive tone AZ 5214E photoresist is spin coated and soft baked. The wafer is then aligned and exposed with 365 nm UV Hg-Xe lamp. After photoresist development in 2.38% water-based TMAH, it is hard baked at 130 °C for better durability during wet etching. Last step before wet etching is descum (short low power plasma ashing in O_2 to remove possible resist residues in mask openings).

4.3.6 Photonic crystal and trenches

The PhC pattern, as well as current-blocking trenches, wire waveguides and grating couplers are defined by means of e-beam lithography[7]. In order to achieve high quality factor values for optical cavities in PhC, etched holes need to be smooth, well-defined with circular shape and with vertical sidewalls. This imposes high requirements on the process of holes definition and dry etching.

Since lithography resolution plays crucial role in PhC holes definition, high resolution positive tone e-beam resist ZEP (ZEP520A) is used. Previous work with ZEP usage [206] reported critical problem of unability of ZEP to withstand InP reactive ion etch (RIE) process, resulting in ZEP foaming and very poor quality etch. Due to this, utilization of PECVD silicon nitride hard mask became a standard for PhC fabrication [136, 197, 207].

The process starts with PECVD deposition of 100 nm SiN_x layer. Then, ZEP resist is spin coated and baked on the wafer, resulting in ∼500 nm thickness. The wafer is aligned and exposed in e-beam writer tool (JEOL JBX-9500FS). Resist is then developed using ZED N50 developer. Pattern is transferred from ZEP layer to SiN_x hard mask layer by dry etching with CHF_3/O_2 chemistry. ZEP resist is then stripped. Pattern is further transferred to InP layer by either ICP dry etching process with HBr chemistry at 180 °C, or by RIE cyclic process at

[7] PhC design, e-beam lithography and dry etching were performed by Aurimas Sakanas (active samples, lasers) and Dagmawi Alemayehu Bekele (passive samples, switches).

room temperature with CH_4/H_2 etching steps alternating with O_2 polymer cleaning steps. After processing, the nitride hard mask layer is not removed, since unmasked wet etching with BHF would undercut InP wire waveguides, lying on thermal SiO_2 layer. Nitride located on top of the PhC membrane is later etched during the membranization stage (Subsection 4.3.8).

The hole radius is the critical parameter, because even small size variation causes a shift of the resonance wavelength range of the fabricated devices. The difficulty of controlling the hole radius arises from the fact that many factors influence it, e.g., e-beam exposure dose, resist development, SiN_x and InP dry etching. The final hole size is typically ∼1.3x larger than designed, therefore, the mask design needs to be adjusted to compensate for the hole widening.

The stage of PhC dry etching turned out to be the limiting factor for obtaining the working devices. Significant difficulties related to the reproducibility of the PhC and grating coupler definition process resulted in many samples being failed, including the discussed in Chapter 7 Fano switches with n-type InP doped by means of Si ion implantation. The requirement of the wide range variation of both PhC and grating coupler airhole radii in order to increase the probability to hit the targeted values resulted in a drastic decrease of a number of potentially useful devices. Additional difficulty consisted in the transfer from small chip processing to 4" wafer processing under the frame of NATEC HERO project, with the need to reoptimize the dry etching procedures.

In case of the samples intended for doping tests only, PhCs are not defined, however, current-blocking trenches are still required for current confinement in TLM test structures (Subsection 4.5.1) and p-i-n junction test structures. Since there are no high requirements for trenches definition, the mask is defined using standard UV lithography with positive tone photoresist AZ 5214E, and the SiN_x hard mask is not used.

4.3.7 Metal contacts

Fabrication of metal contacts is done by means of the lift-off technique and UV lithography. First, the wafer is primed by hexamethyldisilazane (HMDS) vapor. HMDS can be used instead of SurPass 3000 for adhesion promoting since almost all the surface is covered by the SiN_x layer left after the PhC definition stage. Then, negative tone UV photoresist AZ nLOF 2020 (Microchemicals) is spin coated and soft baked. After alignment and UV exposure, PEB step is done at 110 °C to cross-link exposed photoresist. Not exposed resist is then developed by 2.38% water-based TMAH single puddle. To improve resist durability during subsequent SiN_x wet etching, resist is flood exposed and hard baked at 150 °C. However, since photoresist layer is to be removed during lift-off process, there is a trade-off between durability during wet etching and easiness of removal during lift-off. The next step is descum plasma ashing of possible resist residues.

Since the nitride hard mask layer is left on top of the III-V material after the PhC definition, it needs to be removed in areas designed for metal contacts to ensure electrical connection. SiN_x is wet etched by BHF. It is important to make sure that no SiN_x is left after etching. Since the exact etch rate value can fluctuate, etching end point is verified by inspecting color of mask opening in optical microscope, as shown in Fig. 4.20: no color change after another BHF interval implies that III-V surface is reached.

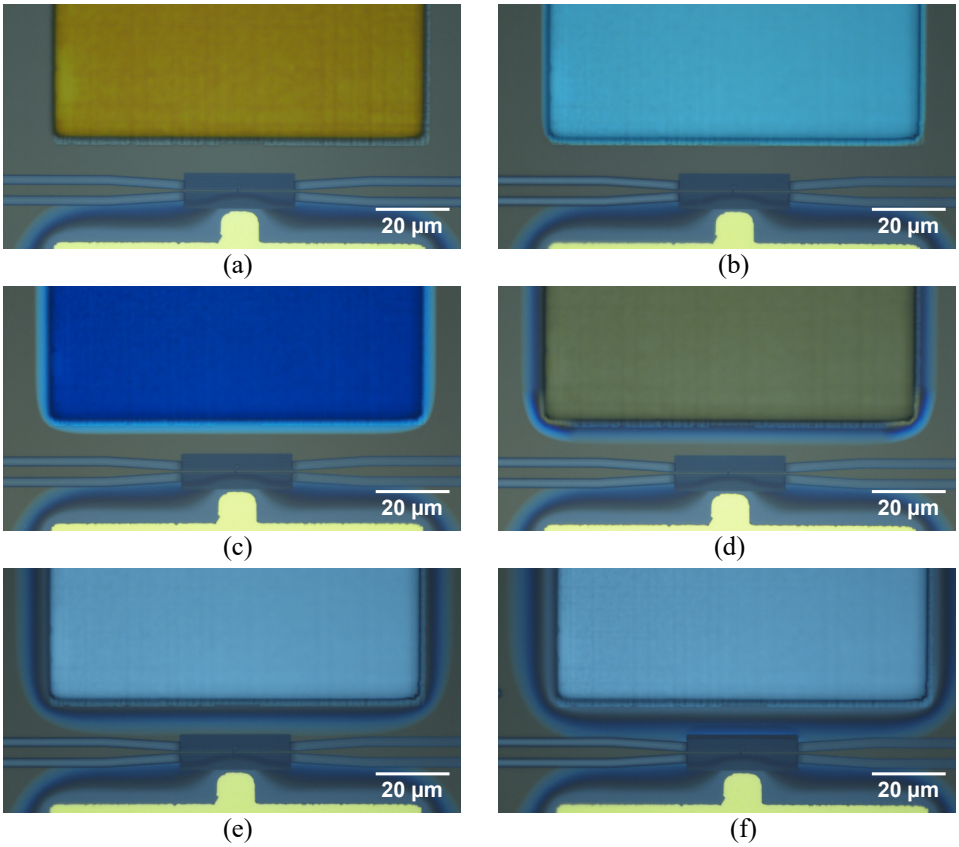
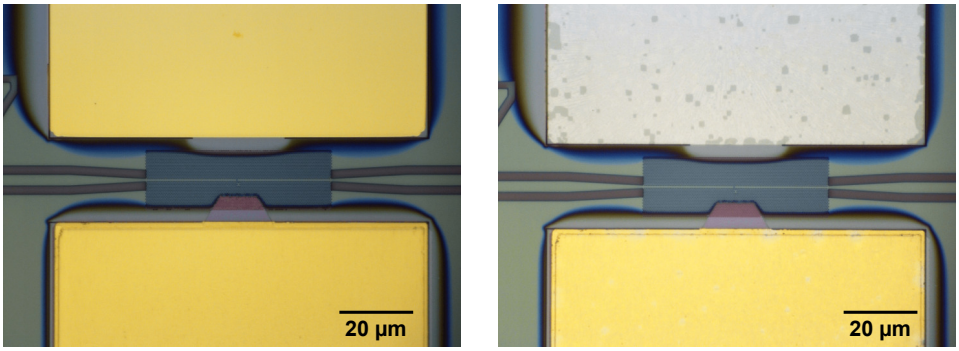


Figure 4.20: Optical microscope images of photoresist mask opening for P metal contact. (a): Before SiN_x wet etching, (b): after 1 min of BHF, (c): 2 min of BHF, (d): 3 min of BHF, (e): 4 min of BHF, (f): 5 min of BHF. No color change between (e) and (f) constitutes absence of SiN_x layer in mask opening. Gradually increasing mask undercut can be seen.

After SiN_x etching, the required metal combination is deposited by e-beam

evaporation. Ni/Ge/Au (40 nm/50 nm/125 nm) is used to make contact to n-InP, and Ti/Pt/Au (30 nm/50 nm/250 nm) to p-InGaAs/p-InP, as these combinations are known to produce good quality ohmic contacts [208]. Then, lift-off of metal and resist in masked regions is done in Remover 1165 (Dow Chemicals). The whole processing cycle is repeated two times for N and P metal contacts.

In order to form ohmic contact between Ni/Ge/Au and n-InP, contact needs to be alloyed [208]. This is done by rapid thermal annealing (RTA) of the sample at 430 °C for 30 s. Annealing is done under N_2 flow to prevent oxidation at high temperature. The ohmic contact is formed by decomposition of the ternary Ni-In-P phase at the InP surface with the formation of Ni_xP, Au_xIn_y phases and Ge doping of top InP layer [209]. Alloying can be visually checked by inspecting color of N contact: as shown in Fig. 4.21, after RTA previously yellow contact turns white. Ni/Ge/Au metal contacts are known to suffer from metal spiking issue [210], but in the scope of this work it is of lesser importance due to lateral geometry device configuration.



(a) (b)

Figure 4.21: Optical microscope images of metal contacts (a) before and (b) after RTA at 430 °C for 30 s. Change of N contact color from yellow to white indicates successful alloying of Ni/Ge/Au.

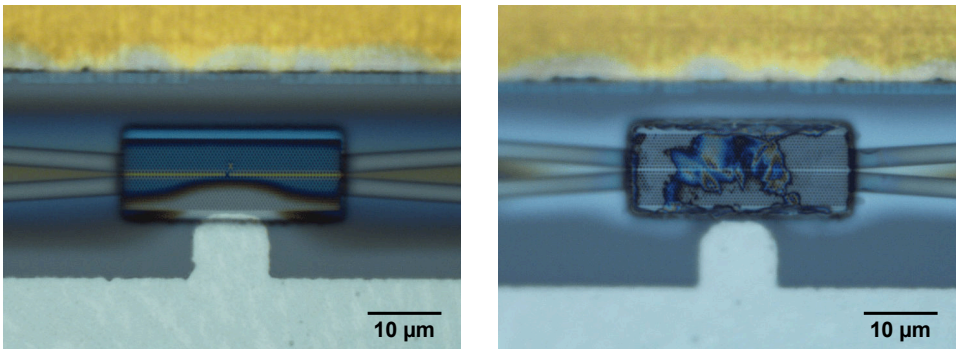
The fact, that top InP layer under the N contact pads becomes heavily n-doped due to Ge diffusion, allows the formation of a p-i-n junction in InP even without Si ion implantation for n-doping. However, the i-region becomes very large, which may degrade device performance. But, since ion implantation is not available in-house, for early sample batches it was skipped with p-i-n junction still being fabricated.

4.3.8 Membranization

The final stage in device fabrication is membranization. Its purpose is to release PhC membrane by wet etching of the underlying thermal SiO_2 layer with SiOetch

wet etchant (BHF with wetting agent) through the PhC holes. The remaining SiN_x layer on top of the PhC membrane is also etched. In order to protect the SiO_2 under InP wire waveguides and grating couplers, as well as the titanium in P metal contacts, from BHF attack, a AZ 5214E hard baked mask is defined by UV lithography.

Wafer position during wet etching is found to be the important factor. In case of horizontal wafer position in the etching solution, thin resist residues occasionally appear inside membranization windows, as shown in Fig. 4.22. This happens due to resist being attacked by wet etchant for prolonged period of time (7–10 min depending on oxide thickness). Resist residues are unwanted due to possibility of random partial masking of PhC membrane and, as a consequence, not controlled non-uniform etching. However, resist residues build-up in mask openings is avoided by the use of vertical wafer holder during wet etching. In this case, residues most probably float away from the wafer instead of gravity-assisted congregating.



(a) (b)

Figure 4.22: Optical microscope images of membranization window (a) before wet etching and (b) after wet etching in case of sample placement in horizontal holder.

In order to fit the sample on the relatively small measurement setup stage, it is cleaved into small chips after photoresist mask definition. The cleaving is done before membranization wet etching step, because the cleaving process may harm potentially fragile free-standing membranes. After photoresist stripping, the chips are taken out from the cleanroom for the measurements.

4.4 Effect of high temperature annealing on active material properties

As discussed in detail in Subsection 5.1.2, activation of Si impurities after Si ion implantation involves annealing at temperature in 650–800 °C range. This high

temperature treatment can affect the active material properties. In order to investigate this, a QW sample bonded to SiO_2/Si is cleaved in pieces and annealed with different parameters. The active material is one layer of InGaAsP QW with InAlGaAs barrier layers embedded in InP. Total thickness of III-V membrane is 175 nm.

The most convenient way to characterize active material quality is photoluminescence (PL) measurement. Change of PL peak intensity and/or wavelength after the annealing can give the information about the condition of active material. PL measurement is performed before and after the annealing under optical pumping with a CW laser at 532 nm wavelength at room temperature. The QW before the annealing exhibits maximum in PL intensity in 1520–1530 nm range, the slight variation is most likely caused by minor composition and thickness non-uniformity across the wafer.

In the first place, the effect of annealing temperature on PL signal is investigated. Prior to annealing, the samples are coated by PECVD-deposited borophosphosilicate glass (BPSG) 100 nm layer to prevent InP thermal decomposition. Annealing is done in RTA tool under N_2 atmosphere with 15 K/s ramp rate on both heating and cooling steps, however, actual cooling ramp rate is lower than setpoint and temperature-dependent.

The resulting PL spectra are shown in Fig. 4.23. After annealing at 650 °C, PL peak intensity drops to 36% of the initial value (Fig. 4.23a). Annealing at higher temperatures gives even larger PL decrease, with 13% of the initial intensity remaining after 700 °C annealing and 3% after 750 °C (Fig. 4.23b,c). After 800 °C annealing, PL signal disappears completely (Fig. 4.23d). This behavior can be explained by QW degradation due to dislocations formation in III-V membrane caused by thermal strain [33]. Significant mismatch of thermal expansion coefficients of InP ($4.48 \times 10^{-6}\,K^{-1}$) and Si substrate ($2.57 \times 10^{-6}\,K^{-1}$) [211] is the reason for thermal strain. However, such drastic decrease in PL intensity is surprising given the small thickness of III-V membrane, being 175 nm.

Since the fabrication process involves several steps, which require annealing at not less than 650 °C (Si activation, BH MOVPE regrowth), further investigation of QW thermal stability is conducted at 650 °C. The effect of heating and cooling ramp rate during RTA is investigated. As can be seen in Fig. 4.24(a-c) and Fig. 4.23(a), no trend is observed in degree of degradation after annealing with ramp rates in 1–15 K/s range. PL peak intensity after annealing constitutes ∼40% regardless of used ramp rate.

In another experiment, the sample is annealed not by RTA, but in MOVPE reactor at 650 °C for 15 min. Instead of BPSG capping layer deposition, PH_3 atmosphere is used for InP protection. Ramp rate is 1 K/s. As can be seen in Fig. 4.24(d), degree of QW degradation is the same as in case of RTA annealing, with PL peak intensity being ∼40% from the initial. This fact gives evidence of QW degradation dependence only on annealing temperature, with annealing method,

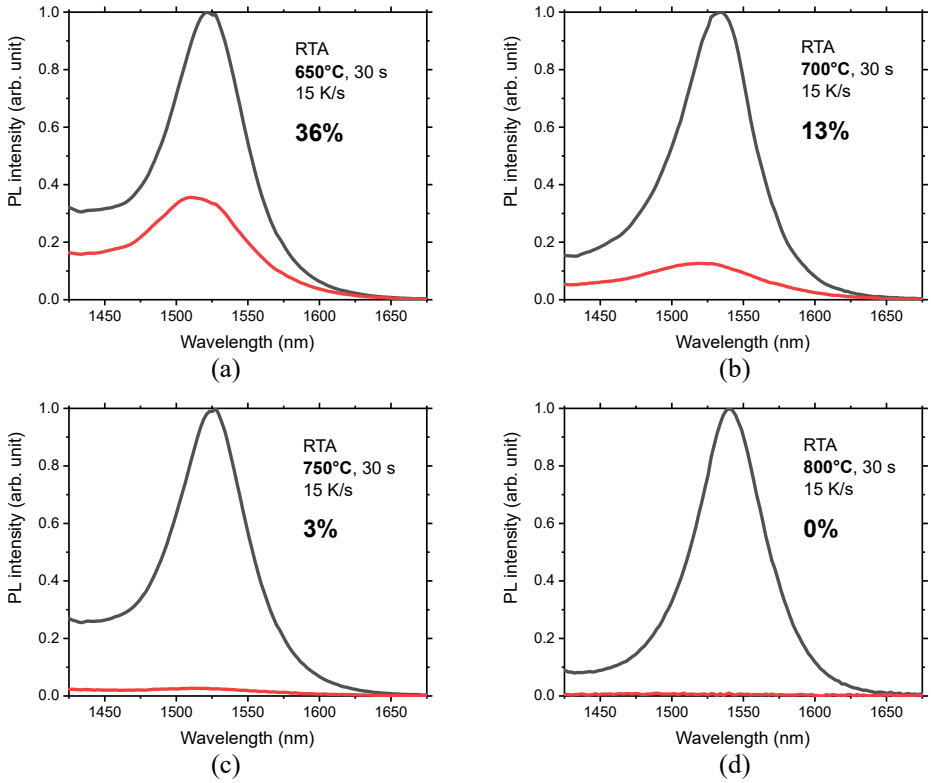


Figure 4.23: PL measurement data for QW samples on SiO_2/Si before and after RTA at different temperatures: (a) 650 °C, (b) 700 °C, (c) 750 °C, (d) 800 °C. Data is normalized relative to PL intensity before annealing. Duration of annealing is kept at 30 s, ramp rate is 15 K/s. Prior to annealing, BPSG capping layer is deposited to protect InP from decomposition.

III-V protection method and ramp rate having no effect. Furthermore, subsequent annealing of the same sample the second time in MOVPE with the same parameters does not induce further damage, with PL signal staying at approximately the same level (Fig. 4.24d).

It should be noted that in all cases slight ∼10 nm blue shift of PL peak wavelength is observed after annealing. It could be explained by QW intermixing, however, this contradicts with the fact that the peak wavelength stays the same after the second annealing, as shown in Fig. 4.24(d).

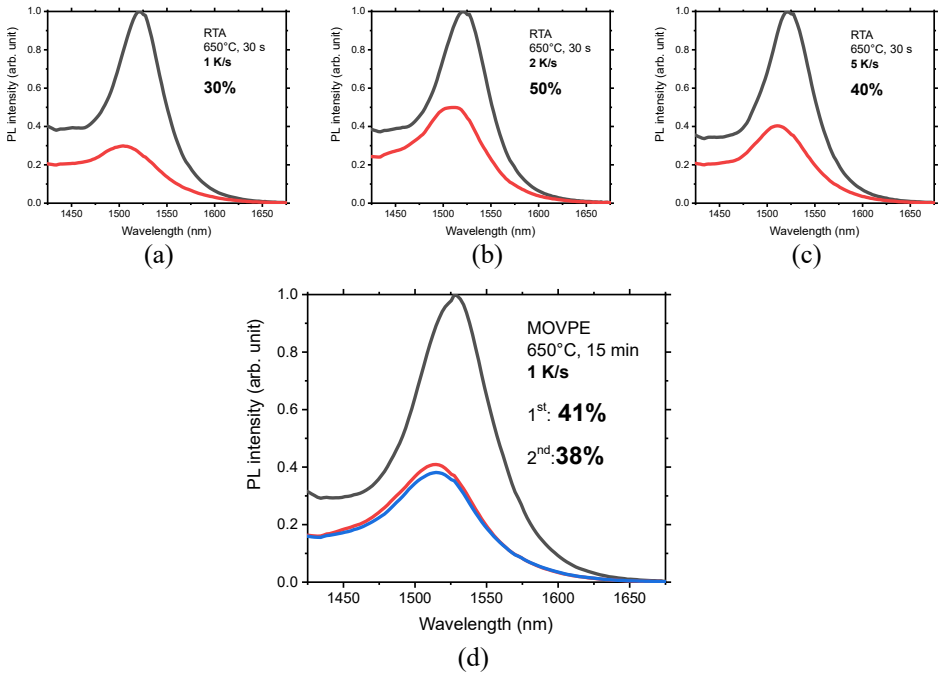


Figure 4.24: PL measurement data for QW samples on SiO_2/Si before and after RTA at 650 °C for 30 s with different ramp rates: (a) 1 K/s, (b) 2 K/s, (c) 5 K/s. Prior to annealing, BPSG capping layer is deposited to protect InP from decomposition. (d): PL measurement data for the sample annealed two times in MOVPE under PH_3 atmosphere at 650 °C for 15 min with ramp rate 1 K/s. For all graphs data is normalized relative to PL intensity before annealing.

4.5 Electrical characterization

4.5.1 Transmission line method

Considerable part of this work is related to development and optimization of doping technologies of InP. It is important to be able to get quantitative data on electrical properties of doped InP. Moreover, metal-semiconductor contacts need to exhibit ohmic behavior to both n-InP and p-InP with sufficiently low contact resistance. In this work, the transmission line method (TLM) is implemented as a method to characterize electrical properties of doped semiconductor material and metal-semiconductor contacts.

The schematic of a test structure that can be used for TLM measurements is shown in Fig. 4.25. It consists of the array of the metal contacts with fixed width W

separated by different lengths $L_1, L_2, ..., L_n$. A semiconductor layer lying between the metal contacts must be electrically isolated from the surrounding material.

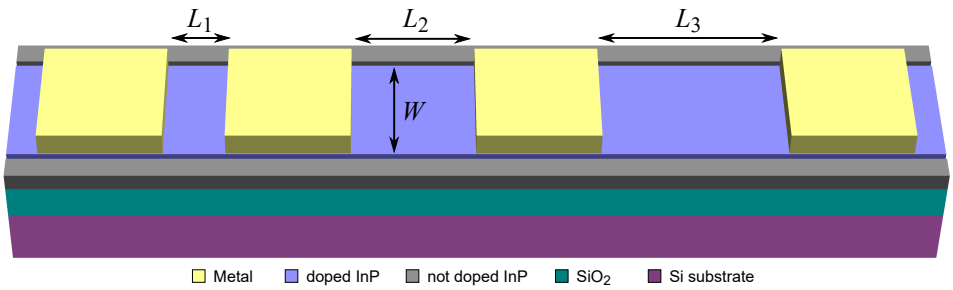


Figure 4.25: Schematic illustration of TLM test structure used in this work.

By probing two adjacent contacts, it is possible to get the value of resistance R, which is defined by

$$R = R_{\text{semi}} + 2R_{\text{c}} + 2R_{\text{Me}}\,, \tag{4.1}$$

where R_{semi} is the resistance of the semiconductor layer between contacts, R_{c} is the resistance of one semiconductor-metal contact and R_{Me} is the resistance of the metal. It is assumed that both contacts are identical. R_{Me} is negligible compared to other terms and can be omitted.

Resistance of the semiconductor layer can be written as

$$R_{\text{semi}} = R_{\text{sh}}\frac{L}{W}\,, \tag{4.2}$$

where R_{sh} is the sheet resistance of semiconductor layer, which is independent of particular geometry, L and W are the length and the width of the semiconductor layer.

By plotting resistances for different contact pairs versus L/W, it is possible to get values of sheet resistance and contact resistance by using

$$R = R_{\text{sh}}\frac{L}{W} + 2R_{\text{c}}\,. \tag{4.3}$$

The value of contact resistance depends on specific geometry, so it can't be used for contact quality comparison. For that purpose specific contact resistivity (ρ_{c}) is used, which is defined as

$$\rho_{\text{c}} = R_{\text{c}}A_{\text{c,eff}}\,, \tag{4.4}$$

where $A_{\text{c,eff}}$ is the effective contact area. To determine $A_{\text{c,eff}}$, current density distribution under the contact pad needs to be taken into account. Current density

is largest close to the contact edge and drops exponentially when moving away from it. To describe this current crowding, transfer length L_t can be introduced, which is defined as [212]

$$L_t = \sqrt{\frac{\rho_c}{R_{sh}}}\,. \tag{4.5}$$

Then $A_{c,eff}$ can be written as $L_t W$. Substituting it into Eq. (4.4), we get

$$\rho_c = \frac{R_c^2 W^2}{R_{sh}}\,, \tag{4.6}$$

which can be calculated using values of R_c and R_{sh}, obtained by linearization of Eq. (4.3). Semiconductor-metal contact is considered to have good quality if its ρ_c is on the order of or less than $10^{-6}\,\Omega\,\mathrm{cm}^2$ [212].

An example of fabricated TLM test structure is shown on Fig. 4.26. It consists of several contact arrays, separated from each other by trenches etched in semiconductor layer. The bottom side of semiconductor layer is electrically isolated by SiO_2 layer. Each array is dedicated to the specific semiconductor type and configuration. Contact dimensions are 100x100 µm, the size was chosen to facilitate easy probing. Separation between contacts varies from 10 µm to 210 µm with increment of 20 µm.

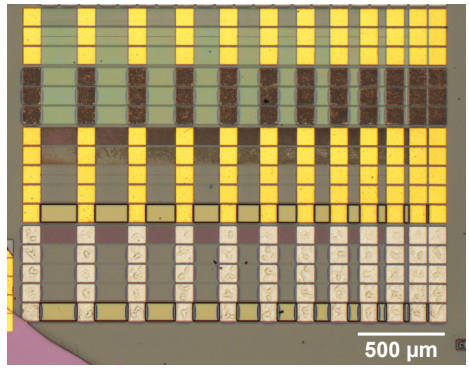


Figure 4.26: Optical microscope image of fabricated TLM test structures with different semiconductor layers, separated from each other with current-blocking trenches.

Figure 4.27(a) shows typical set of current-voltage characteristics for one TLM array. Linear shape of all I-V curves indicates that contacts have ohmic behavior. Resistance values are obtained from the slopes of I-V curves and plotted versus L/W (Fig. 4.27b). Equation (4.3) is then used for data approximation with R_{sh} slope and $2R_c$ intercept.

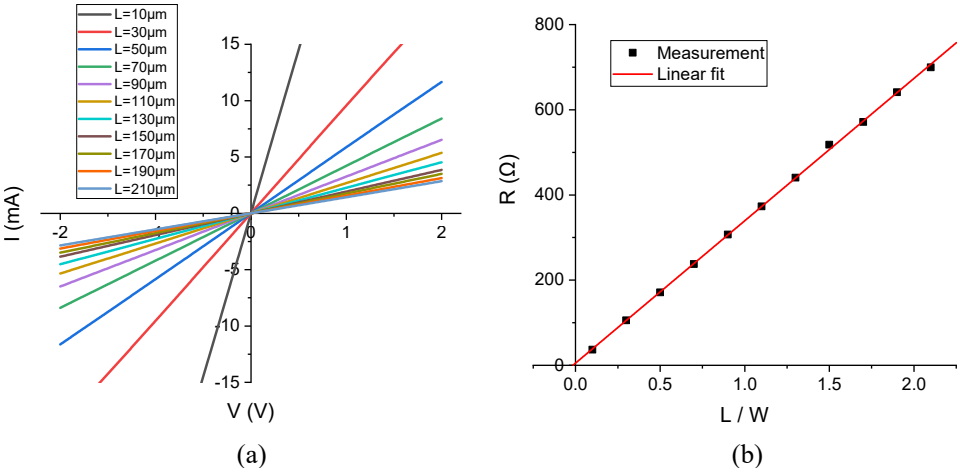


Figure 4.27: An example of typical set of TLM measurements data. (a) Set of I-V curves for p-InGaAs/p-InP TLM array. (b) Linear fit of resistance versus L/W for the same data set. Obtained values are: $R_{\mathrm{sh}} = (334.2 \pm 2.3)\,\Omega\square$, $R_{\mathrm{c}} = (2.6 \pm 1.4)\,\Omega$, $\rho_{\mathrm{c}} = 2 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$.

Due to large relative error in contact resistance determination, it is difficult to obtain precise specific contact resistivity values. But the high level of precision is not really needed. It can be concluded that good contact quality is achieved for all metal-semiconductor combinations (in case of doped semiconductors), because in most cases ρ_{c} is lying in 10^{-7}–$10^{-6}\,\Omega\,\mathrm{cm}^2$ range. In the scope of this work, the primary application of TLM is to obtain sheet resistance values for investigated doped semiconductors.

4.5.2 Hall effect measurements

In this work, Hall effect measurements[8] are implemented for carrier concentration and mobility evaluation using fabricated Hall bar test structures, shown in Fig. 4.28. Utilization of Hall bar geometry is advantageous since test structures can be easily incorporated into existing mask design and be fabricated alongside other devices. Hall bar of pre-designed semiconductor type is electrically isolated by SiO_2 layer underneath and dry etching of surrounding semiconductor material. Metal contacts of corresponding type are then made.

If current I is applied between contacts numbered **5** and **6** in Fig. 4.28 with magnetic field B perpendicular to sample surface, Lorentz force acting on charge

[8]Hall effect measurements were performed by Dennis Christensen (DTU Energy).

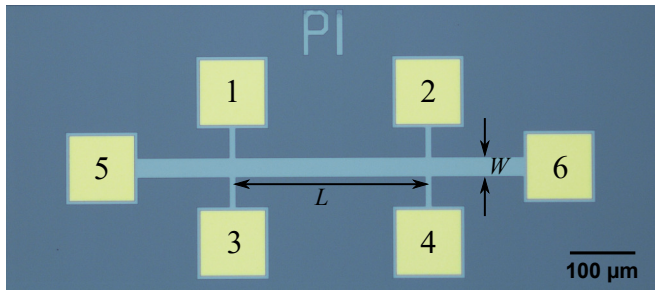


Figure 4.28: Optical microscope image of fabricated test structure with Hall bar geometry.

carriers results in Hall voltage V_{Hall}, that can be measured between contacts **2** and **4**. Hall coefficient R_{Hall} can then be calculated using formula

$$R_{\mathrm{Hall}} = \frac{V_{\mathrm{Hall}} t}{IB}\,, \tag{4.7}$$

where t is the material thickness [212]. In approximation of extrinsic semiconductor with only one carrier type, Hall coefficient can be written as $\frac{r}{qp}$ or $-\frac{r}{qn}$, where r is scattering factor, q is elemental charge, p and n are hole and electron concentrations, respectively. The sign of Hall coefficient gives information about carrier type, which can be useful in case of ambiguous samples.

Scattering factor r can be assumed to be unity due to operation in high magnetic field limit [213] ($B = 2\,\mathrm{T}$ was used). This allows carrier concentration to be evaluated by formulae

$$p = \frac{IB}{qV_{\mathrm{Hall}}t};\;\; n = -\frac{IB}{qV_{\mathrm{Hall}}t}\,. \tag{4.8}$$

Carrier mobility μ can be found using

$$\mu = \frac{|R_{\mathrm{Hall}}|}{\rho}\,, \tag{4.9}$$

where ρ is resistivity at zero magnetic field [212]. Resistivity value can be obtained by measurement of voltage V_{12} between contacts **1** and **2** in Fig. 4.28 and using the formula

$$\rho = \frac{Wt}{L}\frac{V_{12}}{I}\,, \tag{4.10}$$

where W is the width of Hall bar and L is the distance between contacts **1** and **2**.

Chapter 5

Experimental investigation of doping technologies

5.1 Si ion implantation

In order to define the n-doped region of lateral p-i-n junction in InP, Si ion implantation is used. The advantages of this method are described in Section 3.1. Alignment of doped regions in respect to PhC and BH is crucial, as well as the ability to pattern small structures with the sizes less than 1 µm. UV lithography with manual alignment cannot achieve these requirements, therefore DUV lithography is used for both n- and p-doped regions definition.

Si ion implantation was the only step in the whole process flow which was not done in DTU Nanolab cleanroom due to a lack of the required equipment. The samples were sent to Ion Beam Services company (Peynier, France).

5.1.1 Si ion implantation simulation

Before actual processing, important Si ion implantation parameters, such as ion energy, dose (sometimes called fluence) and minimum mask thickness, need to be determined. The ion energy is responsible for the distribution of ions in the targeted material, dose (number of implanted ions per unit area) determines the absolute value of ion concentration, and mask needs to be thick enough to completely block implanted ions in masked regions. Values of optimal ion energy and mask thickness can be obtained by simulation of the implantation process, which can be done using the program Transport of Ions in Matter (TRIM) included in software package Stopping and Range of Ions in Matter (SRIM) [214]. TRIM performs Monte Carlo simulation of interactions between implanted ions and target atoms according to a binary collision approximation. TRIM does not take into account the crystalline nature of the target material, assuming it to be amorphous, so it is not possible

to include channeling effect into the simulation. However, if the target surface is tilted in respect to ion beam, channeling can be reduced. In this work a tilt angle of 7° between the surface normal and implantation direction is used, in addition, wafer is rotated by ∼30° from the major flat.

The input data for the simulation is the following: type of implanted ion (in this work $^{29}Si^{+}$ is used), ion energy, sample tilt and targeted layer structure, which is the following: BARC (65 nm), InGaAs (50 nm), InP (250 nm), Al_2O_3 (5 nm), SiO_2 (1100 nm). The number of simulated ions is 1×10^7 to ensure a sufficient precision. In the output TRIM produces the data about ion distribution in both longitudinal and lateral directions, as well as vacancy (induced defects) distribution. The results of the ion energy variation are shown on Fig. 5.1(a). Optimal ion energy, at which most of Si^{+} ions stop in InP layer, is found to be 180 keV. At this energy maximum lateral projected range is 74 nm with maximum straggling (standard deviation) 92 nm. This lateral spread is accounted for in the mask design by 200 nm offset of n-doped regions.

In the final device only InP needs to be n-type, n-InGaAs is etched away during the processing. Having InGaAs on top of InP, however, can be advantageous in terms of implantation-induced lattice damage. Defect distribution is shifted towards the target surface compared to ion distribution [150], this means that InGaAs protects InP from excessive damage.

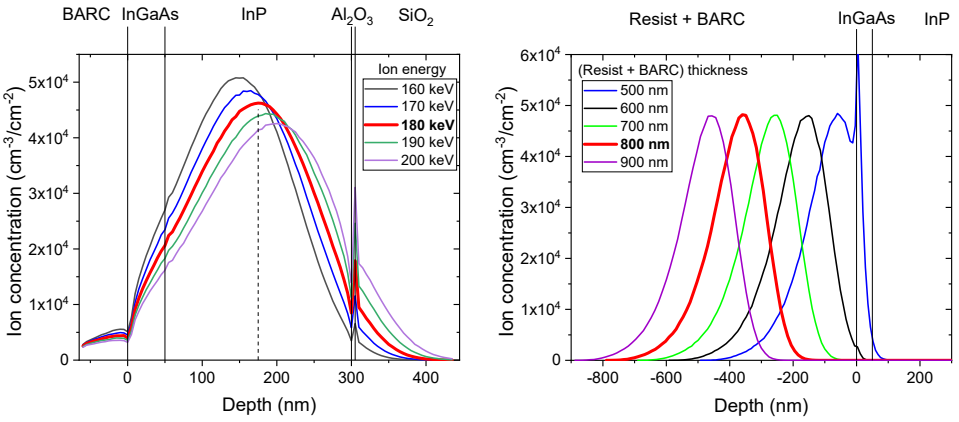


Figure 5.1: Results of Si ion implantation simulation using SRIM software. (a) Variation of Si^{+} ion energy. Dashed line corresponds to the middle of InP layer. (b) Variation of combined DUV photoresist and BARC thickness with fixed ion energy (180 keV). In both graphs BARC/InGaAs interface is taken as zero depth.

Since implantation is performed at room temperature, there is no need to trans-

fer the pattern to a hard mask, and DUV photoresist can be used as masking material. In order to find the minimum photoresist thickness, which would completely protect underlying layers from ion implantation, photoresist is included in the simulation. Figure 5.1(b) shows that combined photoresist and BARC thickness needs to be more than 700 nm. For the processing DUV resist thickness is chosen to be 750 nm due to availability of well-established spin coating recipe. Together with 65 nm of BARC this results in 815 nm of mask layer.

Choice of optimal implantation dose involves trade-off between high carrier concentration and low induced lattice damage. In this work total ion dose is varied between $2 \times 10^{13}\,\mathrm{cm}^{-2}$ and $2 \times 10^{14}\,\mathrm{cm}^{-2}$. According to the simulation, 84% of Si ions go to the InP layer. This results in an average Si concentration in InP at $6.7 \times 10^{17} - 6.7 \times 10^{18}\,\mathrm{cm}^{-3}$.

5.1.2 Si activation

After ion implantation most of Si impurities are electrically inactive, hence an activation step is necessary (see Section 3.1). Activation is done by annealing the sample at high temperature (650–800 °C in this work). Since InGaAs/InP starts to decompose at those temperatures, it needs to be protected either by capping layer or Group V gas overpressure.

The first choice for capping layer material was 100 nm of PECVD SiN_x. As shown in Fig. 5.2(a), after RTA in N_2 atmosphere at 770 °C for only 5 s all the sample surface became hugely deteriorated with III-V material looking like "melted". This could be explained by thermal stress-induced microcracking of SiN_x film caused by thermal expansion coefficient mismatch of SiN_x and InGaAs/InP.

To negate thermal stress problem, BPSG was chosen as a capping layer material due to its different thermal expansion coefficient and the ability to reflow at high temperatures [215], which leads to reduced stress. Indeed, deposition of ∼100 nm of BPSG significantly improves surface quality after annealing, as shown in Fig. 5.2(b). Nevertheless, quite large area still became deteriorated, especially close to the edges of the III-V bonded region. After optimization of the PECVD process it was found that reducing N_2O flow, which acts as oxygen source, results in oxygen-poor BPSG deposition, which leads to absence of any III-V deterioration after annealing at 800 °C for 30 s (see Fig. 5.2c).

It should be noted that Ga outdiffusion, which is known to occur at high temperatures from the InGaAs to glass layer, is suppressed in case of BPSG due to doped glass being more dense and void-free compared to standard SiO_2 [216].

The other way to prevent InGaAs/InP degradation during Si activation is annealing in AsH_3 atmosphere (AsH_3 is used since InGaAs, not InP, constitutes the sample surface at that stage). In this case RTA cannot be used due to unavailability of other from N_2 gases in the RTA equipment. The Si activation can be incorporated in the Zn diffusion recipe done in MOVPE machine by addition of annealing step under arsine flow just before Zn diffusion step. However, in this case

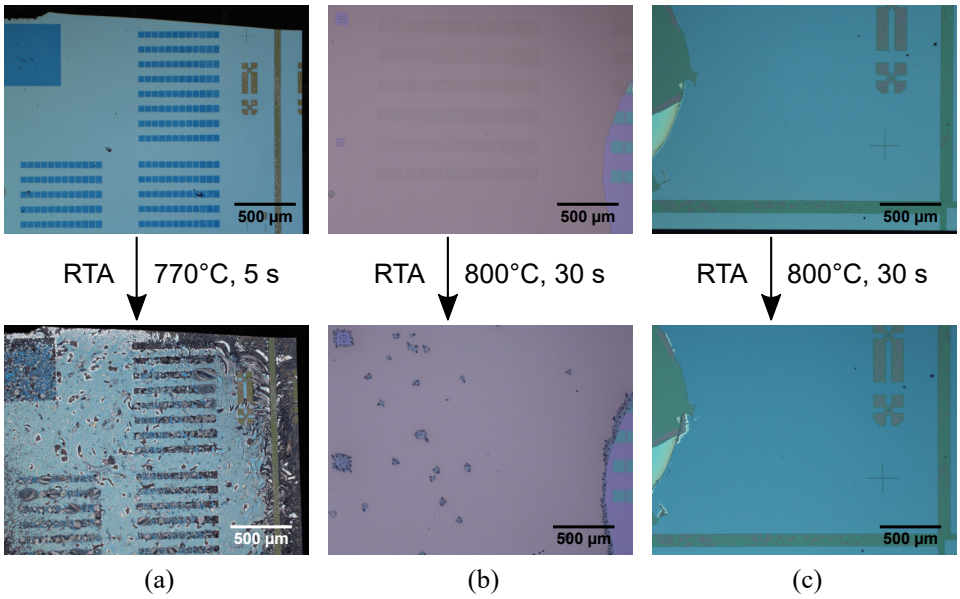


Figure 5.2: Optical microscope images of InGaAs/InP bonded to SiO_2/Si with (a) SiN_x, (b) BPSG and (c) oxygen-poor BPSG as a capping layer before and after RTA.

annealing with short (sub-minute) duration becomes difficult due to low heating and cooling ramp rates. Increasing the annealing time while keeping the temperature at 800 °C can in principle lead to sizable Si diffusion and redistribution [217], therefore, annealing temperature should be reduced. In this work annealing at 650 °C for 15 min is done. It should be noted that the annealing step at 650 °C in MOVPE is done even for RTA-activated samples.

Figure 5.3 shows sheet resistance values obtained by the transmission line method for different Si activation temperatures and ion doses. There is a trend of sheet resistance decrease with Si activation temperature increase for both tested ion doses, with the lowest R_{sh} value of 75 Ω/□ for the sample with dose $2 \times 10^{14}\,\mathrm{cm}^{-2}$ annealed at 800 °C.

Hall effect measurements at room temperature were performed for the samples annealed at 800 °C, the obtained data is given in Table 5.1. Activation ratio is defined as the ratio between measured carrier concentration and simulated Si ion concentration in the InP layer.

As can be seen from the data, RTA at 800 °C for 30 s results in almost half of the Si ions being electrically active. Electron mobility $\mu_{\mathrm{e,Hall}}$ is two times smaller in case of higher ion dose, which can be explained by increased residual implantation-

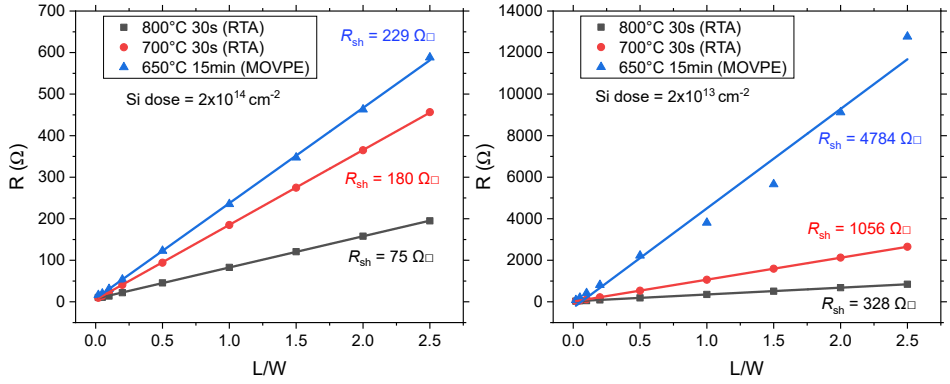


Figure 5.3: TLM data for n-type InP with different Si activation temperatures. (a): Si dose = $2 \times 10^{14}\,\mathrm{cm}^{-2}$. (b): Si dose = $2 \times 10^{13}\,\mathrm{cm}^{-2}$.

Table 5.1: Hall effect measurements data for the samples annealed at 800 °C.

Ion dose, cm^{-2}	Annealing type	Temperature, time	n_{Hall}, cm^{-3}	$\mu_{\mathrm{e,Hall}}$, $\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$	Activation ratio
2×10^{13}	RTA	800 °C, 30 s	3.27×10^{17}	2138	49%
2×10^{14}	RTA	800 °C, 30 s	2.94×10^{18}	1042	44%

induced lattice damage and increased carrier impurity scattering.

Assuming the same electron mobility values for the respective ion doses, average electron concentration n_{TLM} in n-InP can be estimated based on TLM data using the formula

$$n_{\mathrm{TLM}} = \frac{1}{R_{\mathrm{sh}}\,\mu_{\mathrm{e,Hall}}\,e\,t}\,, \tag{5.1}$$

where R_{sh} is the sheet resistance obtained by TLM, e is the elementary charge and t is the thickness of InP layer (250 nm). Note that the actual electron mobility values for samples annealed at lower temperatures (700 °C and 650 °C) may differ from assumed. On the one hand, mobility can be lower due to possible not complete recovery of implantation damage. On the other hand, mobility can be higher due to lower carrier scattering because of lower carrier concentration.

Activation ratio can then be calculated, the resulting data is presented in Table 5.2.

Obtained n_{TLM} values for the samples annealed at 800 °C are close to n_{Hall} values, however, TLM gives values overestimated by $\sim 9\%$ compared to Hall mea-

Table 5.2: Estimation of electron concentration based on TLM data.

Ion dose, cm^{-2}	Annealing type	Temperature, time	n_{TLM}, cm^{-3}	Activation ratio
2×10^{13}	RTA	800 °C, 30 s	$\sim 3.6 \times 10^{17}$	~53%
2×10^{14}	RTA	800 °C, 30 s	$\sim 3.2 \times 10^{18}$	~47%
2×10^{13}	RTA	700 °C, 30 s	$\sim 1.1 \times 10^{17}$	~16%
2×10^{14}	RTA	700 °C, 30 s	$\sim 1.3 \times 10^{18}$	~20%
2×10^{13}	MOVPE	650 °C, 15 min	$\sim 2.4 \times 10^{16}$	~4%
2×10^{14}	MOVPE	650 °C, 15 min	$\sim 1.04 \times 10^{18}$	~16%

surements.

With decrease of the annealing temperature, the activation ratio also decreases, but not drastically in case of ion dose $2 \times 10^{14}\,cm^{-3}$, even with $T = 650\,°C$ electron concentration is larger than $10^{18}\,cm^{-3}$. In case of ion dose $2 \times 10^{13}\,cm^{-3}$, the activation ratio decrease is much more pronounced, which is quite unexpected.

As described in Section 4.4, in case of the sample with QW active material, annealing temperature needs to be as low as possible to prevent QW degradation, therefore, MOVPE annealing at 650 °C for 15 min is used to activate the Si impurities. If the active material is constituted by QDs, higher annealing temperature can be probably tolerated due to higher QDs stability to thermal processing and possible annealing-induced defects, and larger electron concentration can be achieved with Si activation done by RTA at 800 °C with BPSG as a capping layer. The same applies for all-passive samples without any active material for all-optical Fano switch testing. Unfortunately, during real samples fabrication BPSG deposition was impossible due to the B_2H_6 and PH_3 gas manifold in the PECVD machine being out of use for half a year. Because of that, for all real samples MOVPE annealing at 650 °C for 15 min was used.

5.1.3 Mobility comparison with MOVPE-doped InP:Si

In a separate early experiment on investigation of fabrication of lateral p-i-n junction in InP membrane, the InP layer was n-doped by addition of Si_2H_6 during the initial growth of the membrane by MOVPE. This was done in order to avoid the need in Si ion implantation, since ion implantation equipment was not available in-house. The resulting InP:Si layer was characterized by means of Hall effect measurements at room temperature using the same configuration as for Si implanted samples. Obtained values of electron concentration and mobility are the following: $n_{Hall} = 2.56 \times 10^{17}\,cm^{-3}$, $\mu_{e,Hall} = 2063\,cm^2\,V^{-1}\,s^{-1}$. These values are very close to the ones for the Si implanted sample with ion dose $2 \times 10^{13}\,cm^{-2}$ annealed at 800 °C ($n_{Hall} = 3.27 \times 10^{17}\,cm^{-3}$, $\mu_{e,Hall} = 2138\,cm^2\,V^{-1}\,s^{-1}$). Since MOVPE

grown InP:Si is expected to be with very high crystalline quality and electrical dopant activation at used concentration, the similarity of electron mobility values at approximately the same carrier concentration indicates the same material quality of Si implanted InP. This means that all implantation-induced lattice damage is healed during the Si activation step in case of lower ion dose.

5.1.4 Undesired overall p-doping after Si implantation

During TLM data processing of Si implanted samples, quite unexpected result was obtained: samples with Si activation done only in MOVPE at 650 °C exhibited significant conductivity with resistance R lying in kΩ range in InP areas which were intrinsic by design. At the same time, the conductivity of intrinsic InP in samples activated by RTA was very low with R being in GΩ range (Fig. 5.4).

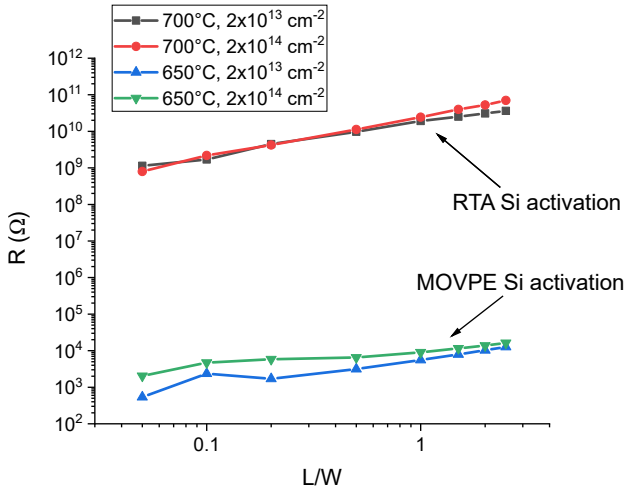


Figure 5.4: Transmission line method data for intrinsic by design InP in samples with different type of Si activation. “P”-type metal combination (Ti/Pt/Au) is used to make contacts to InP in all cases.

In order to determine the sign of the observed overall doping, TLM measurements were done for the same intrinsic by design InP on the same sample, but with different type of metal contacts: “N”-type with Ni/Ge/Au metal combination with InP under metal pads being n-doped by design, and “P”-type with Ti/Pt/Au metal combination with InP under metal pads being p-doped by design. Figure 5.5(a) shows that obtained IV curves for “P”-type array are linear with behavior typical for ohmic contacts. Contrary, IV curves for “N”-type array are significantly bent (Fig. 5.5b), which can be explained by the existence of n-p-n junction formed by n-type InP under metal pads and p-type InP between contacts. Moreover, the current

level for the “P”-type array is four orders of magnitude higher than for “N”-type array, which further implies that intrinsic by design InP is in reality p-doped.

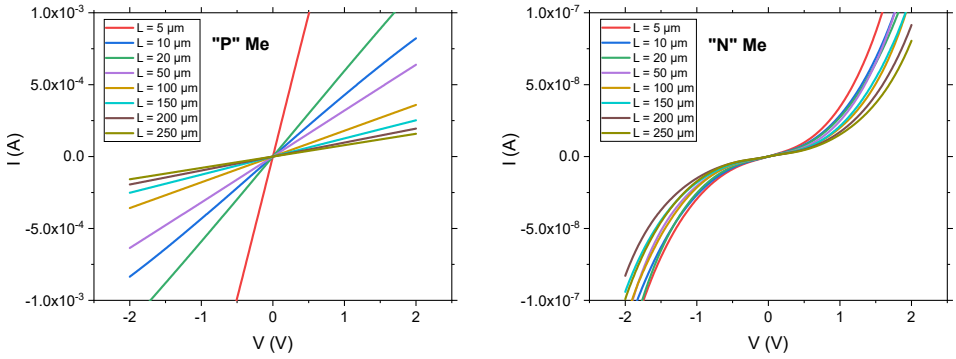


Figure 5.5: IV curves of TLM arrays for intrinsic by design InP. The sample is Si activated in MOVPE at 650 °C, ion dose is $2 \times 10^{13}\,\mathrm{cm}^{-3}$. (a): “P”-type metal contacts are used. (b): “N”-type metal contacts are used.

Sheet resistance value for non-intentionally p-doped InP is $4.67 \times 10^3\,\Omega/\square$ based on TLM data. Assuming hole mobility to be $\sim 100\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ [218], hole concentration can be estimated using Eq. (5.1), the obtained value is $\sim 5.4 \times 10^{17}\,\mathrm{cm}^{-3}$ (assuming uniform layer doping), which is quite significant.

SEM imaging can give further insight in the problem of overall p-doping through existence of image contrast caused by doping. P-type material appears brighter than n-type material in secondary electron SEM image due to lower energy required for the secondary electrons to be emitted [219]. Due to this phenomena, doped regions in InP can be visualized [220].

In Fig. 5.6(a), a p-i-n junction in InP is shown in a SEM image of the sample Si activated with RTA at 700 °C. Bright p-InP and dark n-InP, surrounded by i-InP with medium brightness, are easily distinguishable. The situation is different in case of the sample Si activated with MOVPE at 650 °C (Fig. 5.6b), for which there is almost no difference in brightness of p-InP and surrounding “i”-InP, which indicates p-type nature of “i”-InP. This fact agrees with TLM data in Fig. 5.4. Moreover, n-type InP is not uniform anymore: it is degraded by the bright spots, which become less pronounced in the inner region of n-type area.

After comparing process flow sequences for the samples, conclusion was made that the core reason behind the emergence of overall p-doping in case of MOVPE activated samples was the absence of BHF wet etching step before Zn diffusion (in case of RTA activated samples BHF was used to strip BPSG capping layer). A hypothesis was made that BHF was responsible for cleaning the sample surface

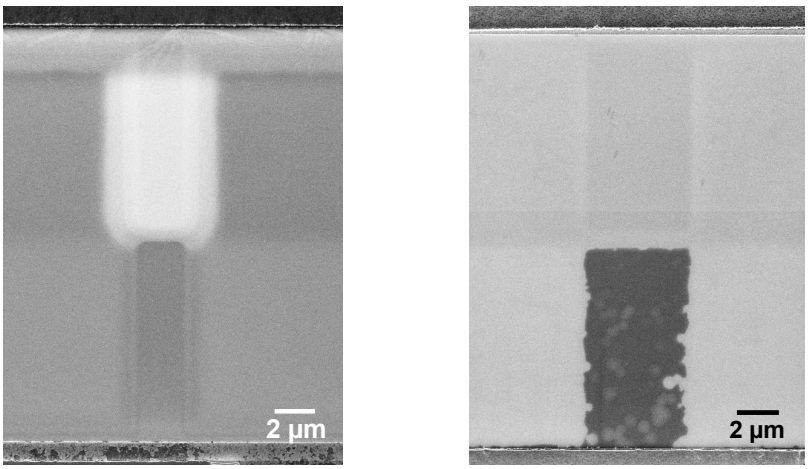


Figure 5.6: SEM images of p-i-n junction in InP. (a): Si activation is done with RTA at 700 °C. (b): Si activation is done with MOVPE at 650 °C. In both images Zn-diffused (p) area is on top, Si-implanted (n) area is on bottom, p-i-n junction is surrounded by intrinsic by design InP from the sides and metal contacts from the top and bottom sides.

from some kind of contaminant, which produced overall p-doping of InP during subsequent prolonged (∼1 h in total) high temperature annealing in Zn diffusion step. This contaminant would be the DUV photoresist crust, which formed during the Si ion implantation. Formation of such photoresist crust was reported in [221], however, with much larger ion dose. Even though plasma ashing was used to strip DUV photoresist after ion implantation, apparently, it failed to get rid of the crust.

The photoresist crust mainly consists of carbonized residual organic compounds with inclusion of silicon atoms trapped during ion implantation. During Zn diffusion step sample temperature is larger than 500 °C most of the time, so "drive-in" of crust dopant in underlying InGaAs/InP can occur. At the same time, photoresist crust is located under a SiO_2 hard mask, so it is not able to escape to the atmosphere.

Silicon is highly not probable to be the crust dopant responsible for overall p-doping. Although Si is well-known to be amphoteric dopant to InP [222], donor positions are highly favorable for Si compared to acceptor ones. Also, Si diffusivity in InGaAs/InP is very low at $T < 650$ °C. Carbon is another option. It is known to be p-type dopant in GaAs, however, in InP it is usually a weak n-type dopant [150]. Moreover, C diffusivity is also very low. Therefore, observed overall p-doping is difficult to explain. It might be related to the preferential formation of

native defects contributing to the observed p-doping due to thermal decomposition of residual organic compounds in the crust layer, however, observed high carrier concentration is very unlikely to be explained in such a way, moreover, damaged InP is usually found to be n-type [223]. Another hypothesis is the partial Zn diffusion through PECVD SiO_2 hard mask, which is probably degraded due to the existence of the crust.

The crust can originate not only from DUV photoresist, but also from BARC layer, which covers the whole sample surface during Si ion implantation, including Si-implanted regions. This means that n-doped InP can also be affected by undesired p-doping. But BARC thickness in implanted regions is more than order of magnitude thinner than combined thickness of DUV photoresist and BARC in masked regions (65 nm vs (750 + 65) nm), therefore, much less pronounced effect of undesired p-doping in Si-implanted InP is expected. This hypothesis is supported by SEM images in Fig. 5.6(b) and 5.7, where bright spots in n-InP, which constitute the effect of undesired p-doping, have the maximum brightness only in the vicinity of the region masked during ion implantation, with the inner BARC-related spots being much dimmer. The fact that bright photoresist-related spots appear in outer n-InP, where only BARC-related crust initially exists, gives evidence of lateral crust spreading during annealing in Zn diffusion step. This crust spreading can also be seen in the highlighted region of Fig. 5.7, where there are no crust-related spots in the region ∼4 µm close to Zn diffused InP. Most probably, during Zn diffusion BARC-related crust spreads to the mask opening and escapes to the gas phase.

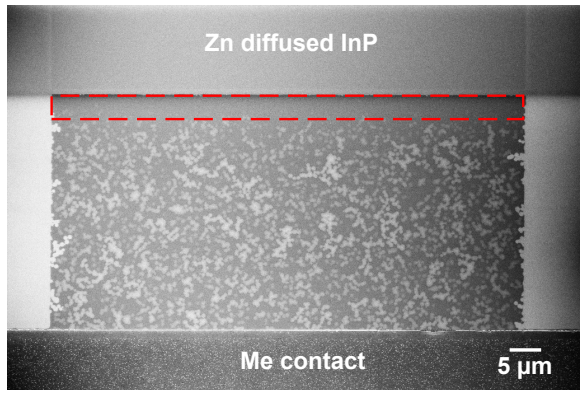
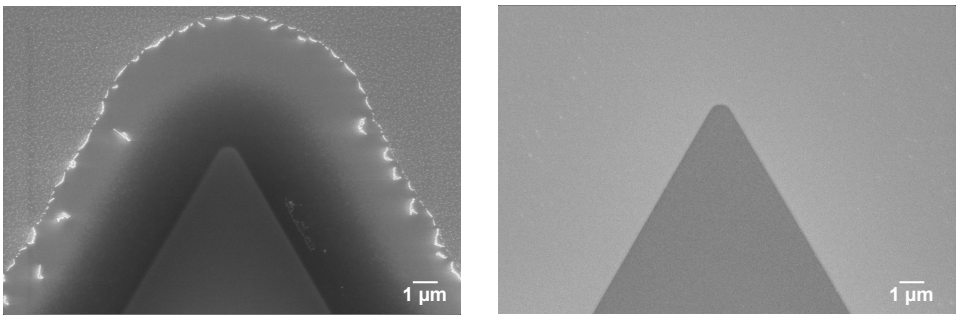


Figure 5.7: SEM image of Si-implanted area with 75 µm width. The region of Si-implanted InP in the vicinity of Zn-diffused InP, which does not have signs of undesired p-doping, is highlighted.

During the processing of successive samples, photoresist crust formation was confirmed by SEM imaging after prolonged plasma ashing, as can be seen in Fig. 5.8(a). After BHF treatment for 30 s, no sign of photoresist crust was vis-

ible (Fig. 5.8b). These samples were then annealed in MOVPE for Si activation in the same way as the samples with overall p-doping, and during electrical measurements, intrinsic by design InP showed no overall doping. This confirms that BHF cleaning step after plasma ashing of ion implanted photoresist is essential in order to avoid undesired overall p-doping.



(a) (b)

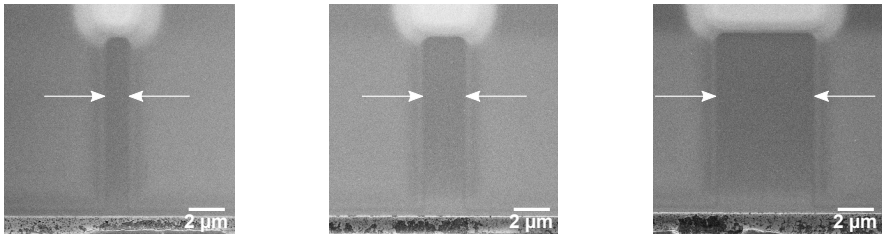
Figure 5.8: SEM images of Si implanted region after DUV photoresist plasma ashing (a) before and (b) after BHF treatment for 30 s.

5.1.5 Lateral Si redistribution

In order to be able to accurately control the position and dimensions of doped regions, lateral dopant redistribution must be taken into account. It is defined as the distance between the patterned edge of the mask opening during the doping process and the edge of the actual dopant extent in the final device, assuming an abrupt dopant distribution. This dopant distribution deviation from the designed pattern can happen during the doping process or subsequent annealing at high temperature steps, which would allow dopant impurities to diffuse. In case of ion implantation, lateral dopant redistribution happening during ion implantation process is called lateral projected range and can be simulated, see Subsection 5.1.1.

Lateral dopant redistribution can be characterized by different methods, e.g., scanning capacitance microscopy [224]. In this work SEM and electrical measurements of specifically designed test structures are used.

As already described in Subsection 5.1.4, SEM doping contrast can be used to visualize doped regions. It also gives the possibility to measure the dimensions of doped regions and then, by comparing obtained values with designed ones, lateral dopant redistribution can be evaluated. Figure 5.9 shows the examples of such evaluation. After statistics collection, average lateral Si redistribution distance is found to be (0.18 ± 0.03) µm.



(a) (b) (c)

Figure 5.9: SEM images of Si implanted regions with different designed widths: (a) 1 µm, (b) 2 µm, (c) 5 µm. Arrows indicate the measured width of n-type InP. Obtained values of lateral Si redistribution are: (a) 0.21 µm, (b) 0.19 µm, (c) 0.22 µm. Ion dose is $2 \times 10^{14}\,\mathrm{cm}^{-2}$, Si activation is done by RTA at 700 °C.

Another method used in this work to quantify lateral dopant redistribution is electrical measurement of pre-fabricated TLM-like test structure. The schematic of such test structure is shown in Fig. 5.10. One working element consists of two metal contacts with InP in between. InP is doped close to the metal contacts, but is left undoped in the middle. The array of such elements is made, with the total designed length of doped InP L_0 being kept the same and the length of not doped InP d being varied.

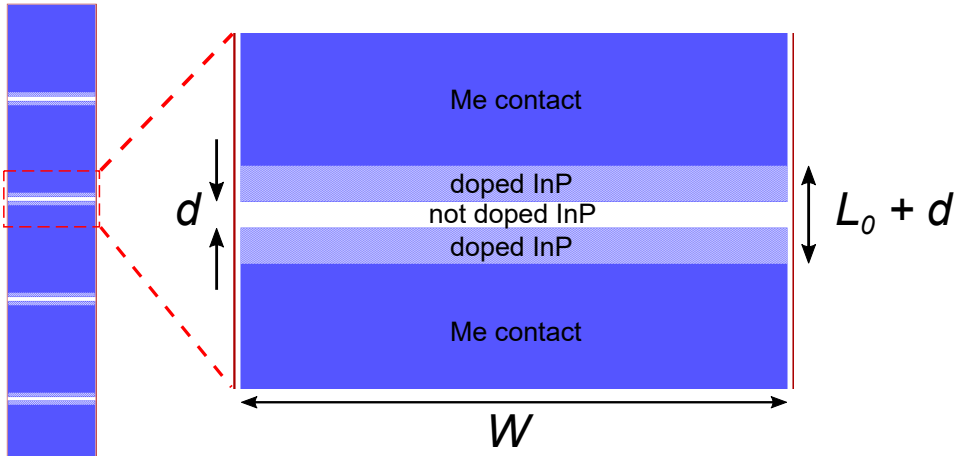


Figure 5.10: Schematic representation of TLM-like test structure used for electrical measurement of lateral dopant redistribution. Contacts array is isolated from the surrounding material by trenches etched in InP.

If we denote lateral dopant redistribution length by l, the total real length of doped InP becomes $L_0 + 2l$, since we have two sides of doped InP (see Fig. 5.10). Here, an assumption is made that lateral dopant redistribution is abrupt and can be characterized by specific length l. Then, if the length of undoped by design InP d is less than $2l$, in real sample there is no gap between doped regions. But if d becomes larger than $2l$, then undoped InP appears in real sample with the length being $d - 2l$.

By modifying the standard TLM equation (4.3) for the case of two materials with different sheet resistance in series, we get

$$R = \begin{cases} R_{\mathrm{sh},1}\dfrac{L_0 + d}{W} + 2R_{\mathrm{c}}\,, & \text{if } d \le 2l\,, \\ R_{\mathrm{sh},1}\dfrac{L_0 + 2l}{W} + R_{\mathrm{sh},2}\dfrac{d - 2l}{W} + 2R_{\mathrm{c}}\,, & \text{if } d > 2l\,, \end{cases} \tag{5.2}$$

where R is measured element resistance, $R_{\mathrm{sh},1}$, $R_{\mathrm{sh},2}$ are sheet resistances for doped and undoped InP, respectively, W is array width and R_{c} is contact resistance. The value of $2l$ can then be obtained as the coordinate of intersection of two lines.

The experimental data, which is linearized according to Eq. (5.2), is shown in Fig. 5.11. L_0 is fixed at 10 µm. The obtained value of $l = 0.25$ µm is larger than obtained by means of SEM (0.18 µm), which can probably indicate some underestimation of lateral Si redistribution by SEM method. However, obtained values are quite close. It should be noted that some amount of carriers is injected into undoped InP under bias, which may affect the measurements.

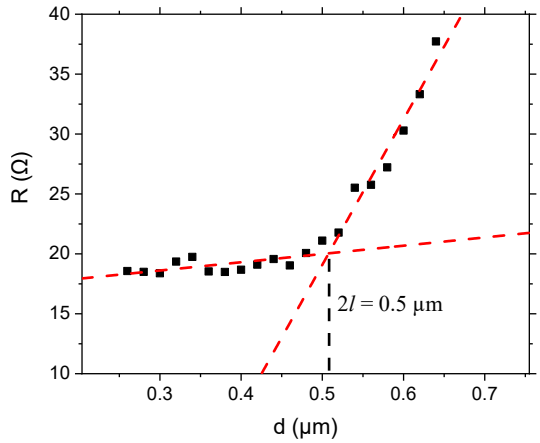


Figure 5.11: Evaluation of lateral Si redistribution by electrical measurement of TLM-like test structure. Ion dose is $2 \times 10^{14}\,\mathrm{cm}^{-2}$, Si activation is done by MOVPE at 650 °C.

5.2 Zn diffusion

As described in Section 3.2, Zn diffusion from the gas phase in the MOVPE reactor using a zinc-organic compound as a precursor is a promising method of post-growth InP p-doping. Considerable amount of publications has been made on this topic, however, there are none describing Zn diffusion in InP epilayer bonded to different substrate (in our case SiO_2/Si substrate). Also, each of the fabrication setups is somewhat unique in terms of used sets of parameters, therefore, in case of a new setup all optimization and calibration must be made almost from a scratch.

5.2.1 Process description

The aim of using Zn diffusion in this work is to create a p-doped region in the InP membrane, which is the main element of the final device, whether laser or optical switch. However, thin (50 nm) lattice matched InGaAs layer is left on top of InP during Zn diffusion. The purpose of having InGaAs is the following: firstly, to improve metal contact quality to p-InP, secondly, to enhance carrier concentration in InP, as shown in [182], and thirdly, to protect the InP layer from possible Zn outdiffusion during the cooling down step.

Since Zn diffusion occurs at elevated temperatures in a MOVPE reactor, photoresist cannot be used as a masking material, so pattern transfer to a hard mask is needed. For that purpose 100 nm of PECVD SiO_2 is deposited before lithography processing.

As in the case of n-doping, there are high requirements for accurate positioning of p-type doped region with respect to other device components. Therefore, DUV lithography is used to define the mask pattern for Zn diffusion. After resist development, the pattern is transferred from the DUV photoresist layer to the BARC layer by low pressure anisotropic O_2 dry etching. Then, the SiO_2 hard mask is dry etched with CF_4/H_2 chemistry. Finally, photoresist and BARC are stripped by a combination of acetone treatment and plasma ashing.

Just before loading the sample in MOVPE load-lock, the sample is immersed in concentrated sulfuric acid for 3 min in order to clean the surface from possible organic contaminants and to etch InGaAs native oxides. This is the standard procedure for all pre-processed III-V samples going into MOVPE, it was decided not to alter it. Then, the sample is rinsed with H_2O, blow dried with a nitrogen gun and loaded in the MOVPE loadlock, where high vacuum of $\sim 10^{-4}$ mbar is reached before transferring the sample in MOVPE reactor chamber. The description of the MOVPE system is given in Subsection 4.3.1.

During the MOVPE processing, the overall gas flow is around 2.8×10^4 sccm with most of it being H_2 used as a carrier gas. In principle, N_2 could also be used as a carrier gas in MOVPE during diffusion [225], but in order to avoid constant transitions between carrier gases in the shared MOVPE tool, common H_2 is used instead. Chamber pressure is kept at 80 mbar.

The temperature profile of a typical Zn diffusion run is shown in Fig. 5.12. When the temperature exceeds 300 °C, AsH_3 flow is turned on to ensure As-rich atmosphere to protect the InGaAs from thermal degradation. The sample is then annealed at 650 °C for 15 min. This step is required for activation of previously implanted Si (see Subsection 5.1.2). After that, the temperature is lowered down to the value in 500–550 °C range, and following the temperature stabilization, DEZn is injected in the reactor chamber. DEZn molecules are then thermally decomposed and give rise to Zn available for indiffusion.

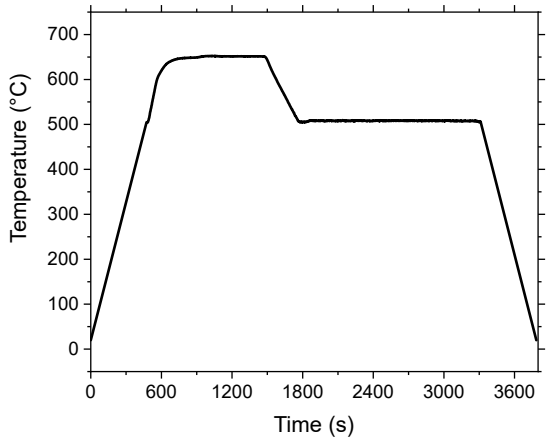


Figure 5.12: Temperature profile of Zn diffusion run. Emissivity-corrected pyrometer is used to measure temperature of the sample surface. The data is extrapolated for the temperatures lower than 500 °C due to pyrometer limitations.

After MOVPE processing, RTA at 450 °C for 5 min under N_2 atmosphere is used to enhance Zn electrical activation ratio. Since incorporated Zn can be electrically inactive partly due to formation of Zn−H complexes during diffusion, nitrogen atmosphere is important for hydrogen outdiffusion during Zn activation.

5.2.2 Zn diffusion on InP substrate

The investigation of Zn diffusion was started with a test run on an unmasked 2" InP substrate with 500 nm of undoped InP and 50 nm of lattice matched InGaAs grown on top to be able to get information about carrier concentration profile by means of electrochemical capacitance-voltage (ECV) profiling. Diffusion was carried out at 500 °C for 5 and 10 minutes. DEZn in H_2 carrier gas flow was 50 sccm, which corresponded to molar flow at 35.2 µmol/min. Arsine gas flow was 175 sccm with corresponding molar flow of 7810 µmol/min.

According to ECV measurements data, shown in Fig. 5.13, a hole concentration of $\sim 10^{18}\,\mathrm{cm}^{-3}$ in InP can be achieved for the 250 nm top layer in case of diffusion duration larger than 10 minutes.

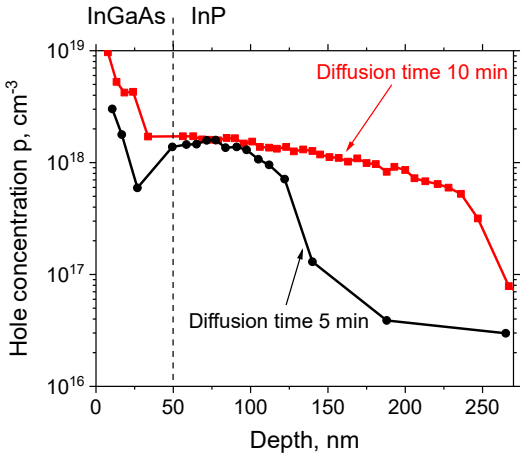


Figure 5.13: Hole concentration profiles for different duration of Zn diffusion on InP substrate, obtained by means of ECV profiling with the use of back side contacts.

In further investigations, Zn diffusion is conducted for 20 minutes. At this duration, the InGaAs/InP (50 nm / 250 nm) membrane is expected to be completely p-doped with not too large effect of lateral diffusion under the mask.

For the samples with InGaAs/InP membrane bonded to SiO_2/Si substrate, ECV profiling is difficult due to the insulating dielectric SiO_2 layer. One could, in principle, use front side contacts, but the resistivity may be high and affect the profiling. Therefore, for bonded samples the main experimental method to perform electrical characterization is TLM, discussed in detail in Subsection 4.5.1. It also has the advantages of being non-destructive method and requiring small amount of surface space, which gives the possibility to integrate TLM test structures in the design with real devices.

5.2.3 Electrical properties

Electrical properties optimization was performed for Zn diffusion in InGaAs/InP membrane bonded to a SiO_2/Si substrate. The InP layer is 250 nm thick since this is the target thickness for nanolaser PhC design. The InGaAs thickness is chosen to be 50 nm. Lithography patterns are designed in a way to allow TLM measurements for different semiconductor layers and doping types, therefore, sheet resistance values could be obtained for both p-InP and p-InGaAs/p-InP.

In early runs, test samples were fully processed according to the process flow discussed in Chapter 4 with the exception of skipped BH definition and Si ion implantation stages. As a consequence, significant amount of time was required for each Zn diffusion optimization iteration. Moreover, several sample batches were completely ruined due to then undiscovered MOVPE DEZn source bath malfunctioning, which caused a significant decrease in real DEZn molar flow relative to the expectation with the volume flow being the same. Eventually, a strategy of quick Zn diffusion tests on small wafer pieces with greatly simplified process flow was implemented. All lithography and alignment cycles were skipped, except for P metal contacts lift-off process, for which first print UV exposure was done. Zn diffusion was performed on blanket (without any pattern) InGaAs/InP/SiO_2/Si samples, and InGaAs was etched after P metal contacts definition only on one cleaved part of the sample to be able to obtain data for both p-InP and p-InGaAs/p-InP layers. The drawback of such approach is that information about lateral Zn redistribution cannot collected due to absence of SiO_2 mask. Also, there could be some difference in absolute values of electrical properties for blanket and patterned Zn diffusion cases, but overall trends of parameters variation are expected to be the same.

In order to be able to use the same P metal contacts mask design for the TLM structures while skipping the stage of dry etching of current confining trenches, 2D finite element simulation of current spreading in such scenario was done in COMSOL Multiphysics software, see Fig. 5.14(a,b). The obtained coefficients of current increase were then used to correct experimental TLM data of the samples without trenches (Fig. 5.14c). The corrected data then could be used for usual sheet resistance calculation (Fig. 5.14d). It should be noted that the other option would have been to use a ring contact geometry, but that would require a new lithography mask.

The most important processing parameters, which affect Zn diffusion, include process temperature, DEZn flow and AsH_3 flow. Optimization of these parameters is further discussed.

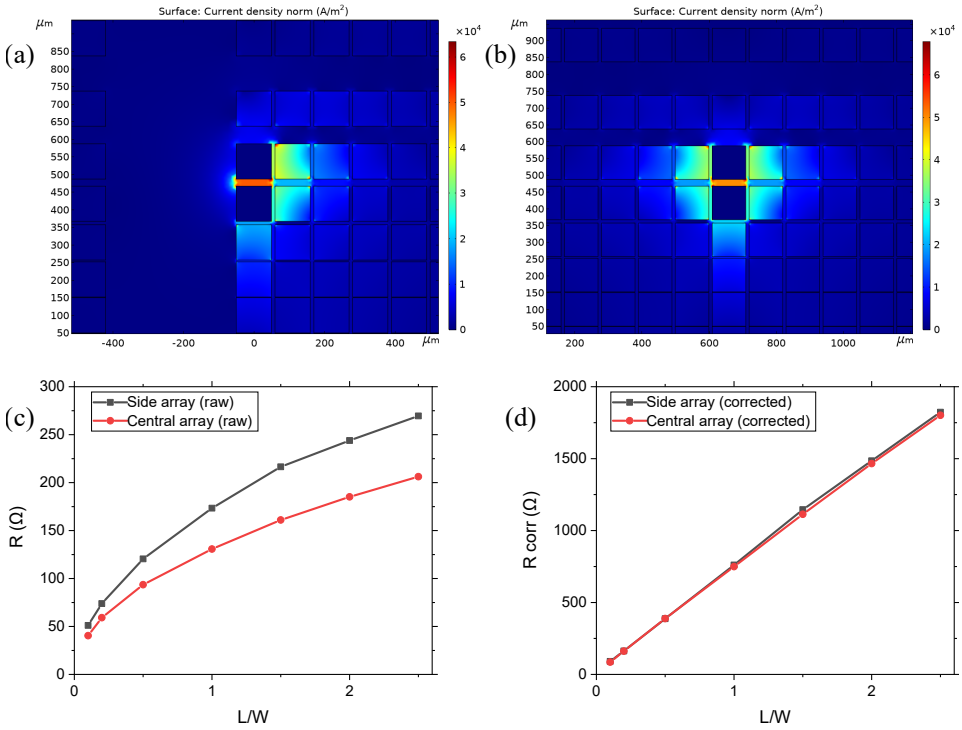


Figure 5.14: COMSOL simulation of current spreading in TLM structures in absence of etched trenches in case of (a) side and (b) central TLM array. (c): An example of uncorrected experimental TLM data. Significant deviation from linearity is observed. (d): An example of corrected TLM data.

Temperature

The process temperature, typically used for MOVPE-based Zn diffusion in III-V materials, lies in the 500–550 °C range, as discussed in Subsection 3.2.2. However, the exact optimal temperature values can deviate due to the differences in the particular process conditions and the utilized equipment. The lower temperature limit is determined by the formation of parasitic ZnP_x or, in our case, $ZnAs_x$ layer.

In this work, 505 °C and 540 °C are tested with the rest of the parameters being kept the same. The choice of 505 °C temperature instead of 500 °C is determined by the chosen option of pyrometer temperature control.[1]

[1]Since 500 °C is the lower limit of MOVPE pyrometer working range, processing at this temperature occasionally results in lost signal, which causes power supply to ramp up power in a not controlled way.

After diffusion, in case of both temperatures, no zinc arsenide deposition is observed, and the wafer surface remains mirror-like. However, sheet resistance values of both p-InP and p-InGaAs/p-InP diffused at 505 °C are almost two times lower compared to the diffusion done at 540 °C, as shown in Fig. 5.15(a,b). This fact can be attributed to the increased rate of Zn evaporation from the surface in case of higher temperature, which results in less Zn available for indiffusion.

Consequently, further investigations are conducted with 505 °C diffusion temperature.

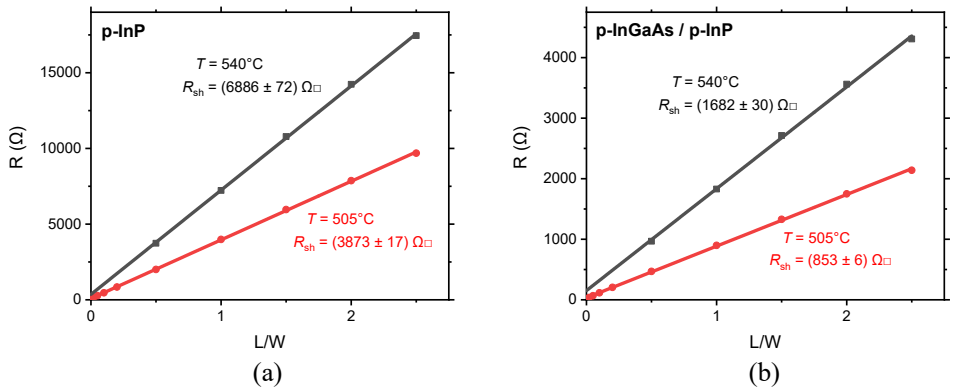


Figure 5.15: TLM data for (a) p-InP and (b) p-InGaAs/p-InP layers diffused at different temperatures: 540 °C and 505 °C. Blanket Zn diffusion is performed for 20 min with DEZn molar flow 114 µmol/min and AsH_3 molar flow 7810 µmol/min.

DEZn flow

The other important parameter of Zn diffusion is DEZn flow, which directly affects the Zn concentration on the InGaAs surface. A DEZn molar flow sweep in the 26–307 µmol/min range is performed for blanket diffusion test at 505 °C for 20 min with AsH_3 molar flow 7810 µmol/min. As shown in Fig. 5.16(a,b), a gradual increase of membrane conductivity is observed for both p-InP and p-InGaAs/p-InP with DEZn molar flow increase. No substantial saturation of conductivity is observed within the investigated DEZn flow range. A further increase of DEZn flow is impossible in the utilized MOVPE system due to limitations imposed by mass flow controllers. In order to achieve the maximum molar flow in this experimental series, even heating of DEZn bubbler bath from the standard 18 °C up to 30 °C has to be done. In principle, if even larger flows are required, DMZn can be used as Zn source instead of DEZn due to much larger vapor pressure (299.1 Torr for DMZn compared to 12.1 Torr for DEZn at 20 °C) [226].

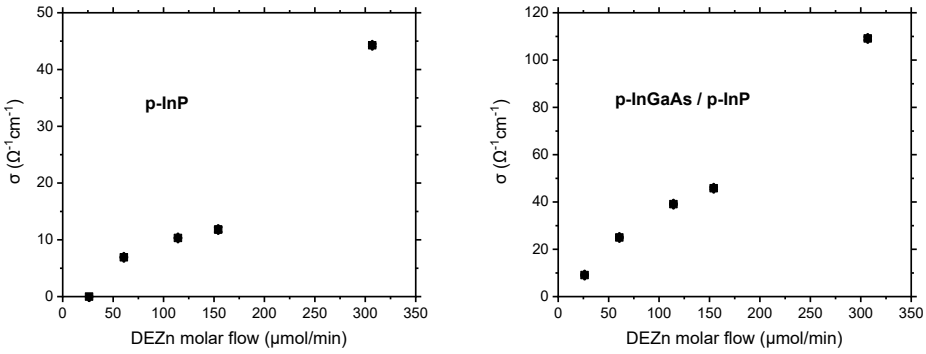


Figure 5.16: Electrical conductivity data for (a) p-InP and (b) p-InGaAs/p-InP layers diffused with different DEZn molar flows. Blanket Zn diffusion is performed for 20 min at 505 °C with AsH_3 molar flow 7810 µmol/min. Conductivity values are calculated from sheet resistance values obtained by TLM.

In case of the sample diffused with the largest DEZn molar flow (307 µmol/min), hole concentrations are estimated for p-InP and p-InGaAs layers based on TLM sheet resistance values of p-InP (903 Ω/□) and p-InGaAs/p-InP (305 Ω/□), respectively. In order to extract information about sheet resistance of only p-InGaAs, a parallel connection model is used. The hole mobility value for both p-InP and p-InGaAs is assumed to be $100\,cm^2\,V^{-1}\,s^{-1}$ [218], which results in average hole concentrations of $\sim 2.8 \times 10^{18}\,cm^{-3}$ for p-InP and $\sim 2.7 \times 10^{19}\,cm^{-3}$ for p-InGaAs.

The same Zn diffusion parameters were used for the device sample with patterned SiO_2 mask. Since in this case Zn diffusion occurs only in the relatively small areas (low loading), the local increase of the available Zn species might be expected. The estimated hole concentration in p-InP was found to be approximately the same ($\sim 2.7 \times 10^{18}\,cm^{-3}$) as in the case of blanket diffusion on the test sample, which might indicate no influence of mask pattern on p-InP electrical properties. Another explanation can be the reached saturation of the hole concentration at the used maximum DEZn flow level (further DEZn flow increase to check the saturation was not possible).

Arsine flow

The role of arsine in the Zn diffusion process is two-fold: on the one hand, AsH_3 overpressure prevents the top InGaAs layer from thermal degradation, on the other hand, arsine presence can affect the Zn diffusion via the influence on the lattice point defects. Figure 5.17 shows the electrical conductivity data for the samples

diffused with different AsH_3 molar flows with other diffusion parameters kept the same. Electrical conductivity dependence is not monotonic and exhibits a maximum in the medium AsH_3 flow range for both p-InP and p-InGaAs/p-InP membranes. The obtained results are consistent with the data presented in [184] for Zn diffusion in InGaAs at 525 °C with DMZn as Zn source. The authors propose the hypothesis of the enhancement of DMZn pyrolysis in AsH_3 presence, but Zn-organic compounds (both DMZn and DEZn) are considered to be already completely decomposed at >500 °C temperatures [191, 227]. However, if the gas residence time is very small, then Zn incorporation might be affected by the pyrolysis rate. Nevertheless, the influence of AsH_3 partial pressure on the concentration of point defects, namely, In vacancies as Zn incorporation sites, is the more probable explanation of the obtained results.

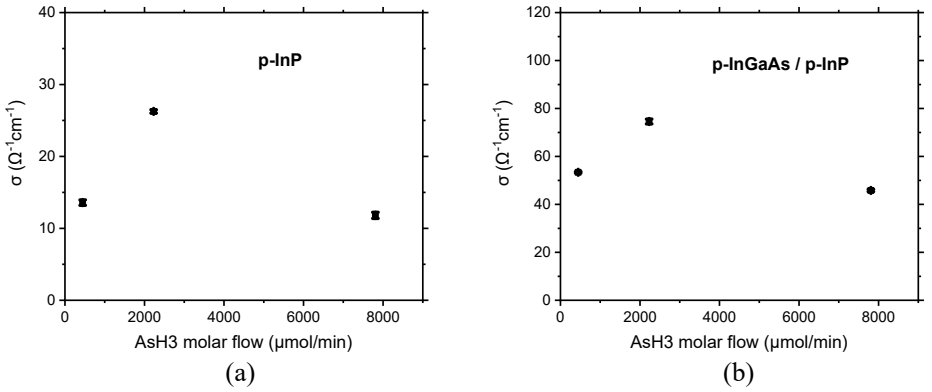


Figure 5.17: Electrical conductivity data for (a) p-InP and (b) p-InGaAs/p-InP layers diffused with different AsH_3 molar flows. Blanket Zn diffusion is performed for 20 min at 505 °C with DEZn molar flow 154 µmol/min. Conductivity values are calculated from sheet resistance values obtained by TLM.

Surface treatment

InGaAs surface treatment before Zn diffusion can in principle affect diffusion process. For instance, in this work p-doping pattern is defined by reactive ion etching of a 100 nm thick SiO_2 hard mask. The etching duration is optimized to be slightly larger than required to etch 100 nm of SiO_2 to ensure that no residues are left in mask openings. However, during overetching ions bombard the InGaAs surface. In order to evaluate the effect of ion bombardment on the subsequent Zn diffusion process, an experiment was performed with two pieces of the same InGaAs/InP/SiO_2/Si sample with no SiO_2 deposited. One piece was subject to

usual dry etching procedure before Zn diffusion, but the other was not dry etched. Blanket Zn diffusion was then performed in one run on both samples. As can be seen in Fig. 5.18, sheet resistance values are very close for both samples, which gives evidence of no dry etching effect on the Zn diffusion process.

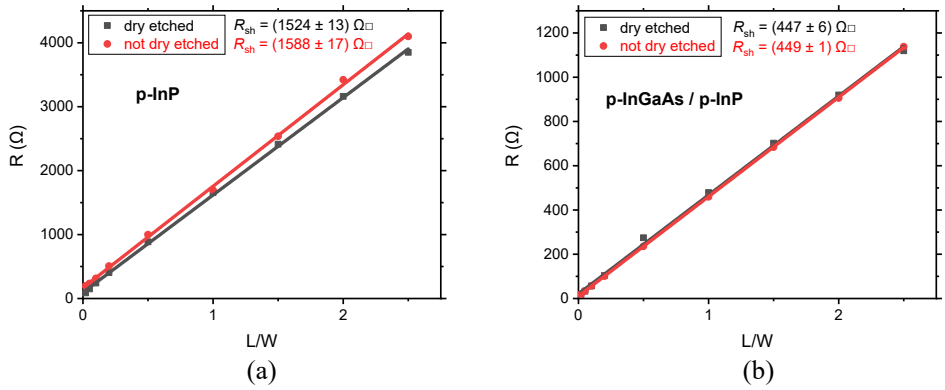


Figure 5.18: Comparison of TLM data for (a) p-InP and (b) p-InGaAs/p-InP layers in case of dry etched and not dry etched prior to diffusion. Blanket Zn diffusion is performed at 505 °C for 20 min with DEZn molar flow 154 µmol/min and AsH_3 molar flow 2230 µmol/min.

PhC airholes effect

Electrical properties measurements for all previously discussed experiments are performed for continuous semiconductor layers. However, in real devices the doped InP regions are not continuous, since the PhC airholes are etched through InP, reducing the amount of conducting semiconductor in the membrane. To evaluate the effect of airholes on electrical properties, for some device samples (i.e., with full processing) PhC pattern is etched with cyclic RIE process (alternating steps of CH_4/H_2 etching and O_2 cleaning) in p-InP between P-type metal contacts in TLM test structures. Filling factor f, defined as the ratio of the area taken by airholes to the total PhC area, in case of hexagonal lattice can be calculated according to the formula

$$f = \frac{2\pi r^2}{a^2\sqrt{3}}, \tag{5.3}$$

where r is an airhole radius and a is a PhC period. For the values of $r = 130$ nm and $a = 450$ nm, filling factor is 30%. Ratio of electrical conductivity values of p-InP with and without etched airholes is then calculated based on corresponding TLM sheet resistances. Airholes etching results in 46% reduction in conductivity

value, which is noticeably larger than PhC filling factor. This fact can be explained by the existence of a large number of surface states in the airholes sidewalls, which act as carrier traps. If the model of completely not conducting region with the width δ around the holes is applied, then the value of δ can be found by taking the experimental conductivity reduction as a filling factor for PhC with the effective radius $r + \delta$. In this work the value of δ is determined to be 30 nm, which is less than 42 nm found in [228]. It should be noted that the comparison is complicated by the different type of used dry etching and InP configuration.

5.2.4 Lateral Zn redistribution

As opposed to Si lateral redistribution, which is small and easily controlled due to the low Si diffusivity in InP, lateral Zn redistribution can be significant due to fast Zn diffusion in InP. In order to be able to accurately control the position of the p-doped region relative to the BH in the nanolaser or Fano cavity in the all-optical switch, the extent of lateral Zn diffusion needs to be carefully calibrated and adjusted for in the mask design.

The p-doped regions can be visualized using SEM. Due to SEM doping contrast, p-doped material appears brighter than the surrounding. Examples of SEM images used for lateral Zn redistribution evaluation are shown in Fig. 5.19. Lateral Zn redistribution is calculated using formula $(w_1 - w_0)/2$, where w_0 is the designed doped channel width and w_1 is the observed channel width. The obtained value of Zn lateral diffusion in p-InGaAs is (0.63 ± 0.02) µm, in p-InP (0.83 ± 0.08) µm. Lateral Zn redistribution is slightly smaller in case of p-InGaAs, which agrees with lower Zn diffusivity in InGaAs compared to InP [180].

In case of p-doped channel in InP (Fig. 5.19c,d), an additional contrast level, denoted as w_2, is observed, with $(w_2 - w_0)/2$ value being around 3 µm. However, from electrical characterization of TLM test structure with P-type contacts and i-InP in between, it is known that lateral Zn diffusion value lies in 0.5–2.5 µm range. Additional contrast level could stem from depletion region in p-n junction formed by Zn diffused p^+-InP and surrounding n^--InP, which is non-intentionally n-doped during MOVPE growth. If we take $(w_2 - w_1)/2 = \sim 2$ µm as depletion layer width, estimated background InP n-doping concentration is $\sim 4 \times 10^{14}\,\mathrm{cm}^{-3}$, which is a reasonable value.

Unfortunately, it turned out that the samples in the NATEC HERO batch were grown with InGaAs being lattice mismatched.[2] This fact resulted, first of all, in a hugely deteriorated p-InP surface (as shown in Fig. 5.20(a) and discussed in the next Subsection 5.2.5). Lateral Zn diffusion is also affected, becoming non-uniform and significantly larger, as can be seen in Fig. 5.20(a). Based on SEM doping contrast, Zn lateral redistribution is estimated to be (2.5 ± 0.5) µm in p-InP. As

[2]InGaAs composition was not controlled in a proper manner during MOVPE growth of NATEC HERO samples due to unavailability of X-ray diffraction (XRD) tool for InGaAs lattice constant calibration at that moment of time. XRD tool was out of use for three months.

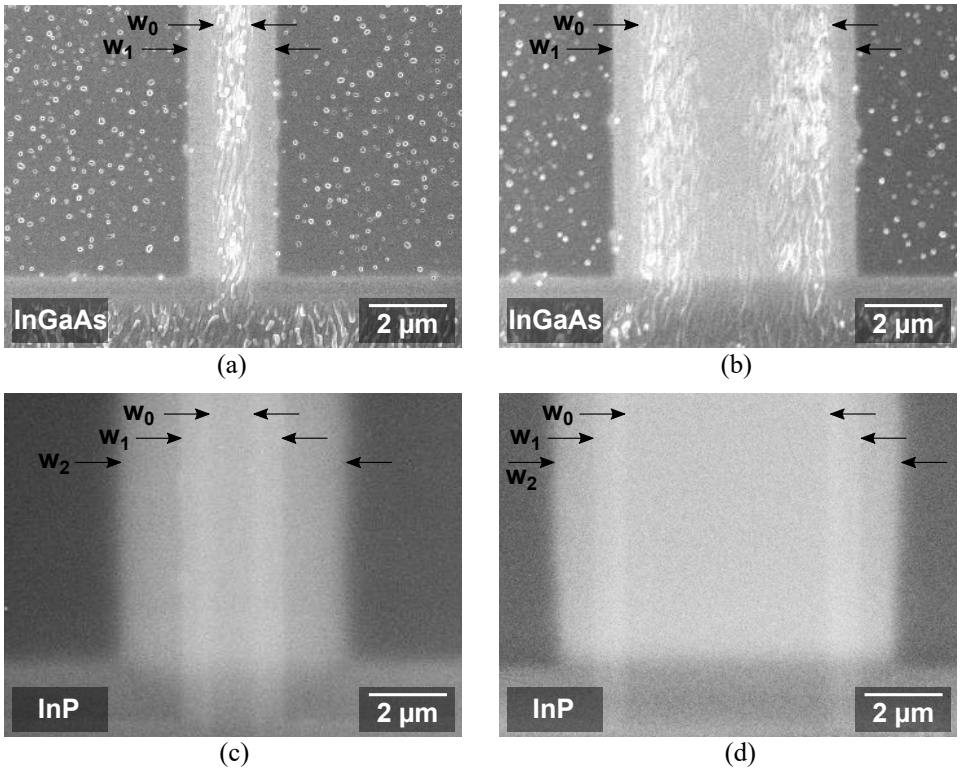


Figure 5.19: SEM images of p-doped channels after Zn diffusion. (a) Doped channel in InGaAs, designed width 1 µm. (b) InGaAs, 5 µm. (c) InP, 1 µm. (d) InP, 5 µm. Zn diffusion is performed at 505 °C for 20 min with DEZn molar flow 307 µmol/min and AsH_3 molar flow 7810 µmol/min. In case of InP images (c,d), top InGaAs layer is wet etched. Note that InGaAs is deteriorated (a,b), however, deterioration is not transferred to InP (c,d).

shown in Fig. 5.21(a,b), the method of electrical measurement of TLM-like test structures, described in Subsection 5.1.5, gives values of Zn lateral diffusion in p-InP 2.3 µm and in p-InGaAs 2.2 µm, which agrees with SEM data.

As shown in Fig. 5.20(b), reduction of DEZn flow during Zn diffusion on the sample from the same batch with lattice mismatched InGaAs allowed to avoid deterioration of p-InP surface, as well as to decrease Zn lateral redistribution, with estimated based on SEM contrast value being (1.1 ± 0.2) µm. However, lateral Zn diffusion remained non-uniform with wavy front shape. The reason for non-uniform lateral Zn diffusion can be increased density of defects, namely, threading

dislocations in strained material, with Zn diffusing faster along the defects [229, 230].

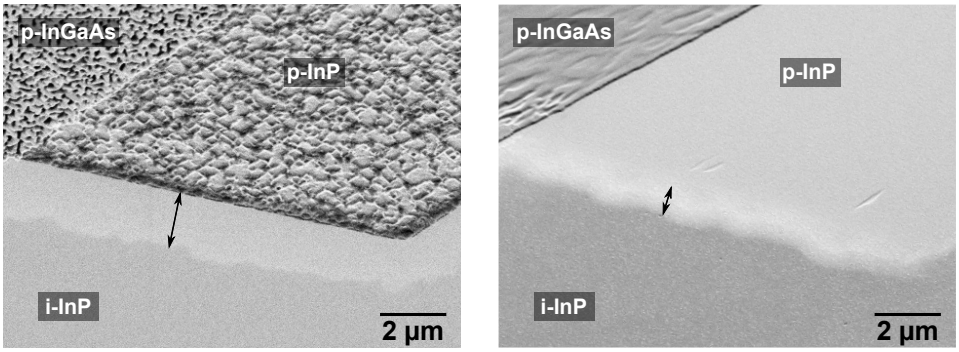


Figure 5.20: SEM images of Zn diffused InP with (a) high DEZn molar flow (307 µmol/min) and (b) low DEZn molar flow (154 µmol/min) in case of the samples with lattice mismatched InGaAs. Arrows indicate the extent of lateral Zn redistribution. Zn diffusion is performed at 505 °C for 20 min with AsH_3 molar flow 2230 µmol/min. Note that p-InP is significantly deteriorated in case of high DEZn flow (a), but is smooth in case of low DEZn flow (b). Sample tilt is 45°.

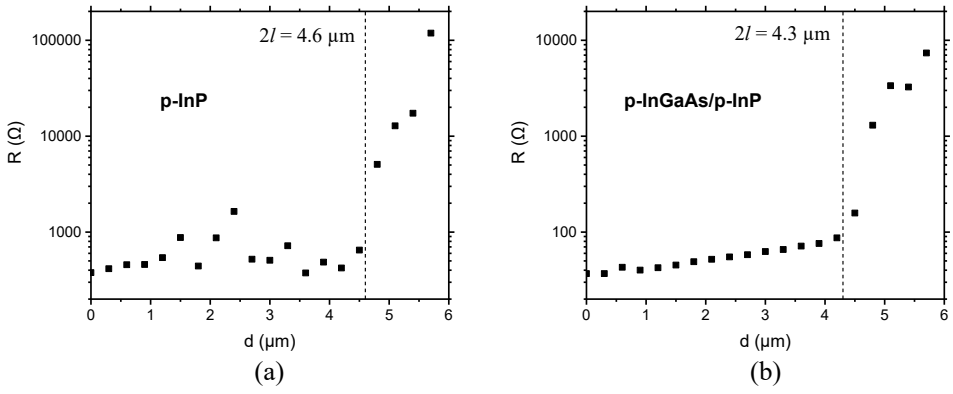


Figure 5.21: Evaluation of Zn lateral redistribution for the sample shown in Fig. 5.20(a) by electrical measurement of TLM-like test structures in case of (a) p-InP and (b) p-InGaAs/p-InP.

5.2.5 Zn-induced material deterioration

Deterioration in diffused area

Under certain circumstances, InGaAs and InP layers can become deteriorated after Zn diffusion. InGaAs degradation can be tolerated upon condition of preserved electrical properties, since in the final device it is used only for establishing of P metal contact. However, the InP layer is required to be defect-free to minimize optical losses. Atomic force microscope (AFM) scans of p-InP surface after Zn diffusion and InGaAs etching are shown in Fig. 5.22(a) in case of no deterioration and in Fig. 5.22(b) in case of InP degradation. Elongated defects, which are approximately aligned in the same direction, can be seen in Fig. 5.22(b).

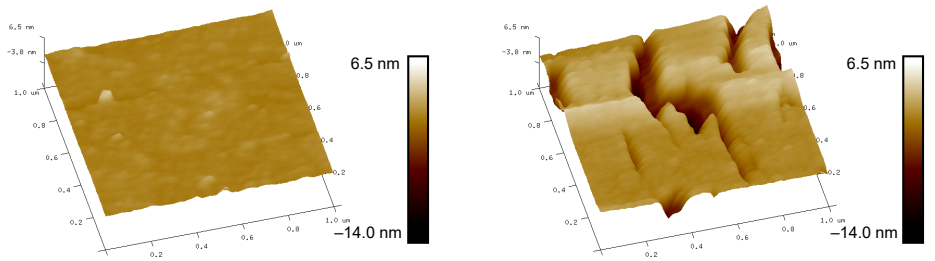


Figure 5.22: AFM scans of p-InP after Zn diffusion and InGaAs etching. (a): No deterioration is observed, average roughness Ra is 0.20 nm. (b): Elongated defects are observed, Ra is 1.46 nm.

Three factors have been identified to have influence on diffusion-induced material deterioration: accuracy of InGaAs lattice matching to InP, DEZn flow and mask pattern.

InGaAs lattice matching to InP is found to be the crucial factor in material degradation. If III-V layers are strained, dislocation formation during annealing is eased, which is further enhanced by the presence of Zn impurities. Sufficient reduction of DEZn flow[3] helps to avoid transfer of deterioration from p-InGaAs to p-InP, with only p-InGaAs being affected (see Fig. 5.20).

The mask pattern also affects p-InP deterioration, as shown in Fig. 5.23. In case of low density of diffusion mask openings (low loading), p-InP is heavily deteriorated (Fig. 5.23d), however, if diffusion loading is high, p-InP has smooth surface with only p-InGaAs being slightly deteriorated (Fig. 5.23b). Such behavior gives evidence of mass transport limited regime, with Zn migration from masked area to diffused openings playing a role. However, this finding contradicts with the

[3]Reduction of DEZn flow is expected to compromise p-InP electrical properties to a certain extent, but surface deterioration issue is thought to be more critical.

fact that no significant difference has been found between electrical properties of blanket and patterned Zn diffusion runs. This contradiction could mean that implemented TLM test structures design is too dense (with high local loading factor) to observe the effect.

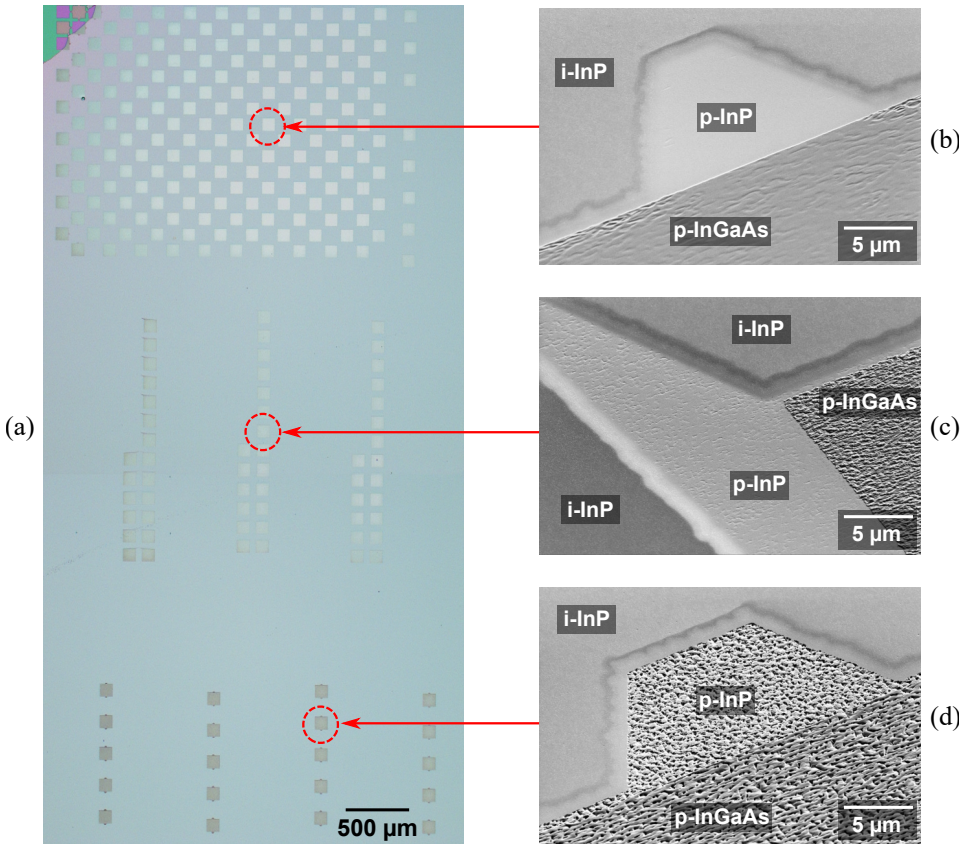


Figure 5.23: (a): Optical microscope image of the sample with lattice mismatched InGaAs after Zn diffusion and InGaAs etching stages. Zn diffusion is performed at 505 °C for 20 min with DEZn molar flow 154 µmol/min and AsH_3 molar flow 2230 µmol/min. (b-d): SEM images of p-InP and p-InGaAs. (b): High diffusion loading, (c): medium loading, (d): low loading. Sample tilt is 45°.

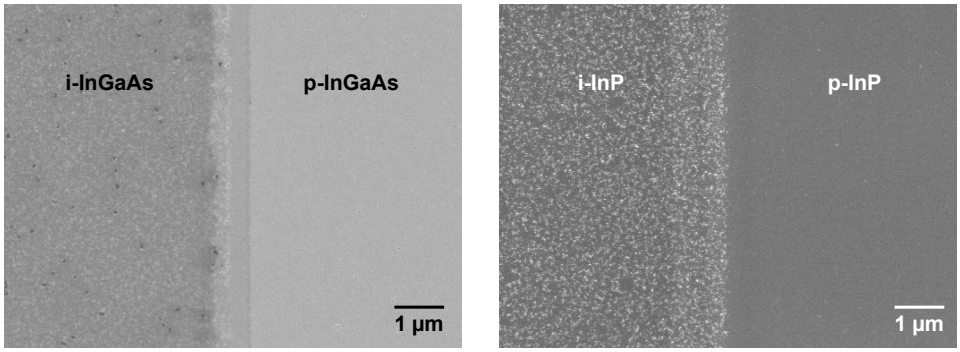
It should be noted that even in case of perfectly lattice matched InGaAs, still some material degradation has been observed, but only in p-InGaAs layer, as shown in Fig. 5.19(a,b). It is most probably related to zinc arsenide formation on p-InGaAs, which can occur during Zn diffusion in InGaAs under AsH_3 atmosphere

[184]. However, this deterioration is not transferred to the p-InP layer, as shown in Fig. 5.19(c,d).

Deterioration in masked area

Quite unexpectedly, for some samples material, which is situated under PECVD SiO_2 mask during Zn diffusion, can also become deteriorated. For most samples only i-InGaAs is affected, for example, as shown in Fig. 5.19(a,b). Gallium outdiffusion from InGaAs to SiO_2 layer, which is widely used for QW intermixing using impurity free vacancy disordering method [231], is unlikely to contribute to masked InGaAs deterioration, since the highest annealing temperature in Zn diffusion processing is 650 °C, and noticeable effect of SiO_2 layer on interdiffusion is reported to occur only at temperatures higher than 750 °C [232].

For one sample batch, masked material degradation is especially pronounced, with deterioration propagating even to i-InP layer. As shown in Fig. 5.24(b), in i-InP layer it manifests itself as increased surface roughness. This problem might be related to slightly changed stoichiometry of PECVD-deposited SiO_2 mask layer due to later discovered malfunction of SiH_4 mass flow controller in PECVD tool, but the mechanism of degradation is not known. Possible contamination could also be a factor, since PECVD tool experienced problems with high particle count at that point of time.



(a) (b)

Figure 5.24: SEM images of mask opening edge after Zn diffusion and SiO_2 mask wet etching. (a): i-InGaAs/p-InGaAs interface. (b): i-InP/p-InP interface after InGaAs wet etching.

5.3 Summary

To summarize, Si ion implantation and Zn thermal diffusion techniques have been successfully developed and optimized for selective area doping of InP membrane bonded to Si substrate. High carrier concentration values larger than $10^{18}\,\mathrm{cm}^{-3}$ have been achieved for both n-type and p-type InP. Dopant lateral redistribution has been characterized. The considerations regarding the trade-off between high electron concentration in n-InP and the reduction of thermal degradation of the active material in the membrane are discussed. Various accompanying important issues related to the processing are described and successfully solved, such as the development of capping layer for high temperature annealing, the problem of undesired overall p-doping, the issue of the material degradation after Zn diffusion.

Chapter 6

Light emitting device characterization

The developed doping technologies are implemented to fabricate lateral p-i-n junctions in InP membranes, which can be used for electrical pumping of lasers, as well as carrier sweep-out from the Fano switches. The switches are discussed in the next Chapter 7, the light emitting devices are in the focus of this chapter.

6.1 Lateral p-i-n junction

The essential requirement for laser operation is a carrier population inversion in the gain medium. In case of optical pumping, it is achieved by absorption of incoming photons. In case of electrical pumping, laser is basically a p-i-n diode, with holes and electrons injected from p- and n-regions into the intrinsic active region under applied forward bias. The advantages of lateral carrier injection scheme are discussed in Subsection 2.4.1.

The important property of the p-i-n junction is its series resistance, which significantly affects the laser performance. Lowering the series resistance allows the reduction of the laser power consumption. It also provides a steeper slope of diode IV characteristic with a smaller voltage swing required to modulate the current. Reduction of a heating effect is also very important, especially for membrane lasers, which are known to greatly suffer from the heating limitation. Consequently, lowering the series resistance gives the possibility for increasing the optical output power, required for low bit error rate (BER) data transmission. The series resistance can be lowered by enhancing the doping of p-type and n-type regions.

Another key diode property is a junction capacitance, which, together with the series resistance, determines RC modulation speed limit. However, in case of lateral geometry configuration, the capacitance is quite small due to inherently small junction cross-section areas.

In order to achieve efficient laser operation, ideally, all current needs to be directed to the laser active region. However, in reality the current can bypass the

active region. The leakage current increases the threshold current and the operation current, increasing the power consumption and contributing to membrane heating. Thus, it is crucial to confine the current in the designed path by, e.g., introduction of current-blocking trenches. In addition, lowering the series resistance of the designed path allows the usage of lower voltage, thus decreasing the magnitude of the leakage current.

The initial fabrication runs were dedicated to the development of the Zn thermal diffusion process in InP membrane. Since ion implantation equipment was not available in-house, n-doping by Si ion implantation was skipped to reduce turnaround time. Nevertheless, p-i-n junctions were still successfully fabricated with n-type InP originating from Ge doping underneath the alloyed N metal contacts with Ni/Ge/Au metal combination. An example of current-voltage characteristics of such p-i-n junction under varied illumination levels is shown in Fig. 6.1. The typical photodiode behavior is observed, with the pronounced effect of external light intensity due to large intrinsic area. This confirms the existence of p-i-n junction and successful p-doping by Zn diffusion. However, for a substantial number of failed experiments this was not the case due to later discovered malfunction of DEZn source bubbler in MOVPE system, which did not give any indications at the moment of processing.

Quite obviously, such p-i-n junction configuration is not suitable for laser operation due to ineffective current confinement and very high series resistance ($\sim$100 kΩ). However, it was utilized for the initial tests of the later discussed Fano switches.

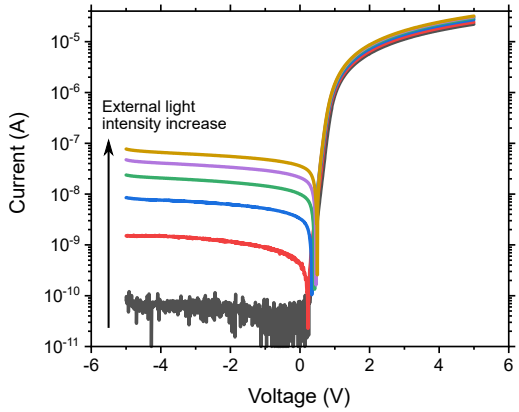


Figure 6.1: Semilog plot of IV characteristics of p-i-n junction in InP membrane under varied illumination levels. Si ion implantation was skipped. Absolute current values are plotted. Typical photodiode behavior is observed.

The later tests included Si ion implantation stage for the definition of n-type

regions. Figure 6.2(a) demonstrates IV characteristics of p-i-n junctions in continuous InP membrane with varied width of the doped regions, which in this case have rectangular shape. Figure 6.2(b) shows the obtained series resistance values, determined as the values of the differential resistance in high voltage range (2–5 V). Reasonable values of the series resistance are obtained even for the narrow doped channels.

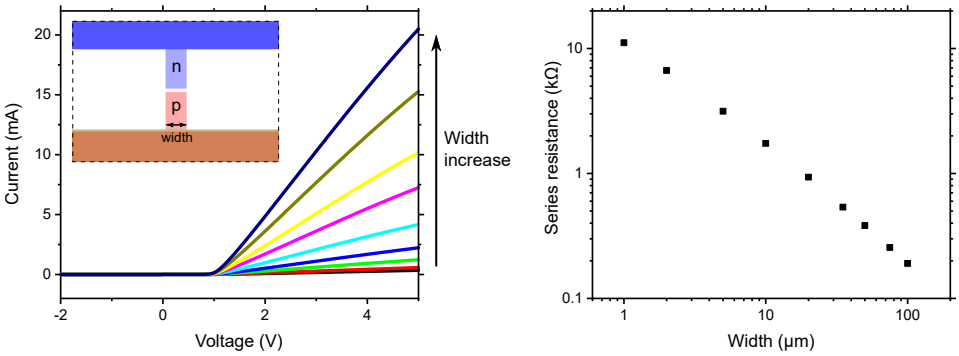


Figure 6.2: (a): IV characteristics of p-i-n junctions in InP membrane with varied width of the doped regions. The distance between metal contacts is kept at 20 µm. The designed length of the intrinsic region is 1 µm, however, the real length is estimated to be only marginally larger than zero due to dopant lateral redistribution. (b): Log plot of series resistance vs width of the corresponding p-i-n junctions.

In case of the actual device samples for the laser demonstration, PhC pattern was etched in InP membrane. The shape of the doped regions was tapered according to a trade-off between lowering the series resistance and lowering the leakage current. The narrowest dimension of the doped regions was determined by BH dimensions inside the optical cavity. The offsets to account for the dopant lateral redistribution were included in the design. To improve current confinement, isolating trenches were etched in InP close to metal contacts.

An example of IV characteristic of a fabricated BH PhC membrane device is shown in Fig. 6.3(a), with the corresponding differential resistance shown in Fig. 6.3(b). The obtained series resistance value is 5.3 kΩ. This type of devices is discussed in the following section.

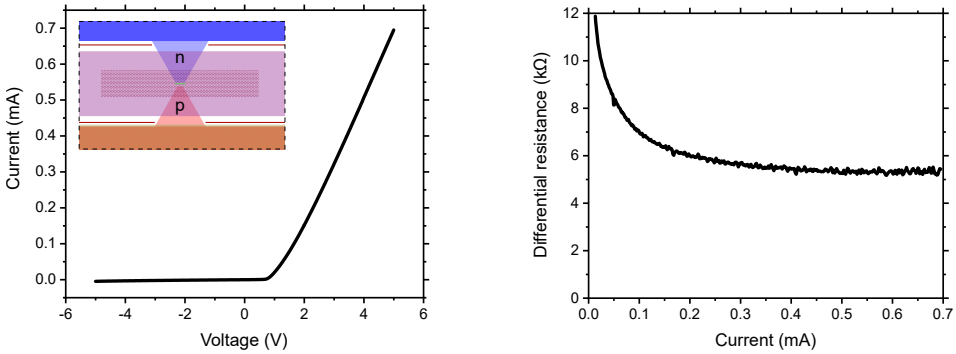
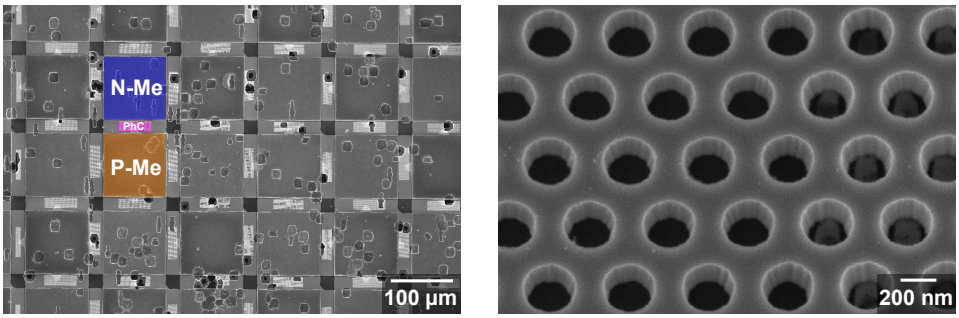


Figure 6.3: (a): IV characteristic of a fabricated BH PhC membrane device. The dimensions of a BH are 0.4x3.5 µm^2, n-type and p-type tapers are designed with 0.2 µm and 1.3 µm offsets from the BH, respectively. The distance between metal contacts is 25 µm. (b): Plot of differential resistance vs current for the device.

6.2 Optical device characterization

In the scope of this work the laser device samples (with the definition of BH) were fabricated within the NATEC HERO project. The great number of different device configurations was designed and fabricated, as described in Section 4.2. Unfortunately, the fabrication procedure was plagued with various issues. First of all, there was a large density of bonding defects, as shown in Fig. 6.4(a), which affected most of the devices, especially with considerable size. Nevertheless, there was still a sufficient number of the "survived" devices to perform the measurements. The exact nature of these defects is not known, probably, they were caused by not perfectly compensated membrane internal stress. Secondly, the two step dry etching of PhC holes in InP was not properly optimized at the time of the processing of the first NATEC HERO samples due to the difficulty to adapt the recipes, which were previously optimized for small chips ($\sim$ 10x10 mm^2), for the reproducible processing of the large 4" HERO samples. As a result, PhC airholes did not have the perfect sidewalls, as can be seen in Fig. 6.4(b). Thirdly, the first HERO samples were affected by significant surface deterioration in p-doped regions, as described in Subsection 5.2.5. The issue of surface deterioration was later solved for the later HERO samples, however, their fabrication was not finished at the time of writing this work due to the delays in the optimization of the PhC dry etching procedure.



(a) (b)

Figure 6.4: SEM images of the fabricated NATEC HERO BH PhC laser devices. (a): Array of the devices for the objective light collection. Large number of defects is visible. (b): Tilted image of PhC airholes. Not perfect sidewalls are visible.

The schematic of the experimental setup used for optical characterization of the fabricated devices[1] is shown in Fig. 6.5. A sample is located on the adjustable stage. The current is supplied from the Keithley 4200-SCS source measure unit (SMU)

[1]Experimental optical characterization was performed together with Aurimas Sakanas and Evangelos Dimopoulos.

via the needle probes. Emitted light is collected by the microscope objective lens (50X). Light is then either directed to the infrared (IR) camera, or reflected by the inserted beamsplitter and coupled into the multimode fiber on the piezo stage. The output is then split and directed to the optical spectrum analyzer (OSA) and the photodetector. The photodetector signal can then be used to automatically adjust the piezo stage position for better light coupling, as well as to record the total optical output power. The measurements are performed at room temperature.

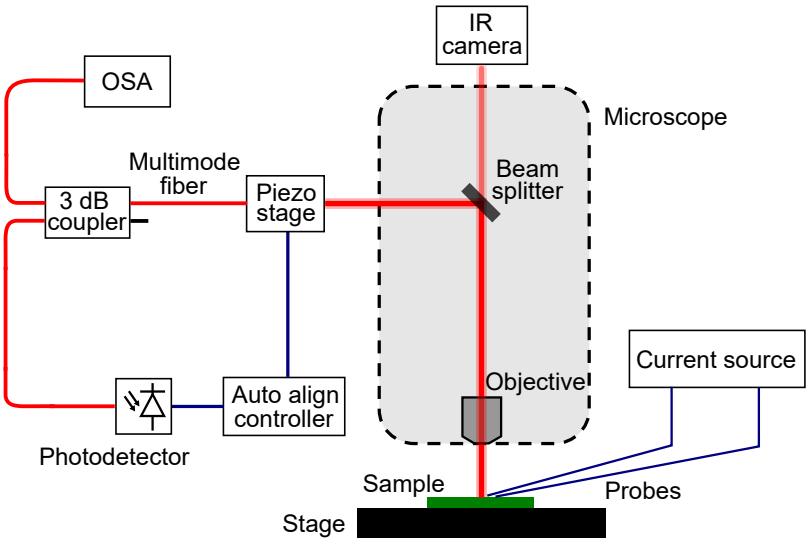


Figure 6.5: Schematic illustration of the experimental setup used for optical light emitting devices characterization under electrical pumping.

An example of the light emission from a BH PhC membrane device with the BH active region constituted by three layers of InGaAsP/InGaAlAs QWs is shown in IR camera image in Fig. 6.6. Light emission under electrical pumping is observed from the optical cavity region, which gives evidence of the successful realization of a LED. However, no meaningful optical spectrum could be recorded by OSA for any of the found working devices due to the very low output power and substantial losses in the setup. Unfortunately, no lasing was achieved for all the tested devices under electrical pumping.

An example of power-current (LI) characteristic for one of the devices under electrical pumping is shown in Fig. 6.7. Total output optical power is plotted as measured by the photodetector. Saturation and decrease of the collected emission is observed at high current levels due to excessive heating of the membrane. The fact that no reliable spectrum could be obtained by OSA gives evidence of the very broad emission spectrum and LED-mode device operation.

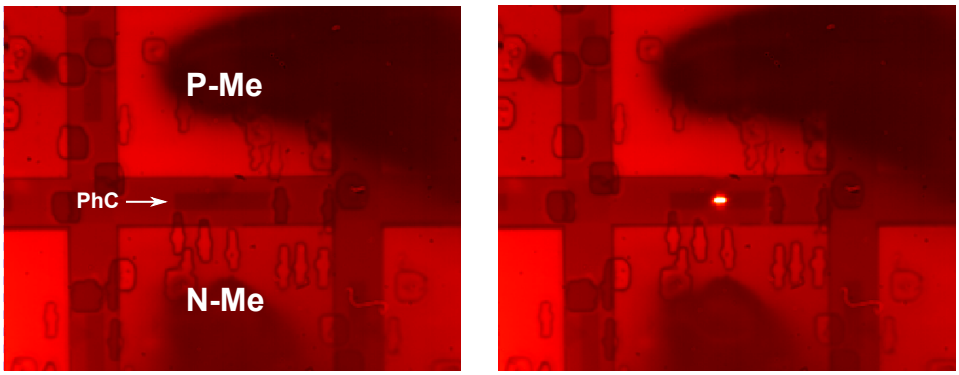


Figure 6.6: IR camera images of BH PhC membrane device (a) with no applied current, (b) with applied current. Light emission from the BH optical cavity region under electrical pumping is observed in (b). Optical cavity is L8-type (line defect with eight omitted airholes). The external illumination is turned on to visualize the device.

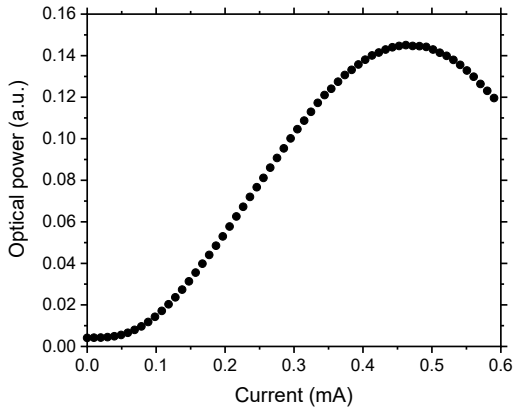


Figure 6.7: LI characteristic of BH PhC device under electrical pumping. Output optical power is measured by the photodetector. Note that the optical losses in the setup are not exactly known, thus, only approximate calibration of the photodetector responsivity is performed. One power arbitrary unit should correspond to one microwatt.

The main problem which did not allow to achieve lasing under electrical pumping in the first generation of NATEC HERO samples is thought to be the issue of significantly deteriorated p-doped region in InP membrane. Due to hugely en-

hanced scattering, optical cavity losses became too high. Another issue related to p-doping was larger than anticipated lateral Zn diffusion, which experimental value was estimated to be ∼2.3 µm (see Subsection 5.2.4), as opposed to the designed offsets of only 0.8 µm or 1.3 µm. Zn-induced QW intermixing might occur, as well as the further increase in optical cavity losses due to cavity material becoming p-doped. Not optimized dry etching of PhC holes could also contribute to the lack of lasing. Another problematic issue could be the QW degradation during Si activation step at 650 °C, although it is not considered to be critical since the annealed at 650 °C uniform QWs still show significant PL signal (see Section 4.4), and enclosing the QW in a very small BH region significantly reduces the chance of active material being affected by possible dislocations.

Unfortunately, the processing of the second generation of NATEC HERO samples with either QW or QD active material with eliminated deterioration of p-InP morphology, as well as controlled lateral Zn diffusion, was delayed by the difficulties related to reproducible dry etching of PhC holes in SiN_x hard mask and InP membrane with the controlled hole radius in case of 4" wafer processing, since the already existing etching procedure was optimized for small chip processing.

Chapter 7

All-optical Fano photonic crystal switches

Lateral p-i-n junction in InP membrane can also be implemented for the improvement of the high-speed performance of Fano all-optical switches[1], as further discussed in this chapter.

7.1 Fano resonance in PhC for all-optical switching

PhC membrane platform is very flexible and powerful in terms of realization of various device concepts. In particular, significant attention is brought to the idea of constructing PhC structures which exhibit Fano resonance [76]. One potential application is a Fano laser with a narrowband mirror based on Fano resonance, which was experimentally demonstrated [233]. It was theoretically predicted, that ultrahigh speed operation of such laser, not limited by relaxation oscillation frequency, could be achieved by modulating the Fano mirror [234]. Another promising application is all-optical signal processing, which is in the scope of this chapter.

Fano resonance is a general wave phenomenon, which occurs as a result of the interference between a discrete state and a continuum band of states [235]. In a PhC it can be realized in a structure consisting of a line defect waveguide (continuum of modes) with a side-coupled nanocavity (single mode or only a few modes). SEM image of a fabricated PhC Fano structure in air-suspended InP membrane bonded to SiO_2/Si substrate is shown in Fig. 7.1. The waveguide is formed by omitting one row of airholes and shifting the closest airhole rows toward the waveguide. The H0-type nanocavity is formed by shifting the neighboring airholes away from the center of the cavity [236]. Partially transmitting element (PTE), which is constituted by

[1] Fabrication and characterization of Fano switches was performed together with Dagmawi Alemayehu Bekele.

an additional airhole, is introduced in the center of the waveguide. The position of the PTE airhole in respect to the cavity controls the shape of the transmission spectrum [237]. In the case of this work, it is shifted one lattice period from the cavity, giving rise to asymmetric transmission lineshape, with the transmission minimum blue-shifted compared to the transmission maximum (blue-parity).

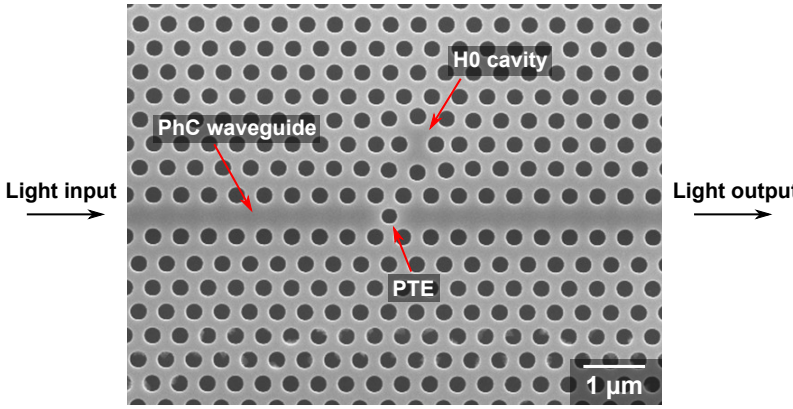


Figure 7.1: SEM image of a fabricated PhC InP membrane structure which exhibits Fano resonance. H0 nanocavity is side-coupled to PhC waveguide with PTE.

The theoretical calculation of a transmission spectrum of a such type of Fano structure is shown in Fig. 7.2. Optical switching of a signal located in a red-shaded spectral range can be performed by shifting the resonance via the cavity refractive index change. When the resonance is in initial state (solid line), the switched signal experiences minimum transmission (switch-off state), however, when the resonance is shifted (dashed line), the switched signal experiences maximum transmission (switch-on state).

The possibility to obtain an asymmetric lineshape with a small spectral separation between maximum and minimum transmission constitutes the advantage of Fano structures over the structures with symmetric Lorentzian lineshape in application for optical switching, since in order to achieve a similar level of the switching contrast, a smaller resonance shift is required in case of Fano structures compared to Lorentzian ones. Consequently, less energy is required to shift the Fano resonance between "off" and "on" states, which paves the way for energy efficient integrated optical switches [76, 238].

In case of the pump-probe based all-optical switching, the resonance shift is achieved by exciting the cavity mode by the pump signal. Since the PhC cavity is characterized by a strong temporal and spatial field confinement (high quality factor with low mode volume), this leads to highly localized intensity build-up in

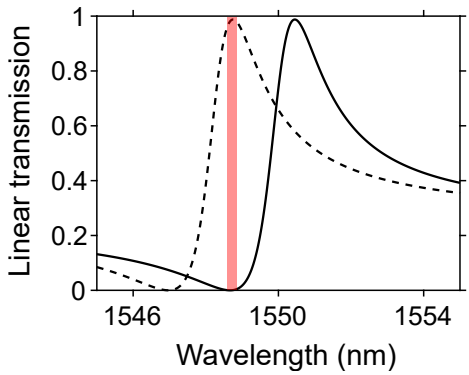


Figure 7.2: Theoretical calculation of the transmission of the Fano PhC structure (solid line). Dashed line represents the resonance shift induced by a decrease of the refractive index. The red shade represents the spectral location of a signal to be switched. Adapted from [207].

the cavity, which causes a change in the refractive index. In case of InP at telecom wavelengths, two-photon absorption (TPA) process dominates over Kerr effect, therefore, free carriers generated by TPA determine the refractive index change. Three carrier-induced nonlinear processes are distinguished: free carrier absorption (plasma dispersion), band filling and bandgap shrinkage effects [239]. In addition, the generated carriers also contribute to thermo-optic effect. The combination of all these processes results in a decrease of the cavity refractive index and the blue-shift of the resonance [76], as shown in Fig. 7.2.

7.1.1 Enhancement of operation speed

The drawback of utilizing carrier-induced refractive index change mechanism for all-optical switching is the limitation on the achievable operating speed imposed by carrier relaxation processes. The time scale of the resonance shift recovery is determined by the rate at which the initially accumulated TPA-generated free carriers leave the cavity region. Three main processes have a contribution: carrier diffusion, surface recombination and bulk recombination. Carrier bulk recombination in InP is a slow process with a typical time scale on the order of tens to hundreds of nanoseconds [240]. The fastest relaxation process is carrier diffusion, which, together with surface recombination, mainly determines the carrier dynamics in PhC cavities [241]. Due to high surface area to volume ratio in PhC structures, surface recombination is especially pronounced. In addition, the cavity design also has an influence on the carrier dynamics, with the fastest relaxation achieved for H0-type cavity due to ultrasmall size (fast outdiffusion) [75] and generation of carriers close to the airholes, where they can recombine (enhanced surface recombination) [242].

One way to improve the operation speed is to utilize p-doped InP membrane [243]. The idea is to enhance carrier relaxation due to much faster minority carrier (electron) diffusion in p-InP compared to ambipolar diffusion in intrinsic InP. However, in such case optical losses are expected to be increased.

Another option is to apply the electric field to sweep out the carriers from the cavity. However, the drawback can be the increased device power consumption. The possibility of carrier extraction from PhC cavity in Si was demonstrated by implementation of lateral metal-semiconductor-metal (MSM) Schottky junction [244] or lateral p-i-n junction [245]. However, MSM junction is disadvantageous due to the higher reverse current and the requirement to bring metal contacts very close to the cavity. In this work, the approach of lateral p-i-n junction for carrier sweep-out is applied to the Fano switch in InP membrane.

7.2 Fano switch with lateral p-i-n junction

The process flow of the fabrication of the Fano switches is essentially the same as for the lasers, with only the BH definition stage being skipped. Instead, the work is done on passive InP membranes without the active material.

The optical microscope image of the fabricated Fano switch with lateral p-i-n junction in InP membrane on SiO_2/Si substrate is shown in Fig. 7.3(a). Light is coupled from the fiber to InP wire waveguide via the grating coupler (shown in Fig. 7.3b) at an incident angle of 13°. The light is guided by an InP wire waveguide, which is tapered down to fit the PhC waveguide. The PhC part (shown in Fig. 7.3c) has the Fano design with H0 nanocavity and PTE airhole, as already demonstrated in Fig. 7.1. Reverse bias voltage is applied to metal contacts, which generates the electric field across the PhC Fano cavity located in the intrinsic region of the lateral p-i-n junction, and the carriers are swept out from the cavity under the applied electric field. The light is then outcoupled to the fiber through another InP wire waveguide and the grating coupler. The total length of the device is 1.1 mm in order to be able to fit the coupled optical fibers in the setup. It should be noted that the demonstrated device does not have Si-implanted regions, with n-type InP achieved only by Ge doping underneath Ni/Ge/Au metal contacts. This is suboptimal structure due to large intrinsic area and, as a consequence, lower electric field intensity. Unfortunately, the samples with performed Si ion implantation were unsuccessful due to the difficulties at PhC and grating couplers dry etching stage.

As shown in Fig. 7.4(a), the fabricated device exhibited typical for p-i-n junctions IV characteristic, which is similar to demonstrated in Fig. 6.1, where Si ion implantation was also skipped. The experimental transmission measurement of a fabricated device is shown in Fig. 7.4(b). Characteristic asymmetric lineshape is observed. Extinction ratio is ∼28 dB with the spectral separation of ∼2 nm between maximum and minimum transmission. The pronounced ripples are most likely caused by the reflections from the grating couplers used for fiber-device light

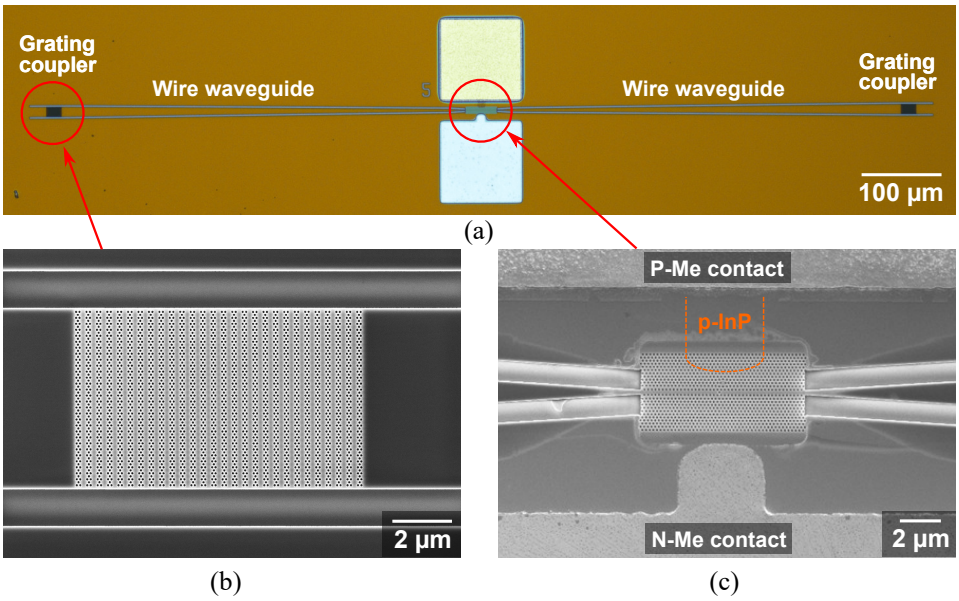


Figure 7.3: (a): Optical microscope image of the fabricated Fano switch. (b): SEM image of one of the grating couplers. (b): SEM image of the main part of the device. Lateral p-i-n junction is fabricated across the PhC. Note that Si ion implantation was not performed for this device.

coupling.

The switching capability of the fabricated Fano structure is demonstrated in wavelength conversion experiment, which involves the transfer of a bit pattern from one wavelength (pump signal) to the other (probe signal). The schematic of the experimental setup is shown in Fig. 7.5. 10 Gbit/s RZ-OOK (return-to-zero on-off keying) modulated pump signal is amplified and combined with CW low power probe signal. Since PhC waveguide supports TE-polarized guided modes, polarization of both signals is controlled. The spectral location of the pump signal is chosen to be close to the cavity resonance frequency, while the probe signal is located at the resonance transmission minimum (Fig. 7.4b). When the pump signal represents "0" bit, transmission of the probe signal is suppressed, but when the pump signal represents "1" bit, it excites the Fano cavity, causing the resonance blue-shift and enhanced probe signal transmission. Static reverse bias is applied to the lateral p-i-n junction across the PhC part of the device to sweep out the generated carriers from the cavity and accelerate the process of resonance shift-back. After the device, the probe signal is filtered, amplified and detected by 10 Gbit/s receiver.

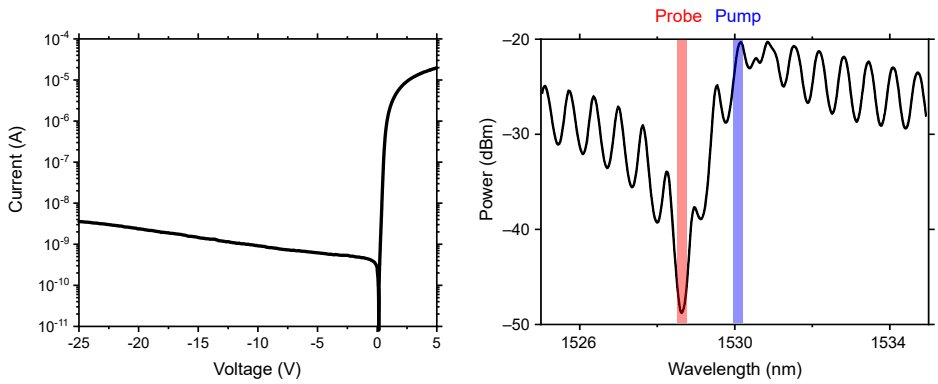


Figure 7.4: (a): IV characteristic of a p-i-n junction in the fabricated Fano switch. (b): Experimental transmission spectrum of the fabricated Fano switch.

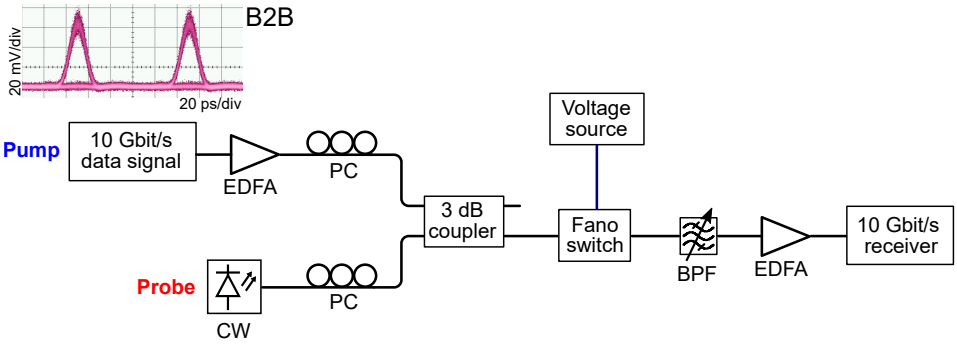


Figure 7.5: Schematic of the setup used for the wavelength conversion experiment. EDFA stands for erbium-doped fiber amplifier, PC for polarization controller, BPF for bandpass filter. Eye diagram of the back-to-back (B2B) reference measurement, performed by sending the pump 10 Gbit/s signal directly to the receiver bypassing the Fano switch, is shown.

The obtained eye diagrams of the wavelength converted signal with varied applied reverse bias are demonstrated in Fig. 7.6. Under no applied bias (0 V), the slowly decaying transmission tail is clearly visible. It is caused by the slow relaxation of the TPA-generated free carriers in the cavity region. When the reverse bias voltage is applied, the signal tail can be noticed to become less pronounced, which indicates the successful enhancement of carrier relaxation by sweeping the carriers out from the cavity by applied electric field. However, it should be noted that the observed effect is far from being very pronounced, which is attributed to

not optimal lateral p-i-n junction configuration in this particular sample (Si ion implantation was skipped due to unavailability of the equipment). The same explanation applies to the problem of a quite high reverse bias needed to observe the effect (tens of volts). If the intrinsic region length is reduced by defining n-InP area by Si ion implantation, much lower voltage is expected to be required to achieve high electric field intensity in the intrinsic region for efficient carrier extraction [246]. It should also be noted that the high noise level is caused by the significant coupling losses to and from the device due to fabrication challenge of obtaining the targeted parameters of the grating couplers.

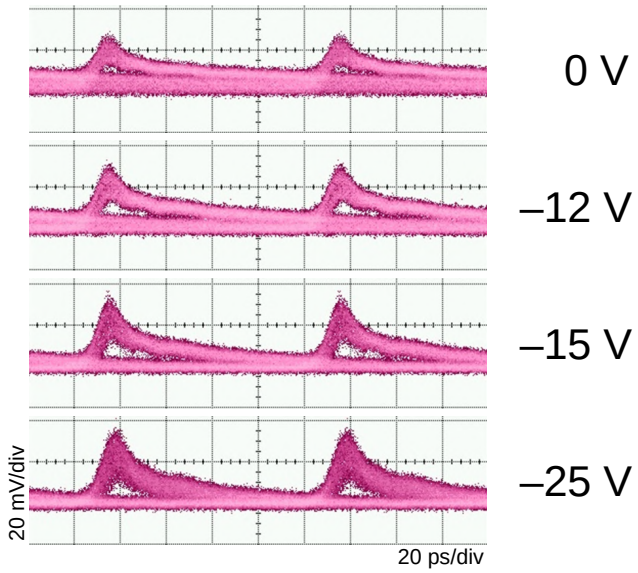


Figure 7.6: Eye diagrams of the wavelength converted 10 Gbit/s signal under the varied reverse bias voltage in lateral p-i-n junction across the Fano switch. Noticeable reduction of the signal tail is observed under the applied reverse bias.

In a rather different application area, absolutely the same configuration of Fano PhC structure with lateral p-i-n junction can also be utilized as a thermo-optic switch. If a forward bias is applied to the p-i-n junction, generated heat induces the refractive index increase due to thermo-optic effect, which leads to the red-shift of the Fano resonance. Thermo-optic switching on the $\sim$10 µs time scale was successfully demonstrated in our other work [247].

Chapter 8

Conclusion and outlook

8.1 Summary and conclusion

The focus of this work was on the development of the technologies for experimental realization of electrically pumped buried heterostructure (BH) photonic crystal (PhC) lasers and PhC all-optical switches based on Fano resonance on InP-on-Si platform. A special attention was brought to the selective area doping technologies for the fabrication of lateral p-i-n junction in InP membrane directly bonded to Si substrate, which is essential for current injection into the laser active region, as well as for carrier sweep-out from the Fano switch cavity.

Silicon ion implantation process was investigated for the purpose of n-type InP doping. Various process aspects, such as ion energy, ion dose and activation annealing details, were studied. Deposition of borophosphosilicate glass (BPSG) capping layer was developed for Si activation by rapid thermal annealing (RTA) of implanted InP membrane on Si substrate at temperatures up to 800 °C with not degraded material morphology. Sheet resistance values as low as 75 Ω/□ with the corresponding electron concentration of $3 \times 10^{18}\,\mathrm{cm}^{-3}$ were achieved for 250 nm thick n-InP after Si activation by RTA at 800 °C. However, that high temperature was found to significantly degrade the emission properties of quantum well (QW) active layer due to thermal stress caused by thermal expansion coefficient mismatch between the membrane and the substrate. A trade-off between high Si activation and low QW degradation was found at the annealing temperature of 650 °C, with the obtained electron concentration at $10^{18}\,\mathrm{cm}^{-3}$ level. The possible drawback of undesired overall p-type doping was solved by introduction of additional resist strip step, which helped to eliminate the implanted resist crust.

Zinc thermal diffusion process in metalorganic vapor phase epitaxy (MOVPE) reactor was studied for selective area p-type InP doping. Diffusion temperature, Zn source flow, arsine flow, surface pre-treatment factors were investigated regarding the influence on electrical properties of p-InP membrane. The lowest achieved

sheet resistance of 250 nm thick p-InP was 903 Ω/□ with the estimated hole concentration of $\sim 3 \times 10^{18}\,\mathrm{cm}^{-3}$. The effect of etching PhC airholes on the reduction of membrane conductivity was quantified. The issue of Zn-induced material deterioration was identified and solved. The mass transport controlled regime of Zn diffusion process was evidenced. In addition, lateral dopant redistribution was characterized for both p-type and n-type InP.

The complete sequence of fabrication of BH PhC lasers, as well as PhC Fano switches with lateral p-i-n junction, was developed and optimized. Various fabrication aspects, such as alignment marks etching procedure, elimination of undesired III-V material grown on top of alignment marks during BH definition, were addressed and improved.

Regarding lasers, light emission under current injection was observed for BH PhC devices with three layers of QWs. Unfortunately, room temperature lasing was not achieved due to unresolved at that point of time fabrication issues of Zn-induced morphology degradation and suboptimal dry etching of PhC pattern on a 4" substrate. Those issues were later solved, and there are high expectations of the ongoing work.

In case of Fano switches, pump-probe wavelength conversion experiment was successfully performed. The evidence was observed for carrier lifetime reduction in Fano cavity due to carrier sweep-out under reverse bias applied to lateral p-i-n junction, which paves the way for higher speed operation of PhC Fano all-optical switches. Although, the effect was not pronounced due to suboptimal p-i-n junction configuration with extended intrinsic region, with the significant progress expected in ongoing work.

8.2 Outlook

Doping technologies for InP membrane on Si substrate have been developed, however, devices demonstration was greatly hindered by the various fabrication issues and large typical time scale of the processing with significant equipment related delays. However, based on the performed groundwork and established design and fabrication sequence within the framework of NATEC HERO project, significant progress is expected in the nearest future. In fact, at the time of finishing this thesis, the second generation of NATEC HERO samples with not degraded morphology of p-doped InP was already at the stage of PhC dry etching. Full exploitation of the extensive NATEC HERO design with a wide variety of device configurations is expected to remedy the current lack of performing devices. In particular, electrically pumped Fano BH lasers with tunable Fano mirror and integrated on-chip photodetectors are of great interest. Additional interest is brought by the samples with InAs quantum dots as active material.

In addition, further improvement of Fano switches capability for high speed operation is anticipated with the implementation of optimized lateral p-i-n junction

design with n-type InP defined by Si ion implantation. Static electric field would become much stronger across the Fano cavity, which would result in more efficient carrier sweep-out and, consequently, further reduced carrier lifetime.

Appendix A

Process flow

In this chapter, the detailed step-by-step optimized process flow is presented for fabrication of electrically pumped BH PhC membrane lasers. In case of all-optical Fano switches or doping test samples, there are some alterations, as discussed in Chapter 4.

Step Heading	**Equipment**	**Procedure**	**Comments**
1. **Initial steps before bonding**			
1.1. *MOVPE sample growth*			**InP substrate (50 mm)**
1.1.1. Epitaxial growth	MOVPE	Grow InP with active QWs or QDs layers + Ga(1-x)In(x)As etch-stop layer (x = 0.53, d = 200 – 250nm)	InP layer thickness (depending on the active layers) d = 170 – 200 nm (aiming for the final device thickness of d = 250 nm)
1.1.2. PL characterization	PL mapper	532/980 nm, surface-map/wide-scan	
1.2. *Si thermal oxidation*			**Si substrate (100 mm)**
1.2.1. Thermal oxidation	Furnace: Anneal-oxide (C1)	Wet oxidation at 1100°C for 4h05min Annealing for 20min	Expected SiO_2 thickness 1085 nm
1.2.2. SiO_2 thickness measurement	Ellipsometer VASE		
2. **Direct bonding**			
2.1. *Al_2O_3 deposition in ALD for realization of bonding interface*			**2" InP with 4" SiO_2/Si**
2.1.1. Dummy run	ALD	Temperature: 250 °C Deposition: 25x(Al_2O_3+H_2O), 4xH_2O	Empty chamber
2.1.2. Loading	ALD	Gently place wafers on the metal grid, close the chamber, evacuate	

Step Heading	**Equipment**	**Procedure**	**Comments**
2.1.3. Deposition run	ALD	Temperature: 250 °C Deposition: 25x(Al_2O_3+H_2O), 4xH_2O	
2.2. *Wafer pre-bonding*			**2" InP with 4" SiO_2/Si**
2.2.1. Si wafer unloading	Teflon bonding chuck	Place and align on the teflon chuck (face up), add the teflon corner tool on top	
2.2.2. InP wafer unloading	Teflon bonding chuck	Position and align a few mm above the Si wafer (face down)	
2.2.3. Putting in contact	Teflon bonding chuck	Release the InP wafer, let it drop on Si, guided by the teflon corner tool	
2.2.4. Applying pressure	Teflon pressing tool	Quickly press with the Teflon pressing tool in the middle of the InP wafer, then press around	At this point, wafers should be sticked together
2.3. *Wafer bonding in a wafer bonder*			**2" InP with 4" SiO_2/Si**
2.3.1. Loading	Wafer Bonder 02	Place on the chuck	
2.3.2. Bonding process	Wafer Bonder 02	Recipe: "300Cbonding - 2to4inch" Temperature: 300 °C Force: 2 kN Pressure: vacuum	Total time ~2.5 h
2.3.3. Unloading	Wafer Bonder 02		Inspect if no cracks are visible
2.4. *Substrate removal*			
2.4.1. Wet etching	HCl	Time: ~1 h	Preferably use magnetic stirrer for agitation
2.4.2. Rinse	DI water		
2.4.3. Blow dry	N_2		
2.5. *Stop layer removal*			
2.5.1. InGaAs wet etching	H_2SO_4, H_2O_2	Mixture: (10 %)H_2SO_4:H_2O_2 = 1:1 Time: 30 s	
2.5.2. Rinse	DI water		
2.5.3. Blow dry	N_2		
2.6. *PL mapping*			
2.6.1. Emission characterization	PL mapper	532/980 nm, surface-map/wide-scan	Use the same parameters as before for comparison
2.7. *Thickness mapping*			

Step Heading	**Equipment**	**Procedure**	**Comments**
2.7.1. Thickness estimation	Ellipsometer VASE	Angle scan: 65° – 70° – 75° Acq. time: 5 s	
3. **Opening pre-alignment areas for alignment marks**			**UV with positive resist**
3.1. *Adhesion promoting*			
3.1.1. Baking	Hot plate	5 min, 100 °C	
3.1.2. Adhesion promoting	Surpass3000	1 min dip	
3.1.3. Rinse (beaker)	DI water	1 min dip	
3.1.4. Rinse	DI water		
3.1.5. Blow dry	N_2		
3.2. *AZ5214 spin coating*			
3.2.1. AZ5214 spin coating	Spin coater: Gamma UV	Sequence (3410 on Gamma UV, 4110 on Gamma e-beam & UV) DCH 100mm 5214E 1.5um. It includes 1) Dispense 3ml@800rpm 2) Spin-off for 30s@4500rpm 3) Soft baking for 90s@90C.	Expected thickness 1.5um Without HMDS
3.3. *UV exposure*			
3.3.1. UV exposure	Aligner MA6-2	Mask “HERO NATEC PRE-ALIGN” (dark field) Flat alignment Hard contact mode Time 7s, intensity 11 mW/cm2	
3.4. *AZ5214 development*			
3.4.1. Development	Developer: TMAH UV-lithography	Sequence: DCH 100mm SP 60s	
3.5. *Descum*			
3.5.1. Plasma ashing	Plasma Asher 1	20 s, 0.8 mbar, O2 = 300 ml/min, power 400 W	
3.6. ***(Only QDs)*** *Dry etching of openings for alignment marks*			
3.6.1. Chamber preparation	III-V ICP	Temperature: heat up 20°C–120°C Chamber cleaning: 30 min O_2 clean	

Step Heading	**Equipment**	**Procedure**	**Comments**
3.6.2. Chamber preconditioning	III-V ICP	Recipe: InP_HBr_prealign_andrma Time: 15 min Carrier: dummy 4” AZ5214/Si	
3.6.3. Dry etching	III-V ICP	Recipe: InP_HBr_prealign_andrma Time: 15 min	Could be that additional etching time is needed, decide after inspection
3.6.4. Unloading	DI water	Put into the glass beaker with DI water to neutralize Br	
3.6.5. Chamber cleaning	III-V ICP	30 min O_2 clean Temperature: cool down 120°C–20°C	
3.6. ***(Only QWs)*** *Wet etching of III-V in openings for alignment marks*			
3.6.1. InP wet etching	1HCl : $4H_3PO_4$	30 s	With stirring
3.6.2. QWs wet etching	$1H_2SO_4$(10%) : $1H_2O_2$	30 s	
3.6.3. InP wet etching	1HCl : $4H_3PO_4$	30 s	With stirring. Could be that additional etching time is needed, decide after inspection
3.7. *Dry etching of SiO_2 in openings for alignment marks*			
3.7.1. Chamber preparation	III-V ICP	Chamber cleaning: 15 min O_2 clean	
3.7.2. Chamber preconditioning	III-V ICP	Recipe: SiO2_andrma Time: 15 min Carrier: dummy 4” AZ5214/Si	
3.7.3. Dry etching	III-V ICP	Recipe: SiO2_andrma Time: 23 min	Etch rate 44 nm/min SiO_2 is not fully etched (to avoid Si surface bombardment)
3.7.4. Chamber cleaning	III-V ICP	15 min O_2 clean	
3.8. *Resist stripping*			
3.8.1. Stripping	Acetone	~5 min	Could be difficult in case of samples with III-V dry etching since resist is effectively hard baked in ICP.
3.8.2. Cleaning	IPA / ethanol	Rinse	
3.8.3. Cleaning	DI water	Rinse	
3.8.4. Blow dry	N_2		

Step Heading	**Equipment**	**Procedure**	**Comments**
3.8.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	In case of failed acetone strip longer plasma ashing is needed
3.9. *SiO_2 wet etch*			
3.9.1. Wet etching	BHF	Time = 3 min	Thermal SiO_2 etch rate 75 nm/min. Check with dektak that all remaining SiO_2 is etched.
4. **Alignment marks definition**			**UV with positive resist**
4.1. *Adhesion promoting*			
4.1.1. Baking	Hot plate	5 min, 100 °C	
4.1.2. Adhesion promoting	Surpass 3000	1 min dip	
4.1.3. Rinse (beaker)	DI water	1 min dip	
4.1.4. Rinse	DI water		
4.1.5. Blow dry	N_2		
4.2. *AZ5214 spin coating*			
4.2.1. AZ5214 spin coating	Spin coater: Gamma UV	Sequence (3410 on Gamma UV, 4110 on Gamma e-beam & UV) DCH 100mm 5214E 1.5um. It includes 1) Dispense 3ml@800rpm 2) Spin-off for 30s@4500rpm 3) Soft baking for 90s@90C.	Expected thickness 1.5um Without HMDS
4.3. *UV exposure*			Check mask cleanliness before exposure, if necessary, clean mask in H_2SO_4
4.3.1. UV exposure	Aligner MA6-2	Mask “HERO NATEC ALIGN MARKS” (dark field) Alignment to “A” alignment marks Hard contact mode Time 7s, intensity 11 mW/cm2	Alignment doesn’t need to be very accurate
4.4. *AZ5214 development*			
4.4.1. Development	Developer: TMAH UV-lithography	Sequence (1002): DCH 100mm SP 60s	
4.5. *Descum*			
4.5.1. Plasma ashing	Plasma Asher 1	10 s, 0.8 mbar, O2 = 300 ml/min, 400 W	

Step Heading	**Equipment**	**Procedure**	**Comments**
4.6. *Alignment marks etching*			
4.6.1. Chamber preparation	III-V ICP	Chamber cleaning: 30 min O_2 clean	
4.6.2. Chamber preconditioning	III-V ICP	Recipe: "Si_etch_SF6_O2_andrma" Time: 4 min Carrier: dummy 4" AZ5214/Si	
4.6.3. Si etching using AZ5214E mask	III-V ICP	Recipe: "Si_etch_SF6_O2_andrma" Time: 50 s	
4.6.4. Chamber cleaning	III-V ICP	30 min O_2 clean	
4.7. *Resist strip*			
4.7.1. Stripping	Acetone	~5 min	
4.7.2. Cleaning	IPA / ethanol	Rinse	
4.7.3. Cleaning	DI water	Rinse	
4.7.4. Blow dry	N_2		
4.7.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
5. **BH definition**			**e-beam with negative resist**
5.1. *Sample surface preparation before e-beam resist coating*			
5.1.1. Wet etching	BHF	Time: >10 s	A very important step for proper HSQ adhesion to the InP surface. Also BHF removes possible Si etching residues
5.1.2. Rinse	DI water		
5.1.3. Blow dry	N_2		
5.2. *E-beam resist coating*			
5.2.1. Baking	Hot plate	5 min, 220 °C	
5.2.2. Spin-coating	HSQ Fox-15	60 s, 6000 RPM, 3000 /s^2	Take the HSQ bottle out of the refrigerator ~30 min before opening
5.2.3. Baking	Hot plate	2 min, 120 °C 2 min, 220 °C	
5.3. *Buried heterostructure mask exposure in e-beam*			

Step Heading	Equipment	Procedure	Comments
5.3.1. Cassette loading	E-beam	preferably 4" Ti cassette	Keep the cassette inside the e-beam machine for >30 min to stabilize the temperature, check it with the temperature monitor software
5.3.2. Pre-alignment	E-beam pre-alignment stage	Choose good quality P and Q global alignment marks	
5.3.3. Exposure	E-beam	Condition file: 45na_ap8 Dose: 3800 μC/cm^2, with PEC Alignment: P and Q global marks; chip marks for individual chips	Optimized e-beam alignment marks detection parameters (InP marks on SiO_2): BE Coarse gain: 1 BE Middle gain: 12 BE Fine gain: 128 WAVE offset: 128 BE offset: 1806 16 scans for chip marks.
5.4. *E-beam resist development*			
5.4.1. Development	AZ400K, H_2O	Mixture: AZ400K:H_2O = 1:3 Time: 2 min 40 s	
5.4.2. Rinse	DI wafer		
5.4.3. Blow dry	N_2		
5.5. *Formation of mesa-structures by dry etching*			
5.5.1. Chamber preparation	III-V ICP	Temperature: heat up to 180 °C Chamber cleaning: run 30 min O_2 clean	
5.5.2. Chamber preconditioning	III-V ICP	Recipe: ausa/"HBr etch (low p)" Time: 15 min Carrier: dummy 4" Si	Updated recipe with pressure reduced from 5 to 1 mTorr (and added strike pressure to ignite plasma), resulting in better sidewall roughness
5.5.3. Dry etching	III-V ICP	Recipe: ausa/"HBr etch (low p)" Time: 20 – 60 s	Better set etch time for a couple of minutes and then stop manually by tracking EtchDirector signal according to the sample layer model
5.5.4. Unloading	DI water	Put into the glass beaker with DI water to neutralize Br	
5.5.5. Chamber cleaning	III-V ICP	30 min O_2 clean if no more InP etching is done	

Step Heading	**Equipment**	**Procedure**	**Comments**
5.6. *Thickness mapping*			
5.6.1. Thickness estimation	Ellipsometer VASE	Angle scan: 65° – 70° – 75° Acq. time: 5 s	
5.7. *Sample preparation for the 1st re-growth*			**Right before the re-growth**
5.7.1. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
5.7.2. Cleaning/wet etching	H_2SO_4	Mixture: concentrated H_2SO_4 Time: 3 min	~25 nm InP etch assumed; use new H_2SO_4 every time, because re-using it can cause problems (particles after re-growth); etch in the III-V fumehood, rinse the sample and then transport it in the beaker with water to the MOVPE wetbench for additional DIW rinsing
5.7.3. Rinse	DI water	Time: 1 min	
5.7.4. Rinse (bubbler)	DI water	Time: 3 min	
5.7.5. Blow dry	N_2		No more tweezers, use vacuum handler
5.8. *1st MOVPE re-growth (selective area growth)*			
5.8.1. Sample loading into the load-lock	MOVPE	Load and evacuate for >15 min	Make sure wafer backside is completely dry
5.8.2. InP regrowth	MOVPE	Regrowth thickness: aiming for what was etched in III-V ICP + H_2SO_4 cleaning/etching	Estimated from the EtchDirector data and from comparing ellipsometer thickness maps
5.9. *Thickness mapping*			
5.9.1. Thickness estimation	Ellipsometer VASE	Angle scan: 65° – 70° – 75° Acq. time: 5 s	
5.10. *E-beam resist removal from the buried heterostructure regions*			
5.10.1. Wet etching	BHF	Time: 2 min	
5.10.2. Rinse	DI water		
5.10.3. Blow dry	N_2		
5.11. *Sample preparation for the 2nd re-growth*			**Right before the re-growth**
5.11.1. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	

Step Heading	Equipment	Procedure	Comments
5.11.2. Cleaning/wet etching	H_2SO_4	Mixture: concentrated H_2SO_4 Time: 3 min	~25 nm InP etch assumed; use new H_2SO_4 every time, because re-using it can cause problems (particles after re-growth); etch in the III-V fumehood, rinse the sample and then transport it in the beaker with water to the MOVPE wetbench for additional DIW rinsing
5.11.3. Rinse	DI water	Time: 1 min	
5.11.4. Rinse (bubbler)	DI water	Time: 3 min	
5.11.5. Blow dry	N_2		No more tweezers, use vacuum handler
5.12. *2nd MOVPE re-growth (planarization)*			
5.12.1. Sample loading into the load-lock	MOVPE	Load and evacuate for >15 min	Make sure wafer backside is completely dry
5.12.2. InP regrowth	MOVPE	Re-growth thickness: aiming for 250 nm final InP membrane thickness and 50 nm InGaAs thickness	Estimated from comparing ellipsometer thickness maps
5.13. *Thickness mapping*			
5.13.1. Thickness estimation	Ellipsometer VASE	Angle scan: 65° – 70° – 75° Acq. time: 5 s	
6. **Alignment marks cleaning from grown III-V**			**UV with positive resist**
6.1. *Adhesion promoting*			
6.1.1. Baking	Hot plate	5 min, 100 °C	
6.1.2. Adhesion promoting	Surpass 3000	1 min dip	
6.1.3. Rinse (beaker)	DI water	1 min dip	
6.1.4. Rinse	DI water		
6.1.5. Blow dry	N_2		
6.2. *AZ5214 spin coating*			
6.2.1. AZ5214 spin coating	Spin coater: Gamma UV	Sequence DCH 100mm 5214E 4.2um.	Expected thickness 4.2um Without HMDS
6.3. *UV exposure*			

Step Heading	**Equipment**	**Procedure**	**Comments**
6.3.1. UV exposure	Aligner MA6-2	Mask "HERO NATEC PRE-ALIGN" (dark field) Hard contact mode Time 25s, intensity 11 mW/cm2	Rough alignment to existing pattern
6.4. *AZ5214 development*			
6.4.1. Development	Developer: TMAH UV-lithography	Sequence (1002): DCH 100mm SP 60s	
6.5. *Descum*			
6.5.1. Plasma ashing	Plasma Asher 1	20 s, 0.8 mbar, O2 = 300 ml/min, 400 W	
6.6. *Hard bake*			
6.6.1. Hard bake	Developer: TMAH UV-lithography / Stepper	130°C 90s	
6.7. *III-V wet etching*			
6.7.1. InGaAs etch	$1H_2SO_4$(10%) : $1H_2O_2$	2 min	
6.7.2. InP etch	1HCl : $4H_3PO_4$	40 min (with stirring)	
6.8. *Resist strip*			
6.8.1. Stripping	Acetone	~5 min	
6.8.2. Cleaning	IPA / ethanol	Rinse	
6.8.3. Cleaning	DI water	Rinse	
6.8.4. Blow dry	N_2		
6.8.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
7. **Si ion implantation**			**DUV with positive resist**
7.1. *DUV resist coating*			
7.1.1. BARC spin coating	Spin coater: Süss Stepper	Sequence (1202) DCH 100mm BARC 65nm	Dispense 1.6ml@1000rpm; spin-off 30s@3000rpm; softbake 60s@175°C
7.1.2. KRF M35G spin coating	Spin coater: Süss Stepper	Sequence (1402) DCH 100mm KRF M35G 750nm	Dispense 1ml@1000rpm; spin-off 60s@5000rpm; softbake 90s@130°C
7.2. *DUV exposure*			
7.2.1. Loading sample	4"—>6" adapter		

Step Heading	Equipment	Procedure	Comments
7.2.2. DUV exposure	DUV stepper Canon FPA 3000	Reticle "NATEC_Hero_N_doped". Dose 350 J/m2 Focus offset -0.25um Semi-manual TVPA alignment, automatic AGA alignment in 4 chips	
7.3. *Development*			
7.3.1. Post-exposure bake and development	Developer TMAH: Stepper	Sequence (1003) DCH PEB_90s and DEV_60s	It is possible to run separate sequences for PEB and development
7.4. *Si ion implantation*			
7.4.1. Si ion implantation	Ion Beam Services	Dose $2x10^{14}$ cm^{-2} Tilt 7° RT Rotation 30°	Send samples to Ion Beam Services. Implantation is done in BARC/InGaAs/InP
7.5. *Resist strip*			
7.5.1. Plasma ashing	Plasma Asher 1	20 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
7.6. *Resist crust removal*			
7.6.1. Wet etching	BHF	BHF (standard, 7:1) 1 min.	Very important step to avoid overall p-doping
7.6.2. Rinse	DI water		
7.6.3. Blow dry	N_2		
8. **Zn diffusion**			**DUV with positive resist**
8.1. *Hard mask (SiO_2) deposition*			
8.1.1. SiO_2 PECVD	PECVD4	HF SiO2 with wafer clean for 94 s.	Test on a dummy. Thickness 100 nm.
8.2. *DUV resist coating*			
8.2.1. BARC spin coating	Spin coater: Süss Stepper	Sequence (1202) DCH 100mm BARC 65nm	Dispense 1.6ml@1000rpm; spin-off 30s@3000rpm; softbake 60s@175°C
8.2.2. KRF M35G spin coating	Spin coater: Süss Stepper	Sequence (1402) DCH 100mm KRF M35G 750nm	Dispense 1ml@1000rpm; spin-off 60s@5000rpm; softbake 90s@130°C
8.3. *DUV exposure*			
8.3.1. Loading sample	4"—>6" adapter		

Step Heading	Equipment	Procedure	Comments
8.3.2. DUV exposure	DUV stepper Canon FPA 3000	Reticle "NATEC_Hero_P_doped". Dose 350 J/m2 Focus offset -0.25um Semi-manual TVPA alignment, automatic AGA alignment in 4 chips	
8.4. *Development*			
8.4.1. Post-exposure bake and development	Developer TMAH: Stepper	Sequence (1003) DCH PEB_90s and DEV_60s	It is possible to run separate sequences for PEB and development
8.5. *BARC etching*			
8.5.1. BARC dry etching	III-V RIE	Recipe "BCB_LP" 1 min.	
8.6. *Pattern transfer to SiO_2 hard mask (SiO_2 etching)*			
8.6.1. Chamber preparation	III-V ICP	Chamber cleaning: 30 min O_2 clean	
8.6.2. Chamber preconditioning	III-V ICP	Recipe: "SiO2_CF4_H2_v1" Time: 15 min Carrier: dummy 4" AZ5214/Si	
8.6.3. Si etching using AZ5214E mask	III-V ICP	Recipe: "SiO2_CF4_H2_v1" Time: 190s	
8.6.4. Chamber cleaning	III-V ICP	30 min O_2 clean	
8.7. *Resist strip*			
8.7.1. Stripping	Acetone	~5 min	
8.7.2. Cleaning	IPA / ethanol	Rinse	
8.7.3. Cleaning	DI water	Rinse	
8.7.4. Blow dry	N_2		
8.7.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
8.8. *Sample preparation for Zn diffusion*			Set DEZn bubbler T to 30°C at least several hours before (if InGaAs is lattice matched enough).
8.8.1. Cleaning	H_2SO_4	Time: 3 min	
8.8.2. Rinse	DI water	Time: 1 min	
8.8.3. Rinse (bubbler)	DI water	Time: 3 min	
8.8.4. Blow dry	N_2		Use vacuum handler
8.9. *Zn diffusion (MOVPE)*			

Step Heading	Equipment	Procedure	Comments
8.9.1. Zn diffusion	MOVPE	1) T=650°C, t=15min, AsH_3=175sccm 2) RT control, T=505°C, t=20min, AsH_3=50sccm, $DEZn_{eff}$=6.9sccm, Pr.=500sccm	DEZn bubbler T=30°C (if InGaAs is properly lattice matched), otherwise T=18°C
8.10. *Zn activation*			
8.10.1. Rapid thermal annealing	Jipelec RTP	T/C control T = 450°C t = 5 min N_2 200 sccm	Always do a dummy run to calibrate T setpoint
8.11. *Hard mask removal (SiO_2 wet etching)*			
8.11.1. SiO_2 wet etching	BHF	t = 1 min.	
8.11.2. Rinse	DI water		
8.11.3. Blow dry	N_2		
9. **InGaAs etching**			**UV with positive resist**
9.1. *Adhesion promoting*			
9.1.1. Baking	Hot plate	5 min, 100 °C	
9.1.2. Adhesion promoting	Surpass3000	1 min dip	
9.1.3. Rinse (beaker)	DI water	1 min dip	
9.1.4. Rinse	DI water		
9.1.5. Blow dry	N_2		
9.2. *AZ5214 spin coating*			
9.2.1. AZ5214 spin coating	Spin coater: Gamma UV	Sequence (3410 on Gamma UV, 4110 on Gamma e-beam & UV) DCH 100mm 5214E 1.5um. It includes 1) Dispense 3ml@800rpm 2) Spin-off for 30s@4500rpm 3) Soft baking for 90s@90C.	Expected thickness 1.5um Without HMDS
9.3. *UV exposure*			
9.3.1. UV exposure	Aligner MA6-2	Mask "HERO_InGaAs_cap" (bright field) Alignment to "IGA" alignment marks Hard contact mode Time 7s, intensity 11 mW/cm2	

Step Heading	**Equipment**	**Procedure**	**Comments**
9.4. *AZ5214 development*			
9.4.1. Development	Developer: TMAH UV-lithography	Sequence: DCH 100mm SP 60s	
9.5. *Hard bake*			To improve resist durability during wet etching
9.5.1. Hard bake	Developer: TMAH UV-lithography	130°C 90s	
9.6. *Descum*			
9.6.1. Plasma ashing	Plasma Asher 1	20 s, O2 = 300 ml/min, 400 W, 0.8 mbar	
9.7. *InGaAs wet etching*			
9.7.1. InGaAs wet etching	$1H_2SO_4$(10%) : $8H_2O_2$: $8H_2O$	20 s.	Diluted etching solution. Endpoint can be detected by observing change of colour.
9.8. *Resist strip*			
9.8.1. Stripping	Acetone	~5 min	
9.8.2. Cleaning	IPA / ethanol	Rinse	
9.8.3. Cleaning	DI water	Rinse	
9.8.4. Blow dry	N_2		
9.8.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
10. **PhC definition**			**e-beam with positive resist**
10.1. *Hard-mask deposition*			
10.1.1. Test deposition	PECVD4	Recipe: "HF SIN with wafer clean" Time: ~17 min	On dummy Si
10.1.2. Thickness estimation	Ellipsometer VASE	Determine SiN_x thickness and deposition rate on dummy Si	
10.1.3. Real deposition	PECVD4	Recipe: "HF SIN with wafer clean" Time: ? min	Aim for ~100 nm (reduced thickness from earlier 200 nm for better dry etching)
10.2. *E-beam alignment/exposure of photonic crystal patterns*			
10.2.1. Baking	Hot plate	5 min, 180 °C	
10.2.2. Resist coating	ZEP520A	5 s, 500 RPM, 200 /s^2 60 s, 2600 RPM, 1500 /s^2	
10.2.3. Baking	Hot plate	3 min, 180 °C	

Step Heading	Equipment	Procedure	Comments
10.2.4. Cassette loading	E-beam	preferably 2" Ti cassette, slot D	Keep the cassette inside the e-beam machine for >30 min to stabilize the temperature, check it with the temperature monitor software
10.2.5. Pre-alignment	E-beam pre-alignment stage	Choose good quality P and Q global alignment marks	
10.2.6. Exposure	E-beam	Condition file: 2na_ap4 Dose: 260 – 290 μC/cm^2, with PEC Alignment: P and Q global marks; chip marks for individual chips	Optimized e-beam alignment marks detection parameters (InP marks on SiO_2): BE Coarse gain: 1 BE Middle gain: 15 BE Fine gain: 200 WAVE offset: 85 BE offset: 2020 16 scans for chip marks.
10.3. *E-beam resist development*			
10.3.1. Development	Developer: E-beam	Recipe: N-50-180s Developer: ZED N50 Rinsing: IPA Time: 3 min	
10.4. *Transfer of the photonic crystal patterns into the hard-mask*			
10.4.1. Chamber preparation	III-V ICP	Chamber cleaning: run 30 min O_2 clean	
10.4.2. Chamber preconditioning	III-V ICP	Recipe: ausa/"SiNx etch w/ strike" Time: 15 min Carrier: dummy 4" Si	
10.4.3. Dry etching	III-V ICP	Recipe: ausa/"SiNx etch w/ strike" Time: 5 – 6.5 min	Track EtchDirector signal, for optimal etching signal should go through around 1.1 cycle
10.4.4. Chamber cleaning	III-V ICP	30 min O_2 clean	
10.5. *E-beam resist strip*			
10.5.1. Stripping	Ultrasonic bath	Mixture: Remover 1165 Level: 1 Temperature: <60 °C Time: 1 h	III-V ICP etching does not burn ZEP, so its removal is easier. Usually less than an hour is enough, bath can be set to heating just during the removal.
10.5.2. Cleaning	Acetone	~5 min	

Step Heading	**Equipment**	**Procedure**	**Comments**
10.5.3. Cleaning	IPA	Rinse	
10.5.4. Cleaning	Ethanol	Rinse	
10.5.5. Blow dry	N_2		
10.5.6. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
10.6. *Transfer of the photonic crystal patterns into the InP layer*			
10.6.1. Chamber preparation	III-V ICP	Temperature: heat up to 180 °C Chamber cleaning: run 30 min O_2 clean	
10.6.2. Chamber preconditioning	III-V ICP	Recipe: ausa/"HBr etch (low p), PP 80 W" Time: 15 min Carrier: dummy 4" Si	Recipe is the same as for BH etching, except that platen power is increased to 80 W for better sidewalls verticality
10.6.3. Dry etching	III-V ICP	Recipe: ausa/"HBr etch (low p), PP 80 W" Time: 75 s	Exact optimal time is still being optimized.
10.6.4. Unloading	DI water	Put into the glass beaker with DI water to neutralize Br	
10.6.5. Chamber cleaning	III-V ICP	30 min O_2 clean if no more InP etching is done	
11. **N-Me contacts**			**UV with negative resist** P-Me and N-Me cycles can be swapped
11.1. *nLOF2020 spin coating*			
11.1.1. nLOF2020 spin coating	Spin coater: Gamma UV	Sequence (2441) DCH 100mm nLOF 2020 4um HMDS.	Adhesion promotion is done with HMDS in spin coater since almost all the surface is covered with silicon nitride.
11.2. *UV exposure*			
11.2.1. UV exposure	Aligner MA6-2	Mask "HERO_N_Me" (bright field) Alignment to "N" alignment marks Hard contact mode Time 20s, intensity 11 mW/cm2	
11.3. *nLOF cross-linking and development*			

Step Heading	Equipment	Procedure	Comments
11.3.1. PEB and development	Developer: TMAH UV-lithography	Sequence: 3001 DCH 100mm PEB60s@110C+SP60s	Check alignment in optical microscope. Development time could be increased, but 60s is also fine
11.4. *Hard baking*			To improve resist durability during wet etching
11.4.1. Flood exposure	Aligner MA6-2	Time 30 s, intensity 11 mW/cm2	
11.4.2. Hard baking	Hotplates near manual spin coaters	1min@110C, 3min@150C, 15s@110C	Hotplate setpoints 121°C and 165°C. Heating and cooling is done in two steps to avoid possible cracks in resist
11.5. *Descum*			
11.5.1. Plasma ashing	Plasma Asher 1	20 s, O2 = 300 ml/min, 400 W, 0.8 mbar	
11.6. *Nitride wet etching*			
11.6.1. SiN_x wet etching	BHF	t = 2 min 15 s	Check the colour of the openings in the microscope, if nitride is fully etched. Be careful not to undercut resist too much. Etching time is for 100 nm SiNx.
11.6.2. Rinse	DI water		
11.6.3. Blow dry	N_2		
11.7. *N-Metal (Ni\Ge\Au) deposition*			
11.7.1. Metal e-beam evaporation	Physimeca / Temescal	Ni 40nm, Ge 50nm, Au 125nm. Deposition rate 5 Å/s.	Deposition rate is not very important
11.8. *Lift-off*			
11.8.1. Lift-off	Lift-off bench Remover 1165 bath	~15 min, 55°C – 60°C, ultrasound 9.	Large passive areas in e-beam chip #2 could take ~1h to be lifted off. Be careful with overheating as bench gives alarm at T>62°C.
11.8.2. Rinse	Lift-off bench IPA bath	5 min, RT, ultrasound 9.	
11.8.3. Rinse	Lift-off bench DI water bath	1 rinsing cycle.	
11.9. *Resist residues strip*			

Step Heading	**Equipment**	**Procedure**	**Comments**
11.9.1. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
12. **P-Me contacts**			**UV with negative resist**
12.1. *nLOF2020 spin coating*			
12.1.1. nLOF2020 spin coating	Spin coater: Gamma UV	Sequence (2441) DCH 100mm nLOF 2020 4um HMDS.	Adhesion promotion is done with HMDS in spin coater since almost all the surface is covered with silicon nitride.
12.2. *UV exposure*			
12.2.1. UV exposure	Aligner MA6-2	Mask "HERO_P_Me" (bright field) Alignment to "P" alignment marks Hard contact mode Time 20s, intensity 11 mW/cm2	
12.3. *nLOF cross-linking and development*			
12.3.1. PEB and development	Developer: TMAH UV-lithography	Sequence: 3001 DCH 100mm PEB60s@110C+SP60s	Check alignment in optical microscope. Development time could be increased, but 60s is also fine
12.4. *Hard baking*			To improve resist durability during wet etching
12.4.1. Flood exposure	Aligner MA6-2	Time 30 s, intensity 11 mW/cm2	
12.4.2. Hard baking	Hotplates near manual spin coaters	1min@110C, 3min@150C, 15s@110C	Hotplate setpoints 121°C and 165°C. Heating and cooling is done in two steps to avoid possible resist cracking
12.5. *Descum*			
12.5.1. Plasma ashing	Plasma Asher 1	20 s, O2 = 300 ml/min, 400 W, 0.8 mbar	
12.6. *Nitride wet etching*			
12.6.1. SiN_x wet etching	BHF	t = 2 min 15 s	Check the colour of the openings in the microscope, if nitride is fully etched. Be careful not to undercut resist too much. Etching time is for 100 nm SiNx.
12.6.2. Rinse	DI water		

Step Heading	Equipment	Procedure	Comments
12.6.3. Blow dry	N_2		
12.7. *P-Metal (Ti\Pt\Au) deposition*			
12.7.1. Metal e-beam evaporation	Physimeca / Wordentec / Temescal	Ti 30nm, Pt 50nm, Au 250nm. Deposition rate 5 Å/s.	Deposition rate is not very important
12.8. *Lift-off*			
12.8.1. Lift-off	Lift-off bench Remover 1165 bath	~15 min, 55°C – 60°C, ultrasound 9.	Large passive areas in e-beam chip #2 could take ~1h to be lifted off. Be careful with overheating as bench gives alarm at T>62°C
12.8.2. Rinse	Lift-off bench IPA bath	5 min, RT, ultrasound 9.	
12.8.3. Rinse	Lift-off bench DI water bath	1 rinsing cycle.	
12.9. *Resist residues strip*			
12.9.1. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	
12.10. *Me contact thermal alloying*			
12.10.1. Rapid thermal annealing	Jipelec RTP	Recipe “anma_nall2” T/C control T = 430°C t = 30 s N_2 200 sccm	Always do a dummy run to calibrate T setpoint. After annealing check N-Me colour, it should turn white (indication of successful alloying)
13. **Membranization**			**UV with positive resist**
13.1. *AZ5214 spin coating*			
13.1.1. AZ5214 spin coating	Spin coater: Gamma UV	Sequence (3421) DCH 100mm 5214E 2.2um HMDS.	
13.2. *UV exposure*			
13.2.1. UV exposure	Aligner MA6-2	Mask “Membranization” (dark field) Alignment to “M” alignment marks Hard contact mode Time 12s, intensity 11 mW/cm2	
13.3. *AZ5214 development*			
13.3.1. Development	Developer: TMAH UV-lithography	Sequence (1002): DCH 100mm SP 60s	
13.4. *Descum*			

Step Heading	**Equipment**	**Procedure**	**Comments**
13.4.1. Plasma ashing	Plasma Asher 1	20 s, 0.8 mbar, O2 = 300 ml/min, 400 W	
13.5. *Hard baking*			To improve resist durability during wet etching
13.5.1. Hard baking	Developer: TMAH UV-lithography / Stepper	Sequence (2008) PEB 130°C, 90 s	Don't forget to return T setpoint back to 110°C (in case of Developer UV-Lithography). Hotplate near manual spin coater could also be used.
13.6. *Cleaving wafer into chips*			
13.6.1. Cleaving	Cleaving fumehood	Manual cleaving	
13.7. *Membranization*			
13.7.1. Wet etching	SiOetch	7 min	
13.7.2. Rinse	DI water		
13.7.3. Blow dry	N_2		
13.8. *Resist strip*			
13.8.1. Stripping	Acetone	~5 min	
13.8.2. Cleaning	IPA / ethanol	Rinse	
13.8.3. Cleaning	DI water	Rinse	
13.8.4. Blow dry	N_2		
13.8.5. Plasma ashing	Plasma Asher 1	5 min, 0.8 mbar, O2 = 300 ml/min, 400 W	Check in optical microscope for possible resist residues

List of Acronyms

AFM atomic force microscope.

ALD atomic layer deposition.

BARC bottom anti-reflective coating.

BCB benzocyclobutene.

BER bit error rate.

BH buried heterostructure.

BHF buffered hydrofluoric acid.

BPSG borophosphosilicate glass.

CMOS complementary metal-oxide semiconductor.

CW continuous wave.

DBR distributed Bragg reflector.

DEZn diethylzinc.

DFB distributed feedback.

DML directly modulated laser.

DMZn dimethylzinc.

DOS density of states.

DUV deep ultraviolet.

E/O electrical to optical.

ECV electrochemical capacitance-voltage.

FEC forward error correction.

HMDS hexamethyldisilazane.

HSQ hydrogen silsesquioxane.

ICP inductively coupled plasma.

ICT information and communications technology.

IR infrared.

LEAP lambda-scale embedded active region photonic crystal.

LED light emitting diode.

MBE molecular beam epitaxy.

MOVPE metalorganic vapor phase epitaxy.

OSA optical spectrum analyzer.

OTDM optical time-division multiplexing.

PBG photonic bandgap.

PEB post-exposure bake.

PECVD plasma-enhanced chemical vapor deposition.

PhC photonic crystal.

PIC photonic integrated circuit.

PL photoluminescence.

PSG phosphosilicate glass.

PTE partially transmitting element.

QD quantum dot.

QW quantum well.

RIE reactive ion etch.

RT room temperature.

RTA rapid thermal annealing.

SEM scanning electron microscope.

SOI silicon-on-insulator.

SRIM Stopping and Range of Ions in Matter.

TE transverse electric.

TLM transmission line method.

TM transverse magnetic.

TMAH tetramethylammonium hydroxide.

TMAl trimethylaluminum.

TMGa trimethylgallium.

TMIn trimethylindium.

TPA two-photon absorption.

TRIM Transport of Ions in Matter.

UV ultraviolet.

VCL vertical-cavity laser.

VCSEL vertical-cavity surface-emitting laser.

WDM wavelength-division multiplexing.

XRD X-ray diffraction.

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