Two-Mode Controlled Single/Dual-Input DC-AC Inverter with Wide-range DC Input

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Abstract—this paper presents a two-mode controlled step-up inverter (TMCSI), which is capable of handling single or dual inputs with a wide range of dc input voltage. In comparison of traditional multi-stage dc/dc power conversion systems, the power conversion stage is reduced and the voltage/current stress of device is significantly alleviated without using high-voltage dc-bus capacitors. As a result, the reliability and overall conversion efficiency are improved accordingly. By combining the two working modes, the proposed inverter achieves uniform distribution of duty ratio under single/dual-input with a wide range of input voltage, and thereby is very suitable for systems having large input voltage variation. Moreover, based on the dual-input TMCSI a novel power allocation method is also proposed to improve the system load-bearing ability. The power allocation method is controlled separately from two working modes that allows the two-input sources directly supply the ac load simultaneously. In this paper, topology derivation, two-mode control strategy, characteristics of steady principle and design criteria for the key circuit parameters are systematically analyzed, and important conclusions are obtained. Finally, the experimental results from the single/dual-input 500VA 96-192VDC input and 220VAC/50Hz output inverter prototype verify the effectiveness of the proposed TMCSI topology and its associated power regulation approach.

Index Terms—Buck-Boost converter, full bridge inverter, step-up inverter, two-mode control, wide range input voltage

I. INTRODUCTION

Nowadays applying renewable energies to distributed generation, transportation, multi-energy systems etc. has become a key technology for future developments towards a fossil-free society. Dc-ac inverters have significance of power transforming for ac load or grid, and thereby are critical in the application of solar energy, wind and hydrogen.

Many researches have been done to pursue both high conversion efficiency and high ac quality in a hybrid system with multiple and various dc inputs, such as photovoltaics, fuel cells and batteries [1]-[4]. Usually a step-up function is needed in such dc-ac power conversion systems [3], [4]. The traditional low-frequency link inverter proposed in [5], [6] is cascaded by full/half-bridge inverter and a step-up line-frequency transformer. It inherits buck-type inverters’ advantages, e.g. high efficiency, high reliability, simple modulation and control; however, an inverter system employing line-frequency (50/60 Hz) transformers, suffers from high cost, bulky size and loud acoustic noise. Ref. [7] and [8] presented a multi-stage dc-ac power system, including: 1) the conventional two-stage dc-ac power system in [9] and [10], which consists of a boost converter as the front-end dc-dc step-up converter and a full/half-bridge inverter; 2) the multi-stage high-frequency link (HFL) inverter proposed in [11] and [12], which is configured by a dc-dc converter with a high-frequency transformer and a full-bridge inverter, in which bidirectional switches are normally adopted; 3) the differential-mode HFL inverter presented in [13] and [14], which connects the output of two identical HFL dc-dc converters in a differential output. These cascade-connected conversion systems have a relatively high voltage boosting ability, but induce high conduction and switching losses, so that the overall efficiency suffers.

On the other hand, when these inverters are powered by renewable or clean energy sources that have varied output voltage due to the random and intermittent characteristics e.g. photovoltaics, or their inherent electrochemical features e.g. fuel cells, the overall power conversion efficiency suffers because the wide input voltage range causes a narrow or even extreme duty ratio regulating range under a ultra-high or low input voltage. The quasi-Z source inverter, as a single-stage converter, proposed in [15], [16] can handle wide-range input voltage, and has less number of active switches and high quality ac output waveform, but high current and voltage stresses over active switches, bulky passive components and complicated control make it difficult to achieve high efficiency and low cost for matching the demand of the large-scale usage in mass production. A new concept of dual-dc-port asymmetrical multilevel inverter (DP-AMI) is studied in [17]. Due to the asymmetrical multiple voltage levels generated in the inverter, the proposed DP-AMI can achieve reduced number of power stages as well as lower voltage/current stresses over switches. In [18]-[20], the promising multilevel inverters in medium and high power

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**NOMENCLATURE**

- $D_{S10}$: Duty ratio of selective switch $S_{10}$.
- $d_{i}/d_{ST1}$: Duty ratio of full-bridge inverter/ buck-boost converter.
- $u_{gb}$: Output voltage of full bridge.
- $u_{i1}/u_{i2}$: Output voltage of two input units.
- $U_{oi}/U_{io}$: Output voltage/current of the input source $n$.
- $U_{os}$: High-frequency switching voltage $U_{os} = (D_{S10}U_{i1} + D_{S22}U_{i2})$.
- $P_{i1M}$: Maximum output power of PV cells.
- $U_{i1M}$: PV’s output voltage at maximum power point.
- $U_{il_{ref}}$: Reference power for PV cells.
- $I_{il_{ref}}$: Reference current for PV cells.
- $P_{0}$: Output power of the inverter.
- $k$: Output value of the voltage regulator.
- $K_{m}$: Maximum value of $k$.
- $U_{cm}$: Modulation signal of carrier waveform.
- $U_{cm}$: Amplitude of carrier waveform.
- $p_{i1}/p_{i2}$: Output power of the two input sources $U_{i1}/U_{i2}$.
- $I_{1avg}$: Average current of inductor $L_1$.

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**References**

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Applications are proposed, which can handle the series-connected separate dc-voltage source or regulated voltage from the conventional dc-dc converter for ac load supply, and generate high-quality staircase pseudo sinusoidal voltage waveform with low total harmonic distortion. These multilevel inverters allow use of less sizable output filters and offer robust, efficient, and fault-tolerant features.

The major contribution of this paper is to propose a new family of a two-mode controlled step-up inverter (TMCSI) and its associated control strategy. The proposed dc-ac power system has following advantages.

1) Both the number of power conversion stages and the voltage/current stress of devices are reduced without using high-voltage bus capacitors that is beneficial for improving efficiency and reducing converter size/volume.

2) Using the two working modes, the proposed inverter can be effectively used in the application of wide-range input voltage for a uniform distribution of duty ratio under input voltage variation.

3) A TMCSI-based dual-input inverter with a power allocation control is proposed. This dual-input inverter allows two input dc sources to directly supply an ac load simultaneously, and also inherits the advantages of the two-mode control method, which help to achieve the uniform distribution of duty ratio under single- or dual-input operation. Therefore, semiconductors’ current stress is reduced significantly.

This paper is organized as follows. After the introduction, Section II presents the derivation of the proposed TMCSI and its topology family. Section III provides the analysis of two-mode control strategy and operation principle under single- and dual-input. Section IV discusses the proposed inverter’s characteristics and its design considerations. Section V gives experimental results to verify the theoretical analysis and design. Finally, Section VI summarizes the major conclusions of this paper.

II. THE PROPOSED TMCSI AND ITS TOPOLOGY FAMILY

The proposed TMCSI is shown in Fig. 1, which consists of n T-networks and a full-bridge inverter. The more the number of T-network is, the higher voltage gain i.e. the lower input voltage that the inverter can have. The T-network is actually a Buck/Boost dc circuit that composes of inductor \( L_i \), capacitor \( C_1 \) and power switches \( S_{T1}, S_{T2} \). It can realize bidirectional power transforming as well as boost input voltage. It is noteworthy that the shoot through issue of H-bridges can be avoided due to the T-network circuit that results in high system reliability. Therefore, the proposed inverter based on Buck/Boost converter (BBC) can also be called as TMCSI-BBC. Taking \( n=1 \) and positive cycle of output voltage \( u_o \) as an example, there are two working modes.

Mode I: when \( U_i > |u_o| \), \( S_{T1} \) keeps OFF and \( S_{T2} \) is ON. The full-bridge inverter is controlled by sinusoidal pulse width modulation (SPWM), and the output \( u_{ab} \) is a PWM waveform. Its equivalent circuit is plotted in Fig. 2(a). It can be seen that a new power flow path between the low-voltage input \( U_i \) and ac output side is constructed that allows \( U_i \) to supply the load directly due to the low impedance characteristic of the intermediate capacitive link under high frequency.

Mode II: When \( U_i < |u_o| \), the T-network has complementary SPWM switching, \( U_i \) and \( C_1 \) supply the load in series, and at the same time the full-bridge inverter works in a low frequency polar-inversion manner, as shown in Fig. 2(b). Therefore, the regulation of ac output voltage can be realized by combing the two working modes and shifting between these two modes based upon the voltage relationship of \( U_i \) and \( |u_o| \).

Besides the T-network structure, the proposed two-mode control can be extended further to the Z-source inverter and its derivatives. By replacing \( C_1 \) and \( C_2 \) with small film capacitors, the conventional Z-source inverter can be controlled by the same aforementioned two-mode control approach. As a result, the voltage and current stress on both \( L_1, L_2 \) and the power switches is reduced that can decrease component size and cost, as well as improve the overall converter efficiency. When \( U_i > |u_o| \), the full-bridge inverter works with SPWM, as shown in Fig. 3. When \( U_i < |u_o| \), the shoot-through duty ratio of the full-bridge inverter legs can be regulated to boost \( U_i \). By combining these two working modes, the output voltage inversion is achieved. Therefore, this proposed TMCSI based on the simplified Z-network can be called TMCSI-ZN. The topology of quasi-Z source inverter is shown in Fig. 4 (a), the two-mode control can also be used as TMCSI-ZN does. To obtain higher boost ability, the topology can be changed as shown in Fig. 4(b), and this proposed TMCSI based on the simplified quasi-Z-network can then be called as TMCSI-QZ.

Moreover, the proposed topology family can be extended to multiple-input inverters. Therefore, an additional input can be added to the proposed TMCSI-BBC, and forms a dual-input inverter as shown in Fig 5 and the 2nd input is recommended to be connected in series with \( L_1 \). The two inputs of \( U_{i1} \) and \( U_{i2} \) can supply the ac load simultaneously.
More generally speaking, if the power allocation among \( n \) input sources is needed, each input source \( U_i \) should be equipped with a corresponding selective switch \( S_{in} \) and a by-pass diode \( D_{in} \). By regulating the duty ratio \( d_{in} \) of \( S_{in} \) with the line frequency \( f_L \) of 50 Hz, and \( f_L \ll f_c \) (PWM carrier frequency), the converter can realize power allocation between input sources.

Fig. 3. Equivalent circuit of TMCSI-ZN under \( U_i > |u_o| \).

(a) Quasi-Z source inverter

(b) TMCSI-QZ

Fig. 4. Topology of the proposed TMCSI based on quasi-Z network.

Fig. 5. Topology of the proposed dual-input inverter based on TMCSI-BBC.

Fig. 6. Typical waveforms of two-mode control strategy.

III. TWO-MODE CONTROL STRATEGY AND OPERATION PRINCIPLE

The operation principle of two-mode control strategy under single input and dual inputs is the same. Nevertheless, power allocation control is needed for the two input sources in the dual-input case.

A. Two-mode control strategy

Taking the proposed TMCSI-BBC with single input as an example, the typical waveforms of two-mode control strategy are shown in Fig. 6. Due to symmetry of an entire sinusoidal period of \( u_o \), only the positive half cycle is analyzed, where \( S_1 \) remains ON and \( S_2 \) is OFF. When \( |u_o| \) is lower than the switching voltage \( U_{os} = U_i \), \( S_{T1} \) and \( S_{T2} \) always keep OFF and ON, respectively. The full-bridge inverter is controlled by SPWM, and the output \( u_{ab} \) is a PWM waveform.

However, when \( |u_o| \geq U_{os} = U_i \), \( S_1 \) and \( S_2 \) keep ON and OFF, respectively. \( S_{T1} \) and \( S_{T2} \) of Buck/Boost converter work with complementary SPWM driving signals, and \( u_{ab} = U_i + u_c1 \) to realize boosting the input voltage. By combining these two operation modes i.e. full-bridge mode and Buck/Boost mode, depending on \( |u_o| \) and \( U_{os} = U_i \), the inverter can output ac sinusoidal voltage.

B. Operation principles for the dual-input system

For the dual-input operation, based on the proposed two-mode control strategy, power allocation for the two input sources is also needed by adjusting the duty ratio \( d_{in} \) of \( S_{in} \). For example, if \( U_{i1} \) and \( U_{i2} \) employ photovoltaic (PV) cells and fuel cells as the input sources, respectively, a master-slave energy management is adopted to achieve the full use of power generated from PV. Namely, the 1st input \( U_{i1} \) is chosen as the master power supply and need tracking its maximum power point (MPP), and the 2nd input \( U_{i2} \) with adjustable output power supplements the power difference between the first input \( U_{i1} \) and the load in off-grid systems.
Km>1 is the maximum value of $|\frac{d}{dt}v|$. The two operating states, as shown in Fig. 8(a) and (b), respectively. Each operating state consists of two working modes, and their equivalent circuits are shown in Fig. 9 (a).

Buck-Boost mode [Interval $t_1$-$t_2$]; when $u_c$>U_{os}, S_1 keeps on, S_2 is OFF, only the Buck/Boost converter works with complementary SPWM switching. U_{ii} and C_1 in series supply the load, shown as the equivalent circuit C in Fig. 9 (b).

2) State II [see Fig. 9(b)]: If P_{rM} provided by U_{ii} continues to decrease below P_{rM}/(U_{im}+U_{i2})>P_{rM}, k will be regulated from 0 to –K_m. Thus D_{s2}=1-k is clamped to D_{s2}=1, and 1>D_{s1}≥0, which means S_2 keeps ON, the part of P_{r} provided by U_{ii} is regulated by D_{s1}, and makes U_{ii} track MPP, and U_{o2} supplements the power difference between P_{rM} and P_{r}. U_{os} can be expressed as $U_{os}=D_{s1}U_{i1}+U_{o2}$ in State II.

Buck mode [Interval $t_1$-$t_2$]; when $u_c$<U_{os}, the Buck/Boost converter works, $D_{s1}$U_{i1} and C_1 supply the load in series, and its equivalent circuit B is shown in Fig. 9 (a).

In summary, when P_{rM} decreases, k will decrease by the voltage regulator to reduce the output power of U_{ii} and make U_{ii} achieve MPPT, and vise versa. The dual-input system has two operating states, and each state consists of the two working modes, which have been listed in Table I. Combining the two working modes, the proposed inverter achieves voltage inversion under single/dual-input source.

The proposed control method is complex than the conventional multi-stage dc/ac power conversion system. However, it should be noted that at a certain time, only one pair of switches operate in high frequency that is in Buck mode: S_1 and S_2 (zero voltage switching-ZVS), or S_1 (ZVS) and S_2 in the positive and negative half cycles, respectively; in Buck-Boost mode: S_1 and S_2 (ZVS) in high frequency, and S_1-S_2 operate in line frequency. The Buck mode and Buck-Boost mode are controlled independently, which make the system have high reliability and simple control logic. Moreover, the proposed power allocation method for the two inputs is implemented separately from the two-mode control, therefore, in practice, this control under single/dual-input can be easily realized using a digital signal processor.

### Table I. Two Operation States

<table>
<thead>
<tr>
<th>Operating State</th>
<th>k</th>
<th>$D_{s1}=1$</th>
<th>$D_{s2}=1$</th>
<th>Two Working Modes</th>
<th>Typical Waveforms in Fig. 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$K_m&gt;2$</td>
<td>$D_{s1}=0$, $1&gt;D_{s2}&gt;0$</td>
<td>A</td>
<td>(a)</td>
<td></td>
</tr>
<tr>
<td>II</td>
<td>$0&lt;k&lt;K_m$</td>
<td>$1&gt;D_{s1}&gt;0$, $D_{s2}=1$</td>
<td>B</td>
<td>D</td>
<td>(b)</td>
</tr>
</tbody>
</table>

Fig. 8. Typical waveforms of two operating states in a LF period.
IV. CHARACTERISTICS AND DESIGN CONSIDERATION

A. Output characteristics

When the full-bridge inverter operates in steady state, the output voltage of $u_o$ as a function of $U_{i1}$ and $U_{i2}$ can be expressed as

$$u_o = \begin{cases} d_i (U_{i1} + D_{s2} U_{i2}) & D_{s1} \geq d_i \\ D_{s2} U_{i1} + d_i D_{s2} U_{i2} & D_{s1} < d_i \end{cases}$$

where $d_i$ is the duty ratio of the full-bridge inverter. When the Buck-Boost converter operates, the output voltage is calculated by

$$u_o = \begin{cases} D_{s1} U_{i1} + d_{ST1} U_{i1} + D_{s1} U_{i2} & D_{s1} \geq d_{ST1} \\ D_{s1} U_{i1} + D_{s2} U_{i1} + D_{s1} U_{i2} & D_{s1} < d_{ST1} \end{cases}$$

where $d_{ST1}$ is the duty ratio of the Buck-Boost converter.

Then switching voltage $U_{os}$ between the two working modes can be derived from (1) or (2), where $d_i=1$ or $d_{ST1}=0$.

$$U_{os} = D_{s1} U_{i1} + D_{s2} U_{i2}$$

The corresponding output characteristic curves, which are obtained from (1) and (2), can be plotted in Fig. 10. It shows that $U_{os}$ increases with increasing $D_{s1}$, and the working time of full-bridge inverter becomes longer, and conversely the Buck-Boost’s operation time is shorter. When $U_{i2} > \sqrt{2} U_o$ (output voltage RMS value), the Buck-Boost converter stops working. When $U_i<|u_o|$, the voltage gain of the proposed TMCSI-BBC, the two mode controlled Z-source/Quasi-Z source inverter and TMCSI-QZ can be expressed in (4)-(6), respectively.

$$U_o_{TMCSI-BBC} = U_i (1-d_{ST1})$$

$$U_o_{ZQS} = U_i (1-d_{ST1})(1-2d_{ST1})$$

$$U_o_{TMCSI-QZ} = U_i (1-2d_{ST1})$$

B. Design consideration

When the Buck/Boost converter works, the devices $L_i$ and $C_i$ act as an additional filters, so a smaller $C_i/L_i$ can be chosen with a larger high-frequency voltage/current ripple. Ignoring the current of $C_i$, in steady state, the average current of $L_i$ in one high frequency period can be expressed as

$$I_{Link} = \frac{u_o}{R_L (1-d_{ST1})}$$

where $R_L$ is the load resistance.
The impedance of power allocation for the two input sources, and allow $Z_1=0$, in Fig. 11. It can be seen that when $C_1$ is the minimum input voltage.

In the same way, $L_1$ can be derived in (9) based on the $40\%$ of the maximum average output current. When $u_0=U_i/2$, $L_1$ gets the minimum value.

$$L_1 = \frac{u_1 (U_i - u_0) R_{L_{\text{min}}} T_s}{40\% \sqrt{2} U_i} \quad (9)$$

When the full-bridge inverter works, $L_1$ is connected with $C_1$ in parallel, and the corresponding equivalent impedance is $Z_L = \frac{1}{sL_1} + \frac{1}{sC_1}$, where $s$ is the Laplace complex frequency. The impedance of LC-type output filter is $Z_L = \frac{1}{sL_1} + \frac{1}{sC_1}$. Assuming that $U_{d0}/U_i = Z_L (Z_L + Z_0)$, and the relationship between $U_{d0}/U_i$, $C_1$ and frequency $f$ is plotted in Fig. 11. It can be seen that when $C_1=0$, $U_{d0}/U_i$ is up to 0.5 in the intermediate and higher frequency range. With the increase of $C_1$, the band-stop frequency bands around the switching frequency get narrower. To obtain fast dynamic response and also reduce the reactive current, size/volume of the conversion system, $C_1=2.67\mu F$ is selected for the experimental prototype.

C. Power relationship between the two inputs and output

When the full-bridge inverter works, the load power $P_o$ supplied by each inputs can be derived as

$$P_o = \frac{D_{s1} U_{i1}}{D_{s21} U_{i1} + D_{s22} U_{i2}} P_{i1} \quad (10)$$

When the Buck-Boost converter works, the average input current $i_{12}$ of $U_{i2}$ under can be expressed as

$$i_{12} = D_{s22} I_1^{\text{avg}} \quad (11)$$

The instantaneous output power $P_{i1}$ provided by $U_{i1}$ can be derived from (2), (7), and (11), and expressed as

$$P_{i1} = D_{s21} U_{i2} I_{12}^{\text{avg}} = D_{s21} U_{i2} \frac{U_0}{R_L (1 - d_{ST1})} \quad (12)$$

In (12), $P_{i1}$ is the function of $D_{s21}$ and $d_{ST1}$. In operating State I, $P_{i1}$ increases with increasing $D_{s21}$. In State II, $D_{s21}=1$, as $D_{s1}$ decreasing, $d_{ST1}$ will increase and $P_{i1}$ increase. Therefore, by adjusting $D_{s1}$, the control strategy can realize power allocation for the two input sources, and allow $U_{i1}$ to track the MPP, and $P_o$ supplied by $U_{i1}$ can be expressed as $P_{i1} = P_o - P_{i2}$.

V. EXPERIMENTAL RESULTS

The proposed dual-input inverter based on TMCSI–BBC with master-slave power distribution has been constructed in laboratory and the corresponding experimental test is carried out. The 1st input source $U_{i1}$ uses a programmable solar simulator TC.P.16.800.400.S to simulate PV cells and the 2nd input $U_{i2}$ uses a power supply of 62012P-600-8 to supplement the load. The converter specifications as well as adopted components are listed in Table II. The prototype is shown in Fig. 12.

![Prototype of the proposed dual input inverter.](image)

**Fig. 12. Prototype of the proposed dual input inverter.**

The maximum voltage stress over semiconductor devices of the proposed single-input TMCISI is $\sqrt{2} U_d$. However, the voltage stress of the dual-input inverter based on TMCISI–BBC is $(1 - D_{s21}) U_D + \sqrt{2} U_d$, in BuckBoost mode under operating State II, where the full-bridge inverter have no switching spike voltage. To lower the voltage stress, $D_{s21}$ is limited at $1 \geq D_{s21} \geq 0.2$, which means the MPPT for $U_{i1}$ stops working under some extremely low power conditions like partial shading or cold rainy weather, and IXFQ34N50P3 with rated voltage of 500V is chose for the proposed inverter. A RC snubber, placed in front of the full-bridge inverter and connected in parallel, can also be used.

![Voltage stress comparison.](image)
The steady-state experimental waveforms of the off-grid dual-input system with the rated resistive load are shown in Fig. 13. The experimental results show that: (1) $S_4$ remains ON in the positive half-cycle of $u_o$. When $|u_o| < U_{os}$, $S_1$ keeps OFF and $S_2$ is ON, the full-bridge inverter works in high frequency and $u_{ab}$ is a PWM wave. When $|u_o| > U_{os}$, $S_1$ keeps ON, $S_1$ and $S_2$ work in high frequency alternatively, and $u_{ab} = D_{Ss1} U_{i1} + u_{c1}$. (2) When the full-bridge inverter works, the SPWM voltage is $U_{os} = D_{Ss2} U_{i1} + D_{Ss1} U_{i2}$ as shown in Fig. 13 (a), when the Buck-Boost converter works, the maximum drain-source voltage of $S_{T1}$ in State II is $u_{dsT1} = D_{Ss1} U_{i1} + u_{c1}$, as shown in Fig. 13 (b). (4) By combining the two working modes, high quality 220V/50Hz AC waveforms are obtained at output in each operating state by filtering $u_{ab}$ with $L_f, C_f$. (5) The working time of the full-bridge inverter increases with increasing $U_{os}$, and the operating time of the Buck-Boost converter decreases, as shown in Fig. 13 (b)-(d). The experimental waveforms are in accordance with the theoretical analysis.

The experimental waveforms under single input $U_{i1} = 148$VDC with the rated reactive load are shown in Fig. 14. The experimental results show that the proposed inverter can achieve bidirectional power flow under single-input source, and has high-quality waveform of $u_o$.

The transient experimental waveforms with load abruptly changing from the rated resistive load to no load under single-input $U_{i1} = 96$VDC are shown in Fig. 15. The experimental results show that: When the load abruptly changes, the system has fast dynamic response, and the response time is about 0.6ms.

The dynamic experimental waveforms with single-input $U_{i1}$ slowly changing between 96V to 192V under rated resistive load are shown in Fig. 16. The results show that when $U_{i1}$ changes with a 10V/ms maximum speed (restrained by the Chroma 62100H-600 Programmable DC source), the output $u_o$ is unaffected, and the inverter achieves uniform distribution of duty ratio under the input voltage variation.

The transition experimental waveforms of the proposed off-grid system under the 1st input MPP (192W, 96V) and the 2nd input $U_{i2} = 96$V with the resistive load abruptly changing...
(a) Load abruptly changes from the light load to the rated one.

(b) Load abruptly changes from the rated load to the light one.

Fig. 17. Transition experimental waveforms of the proposed off-grid dual-input system with resistive load abruptly changing.

(a) From 1000W/m² to 400W/m²

(b) From 400W/m² to 1000W/m²

Fig. 18. Transition experimental waveforms among different operating states of the proposed off-grid system with abrupt light intensity change.

are shown in Fig. 17. In Fig. 17(a), firstly, the maximum output power of $U_{i1}$ is $P_{i1M}>P_o$, $U_{i1}$ supplies the light load alone. Once load increases to the rated, the 1st input source tracks to its MPP (96V, 2A, 192W), and $U_{i2}$ supplements the load. The system can smoothly changes from State Ⅰ to State Ⅱ. Fig. 17(b) shows that the smooth transition can also be realized as load changing from the rated one to the light one.

The transition experimental waveforms under the rated resistive load, the 1st input MPP (576W, 96V) and the 2nd $U_{i2}$=96V with abrupt light intensity change are shown in Fig. 18. In Fig. 18(a), at first, $P_{i1M}>P_o=0.5kW$, and $U_{i1}$ supplies the load alone. With the light intensity decreases, once the power supplied by $U_{i1}$ is insufficient, $U_{i2}$ starts supplying the load to help $U_{i1}$ track its MPP, and the system can smoothly transits from State I to State II. Fig. 18(b) shows that the transition can also be smooth as the light intensity increases from 400W/m² to 1000W/m².

The conversion efficiency and output voltage THD curves of the inverter prototype with different resistive load are measured and plotted in Fig. 19. In Fig. 19 (a), the efficiency curves under different single-input voltage $U_{i}=96V$, 148V and 192V and dual-input supply $U_{i1}$ (192W, 96V)/$U_{i2}$ (96V) are presented, respectively.

It can be seen that: (1) The conversion efficiency all increase first and then decrease with the load power increases, for the hard-switching loss of power switches at light load, and increasing conduction loss of devices under heavy load. (2) With the input voltage increasing, the conversion efficiency increases, since the power loss of device caused by boosting input voltage of the Buck-Boost converter decreases. (3) The conversion efficiency under three different single-input voltage 96V, 144V, 192V with the rated load is 92.5%, 93%, 95.5% respectively, and the maximum efficiency is 94.5%, 95.7%, 97%, respectively. 4) The maximum and full-load conversion efficiencies under dual inputs are 95.2% and 93.3%, respectively. Fig. 19(b) shows the output voltage THD curves under the dual-input source $U_{i1}$ (192W, 96V)/$U_{i2}$ (96V), it shows that: (1) The output THD under the 1st input decreases with the load increasing, and THD under the dual inputs decreases first, and then increases, which is mainly because the effect of output filter is weakened in State II. (2) The minimum and full-load THD of $u_o$ under dual-input supply is 1.48% and 1.9% respectively, while under the 1st input is all 1.69%.

Combining the two working modes, the proposed inverter achieves uniform distribution of duty ratio under single/dual input with wide range varied input voltage. For $S_{T1}$, $S_{T2}$ and $S_1$–$S_4$, only a pair of switches operate in high frequency at a

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Equivalent input voltage</th>
<th>Maximum efficiency (%)</th>
<th>Type</th>
<th>Power allocation for the inputs?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed dual-input step-up inverter</td>
<td>$U_{i}=192V$</td>
<td>~97%</td>
<td>Buck-Boost</td>
<td>Yes</td>
</tr>
<tr>
<td>CIPS in [17]</td>
<td>$U_{i}=100V$</td>
<td>~96%</td>
<td>Buck-Boost</td>
<td>No</td>
</tr>
<tr>
<td>DPR-AMI proposed in [17]</td>
<td>$U_{i}=190V$</td>
<td>~97%</td>
<td>Buck</td>
<td>No</td>
</tr>
</tbody>
</table>
achieved efficiency is 97% and the output voltage THD is consistent with the theoretical analysis. The maximum comprehensive performance, and the experimental results are two operating states, and each state consists of two working issues anymore. The proposed dual-input set-up inverter has DP-AMI is just a buck-type inverter when powered by two input sources, and can also not realize power allocation between the two inputs. Its maximum efficiency is almost the same as the proposed under the same input voltage, but conversion efficiency under light load is relatively lower compared to the inverter in this paper due to the inherent power loss caused by the front-end boost converter.

VI. CONCLUSION

A novel two-mode controlled step-up inverter with high efficiency was proposed and verified in this paper. Based on low impedance of the intermediate capacitive link under high frequency, a new power flow path between the low-voltage input source and the ac output side is constructed. When the instantaneous input voltage is lower than input voltage of the intermediate capacitive link boosts the input voltage, and supply the ac load with directly. This solution was realized by proposing a family of TMCSI. With the proposed TMCSI, the input power is processed without the front-end dc/dc set-up converter, and the conversion stage is reduced, which is beneficial for the reducing current/voltage stress, switching losses and size/volume of the conversion system.

The dual-input inverter based on TMCSI–BBC with a novel power allocation method is also studied to improve load capability. This power allocation method is controlled separately from the two-mode control strategy by adjusting Dso, with line frequency, which can help to improve the dual-input system’s reliability, since there is no overshoot issue anymore. The proposed dual-input set-up inverter has two operating states, and each state consists of two working modes. The designed and developed 500VA 96-192VDC input and 220V50Hz AC inverter prototype has excellent comprehensive performance, and the experimental results are consistent with the theoretical analysis. The maximum achieved efficiency is 97% and the output voltage THD is lower than 2% over the entire power range.

REFERENCES


