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Alternative Source-Port-Tolerant Series-Connected Double-Input DC–DC Converter

Xiaofeng Sun, *Member, IEEE*, Yue Zhou, Wei Wang, Baocheng Wang, and Zhe Zhang, *Member, IEEE*

Abstract—The two input sources of a series-connected double-input dc/dc converter (SCDIC) can power the load simultaneously or individually. But the two sources must supply the load simultaneously when the output voltage is greater than either of the two input voltages. This is a big issue, especially in double-input alternative power systems in which two input ports are, respectively, interfaced with a renewable energy source and a storage element due to the randomness and intermittency of renewable energy sources. This paper proposes a topology scheme using a combination of a charging switch and an SCDIC. In the case of one port powering or one input being short-circuit, the proposed topology forms a bootstrap circuit with the help of the charging switch and SCDIC switches to charge the powered off port and maintain the expected output voltage, which enhances the reliability of double-input conversion, making it robust against one input powering off and fault tolerance against one input short-circuit. The operation principle and the corresponding power management strategy are presented in detail. In addition, charge–discharge feature of the bootstrap mode is analyzed and the charging loss is calculated. Experimental results validate the feasibility of the proposed scheme.

Index Terms—Bootstrap circuit, charging loss, fault tolerance, mode transition, multi-input converter, power management, robust design.

I. INTRODUCTION

IN RENEWABLE power systems, a multiple-input converter (MIC) has the following advantages over conventional solutions that employ multiple single converters: 1) MIC has a simpler structure, higher power density, and a lower cost characteristic because of multiplexing or sharing active switches and reactive components [1]–[3], and 2) MIC can improve the dynamic performance and avoid the complex communication among multiple different sources due to the unified power management with centralized control [4]–[7]. Therefore, MIC is an excellent candidate for small scale renewable power systems which is economic and therefore has good development prospects [8]–[13].

An isolated MIC topology can be constructed by utilizing the magnetic coupling through a multi-winding transformer [14]–

[16]. These MICs are good candidates for the applications where galvanic isolation is required. However, the major problem is that too many active switches are used. In contrast to isolated MIC designs, nonisolated MIC features compact packaging, high power density, and high system efficiency. Due to their remarkable merits, many nonisolated MICs have been proposed for various applications [17]–[22].

Mostly, the nonisolated MICs are proposed based on the structure of the buck or boost dc–dc converters. A three-input boost dc–dc converter is proposed in [17], which can combine a photovoltaic source, a fuel cell (FC) source, and a battery in a unified structure. In [18], a buck voltage source cell parallel-connected MIC is presented based upon a time-multiplexing scheme, and this converter can operate in different modes, such as buck, boost, or buck–boost mode; however, only one input source is allowed to deliver energy at a time.

The two-input series-connected buck dc–dc converter proposed in [19]–[21] has a simple circuit structure, exhibits high renewable energy utilization, and is also capable of delivering power from two power sources to a dc load simultaneously or individually. In [20], a series-connected two-input converter was introduced for nanogrid application, where one port is connected to a renewable energy source and the other is interfaced with a storage element. For these schemes, when one input source is powered off, the other port stands the operation and the output voltage will be less than the existing input voltage, which means that the converter is not able to maintain the expected output voltage in the single input case if the output voltage is greater than either of two input voltages. Due to the randomness and intermittency such as photovoltaic cell and wind energy, the converter in nanogrid should have a flexible compensation program and be able to work when the renewable source is powered off, which could not be realized by series-connected double-input dc/dc converter (SCDIC). This paper proposes a topology scheme using a combination of a charging switch and an SCDIC. In the case one port powering on, the proposed topology forms a bootstrap circuit with the assistance of the charging switch and SCDIC switches to charge the powered off port and maintain the expected the output voltage. In other words, when the renewable source is not available, the alternative power port will be charged by the available storage unit such as FC port to keep the converter's output stable, and hereby the proposed scheme enhances the reliability of renewable energy conversion systems, making it robust against renewable source port powering off or failures in one of the inputs.

In comparison with the method of the two parallel boost converters, the proposed converter employs only a single inductor. It can add more input sources if necessary by sharing the output

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inductor. Although the parallel boost converter is easily modular, each unit has to incorporate an inductor, thus increasing volume and cost and slowing down system dynamic response as well. The proposed topology is also concerned about fault tolerance when one input is short-circuited. With a blocking diode or breaker, the short-circuit input port can be separated from the converter and the port can be charged by the bootstrap circuit, which facilitates the proposed converter working in double-input mode. The operation principle is the same as the case of one port powered off. In addition, the proposed series-connected double-input structure decreases the voltage stress on power switches.

The circuit operation principles, the input–output voltage relationship and the corresponding power management strategy of the proposed converter are presented in detail in this paper. In addition, the charge–discharge features of the bootstrap mode are analyzed and the charging loss is calculated. A 200 W prototype has been built to verify the effectiveness of the proposed topology both under double-input condition and the case of single FC port being powered on.

This paper is organized as follows. After Section I, the robustness of the proposed converter is explained in Section II. In Section III, operation principles and power management are given. Section IV describes the charge–discharge features of the bootstrap mode. Experimental results are presented in Section V, and finally, Section VI concludes this paper.

II. ROBUSTNESS DESIGN OF THE DOUBLE-INPUT DC–DC CONVERTER

The double-input dc–dc converter with the bootstrap circuit is shown in Fig. 1, where V_{in1} and V_{in2} are the two input sources. The bootstrap capacitor C_1 is connected in parallel with the switch pair of S_{11} , S_{12} and interfaces the first input source, the switch pair of S_{21} , S_{22} interfaces the second input source, and the switches S_{11} , S_{12} , S_{21} , and S_{22} are connected in series. The switches S_{11}/S_{12} , S_{21}/S_{22} are operated in a complementary manner. S_{C1} and S_{C2} are the charging switches. L_f , C_f , and R_L represent the filter inductor, capacitor, and load resistance, respectively. The converter has one input port connected to the renewable source V_{in1} , such as solar panels, wind turbines, or FCs, D_{in1} is the blocking diode. When input source is short-circuited, the input port is separated from the converter. The other input port is connected to a backup source V_{in2} , such as a mains supply, battery, or FC. In Fig. 1(a), S_{11} , S_{22} , and S_{C1} are diodes and the power flow of power source 2 is of single direction; and in Fig. 1(b), S_{11} , S_{22} , and S_{C1} are MOSFETs and the power flow of power source 2 can be reversible; hence, the load or renewable port 1 can feed energy back to the backup port, i.e., V_{in2} .

In order to simplify the analysis, the assumptions are made: all switching devices are ideal; the capacitors and inductors are big enough. There are two operating states under the condition where only one input source is available and the corresponding equivalent circuits in each state are illustrated in Fig. 2(a) and (b), as the case that the output voltage is greater than either of two input voltages is considered, the duty ratio of S_{21} , which

Fig. 1. Topology of the double-input converter with bootstrap circuit. (a) A single power flow for port 2. (b) A bidirectional power flow for port 2.

belongs to the input powering unit, should be maximum, so S_{21} should be kept on in this mode. Fig. 2(c) shows the key waveforms of converter in one switching cycle, where v_{GS12} and v_{GS21} are the pulsewidth-modulated (PWM) signals, with the duty cycle of D_1 and D_2 , for S_{12} and S_{21} . The driving signal of S_C is the same with S_{11} .

State I [see Fig. 2(a)]: S_{11} , S_{21} , and S_C are on, and S_{12} and S_{22} are off. V_{in2} charges C_1 through S_{11} , S_{21} , and S_C . u_{AB} , representing the voltage across A and B, equals to V_{in2} . A negative voltage is imposed on the inductor L_f and hereby i_{L_f} decreases, indicated as S.I in Fig. 2(c) and the input source V_{in2} delivers power to the load solely

$$\frac{di_{L_f}}{dt} = \frac{V_{in2} - V_o}{L_f}. \quad (1)$$

State II [see Fig. 2(b)]: S_{12} , S_{21} are ON, and S_{11} , S_{22} , and S_C are OFF. The input source V_{in2} connects with C_1 in series; hereby, $u_{AB} = 2V_{in2}$. A positive voltage that equals $u_{AB} - V_o$ is applied across the inductor L_f , making i_{L_f} increased, indicated as S.II in Fig. 2(c)

$$\frac{di_{L_f}}{dt} = \frac{2V_{in2} - V_o}{L_f}. \quad (2)$$

As mentioned earlier, it shows that when V_{in1} is out of work, the port can be charged by V_{in2} through bootstrap circuit and converter switches, so the proposed scheme is robust against input source powering off.

Fig. 2. Equivalent circuits and key steady-state waveforms when V_{in1} is powered off. (a) State I. (b) State II. (c) Key waveforms with $1 > D_1 > 0$ and $D_2 = 1$.

Therefore, when only V_{in2} is connected, in the steady state, applying the volt-second balance principle to the inductor L_f

$$(V_{in2} - V_o)(1 - D_1) + (2V_{in2} - V_o)D_1 = 0. \quad (3)$$

Accordingly, the steady-state input to output voltage transfer function as a function of D_1 can be derived as

$$V_o = V_{in2}(1 + D_1). \quad (4)$$

III. CONTROL STRATEGY OF THE CONVERTER

A. Operational Principle Under the Condition of Both the Two Input Sources are Available

The following analysis is under the condition of both the two input sources are available, as shown in Fig. 3(a)–(d): the two sources are able to deliver power to a dc load simultaneously, the converter working under a regular double-input converter mode and S_C is off.

State III [see Fig. 3(a)]: S_{12} and S_{21} are in ON state, and in contrast, S_{11} , S_{22} , and S_C are in OFF state. The two input sources are connected in series to deliver power to the load. u_{AB} , equals the sum of V_{in1} and V_{in2} . So that $u_{L_f} = u_{AB} - V_o$, which is positive, and i_{L_f} increases linearly, indicated as S.III in Fig. 3(e)–(f)

$$\frac{di_{L_f}}{dt} = \frac{V_{in1} + V_{in2} - V_o}{L_f}. \quad (5)$$

State IV [see Fig. 3(b)]: S_{12} and S_{22} are on, and S_{11} , S_{21} , and S_C are off. Only the input source V_{in1} transfers power to the load; therefore, $u_{AB} = V_{in1}$. A positive voltage is applied across the inductor and i_{L_f} increases, indicated as S.IV in Fig. 3(e)

$$\frac{di_{L_f}}{dt} = \frac{V_{in1} - V_o}{L_f}. \quad (6)$$

State V [see Fig. 3(c)]: S_{11} and S_{21} are ON, and S_{12} , S_{22} , and S_C are OFF. Accordingly, only the input source V_{in2} supplies energy to the load. Then, u_{AB} equals V_{in2} . A negative voltage is imposed across the inductor and i_{L_f} decreases, shown as S.V in Fig. 3(f)

$$\frac{di_{L_f}}{dt} = \frac{V_{in2} - V_o}{L_f}. \quad (7)$$

Fig. 3. Equivalent circuits and key steady-state waveforms when V_{in1} is powered on. (a) State III. (b) State IV. (c) State V. (d) State VI. (e) Key waveforms with $1 > D_1 > D_2 > 0$. (f) Key waveforms with $1 > D_2 > D_1 > 0$.

State VI [see Fig. 3(d)]: S_{11} and S_{22} are ON, and S_{12} , S_{21} , and S_C are OFF, i_{L_f} freewheels through S_{11} and S_{22} and decreases; as a result, $u_{AB} = 0$, as shown in S.VI in Fig. 3(e) and (f)

$$\frac{di_{L_f}}{dt} = \frac{-V_o}{L_f}. \quad (8)$$

Fig. 3(e) and (f) shows the key waveforms of converter in one switching cycle under the condition of the two input sources working well. Assume that S_{12} and S_{21} are turned on

Fig. 4. Schematic diagram of control strategy in Mode I.

Fig. 5. Schematic diagram of control strategy in Mode II.

simultaneously and D_1, D_2 represent their duty cycles. Fig. 3(e) shows the waveforms for the three states—III, IV, and VI, with $1 > D_1 > D_2 > 0$, and Fig. 3(f) shows the three states—III, V, and VI in one switching cycle, with $1 > D_2 > D_1 > 0$.

In the steady state, applying the volt-second balance principle to the inductor L_f

$$V_o = D_1 V_{in1} + D_2 V_{in2}. \quad (9)$$

With small-signal approximation, the input currents at steady state are expressed as

$$I_{in1} = D_1 I_o \quad (10)$$

$$I_{in2} = D_2 I_o. \quad (11)$$

B. Power Management for the Proposed Converter

The power management of MIC includes the output voltage regulation and the input power distribution between the input sources. The load should be supplied by the renewable source as much as possible and the rest is provided by the backup power. All the analysis followed are based on Fig. 1(a), where only a single power flow is considered for port 2. The renewable energy source such as solar panel connects to port 1, which is served as the main power source, and the backup power source, such as FC connects to port 2. Assuming that the available power of input source 1 is P_{in1} and the demanded load power is P_o , there are three operating modes, described as follows.

Operation Mode I: When $P_o > P_{in1}$, or $P_o \leq P_{in1}$ but $V_o > V_{in1}$, the two input sources deliver power to the load simultaneously. The input source 1 provides maximum power P_{in1} , while the input source 2 offers the rest of the demanded load power. The block diagram of the power management in the first mode is shown in Fig. 4. When the enable signal of the multiplexer EN is Mode I, $Ao = AX$, $Bo = BX$, $Co = CX$, $Do = DX$. So the switch S_{12} in the first port is controlled to regulate the input current of source 1 with a current PI regulator, the switch S_{21} in the second port is controlled to regulate the output voltage with a voltage PI regulator, and the switch S_C is shut down completely.

Operation Mode II: When $P_o \leq P_{in1}$ and $V_o < V_{in1}$, the load power is provided by the input source 1, and the input source 2 is

Fig. 6. Schematic diagram of control strategy in Mode III.

powered off. Therefore, the block diagram of the power management in Mode II is shown in Fig. 5. When the enable signal of the multiplexer EN is Mode II, $Ao = AY$, $Bo = BY$, $Co = CY$, and $Do = DY$. A voltage and current double closed-loop control method is employed, i.e., an outer voltage loop and an inner current loop. In this case, the switch S_{12} is assigned to regulate the output voltage and the switches S_{21} and S_C are shut down completely.

Operation Mode III (Bootstrap Mode): When $P_{in1} = 0$, the input source 1 is shut down and the load power is provided by the input source 2 and the bootstrap capacitor. The block diagram of power management in Mode III is shown in Fig. 6. When the enable signal of the multiplexer EN is Mode III, $Ao = AZ$, $Bo = BZ$, $Co = CZ$, and $Do = DZ$. Hence, only a voltage compensator is used to regulate the output voltage, and the current regulator is bypassed, consequently. Furthermore, since S_{21} is always on, D_1 is assigned to regulate the output voltage. When S_{11} and S_{21} are turned on, the input source 2 charges the capacitor C_1 through S_C . As a result, the input source 2 and the bootstrap capacitor are connected in series to deliver power to the load.

IV. CHARGE-DISCHARGE ANALYSIS IN BOOTSTRAP MODE

A. Bootstrap Capacitor Charge-Discharge Analysis

When the proposed converter works in bootstrap mode, the main operation states are: 1) V_{in2} provides energy to the load

Fig. 7. Charge-discharge equivalent model. (a) Charging model. (b) Discharging model.

port and charges C_1 ; 2) C_1 and V_{in2} are connected in series as input source. Charge-discharge equivalent model of the bootstrap capacitor are shown in Fig. 7. For simplicity, the following assumptions are made: 1) all power switches are MOSFETs and R_{DS} represents the drain-source on-state resistance; 2) R_{ESR} is the equivalent series resistance (ESR) of the bootstrap capacitor; 3) the equivalent resistance of the inductor and the power switches' on-off transition can be negligible; and 4) the parasitic inductance in the charging circuit has a so great impact on the system performance that we cannot ignore it.

Considering the parasitic inductance, the charging model is derived in Fig. 7(a). It can be seen that the charging circuit is a three-order circuit. Based upon Fig. 7(a), we obtain

$$\begin{cases} i_{in2} = i_{C1} + i_o \\ V_{in2} - 2R_{DS}i_{in2} = L_f \frac{di_o}{dt} + V_o \\ = (2R_{DS} + R_{ESR})i_{C1} + L_p \frac{di_{C1}}{dt} + u_{C1} \end{cases} \quad (12)$$

where L_p is the parasitic inductance in the charging circuit.

Equation (12) can be rewritten as

$$\begin{aligned} & \frac{L_f L_p C_1}{2R_{DS}} \frac{d^3 u_{C1}}{dt^3} + \left(L_f C_1 \frac{(2R_{DS} + R_{ESR})}{2R_{DS}} + L_f C_1 + L_p C_1 \right) \\ & \times \frac{d^2 u_{C1}}{dt^2} + \left(\frac{L_f}{2R_{DS}} + C_1 (2R_{DS} + R_{ESR}) \right) \frac{du_{C1}}{dt} \\ & + u_{C1} - V_o = 0. \end{aligned} \quad (13)$$

Equation (14) gives the initial conditions in the charging process

$$\begin{cases} u_{C1}(0_+) = V_{10} \\ \frac{du_{C1}}{dt}(0_+) = -\frac{I_o}{C_1} \\ \frac{d^2 u_{C1}}{dt^2}(0_+) = \frac{V_{in2} - 2R_{DS}i_{in2}(0_+) - u_{C1}(0_+)}{L_p C_1} \\ - \frac{C_1(2R_{DS} + R_{ESR})(du_{C1}/dt)(0_+)}{L_p C_1} \\ = \frac{V_{in2} + I_o R_{ESR} - V_{10}}{L_p C_1} \end{cases} \quad (14)$$

where V_{10} is initial capacitor voltage before charging.

The discharging circuit is a two-order circuit. According to Fig. 7(b), we have

$$\begin{cases} L_f C_1 \frac{d^2 u_{C1}}{dt^2} + C_1(2R_{DS} + R_{ESR}) \frac{du_{C1}}{dt} + u_{C1} = V_o - V_{in2} \\ u_{C1}(0_+) = V_{20}, \quad \frac{du_{C1}}{dt}(0_+) = -\frac{I_o}{C_1} \end{cases} \quad (15)$$

where V_{20} is initial capacitor voltage before discharging.

B. Bootstrap Capacitor Voltage Analysis

During the discharging time, C_1 and L_f are connected in series. Assuming that the inductor is large enough, the capacitor current i_{C1} can be considered as constant

$$C_1 \frac{du_{C1}}{dt} = I_o. \quad (16)$$

The voltage variation across C_1 can be expressed as

$$\Delta U_{C1} = \frac{I_o D_1}{C_1 f_s} = \frac{V_o D_1}{R_L C_1 f_s}. \quad (17)$$

The capacitor voltage ripple coefficient γ can be derived by

$$\gamma = \frac{\Delta U_{C1}}{V_{in2}} \times 100\% = \frac{V_o D_1}{V_{in2} R_L C_1 f_s}. \quad (18)$$

According to (4), (18) can be rewritten as

$$\gamma = \frac{(1 + D_1)D_1}{R_L C_1 f_s}. \quad (19)$$

The curve of the ripple coefficient γ versus capacitance C_1 and frequency f_s at a certain duty cycle and load is shown in Fig. 8. It is drawn under the condition of $D_1 = 0.45$ and $R_L = 8\Omega$. It can be seen that the ripple coefficient γ is decreased with the increase of C_1 and f_s . Therefore, a larger C_1 is chosen to obtain a small ripple coefficient as well as to improve the system steady characteristic.

C. Charging Current Analysis

The input source 2 and the capacitor are connected in parallel in the bootstrap mode. If the input source 2 and the capacitor voltage are not equal, the charging current will reach to the maximum value sharply. In fact, there is a parasitic inductance

Fig. 8. Curves of the ripple coefficient γ versus C_1 and f_s .

Fig. 9. Charging current with $C_1 = 16.5$ mF.

existing in the charging circuit, which imposes a certain impact on the charging current.

All the power switches are implemented with IRFP250M and the on resistance $R_{DS} = 0.075 \Omega$. With the help of simulation in Maxwell/Q3D, the parasitic inductance is about 300 nH.

When capacitance C_1 is chosen as 16.5 mF, the ESR $R_{ESR} = 0.016 \Omega$ by the parameter from handbooks. Take these parameters into (13) and (14), and the theoretical charging current can be derived, as shown in Fig. 9, which is marked with blue dotted line. And the simulation result under the same condition in PSIM is also plotted in Fig. 9 with the red solid line. It can be seen that the simulation result is in accordance with the theoretical value to some extent.

Similarly, when capacitance $C_1 = 220 \mu\text{F}$, the ESR $R_{ESR} = 1.2 \Omega$ by the parameter from handbooks. The theoretical value and simulation result are depicted in Fig. 10.

As mentioned earlier, the simulation results are in good agreement with the theoretical analysis, thus verifying the effectiveness of the charging model. It also can be seen that the trend of the charging current is determined by the charging time constant. With a large capacitor, the charging current will continue to rise in a switching cycle. On the contrary, it will rise at first and then fall due to a smaller one.

Fig. 10. Charging current with $C_1 = 220 \mu\text{F}$.

Fig. 11. Equivalent circuit of the charging process.

D. Charging Loss Analysis

The equivalent circuit of the charging process is shown in Fig. 11, where U is the steady-state voltage across the capacitor, and ΔU_{C_1} is the dynamic variation. The output power P_{out} can be divided into two parts: the first part is stored in capacitor, named as P_{in} and the other part is consumed by R_{eq} , as P_{loss} .

The input power P_{in} is expressed as

$$\begin{aligned} P_{in} &= f_s \left[\frac{1}{2} C U^2 - \frac{1}{2} C (U - \Delta U_{C_1})^2 \right] \\ &= \frac{1}{2} f_s C \Delta U_{C_1} (2U - \Delta U_{C_1}). \end{aligned} \quad (20)$$

The output power P_{out} is expressed as

$$P_{out} = f_s \int_0^{(1-D_1)T_s} U i_{C_1}(t) dt = f_s C U \Delta U_{C_1}. \quad (21)$$

According to (20) and (21), the charging loss can be obtained

$$P_{loss} = P_{out} - P_{in} = \frac{1}{2} f_s C \Delta U^2. \quad (22)$$

The charging efficiency η_{charge} can be derived as

$$\begin{aligned} \eta_{charge} &= \frac{P_{in}}{P_{out}} = \frac{(1/2) f_s C \Delta U_{C_1} (2U - \Delta U_{C_1})}{f_s C U \Delta U_{C_1}} \\ &= 1 - \frac{\Delta U_{C_1}}{2U} = 1 - \frac{V_o D_1}{2V_{in2} R_L C_1 f_s}. \end{aligned} \quad (23)$$

The curve of the charging efficiency η_{charge} versus capacitance C_1 and frequency f_s under the condition of $V_o = 40$ V, $D_1 = 0.45$, $R_L = 8 \Omega$, and $V_{in2} = 30$ V is shown in Fig. 12. It is noticed that charging efficiency can be improved by increasing

Fig. 12. Curve of the charging efficiency η_{charge} versus C_1 and f_s .

TABLE I
UTILIZED COMPONENTS AND PARAMETERS

Components and parameters	Value
Main control chip	TMS320LF2407A EPM7128STC100-7
Driving chip	IR2110+HCPL-J312
Power switch (MOSFET)	IRFP250M (200 V, $R_{DS(on)} = 0.075 \Omega$, 33 A at 25 °C)
Bootstrap capacitor C_1	16.5 mF/220 μF
Filter inductance L_f (μH)	400
Filter capacitance C_f (μF)	300
Switching frequency f_s (kHz)	50
Input source 1 V_{in1} (V)	50
Input source 2 V_{in2} (V)	30
Input power P_{in1} (W)	125
Load power in Mode I/II/III P_o (W)	200/100/200
Output voltage V_o (V)	40

C_1 and f_s . The proposed converter is based on high-frequency charge–discharge of the capacitor; therefore, the capacitor must have enough margins in order to keep the converter functioning reliable under the condition of overtime running. Hence, here five 3300 $\mu\text{F}/60$ V electrolytic capacitors in parallel are employed in the experiment to meet the ripple and the charging efficiency requirements.

V. EXPERIMENTAL VERIFICATIONS

A 200-W experiment prototype was built to verify the feasibility of the proposed double-input dc–dc converter with bootstrap circuit. The key parameters are given in Table I.

A. Steady-State Experiment

Fig. 13 shows the experimental waveforms of u_{AB} , u_o and i_o . Fig. 13(a) shows the experimental waveforms of operating Mode I when $P_o > P_{in1}$. It shows that u_{AB} has a three voltage levels, which indicates that the two input sources deliver power to the load simultaneously. It also can be seen that the duty cycles of D_1 and D_2 , for S_{12} and S_{21} are 0.48 and 0.6, respectively, which matches the analysis well in (9) by ignoring the transistor voltage drop. Fig. 13(b) shows the experimental waveforms in operating Mode II when $P_o < P_{in1}$ and the load power is only provided by the input source 1. It can be seen that the duty cycle of D_1 for S_{12} is 0.83. The experimental results verify the equation derived in (9).

Fig. 13. Experimental waveforms of u_{AB} , u_o , i_o . (a) Mode I. (b) Mode II.

The steady waveforms of the converter in operating Mode III is shown in Fig. 14. Fig. 14(a) shows the experimental waveforms of u_{AB} , u_o , and i_o in this mode. It can be seen that u_{AB} has two voltage levels with a dc bias. The corresponding duty cycle of D_1 , for S_{12} is 0.45. According to the formula derived in (4), the theoretical value of the output voltage is larger than the actual value. That is because u_{C1} is slightly less than V_{in2} due to the voltage drop of charging path. Fig. 14(b) shows the experimental waveforms of bootstrap capacitor voltage u_{C1} and input source $2V_{in2}$. The driving signal and drain-to-source voltage on S_{C2} are given in Fig. 14(c), which indicates that the voltage on S_{C2} is capacitor voltage when switch is turned off.

Fig. 15 shows enlarged waveforms of u_{C1} with different capacitance. It can be seen that Δu_{C1} becomes larger with the decrease of the capacitance. In the case that $C_1 = 16.5$ mF, the voltage variation in charging time is only 40 mV, while in the case of 220 μF , it increases to 0.6 V. Fig. 15 also shows the waveforms of the charging current. With a large capacitance of 16.5 mF, the charging current will continue to rise in a switching cycle, whereas in the case of 220 μF , it will rise at first and then go down. In the discharging time, i_{C1} can be considered to be unchanged. The experimental results can match the analysis well.

B. Mode Transition Experiment

The transient waveforms with stepping up and down load resistor are given in Fig. 16(a). It can be seen that when the output load transforms between 2.5 and 4 A, the converter is shifted between Mode II and Mode I. However, it is observed that during mode transients, the output voltage u_o has a large overshoot due to the low bandwidth of the voltage loop. The operation mode switching between Mode II and Mode III are tested, and

Fig. 14. Experimental waveforms in Mode III. (a) u_{AB} , u_o , i_o . (b) u_{C1} , and u_{in2} . (c) Driving signal and drain-to-source voltage on S_{C2} .

Fig. 15. Experimental waveforms of u_{C1} and i_{C1} with. (a) $C_1 = 16.5$ mF. (b) $C_1 = 220$ μF.

Fig. 16. Experimental waveforms of mode transition. (a) Between Modes II and I. (b) Between Modes II and III. (c) Between Modes I and III.

the waveforms are presented in Fig. 16(b). When the converter operates at Mode II, the input source 1 supplies the load and $u_{C1} = V_{in1} > V_{in2}$. When the input source 1 is powered off, u_{C1} decreases until $u_{C1} < V_{in2}$. After the converter is switched from Mode III to Mode II, the input source 1 can charge C_1 , and the output voltage has a small drop. The operation mode switching between Mode I and Mode III are also tested and the waveforms are given in Fig. 16(c). It can be seen that the output voltage is regulated well as a constant during the mode transition.

C. Efficiency Curves Analysis

The efficiency curves of the converter have been tested and given in Fig. 17. It can be seen that the efficiency of the converter is about 92%–96%. When the output power is in the range of 40–110 W, the input voltage of Mode II is 50 V, while the value of Mode III is assumed to be 60 V, making the current of Mode III smaller than that of Mode II. Based on this, it can be concluded that the efficiency in Mode III is higher than that in Mode II at the same output power. Similarly, with a range of 110–200 W, the input voltage of Mode I is 80 V, making the current of Mode I smaller than that of Mode III. Hence, the efficiency of Mode III is lower than Mode I under the same output power.

Fig. 17. Overall efficiency in different operation modes.

Mode IV is a double-input MIC mode under condition $V_{in1} = 30$ V, $V_{in2} = 30$ V, and $V_o = 40$ V, which is done to illustrate the extra power loss in Mode III, where the two input sources share V_{in2} by the help of bootstrap circuit. It can be seen that the efficiency of Mode III is only a little lower than Mode IV because of charging loss.

VI. CONCLUSION

In this paper, a robustness design of a double-input dc–dc converter under one port powered off is proposed to overcome distributed power source randomness and intermittency, in which with the help of bootstrap switch pair, the renewable source port can be charged by the FC port and keeps to work when the alternative source is shut down. Simulation and experimental tests were carried out to validate the effectiveness of the proposed scheme against input source powering off. The proposed converter offers the advantage of simple topology and control, and high efficiency, which is suitable for renewable power system.

REFERENCES

- [1] K. Jin, X. Ruan, M. Yang, and M. Xu, "A hybrid fuel cell power system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1212–1222, Apr. 2009.
- [2] W. Jiang and B. Fahimi, "Active current sharing and source management in fuel-battery hybrid power system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 752–761, Feb. 2010.
- [3] L. Khanh, J. Seo, Y. Kim, and D. Won, "Power management strategies for a grid-connected PV-FC hybrid system," *IEEE Trans. Power Delivery*, vol. 25, no. 3, pp. 1874–1882, Jul. 2010.
- [4] Z. Liao and X. Ruan, "Energy management control strategy for stand-alone photovoltaic power system," in *Proc. CSEE*, Jul. 2009, vol. 29, no. 21, pp. 46–52.
- [5] Y.-M. Chen, Y. C. Liu, and S. H. Lin, "Double-input PWM DC–DC converter for high/low-voltage sources," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1538–1545, Oct. 2006.
- [6] D. Yang, M. Yang, and X. Ruan, "One-cycle control for double-input DC/DC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4646–4655, Nov. 2012.
- [7] Z. Qian, O. Abdel-Rahman, H. Al-Atrash, and I. Batarseh, "Modeling and control of three-port DC/DC converter interface for satellite applications," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 637–649, Mar. 2010.
- [8] A. Kwasinski, "Identification of feasible topologies for multiple-input dc–dc converters," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 856–861, Mar. 2009.
- [9] Y. C. Liu and Y. M. Chen, "A systematic approach to synthesizing multiple-input dc–dc converter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 116–127, Jan. 2009.
- [10] Y. Li, X. Ruan, D. Yang, F. Liu, and C. K. Tse, "Synthesis of multiple-input DC/DC converters," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2372–2385, Sep. 2010.
- [11] Q. Wang, J. Zhang, X. Ruan, and K. Jin, "Isolated single primary winding multiple-input converters," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3435–3442, Dec. 2011.
- [12] F. Liu, J. Ruan, and X. Ruan, "A systematic approach to synthesize multi-port DC/DC converters—adopting unipolar pulsating source cells," in *Proc. CSEE*, Feb. 2012, vol. 32, no. 6, pp. 72–80.
- [13] F. Liu, Y. Mao, Z. Wang, and X. Ruan, "Asymmetrical double-input DC/DC converters adopting pulsating voltage source cells," in *Proc. CSEE*, vol. 32, no. 21, pp. 15–22, Jul. 2012.
- [14] J. L. Duarte, M. A. M. Hendrix, and M. G. Simões, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 480–487, Mar. 2012.
- [15] C. Zhao, S. D. Round, and W. Johann, "An isolated three-port bidirectional DC–DC converter with decoupled power flow management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443–2453, Sep. 2008.
- [16] M. Sarhangzadeh, S. H. Hosseini, M. B. B. Sharifian, and G. B. Gharehpetian, "Multiinput direct DC–AC converter with high-frequency link for clean power-generation systems," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1777–1789, Jun. 2011.
- [17] F. Nejabatkhah, S. Danyali, S. H. Hosseini, M. Sabahi, and S. M. Niapour, "Modeling and control of a new three-input dc–dc boost converter for hybrid PV/FC/battery power system," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2309–2324, May 2012.
- [18] A. Khaligh, J. Cao, and Y. Lee, "A multiple-input DC–DC converter topology," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 862–868, Mar. 2009.
- [19] Y. Li, D. Yang, and X. Ruan, "A new double-input DC–DC converter," *Trans. China Electrotech. Soc.*, vol. 23, no. 6, pp. 77–82, Jun. 2008.
- [20] Y. Li, X. Ruan, D. Yang, and F. Liu, "Interleaved dual-edge modulation scheme for double-input Buck converter," *Trans. China Electrotech. Soc.*, vol. 24, no. 4, pp. 139–146, Apr. 2009.
- [21] Y. Li, X. Ruan, D. Yang, and F. Liu, "Modeling and design of control system for double-input DC/DC converter," *Trans. China Electrotech. Soc.*, vol. 25, no. 11, pp. 90–99, Nov. 2010.
- [22] L. Solero, A. Lidozzi, and J. A. Pomilio, "Design of multiple-input power converter for hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1007–1016, Sep. 2005.