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Analysis and Design of 10 MHz Capacitive Power Transfer with Multiple Independent Outputs for Low Power Portable Devices

Morten Birkerod Lillholm, Student Member, IEEE, Yi Dou, Student Member, IEEE, Xu Chen, Member, IEEE, and Zhe Zhang, Senior Member, IEEE

Abstract—This paper proposes a multiple-output capacitive power transfer (CPT) system using the LCCL compensation network for low-power (<20 W) battery charging application, e.g., consumer electronics. For CPT, reliable operation is still a challenge under a wide range of receiver configurations, due to variations in receiver position or load impedance. In this paper, employing constant voltage property of the LCCL network, the proposed multiple-output CPT system is able to achieve output independence among different receivers. Moreover, based on first harmonic approximation, a design method is proposed and studied in depth to maintain a minimal current stress on power devices and inductors, as well as zero voltage switching (ZVS) within a defined range. The proposed method considers the impact of component value ratios to limit the resonant current magnitude and determine the phase angle, and selects inductance values for the most efficient system operation. Finally, a constructed 10 MHz experimental prototype achieves capacitive power transfer from one transmitter to three independent 5 W receivers, with plate voltages less than 55 V. The measured power efficiency of the prototype is up to 83.6% at 15 W output.

Index Terms—Capacitive power transfer, wireless power transfer, LCCL compensation, constant voltage property, multi-output wireless power transfer

I. INTRODUCTION

Wireless power transfer (WPT) is an emerging technology whereby power is transferred without direct connection by an electric conductor. WPT has received increasing attention in recent years, with wireless charging of mobile phones becoming available using the Qi standard in 2012 [1]. It has also been applied to medical implants [2] and electric vehicles (EVs) [3]. So far, inductive power transfer (IPT) is the most widespread approach. More recently, capacitive power transfer (CPT) was proposed as a method of WPT. Compared to IPT, CPT has less loss through eddy currents in surroundings [4], and lower cost in fabrication of coupling structures [5]. Besides, CPT has potential for increased positional freedom, therefore, which makes more and more new applications possible for WPT with capacitively coupling [6].

A resonant compensation network is required to compensate for the capacitive impedance of the CPT coupling. These compensation networks are usually tuned to operate in receiver and transmitter well aligned conditions, so that have well constrained coupling capacitance. Various methods are proposed taking component value variation into account, for instance, [7] using the double-sided LC compensation network. Besides, some publications have considered the consequence of transient changes in the coupling capacitance, when for instance the receiver is removed [8], [9]. However, very few publications have demonstrated CPT with multiple outputs and their associated compensation network design. In [10] a 3-output CPT system was realised using a CLC-resonant circuit with a tunable inductor and a large relay-switched matrix grid of many capacitive coupling plates, which complicates the circuit and requires many components. Commonly, compensation networks are tuned to output a constant current into the capacitive coupling structures or to the receiver. This approach is beneficial for single output systems, if the transmitter and receiver coupling capacitances are already known and kept constant. However, this is not practical for a multi-output system and the constant current operation cannot be well maintained if receivers are suddenly added or removed. Furthermore, it is difficult to achieve independence between receivers with the constant current approach.

The research into compensation network topologies for CPT can roughly be divided into LC networks, CL networks or combinations thereof. The receiver circuit often mirrors the transmitter circuit, creating a symmetric or double-sided compensation network. Conversely, some have single-sided topologies [11], [12]. The simplest is series L compensation, as proposed in [13], [14], which can be considered a subgroup of LC networks. LC compensation operating with a constant load current and its associated voltage stress optimisation has been proposed in [15]. Also, CL compensation was proposed in [16] operating with constant load current and voltage stress optimisation. Furthermore, LC compensation has been shown to work in both constant load voltage and constant load current operation. A common issue with L and LC compensation is that they are sensitive to variation in coupling capacitance, and it has been proposed that LCLC topologies are less sensitive to variations in frequency and may achieve higher efficiency [17]. LCL and LCLC compensation networks have been proposed in [5] and [18] to operate with constant load current. Adding multiple stages of LC networks together may be more efficient in theory, however, this has not been verified experimentally [19]. Transformer based networks have been proposed to transform the capacitive impedance and boost the plate voltage such as the CLLC-like coupled inductor system

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in [20].

A common trait shared between these single-receiver systems is that they are analysed in a single stage, treating the transmitter and receiver as a single resonant circuit. However, this is not useful for multi-output systems. In order to achieve independence between receivers, a two-stage approach is required, such as the proposed multiple output system in [10]. The first stage is a transmitter-side CLC network acting as a voltage source on the capacitive coupling plates. The second stage is a receiver-side CLC network in the constant load current mode, enabling multiple receivers. Transmitter-side LC and LCLC networks cannot be used as voltage sources on the capacitive coupling, while also allowing ZVS. This renders them less practical for a multi-output CPT system using the two-stage approach.

An LCCL compensation network has been proposed for IPT [21]–[23]. Due to its ability to allow ZVS of the inverter while operating in constant voltage mode, the LCCL network is a promising solution for a multi-output CPT system. Furthermore, in order to improve power transferring capability and reduce capacitor plate voltages of a CPT system, switching frequency must be increased significantly, since it is directly proportional to power but inversely to plate voltage. In [24], an efficient 13.56 MHz CPT system has been demonstrated. More importantly, for consumer electronics, lower plate voltage is very critical and has become an major concern for usability of CPT in the future. Therefore, ensuring soft switching operation, i.e. zero voltage switching (ZVS) or zero current switching (ZCS), as well as its parameter design methodology, has significance to high frequency CPT systems.

This paper proposes a CPT system with multiple outputs, where the power transfer to each receiver is independent from other receivers. This is achieved by ensuring a load-independent voltage across the transmitter capacitive coupling plates. The LCCL resonant circuit is adopted as a transmitter side compensation network for CPT. The LCCL network is operated in the constant voltage mode to ensure power delivery over a wide load range. Accordingly, an analysis and design method is proposed to select the LCCL parameters that will minimise the input resonant current and therefore reduce both losses and component stress. Moreover, this method takes into account soft switching criteria to guarantee ZVS from zero up to a desired numbers of receivers. The parallel-series LC network is used for the secondary side compensation in each receiver. This circuit utilises parasitic capacitance in the capacitive coupling structure and the junction capacitance of rectifier diodes to achieve constant current delivered to the load in well aligned cases. An experimental prototype is constructed and verifies the efficient power transfer from one transmitter to three receivers. The observed plate voltages of 55 V are much lower than other works, thus reducing safety concerns.

This paper is organised as follows. After this introduction, Section II presents a simple 3-capacitor model of the capacitive coupling with multiple outputs. Section III analyses the LCCL primary compensation network. A method for minimising the resonant current and achieving ZVS is studied. Section IV provides the design equations for the secondary compensation network. Section V gives the multi-output CPT prototype design and the experimental results verifying the operation of the prototype. Section VI concludes the paper.

II. MULTIPLE-OUTPUT CPT SYSTEM

An overview of the multiple output CPT system is shown in Fig. 1. On the transmitter (or primary) side, the inverter generates an ac voltage, which drives a primary side compensation network. The compensation network is a resonant circuit used for impedance transformation of the capacitive coupling, so that it supplies an ac current to a capacitive coupling structure. This capacitively coupled structure is made of a pair of transmitter conductive plates that couple across the isolation barrier and air gap to several pairs of receiver (or secondary) side conductive plates. The secondary side may have a compensation network, which then can supply an ac current to a rectifier and a load.

Several capacitive coupling structures have been proposed, incl. two-plate structure [25], [26], four-plate parallel structure [17], four-plate stacked structure [5], [20] and six-plate structure [27]. Also more complicated structures using many coupling plates have been proposed to increase the positional freedom [28]–[30]. All these structures are modelled in a similar way and thus the 4-plate parallel structure can be used as an example due to its simplicity [31]. The capacitance of the four-plate parallel coupling structure is modelled as in [5]. The resulting 3-capacitor Π-shaped model for a single receiver is shown in Fig. 2. Assuming a simple resistive impedance of the receiver circuit placed on the $V_2$ terminal, several receivers can be placed in parallel as shown in Fig. 3, where each circuit component can assume different values.
To facilitate further analysis, it is assumed that all receivers are identical. This allows the simplification of the circuit in Fig. 3 to a single equivalent circuit with \( N \) identical receivers in Fig. 4. This assumption is useful because the analysis is performed as seen from the transmitter. The transmitter will only see the combined total impedance of all receivers, \( Z_o \) defined as (1). This means that several smaller receivers might look similar to one larger receiver, in terms of the load impedance on the transmitter side. As seen from the transmitter, the impedance is mainly capacitive in any case. The main concern is to create an upper and lower limit for the capacitive loading on the transmitter. If it is guaranteed by design, that the impedance does not exceed these boundaries, the circuit can be analysed within the limited design space. The following analysis will use the circuit in Fig. 4 to calculate the impedance (2) with parameters given in (3) and (4). This will estimate the load impedance seen from the transmitter as multiple receivers are added.

\[
Z_o = \frac{V_1}{I_C} \quad (1)
\]

\[
Z_o = \frac{j (C_M + C_S) R \omega + 1}{j (C_M + C_P) \omega - (C_P C_S + C_M C_S + C_M C_P) R \omega^2} \quad (2)
\]

where

\[
C_P = C_{P_0} + N C_{P_N}, \quad C_M = N C_{M_N}
\]

\[
C_S = N C_{S_N}, \quad R = \frac{R_N}{N} \quad (4)
\]

A. Limitations of the Identical Receiver Model

The model of a multiple receiver system presented in Fig. 4 has some limitations if used as a general model. The model is valid if:

- Receiver circuit is resistive
- Receivers are well aligned
- There is little parasitic capacitance
- Receivers are identical or a scaled version of each other

If these assumptions cannot be secured, a more complicated model might be required, depending on the application. Otherwise, if a secondary compensation circuit is used, the values in Fig. 4 may be transformed to apply with the model. For the application in this paper, which serves as an example of the concept, the model is adequate.

III. PRIMARY SIDE LCCL COMPENSATION NETWORK ANALYSIS FOR CONSTANT VOLTAGE OPERATION

The LCCL primary compensation circuit is shown in Fig. 5. It is excited by an high frequency ac voltage \( V_{ac} \) from the inverter. Using the first harmonic approximation (FHA), this voltage is assumed to be sinusoidal. The compensation circuit generates a voltage across the impedance \( Z_o \), which is calculated by (2). The purpose of the LCCL circuit is to compensate for the capacitive impedance of the capacitive coupling to improve power transfer. There are 3 design goals of the primary compensation circuit that must be achieved:

1) Maintain constant magnitude of primary side plate voltage \( V_1 \)
2) Achieve zero voltage switching (ZVS) of the inverter
3) Minimise the input current \( I_1 \) into the resonant circuit

The magnitude of voltage \( V_1 \) must be maintained at a constant level no matter how many receivers are coupled. This is required to achieve independence of all the receivers, so that the power transfer to each receiver is not affected by other receivers even if they are on the same transmitter. The voltage gain \( G_{v1} \) is defined as (5). The voltage gain is normalised to the constant voltage gain and plotted in Fig. 6, where the number of receivers, \( N \), is 0 to 3.

It is observed that there exists a constant voltage frequency \( \omega_{CV} \) where the gain \( G_{v1} \) of the LCCL circuit is constant no matter how many receivers are coupled. The gain \( G_{v1,CV} \) at this frequency is defined as (6).

\[
G_{v1} = \frac{|V_1|}{|V_{ac}|} \quad (5)
\]

\[
G_{v1,CV} = G_{v1}(\omega_{CV}) \quad (6)
\]

The voltage gain \( G_{v1} \) is calculated by solving the nodal equations of the circuit in Fig. 5. The derivative of (5) with regards to \( Z_o \) must be zero to find the constant voltage frequency \( \omega_{CV} \). Solving (7) yields the expression (8) for \( \omega_{CV} \).
The phase angle $\phi$ of the input current $I_1$ depends on the capacitive loading on the transmitter plates. This means that adding multiple receivers will alter $\phi$ as seen in Fig. 7. At a specific capacitive load, $\phi$ becomes zero. This is the zero phase angle (ZPA) point. Increasing $N$, and thus increasing the capacitive load, beyond the ZPA point results in a positive $\phi$. This is undesired, as ZVS requires a negative $\phi$. The circuit can be tuned to ensure non-positive $\phi$ for any capacitive load, up to a defined maximum capacitive load by selecting the correct value of $\gamma$ as defined in (11). The effect of $\gamma$ on $\phi$ is illustrated in Fig. 8a. Lower values of $\gamma$ will increase the maximum capacitive load, at which ZVS is possible.

An important design goal is to minimise the magnitude of the resonant current $I_1$ to avoid excessive current stress on the inverter and inductor $L_1$. The ratio $\gamma$ affects the transconductance $G_{i_1}$ defined by (16) and thus the resonant current, shown in Fig. 9a. The circuit can be tuned to achieve a minimal resonant current by selecting the appropriate value of $\gamma$.

At $\gamma = \gamma_{opt}$, the current magnitude $I_1$ is the lowest while still ensuring non-positive phase angle $\phi$. If $\gamma$ is decreased from this value, the resonant current increases for the defined cases, as seen in Fig. 9a.

$$Z_{\text{in}} = \frac{V_{ac}}{I_1} = \frac{j\gamma\sqrt{\alpha}Z_o}{j\gamma\sqrt{\alpha}(\beta + 1)^2 + (\beta^2 + (2 - \gamma)\beta + 1)Z_o}$$  \hspace{1cm} (15)

### A. Magnitude and Phase of Resonant Current $I_1$

The input current $I_1$ can be minimised only for a specific load condition, meaning a specific value of $Z_o$. In that scenario, the load impedance $Z_o$ has a value, which can be defined as the optimisation impedance $Z_{opt}$. Assuming $Z_{opt}$ is a complex impedance of the form (17), the input impedance of the LCCL resonant circuit can be found by substituting (17) into (15). The resulting input impedance is (18).

$$Z_{opt} = R_{opt} + jX_{opt}$$  \hspace{1cm} (17)

$$Z_{in} = \frac{V_{ac}}{I_1} = \frac{j\gamma\sqrt{\alpha}(R_{opt} + jX_{opt})}{j\gamma\sqrt{\alpha}(\beta + 1)^2 + (\beta^2 + (2 - \gamma)\beta + 1)(R_{opt} + jX_{opt})}$$  \hspace{1cm} (18)

The magnitude of $Z_{in}$ has the maximum value at the optimal $\gamma$, which is found by solving (19) for the derivative of $|Z_{in}|$ equal to zero.

$$\frac{\partial}{\partial \gamma} |Z_{in}| = 0$$  \hspace{1cm} (19)

The optimal ratio $\gamma_{opt}$, which will minimise the input current $I_{1}$ for a given $Z_{opt}$, is then expressed as (20). If using this expression, $\gamma$ is no longer an independent variable,
but rather a function of $\alpha$ and $\beta$ as well as the chosen load impedance $Z_{opt}$.

$$\gamma_{opt} = \frac{(\beta + 1)^2 (R_{opt}^2 + X_{opt}^2)}{\beta (R_{opt}^2 + X_{opt}^2) - \sqrt{\alpha} (\beta + 1)^2 X_{opt}}$$  \hspace{1cm} (20)$$

Moreover, the value $\gamma_{opt}$ will result in a minimal magnitude and zero phase angle of the current $I_1$ if the load impedance $Z_o = Z_{opt}$.

B. Plate Voltage Limit and Switching Frequency

Voltage gain $G_{v1}$ depends on the capacitance ratio $\beta$ as expressed in (14). When increasing the voltage gain $G_{v1}$, the input current $I_1$ must increase, according to energy conservation. This means that the selection of $\beta$ must consider both the desired voltage gain and the input current $I_1$, in order to avoid excessively large input currents. If the current $I_1$ must be limited to a safe level, then the value of $\beta$ must be calculated from the $Z_o$ that results in the largest input current $I_1$. Substituting (20) into (18) and solving for $\beta$ yields (24), with $\xi$ defined as (23), where $I_{1_{max}}$ is the maximally allowed current $I_1$. Note that now, $\beta$ is independent of $\alpha$.

$$a_0 = R_{opt}^4, \hspace{1cm} a_1 = -2R_{opt}^2 X_o, \hspace{1cm} a_2 = R_o^2 + 2R_{opt}^2 + X_o^2, \hspace{1cm} a_3 = -2X_o X_{opt}^2$$ \hspace{1cm} (21)$$

$$\xi = \frac{(R_o^2 + X_o^2)(R_{opt}^2 + X_{opt}^2)^2}{X_{opt}^4 + a_3 X_{opt}^3 + a_2 X_{opt}^2 + a_1 X_{opt} + a_0}$$ \hspace{1cm} (22)$$

$$\beta = \sqrt{\frac{I_{1_{max}} \sqrt{\xi}}{V_{ac}}} - 1 = \sqrt{G_{v1} \sqrt{\xi}} - 1$$ \hspace{1cm} (24)$$

If using (24), the current $I_1$ will not exceed the limit value $I_{1_{max}}$ at $Z_o$. The limit for $\beta$ is found as a function of the input current, input voltage and the load impedance, and a solution plane can be defined. Using (14) and assuming a half-bridge inverter employed with an input voltage $V_{in}$, $V_{ac}$ can be calculated by (25) [32]. In Fig. 10, the resulting limit of the plate voltage $V_1$ as a function of frequency is shown for an input current $I_{1_{max}} = 5$ A. The solution plane is the area bounded by the curve and the axes of the plot. This means that any point on the curve will result in an input current of exactly $5$ A in this case. It is seen that a higher frequency demands a lower plate voltage, and furthermore an increase in input voltage allows higher plate voltages.

$$V_{ac} = \frac{2V_{in}}{\pi}$$ \hspace{1cm} (25)$$

C. Minimal Inductor Loss

The ratio $\alpha$ determines how large the inductance is relative to the capacitance in the LCCL network. Bigger $\alpha$ means larger inductance. If using (24), the current magnitude $I_1$ is independent of the value of $\alpha$. However, bigger inductance may result in larger series resistance. Conversely, the inductor current $I_{L2}$ does, in fact, depend on $\alpha$. This means there is an optimal value of $\alpha$, which can be found by using FHA.

Defining inductor quality factor $Q_L$ as (26), then the power loss in inductor $L_1$ is written as (27). Due to the constant voltage property, the voltage $V_1$ is constant across inductor $L_2$, meaning that the power loss in $L_2$ is expressed as (28).

$$Q_L = \frac{\omega L}{R_L}$$ \hspace{1cm} \hspace{1cm} (26)$$

$$P_{L1} = \frac{I^2_{RMS} \sqrt{\alpha}}{Q_{L1}}$$ \hspace{1cm} (27)$$
\[ P_{L_2} = \frac{V_{1RM}^2}{Q_{L_2} \gamma \sqrt{\alpha}} \]  (28)

The RMS value of the current with magnitude \( I_1 \) is found as (29) using the transconductance (16). The RMS of the voltage with magnitude \( V_1 \) is found as (30) using the voltage gain (14).

\[ I_{1RM} = \frac{V_{ac} G_{iv1}}{\sqrt{2}} \]  (29)

\[ V_{1RM} = \frac{V_{ac} (\beta + 1)}{\sqrt{2}} \]  (30)

To find the minimum, the derivative of the total inductor loss with respect to \( \alpha \) has to be zero as in (31).

\[ \frac{\partial}{\partial \alpha} (P_{L_1} + P_{L_2}) = 0 \]  (31)

By substituting (20) into (28) and solving (31) for \( \alpha \), the minimum inductor loss is found when the \( \alpha \) ratio is calculated as (32).

\[ \alpha = \frac{Q L_1 \beta}{Q L_2 G_{iv1}} \]  (32)

The assumption of purely sinusoidal current waveforms is valid if higher order harmonics are attenuated sufficiently by the LCCL network. Calculating the level of harmonic distortion that can be allowed is not within the scope of this paper, however, an estimation can be made regarding the validity of the approximation. At higher frequencies, the input impedance \( Z_{in} \) is dominated by the first LC network consisting of \( L_1 \) and \( C_1 \). The attenuation of higher order harmonics is then determined by the characteristic impedance \( Z_1 \) defined as (33). Larger \( Z_1 \) means more attenuation of higher order harmonic frequencies. Thus, increasing \( \alpha \) will decrease the harmonic distortion of the resonant current.

\[ Z_1 = \sqrt{\frac{L_1}{C_1}} \]  (33)

D. Design Procedure

The design flow for the LCCL primary compensation network is shown in Fig. 11. Only four initial parameters are required for the design. The operating frequency \( \omega \), the minimal number of receivers \( N_{min} \), the maximal number of receivers \( N_{max} \) and the transconductance \( G_{iv1} \). The resulting load impedances are then calculated for the minimal case \( N_{min} \) and \( N_{max} \). If using \( N_{min} = 0 \), then \( Z_{min} \) is found using the capacitance of the capacitive coupler without any receivers. The optimisation impedance \( Z_{opt} \) can be based on the maximal number of receivers \( N_{max} \). This will ensure a minimum of the input current at \( N = N_{max} \). When \( \beta \), \( \gamma \) and \( \alpha \) are found, the FHA must be validated in the case that \( \alpha \) is very small, for instance by using (33). Increasing \( \alpha \) may be necessary to reduce harmonic distortion of the resonant current. Finally, the component values can be found. The resulting design should achieve the following criteria:

- Current magnitude \( I_1 \) does not exceed the value given by \( G_{iv1} \)
- Current magnitude \( I_1 \) is minimal at \( N_{opt} \)
- Current magnitude \( I_1 \) is maximal at \( N_{min} = 0 \)
- Phase angle of current \( I_1 \) is negative for \( N = [0, N_{opt} - 1] \)
- Phase angle of current \( I_1 \) is zero for \( N = N_{opt} \)

IV. Parallel-Series LC Secondary Compensation

The secondary side compensation network is a parallel-series (PS) LC resonant circuit as shown in Fig. 12. This circuit can be made with two external components, the inductor \( L_3 \) and the capacitor \( C_3 \). The parallel capacitance \( C_S \) already exists due to the capacitive coupling structure. The capacitance \( C_D \) is the equivalent parallel capacitance in the rectifier, typically from a diode bridge. The resulting compensation network can utilise the parasitic capacitance in the circuit. The voltage to current magnitude transfer function \( G_{iv2} \), defined as (34), is plotted in Fig. 13, and normalised to the

\[ V_{out} = \frac{V_{in}}{\frac{1}{G_{iv2}}} \]
Fig. 12. Topology of secondary parallel-series LC compensation circuit

Fig. 13. Transconductance dependence on frequency of the PS LC circuit

calculated as (38), based on the desired transconductance \( G_{iv2} \). If desired, external capacitance can be added in parallel with \( C_D \) or \( C_S \), it will reduce the required inductance and increase the inductor current through \( L_3 \).

\[
L_3 = \frac{G_{iv2}}{\omega_{CC}^2 (C_M C_D \omega_{CC} + C_M G_{iv2} + C_S G_{iv2})}
\]

The external capacitance \( C_3 \) can then be found as (39). Generally, a smaller value of \( C_3 \) will result in a higher transconductance.

\[
C_3 = \frac{C_D C_M \omega_{CC}}{G_{iv2} - C_M \omega_{CC}}
\]

From (39) it is apparent that the transconductance \( G_{iv2} \) has a minimum value if the circuit has to be implemented with positive capacitance values. The minimal current gain is expressed as (40).

\[
G_{iv2} \geq C_M \omega_{CC}
\]

The effect parasitic capacitance was not studied in depth for this paper, however some considerations can be stated. For the primary LCCL compensation network, the constant voltage property is in principle unaffected by changes in the coupling capacitance due to different receivers, and also due to parasitic capacitances. This means that the power transfer is unaffected but the efficiency might be affected, due to increasing resonant current. The tolerance to component value variation can be improved by using an external capacitance in parallel with \( L_2 \), however, at the cost of efficiency.

For the receiver side, the PS LC network relies on specific values of \( C_M \) and \( C_S \) to deliver the desired power level, and thus any decrease in \( C_M \) or increase in \( C_S \) will decrease the power transfer, and thus the system efficiency. This can be solved by the coupling structure geometry.

V. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL RESULTS

The proposed circuit for the multiple-output capacitive power transfer prototype is shown in Fig. 14. It consists of the half-bridge inverter, LCCL primary compensation network, the parallel-series LC secondary compensation network (in each of the the receivers) and a full-bridge diode rectifier. The power transistors used in the inverter are EPC8009 and the rectifier diodes are ZHCS1000 Schottky diodes. For the PS LC secondary compensation circuit, the component values are found using (38) and (39) based on a diode capacitance \( C_D = 150 \text{ pF} \). The prototype design parameters are shown in Table I. The coupling capacitances are found in Table II and assuming a single receiver only.

The estimated loss distribution for the CPT prototype is shown for 0 to 3 receivers in Fig. 15. The estimation is based on simulation of the circuit with manufacturer SPICE models for the EPC8009 FET and the ZHCS1000 diode, with a fixed dead-time of 3.5 ns for the power inverter gate signals. The inductor resistances at 10 MHz are measured to be: \( R_{L_1} = 66 \text{ m\Omega}, R_{L_2} = 155 \text{ m\Omega}, R_{L_3} = 600 \text{ m\Omega} \). The
inductors constitute around half of the loss in both the single receiver and the multiple-receiver case. When adding more receivers, the proportion of rectification loss increases and inverter loss decreases.

A. Coupler Experiment

A capacitive coupler based on the four-plate parallel structure is constructed. This simple structure is chosen to verify the functionality of the multiple receiver system. A top-down illustration of the coupler with 3 receivers is shown in Fig. 16 with physical dimensions. The gap between transmitter and receiver is less than 1 mm and consists of glass material, to ensure a large capacitance. The transmitter conductive plates are made of thin copper sheets and the receiver conductive plates are made of 0.2 mm copper tape.

A characteristic of the equivalent capacitances for the \( \Pi \)-model is shown in Fig. 17 for different positions in the Y-axis. The characteristic is roughly symmetric around \( Y = 30 \text{ mm} \).

In Fig. 18, the capacitances are shown across positions on the X-axis with \( Y = 30 \text{ mm} \). It shows little change along the length of the coupler.

B. Experimental Results

The experimental prototype is shown in Fig. 19. The prototype is tested with up to 3 identical receivers. The measured

![Fig. 14. Topology of transmitter and receiver with compensation (one receiver shown)](image1.png)

![Fig. 15. Estimated loss distribution at 5 W output power per receiver](image2.png)

![Fig. 16. Illustration of transmitter plates with 3 receivers](image3.png)

![Fig. 17. Capacitance for one receiver with varying Y-position fitted with a 4th order polynomial](image4.png)

![Fig. 18. Capacitance at center position Y = 30 mm across length of coupler](image5.png)
TABLE II
SELECTED CAPACITANCE VALUES FROM THE COUPLER CHARACTERISTIC

<table>
<thead>
<tr>
<th>Position</th>
<th>( C_{P_0} )</th>
<th>( C_{M_N} )</th>
<th>( C_{P_N} )</th>
<th>( C_{S_N} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center (( Y = 30 ) mm)</td>
<td>20 pF</td>
<td>91 pF</td>
<td>30 pF</td>
<td>38 pF</td>
</tr>
</tbody>
</table>

waveforms are obtained with a Rohde & Schwartz RTO 1024 2 GHz 10 Gsa/s oscilloscope and 500 MHz voltage probes. The current probe is a 50 MHz Hioki 3273-50.

The main function of the proposed LCCL compensation network is to maintain a constant magnitude of voltage \( V_1 \) between the transmitter plates. In Fig. 20 the voltage \( V_1 \) is for different number of receivers from \( N = 0 \) to \( N = 3 \) receivers. The voltage magnitude is maintained within \( \pm 2\% \). Therefore, the voltage is unaffected by the number of receivers that validates the constant voltage property in steady state.

In Fig. 21, a long time-scale experiment is shown. This experiment shows the current \( I_C \) flowing into the capacitive coupling from the transmitter side and the plate voltage \( V_1 \) as receivers are added to the coupler one by one. As each receiver is added, the current \( I_C \) jumps up to a higher magnitude. The voltage \( V_1 \) is maintained at around 50 V during the entire experiment, showing no transient overshoot due to the increased current consumption.

The secondary side plate voltage \( V_2 \) is not constant as it is related to the position and load of the receivers. In Fig. 22, the primary and secondary side plate voltages are shown at center alignment with 50 \( \Omega \) load. The amplitude of \( V_1 \) is 51 V and amplitude of \( V_2 \) is 55 V. There is approximately a 62\(^\circ\) phase shift between the voltages. Some distortion of \( V_2 \) is observed due to the non-linear diode behaviour.

According to the design method, the resonant current \( I_1 \) in inductor \( L_1 \) and the power inverter should decrease when receivers are added from 0 to 3, achieving minimal current at 3 receivers. This should result in lower power loss in the inverter. In Fig. 23, the inverter power loss is measured for 0 to 3 receivers and compared to the circuit simulation. As predicted, the power loss is reduced when adding receivers.

The power efficiency for a single receiver is shown in Fig. 24. This is shown at a constant output voltage of around 15 V. It is seen that the maximal power is around 4.7 W at around 67 % efficiency.

In Fig. 25 the efficiency for multiple receivers is shown at
Fig. 24. Power efficiency for single receiver at $V_{\text{out}} = 15$ V

Fig. 25. Power Efficiency for multiple receivers with $R_{\text{load}} = 50$ Ω

50 Ω on each receiver up to $N = 3$. The total system efficiency increases as more receivers are added. The efficiencies are 67%, 81% and 84% for 1, 2 and 3 receivers respectively.

In Fig. 26 the power output on a 50 Ω load is shown across different positions on the transmitter. The desired power is only achieved at the centered position. This is due to the geometry of the coupling structure. The measurements are compared to calculated values based on the transconductance from (34) and the fitted coupler characteristic shown in Fig. 17. The expected power level (5 W) is almost reached (4.7 W).

C. Comparison to Other Work

The work in this paper is compared to previous works as shown in Table III. The selection criteria for these works are that they demonstrate capacitive power transfer in the range of 1 W to 30 W and that all numbers are verified experimentally. The works in which the plate voltages in the capacitive coupling are not disclosed are thus excluded from this comparison. It is seen that this work achieves a very efficient power transfer at this power level. Furthermore is achieved at a much lower plate voltage than previous works. This is made possible due to the higher frequency of operation, facilitating higher power density. None of the compared works have demonstrated power transfer to multiple devices simultaneously, whereas this work demonstrates power transfer to 3 independent receivers.

VI. Conclusion

This paper has demonstrated a 10 MHz CPT system with multiple independent outputs. The multiple output CPT system was modelled as a single equivalent receiver circuit to determine the load impedance on the transmitter that simplified the design process. The constant voltage operation was proposed to achieve independence of the receivers. The LCCL compensation network design procedure was presented, where component value ratios can be used to minimise the current stress and therefore the loss in the inverter and resonant inductors. The design method can ensure ZVS operation. The current is minimised for the maximal number of receivers, meaning that the transistor and inductor loss is decreasing when more receivers are added, ensuring efficient operation at the highest output power levels. The experimental prototype verified the constant voltage operation and thus the independence of receivers. The prototype also showed an increasing efficiency with increasing number of receivers. The power transfer is achieved with low plate voltages of <55 V in all cases of operation. In the future, multiple-output CPT will be investigated for different coupling structures to improve the positional freedom. The concept can be expanded to even more receivers or different size receivers broadening the applicability. Further investigation could be made into the effect of detuning the inductance ratio to increase the ZVS operation, and higher power levels are possible with higher frequency, plate voltage or coupling capacitance.

REFERENCES


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