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Composite Robust Quasi-Sliding Mode Control of DC-DC Buck Converter With Constant Power Loads

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***Abstract*—To address the stability issues aroused by the negative-resistance effect of constant power loads (CPLs), this paper proposes a composite robust discretized quasi-sliding mode control (DQSMC) scheme for stabilization of buck-converter fed dc microgrids with CPLs. In the outer control loop, a robust DQSMC voltage controller is proposed. First, a discrete integral sliding surface is designed to obtain a fast and robust dynamic response of dc-bus voltage. Then, to tackle the varying load disturbances and model uncertainties, a second-order sliding mode disturbance observer is embedded in the voltage controller for disturbance estimation and compensation. The resulting composite DQSMC scheme features enhanced disturbance rejection, inherent chattering suppression, and guaranteed dynamics. Meanwhile, a PI current controller is retained in the inner control loop to realize the current control and limitation. Robustness and stability analysis of the whole composite controller are proved to assure large-signal stability. Simulation and experimental results confirm the superiority of the presented approach.**

***Index Terms*—Microgrid, buck converter, constant power load (CPL), chattering suppression, sliding mode control (SMC).**

I. Introduction

MICROGRID (MG) is emerging as an efficient solution for the high integration of distributed renewable energies (DREs), energy storage systems (ESSs), and flexible loads in modern power systems [1], [2]. Generally, MGs can be grouped as ac MGs and dc MGs by the property of common-bus voltage. In comparison to ac MGs, dc MGs, serving as more nature interfaces for various DREs, have gained wide acceptance in recent years due to their simple implementations (i.e., no reactive-power flow, harmonics, and synchronization issues), good compatibility, and high-efficiency [3].

In a dc MG, numerous power converters are configured as interfaces between DREs and loads, providing more flexible operation modes than an individual DER unit [4]. Nevertheless, these power-converter loads may cause adverse impacts when tightly regulated, since they exhibit constant-power-load (CPL) characteristics, i.e., incremental negative resistance effect. This effect may degrade the system damping and even destabilize the dc MGs [5]. Till now, numerous stabilization strategies have been proposed for dc MGs with CPLs. Initially, passive-damping methods are proposed to increase the system damping, which is implemented by passive components like resistors, inductors, or capacitors [5], [6]. However, these approaches inevitably increase power losses, thus decreasing system efficiency. In contrast, active-damping stabilization methods are proposed by adding extra control loops to adjust the virtual impedance without changing too much the system hardware [7], [8]. Nevertheless, this method is sensitive to the switching frequency and may degrade the load performance due to the nature of power injection [9]. Besides, the aforementioned methods can only stabilize dc MGs near nominal operating points since the linear small-signal model is adopted. When considerable disturbances occur, large-signal stability cannot be guaranteed using these approaches.

Given the nonlinear nature of power converters, nonlinear control algorithms have emerged as promising alternatives to stabilize dc MGs with CPLs under large-signal disturbances [10]–[13]. In [10], [11], model-predictive-control based CPL-stabilization approaches are proposed, which are realized by optimizing a predefined cost function. However, a non-negligible computational burden hinders the application of this approach. In [12], an adaptive back-stepping control strategy is proposed for the stabilization of boost converters loaded by CPLs, in which a Kalman filter or an observer is employed to realize the disturbance rejection. In [13], a finite-time controller is proposed for stabilizing CPLs, which enhances the system dynamic performance. However, these approaches are not intuitive and require a high level of expertise in control theory to understand and implement.

Note that sliding mode control (SMC) has gained increasing popularity for its merits of intuitive concept, strong robustness to model uncertainties, and low computational cost. Most of SMC schemes are designing a control law based on sliding function and system dynamic model (normally linear state-space model). The non-linearity of SMC is reflected by the controller itself, i.e., a sign function is included in the control law, which drives the system states to reach and maintain on the sliding surface. As a result, SMC's promising merit is inherent robustness and invariance to disturbances and parameter variations. Moreover, the stability of SMC can be verified by the Lyapunov theorem, thus the large-signal stability is guaranteed. Several SMC schemes have been investigated for DC-DC buck converters [14]–[18]. In [14], a hysteresis-modulated SMC is proposed to improve the dynamic voltage-tracking performance. However, this control

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strategy suffers from a variable switching frequency, which increases switching losses and complexity of filter design. To tackle these issues, pulse-width-modulation (PWM) based SMC scheme is proposed [15]. By mapping the duty cycle to the equivalent control signal, a constant switching frequency is obtained. In [16], a total SMC approach is proposed for boost converters, eliminating the approaching phase of the system states. In [17], a parabolic modulated SMC scheme is proposed, overcoming the drawbacks of hysteresis-modulated SMC while having a complex hardware circuit. However, the SMC schemes mentioned above only focus on stabilizing the resistive load. In [18], a duty-ratio based SMC scheme is proposed for stabilizing buck converters feeding CPLs over a wide load-variation range. Nonetheless, this method deteriorates the ripple filtering and the equivalent output impedance.

Besides, it is vital to mention that all the aforementioned SMC schemes are designed from the continuous-time domain viewpoint. The digital implementation is realized by discretizing the final continuous-time SMC (CSMC) control law, which may cause stability issues in digital implementations [19]. Practically, the control signal is frozen within a sampling period and only varies at each sampling instant, causing an actuation delay. As a result, ideal sliding motion in CSMC cannot be reached, and only a quasi-sliding mode (QSM) near the ideal sliding surface is obtained [20]. Theoretically, it is proved that the stability criterion of CSMC is not fully applicable to discrete cases, which is only a necessary condition for discrete stability [19]. Hence, discretized QSM control (DQSMC) cannot be converted from CSMC via simple equivalence. In other words, directly applying CSMC to discrete systems may cause unexpected chattering issues. Also, the parameter design of CSMC does not consider the sampling period in digital implementations. The performance of a well-designed CSMC may be degraded when executed by a digital controller due to the finite sampling frequency. Nevertheless, the research on DQSMC is still limited and insufficient [21]. Hence, developing a DQSMC based stabilization method for buck converter fed dc MGs with CPLs is of great attractiveness due to its intuitive concept, inherent robustness to various disturbances, and guaranteed discretization stability. If we can directly design a DQSMC with desired performance and guaranteed stability, there is no need to firstly design the CSMC and then convert it for digital implementations since the conversion would cause unexpected stability issues under certain sampling frequencies. Additionally, it should be noted that all the linear or nonlinear methods above cannot simply realize the current limitation for over-current protection.

To this end, this paper proposes a composite robust DQSMC scheme in a multi-loop framework for stabilizing the buck-converter fed dc MGs with CPLs. The contributions are as follows.

(1) A composite DQSMC voltage controller in a multi-loop framework is proposed for stabilizing the bus voltage, featuring strong versatility, fast dynamic performance, enhanced robustness, and simple current limitation.

(2) A second-order sliding mode disturbance observer (S^2MDO) with a finite time convergence rate is embedded for lumped-disturbance compensation, enhancing the disturbance and chattering suppression capability of the overall system.

(3) Stability, robustness and chattering analysis of proposed controller are given, guaranteeing both discretization stability and large-signal stability.

The rest of this work is arranged below. Section II is the system description. Section III elaborates the principle of proposed controller. Section IV presents the simulation and experimental results, and Section V concludes the work.

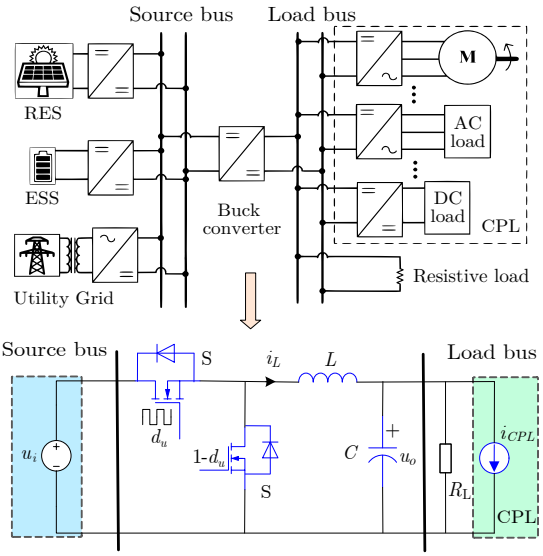

Fig. 1. Topology of a DC-DC buck converter feeding CPLs in a dc MG.

II. System Modeling and Problem Statement

Fig. 1 depicts a typical topology of DC-DC buck power converter based dc MG and its equivalent circuit, which comprises a source-bus voltage u_i, a DC-DC buck converter, and a load-bus voltage u_o with various loads. The source bus is powered by DREs, ESSs or the utility grid. The intermediate buck converter aims to adjust the source-bus voltage level to the load-bus voltage level. Multiple CPLs (such as DC/AC or DC-DC converter loads) or resistive loads are connected to the load bus, which can be modeled as a voltage-controlled current source [9]

$$i_{CPL} = \frac{P_{CPL}}{u_o} \tag{1}$$

where P_{CPL}, u_o and i_{CPL} donate the power, voltage and current of a CPL, respectively.

Correspondingly, the nominal dynamic model of a DC-DC buck converter with a CPL in Fig. 1 is described as

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{u_i}{L}d_u - \dfrac{u_o}{L} \\ \dfrac{du_o}{dt} = \dfrac{1}{C}i_L - \dfrac{u_o}{R_L C} - \dfrac{P_{CPL}}{Cu_o} \end{cases} \tag{2}$$

where u_i, u_o, i_L, and $d_u \in [0, 1]$ are source-bus voltage, load-bus voltage, filter-inductor current and duty ratio, respectively.

Considering the varying load disturbances and system-parameter uncertainties, the first-order voltage state-space model is derived from (2) as

$$\frac{du_o}{dt} = -\frac{1}{R_L C}u_o + \frac{1}{C}i_L + \omega \tag{3}$$

where ω is the lumped disturbance, which is assumed to be bounded and defined as

$$\begin{aligned}\omega = &(\frac{1}{R_L C} - \frac{1}{(R_L+\Delta R_L)(C+\Delta C)})u_o \\ &+ (\frac{1}{C+\Delta C} - \frac{1}{C})i_L - \frac{P_{CPL}}{(C+\Delta C)u_o}\end{aligned} \tag{4}$$

where ΔR_L and ΔC are resistive-load disturbances and filter-capacitor uncertainties.

Further, applying the forward Euler discretization to (3) yields the discretized dynamic voltage model

$$u_{o,k+1} = G u_{o,k} + H i_{L,k} + p_k \tag{5}$$

where $u_{o,k}$, $i_{L,k}$ and p_k represent the discretized load-bus voltage, inductor current and lumped disturbance. T_s is the sampling period and the coefficients are calculated as

$$G = 1 - \frac{T_s}{R_L C},\ H = \frac{T_s}{C},\ p_k = T_s \omega_k. \tag{6}$$

The primary control objective of this paper is to achieve desired dc-bus voltage reference tracking performance with a fast dynamic response, enhanced robustness to lumped disturbances, as well as guaranteed stability. Meanwhile, the sub-objective is to realize the current limitation for hardware over-current protection.

III. Proposed Composite Robust DQSMC in a Multi-Loop Framework

In this section, the design procedures of the proposed composite robust DQSMC in a multi-loop framework is presented, which contains two main control loops. In the outer loop, an S^{2}MDO-embedded composite robust DQSMC is designed to stabilize the dc-bus voltage with enhanced dynamics, while the inner-loop linear current control aims to realize further voltage dynamics improvement and current limitation, which is elaborated below.

A. Outer-Loop Baseline DQSMC Voltage Controller

The general design procedures of the outer-loop baseline DQSMC comprise the sliding surface design and the control law derivation.

1) Discrete Integral Sliding Surface: Taking into account the robustness during the reaching phase of the voltage, a discretized integral sliding function is defined by the load-bus voltage tracking error and its integral as follows

$$\begin{cases} s_k = \rho({u_{o,k}}^{\text{ref}} - u_{o,k}) + \lambda \sigma_k \\ \sigma_k = \sigma_{k-1} + ({u_{o,k}}^{\text{ref}} - u_{o,k}) \end{cases} \tag{7}$$

where s_k is the discretized sliding function. ${u_{o,k}}^{\text{ref}}$ is the load-bus voltage reference. σ_k is the voltage tracking error integral term, aiming at eliminating the steady-state error. ρ and λ are the positive constants to be designed.

It is worth mentioning that the integral initial value σ_0 affects the system initial trajectory. To avoid the initial approaching phase, initial error integral σ_0 in (7) is set as

$$\begin{aligned}\sigma_0 &= -\frac{\rho}{\lambda}({u_{o,0}}^{\text{ref}} - u_{o,0}) \\ &\Rightarrow s_0 = 0\end{aligned} \tag{8}$$

where ${u_{o,0}}^{\text{ref}}$ and $u_{o,0}$ are the initial voltage reference and feedback. Hence, the initial system trajectory is located on the discretized sliding surface, enabling the system to behave a total robustness against load disturbances and system-parameter uncertainties.

2) Baseline Control Law Design: To reduce implementation complexity, a discretized equivalent control law is utilized to derive the baseline DQSMC controller, i.e.,

$$s_{k+1} - s_k = 0. \tag{9}$$

In (9), s_{k+1} can be calculated using the one-step forward recursion of the sliding function in (7) as

$$s_{k+1} = \rho({u_{o,k+1}}^{\text{ref}} - u_{o,k+1}) + \lambda(\sigma_k + {u_{o,k+1}}^{\text{ref}} - u_{o,k+1}). \tag{10}$$

Since the sampling period T_s is very small, the voltage reference is considered as constant in a T_s, i.e., ${u_{o,k+1}}^{\text{ref}} = {u_{o,k}}^{\text{ref}}$. Then, the control law is introduced by substituting the voltage dynamic model (5) into (10) as

$$s_{k+1} = (\rho+\lambda)({u_{o,k}}^{\text{ref}} - G u_{o,k} - H i_{L,k} - p_k) + \lambda \sigma_k. \tag{11}$$

Further substituting (7) and (11) into (9), then, the baseline DQSMC voltage controller is obtained by

$$i_{L,k}^{\text{eq}} = (\gamma H)^{-1}[\lambda {u_{o,k}}^{\text{ref}} - (\gamma G - \rho)u_{o,k} - \gamma p_k] \tag{12}$$

where $\gamma = \rho + \lambda$, and $i_{L,k}^{\text{eq}}$ is the inductor current reference that would be fed to the inner current loop.

B. Embedded Lumped-Disturbance Estimator: S^{2}MDO

Note that the baseline control law (12) requires accurate lumped disturbance p_k, which is unknown and immeasurable practically. Hence, online estimation of p_k is inevitable for controller implementation. Typical linear observers like full-order observers, disturbance observers, and extended state observers are asymptotically convergent, which have slow dynamics and are sensitive to system uncertainties. To obtain a fast and robust lumped-disturbance estimation, an S^{2}MDO is designed in this section.

For simplicity, taking into account an auxiliary equation as

$$\dot{x} = u + d \tag{13}$$

where x, u and d represent the system state variable, control input and bounded lumped disturbance, respectively.

Follow the design procedures in [22], a S^{2}MDO can be constructed with its simplest form as

$$\begin{cases} \dot{\hat{x}} = u + \hat{d} + \alpha |x - \hat{x}|^{1/2} \operatorname{sign}(x - \hat{x}) \\ \dot{\hat{d}} = \beta \operatorname{sign}(x - \hat{x}) \end{cases} \tag{14}$$

where the notation '^' is the estimated value. α and β are the positive S^{2}MDO gains to be designed.

Accordingly, the Euler discretization implementation of (14) is formulated as

$$\begin{cases} \hat{x}_{k+1} = \hat{x}_k + T_s[u_k + \hat{d}_k + \alpha |x_k - \hat{x}_k|^{1/2} \operatorname{sign}(x_k - \hat{x}_k)] \\ \hat{d}_{k+1} = \hat{d}_k + T_s \beta \operatorname{sign}(x_k - \hat{x}_k). \end{cases} \tag{15}$$

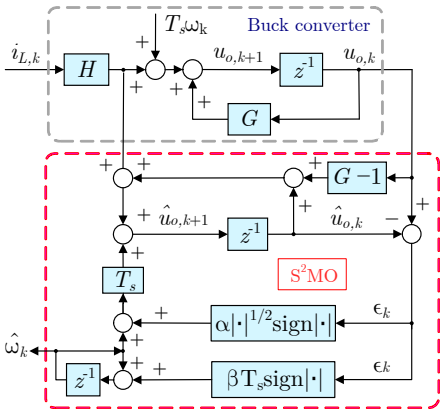

Fig. 2. Block diagram of S^{2}MDO for lumped disturbance estimation of a buck converter.

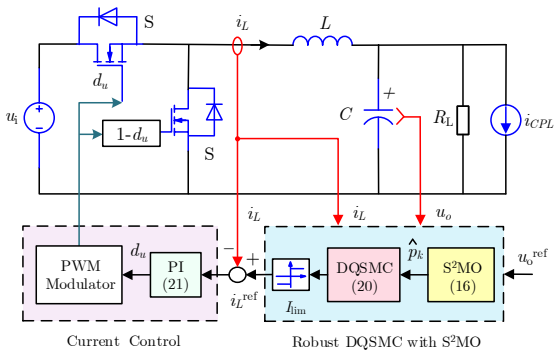

Fig. 3. Block diagram of the proposed composite robust DQSMC scheme in a multi-loop framework.

The discrete stability conditions of S^{2}MDO in (15) are discussed in [22], which indicates that a valid choice is $\alpha = 1.5L_c^{1/2}$ and $\beta = 1.1L_c$ with L_c as the only design parameter. A larger L_c can increase the convergence rate of the estimator but is also more sensitive to external noises. It is important to mention that due to the discrete-sampling effect, the ideal estimation $\hat{d}_k = d_k$ cannot be directly achieved and an estimation error would be caused.

By applying the discretized S^{2}MDO in (15) to the buck converter model in (5), the resulting S^{2}MDO for lumped-disturbance estimation of buck converter is expressed as

$$\begin{cases} \hat{u}_{o,k+1} = \hat{u}_{o,k} + T_s(-\dfrac{1}{R_L C}u_{o,k} \\ \qquad + \dfrac{1}{C}i_{L,k} + \hat{\omega}_k + \alpha|\epsilon_k|^{1/2}\,\mathrm{sign}(\epsilon_k)) \\ \hat{\omega}_{k+1} = \hat{\omega}_k + T_s\beta\,\mathrm{sign}(\epsilon_k) \end{cases} \tag{16}$$

where $\epsilon_k = u_{o,k} - \hat{u}_{o,k}$ is the voltage estimation error.

The block diagram of the S^{2}MDO for lumped-disturbance estimation of a buck converter is shown in Fig. 2.

By following *Theorem* 1 in [22], it can be easily obtained the convergent time as $T \le \sum \frac{|\tilde{u}_{o\,i}|}{(\beta - f^+)}$, where $\dot{\tilde{u}}_{o\,i}$ is the changing rate of the voltage estimation error, β is the observer gain, and f^+ is the upper bound of the lumped disturbance. It should be noted that the attractive features of the S^{2}MDO are that it not only retains strong robustness against model uncertainties, but also offers a finite-time convergence rate (i.e., faster transient estimation response) of $\hat{p}_k$, which would improve the system dynamic response.

C. Synthesis of Composite Robust Controller

Next, the estimated $\hat{p}_k = T_s\hat{\omega}_k$ in (16) is fed to the baseline DQSMC control law in (12) to replace the actual p_k for practical implementation, which serves a disturbance feed-forward compensation as

$$i_{L,k}^{\mathrm{eq}} = (\gamma H)^{-1}[\lambda {u_{o,k}}^{\mathrm{ref}} - (\gamma G - \rho)u_{o,k} - \gamma\hat{p}_k] \tag{17}$$

with the disturbance estimation error satisfying [22]

$$|\hat{p}_k - p_k| \le \kappa_p T_s^2 = \Delta_e \tag{18}$$

where $\kappa_p > 0$ and Δ_e represents the upper bound of the disturbance estimation error.

Comparing (12) and (17), it can be concluded that the equivalent control only takes effect with no disturbance-estimation error, i.e., $\hat{p}_k = p_k$. However, $\hat{p}_k$ cannot be exactly equal to p_k due to the estimation error in (18). Hence, only using (17) cannot guarantee the system states to be always maintained within the QSM. To solve this issue, a composite robust DQSMC scheme is further derived by adding an extra discontinuous switching control term, which aims to resist the lumped-disturbance estimation error. The switching control term is constructed as

$$i_{L,k}^{\mathrm{sw}} = (\gamma H)^{-1}K_{\mathrm{sw}}\mathrm{sign}(s_k) \tag{19}$$

where K_{sw} is a positive switching gain and sign (.) is the sign function.

Hence, combining (17) with (19) yields the final form of the proposed composite robust DQSMC voltage controller

$$\begin{aligned} i_{L,k}^{\mathrm{ref}} &= i_{L,k}^{\mathrm{eq}} + i_{L,k}^{\mathrm{sw}} = (\gamma H)^{-1}[\lambda {u_{o,k}}^{\mathrm{ref}} \\ &- (\gamma G - \rho)u_{o,k} - \gamma\hat{p}_k + K_{\mathrm{sw}}\mathrm{sign}(s_k)]. \end{aligned} \tag{20}$$

D. Inner-Loop Current Controller

To further improve the voltage dynamic response and realize current limitation, a discrete PI current control is retained in the inner control loop as

$$d_u = K_{pi}(i_{L,k}^{\mathrm{ref}} - i_{L,k}) + K_{ii}T_s\sum_{i=1}^{k}(i_{L,i}^{\mathrm{ref}} - i_{L,i}) \tag{21}$$

where d_u is the duty cycle. K_{pi} and K_{ii} are proportional and integral gains, while ${i_{L,k}}^{\mathrm{ref}}$ is the inner-loop reference generated from the outer-loop voltage controller (20).

Hence, a current saturation limit link I_{lim} can be simply added before the inner-loop current reference for over-current protection as shown in Fig. 3, which cannot be simply achieved by typical CSMC schemes.

Finally, the resulting duty cycle d_u is modulated to generate fixed-frequency PWM signals and applied to the buck converter.

E. Stability Analysis

1) Stability of Composite DQSMC: Note that the stability condition of CSMC is only necessary for the discretized stability [19]. Hence, it is necessary to analyze the stability of the proposed composite robust DQSMC. Since the inner-loop dynamics are usually designed much faster than the outer control loop, the inner control loop can be simplified to an unity gain; then the feedback inductor current can be considered to be equal to its reference, i.e., $i_{L,k} = i_{L,k}^{\text{ref}}$ [23]. Based on this, the closed-loop sliding-mode dynamics are obtained by substituting (20) into (11) as

$$\begin{aligned} s_{k+1} &= \rho(u_{o,k}{}^{\text{ref}} - u_{o,k}) + \gamma(\hat{p}_k - p_k) - K_{\text{sw}}\text{sign}(s_k) + \lambda\sigma_k \\ &= s_k + \gamma(\hat{p}_k - p_k) - K_{\text{sw}}\text{sign}(s_k). \end{aligned} \tag{22}$$

Considering (18) and (22), a sufficient condition that can guarantee the discrete stability of DQSMC is given as follows

$$K_{\text{sw}} > \gamma\Delta_e. \tag{23}$$

Under condition (23), the stability analysis of the proposed composite DQSMC is discussed. On the one hand, for $\forall k > 0$, if $s_k > 0$, then (22) can be rewritten as

$$\begin{aligned} s_{k+1} &= s_k + \gamma(\hat{p}_k - p_k) - K_{\text{sw}} \\ &\le s_k + \gamma\Delta_e - K_{\text{sw}} \\ &< s_k. \end{aligned} \tag{24}$$

On the other hand, if $s_k < 0$, then (22) is described as

$$\begin{aligned} s_{k+1} &= s_k + \gamma(\hat{p}_k - p_k) + K_{\text{sw}} \\ &\ge s_k - \gamma\Delta_e + K_{\text{sw}} \\ &> s_k. \end{aligned} \tag{25}$$

Hence, one can conclude from (24) and (25) that

$$|s_{k+1}| < |s_k|. \tag{26}$$

It can be deduced that (26) satisfies the necessary and sufficient condition of the existence of QSM [19]. Hence, system states using the proposed method can finally enter into the QSM, and the system is stable.

Regarding the case of inductor current (i.e., control input) saturation, note that the inductor current feedback is different from its normal-operation value due to the saturation limit, which is equivalent to a result of current sampling error. Hence, this error can be categorized as an extra disturbance and merged to (4). Based on the stability condition in (23), it can be deduced that the switching gain K_{sw} is determined by the lumped disturbance. Hence, by selecting a proper K_{sw} that satisfies (23), the stability of the closed-loop voltage controller can still be guaranteed with control-input saturation. Under this K_{sw}, the system states would gradually be driven to the sliding surface. In other words, the inductor current would undergo a de-saturation process and the closed-loop system would still be stable.

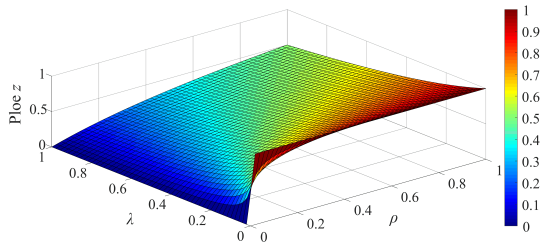

Fig. 4. Relationship between parameters ρ, λ and closed-loop pole z.

2) Robustness and Chattering Suppression: Nominal SMC and DQMSC are usually designed based on the nominal dynamic model (2) without considering the lumped-disturbance compensation [18]. Similarly, if the S^{2}MDO is not employed (i.e., setting $\hat{p}_k = 0$ in (20)), the proposed composite controller degrades into a nominal DQSMC controller. The reason why the proposed composite controller can suppress the lumped disturbance and chattering is explained below.

Assumed that the original lumped disturbance in (5) is bounded with

$$|p_k| = |\omega_k| T_s \le \Delta_p \tag{27}$$

where Δ_p is the upper bound of the lumped disturbance.

Then, by setting $\hat{p}_k = 0$ in (22), the stability condition of the nominal DQSMC is obtained by

$$K_{\text{sw}} > \gamma\Delta_p. \tag{28}$$

Comparing (18) with (27), it can be deduced that Δ_e is much smaller than Δ_p due to the small T_s. This indicates that the original large disturbance is suppressed to be a small disturbance-estimation error by the proposed composite controller. Hence, to resist the same lumped disturbance, a much smaller K_{sw} can be chosen, which inherently suppresses the chattering and improves the steady-state accuracy. In other words, using the same K_{sw}, typical DQSMC (without S^{2}MDO) would achieve worse robustness than the proposed controller. Hence, enhanced disturbance rejection ability is obtained using the proposed controller.

3) Closed-Loop Dynamics Analysis: The closed-loop dynamics are derived by substituting (20) into (5) as

$$u_{o,k+1} = \gamma^{-1}(\lambda u_{o,k}{}^{\text{ref}} + \rho u_{o,k} + QSM_k) \tag{29}$$

where $QSM_k = K_{\text{sw}}\text{sign}(s_k) - \gamma(\hat{p}_k - p_k)$ is a very small exogenous disturbance related to the QSM band, which can be neglected in the steady state.

Then, the z-domain voltage transfer function of the closed-loop system is formulated as

$$\frac{u_o(z)}{u_o{}^{\text{ref}}(z)} = \frac{\lambda}{\gamma z - \rho} \tag{30}$$

with closed-loop pole as

$$z = \frac{\rho}{\gamma} = \frac{\rho}{\rho + \lambda} = \frac{1}{1 + \frac{\lambda}{\rho}} \in (0, 1) \tag{31}$$

The relationship between parameters ρ, λ, and the pole z are shown in Fig. 4. It can be deduced from (31) that the desired control bandwidth can be obtained by using a pole-placement

TABLE I
COMPARISON BETWEEN EXISTING CSMC AND PROPOSED COMPOSITE DQSMC

Comparative items	Typical CSMC [18]	Parabolic-modulated CSMC [17]	Second-order CSMC [24]	Proposed DQSMC
Implementation mode	Digital controller	Hardware circuit	Digital controller	Digital controller
Design time domain	Continuous-time	Continuous-time	Continuous-time	Discrete-time
Control framework	Single-loop	Single-loop	Single-loop	Multi-loop
Sliding function	$s(t)=\left(\frac{d}{dt}+\alpha_1\right)x$	$s(t)=\left(\frac{d}{dt}+\alpha_1+\alpha_2\int\right)x$	$\ddot{s}(t)=a(t,x)+b(t,x)u$	$\begin{cases} s_k=\rho({u_{o,k}}^{\text{ref}}-u_{o,k})+\lambda\sigma_k \\ \sigma_k=\sigma_{k-1}+({u_{o,k}}^{\text{ref}}-u_{o,k}) \end{cases}$
Stability judgment	$\dot{V}(s)=s\dot{s}<0$	$\dot{V}(s)=s\dot{s}<0$	$\dot{V}(s)<0$	$\lvert s_{k+1}\rvert<\lvert s_k\rvert$
Discretization stability	Only necessary	Only necessary	Only necessary	Necessary & sufficient
Current limitation	No	No	No	Yes
Switching frequency	Constant	Quasi-constant	Variable	Constant
Disturbance suppression	No	No	No	Yes
Applicable load type	CPLs	Resistors	Resistors	CPLs

strategy [25]. A trade-off should be made in the selection of parameters ρ and λ. For simplicity, ρ can be fixed as 1, and λ becomes the only design parameter. A faster dynamic response is obtained when the pole is close to the origin (i.e., setting a larger λ), while stronger robustness is achieved when the pole is close to the unit circle. Since the closed-loop pole is always within the unit circle, the closed-loop system is stable.

F. Comparison with Existing CSMC Schemes

To intuitively compare the existing CSMC with the proposed method, differences between four SMC methods are listed in Table I. From Table I, it can be intuitively seen the differences between proposed DQSMC and existing CSMC schemes. First, parabolic-modulated CSMC implements the SMC algorism using a hardware circuit while the other three SMC methods are based on a digital controller. Then, the design domain, control structure, and principles (i.e., sliding function and stability criterion) are different. The proposed method is a multi-loop discrete-time SMC scheme, which is more direct for digital implementations and has guaranteed discrete stability. However, the other three methods are single-loop continuous-time SMC, which may induce unexpected chattering and stability issues in digital implementations. Compared to the three CSMC methods, the proposed method embeds an S^2MO, thus it is more robust to disturbances. Moreover, the proposed method is deployed in a multi-loop framework, which is easy to handle the inductor-current limitation. It is also worth mentioning that CSMC methods in [17] and [24] are only designed for resistive loads instead of CPLs; and second-order SMC in [24] has a variable switching frequency, which may degrade the steady-state output accuracy.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Comparative simulations in MATLAB/Simulink of the proposed composite controller with conventional cascaded PI controller are investigated. The simulation parameters of system and controllers are listed in Table II and Table III, which guarantee that the inner-loop bandwidth is much larger than

TABLE II
PARAMETERS OF BUCK CONVERTER SYSTEM

Source-bus voltage reference	u_i = 120 V
Load-bus voltage reference	u_o^{ref} = 48 V
Nominal inductance filter	L = 1.3 mH
Nominal capacitance	C = 470 μF
Sampling frequency	f_s = 20 kHz
Maximum current limit	I_{lim} = 12 A

TABLE III
PARAMETERS OF TWO CONTROLLERS

Robust DQSMC		PI control	
Parameter	Value	Parameter	Value
ρ	1	K_{pv}	1
λ	0.1	K_{iv}	250
L_c	5×10^5	K_{pi}	0.2
K_{sw}	0.2	K_{ii}	500

that of the outer control loop [13]. In addition, the conventional outer-loop discretized PI voltage controller is expressed as

$$i_{L,k}^{\text{ref}}=K_{pv}({u_{o,k}}^{\text{ref}}-u_{o,k})+K_{iv}T_s\sum_{i=1}^{k}({u_{o,i}}^{\text{ref}}-u_{o,i}) \quad (32)$$

where K_{pv} and K_{iv} are the proportional and integral gains.

A. Parameter-Tuning Guidelines

From Table III, it can be seen that three key parameters λ, L_c and K_w in the proposed controller need to be appropriately selected to assure the desired control performance. First, the dynamic start-up response of the load-bus voltage with different λ is depicted in Fig. 5 (a). As is shown, a larger λ can result in faster dynamic response. It should also be mentioned that a too-large λ may induce an overshoot. Hence, a tradeoff should be made between the voltage-tracking dynamic response and the overshoot, which is consistent with the theoretical analysis in Section III-E. Then, the dynamic convergent response of S^2MDO with different L_c is shown

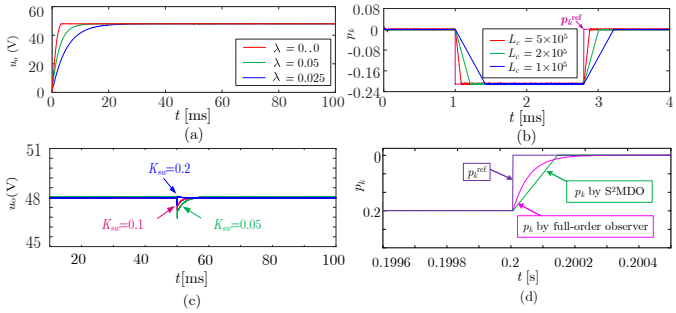

Fig. 5. Simulated dynamic response of load-bus voltage and disturbance estimation with different control parameters. (a) Load-bus voltage start-up response with different λ. (b) S^{2}MDO dynamic convergent response with different L_c. (c) Load-bus voltage dynamic response with different K_{sw}. (d) Comparison of disturbance-estimation dynamics using S^{2}MDO and conventional full-order disturbance observer.

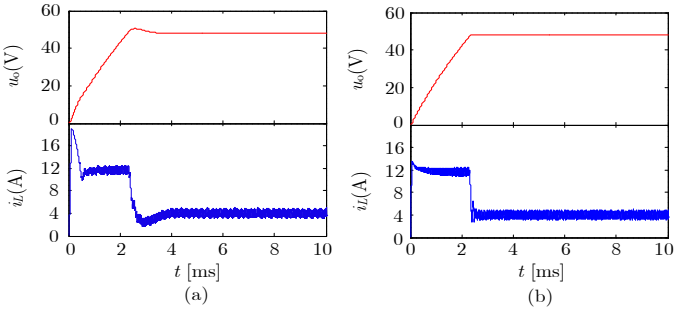

Fig. 6. Simulation comparison of system start-up response. (a) Cascaded PI controller. (b) Proposed controller.

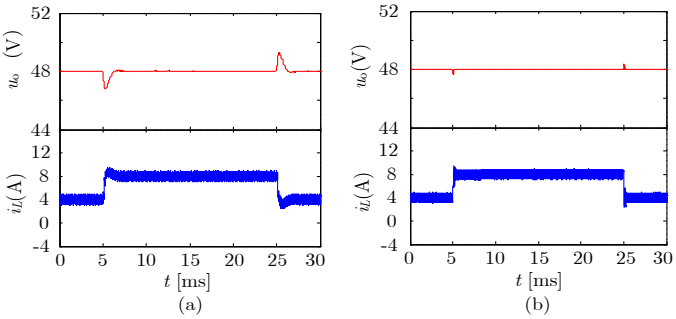

Fig. 7. Simulation comparison of system dynamic response with step CPL disturbances. (a) Cascaded PI controller. (b) Proposed controller.

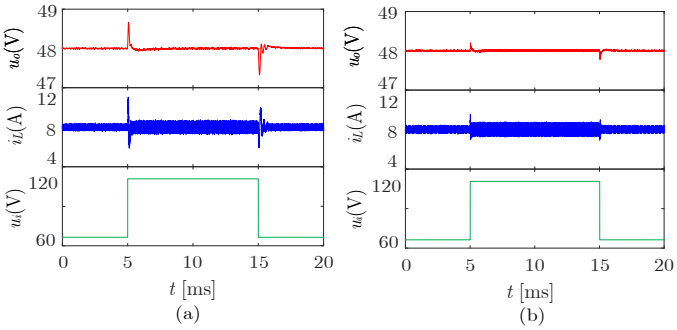

Fig. 8. Simulation comparison of system dynamic response with source-bus voltage disturbances. (a) Cascaded PI controller. (b) Proposed controller.

in Fig. 5 (b) with a step CPL. Similarly, a larger L_c can increase the convergence rate of the disturbance estimation, while S^{2}MDO is also more sensitive to the external noises. Still, a tradeoff should be made between the dynamic response and anti-noise performance. Fig. 5 (c) shows the dynamic response of the load-bus voltage with different K_w under a step-change CPL (192 W $\rightarrow$ 384 W) at 50 ms. The results reveal that increasing K_{sw} would lead to a better voltage-tracking dynamic response with lower voltage deviation and restoration time, i.e., stronger robustness to CPL variations. It should be noted that since K_{sw} is the switching gain, a too-large K_{sw} would somewhat increase the switching ripple. Hence, K_{sw} can be chosen based on the expected dynamics. Fig. 5 (d) compares the disturbance-estimation dynamics using using S^{2}MDO and conventional full-order observer in [26]. It can be easily observed that conventional full-order disturbance observer has an asymptotic convergent rate. In contrast, the proposed S^{2}MDO has a finite-time convergent rate, of which disturbance estimation dynamics are faster.

B. Simulation Comparison

Fig. 6 shows the simulation comparison of the start-up response of the load-bus voltage u_o using the conventional cascaded PI controller and the proposed controller. As is shown, the voltage start-up response using the proposed controller has a smaller rising time with no explicit overshoot (i.e., faster stabilization) than the cascaded PI. Besides, due to the inner current loop control, both controllers can limit the inductor current to 12 A. Nonetheless, the proposed controller has a much smaller inductor-current overshoot in the transient process; thus, a better current-limiting capability is achieved.

Fig. 7 depicts the dynamic response of load-bus voltage with a step CPL disturbance (192 W $\rightarrow$ 384 W $\rightarrow$ 192 W) using cascaded PI controller and the proposed controller. It reflects that the load-bus voltage is faster stabilized with lower voltage deviation and restoration time using proposed controller, which achieves stronger robustness against load disturbances.

Fig. 8 depicts the dynamic system response with a source-bus voltage step change (60 V $\rightarrow$ 120 V $\rightarrow$ 60 V). It can be observed that compared to cascaded PI control, much smaller fluctuations of both load-bus voltage and inductor current are obtained by the proposed method. Hence, the proposed method exhibits enhanced robustness and stability in reference-voltage tracking response under source-bus voltage variations.

Fig. 9 shows a comparison of system and sliding function dynamics using the nominal DQSMC (without S^{2}MDO) and proposed composite controller. As is shown in Fig. 9 (a), the load-bus voltage cannot be restored to its reference with a large voltage deviation, and S_k cannot be maintained within QSM using nominal DQSMC. In sharp contrast, in Fig. 9 (b), the sliding surface S_k can fast converge within the QSM under CPL variations. Hence, the proposed method offers enhanced voltage-tracking accuracy and guarantees the system stability and robustness under large load disturbances. Fig. 9 (c) depicts the chattering suppression capability of the proposed composite controller compared to nominal DQSMC. It can be seen that for nominal DQSMC, the switching gain K_{sw} should be selected much larger than that of the proposed method to guar-

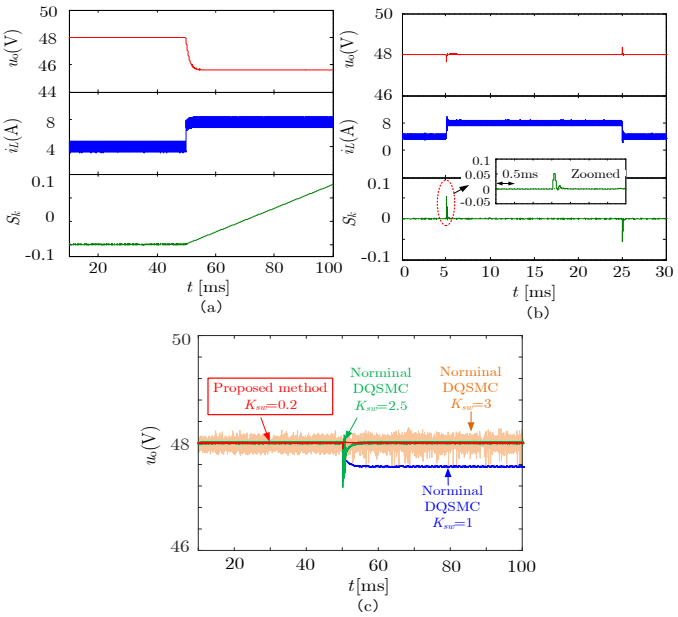

Fig. 9. Simulation comparison of sliding function dynamics and chattering with CPL disturbances. (a) Sliding-function dynamics using nominal DQSMC. (b) Sliding-function dynamics using proposed controller. (c) Chattering suppression comparison between nominal DQSMC and proposed controller.

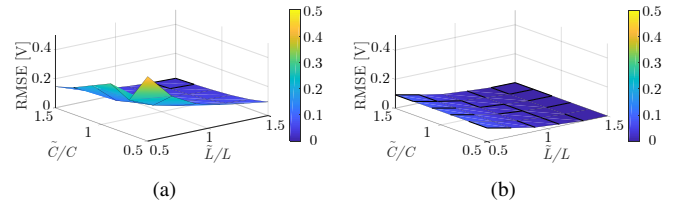

Fig. 10. Simulation comparison of load-bus voltage tracking RMSE with model uncertainties. (a) Cascaded PI controller. (b) Proposed controller.

antee system stability under the same load disturbance. When $K_{sw} = 1$, nominal DQSMC cannot guarantee the robustness, thus leading to a voltage deviation. Keep increasing K_{sw} to 2.5, the robustness of nominal DQSMC becomes stronger but still cannot obtain the same robustness as the proposed method with $K_{sw} = 0.2$. When $K_{sw} = 3$, the robustness using nominal DQSMC is further enhanced while a large chattering is induced. Hence, to obtain similar robustness, the proposed method can significantly decrease K_{sw} due to the embedding of S^{2}MDO. As a result, the chattering is inherently suppressed using the proposed method compared to nominal DQSMC.

To verify the robustness to model uncertainties using the proposed method, simulation comparison of load-bus voltage tracking root-mean-square error (RMSE) under system-parameter uncertainties $\tilde{C}$ and $\tilde{L}$ (i.e., changing $\pm 50\%$ of nominal C and L) using two methods are shown in Fig. 10. The results reflect that under a wide range of parameter uncertainties, the proposed method can achieve better voltage-tracking accuracy and robustness over cascaded PI control.

C. Experimental Comparison

Experiments are also carried out to validate the superiority of the proposed composite controller. Fig. 11 depicts the block

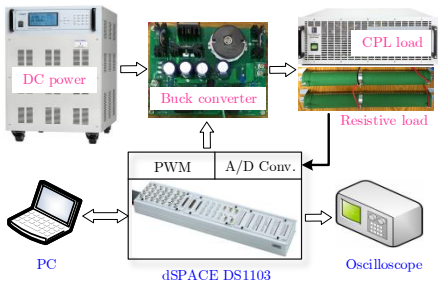

Fig. 11. Experimental platform for validating the proposed method.

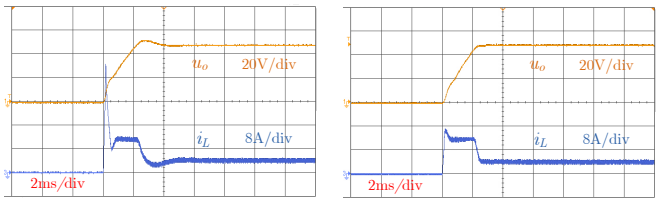

Fig. 12. Experimental results of system start-up response (u_o : 0 V $\rightarrow$ 48 V with CPL power 192 W). (a) Cascaded PI control. (b) Proposed controller.

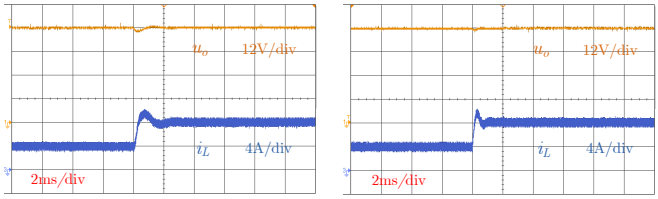

Fig. 13. Experimental results of system dynamic response with a CPL step injection (192 W $\rightarrow$ 384 W). (a) Cascaded PI control. (b) Proposed controller.

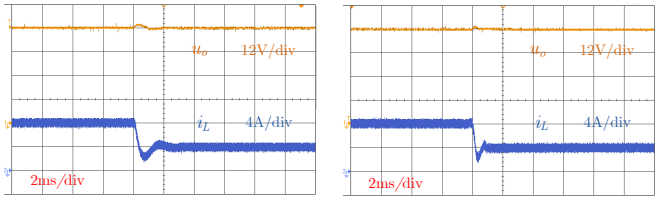

Fig. 14. Experimental results of system dynamic response with a CPL step remove (384 W $\rightarrow$ 192 W). (a) Cascaded PI control. (b) Proposed controller.

diagram of the experimental platform, which comprises a DC power supply, DC-DC buck converter, resistive loads, and CPLs using the parameters in Table II. All control algorithms are executed in dSPACE DS1103 with the controller parameters listed in Table III.

Fig. 12 illustrates the experimental comparison of load-bus voltage start-up response with cascaded PI control and the proposed controller, where the load-bus voltage u_o and the inductor current i_L are given. It reveals that the voltage start-up response using the proposed controller has a lower rising time without explicit overshoot, resulting in a faster stabilization of the system. Moreover, i_L using the proposed

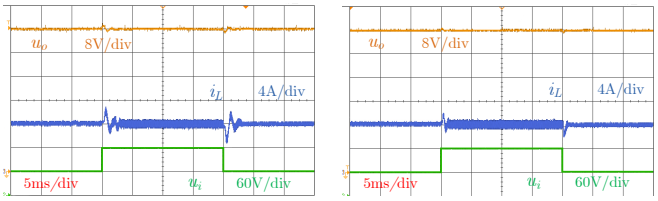

Fig. 15. Experimental results of system performance with a source-bus voltage step change. (a) Cascaded PI control. (b) Proposed controller.

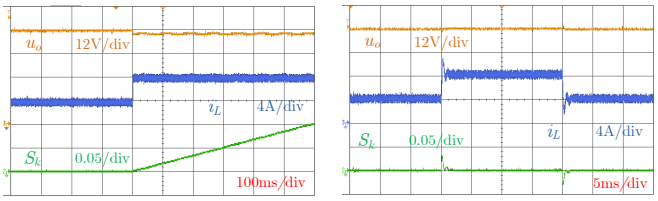

Fig. 16. Experimental results of system and sliding function response with a CPL step change. (a) Nominal DQSMC. (b) Proposed controller.

controller can be limited to the preset $I_{\text{lim}} = 12$ A with a much smaller overshoot. Hence, the proposed controller has a faster and smoother start-up dynamic performance than cascaded PI control, which is consistent with the simulation results.

Fig. 13 and Fig. 14 illustrate the dynamic system response with a step injection (192 W $\rightarrow$ 384 W) and remove (384 W $\rightarrow$ 192 W) of a CPL using cascaded PI control and the proposed method. As is observed, the load-bus voltage deviation and settling time using the proposed controller is much smaller than that of the cascaded PI control. Hence, the proposed method has a much faster dynamic voltage-tracking response with enhanced robustness than cascaded PI control.

Fig. 15 shows the transient system response with a source-bus voltage step change (60 V $\rightarrow$ 120 V $\rightarrow$ 60 V). It can be seen that the load-bus voltage can be quickly stabilized with a better dynamic voltage restoration performance (smaller voltage deviation and restoration time) using the proposed method. Hence, the proposed method manifests stronger robustness to source-bus voltage disturbances over cascaded PI control.

Fig. 16 depicts the system and sliding-function dynamic response using nominal DQSMC and the proposed controller with the same K_{sw}, where the load-bus voltage u_o, the inductor current i_L, and the sliding function S_k are shown. The nominal DQSMC (without S^{2}MDO) in Fig. 16 (a) cannot restore the load-bus voltage to its reference, and cannot drive S_k back to QSM under a step CPL disturbance. In contrast, Fig. 16 (b) shows that the proposed method can drive S_k to fast converge and maintain within the QSM. In other words, to obtain the same disturbance rejection, nominal DQSMC requires a much larger K_{sw} than the proposed method, doubtlessly inducing a larger chattering. Hence, enhanced disturbance rejection, inherent chattering suppression, as well as assured stability are achieved by the proposed method.

V. Conclusion

This paper presents a composite robust discretized DQSMC in a multi-loop framework for stabilizing buck converters with CPLs. An S^{2}MDO-embedded robust DQSMC voltage controller is proposed in the outer loop, achieving a fast dynamic response, enhanced robustness to lumped disturbance, as well as chattering suppression. Meanwhile, a PI-based current controller is retained in the inner loop for current limiting. The closed-loop dynamics and stability analysis of the proposed composite controller are given, guaranteeing the large-signal stability. Simulation and experimental results verify the superiority of the proposed approach.

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