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A study on the formation of thin-film CZTS solar cells via the aprotic molecular ink approach

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The DMSO aprotic molecular ink route has recently proven a competitive approach for synthesis of the sulfo-selenide $Cu_2ZnSn(S,Se)_4$ with power conversion efficiencies exceeding 10% [Xin2014, Haass2015, Clark2017]. Meanwhile, limited effort has been devoted to synthesis of the pure-sulfide Cu_2ZnSnS_4 (CZTS) from the solvent DMSO, even though the sulfide kesterite and its alloys have more favorable band gaps for advanced tandem concepts. In this work, CZTS solar cells with an efficiency of 4.65% were synthesized under ambient conditions. This was achieved without an anti-reflective coating, any cation incorporation, or regulated alkali doping.

We map out the process from ink to film to understand the mechanism of formation. Several things happen from once you mix your salts until the final film has formed. We review processes such as complex formation, the thermal behavior of the ink, and how the film dries and crystallizes.

For formulating the ink, we investigate the optimal sulfur-to-metal ratio in the ink by Raman spectroscopy. Furthermore, ICP-OES is used to evaluate the reproducibility of the composition of the ink, and whether it is affected by filtering. The thermal behavior of the ink is analyzed and we find that more than 90% of the mixture has evaporated at 250°C. Furthermore, mass spectrometry reveals that most of the complexes have thermally decomposed at this temperature, while chlorine and sulfoxide species are continually released until 500°C.

For thin-film deposition, spin-coating is used, where a standard deposition routine includes repeated steps of (1) spin-coating, (2) pre-annealing on a hot plate, and (3) cooling. Here, we study different thermal exposure during pre-annealing ranging from 10 s at 250°C to 30 s at 450°C. The investigation resulted in the following observations: Optical microscopy revealed a so-called “worm-like pattern” in the spin-coating films at low thermal exposure, which causes micro-inhomogeneities in film morphology. This pattern is seen to disappear at higher temperatures. Nonetheless, the best devices were fabricated at a lower thermal exposure, because the short-circuit current (J_{SC}) drops as temperature is increased. The reason could be found in the film structure: A lower thermal exposure during pre-annealing results in larger grains and a thicker MoS_2 layer at the CZTS/Mo interface. On the other hand, devices completed at higher pre-annealing temperatures display incomplete sulfurizations with smaller grains and the existence of a fine-grain layer at the back interface.

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