DTU Library

## Advances in Resonant Power Conversion for Offline Converter Applications

## Ammar, Ahmed Morsi

Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

Link back to DTU Orbit

Citation (APA):
Ammar, A. M. (2020). Advances in Resonant Power Conversion for Offline Converter Applications. Technical University of Denmark.

[^0]Ahmed Morsi Ammar

## Advances in Resonant Power Conversion for Offline Converter Applications



PhD Dissertation
DTU Electrical Engineering
May 2020

# Advances in Resonant Power Conversion for Offline Converter Applications 

Ph.D. Thesis

By
Ahmed Morsi Ammar

Supervised By
Arnold Knott,
DTU Electrical Engineering

| Copyright: | Reproduction of this publication in whole or in part must include the <br> customary bibliographic citation, including author attribution, thesis <br> title, etc. |
| :--- | :--- |
| Edition: | First |
| Cover photo: | Wafa Said Mosleh |
| Published by: | DTU Electrical Engineering, Electronics, Elektrovej, Building 325, <br> Kongens Lyngby, Denmark <br> www.ele.elektro.dtu.dk |

DTU Electrical Engineering Electronics

# Advances in Resonant Power Conversion for Offline Converter Applications 

Ahmed Morsi Ammar<br>Ph.D. Thesis

May 31 ${ }^{\text {st }}, 2020$

If you want to find the secrets of the universe, think in terms of energy, frequency, and vibration

- Nikola Tesla


## Preface and Acknowledgement

This Ph.D. thesis was prepared at the Department of Electrical Engineering at the Technical University of Denmark in fulfillment of the requirements for acquiring a Doctor of Philosophy degree. The research was conducted between June 2017 and May 2020, as part of the European Union's Horizon 2020 project "LEDLUM - Tiny Light Engine for Large Scale LED Lighting", with project number 731466. During the project, a three-month external research stay was conducted at the Department of Engineering Science, University of Oxford.

Over the past three years, a number of people have been involved in conducting this work and achieving the results presented across this thesis. I would like to extend my appreciation and gratitude to everyone who helped complete this work, both colleagues and friends.

I would like to thank my supervisor, Arnold Knott, for giving me the opportunity to work on this project, and his consistent support and keenness on "clearing the clutter" out of the way for me to focus on my research.

A very special gratitude goes to my colleague and friend, Yasser Nour, for the technical guidance and brainstorming many of the ideas presented throughout this work.

Special thanks to my colleagues Frederik Spliid, Nikolai Dahl, Jens Christian Hertel, and Christian Lumby, all of whom helped with the accomplishment of many of the pieces of work presented in this thesis.

My appreciation extends to all the people in the Electronics Group at DTU Electrical Engineering for making it one of the best environments I have worked in. Thanks to my manager, Michael Andersen, for the professional management in addition to the technical support and guidance on many parts of this thesis work. To Henriette Wolff, for the help with settling in Denmark and taking care of so many things that would have otherwise taken quite some of the time spent on this research. To Dorte Svejstrup, Allan Jørgensen, Hans-Christian Andersen, and Maria del Carmen Sandoval for the back-up with many administrative and technical duties. I appreciate it all.

To my colleagues Pere Muntal, Yudi Xiao, Kevin Manez, and Maria del Carmen Mira Albert. Thanks for the great times.

Many thanks to Dan Rogers, Kawsar Ali, and the rest of the Power Electronics Group at the University of Oxford, for facilitating my research visit and the great collaboration that resulted in some nice results in a relatively short time.

My biggest gratitude goes to my family. My mother, father and brother for being there for me all my life. To my fiancée, Wafa, for believing in me and supporting me unconditionally. This work I dedicate to all of you. I am truly blessed with your existence in my life.

## Abstract

Switch-mode power supplies (SMPS) have long served as the driving force that boosted technological innovation and human advancement. As the technologies behind different industrial electronics keep evolving, with the aim for improved performance, reliability and portability, additional requirements are continuously placed on power supply technologies to process more power in less volume.

Hard-switched pulse-width-modulated (PWM) converters have been the primary candidate for the different power supply conversion stages. They can provide high power quality and efficiency with simple control. However, they typically operate at low frequencies, in the range of few hundred kHz, in order to limit the switching losses, which results in large sizes for the passive components needed to store and process the energy transferred to the load every switching cycle. On the other hand, high-frequency designs ( 1 MHz and above) have less efficiency and may incorporate a heatsink for thermal management, which counteracts the gain in power density.

Accordingly, soft-switching resonant converters have been receiving increased attention in recent years. Thanks to their zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) characteristics, they incur substantially lower switching losses compared to their PWM counterparts. That makes them a primary candidate for achieving high efficiencies at high frequencies, resulting in reduced sizes for the passive components and, therefore, higher power densities. In addition, high-frequency operation offers higher loop-gain bandwidths and faster transient responses. This has led to the investigation of their adoption into different applications conventionally dominated by PWM converters, one of which is the grid-powered offline converters. This thesis presents advances in the design and implementation of resonant converters for offline converter applications, and introduces several topologies and techniques that allow for the design of high-frequency designs with high efficiency. Among the main research contributions of this thesis are the following:

With respect to the converter power stage, the thesis investigates resonant front-end AC-DC converters with inherent power factor correction (PFC) capability to eliminate the current regulation loop and simplify control. A 1-MHz $50-\mathrm{W}$ charge-pump-based class-DE seriesresonant converter is presented, achieving an inherent power factor of 0.99 , a total harmonic distortion (THD) of $8.6 \%$ and an efficiency of up to $88 \%$. Several solutions are presented for the front-end DC-DC stage. A 1-MHz 65-W LLC converter is designed and implemented, achieving up to $96 \%$ efficiency with inherent load regulation capability. The power stage architecture is studied, and a converter structure integrating the two stages in a 1.5-stage structure is proposed, where a prototype design for LED driver applications achieves an output power of 42 W with power density of $2 \mathrm{~W} / \mathrm{cm}^{3}$, power factor of 0.99 , THD of $6 \%$, and a peak efficiency of $90 \%$.

With respect to high-frequency modeling and control challenges, this thesis introduces an improved linear model for high-frequency resonant converters. Compared to prior art, the model incorporates the converter parasitics and reduces the DC-gain error by more than 7 dB ,


#### Abstract

with more accurate dynamics. An analysis of the different switching loss modes in class-DE resonant converters with frequency control and fixed dead time is conducted, and a feasible operating region for a given upper-loss bound is defined.

Finally, a study of the figures of merit of the best-in-class switching devices and magnetic materials for high-frequency offline converters is presented, with an investigation of GaN devices reverse conduction characteristics and their corresponding losses in the different implementations.

Through the application of the research described in this work, high-power density resonant converters with frequencies in the range of $1-2 \mathrm{MHz}$ can be implemented with robust control and high power factor and efficiency.


## Resumé

Switch-mode strømforsyninger (SMPS) har længe fungeret som en drivende kraft bag teknologisk innovation og menneskelig udvikling. Da teknologierne bag forskellig industriel elektronik er under forsat udvikling, med mål om forbedret ydelse, pålidelighed og bærbarhed, stilles der løbende nye krav til strømforsyningsteknologier om behandling af større effekt i mindre volumen.

Hård-skiftende omformere med pulsbreddemodulation (PWM) har hidtil været den primære kandidat til de forskellige effekt-omformningstrin. De kan give høj effektfaktor og effektivitet med enkel kontrol. Imidlertid fungerer de typisk ved lave frekvenser i området omkring få hundrede kHz for at begrænse skiftetabene, hvilket resulterer i store størrelser for de passive komponenter, der er nødvendige for at lagre og behandle den energi, der hver skiftecyklus overføres til belastningen. På den anden side har højfrekvente designs ( 1 MHz og derover) lavere effektivitet og kræver ofte køleplader for at begrænse temperaturen, hvilket modvirker gevinsten i effekttæthed.

Af disse årsager har blød-skiftende resonansomformere fået meget opmærksomhed i de senere år. Takket være deres nulspændingsskift (ZVS) og/eller nulstrømsskift (ZCS) har de betydeligt lavere skiftetab sammenlignet med deres PWM-modparter. Dette gør dem til oplagte kandidater til at opnå høj effektivitet ved høje frekvenser, hvilket muliggør mindskede størrelser af de passive komponenter og dermed højere effekttætheder. Derudover tilbyder højfrekvent drift højere båndbredde til sløjfeforstærkning og hurtigere transientresponser. Dette har ført til undersøgelsen af deres brug I forskellige applikationer, der traditionelt har været domineret af PWM-omformere, hvoraf et eksempel er net-forsynede offlineomformere. Denne afhandling præsenterer fremskridt indenfor design og implementering af resonansomformere til offline-omformerapplikationer og introducerer flere topologier og teknikker der muliggør design af højfrekvente omformere med høj effektivitet. Bland de vigtigste forskningsbidrag i denne afhandling er følgende:

Med hensyn til omformerens effekttrin undersøger denne afhandling resonante front-end ACDC omformere med iboende evne for effektfaktorkorrektion (PFC), der eliminerer behovet for en strømreguleringssløjfe og forenkler reguleringen. En 1-MHz 50-W ladningspumpe-baseret klasse DE serie-resonansomformer præsenteres og opnår en effektfaktor på 0.99, en total harmonisk forvrængning (THD) på $8.6 \%$, og en effektivitet på op til $88 \%$. Flere løsninger for front-end DC-DC trinnet præsenteres. En 1-MHz 65-W LLC-omformer designes og implementeres og opnår en effektivitet på op til $96 \%$ med iboende belastningsreguleringsevne. Arkitekturer for effekttrin udforskes, og en omformer der integrerer de to trin i en 1,5-trins struktur fremvises, hvor en prototype til LEDdriverapplikationer opnår en udgangseffekt på 50 W med en effekttæthed på $2 \mathrm{~W} / \mathrm{cm}^{3}$ og en effektivitet på op til 90 \%.

Med hensyn til udfordringer ved højfrekvent modellering og regulering præsenterer denne afhandling en forbedret lineær model for højfrekvente resonansomformere. Sammenlignet med kendte teknologier inkorporerer denne model omformerens parasitiske komponenter og
reducerer DC-forstærkningsfejlen med mere end 7 dB med en mere nøjagtig dynamik. En analyse af de forskellige typer skiftetab i klasse-DE resonansomformere med frekvensstyring og fast dødtid udføres, og der defineres et realiserbart driftsområde for en givent $\varnothing \mathrm{vre}$ tabsgrænse.

Endeligt præsenteres en undersøgelse af nøgleegenskaber for de bedste tilgængelige skifteenheder og magnetiske materialer for højfrekvente offline-omformere med en unders $\varnothing$ gelse af GaN-komponenters omvendte ledningsegenskaber og deres tilsvarende tab i forskellige implementeringer.

Gennem anvendelsen af den forskning, der beskrives i denne afhandling, kan resonansomformere med høj effekttæthed implementeres med skiftefrekvenser i området 12 MHz med robust regulering og høj effektfaktor og effektivitet.

## Contents

PREFACE AND ACKNOWLEDGEMENT .....
ABSTRACT ..... III
RESUMÉ ..... V
CONTENTS ..... VII
LIST OF FIGURES ..... XI
LIST OF TABLES ..... XIII
LIST OF ABBREVIATIONS ..... XV

1. INTRODUCTION ..... 1
1.1 Background and Motivation ..... 1
1.1.1 Offline Converters ..... 2
1.2 Thesis Scope ..... 5
1.3 Thesis Structure ..... 5
2. STATE OF THE ART ..... 9
2.1 Overview of Resonant Converters ..... 9
2.1.1 Topologies ..... 9
2.1.2 Synchronous Rectification ..... 11
2.1.3 VHF Resonant Converters ..... 11
2.1.4 Stacking and Input-Output Arrangement ..... 11
2.1.5 Modeling ..... 12
2.1.6 Control ..... 13
2.2 State-of-the-Art Front-End Converters ..... 13
2.2.1 PFC Converters ..... 13
2.2.2 DC-DC Converters ..... 14
3. RESONANT PFC CONVERTERS ..... 15
3.1 Class-E-Based Resonant PFC Converters ..... 16
3.1.1 Class-E Converter for US mains with Inherent PFC Capability ..... 16
3.1.2 Stacked Class-E VHF Converter for European Mains PFC ..... 18
3.2 Class-DE-Based Resonant PFC Converters ..... 18
3.2.1 Charge-Pump-Based PFC Converters ..... 18
3.2.2 Frequency-Modulated Class-DE PFC Converter ..... 27
3.3 Summary ..... 28
4. RESONANT DC-DC CONVERTERS ..... 31
4.1 Class-DE-Based DC-DC Converters ..... 31
4.2 Class-DE SR Converter ..... 34
4.3 LLC Resonant Converter. ..... 36
4.4 CLLC Resonant Converter ..... 38
4.5 Summary ..... 39
5. POWER STAGE ARCHITECTURE ..... 41
5.1 Converter Stages Integration ..... 41
5.1.1 Single-stage offline converter ..... 41
5.1.2 1.5-stage offline converter ..... 42
5.1.3 Two-stage offline converter .....  .43
5.2 Universal Compatibility ..... 44
5.2.1 Switched-Capacitor Front-end Scaling Converter ..... 44
5.3 Converter Input-Output Rearrangement and Stacking ..... 45
5.4 Variable DC-Bus Voltage ..... 47
5.5 Summary ..... 49
6. DEVICES ..... 51
6.1 Semiconductor Devices ..... 51
6.1.1 Comparison of Commercial Devices ..... 51
6.1.2 Layout Considerations ..... 51
6.1.3 GaN Reverse-Conduction Characteristics ..... 53
6.2 Magnetic devices ..... 54
6.3 Summary ..... 54
7. MODELING AND CONTROL ..... 57
7.1 Modeling ..... 57
7.1.1 High-Frequency Class-DE Converter Model ..... 57
7.2 Control ..... 58
7.2.1 Frequency Control ..... 58
7.2.2 Burst-mode Control ..... 60
7.2.3 Time-Based Control ..... 61
7.3 Summary ..... 63
8. CONCLUSION AND FUTURE WORK ..... 65
8.1 Thesis Summary ..... 65
8.2 Conclusion. ..... 66
8.3 Future Work ..... 67
LIST OF PUBLICATIONS ..... 69
BIBLIOGRAPHY ..... 71
APPENDIX A ..... 83
Prototyping Setup ..... 83
Lab Setup ..... 84
APPENDIX [P1] ..... 87
APPENDIX [P2] ..... 131
APPENDIX [J1] ..... 161
APPENDIX [J2] ..... 175
APPENDIX [J3] ..... 187
APPENDIX [J4] ..... 203
APPENDIX [J5] ..... 223
APPENDIX [J6] ..... 243
APPENDIX [J7] ..... 265
APPENDIX [J8] ..... 271
APPENDIX [C1] ..... 281
APPENDIX [C2] ..... 283
APPENDIX [C3] ..... 285
APPENDIX [C4] ..... 291
APPENDIX [C5] ..... 297
APPENDIX [C6] ..... 305

## List of Figures

Figure 1.1: Conventional offline converter structure ..... 2
Figure 1.2: Peak-detection rectifier ..... 3
Figure 1.3: Thesis structure ..... 6
Figure 2.1: Resonant converter structure ..... 9
Figure 2.2: Class-E Converter ..... 10
Figure 2.3: Class-DE SR Converter ..... 10
Figure 3.1: Classification of presented resonant PFC converter solutions ..... 15
Figure 3.2: Proposed class-E inverter/class-D rectifier converter for PFC applications [J5] ..... 16
Figure 3.3: Class-E PFC Converter experimental waveforms at full-load [J5] ..... 17
Figure 3.5: Charge-pump circuit operation across half a line cycle ..... 19
Figure 3.4: Charge-pump PFC converter equivalent circuit ..... 19
Figure 3.6: Charge-pump PFC converter reported in [J3] ..... 21
Figure 3.7: Charge-pump-based PFC converter design flow chart ..... 22
Figure 3.8: Implemented prototype waveforms at full-load operation [J3] ..... 23
Figure 3.9: Charge-pump PFC converter in [J4] ..... 24
Figure 3.10: Line-frequency waveforms [J4] ..... 25
Figure 3.11: 1.5-stage offline converter [J6]. ..... 25
Figure 3.12: Prototype waveforms at full-load operation [J6] ..... 26
Figure 3.13: Extrapolated input current waveforms across the line cycle [J2] ..... 28
Figure 4.1: Class-DE stage alternatives [P1] ..... 31
Figure 4.2: DC-DC stage design flow chart. ..... 33
Figure 4.3: Switching-frequency waveforms [C1] ..... 34
Figure 4.4: PoE Class-DE SR Converter Experimental Results. ..... 35
Figure 4.6: Resonant tank gain with $k=5$ (top) and $k=10$ (bottom) for the same loads ..... 37
Figure 4.5: LLC converter switching-frequency waveforms ..... 38
Figure 4.7: CLLC Converter Schematic [C6] ..... 38
Figure 4.8: Experimental waveforms for nominal operational point ..... 39
Figure 5.1: Single-stage offline converter structure [P1] ..... 41
Figure 5.2: 1.5-stage offline converter structure [J6] ..... 42
Figure 5.3: Two-stage offline converter structure. ..... 43
Figure 5.4: A 2:1 switched-capacitor converter [J7]. ..... 45
Figure 5.5: Proposed universal-mains architecture [J7]. ..... 45
Figure 5.6: Experimental waveforms for the SC front-end Boost PFC converter [J7] ..... 45
Figure 5.7: Stacked architecture with input-output rearrangement of converters [C2] ..... 46
Figure 5.8: Simulated line-frequency waveforms for the stacked architecture in [C2] ..... 46
Figure 5.9: Comparison between fixed and variable DC-bus voltage architectures ..... 48
Figure 6.1: Comparison of best-in-class switches FoMs [J3] ..... 52
Figure 6.2: Measured reverse conduction characteristics for the GS66502B (left) andGS66508T (right) devices.53
Figure 6.3: Core power-loss density (Pv) vs. magnetic flux density (B) for different magnetic materials at 1 MHz [J3] ..... 54
Figure 7.1: Measured and calculated frequency response (left) and step response (right) of the proposed model vs. prior art [J1]. ..... 58
Figure 7.2: Control-loop responses of the prototype with controllers based on the proposed model and prior art [J1]. ..... 58
Figure 7.3: The regions of operation and their respective switching waveforms [J8] ..... 60
Figure 7.4: Time-based average current mode controller for a PFC boost converter [C5]. ..... 62
Figure 7.5: Line-cycle waveforms from the time-based control model [133]. ..... 62
Figure 8.1: Several implemented prototypes. ..... 65
Figure A.0.1: Modular resonant converter test platform. ..... 83
Figure A.2: Lab Setup. ..... 84

## List of Tables

Table 3.2: Reported PWM PFC converters for low power applications ..... 29
Table 3.1: Comparison between proposed resonant PFC converters ..... 29
Table 4.1: Comparison between class-D switch and rectifier network configurations ..... 32
Table 4.2: Comparison between proposed dc-dc converters ..... 39
Table 5.1: Comparison of DC-DC stage primary-side devices with the same current rating. ..... 49
Table 6.1: Best-in-class devices for low-mid power offline converters. ..... 52

## List of Abbreviations

| CC | Constant Current |
| :---: | :---: |
| CP | Constant Power |
| CT | Center Tapped |
| CV | Constant Voltage |
| EMI | Electromagnetic Interference |
| EV | Electric Vehicle |
| FB | Full Bridge |
| FHA | First Harmonic Approximation |
| FoM | Figure of Merit |
| G2V | Grid to Vehicle |
| GaN | Gallium Nitride |
| HB | Half Bridge |
| HW | Half Wave |
| IT | Information Technology |
| LED | Light-Emitting Diode |
| LTP | Linear Time-Varying Periodic |
| PCB | Printed Circuit Board |
| PEV | Plug-in Electric Vehicle |
| PFC | Power Factor Correction |
| PoE | Power over Ethernet |
| PoL | Point of Load |
| PSiP | Power Supply in Package |
| PWM | Pulse Width Modulation |
| PwrSoC | Power Supply on Chip |
| SC | Switched Capacitor |
| SiC | Silicon Carbide |
| SMPS | Switch-Mode Power Supplies |
| SoC | State of Charge |
| SR | Series Resonant |


| THD | Total Harmonic Distortion |
| :--- | :--- |
| TRL | Technology Readiness Level |
| V2G | Vehicle to Grid |
| VHF | Very High Frequency |
| WBG | Wide Bandgap |
| ZCS | Zero-Current Switching |
| ZVS | Zero-Voltage Switching |

## 1. Introduction

This chapter discusses the background and motivation behind this Ph.D. project, defines the thesis scope, and outlines the structure and the connections with the scientific articles attached in the appendices.

### 1.1 Background and Motivation

Switch-mode power supplies (SMPS) exist in our everyday life on a wide scale. From electric vehicle (EV) chargers to computing power supplies and light-emitting diode (LED) lighting drivers, a SMPS is employed to convert the AC power from the mains to the load electrical characteristics. As technology advances, additional features are continuously added to new products, with a special focus on miniaturization with added performance. While product engineers have managed to develop smaller and highly-portable products for consumer electronics and other industrial applications, the power supplies needed to deliver energy to those products have not scaled at the same pace. The main hinder for size and weight reduction has been the passive components needed in a power converter for energy storage and processing [1].

Since passive component sizes are inversely proportional to the switching frequencies of power converters, researchers have been investigating the opportunities for increasing the converters switching frequencies as a way to reduce their volumes, while achieving the same performance in terms of efficiency and power quality [2][3].

Pulse-width-modulated (PWM) converters have been the primary candidate for SMPS across different applications, thanks to their high power factor and efficiency, as well as simple control. However, their operation is based on hard switching. As a result, they are typically designed to operate at low switching frequencies in order to limit the switching losses. That, in turn, results in the need for bulky passive components to store and process the energy delivered to the load. Whereas high-frequency designs, with operating frequencies above 1 MHz , have less efficiencies owing to the substantial increase in switching power losses, which in some cases requires the incorporation of a heat sink to remove the heat associated with such losses, counteracting the gain in power density.

As a result, soft-switching resonant converters have been receiving much attention in recent years. Thanks to their zero-voltage switching (ZVS) and/or zero-current switching (ZCS) characteristics, they are posed to substantially lower switching losses than their PWM counterparts. That makes them a main candidate for power converters operating at high frequencies with high efficiencies, and accordingly high power densities [2]. In addition, operation at higher frequencies brings along additional features, such as higher loop-gain bandwidths and faster transient responses, which are of key importance for specific applications, e.g. the information technology (IT) sector [4]. This has led to the investigation of their adoption into different applications typically dominated by PWM converters, one of which is the grid-powered offline converters that are the main focus of this thesis.

### 1.1.1 Offline Converters

The conventional solution for offline converters is a two-stage architecture [5], as shown in Figure 1.1. The first stage is a front-end AC-DC power factor correction (PFC) rectifier that interfaces the AC mains. The second stage is a front-end DC-DC converter that provides the voltage and current levels that apply to the load's electrical characteristics. Interfacing the two stages is an energy-storage capacitor that stores the difference between the varying input power and constant output power. The end-to-end conversion has to comply with a number of regulations dictating the shape of the input current and limits on the electromagnetic interference (EMI) generated by the power converter.

## PFC Stage

The power factor of a circuit is defined as the ratio between the real power $P$ consumed by the circuit, i.e. average input power that get delivered to the load (including losses), to the apparent power $S$ seen from the source [6].

$$
\begin{equation*}
P F=\frac{P_{I N}}{S_{I N}}=\frac{P_{I N}}{V_{I N_{r m s}} \cdot I_{I N_{r m s}}} \tag{1.1}
\end{equation*}
$$

A circuit with a power factor of unity is the one that emulates a perfect resistor to the source. Then the instantaneous input current is in phase with and proportional to the input voltage, and the real and apparent powers are equal, with zero reactive power $Q$, i.e. power that circulates in the circuit without getting delivered to the load.

For offline converters, where the input voltage is a sinusoid of a single frequency ( $50 / 60 \mathrm{~Hz}$ ), the power factor can be calculated as the product of the displacement and distortion factors. The displacement factor is function of the phase difference between the input current and voltage $\varphi$ as follows

$$
\begin{equation*}
\text { Displacement Factor }=\cos (\varphi) \tag{1.2}
\end{equation*}
$$

The distortion factor is function of the harmonic content in the input current, and defined as ratio of the RMS fundamental component of the input current to the total RMS value of the current.

$$
\begin{equation*}
\text { Distortion Factor }=\frac{I_{I N 1_{r m s}}}{I_{I N r m s}} \tag{1.3}
\end{equation*}
$$



Figure 1.1: Conventional offline converter structure.

Another common way to express the distortion factor is in terms of the total harmonic distortion (THD), which is defined as the ratio of the RMS value of a waveform excluding the fundamental, to the RMS value of the fundamental component.

$$
\begin{equation*}
T H D=\frac{\sqrt{\sum_{2}^{\infty} I_{n_{p k}}^{2}}}{I_{1_{p k}}} \tag{1.4}
\end{equation*}
$$

Using (1.4) to rewrite (1.3)

$$
\begin{equation*}
\text { Distortion Factor }=\frac{1}{\sqrt{1+\text { THD }^{2}}} \tag{1.5}
\end{equation*}
$$

Accordingly, for offline converters, the power factor is expressed as

$$
\begin{equation*}
P F=\frac{\cos (\varphi)}{\sqrt{1+T H D^{2}}} \tag{1.6}
\end{equation*}
$$

A circuit with low power factor will require a higher RMS input current to deliver the same power as one with a high power factor does. That higher RMS current results in high conduction losses in the wires in addition to contaminating the grid with its harmonic content that can interfere with operation of nearby loads. For these reasons, several international standards have emerged that limit the magnitudes of the harmonic currents that a load can inject into the mains [7]-[9], where the allowed power factor depends on the application and the power level of the load connected to the grid. Throughout this thesis, the power factor and THD figures will be used to compare prior-art as well as proposed PFC converter solutions.

The most basic circuit for performing AC-DC rectification is the peak-detection rectifier shown in Figure 1.2. It is comprised of a diode bridge and an energy-storage capacitor to filter the double-the-line $100 / 120 \mathrm{~Hz}$ ripple for the DC load. While the circuit is simple with few components, the power factor is very low. The input current is comprised of short pulses taking place at the peak of input voltage. While the input current fundamental is essentially in phase with the voltage, i.e. unity displacement factor, the harmonic content of the current is very high, with a distortion factor lying in the range of $55-65 \%$ [1]. For applications with high-enough power rating, e.g. 25 W for lighting applications, this power factor is unacceptable and a PFC converter is required to keep the input current harmonics within the limits set by the standards. While passive PFC circuits have been reported to regulate the input current, with the low line frequency of $50 / 60 \mathrm{~Hz}$, those circuits are bulky and impractical to


Figure 1.2: Peak-detection rectifier.
implement in modern-day applications, and other forms or active PFC circuits based on the SMPS technology are employed [10][11].

## Energy-Storage

In the process of AC-DC conversion, the difference between the instantaneous input power and constant output power needs to be stored within a circuit element. That, in principle, is either a capacitor or an inductor. However, the use of an inductor for double-the-linefrequency energy-storage is impractical with respect to size, weight, and cost considerations. For instance, a $10-\mu \mathrm{F} 100-\mathrm{V}$ capacitor and a $100-\mu \mathrm{H} 30-\mathrm{A}$ inductor can each store about 50 mJ of energy. However, the capacitor is substantially smaller, lighter and cheaper. Accordingly, an energy-storage capacitor is employed after the AC-DC stage, as shown in Figure 1.1. The ripple on the energy-storage capacitor has a low frequency component of double the input line frequency $\omega_{\text {}}$ and an amplitude function of the output power, the DC-bus voltage, and the capacitor size [6], as follows

$$
\begin{equation*}
V_{D C_{-} \text {ripple }} \approx \frac{P_{\text {OUT }}}{2 \omega_{l} \cdot C_{D C} \cdot V_{D C_{-} r m s}} \tag{1.7}
\end{equation*}
$$

The energy-storage capacitor typically constitutes one of the largest single components in an offline converter, as its size is dictated by the $50 / 60 \mathrm{~Hz}$ standard line frequency. The primary solution for the energy-storage capacitor is the electrolytic capacitor, as this technology offers higher capacitive densities than others [12]. However, it is one of the most common causes of failure in offline converters and limits their overall lifetime. As a result, research has been investigating different ways to eliminate the need for the incorporation of electrolytic capacitors, such as active ripple filtering circuits (ripple ports) [13][14] and architectural solutions [15].

## DC-DC Converter

The DC-DC converter stage handles conversion of the DC-bus voltage to the load electrical characteristics in terms of voltage or current. In applications where galvanic isolation is a requirement, the isolation is typically implemented in the DC-DC stage [5]. The typical output voltages for the front end DC-DC stage is between 12 and 48 V for a wide range of DC loads, including LED lights, IT and telecom loads. In many applications, an additional point-of-load (PoL) DC-DC converter is incorporated for further regulation of the output voltage/current and to satisfy the strict control requirements with respect to loop bandwidth and fast transient responses.

For other applications, such as EV battery chargers, a high output voltage between 200 and 500 V is demanded, with different modes of regulation of output power, such as constant current (CC), constant voltage (CV), and constant power (CP) modes. In addition, bidirectional power flow for both offline converter stages is demanded to support the vehicle-to-grid (V2G) technology, which is in great demand to support the grid during voltage sags and frequency dips associated with the high dependence of today's power systems on renewable energy sources [16].

### 1.2 Thesis Scope

The objective of this thesis is to investigate challenges with the adoption of resonant power converters operating at high switching frequencies into offline converter applications, and conclude their gains with respect to conversion efficiency, power factor, and control.

With the challenging control of resonant converters due to their sensitivity to changes in line and load conditions, different topologies with inherent PFC capabilities are investigated to eliminate the need for a current control loop in PFC converters. For the DC-DC stage, a study of design methods to allow for inherent load regulation capability of the converter is conducted.

A current limitation with the state-of-the-art quasi-resonant PWM converters is their limited capability to maintain ZVS operation across wide load and line ranges, which is demanded in several offline converter applications. A study of different resonant converter solutions with the ability to achieve ZVS operation across wide input/output ranges is conducted, where different applications with different power ranges and forward/reverse power flow are considered.

While universal mains compatibility is common across the different industrial offline converters, the high variation in the line input conditions impede the optimization process for the power stage components. Architectural solutions to enable universal mains operation for a converter designed for specific AC mains input are explored.

The power stages integration is a potential means for reducing the bill of materials and converter volume, at the expense of limited efficiency and control performance. Techniques for resonant converter stages integration are investigated for applications with strict specifications on size and cost.

Lastly, high-frequency operation is reliant on the converter components and can have direct effect on converter modeling, control methods. The state-of-the-art semiconductor devices and magnetic materials that enable high-frequency operation are examined, in addition to relevant converter models and control techniques.

### 1.3 Thesis Structure

Figure 1.3 gives an overview of the thesis outline, where the color code links the publications to the most-related chapters. The thesis here is structured as follows:

Chapter 2 presents an overview of resonant power converters, and the state of the art with respect to their topologies, different architectures, modeling and control. In addition, the state-of-the-art solutions for the front-end AC-DC and DC-DC stages are discussed.

The front-end AC-DC stage is the main focus of Chapter 3. Resonant converter solutions for this stage are presented and compared to the state-of-the-art PWM counterparts for the same power range.

Resonant converter solutions for the front-end DC-DC stage are presented in Chapter 4. The design equations and procedures for the different solutions are provided, and different prototype implementations in terms of power range and power directions are discussed.

Chapter 5 introduces different structures for the power stage architecture that aim for high power density and high efficiency, where the concepts of power stages integration, universal compatibility, stacking of converter cells, and variability of the DC-bus are investigated.

The state-of-the-art wide-bandgap semiconductor devices and high-frequency magnetic materials employed in the different prototypes are presented in Chapter 6.


Chapter 7 presents solutions for modeling and control challenges associated with highfrequency operation and resonant power conversion.

Lastly, chapter 8 summarizes the thesis contribution, concludes the presented work, and illustrates the key ideas for future work.

Appendix A includes a description of the modular resonant converter test platform used in the design and prototyping processes throughout this thesis, in addition to an overview of the lab setup used for the implemented converters' characterization. Following, the appendices including the different publications are attached.

## 2. State of the Art

This chapter starts with an overview of the state of the art on resonant power conversion, including their topologies, models, control methods, in addition to associated topics such as synchronous rectification and converter structures. Following, the state of the art front-end AC-DC and DC-DC converter stages are covered.

### 2.1 Overview of Resonant Converters

Resonant converters are derived from radio-frequency amplifiers, which are used to generate a high-frequency current for an antenna [17]. As shown in Figure 2.1, a resonant converter is comprised of two stages [18]. The first stage is an inverter comprising a switch network which converts the $D C$ (or low-frequency $A C$ ) input to a high-frequency $A C$ power that is fed to a resonant tank providing AC-AC gain. The second stage is a high frequency AC-DC rectifier that reforms the energy in the resonant tank and delivers it to the load.

Resonant converters have the advantage of soft-switching operation that is allowed through the intrinsic alternating behavior of the switches currents and voltages. They suffer substantially lower switching losses (ideally zero) compared to their hard-switched counterparts. That allows for the design of converters operating at high switching frequencies with high efficiencies, which makes them a primary candidate for next generation offline converters with smaller volumes and weights.

### 2.1.1 Topologies

There are many different topologies of resonant converters that are made up of different combinations of compatible inverters and rectifiers. Under ideal operating conditions, all topologies achieve ZVS and/or ZCS. In the following, the most common inverter and rectifier topologies reported in literature and used in this thesis are presented.

## Class-E Inverters and Rectifiers

The class-E family of resonant converters is the most commonly used [18][19]. Figure 2.2 shows a class-E converter comprising a class-E inverter and a class-E rectifier. It has the fewest number of active devices, with a single switch in the inverter, and a single diode/switch in the rectifier. Both devices are referenced to ground, which simplifies the gate driving requirements. On the other hand, class-E converter cells have a high number of magnetic


Figure 2.1: Resonant converter structure.
devices, with two inductors in the inverter and one in the rectifier. More importantly, the main drawback of the class-E converters is the high voltage stress on the semiconductor devices, which is highly dependent on the duty-cycle. Typically, the voltage stress across the inverter switch and rectifier diode/switch is 3-4 times the input and output voltages, respectively. Class-E converters are reported in several high-frequency implementations [20]-[23].

## Class-DE Inverters and Rectifiers

The class-D inverter comprises a half- or full-bridge switch network that drives a resonant tank, and a half- or full-wave rectifier network [18]. The main advantage of this family is that the voltage stress across the inverter switches is equal to the input voltage. The same applies for the rectifier diodes with respect to the output voltage. This makes the class-D inverter/rectifier circuits more relevant for high-voltage applications. Additionally, in its simplest forms, it requires a single magnetic device in the resonant tank. On the other hand, in addition to the higher number of active devices, the need for high-side gate drivers is the main limitation of this topology.

The class-D converter designs that take into account the output capacitance of the converter switches in order to achieve ZVS are called class-DE converters, as they combine the advantages of the low voltage stress of the class-D converters and the ZVS capabilities of the class-E converters [24][25]. Figure 2.3 shows the schematic of a class-DE series-resonant (SR) converter comprising a half-bridge series-resonant inverter and a half-wave rectifier. Highfrequency implementations are reported in [26]-[28].


Figure 2.2: Class-E Converter.


Figure 2.3: Class-DE SR Converter.

### 2.1.2 Synchronous Rectification

As diodes are inherently lossy due to their forward voltage drop, synchronous rectification is employed in low output voltage applications and the rectifier diodes are replaced with switches, leading to higher efficiencies [29]-[31]. Another motivation for synchronous rectification is the need for bidirectional power flow in some applications [21], [32]-[36]. One of the main challenges of synchronous rectification is the synchronization of gate signals and phase shift between the inverter and rectifier to achieve ZVS, and several solutions are proposed for that including time-control circuits [33]-[35], self-gating rectifiers [21][37], and matching networks in the resonant tank [32], [38][39].

### 2.1.3 VHF Resonant Converters

In the push for increasing switching frequencies, prior art was reported on the design and implementation of resonant converters switching in the very-high-frequency range (VHF, 30300 MHz ) [2][3], [17], [38], [40]-[42]. There are several opportunities and challenges that have risen with such trend. In the VHF range, the passive component sizes are significantly reduced. That allows for the incorporation of air-core magnetic devices, saving the core loss in magnetic cores. Another advantage of VHF operation is the absence of conducted EMI that lies in the range of 150 kHz to 30 MHz , as the switching frequency and its harmonics lie above that range. On the other hand, the radiated EMI noise poses a challenge for such converters, and requires filtering and EMI shielding to suppress the peaks below the limits set by the standards [43]. In addition, even with soft-switching operation in the power loop, driving the switch-network in the converter using traditional hard-gating methods is impractical in the VHF range, and the gate switching losses are very high. For that reason, several solutions for resonant gate-driving techniques are reported [21]-[23], [44], where the energy use in driving the switches gates is recycled and the gate losses are substantially reduced. That, however, results in limited control of the power stage, especially with switching frequency modulation, which is the simplest means for controlling a resonant converter.

### 2.1.4 Stacking and Input-Output Arrangement

As discussed in Section 2.1.1, the class-E converter has the advantage of the need for a single low-side switch and simpler gate driving circuit, which is of key importance in high-frequency operation. However, the high voltage stress on the switch that reaches 3.6 times the input voltage for a duty-cycle of $50 \%$ complicates the implementation, especially for offline converter applications where the switch stress can reach 610 V for converters designed for US mains, and 1170 V for those designed for European mains. That led to the introduction of the class- $\Phi_{2}$ topology [45][46], which is similar to the class-E converter with the addition of an LC tank in parallel with the switch. The additional tank is designed to have resonance at the second harmonic of the switching frequency, resulting in reduction of the voltage stress across the switch to two times the input voltage at $50 \%$ duty-cycle. That comes with the cost of two additional passive components in the converter.

Another concept reported for voltage stress reduction is the converter input-output rearrangement [47]. By connecting the output to the input, part of the delivered power flows
directly from the input to the output and is not processed by the converter, resulting in higher converter efficiency and reduction of voltage and/or current stress on the converter switches. However, the drawback of such technique is the irrelevance to applications where galvanic isolation is a requirement. In [23][48], another means for stress-reduction in resonant offline converters based on converter cell stacking is reported. By combing the two techniques, i.e. connecting the output to the input and stacking $N$ number of inverter cells, the input voltage for each cell becomes equal to

$$
\begin{equation*}
V_{\text {IN_cell }}=\frac{V_{\text {IN }}-V_{\text {OUT }}}{N} \tag{2.1}
\end{equation*}
$$

### 2.1.5 Modeling

The typical design and modeling procedures for PWM converter do not apply to resonant converters. PWM converters models are based on the small-ripple hypothesis, where the ripple can be averaged and only the underlying linear converter dynamics are taken into consideration [6], [49][50]. This is not applicable on resonant converters, as it would average out the resonance in the resonant tank to zero.

For the analysis and design process, obtaining the characteristics of a resonant convert with the state-space approach is a cumbersome process. This is why the first-harmonic approximation (FHA) approach, sometimes referred to as fundamental-frequency component approach, is widely used in the analysis of resonant converters for the design phase [18]. It provides simple closed-form analytical expressions for converter characteristics, giving insight into circuit operation and the effect of the different circuit parameters on converter performance. However, the FHA equations become invalid if the loaded quality factor of the resonant tank is low (<2.5) and/or the switching frequency is much higher or lower than the resonant frequency (factor of 1.5 and above), as the current and voltage waveforms are no longer sinusoidal, and the converter may enter discontinuous conduction mode. In such cases, the state-space analysis and models must be used.

Models that are able to capture the periodic behavior have been developed for resonant converters. One approach models the converter using multiple systems connected with a reset map [51]-[53]. While this approach maintains all the information of the converter operation, it is impractical for analysis and control design purposes. Another approach commonly employed for active front ends modeling is the Linear Time-Varying Periodic (LTP) model [54]-[58]. This method uses a harmonic state space model to describe how every single input harmonic component impacts every harmonic component of the output. Lastly, several other modeling approaches are based on the generalized averaging model [59]-[62], which extends the original averaging model method by describing the periodic behavior of the system using a Fourier series. Many of these approaches come with a set of assumptions about purely sinusoidal signals or fast-decaying harmonics to simplify the problem, and result in solutions valid for a limited operation range. In addition, the prior art employing these models reports converters operating with switching frequencies up to 200 kHz . At such low frequencies, the circuit parasitic components have negligible effect on circuit operation and can be overlooked in the models. However, with increased switching frequencies in the range of several MHz , these models prove inaccurate.

### 2.1.6 Control

The duty-cycle modulation used in PWM converters, though simple and easy to implement, is not typically used for resonant converters that operate with a fixed duty-cycle. One common means for resonant converters control is through switching frequency modulation [63]-[65], which effectively changes the gain according to the topology transfer function, and output voltage/current can be regulated against changes or disturbances in the line or load conditions.

Another common control method for resonant converters is burst-mode (on/off) control [66][67], which is based on turning the converter on and off at its steady state with a frequency sufficiently lower than the switching frequency, where power is regulated through the burst signal duty-cycle. The advantages of this control method include the linear response and simple controller implementation. On the other hand, the burst signal introduces lowfrequency harmonics that can lead to high EMI noise, requiring filtering of considerable size depending on the burst signal frequency. It is, however, commonly employed for light-load operation to limit the maximum switching frequency needed to achieve lower loads and achiever higher light-load efficiencies than otherwise achieved with frequency control [46][68].

In addition to frequency and burst-mode control methods, out-phasing control is also reported for resonant converters [69][70]. This type of control works by modulating the phase difference between two or more inverters. The inverter outputs are combined through a passive network and the converter output is function of the phase difference between the two-or-more inverter cells. However, it requires a multiple-inverter architecture, or full-bridge-inverter, and strict control of the phase-shift between the inverter cells to balance power processing.

### 2.2 State-of-the-Art Front-End Converters

This section presents an overview of the different reported solutions for the AC-DC and DCDC offline converter stages.

### 2.2.1 PFC Converters

PWM converters have been widely used for the PFC stage in offline converters. The most commonly employed topology is the boost PFC converter [71]-[73]. The boost input inductor offers direct and simple control of the input current with the switch signal duty-cycle modulation. However, it requires the DC-bus voltage $V_{D C}$ to be higher than the peak input voltage, typically 400 V , to ensure proper operation over the entirety of the line cycle. As a result, several solutions have been reported based on the buck [74]-[77], buck-boost [78][79], flyback [80], and SEPIC [81][82] converters. Over the years, other solutions have been introduced for applications with different requirements. For high power applications, with high input currents, bridgeless topologies have been reported to limit the conduction losses in the diode bridge [71], [83]-[86], where the bridge is partly or fully replaced with transistors that are in some cases integrated in the converter. For applications with size and/or control
constraints, several quasi-resonant topologies with reduced switching losses are reported to achieve reliable high-frequency designs [87]-[91].

Switched-capacitor (SC) converters have been reported for use in high-power PFC converters [92]-[94]. The reported topologies are used for input current regulation, and require a large number of switches and capacitors. That, however, proves to be impractical for low-mid power converters in the range of up to few hundred watts, in addition to the complex control to achieve PFC with maintenance of charge balancing in the capacitors.

On the other hand, resonant PFC solutions are reported using the class-E inverter [23], the class-E rectifier [95]-[97], the class-D inverter [98]-[101], and the class-D rectifier [102][103]. Other than the work reported in [23], none of the reported solutions was designed for highfrequency operation, and most of them targeted electronic ballast applications with a highfrequency AC output.

### 2.2.2 DC-DC Converters

For high power applications, a commonly employed PWM topology for the DC-DC stage is the full-bridge converter [104]-[106]. The reported solutions target an output power in the range of 1-1.2 kW, operate with switching frequencies between $80-250 \mathrm{kHz}$, and achieve an efficiency of 95-97 \%. For low power charging applications, the flyback converter is one of the most commonly employed topologies in offline converters [107]-[109]. Prior art targeting an output power of 65 W achieve efficiencies between 92 and $95 \%$ with switching frequencies of less than 1 MHz .

On the other hand, the LLC resonant converter is one of the most commonly employed power converters for DC-DC conversion [110]. It is reported for applications targeting various power levels between few tens of watts to several kilowatts, with switching frequencies between few hundred kHz to few MHz [29]-[31], [111]-[113].

For applications with the need for bidirectional power flow, two common topologies for the DC-DC stage are the phase-shifted full-bridge and the dual active bridge converters [114]. However, with the wide output voltage range in some applications, such as plug-in electric vehicle (PEV) battery chargers, both converters have limited capabilities for maintaining ZVS operation across the wide output voltage range. While the LLC topology can achieve ZVS under any load conditions with proper design, it is incapable of the reverse power flow necessary in bidirectional applications owing to its asymmetric resonant tank. As a result, prior art reported the CLLC converter, which is similar in topology and operation to the conventional LLC converter, with an added $L C$ tank on the secondary side of the transformer [115][116]. That enables bidirectional power flow with the replacement of the rectifier diodes with switches, i.e. synchronous rectification.

## 3. Resonant PFC Converters

This chapter discusses the work done with respect to the first stage in an offline converter, which is responsible for AC-DC rectification and power factor correction. Different resonantbased solutions are proposed for that stage. The proposed solutions can be classified based on the circuit topology, where class-E- and class-D-based converters are presented. Another means for classification of the presented work is based on controlled vs. uncontrolled input current of the converters. That latter classification is important for two reasons. Firstly, as hard-switched PWM converters have long served as the primary solution for the AC-DC stage, most of the available PFC controllers on the market have a bandwidth of few hundred kHz, which limits the PFC stage designs to that range of frequencies, placing an upper limit on the power density. Secondly, as resonant converters are characterized with high sensitivity to line and load changes, they require challenging control to achieve a linear relationship between the input current and voltage across line and load ranges while maintaining ZVS. This has led to their more versatile use in DC-DC converter applications rather than in AC-DC converters. Accordingly, a main focus in this work is invested into the analysis and design of PFC converters with inherent PFC capability. In addition to providing freedom from the limited bandwidths of available PFC controllers and allowing for high-frequency designs, this eliminates the need for the control loop regulating the input current and narrows down the control requirements to output voltage/current regulation. Figure 3.1 illustrates the classification of the relevant articles in the appendices. The topology-based classification is followed in the structure of this chapter.


Figure 3.1: Classification of presented resonant PFC converter solutions.

### 3.1 Class-E-Based Resonant PFC Converters

Resonant PFC converters based on the class-E topology have the advantages and disadvantages of the class-E converter. On one hand, they need a single low-side switch in the power stage, which reduces the active devices count and simplifies gate-driving requirements. The topology features an input inductor, which provides good control of the input current and simplifies the input filter designs. On the other hand, the topology has three magnetic devices compared to one in the class-D converter, which poses a challenge with the high-frequency operation due to the AC losses in magnetic devices, and limits the overall converter power density with the limited energy density of inductors. More importantly, the high-voltage stress on the semiconductor devices is the main challenge with this topology, which can reach 3-4 times the peak input voltage. That places stringent requirements on the semiconductor devices relevant for such applications, especially for designs with universal compatibility.

### 3.1.1 Class-E Converter for US mains with Inherent PFC Capability

In [J5], the class-E inverter is investigated for use in PFC applications. Analytical and statespace models are derived showing the class-E inverter's capability of achieving inherent PFC operation with a constant duty-cycle. A converter incorporating a diode bridge, a class-E inverter, and a class-D rectifier is proposed for the PFC stage in single-phase offline converters. Figure 3.2 shows the schematic of the proposed converter. The circuit analysis resulted in the following equation for the rectifier input resistance

$$
\begin{equation*}
R_{i n}=\frac{1}{\omega_{s} C_{s}}\left[\frac{(1-D)[\pi(1-D) \cos (\pi D)+\sin (\pi D)]}{\tan (\pi D+\varphi) \sin (\pi D)}\right] \tag{3.1}
\end{equation*}
$$

where $\omega_{s}$ is the switching frequency, $C_{S}$ is the effective switch-node capacitance, $D$ is the switch driving signal duty-cycle, while $\varphi$ is the phase shift between the resonant tank current and switch-node voltage and is calculated from the following equation

$$
\begin{equation*}
\tan (\varphi)=\frac{\cos (2 \pi D)-1}{2 \pi(1-D)+\sin (2 \pi D)} \tag{3.2}
\end{equation*}
$$



Figure 3.2: Proposed class-E inverter/class-D rectifier converter for PFC applications [J5].

From (3.1) and (3.2), it is seen that the input resistance is function of the switching frequency and duty-cycle. Therefore, in steady-state, with a constant switching frequency and dutycycle, the converter emulates a resistor to the input source and power factor correction is inherently achieved.

While the analytical approach resulting in (3.1) and (3.2) is based on the FHA approach for analyzing resonant converters, which assumes a high loaded quality factor for the resonant tank and operation near resonance, the result is further affirmed through state-space analysis for the power stage. The state-space analysis takes into account the switch on-resistance and the design parameters are computed numerically, and is eligible for modeling converters with any loaded quality factor of the resonant tank and any size for the input inductor.


Figure 3.3: Class-E PFC Converter experimental waveforms at full-load [J5].

A prototype is implemented to validate the analysis and presented design procedure. The prototype operates from US mains with ZVS across the load range and achieves up to 211 W of output power at an efficiency of $88 \%$, with an inherent power factor and THD of 0.99 and $8.8 \%$, respectively. The measured input current harmonic magnitudes are well-within the limits of the IEC 61000-3-2 standard for class-C devices (lighting equipment), making the converter relevant for LED driver applications. Frequency modulation is used to achieve lower output power down to 25 W , with a power factor of 0.95 , THD of $28 \%$, and an efficiency of $88 \%$. Figure 3.3 shows experimental results for full load operation, with full ZVS and high power factor. Detailed results and waveforms are presented in Appendix [J5].

### 3.1.2 Stacked Class-E VHF Converter for European Mains PFC

The class-E inverter/class-D rectifier PFC converter is also reported in [C2] in a VHF design employing capacitive isolation, where the input-output arrangement and stacking techniques reported in [47] and [23][48], respectively, are utilized to reduce the voltage stress on the switches and the total power processed by the converter. The self-oscillating gate driver reported in [22][44] is employed for driving the switches. A $35-\mathrm{MHz} 50-\mathrm{W}$ converter is designed for operation from European mains. Simulation results show an efficiency of $90 \%$, power factor of 0.93 and THD of $38 \%$, which violates the limits set by the standards [7][8]. The reduced power factor is a result of more architectural than topological considerations. More details on that are given in Chapter 5 and Appendix [C2].

### 3.2 Class-DE-Based Resonant PFC Converters

Resonant PFC converters based on the class-DE topology have the advantage of the reduced voltage stress across the switching devices, where the inverter switches and rectifier diodes/switches are subject to voltage stresses equal to the input and output voltage, respectively. Additionally, the need for less magnetic devices gives this topology a benefit over the class-E converter in many applications. Nonetheless, that comes with the cost of a higher number of active devices and the need for high-side gate driving. In this section, two implementations for the class-DE converter in PFC applications are presented. The first is based on the addition of a charge-pump circuit that achieves control-free PFC operation, and the second works in a controlled manner with no additional circuit/component overhead.

### 3.2.1 Charge-Pump-Based PFC Converters

The use of charge-pump-based techniques for PFC applications was reported in the 90 's for use in electronic ballast circuits [98]-[101]. Through the addition of a capacitor and a diode to a conventional class-D inverter, the input current is regulated to follow the input voltage and achieve PFC. The concept is revisited in this work and used towards AC-DC applications, where a high-frequency rectifier circuit is added to rectify the inverter current.

Figure 3.4 shows the basic charge-pump PFC circuit. The diode $D_{B}$ represent the input diode bridge, while the energy-storage capacitor and the subsequent DC-DC stage are modelled with $C_{D C}$ and $R_{D C}$, respectively. The variable voltage source $V_{H F}$ is equivalent to a high-frequency voltage node in the converter circuit. The energy-storage capacitor $C_{D C}$ is designed in accordance with the pump capacitor $C_{P}$ such that the DC-bus voltage $V_{D C}$ is higher than the


Figure 3.5: Charge-pump PFC converter equivalent circuit.
input voltage $V_{I N}$ across the entire line cycle, and accordingly the diode bridge $D_{B}$ and the pump diode $D_{P}$ do not cross-conduct. Consequently, the input current is equal to the positive charging current of the pump capacitor.

Figure 3.5 shows representative waveforms for circuit operation across one half of a line cycle. The pump capacitor is charged and discharged within the rise and fall times of $V_{H F}$, respectively, and the capacitor charge $\Delta Q_{P}$ is proportional to the voltage difference across the capacitor $V_{P}$, which varies between a low-frequency high value $V_{P_{-}}$high and a constant low value $V_{P_{-} \text {low. }}$. The circuit design ensures that the charge variation of $C_{p}$, which is proportional to the voltage variation across it ( $V_{P_{-} \text {high }}-V_{P_{-} \text {low }}$ ), follows the input voltage $V_{I N}$ across the line cycle ( $50 / 60 \mathrm{~Hz}$ ). Accordingly, the average input current follows the input voltage and a unity power factor can ideally be obtained.

From circuit analysis [C3][J3], the voltage variation across $C_{P}$ in one switching cycle is evaluated as

$$
\begin{equation*}
\Delta V_{P}=V_{P_{-} \text {high }}-V_{P_{-} \text {low }}=V_{I N}-V_{D C}+\left(V_{H F_{-} \text {high }}-V_{H F_{-} \text {low }}\right) \tag{3.3}
\end{equation*}
$$



Figure 3.4: Charge-pump circuit operation across half a line cycle.

From (3.3), in a converter circuit where the voltage $V_{H F}$ has a peak-to-peak amplitude equal to the DC-bus voltage, the voltage variation across the $C_{P}$ becomes equal to the input voltage, and the variation of the pump capacitor charge is

$$
\begin{equation*}
\Delta Q_{P}=C_{P} \cdot \Delta V_{P}=C_{P} \cdot V_{I N} \tag{3.4}
\end{equation*}
$$

The pump capacitor charging current, which is equal to the input current, averaged across one switching cycle, is then equal to

$$
\begin{equation*}
I_{I N}=\frac{\Delta Q_{P}}{T_{S}}=f_{S} \cdot \Delta Q_{P}=f_{S} \cdot C_{P} \cdot V_{I N} \tag{3.5}
\end{equation*}
$$

Where $f_{s}$ is the converter switching frequency. Therefore, at steady state, for a constant switching frequency, the pump capacitor charging current, and accordingly the input current, become proportional to the input voltage, resulting in a high power factor and low THD.

The voltage source $V_{\text {HF }}$ can thus be any high frequency waveform in the circuit with a peak-topeak amplitude equal, or close in value, to $V_{D C}$. With that condition fulfilled, a high power factor is guaranteed.

Assuming the voltage $V_{H F}$ is the half-bridge switching node in a class-DE converter, the circuit becomes impractical for high-frequency operation, as this subjects the half-bridge to a capacitive load, resulting in the loss of ZVS. In addition, the charge pump capacitor will charge and discharge very fast, depending on the capacitor $C_{P}$ size and the switches on resistance $R_{D S(o n)}$, which together give a very low time constant. That results in high current spikes that can reach tens of amperes through the diodes and switches.

To allow for operation at high frequencies, an inductor needs to be placed somewhere in the input current path to smooth the pump capacitor high-frequency current and effectively increase the transition times on the $V_{H F}$ waveform. In the following, three solutions for enabling the use of the charge-pump circuit in high-frequency resonant converters for AC-DC applications are presented.

## Charge-pump-based Class-DE Converter with shared resonant tank

In [C3], [J3], the charge-pump circuit is added to a class-DE series-resonant converter, where the pump capacitor is coupled to the node $V_{R E C}$ interfacing the inverter and the rectifier, as shown in Figure 3.6. The half-bridge is connected across the energy-storage capacitor, or in other words, the energy-storage capacitor is effectively moved to the converter input, which helps achieve ZVS operation across constantly varying input line voltage with a fixed dead time. By coupling the pump capacitor to the $V_{R E C}$ node, the class-DE converter resonant tank is inserted in the pump circuit current path, helping to smooth the pulsating input current and achieve inherent PFC functionality with ZVS operation. On the other hand, that led to the dependence of the power factor on the resonant tank gain, as substituting the high and low values for $V_{R E C}$ in (3.3) leads to the following expression for the input current

$$
\begin{equation*}
I_{I N}=\frac{\Delta Q_{P}}{T_{S}}=f_{S} \cdot \Delta Q_{P}=f_{S} \cdot C_{P} \cdot\left(V_{I N}-V_{D C}+V_{O U T}\right) \tag{3.6}
\end{equation*}
$$



Figure 3.6: Charge-pump PFC converter reported in [J3].
As a result, equation (3.6) sets the specification for the class-DE stage design, where a high resonant tank voltage gain (close to unity) is a condition for eliminating the $V_{O U T}-V_{D C}$ term and achieving a high power factor.

Figure 3.7 shows the design flow chart for the proposed PFC converter. From the design specifications for input voltage, output power, output voltage, and switching frequency, the design process starts by sizing the pump capacitor using the following equation

$$
\begin{equation*}
C_{P} \geq \frac{2 P_{\text {OUT }}}{\eta \cdot f_{s} \cdot V_{I N_{p k}}{ }^{2}} \tag{3.7}
\end{equation*}
$$

where $\eta$ is the converter efficiency. The DC-bus voltage stress resulting from the pump circuit operation is calculated using

$$
\begin{equation*}
V_{D C}=V_{O U T}+\frac{\pi}{2}\left(\frac{V_{I N_{\_} p k}}{2}-\frac{P_{\text {OUT }}}{\eta \cdot f_{S} \cdot C_{P} \cdot V_{I N_{-} p k}}\right) \tag{3.8}
\end{equation*}
$$

Following, the specification for the allowed double-the-line-frequency ripple on the energystorage capacitor that guarantees no cross conduction of the diode bridge and pump diode is calculated as

$$
\begin{equation*}
V_{D C_{-} \text {ripple }}<V_{D C}-V_{I N_{-} p k} \tag{3.9}
\end{equation*}
$$

The energy-storage capacitor is then designed for the specified low-frequency ripple by rearranging (1.7) to

$$
\begin{equation*}
C_{D C} \geq \frac{P_{\text {OUT }}}{2 \omega_{l} \cdot V_{D C_{\text {ripple }}} \cdot V_{D C}} \tag{3.10}
\end{equation*}
$$

The class-DE stage resonant tank design takes place using the FHA equations. For a chosen loaded quality factor $Q_{L}$, the resonant tank values are calculated as follows.

$$
\begin{equation*}
R_{R E C}=\frac{2 R_{L}}{\pi^{2}}=\frac{2 V_{O U T}^{2}}{\pi^{2} \cdot P_{O U T}} \tag{3.11}
\end{equation*}
$$



Figure 3.7: Charge-pump-based PFC converter design flow chart.

$$
\begin{gather*}
L_{R E S}=\frac{Q_{L} \cdot R_{R E C}}{\omega_{o}}  \tag{3.12}\\
C_{R E S}=\frac{1}{\omega_{o} \cdot Q_{L} \cdot R_{R E C}} \tag{3.13}
\end{gather*}
$$

Since this design procedure is a first pass approach, as components parasitics and other nonidealities have been neglected for simplicity, a design decision is made for the power quality, where a design iteration with respect to a larger pump capacitor and/or a larger energystorage capacitor may be needed. The resonant tank current stress is then calculated and used as the specification for the resonant inductor design.

$$
\begin{equation*}
I_{\text {RES_max }}=\pi \cdot P_{\text {OUT }}\left(\frac{2}{\eta \cdot V_{I N_{p k}}}+\frac{1}{V_{\text {OUT }}}\right) \tag{3.14}
\end{equation*}
$$

Based on the resonant tank design, another decision is made on whether the design specifications with respect to power density and efficiency are met, where a design iteration with respect to the class-DE stage design may be required for a different output voltage and/or resonant tank loaded quality factor.

A 1-MHz prototype is implemented and tested to validate the analysis and proposed design flow. The prototype achieves up to 50 W of output power with a power density of $1.2 \mathrm{~W} / \mathrm{cm}^{3}$ a power factor of 0.99 , a THD of $8.6 \%$ at an efficiency of $84 \%$, with harmonic magnitudes well-within the IEC 61000-3-2 standard class-C device limits [7][8]. Figure 3.8 shows experimental results for the implemented prototype waveforms at full-load operation with a
fixed dead time. The line-frequency waveforms show an almost-sinusoidal input current with a phase difference of $5.7^{\circ}$ with the input voltage. The switching-frequency waveforms are taken with infinite persistence to visualize the variations across the half-bridge voltage range, i.e. the double-the-line-frequency ripple on the DC-bus. The resonant tank current shows to be sinusoidal, ensuring the validity of the design equations based on the FHA approach. The switching-node waveforms show that full ZVS is achieved for the mid-range of $V_{D C}$, whereas partial ZVS is observed at the lower end of that range, as longer dead time is needed. On the other hand, a short interval with switches reverse conduction is noticed at the higher end of the range, for which a shorter dead time is required to achieve full ZVS.


Figure 3.8: Implemented prototype waveforms at full-load operation [J3].

While this topology achieves high power factor and low THD inherently with low component overhead (an extra capacitor and diode to the conventional class-DE converter), this comes with the cost of high stress on the resonant tank components, as the resonant tank is shared between the current paths for the charge-pump circuit and the power flow to the output. The high current stress in the tank, measured to 1.6 A peak as seen in Figure 3.8(b), complicated the resonant inductor design and resulted in high losses and limited efficiency at full load (84 $\%$ ). In addition, lower power factor of 0.94 and higher THD of $18 \%$ were obtained at half-load operation, as frequency modulation is used to vary the output power, and operation away from resonance resulted in low resonant tank gain (<1), and accordingly the input current is no longer function of only $f_{s}$ and $V_{I N}$, but rather also on the difference between $V_{D C}$ and $V_{\text {OUT }}$. Furthermore, the circuit achieves partial ZVS with a fixed dead time. In order to achieve full ZVS, an adaptive dead time adjustment technique, such as the one reported in [117], needs to be incorporated. A less-effective yet simpler method is through the incorporation of a larger energy-storage capacitor, which results in reduced ripple across the half-bridge. These factors together constitute a trade-off between efficiency, complexity, and power density. More details in this work are available in Appendix [J3] and Appendix [C3].

## PFC Port

The main reason for the limited efficiency of the previous topology is the need for the classDE stage resonant tank to store and process not only the charge to the load, but also the input charge from the pump circuit. In order to increase the efficiency, the resonant tank stress can be reduced by modifying the power flow. In [J4], the circuit is reconfigured by connecting the load to the DC-bus, as shown by the highlighted wire connection in Figure 3.9. With that modification, the load is supplied directly from the DC-bus, and the class-DE SR converter operates as a PFC port that is connected in parallel with the load and only processing the power for the charge-pump circuit.

A $200-\mathrm{kHz} 50-\mathrm{W}$ prototype is constructed to quantify the gain in the efficiency and size reduction. Figure 3.10 shows the measured line-frequency waveforms, with a sinusoidal input current in phase with the input voltage, with a power factor of 0.99 and THD below $8 \%$, with harmonic contents in compliance with the standards [7][8]. The prototype achieves an efficiency of around $92 \%$ and a THD below $8 \%$ across a load range of 20-50 W, with a remarkably smaller size for the resonant inductor. A $500-\mathrm{kHz}$ design is implemented at a later stage, achieving a power factor of 0.97 and efficiency of $94 \%$ at a power density of $3.6 \mathrm{~W} / \mathrm{cm}^{3}$.


Figure 3.9: Charge-pump PFC converter in [J4].


Figure 3.10: Line-frequency waveforms [J4].
(Scaling is $100 \mathrm{~V} / \mathrm{div}$ and $200 \mathrm{~mA} /$ div with $10 \mathrm{~ms} / \mathrm{div}$ ).
The main drawback of this topology is the limited design freedom for the output voltage, as the load is directly connected to the DC-bus, which is dictated to have a higher voltage potential than the line input across the different loads for proper operation of the pump circuit, and a following high step-down DC-DC converter is required for low-voltage DC loads.

## Splitting the resonant tank

Taking a step back to the class-DE converter in Figure 3.6, by moving the charge-pump coupling from the $V_{R E C}$ node to the switching node $V_{S W}$, the half-bridge is still shared between the two converters, while the class-DE stage resonant tank only processes the power to the output load. That successfully reduces the stress on the resonant tank. However, as previously mentioned, the charge-pump capacitor capacitively loads the half-bridge, resulting in loss of ZVS, in addition to high current spikes run through the diode bridge, the pump diode, and the half-bridge switches.

By adding an inductor in series with the charge-pump capacitor, the pulsating charge pump current can be smoothed. That, however, results in reduction of the power factor, as the voltage change across the pump capacitor is no longer equal to the input voltage, owing to the voltage drop across the inductor. Accordingly, the charge stored in the pump capacitor, and the input current, is no longer proportional to $V_{i n}$.


Figure 3.11: 1.5-stage offline converter [J6].

To bind the voltage across the pump capacitor to $V_{I N}$, two clamping diodes are added to the circuit, resulting in the converter structure proposed in [J6] and shown in Figure 3.11. The halfbridge switch network and its driving circuit are shared between the two stages, resulting in what can be described as a 1.5-stage architecture, where the current paths to the PFC and class-DE stages are split from the switching node. The detailed analysis and design equations are covered in Appendix [J6].

An important feature of this topology is the reduced current stress in the resonant tanks, which simplifies the magnetic devices design and enables higher efficiencies. The circuit analysis gives the following relation between the two stages resonant currents

$$
\begin{equation*}
I_{P_{-} \max }=\frac{8 \cdot V_{D C_{\_} \max }}{\eta \cdot \pi \cdot V_{I N \_p k}} \cdot I_{R E S_{-} \max } \tag{3.15}
\end{equation*}
$$


(a) ) Line-frequency waveforms ( $100 \mathrm{~V} / \mathrm{div}, 200 \mathrm{~mA} / \mathrm{div}$, with $5 \mathrm{~ms} / \mathrm{div}$ ).

(b) Switching-frequency waveforms (100 V/div, 1 A/div, with $200 \mathrm{~ns} / \mathrm{div}$ ).

Figure 3.12: Prototype waveforms at full-load operation [J6].

With a conservative assumption of $V_{D C_{-} \max }$ being equal to $V_{I N_{-} p k}$ and $100 \%$ efficiency, the pump circuit resonant tank current amplitude is at least 2.5 times the class-DE stage resonant current amplitude. Accordingly, the pump circuit resonant current is the one defining the criteria for achieving ZVS operation. The following relation between the switching frequency and the pump tank resonant frequency $f_{p}$ is obtained in the analysis

$$
\begin{equation*}
f_{P}=\frac{1}{2 \pi \sqrt{L_{P} \cdot C_{P}}}=\frac{2 \cdot f_{s}}{\pi} \tag{3.16}
\end{equation*}
$$

Accordingly, the switching frequency is sufficiently higher than the pump tank resonant frequency, which results in inductive mode of operation for the pump tank, achieving ZVS operation of the half-bridge switches.

A 1-MHz 48-V prototype is built for LED driver applications and tested. The prototype delivers up to 42 W of power, with a power density of $2 \mathrm{~W} / \mathrm{cm}^{3}$, and achieves a power factor of 0.99 , a THD of $6 \%$, and an efficiency of $90 \%$ at full load, with harmonic magnitudes well-within the IEC 61000-3-2 standard limits for class-C devices [7][8]. Figure 3.12 shows experimental results for the implemented prototype waveforms at full-load operation. The line-frequency waveforms show an almost sinusoidal input current in phase with the input voltage. The highfrequency waveforms show a sinusoidal transformer-secondary current and a triangular pump inductor current. That is the result of operation at the class-DE stage tank resonance, and well above the pump tank resonance, where the pump tank current is lagging the switching node voltage, achieving full ZVS operation.

### 3.2.2 Frequency-Modulated Class-DE PFC Converter

As mentioned in the beginning of this chapter, resonant converters are characterized with high sensitivity to line and load changes, and accordingly their relevance for PFC applications without external circuitry is questionable. In [J2], a throughout analysis of the class-DE converter operation to achieve a constant input resistance over a wide range of input voltage with a constant output voltage and for different loads is presented. The analysis shows that the converter's effective input impedance depends on the power processed and the switching frequency, and accordingly the switching frequency can be used to compensate for the nonlinearities resulting from power changes across the input voltage range. A set of conditions on the switching frequency and duty-cycle is derived under which the class-DE SR converter can achieve PFC functionality and ZVS operation across load range with no additional circuits.

The analysis takes into account the effective capacitances for the inverter switches $C_{s}$ and rectifier diodes $C_{D}$, and (3.17) defines a lower limit on the switching frequency to achieve a desired input resistance for different input and output voltages [118]. The inverter duty-cycle can then be calculated for any given operational point to achieve ZVS operation.

$$
\begin{equation*}
f_{s} \geq \frac{1}{2 \cdot R_{I N}} \cdot \frac{V_{I N} \cdot V_{O U T}-V_{I N}^{2}}{V_{O U T}}{ }^{2} \cdot C_{D}-V_{O U T} \cdot V_{I N} \cdot C_{S} \tag{3.17}
\end{equation*}
$$

The operation is experimentally verified under DC-DC operation for different operational points corresponding to different load levels across the line-voltage range. Results show PFC-


Figure 3.13: Extrapolated input current waveforms across the line cycle [J2].
compatible operation over an input voltage range of 60-325 V with switching frequencies in the range of 2-2.8 MHz. That input voltage range corresponds to a dead angle of $10.5^{\circ}$ in input current conduction across the line cycle, resulting in a THD of $6 \%$. An extrapolation of the input current waveforms from the measured input resistance values is illustrated in Figure 3.13 , showing an achievable power factor of 0.99 with an estimated efficiency of up to $94 \%$.

### 3.3 Summary

A comparison of the proposed solutions for resonant PFC converters is shown in Table 3.1, and the following points conclude their potentials.

- Even though the work reported in [J5] switched at a low-frequency of 90 kHz , as the target of that prototype was to prove the analysis and inherent PFC capability, the class-E topology shows potential for high-frequency high-power-density implementations that can take benefit of the ZVS capabilities achieved, with controllability through frequency modulation and no additional circuit overhead.
- The use of class-DE converter standalone, with no additional circuit, for PFC applications, though proven possible in [J2], is challenging, since it requires the design of a controller capable of performing the highly nonlinear modulation of the switching frequency and duty-cycle needed to achieve PFC functionality with ZVS operation, which can be impractical for a wide load range.
- The class-DE converter combined with the charge-pump circuit achieves high power factor of 0.99 , low THD of less than $10 \%$, and efficiency of around $90 \%$, with highfrequency 1 MHz designs that give a power density of up to $2 \mathrm{~W} / \mathrm{cm}^{3}$, as shown by the different results in [J3], [C3], [J4], and [J6]. The implementation in [J6] is of special interest as it proposes a solution for the end-to-end offline converter, with the ability to provide for different output voltages and powers across different applications. It also has a reduced bill of material that shares the switch network between the PFC and DC-DC stages, and achieves some of the best-in-class figures for efficiency and power quality.

Table 3.2: Comparison between proposed resonant PFC converters.

| Reference | $[\mathrm{J5}]$ | $[\mathrm{C} 2]$ | $[\mathrm{J3]}$ | $[\mathrm{J4}]$ | $[\mathrm{J} 6]$ | $[\mathrm{J} 2]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Topology | Class-E | Class-E | Class-DE | Class-DE | Class-DE | Class-DE |
| Aux. Circuits | None | None | Charge-pump | Charge-pump | Charge-pump | None |
| Input Voltage [V $\mathrm{rms}^{2}$ ] | 120 | 230 | 230 | 230 | 230 | 230 |
| Output Power [W] | 211 | 50 | 50 | 50 | 50 | 50 |
| Output voltage [V] | 170 | 110 | 300 | 400 | 45 | 450 |
| Switching freq. [kHz] | 90 | 35000 | 1000 | 200 | 1000 | 2000 |
| Power Factor | 0.99 | 0.93 | 0.99 | 0.99 | 0.99 | 0.99 |
| THD [\%] | 8 | 38 | 9 | 6 | 4 | 5 |
| Efficiency [\%] | 88 | 90 | 88 | 92 | 91 | 94 |
| Semiconductors | SiC | -- | GaN/SiC | GaN/SiC | GaN/SiC/Si | GaN/SiC |
| PFC Control | Inherent | Inherent | Inherent | Inherent | Inherent | Frequency + <br> Duty-cycle |
| Output Voltage | Frequency | None | Frequency | Frequency + <br> Control | Burst-mode |  |

From Section 2.2.1, several prior art solutions for low-power PWM PFC converters are summarized in Table 3.2. It can be seen that the majority of the reported solutions achieve a high power factor, low THD, and high efficiency. However, by comparison to the proposed resonant solutions, they mostly operate at low frequencies to limit the switching losses. In addition, all of the reported solutions require a controller for the input current, whereas the majority of the proposed solutions achieve PFC inherently. On the other hand, while most reported PWM PFC converters feature universal mains compatibility, the presented resonant converters are designed for either US or European mains. In Chapter 5, a power stage architecture that provides universal compatibility to any of the proposed PFC solutions is introduced.

Table 3.1: Reported PWM PFC converters for low power applications.

| Reference | [75] | [76] | [72] | [79] | [80] | [81] | [82] |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Year | 2011 | 2013 | 2016 | 2013 | 2017 | 2011 | 2016 |
| Topology | Buck | Buck | Boost | Buck-Boost | Flyback | SEPIC | SEPIC |
| Aux. Circuits | None | Switch and 2 diodes | None | None | None | None | None |
| Input Voltage [ $\mathrm{V}_{\mathrm{rms}}$ ] | Universal | Universal | Universal | Universal | Universal | $100 \mathrm{~V}_{\text {rms }}$ | $220 \mathrm{~V}_{\text {rms }}$ |
| Output Power [W] | 100 | 100 | 150 | 12 | 60 | 65 | 21 |
| Output voltage [V] | 90 | 80 | 250/450 | 112 / 350 | 24 | 48 | 30 |
| Power Factor | 0.98 | 0.96 | --- | 0.98 | 0.99 | --- | 0.99 |
| THD [\%] | --- | 18 | 5 | 8.7 | 8 | 1.6 | 12.6 |
| Efficiency [\%] | 96.5 | 95.5 | 95 | 88 | 90.8 | 92.8 | 91.6 |
| Semiconductors | Si | Si | Si/SiC | Si | Si | Si | Si |
| Switching freq. [kHz] | 25-425 | --- | 125-1000 | 65 | 45-300 | 50 | 50 |
| PFC Control | Constant ON-time | Constant ON-time | PWM / PFM | PWM | Variable ONtime | PWM | PWM |
| Output Voltage Control | Constant ON-time | Constant ON-time | PWM / PFM | PWM | Variable ONtime | PWM | PWM |

## 4. Resonant DC-DC Converters

This chapter's focus is on the second stage in offline converters. The DC-DC stage is responsible for regulating the DC-bus voltage to the voltage/current requirements of the load electrical characteristics. In applications where galvanic isolation is a requirement, the isolation is commonly implemented in the DC-DC stage [5]. Different applications have different requirements with respect to conversion ratio, line/load regulations ranges, control bandwidths, and power flow directions.

While the different resonant converters topologies are broadly used in DC-DC applications, the work presented in this thesis focuses on the class-DE based topologies, as they are well suited for the high-voltage DC-bus, in addition to the flexibility with different variants of the switch network, resonant tank, and rectifier network, which serves the needs for a wide range of applications and system requirements.

### 4.1 Class-DE-Based DC-DC Converters

Figure 4.1 shows several variants of the class-DE converter. The switch network can be configured as a half-bridge (HB) or full-bridge (FB) arrangement. Switches in a HB switch network carry double the current stress of the FB counterpart. Assuming the same power devices, the HB offers reduced device count at the expense of twice as high conduction losses in the switches. In addition, a HB voltage gain of 0.5 requires half the transformer primary winding number of turns for the same overall converter voltage gain and transformer flux density, resulting in half the primary winding resistance. However, the primary copper losses are twice that of the FB, owing to the four times squared RMS current.


Figure 4.1: Class-DE stage alternatives [P1].

The resonant tank is comprised of series and parallel connections of passive components. Among the commonly used resonant tanks are the series-resonant, parallel-resonant, series-parallel-resonant (LCC), and LLC configurations. Depending on the resonant tank design, different output voltages that are higher or lower than the input voltage are achievable, which allows for functioning in buck, boost, or buck-boost fashion.

The rectifier can be configured as half-wave (HW) or bridge configurations. Galvanic isolation and additional converter gain can be implemented through the incorporation of a highfrequency transformer to the rectifier network, enabling an additional transformer centertapped (CT) rectifier configuration. Compared to the bridge, the HW and CT configurations have half the number of devices. However, the HW has double the average diode current, resulting in twice the conduction losses, while the CT rectifier diodes see the same current stress as the bridge, resulting in half the diode conduction losses at the expense of twice the voltage rating. The HW rectifier has twice the voltage gain of CT and bridge. The CT rectifier has two secondary windings, giving double the resistance for the same winding area, resulting in twice the secondary winding copper losses. Table 4.1 shows a comparison between the different class-D switch and rectifier network configurations. The optimal design choice with respect to the converter topology depends on the conversion ratio and power ranges required for a specific application.

## Design Procedure

The main design goal is to maintain ZVS across the switching frequency range needed for output voltage/current regulation across line and load ranges. In order to achieve that, the entire operation has to be within the inductive region of operation of the resonant tank, where the resonant tank current lags the switching node voltage. An optimal design is the one that uses the minimum stored energy in the tank, i.e. minimum quality factor, to achieve ZVS, resulting in high efficiency. The FHA approach is used for the analysis and design of the DC-DC converter solutions presented in this work.

Figure 4.2 shows the proposed design flow chart. From the design specifications for the input voltage, output voltage, output power, and switching frequency, the design process starts by topology selection. In applications with high primary currents, where conduction losses dominate, a FB switch network is chosen to limit losses. In applications with high output voltage, a bridge rectifier is more suitable with the availability of low forward voltage and junction capacitance diodes. On the other hand, for low output voltage and high current

Table 4.1: Comparison between class-D switch and rectifier network configurations.

| Parameter | Switch <br> Network |  | Rectifier Network |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
|  | HB | FB | HW | CT | Bridge |
| No. of semiconductors <br> devices | 2 | 4 | 2 | 2 | 4 |
| Voltage Gain | $1 / 2$ | 1 | 2 | 1 | 1 |
| $R_{\text {REC }}$ |  |  | $2 n^{2} \cdot R_{L} / \pi^{2}$ | $8 n^{2} \cdot R_{L} / \pi^{2}$ | $8 n^{2} \cdot R_{L} / \pi^{2}$ |
| Current Rating | x 2 | x 1 | $2 \pi \cdot I_{\text {OUT }}$ | $\pi \cdot I_{\text {OUT }}$ | $\pi \cdot I_{\text {OUT }}$ |
| Voltage Rating | $V_{I N}$ | $V_{I N}$ | $V_{\text {OUT }}$ | $2 V_{O U T}$ | $V_{\text {OUT }}$ |
| Conduction Loss | x 2 | x 1 | x 2 | x 0.5 | x 1 |
| Winding Copper Loss | x 2 | x 1 | x 2 | x 2 | x 1 |

applications, the center-tapped configuration is more common owing to the lower total conduction losses and component count. Following, the transformer turns ratio is calculated from the nominal input and output voltages. Next is calculating the referred load resistance to the rectifier input $R_{R E C}$ through impedance transformation, as per Table 4.1. The resonant tank gain range is then obtained for the given input voltage range. The tank gain $M_{\text {RES }}$ is calculated from the overall converter voltage gain $M_{v}$, which is the product of the transformer turns ratio, the switch and rectifier network gains, and the resonant tank gain as follows

$$
\begin{equation*}
M_{V}=\frac{V_{O U T}}{V_{I N}}=n \cdot M_{S W} \cdot M_{R E C} \cdot M_{R E S} \tag{4.1}
\end{equation*}
$$

A maximum loaded quality factor $Q_{L}$ corresponding to full-load operation is then designed. A low quality factor design results in less energy stored in the tank and thus higher efficiency. However, it results in less gain sensitivity to frequency modulation, and a larger range of switching frequency is needed to satisfy gain requirements, which complicates control. Also, the extended high frequency needed for the low gain counteracts the gain in efficiency. After choosing a maximum $Q_{L}$ that satisfies the gain requirements within a reasonable frequency range, the resonant tank is designed based on the nominal normalized frequency $f_{n}$ using the following set of equations for the resonant frequency $f_{o}$, the resonant inductor $L_{R E S}$, and the resonant capacitor $C_{\text {RES }}$.

$$
\begin{equation*}
f_{o}=\frac{f_{s}}{f_{n}} \tag{4.2}
\end{equation*}
$$



Figure 4.2: DC-DC stage design flow chart.

$$
\begin{gather*}
L_{R E S}=\frac{Q_{L} \cdot R_{R E C}}{\omega_{o}}  \tag{4.3}\\
C_{R E S}=\frac{1}{\omega_{o} \cdot Q_{L} \cdot R_{R E C}} \tag{4.4}
\end{gather*}
$$

A design decision is then made based on whether ZVS operation across line and load ranges is obtained. While there are different ways to calculate the needed energy to achieve ZVS for specific semiconductor switches analytically, SPICE simulations and design sweeps are conducted in this work across the different ends of the operational range to verify full-ZVS operation. Several design iterations are made with respect to the chosen quality factor and resonant tank design until full-ZVS across operational range is achieved. Finally, a design decision is made on whether the design specifications with respect to power density and efficiency are met, where a design iteration with respect to the topology and resonant tank network can be required to satisfy the design specifications.

### 4.2 Class-DE SR Converter

The class-DE series-resonant converter comprises a resonant tank formed of a series connection of an inductor and a capacitor. The resonant tank gain can be expressed as a function of $Q_{L}$ and $f_{n}$ as follows [J3].

$$
\begin{equation*}
M_{R E S}=\frac{f_{n}}{\sqrt{\left[Q_{L} \cdot\left(f_{n}^{2}-1\right)\right]^{2}+f_{n}^{2}}} \tag{4.5}
\end{equation*}
$$

In [C1], a class-DE SR converter is presented for incorporation in the AC-DC and DC-DC stages in an LED driver. The converter incorporated a half-bridge switch network and a half-wave rectifier. A prototype operating from 350 V input at 1 MHz achieved an output power range


Figure 4.3: Switching-frequency waveforms [C1]. ( $V_{S W} 100 \mathrm{~V} / \mathrm{div}, I_{\text {RES }} 200 \mathrm{~mA} / \mathrm{div}$, HSG/LSG $5 \mathrm{~V} /$ div at $200 \mathrm{~ns} /$ div).
of 20 to 50 W through frequency modulation, with peak efficiency of $96 \%$. Figure 4.3 shows the switching-frequency waveforms with full-ZVS operation and a sinusoidal resonant tank current, which goes in accordance with the FHA approach used in the design procedure. This design forms the basis for the design of the class-DE SR stages in [J2], [C3], [J3], [J4] and [J6].

The same topology is investigated for low-voltage PoL converters, which are in some cases incorporated after the front-end DC-DC stage for further regulation of the output voltage/current and to satisfy the strict control requirements with respect to loop bandwidth and fast transient responses. A prototype is designed and implemented for Power-overEthernet (PoE) applications, with an input voltage range of $36-57 \mathrm{~V}$ according to the PoE standard, and for an output voltage of 30 V . The resonant tank gain is employed for output voltage regulation across the line and load variations, sparing the need for the transformer towards a high power density design. Output voltage regulation is achieved with a PI controller feeding a voltage controlled oscillator that modulated the switching frequency in the range of 4-14 MHz. The controller is designed based on the model introduced in [J1] and covered in Chapter 7.

Experimental results are presented in Figure 4.4. The converter delivers up to 19 W of power with a power density of $2.5 \mathrm{~W} / \mathrm{cm}^{3}$. Line regulation is achieved for an output power of 12 W across the input voltage range, with a maximum error of $2.3 \%$ and a peak efficiency of $90 \%$ at 37 V input. Load regulation is tested from the nominal input voltage of 48 V across a load range of 2-19 W , where a maximum error on the output voltage equal to $0.7 \%$ at light load, with a peak efficiency of $88 \%$ at full load. The reason for the poor efficiency at light load is the increased switching frequency to up to 14 MHz with a fixed dead time used across the operational range, which results in loss of ZVS.


Figure 4.4: PoE Class-DE SR Converter Experimental Results.

### 4.3 LLC Resonant Converter

The LLC converter offers two main advantages that make it a common factor in many of today's offline converters. The first being the capability of maintaining ZVS operation across wide input voltage and load ranges, which is dictated by the system in many applications. That results in high efficiency across the operational range, even with high-frequency designs. The second advantage is its inherent load regulation capability, which is achieved with operation at resonance, simplifying the controller design.

In comparison with the SR converter, an additional shunt inductance is added to the resonant tank. That inductance is higher in value than the series inductance and in most cases is realized through the transformer magnetizing inductance. Accordingly, the main implementation difference with the SR converter is the less ideal transformer with finite magnetizing inductance for the LLC converter. That shunt inductance introduces an additional lower resonant frequency to the gain function, which extends the inductive mode of operation and allows for boost gain in the tank. Proper design ensures that the frequency modulation range needed for line and load regulation lies entirely within the inductive mode of operation, and accordingly ZVS is achieved across operational range.

The resonant tank gain is the magnitude of the LLC circuit transfer function, and is function of $Q_{L}, f_{n}$, and the ratio of the total primary inductance to the resonant inductance $k$ [C4].

$$
\begin{gather*}
M_{R E S}=\frac{f_{n}{ }^{2}(k-1)}{\sqrt{\left(k \cdot f_{n}{ }^{2}-1\right)^{2}+{f_{n}}^{2} \cdot\left({f_{n}}^{2}-1\right)^{2} \cdot(k-1)^{2} \cdot Q_{L}{ }^{2}}}  \tag{4.6}\\
k=\frac{L_{R E S}+L_{M}}{L_{R E S}} \tag{4.7}
\end{gather*}
$$

Figure 4.5 shows plots of the resonant tank gain function with different $k$ values. It can be observed that all load curves cross at $f_{n}=1$ and have a gain of unity. Thus, operation at resonant achieves the same resonant tank gain across all load, resulting in an inherent load regulation capability. The curves peaks define the boundary between the capacitive and inductive regions of the resonant tank impedance across different loads. The value for $k$ constitutes a tradeoff between line regulation capability through frequency modulation and efficiency. A low $k$ value means more deviation away from the series-resonant tank towards an $L L C$ tank, with a more pronouncing second resonance frequency. That results in higher peaking of the resonant tank curve at the second resonance for the same quality factor, allowing for a higher gain variation within a narrow range of frequency modulation, and thus a better line-regulation capability. At the same time, a low $k$ value is achieved through the implementation of a less ideal transformer, with a smaller magnetizing inductance $L_{M}$, which in-turn results in higher magnetizing current and increased conduction losses, and in turn low light-load efficiency. In addition, a low $k$ value can limit the integration of the resonant inductance into the transformer leakage, and two magnetic devices are accordingly needed. The choice of the $k$ value shall accordingly be attributed to the topology selection, where a half-bridge switch network is more relevant for a high-k design with limited magnetizing current.


Figure 4.5: Resonant tank gain with $k=5$ (top) and $k=10$ (bottom) for the same loads.

In [C4], a 1-MHz LLC converter for the DC-DC stage in offline converters is presented. The converter is designed for a common DC-bus voltage of 400 V with $10 \%$ ripple, and an output voltage of 48 V , which is typical for several applications including IT, PoE applications, and lighting. A 65-W prototype is designed and implemented. The prototype incorporates a halfbridge switch network and a bridge rectifier, in relevance with the low primary current and the availability of high-performance Schottky diodes for the output voltage range. A peak efficiency of $96 \%$ is achieved at full load. Inherent load regulation capability is demonstrated in the range of 5-65 W of power with fixed switching frequency. Line regulation for 360 V to 440 V is achieved with a frequency modulation range of $816-1256 \mathrm{kHz}$. Figure 4.6 shows a scope capture for the switching-node voltage, resonant tank current, and the output voltage at 400 V input, 60 W and 1 MHz . The figure illustrates the inductive mode of operation, with the resonant current lagging the switching-node voltage, achieving full ZVS operation. More results and details are available in Appendix [C4].


Figure 4.6: LLC converter switching-frequency waveforms. ( $V_{\text {sw }} 100 \mathrm{~V} /$ div, $I_{\text {RES }} 500 \mathrm{~mA} /$ div, $V_{\text {out }} 20 \mathrm{~V} /$ div at $200 \mathrm{~ns} / \mathrm{div}$ ).

### 4.4 CLLC Resonant Converter

In [C6], a bidirectional CLLC converter is presented for the DC-DC stage in PEVs on-board battery chargers. Figure 4.7 shows a schematic of the designed converter with half-bridges for the inverting and rectifying switch networks. The following equation is derived for the resonant tank gain

$$
\begin{equation*}
M_{R E S}=\frac{k \cdot f_{n}{ }^{3}}{\sqrt{\left[Q_{l} \cdot\left(f_{n}{ }^{4} \cdot(1+2 k)-f_{n}{ }^{2} \cdot(2+2 k)+1\right)\right]^{2}+\left[f_{n} \cdot\left(1-f_{n}{ }^{2} \cdot(1+k)\right)\right]^{2}}} \tag{4.8}
\end{equation*}
$$

Similar to the LLC design, the optimal design is the one with the $k$ value that is low-enough to achieve the required gain yet high-enough to reduce the magnetizing current to the limit that guarantees ZVS at all conditions with minimized circulating energy. A 1-kW 500-kHz prototype is implemented. The prototype operates with ZVS across the operational range, achieving an efficiency of up to $96 \%$. Figure 4.8 shows experimental waveforms for converter operation at resonance with full ZVS across the primary and secondary switching nodes and sinusoidal resonant tanks currents. The proposed architecture allows the converter to operate at resonance for the bidirectional constant-power load range with a variable bus voltage, while frequency modulation is employed for the constant-current load range in the grid-to-vehicle (G2V) mode with a fixed bus voltage, resulting in a limited bus voltage range. This enables the use of 650-V Gallium Nitride (GaN) devices for the overall converter switches.


Figure 4.7: CLLC Converter Schematic [C6].


Figure 4.8: Experimental waveforms for nominal operational point. ( $V_{S W_{-} p} 250 \mathrm{~V} / \mathrm{div}, I_{R_{-} p}$ at $5 \mathrm{~A} / \mathrm{div}, V_{S W_{-} s}$ at $250 \mathrm{~V} / \mathrm{div}, I_{R_{-} s}$ at $5 \mathrm{~A} / \mathrm{div}$ at $500 \mathrm{~ns} / \mathrm{div}$ ).

### 4.5 Summary

This chapter presents the design procedure for class-DE converters for the DC-DC stage in offline converter applications, and describes several solutions that are summarized in Table 4.2. The following points conclude their potentials.

- The transformer-less series-resonant converter used for the PoE converter implementation offers a simple and compact solution for PoL converters.
- The LLC converter offers higher capability of maintaining ZVS operation across wide input voltage and load ranges compared to its PWM full-bridge and flyback counterparts. In addition, operation at resonance results in inherent load regulation

Table 4.2: Comparison between proposed dc-dc converters.

| Reference | [C1] | PoE Converter | [C4] | [C6] |
| :---: | :---: | :---: | :---: | :---: |
| Topology | Class-DE | Class-DE | Class-DE | Class-DE |
| Resonant Tank | SR | SR | LLC | CLLC |
| Input Voltage [V] | 350 | $36-57$ | $360-440$ | $384-540$ |
| Output voltage [V] | 200 | 30 | 48 | $250-450$ |
| Output Power [W] | 50 | 19 | 65 | 1000 |
| Power Flow | Unidirectional | Unidirectional | Unidirectional | Bidirectional |
| Switching freq. [kHz] | $950-1150$ | $4000-14000$ | $816-1256$ | $385-476$ |
| Peak Efficiency [\%] | 96 | 91 | 96 | 96 |
| Semiconductors | GaN/Si | GaN/Si | GaN/Si | GaN/GaN |
| Power Control | Frequency | Frequency | Frequency | Frequency |

capabilities and simplified control. Accordingly, the LLC converter is the optimal solution for high-frequency designs of the front-end DC-DC stage.

- The CLLC converter is the bidirectional variant of the LLC topology, which offers the same ZVS capabilities and high efficiency for applications with requirements for reverse power flow.
- As galvanic isolation is required in many offline converter applications, all of the proposed solutions can support galvanic isolation with the insertion of a highfrequency transformer in the rectifier network.


## 5. Power Stage Architecture

This chapter discusses several architectural solutions for the offline converter power stage. Topics covered include the integration of the two stages in a combined stage that handles both AC-DC and DC-DC conversion, universal compatibility of the presented PFC converters through an architectural solution, converter cells stacking for reduced voltage stress, partial power processing through input-output arrangement, and finally the gains and drawback of a variable DC-bus voltage vs. a fixed one.

### 5.1 Converter Stages Integration

The structures covered in Section 3.2.1 show variants of integration of the two converter stages, based on combining or decoupling the charge-pump PFC circuit and the class-DE converter.

### 5.1.1 Single-stage offline converter

In the converter structure presented in [J3][C3], the two stages share the switch network and the resonant tank. Figure 5.1(a) shows the structure block diagram, while a generic structure topology is shown in Figure 5.1(b), where the split resonant capacitor technique is employed to reduce the AC current stress in $C_{R E S}$ and $C_{D C}$, and a high-frequency transformer is added to the rectifier circuit to provide lower output voltages through the transformer turns-ratio.


Figure 5.1: Single-stage offline converter structure [P1].

A combined control method of switching-frequency modulation with burst-mode operation is proposed for achieving output voltage regulation across line and load changes.

While this structure offers higher integration capabilities through sharing of the resonant tank between the two stages, the integration of the resonant inductor in the transformer is not feasible. This structure also places a high current stress on the resonant tank, which complicates the resonant inductor design and limits efficiency. Another drawback is the limited flexibility with respect to the DC-DC stage design, as having a high resonant-tank gain is a condition for achieving a high power factor. In addition, achieving ZVS across a wide load range is challenging, as the currents in both the PFC and DC-DC stages have the same phase and frequency. A sufficient lag of the current is needed to ensure inductive mode of operation, which dictates operation at a frequency higher than the resonant frequency. That, in turn, reduces the resonant tank gain and accordingly the power factor.

### 5.1.2 1.5-stage offline converter

Compared with the single-stage structure, the 1.5-stage structure presented in [J6], and shown in Figure 5.2, shares only the switch network between the two stages, while the resonant tank is split in two, one for each stage.


Figure 5.2: 1.5-stage offline converter structure [J6].

While this structure has a higher component count over the single-stage, it is offering less component count than the conventional two-stage offline converter structure, in addition to several benefits. With the resonant tanks splitting, the design of magnetic devices becomes simpler, with reduced current stress in each tank, which leads to higher efficiency. The resonant tank split also offers additional flexibility for the DC-DC stage design, as the two stages are more decoupled, with no requirement for a high gain of the DC-DC stage resonant tank. Another advantage is the easier ZVS maintenance, as the charge-pump current peak is sufficiently higher than the class-DE stage current (at least 2.5 times) with more phase-lag, and accordingly dominating ZVS criteria fulfillment. However, this topology offers limited overall converter flexibility than the two-stage structure, as the control metrics in terms of switching frequency and duty-cycle affect both stages' operation. For example, if switching frequency control is employed, the input power increases with the higher $f_{s}$, which leads to a higher $V_{D C}$. However, a higher $f_{s}$ for the DC-DC stage means lower output voltage, as the resonant tank gain is reduced. Accordingly, the effect of $f_{s}$ modulation on both stages is not monotonic, resulting in voltage stress across the energy-storage capacitor. Burst-mode control is found to be of more relevance to this architecture.

### 5.1.3 Two-stage offline converter

While the previous structures offer low component count and compact design, the conventional two-stage architecture, shown in Figure 5.3, still finds its edge for applications with strict control requirements. Compared to the two previous structures, it offers the maximum flexibility, as the two-stages are completely decoupled from each other.

(a) Block diagram.

(b) Schematic example.

Figure 5.3: Two-stage offline converter structure.

In addition, two different control methods and control loops can be employed for the two stages. For instance, the two stages can operate with two different switching frequencies and even duty-cycles, resulting in fine-control capabilities. This structure also offers the lowest switch current stress, where different semiconductor devices can be incorporated for each stage depending on specifications. On the other hand, that comes with the cost of double the number of semiconductor devices and driving circuits. And while ZVS can be easily maintained for the PFC stage half-bridge, careful design is needed for the class-DE stage to achieve ZVS of the stage's half-bridge, with no aid from the PFC resonant tank current as in the 1.5 -stage structure.

### 5.2 Universal Compatibility

Universal offline converters need to handle variations of the AC mains voltage that range from 100 to $240 \mathrm{~V}_{\text {rms }}$. Accordingly, the PFC power stage needs to be designed to handle about double the current (or double the voltage) for the same output power. This variation in the line input conditions impede the optimization process for the power stage components, leading to converters designed for either US or European mains, or otherwise universallycompatible yet bulky implementations.

Take for example the charge-pump based converter reported in [J3]. The reported topology is functional with universal input mains operation, as the charge-pump circuit is able to achieve inherent PFC operation regardless of the input voltage, and that is illustrated in the experimental results with US mains operation in Appendix [J3]. However, as the prototype was designed to deliver 50 W for EU mains operation, it could only deliver a maximum of 13 W from US mains input. In order to achieve full-load operation with the reduced line voltage, two aspects need to be taken into consideration. First, in order to satisfy the condition for obtaining a high power factor, the resonant tank needs to be designed to handle the maximum resonant current. The following equation is used to evaluate the resonant tank current amplitude

$$
\begin{equation*}
I_{R E S}=\pi \cdot P_{O U T}\left(\frac{2}{\eta \cdot V_{I N_{-} \_k}}+\frac{1}{V_{O U T}}\right) \tag{5.1}
\end{equation*}
$$

From (5.1), for half the input line voltage and output voltage, the resonant current amplitude is twice that for the nominal input line voltage. That results in the need for a larger size of the resonant inductor in order to handle the higher current.

### 5.2.1 Switched-Capacitor Front-end Scaling Converter

In [P2], a power stage architecture is presented to reduce the voltage/current stress variation for a PFC circuit through the incorporation of a SC converter as the PFC front-end. The SC front end stage is used to scale the input line voltage to a higher or lower voltage, depending on the following PFC power stage design, where the SC stage is bypassed for the nominal input line voltage for which the PFC power stage is designed.

In [J7], a design is reported for which a $2: 1$ SC front-end stage, shown in Figure 5.4, scales down the EU mains line voltage for a PFC stage designed for US mains operation. An analysis


Figure 5.4: A 2:1 switched-capacitor converter [J7].


Figure 5.5: Proposed universal-mains architecture [J7].


Figure 5.6: Experimental waveforms for the SC front-end Boost PFC converter [J7].
is presented to conclude the effect of the SC front-end stage on the overall PFC converter performance. Figure 5.5 shows the proposed architecture, which is generically usable with any PFC circuit. The SC converter is combined with a conventional boost PFC converter to quantify the effect of the incorporation of the SC front end on power factor and efficiency. Figure 5.6 shows experimental line-frequency waveforms for the converter at 50 W , where a power factor of 0.94 and THD of $11 \%$ at 50 W with $230 \mathrm{~V}_{\text {rms }}$ at the input.

### 5.3 Converter Input-Output Rearrangement and Stacking

Converter cells stacking and input-output rearrangement concepts are employed in resonant converters for voltage stress reduction as well as partial power processing. One topology that is relevant for such architectures is the class-E converter, where three class-E inverters are
stacked in [23] for a US-mains PFC converter. In [C2], the design is extended with the addition of a stacked inverter stage to allow operation from European mains. While the design simulation results are briefly outlined in Section 3.1.2, the focus here is on qualifying the architectural gains. The presented architecture resulted in an input voltage of 54 V across each inverter cell, and accordingly 200-V devices with superior figures of merit (FoMs) can be used, instead of the 1200-V devices otherwise required without the architectural changes. Figure 5.7 shows a block diagram of the power stage architecture. The four inverter stages share the same resonant tank inductor, thus reducing the number of magnetic devices.

It is noteworthy that employing one or both of the architectural concepts results in gatedriving challenges, as most of the inverter switches are not referred to ground (all switches in case of output connection to the input). Accordingly, the resonant self-oscillating gate driver reported in [21][22], [44] becomes attractive in such architectures to simplify the gate-driving requirements. However, it has its limitations with the challenging design and tuning, as well as limited control.


Figure 5.7: Stacked architecture with input-output rearrangement of converters [C2].


Figure 5.8: Simulated line-frequency waveforms for the stacked architecture in [C2].

For the case of PFC converters, the input-output re-arrangement results in a dead angle in the input current conduction, as no current is drawn from the mains until the input voltage exceeds the output voltage. And with the use of the self-oscillating gate driver, additional dead angle results as the voltage across each inverter cell needs to be sufficient to get the gate driver to oscillate. That is the reason for the highly distorted input current of the design in [C2], which is shown in Figure 5.8. Another restriction with the stacking architecture is the need for precise timing of the driving signals for the inverter cells, which is a challenge in highfrequency designs. A mismatch in the conduction angle (across the line cycle) during steadystate or start-up will result in unbalanced voltage distribution across the inverters, and in turn destructive overvoltage on the switching devices.

### 5.4 Variable DC-Bus Voltage

While a fixed DC-bus voltage is typical for offline converters, a variable bus voltage proves to be of key importance in some applications in order to achieve high efficiency. That can be emphasized by the work done in [C6], where a CLLC converter is proposed for the DC-DC stage in EV charger applications. The topology and experimental results are briefly discussed in Section 4.4, and more details on the employed variable DC-bus architecture are presented in this section.

A typical 400-V EV propulsion battery pack has a terminal voltage of around 250 V at the low state of charge (SoC), which increases to 450 V at the high SoC along the battery charging profile.

In order to fast-charge the battery, a charging profile consists of two modes [119]. A CC mode for the battery voltage range between 250 V to 320 V , and a CP mode for the range between 320 V and 450 V . The battery discharge operation in V2G mode is only required for the CP range, as the battery stops delivering power when its voltage reaches 320 V . This is illustrated in Figure 5.9, where three different architectures with respect to the bus voltage range are illustrated.

Architecture 1 represents the conventional fixed-bus voltage solution. While that solution simplifies the design requirements for the PFC stage, it requires the DC-DC stage to convert that fixed voltage into the widely varying battery voltage. In the case of resonant converters, which operate most efficiently at resonance, the overall system efficiency is compromised with operation below and above resonance to provide the needed voltage gain. In addition, the fixed bus voltage add the requirement for boost gain in the resonant tank. In case of the CLLC converter, that requires a low ratio between the transformer magnetizing inductance and the resonant inductance $(k)$, which increases the cycling magnetizing current and complicates magnetic devices design, as discussed in Section 4.4. In addition, a wide range for the switching frequency is needed to cover the overall gain range, placing additional requirements on the DC-DC stage control circuit.

In order to resolve the drawbacks of the fixed bus architecture, prior art reported a varying bus voltage architecture to enable the resonant DC-DC stage to work largely or entirely at resonance [120]. While this architecture, shown in Figure 5.9 as Architecture 2, achieves the highest efficiency for the DC-DC stage, eliminates the need for boost gain in the resonant tank,
and simplifies control with fixed frequency operation, that comes with the need for highvoltage semiconductor devices for the PFC stage and the DC-DC stage primary side switches, in addition to complicating the PFC stage control.

In [C6], a limited bus voltage range is proposed. The converter is designed to operate at resonance, with a unity tank gain, for the entirety of the CP load mode. This eliminates the contribution of the resonant tank voltage gain to the overall converter gain, which is provided through the transformer turns-ratio, thus ensuring symmetry for bidirectional operation (no gain contribution from the resonant tank). For the CC load range, switching frequency modulation is applied with operation above resonance, providing for additional voltage gain on top of the transformer turn ratio to deliver the respective battery terminal voltage range. Although the converter operation is not entirely at resonance as in Architecture 2, high efficiency can still be achieved as the converter operates at resonance across the entire CP load range, with a reduced frequency modulation range over the CC load mode. Similar to Architecture 2, the proposed architecture eliminates the need for boost gain in the resonant tank. And most importantly, the reduce bus voltage range allows for the incorporation of 650V GaN devices for the overall converter switches.


Architecture 1


Fast Charging Profile
Architecture 2


Proposed Architecture

Figure 5.9: Comparison between fixed and variable DC-bus voltage architectures.
Table 5.1 shows a comparison between the device reported in [C6] with those reported in prior art incorporating Architecture 2. The comparison shows that a GaN device rated for the same current and a lower breakdown voltage offers considerable improvement in the device FoM compared to the Silicon Carbide ( SiC ) counterparts. Accordingly, the incorporation of GaN devices for the converter switches can lead to the improvement of the overall system efficiency. Furthermore, the GaN device technology has zero reverse-recovery charge, which
led to the investigation of employing the reverse-conduction characteristics of the rectifying side switches (depending on power flow direction) for the resonant tank high-frequency current rectification. That simplifies the design and eliminates the need for synchronous driving circuitry or matching circuits in the resonant tank. With a peak efficiency of $96 \%$ at 1 kW , it is found that one third of the total power loss is dissipated in reverse-conduction rectification ( 17 W ). Such finding constitutes a tradeoff between efficiency and simplicity/cost for the DC-DC stage design. Additional details on GaN devices reverse conduction losses are given in Section 6.1.

Table 5.1: Comparison of DC-DC stage primary-side devices with the same current rating.

| Application | $[119]$ | $[120]^{*}$ | $[\mathrm{C} 6]$ |
| :--- | :--- | :--- | :--- |
| Max. $V_{\text {bus }}[\mathrm{V}]$ | 680 | 840 | 540 |
| Device | C 3 M 0065100 K | C 3 M 0075120 J | GS 66508 T |
| Technology | SiC | SiC | GaN |
| Breakdown Volt. [V] | 1000 | 1200 | 650 |
| $R_{D S(\text { on })} @ 25^{\circ} \mathrm{C}[\mathrm{m} \Omega]$ | 65 | 75 | 50 |
| $Q_{g}[\mathrm{nC}]$ | 35 | 51 | 5.8 |
| $E_{\text {oss }} @$ max. $V_{\text {bus }}[\mu \mathrm{J}]$ | 18 | 25 | 10 |
| $Q_{r r}[\mathrm{nC}]$ | 310 | 220 | 0 |
| FoM1 = $R_{D S(o n)} \cdot Q_{g}$ | $2.28 \mathrm{E}-09$ | $3.83 \mathrm{E}-09$ | $2.90 \mathrm{E}-10$ |
| $\mathrm{E}-\mathrm{FoM}=R_{D S(\text { on })} \cdot E_{\text {oss }}$ | $1.17 \mathrm{E}-06$ | $1.88 \mathrm{E}-06$ | $0.50 \mathrm{E}-06$ |
| * The $100-\mathrm{A}$ device used in this reference is replaced with a 30-A |  |  |  |
| device for the same rated voltage for a better comparison. |  |  |  |

### 5.5 Summary

This chapter discussed several architectural solutions to improve the performance and efficiency of resonant offline power converters.

Integration of the two converter stages constitutes a trade-off between power density, cost, and performance in terms of controllability. The single-stage structure has the lowest component count, at the expense of limited efficiency and controllability. On the other hand, the two-stage structure provides the maximum design flexibility and high-performance control that comes with the higher cost. The proposed 1.5-stage structure represents a good trade-off between the advantages and drawbacks of the other two architectures. Combined with burst-mode control, the 1.5 -stage architecture is a primary candidate for applications with relaxed control requirements on output power and control resolution, e.g. LED drivers. It is worth noting that while the three structures are presented with a class-DE series-resonant converter for the DC-DC stage, other variants of the class-DE converter are compatible with any of the structures presented, as the charge-pump circuit can be coupled to any kind of waveform with a constant AC amplitude, regardless of its DC bias, as discussed in section 3.2.1. As long as (3.4) is met, a high power factor is achieved.

The architecture discussed in Section 5.2 enables the proposed resonant PFC solutions to operate from universal input mains, with a power stage optimized for handling high-voltage or high-current. Compared with the state-of-the-art SC front-end PFC circuits [92]-[94], the proposed SC stage is used in combination with a resonant/PWM PFC stage, requires only four switches, and operates in open loop. In addition, the PFC stage design is optimized for the
low-voltage input mains, and accordingly the DC-bus voltage can be reduced, which reduces the stress on the PFC stage as well as the following DC-DC stage devices, e.g. 200 V instead of 400 V for a boost converter.

The stacking and input-output rearrangement concepts allow for reduced stresses on the converter components, in addition to possible efficiency improvement through the partial power processing of the converter power stage. However, employing such concepts for the PFC stage results in a highly-distorted current owing to the dead angles in input current waveform. Accordingly, they are more relevant for DC-DC applications with constant input voltage, where the converter can work in continuous conduction mode.

Lastly, as resonant power converters operate most efficiently at resonance, the variable DCbus architecture enables higher efficiency by expanding the region of operation at resonance. By optimizing the DC-bus voltage range to achieve a good balance between operation at resonance, simple synchronous rectification, and incorporation of high-performance semiconductor devices, improved efficiency and reduced cost can be achieved for the end-toend converter solution.

## 6. Devices

The converter's active and passive components play a key role in minimizing the power loss and achieving ZVS operation. An investigation of the best-in-class switching devices and magnetic materials relevant for high-frequency operation is presented in this chapter.

### 6.1 Semiconductor Devices

Wide bandgap (WBG) semiconductor technology has greatly evolved and currently offers many advantages over silicon devices, including better FoMs and reduced reverse-recovery charge. Even with the soft-switching nature of the resonant converters presented throughout this thesis, WBG devices play a critical role in the reduction of conduction and gate-charge related losses in the different designs.

### 6.1.1 Comparison of Commercial Devices

In order to find the best-in-class semiconductor devices for a given application, the following three FoMs are chosen to compare the available devices [121]-[125]

$$
\begin{align*}
& F O M 1=R_{d s(o n)} \cdot Q_{g}  \tag{6.1}\\
& F O M 2=R_{d s(o n)} \cdot Q_{g d}  \tag{6.2}\\
& E F O M=R_{d s(o n)} \cdot E_{o s s} \tag{6.3}
\end{align*}
$$

Where $Q_{g}$ is the total gate charge, $Q_{g d}$ is the gate-to-drain charge, and $E_{o s s}$ is the output capacitance stored energy. Figure 6.1 shows a comparison between the best-in-class switches for low-power offline converter applications across the three commercially available semiconductor technologies. Table 6.1 lists the manufacturers and part numbers for the devices in comparison. GaN FETs show superior performance compared to the silicon superjunction and SiC counterparts. Device \#6 is used for the low power prototypes in this work in [J2][J3], and its PDFN package variant is used in [J4][J6]. For the high-power application reported in [C6], a high-current variant (GS66508T by GaNSystems) is incorporated. In [J5], a 1200-V SiC MOSFET (C3M0075120D by Cree) is employed. SiC Schottky diodes (GB01SLT06214 by GeneSiC) are employed in the high output voltage prototypes in [J2]-[J4] and [J6] for high-frequency rectification, where they showed higher efficiency and thermal stability than the silicon counterparts. For low-voltage high-frequency point-of-load PoE converter described in Section 4.2, the 65-V EPC8009 device is used, as it would incur the lowest gate losses.

### 6.1.2 Layout Considerations

Since offline converter applications involve high-frequency switching of voltages of few hundred volts, several failure mechanisms can take place without the careful layout of the converter printed circuit board (PCB), leading to destructive results. For example, a high parasitic inductance on a GaN device gate may lead to substantial voltage ringing. That ringing may exceed the low gate-oxide breakdown voltage ( 7 V for GS66502B), in addition to the
potential false turn-on of the device that can lead to shoot-through currents in class-D converters. Accordingly, a number of layout considerations are implemented in the different prototypes presented in this thesis.

Table 6.1: Best-in-class devices for low-mid power offline converters.

| $\#$ | Manufacturer | Part no. |
| :---: | :---: | :---: |
| 1 | ST | STD18N55M5 |
| 2 | Infineon | IPL65R195C7 |
| 3 | ROHM | SCT3120AL |
| 4 | UnitedSiC | UF3C065080K4S |
| 5 | Transphorm | TPH3206PSB |
| 6 | GaNSystems | GS66502B |



Figure 6.1: Comparison of best-in-class switches FoMs [J3]. ( $\mathrm{E}-\mathrm{FOM}$ in $\mathrm{m} \Omega \cdot \mu$, and FOM1-2 in $\mathrm{m} \Omega \cdot \mathrm{nC}$ ).

In order to control noise coupling from the power loop to gate-drive loop, the gate driver packages are placed within close proximity to the devices' gate terminals to minimize the gate parasitic inductance. The source terminal connection to the driving and power loops is split in a star-connected fashion in order to alleviate the gate ringing from the common-source inductance. For gate drivers with separate source/sink pins, a chip resistor is added in the path to the gate to control the miller effect. A higher value for the source path resistor is used to reduce the turn-on $\mathrm{dv} / \mathrm{dt}$ slew rate and limit gate oscillation, where a lower value is chosen for the sink path resistor to provide a strong pull-down during turn-off, which helps prevent the false turn-on events with the low threshold voltage of GaN FETS.

### 6.1.3 GaN Reverse-Conduction Characteristics

The reverse conduction characteristics of GaN devices are investigated in this work to quantify the associated power loss. Figure 6.2 shows measurement results for the reverse conduction characteristics of two GaN devices used in this thesis across different temperatures with zero gate-source voltage. The results are obtained using a Keysight B1505A curve tracer. Considering that the GaN device has zero reverse-recovery charge ( $Q_{R R}$ ), the power loss due to reverse conduction is calculated from the switch reverse current $I_{D S}$ and voltage $V_{D S}$ as follows

$$
\begin{equation*}
P_{r c}=\frac{1}{T_{s}} \int_{0}^{T_{s}} I_{D S}(t) \cdot V_{D S}\left(I_{D S}(t)\right) d t \tag{6.4}
\end{equation*}
$$

In [J3], where a fixed dead time is implemented across line and load variations, the reverse conduction characteristics are used to get an estimate of the worst-case power loss due to reverse conduction associated with the fixed dead time across input line variations. By examining the waveforms of the switch reverse current, the corresponding reverse voltage drop across the switch, and the reverse conduction interval, the worst-case power loss due to reverse conduction is calculated to 0.54 W . That sets a trade-off between the efficiency and cost/complexity of adding an adaptive dead time adjustment circuit [117].


Figure 6.2: Measured reverse conduction characteristics for the GS66502B (left) and GS66508T (right) devices.

In [C6], the reverse-conduction characteristics were employed for the resonant tank highfrequency current rectification. In this case, the reverse-conduction interval expands over the entire switching cycle. With a peak efficiency of $96 \%$ at 1 kW , it is found that one third of the total power loss is dissipated in reverse-conduction rectification (17 W). As the target application in this work required bidirectional power flow, this design offers simplicity and
lower cost by eliminating the need for a complex synchronous driving circuitry or a matching network in the resonant tank, at the expense of the additional power loss with the reverse conduction of the rectifying devices.

### 6.2 Magnetic devices

The operation of resonant converters is based on pure AC currents in the resonant tank. For high-frequency designs, choosing a relevant magnetic material for the resonant tank magnetic devices is of key importance to achieve high efficiency. Figure 6.3 shows a comparison of several high-frequency magnetic materials in terms of core losses at 1 MHz [126][127]. The $3 F 46$ material by Ferroxcube shows the lowest losses and is used for the different implementations in [J2]-[J4], [J6], [C4], and [C6]. Another material, ML91S from Hitachi metals [128], is experimented with in later designs and preliminary results show good potential for operation in the $1-2 \mathrm{MHz}$ range.


Figure 6.3: Core power-loss density (Pv) vs. magnetic flux density (B) for different magnetic materials at 1 MHz [J3].

Integration of magnetic devices is exploited in several implementations in this thesis. Through the separation of the primary and secondary windings across the core winding window, a lower coupling coefficient can be achieved and the leakage inductance is used towards the resonant tank series inductance. That is employed in the series-resonant, LLC, and CLLC implementations reported in [J6], [C4], and [C6], saving the space and cost of additional magnetic devices.

### 6.3 Summary

The GaN device technology is found to be the one with highest relevance for offline converter applications with breakdown voltages of up to 650 V . For applications employing topologies with high switch stress, such as the class-E converter, or a high-voltage DC-bus, SiC devices prevail. With respect to magnetic devices, different high-frequency magnetic materials are compared in terms of core losses, and the 3F46 material by Ferroxcube is found to be optimal
for the frequency range of 1-2 MHz. For higher frequency designs, the magnetic devices design is a main challenge, due to the lack of low-loss magnetic materials for frequencies higher than 3 MHz .

## 7. Modeling and Control

This chapter covers different research findings with respect to the modeling and control techniques relevant for high-frequency resonant converters.

### 7.1 Modeling

For analysis and design purposes, the FHA approach was sufficient for the design of the converters presented in [J2]-[J4], [J6], [C3]-[C4], and [C6]. In [J5], the FHA approach is used to model the class-E inverter/class-D rectifier converter to investigate the input current shaping capabilities of the converter, and it is proven that the input impedance of the converter is reduced to a constant resistance with a constant duty-cycle, achieving inherent PFC operation. That is further affirmed by a state-space model for the power stage that takes into account the switch on-resistance with any quality factor and input inductor size.

For the design of feedback controllers employed to meet the specifications on steady-state regulation, transient overshoot, and settling time, a dynamic model of the converter is needed. Many of the previously reported models for resonant converters come with a set of assumptions about purely sinusoidal signals or fast-decaying harmonics to simplify the problem, and result in solutions valid for a limited operation range. In addition, the prior art employing these models reports converters operating with switching frequencies of up to 200 kHz , as mentioned in Section 2.1.5. At such low frequencies, the circuit parasitic components have negligible effect on circuit operation and can be overlooked in the models. However, with increased switching frequencies, those models prove inaccurate. Accordingly, for highfrequency designs, models that take into consideration the converter parasitics need to be employed.

### 7.1.1 High-Frequency Class-DE Converter Model

In [J1], a reduced model for the class-DE series-resonant converter is presented. The model is based on the generalized averaging technique, incorporates the important converter parasitics, and uses multiple harmonics to obtain an accurate linear model. As the resulting model is of a high order, a model reduction approach is applied to simplify the model to a low order that provides computational robustness with high precision.

The proposed model is compared against the prior art. A prototype converter running at 1 MHz is implemented to compare the model-calculated values against measurement results. The results show that the parasitics significantly impact the DC-gain and converter dynamics, where the proposed model reduces the DC-gain error by more than 7 dB and the error in the low-frequency pole from $168 \%$ to $17 \%$. Moreover, the controller design based on prior art model is found to have 40 times larger overshoot in the measured control signal compared to the model prediction, while the controller based on the proposed model shows high correlation between measurements and model simulations.


Figure 7.1: Measured and calculated frequency response (left) and step response (right) of the proposed model vs. prior art [J1].


Figure 7.2: Control-loop responses of the prototype with controllers based on the proposed model and prior art [J1].

Figure 7.1 shows measured frequency and step responses with the calculated responses of the proposed model and prior art. The results show strong correlation between the measured responses and the ones calculated from the proposed model, while the prior art frequency response is too damped, with an offset in the settled value for the step response. PI controllers based on the proposed model and prior art are designed and tested with the implemented prototype to further assess the improvement. Figure 7.2 shows closed-loop step responses for a 1-V step in the reference voltage, equating to 50 V on the output voltage. The responses in the output and control voltages show the higher overshoot of the controller based on the prior art with about the same settling time.

### 7.2 Control

As mentioned in Section 2.1.6, there are three common ways to control resonant converters. Frequency control modulates the gain of the resonant tank by changing the switching frequency. Burst-mode control turns the converter on and off at its steady state with a frequency sufficiently lower than the switching frequency, and the power is regulated through the burst signal duty-cycle. Lastly, out-phasing control works by modulating the phase difference between two or more inverters or half-bridge legs.

### 7.2.1 Frequency Control

Output power modulation through changing the switching frequency is tested in [J2][J3][J5][C1][C3][C4][C6] in open loop. In the work presented in [J1], [J4], and the PoE
converter in Section 4.2, the loop is closed with a PI controller feeding a voltage-controlled oscillator that generates the driving signal. In the different implementations, the range and linearity of load regulation capability achieved through frequency modulation depends on the power stage design and its sensitivity to frequency change. However, frequency control cannot be used solely to control the output power down to zero load, as this requires a very high switching frequency that results in considerably higher gate losses, AC losses in the magnetic devices, and switching losses if ZVS is lost in a fixed dead time implementation. That results in very poor efficiency at light load, which can be observed from the experimental results for the class-DE SR converter shown in Figure 4.4, where the switching frequency is increased from 4 MHz to 14 MHz to regulate the output voltage from 19 W down to 2 W . That resulted in efficiency reduction from $88 \%$ at full-load to $64 \%$ at light load. For that reason, it is common practice to combine frequency control with burst-mode control, where load regulation through frequency modulation is employed for a reasonable high-load range, then burst-mode operation takes over to regulate the output down to zero load. That is implemented in [J4], where power regulation from 50 W down to 25 W is achieved with reducing the switching frequency from 200 kHz to 88 kHz . For lower power levels, the converter output voltage is controlled by a hysteresis controller that stops switching the power stage when the output voltage reaches 450 V and starts switching again when the voltage drops below 350 V .

It is noted that specifically in charge-pump-based circuits, the input power increases with the switching frequency as per (3.5), opposite to the class-DE stage dependence on the frequency. That can result in a voltage stress on the DC-bus capacitor if the overall converter transfer function does not model the linear dependence of the input power on the switching frequency. One way to resolve this is through the use of a two-stage structure with two separate controllers, such as the one in Figure 5.3, where the first controller regulates the DCbus voltage, and the second regulates the output voltage/current. Another resolution is the use of burst-mode control for the entire load range. That is implemented in [J6] for the 1.5stage structure shown in Figure 5.2, where the switching frequency is optimized for full-load at steady state, and on/off switching of the power stage handles the load regulation.

## Switching Losses in Converters with Frequency Control and Fixed Dead Time

Frequency control can affect ZVS operation, as the exact dead time needed to achieve ZVS is function of both the magnitude and phase of the resonant tank current, which in turn are functions of the switching frequency. Continuous adaptation of the dead time to achieve full ZVS operation across the line and load ranges is a challenge, especially in high-frequency designs. In many cases, a fixed dead time is designed and implemented to save the complexity and cost of an adaptive dead time adjustment scheme.

In [J8], an investigation of the different switching loss modes in GaN-Based converters with frequency control and a fixed dead time is conducted. A feasible operation region is identified, where the switches only exhibit reverse conduction losses. Figure 7.3 shows the feasible operation region (labelled 2) for a class-DE SR converter with a resonant tank quality factor of four. The region is bounded on one end by operational points for full-ZVS operation, i.e. the boundary between hard switching and reverse conduction, and on the other end with the
operational points where the resonant current changes direction. The analysis determines an upper bound for the losses within that region, and compares the cases where a fixed dead time is implemented vs. that with fixed duty-cycle of the switches driving signals across the region. It is concluded that a fixed dead time operation is superior to that with a fixed duty cycle. Compared to a fixed duty cycle operation, a reduction in the upper loss limit of $60 \%$ is achieved a fixed dead time across the same frequency range. While for the same upper loss, an expansion of the frequency range for region 2 by $33 \%$ is obtained. The analysis is validated on a 1-MHz class-DE series-resonant converter, where the feasible operation region and worst-case losses are measured. More details on this work are available in Appendix [J8].


Figure 7.3: The regions of operation and their respective switching waveforms [J8].

### 7.2.2 Burst-mode Control

To enable dimming functionality, burst-mode modulation is used in [J6] for output current regulation between 20 and 900 mA for a dimming functionality in an LED driver. A $20-\mathrm{kHz}$ PWM signal is applied to the gate driver enable input for on/off modulation of the converter switching signals, where the output current is modulated using the PWM signal duty-cycle. To suppress the PWM signal noise, an LC filter of a $10-\mathrm{mH}$ choke and a 100-nF shunt capacitor is incorporated on the test-bench board.

Although burst-mode control is limited with respect to control resolution and transient performance, and places additional requirements on the input filter design, it provides a linear control function and achieves an almost-flat efficiency vs. load curve, with remarkably better light-load efficiency than otherwise achievable with frequency control. Furthermore, it does not require the addition of an adaptive dead time adjustment scheme, as the dead time is set with respect to the switching frequency at steady-state and fixed across the entire load range with maintenance of ZVS.

It is worth considering that the burst PWM signal frequency has to be sufficiently lower than the switching frequency, in order to avoid intermodulation of the two signals that can result in distortion of converter output. At the same time, the PWM frequency needs to be sufficiently high above the audible range as well as the $40^{\text {th }}$ harmonic of the line current frequency in order not to violate the standards on input current harmonics in PFC applications
[7]-[9]. Another factor is the dependence of the input filter size on the burst signal frequency. The higher the switching frequency is, the higher the burst signal frequency can be, and the smaller the input filter needed.

## Line-Cycle Skipping Control

While burst-mode control can be perceived as switching-cycle skipping technique, with a minimum number of skipped cycles depending on the resolution of the low-frequency PWM signal, a special case is the one employed in PFC converters where line-cycle skipping is conducted [129]. When the load is reduced to less than a specific limit, one or more line cycles are skipped by the converter. The converter is turned on/off at the line-cycle zero crossing to reduce EMI and current THD. The lower the load is, the more skipped line cycles. However, the more cycles skipped, the higher the ripple is on the output voltage/current at light load, which places additional requirements on the energy-storage capacitor to satisfy hold-up time requirements. In addition to the high ripple, this control scheme suffers high output voltage drop/overshoot with relatively small load transients. As a result, its practicality shall be investigated with respect to different applications. It has been tested on the LED driver converter presented in [J6], and visible flicker could be observed on the LED load with a single skipped cycle and using a $100 \mu \mathrm{~F}$ electrolytic capacitor on the output, thus proving to be impractical for such application. However, if combined with frequency control, it can have an edge for light-load regulation where the energy processed in a line-cycle is already reduced from that processed at full load.

### 7.2.3 Time-Based Control

Over the past few years, signal processing in time was introduced for several applications, one of which is buck DC-DC converters controllers [130]-[132]. Time-based control utilizes the voltage-to-time conversion properties in ring oscillators and delay lines to synthesize gain blocks, integrators, and differentiators in the time domain. In the push for miniaturized power converters, time-based control for high-frequency resonant converters has potential, as it takes advantage of technology scaling and low feature-size devices, which allows for monolithic integration with the power switching devices. That makes it a main candidate for controller design towards the highly integrated power supply in package (PSiP) and power supply on chip (PwrSoC) converters.

Compared to the digital controller, time-based control eliminates the quantization error introduced by the ADC and DPWM blocks, thus behaving like a linear system in steady state, and achieves a small voltage ripple similar to the analog controller. Compared to both analog and digital controllers, the time-based controller eliminates the need for a PWM generator, as the PWM signal is inherently generated in time-based signal processing. Furthermore, the needs for large passives, high gain-bandwidth error amplifiers, high-speed comparators, and ADC are obviated.

In [C5], an investigation of the employment of time-based control in a PFC boost converter is conducted, where two time-based controllers are combined to control the input current and the output voltage, in a similar function to the conventional average current mode controller [6]. The presented scheme is shown in Figure 7.4, and the model proved theoretical feasibility
via simulations of a 600-W PFC boost converter design, achieving a power factor of 0.99 with a constant output voltage of 400 V . The obtained line-frequency waveforms are shown in Figure 7.5.


Figure 7.4: Time-based average current mode controller for a PFC boost converter [C5].


Figure 7.5: Line-cycle waveforms from the time-based control model [133].

### 7.3 Summary

As the sizes of passive devices reduce with high-frequency operation, parasitic components can no longer be ignored in converter models. An improved linear model for high-frequency resonant converters is introduced. The model incorporates the converter parasitics and provides more accurate DC gain and dynamics. While the presented model is applied for a class-DE series-resonant converter topology, the modeling approach holds for variations of the class-DE converter, including the parallel-resonant, $L L C$, and $L C C$ topologies.

The different methods for control of resonant converters are discussed. While frequency control is optimal for line and load regulation at high loads, it is inefficient to use it to regulate the output at light loads. Burst-mode control is remarkably more efficient for light-load regulation, in addition to providing a linear control function and an almost flat efficiency vs. load curve. That, however, comes with the cost of limited control resolution and transient performance (relative to frequency control), and larger input filter. Yet for applications with relatively relaxed requirements for transient performance and output resolution, e.g. dimming functionality in LED drivers, standalone burst-mode control is a primary candidate for output current regulation across the entire load range. Line-cycle skipping is investigated, yet with the high output voltage/current ripple and low hold-up time, it is found impractical for low-power converters with a reasonably sized energy-storage capacitor.

The switching loss modes in a class-DE SR converter are analyzed and a low-loss operation region is defined for converters with frequency control and a fixed dead time. The analysis enables the calculation of the worst-case switching loss in the design phase, prior to prototyping, and provides basis for switching devices selection and controller design. The analysis is applicable on any resonant converter where a sinusoidal current charges and discharges the switching node.

Lastly, time-based control techniques are studied for use in a PFC converter, and results show theoretical feasibility for employing this type of control for high-frequency converters, as its monolithic-integration capabilities find an edge in the highly-integrated forms of converters, such as the PSiP and PwrSoC.

## 8. Conclusion and Future Work

This chapter provides a summary of the work presented in this thesis, a conclusion highlighting the key takeaways from the research findings, and finally the main ideas for future work.

### 8.1 Thesis Summary

This thesis presents advances in resonant power converters design and implementation for single-phase offline converter applications. The topics covered include converter topologies, power stage architecture, devices, modeling, and control. Solutions are proposed for the different offline converter stages, spanning the front-end AC-DC, front-end DC-DC, and PoL converters. The proposed solutions address a range of applications, including LED drivers, adapters, PoE applications, and PEV chargers. The converter designs also covered different frequency ranges, including MF ( $300 \mathrm{kHz}-3 \mathrm{MHz}$ ), HF ( $3-30 \mathrm{MHz}$ ), and VHF ( $30-300 \mathrm{MHz}$ ) for converters delivering few tens of watts to the kilowatt power range. Figure 8.1 shows several implemented prototypes.

Various methods for resonant converters control are employed, including frequency control, burst-mode control, and combination of the two. WBG semiconductor devices are used throughout the different implementations, where a study of the best-in-class devices for offline converter applications is presented, in addition to layout considerations and investigation of reverse-conduction losses. Other topics discussed encompass bidirectional power flow and synchronous rectification.


Figure 8.1: Several implemented prototypes.

### 8.2 Conclusion

The key takeaways from the presented work are as follows:

- Resonant converter technology is a main enabler for the next generation offline converters that will serve the current demand for miniaturization and high performance.
- All of the proposed soft-switching converters have the potential for operation at higher switching frequencies towards higher power densities, as all the circuit passive components scale with the switching frequency (except for the energy-storage capacitor, which is dictated by the standard line frequency of $50 / 60 \mathrm{~Hz}$ ).
- Considering the state-of-the-art devices and magnetic materials, the $1-2 \mathrm{MHz}$ frequency range is currently the optimal balance between efficiency and power density, and the switching frequencies are expected to rise with the ongoing development of semiconductor devices with better FoMs and low-loss magnetic materials.
- Switched-capacitor converters can play a role in the power stage architecture with simple 2:1 or 1:2 conversion ratios. Higher conversion ratios will eat up the power density margin for discrete implementation of low-power converters.
- Converter stages integration can promise high-power density and low-cost solutions at the expense of limited flexibility and control resolution.
- The FHA approach is adequate for the analysis and design process of most resonant power converters. For the design of feedback controllers for high-frequency converters, a dynamic model of the converter that takes into account the circuit parasitics is needed.
- Stacking converter cells and input-output rearrangement structures promise less stress and increased efficiency for non-isolated converter applications. However, the gate-driving requirements pose a challenge for the power density goals with the increased number of stacked converter cells.
- Frequency control is impractical to employ solely for converters with control requirements down to zero load. Combining control methods, e.g. frequency control with burst-mode control for light-load, provides means for achieving high control resolution and efficiency across the load range.
- Employing GaN devices reverse conduction for high-frequency current rectification offers a simple solution for challenges with synchronous rectification, by eliminating the need for precise synchronization circuitry or matching network in the resonant tank. That comes at the expense of additional power loss that is function of the output power and device reverse-conduction characteristics.
- Converters operating in the VHF range are basically limited with respect to the high radiated EMI emission associated with air-core magnetics, in addition to limited control capabilities that are dictated through the use of resonant gate drivers to limit gate losses.


### 8.3 Future Work

As the demand for high-efficiency and compact offline converters will only increase, the following list represents the most relevant ideas for further development of the work presented towards smaller and highly-efficient resonant power converters.

- Building on the class-E PFC converter presented in [J5], a high-frequency high-powerdensity design and implementation will show the real gain of such topology, which shows potential for high-frequency operation with the ZVS capabilities achieved.
- Expansion of the input voltage range of the resonant PFC converters presented in Chapter 3 through the adoption into the architecture presented in [J7] would place them on par with their PWM counterparts that are commonly universally compatible.
- Employing the gains of the model presented in [J1] into a controller design for the LLC converter presented in [C4] with low steady-state ripple, high loop gain bandwidth and fast transient response would offer a high performance compact solution for applications with strict control requirements.
- Quantification of EMI emissions in the converters presented in this work and the design of input filters for electromagnetic compatibility of the proposed solutions is required to increase their technology readiness level (TRL).
- As intensive labor work is conducted to implement Litz-wire-based magnetic devices for high-frequency converters, planar PCB winding magnetics are more relevant for mass production, with much less tolerances in inductances values and turns ratios. Investigation of the AC winding loss minimization, galvanic isolation, and magnetic devices integration in planar implementations for the magnetic components used in this work is another enabler for increasing the proposed solutions' TRL.
- Investigation of circuit design techniques to enable bidirectional power flow of the proposed PFC resonant converters would conclude their potential for incorporation in applications with such requirements, such as the PFC stage in EV charger system presented in [C6].
- With the demand for high-lifetime converters for some applications such as LED drivers, electrolytic capacitors are the bottleneck for a power converter's lifetime. The design of electrolytic-capacitor-free high-power-density converters is of substantial relevance. One suggestion is to reduce the energy-storage capacitor size and realize it using ceramic capacitors, while the DC-DC stage controller regulates the increased $100 / 120 \mathrm{~Hz}$ ripple at steady-state. Another suggestion is to employ active ripple port circuits for high-power applications, where the circuit overhead can be tolerated for increased lifetime.


## List of Publications

## Inventions

[P1] A. M. Ammar, Y. Nour, and A. Knott, "AC-DC Power Converter with Power Factor Correction", patent pending, December 2019.
[P2] Y. Nour, A. M. Ammar, A. Knott, and C. K. Lumby, "Universal Mains High Power-Density AC-DC Converter", patent pending, April 2020.
[P3] A. M. Ammar, Y. Nour, A. Knott, and F. M. Spliid, "High-Frequency Resonant AC-DC Converter", to be published.

## Journal Papers

[J1] N. J. Dahl, A. M. Ammar, A. Knott and M. A. E. Andersen, "An Improved Linear Model for High Frequency Class-DE Resonant Converter using the Generalized Averaging Modeling Technique," in IEEE Journal of Emerging and Selected Topics in Power Electronics, October 2019.
[J2] F. M. Spliid, A. M. Ammar, and A. Knott, "Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, December 2019.
[J3] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability," in IEEE Journal of Emerging and Selected Topics in Power Electronics, January 2020.
[J4] F. M. Spliid, A. M. Ammar, Y. Nour, and A. Knott, "A Series-Resonant Charge-PumpBased Power Factor Correction Port for Single-Phase Mains Rectification," under revision in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[J5] H. Mahdi, A. M. Ammar, Y. Nour, and M. A. E. Andersen, "A Class-E-Based Resonant ACDC Converter with Inherent PFC Capability," under revision in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[J6] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A 1-MHz 1.5-Stage LED Driver with Charge-Pump-Based Power Factor Correction," draft for IEEE Journal of Emerging and Selected Topics in Power Electronics.
[J7] C. K. Lumby, A. M. Ammar, Y. Nour, and A. Knott, "Switched-Capacitor Current Multiplier Front-End Converter for Power Factor Correction Applications," letter draft for IEEE Journal of Emerging and Selected Topics in Power Electronics.
[J8] N. J. Dahl, A. M. Ammar, and M. A. E. Andersen, "Identification of ZVS Points and Bounded Low-Loss Operating Regions in a Class-DE Resonant Converter," under revision in IEEE Transactions on Power Electronics.

## Conference Papers

[C1] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Miniaturization of LED Drivers," 6th International Workshop on Power Supply-On-Chip (PwrSoC), Hsinchu, 2018.
[C2] F. M. Spliid, A. M. Ammar, and A. Knott, "Stacked class E resonant Very High Frequency converter for European mains power factor correction," 6th International Workshop on Power Supply-On-Chip (PwrSoC), Hsinchu, 2018.
[C3] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A Series-Resonant Charge-PumpBased Rectifier with Inherent PFC Capability," 2019 IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, 2019.
[C4] A. M. Ammar, Y. Nour, and A. Knott, "A High-Efficiency 1 MHz 65 W GaN-Based LLC Resonant DC-DC Converter," 2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE), Aswan, 2019.
[C5] C. H. K. Jensen, R. B. Lind, J. C. Hertel, A. M. Ammar, A. Knott, M. A. E. Andersen, "A Time-Based Control Scheme for Power Factor Correction Boost Converter", 2019 IEEE Nordic Circuits and Systems Conference (NORCAS), Helsinki, 2019.
[C6] A. M. Ammar, K. Ali, and D. Rogers, "A Bidirectional GaN-Based CLLC Converter for PlugIn Electric Vehicles On-Board Charger," submitted to IECON 2020-46th Annual Conference of the IEEE Industrial Electronics Society.

## Bibliography

[1] J. M. Rivas, R. S. Wahby, J. S. Shafran and D. J. Perreault, "New Architectures for RadioFrequency DC-DC Power Conversion," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 380-393, March 2006.
[2] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Feb 2009, pp. 1-14.
[3] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. E. Andersen, "Evolution of Very High Frequency Power Supplies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sep. 2014.
[4] S. Jiang, X. Li, "Google 48 V Power Architecture," Proceedings of the IEEE Applied Power Electronics Conference (APEC), Tampa, FL, March 2017.
[5] F. C. Lee, P. Barbosa, Peng Xu, Jindong Zhang, Bo Yang and F. Canales, "Topologies and design considerations for distributed power system applications," in Proceedings of the IEEE, vol. 89, no. 6, pp. 939-950, June 2001.
[6] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd edition. Kluwer Academic Publishers, 2001.
[7] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[8] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[9] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," in IEEE Std 519-2014 (Revision of IEEE Std 519-1992), vol., no., pp.1-29, 11 June 2014.
[10] O. Garcia, J. A. Cobos, R. Prieto, P. Alou and J. Uceda, "Single phase power factor correction: a survey," in IEEE Transactions on Power Electronics, vol. 18, no. 3, pp. 749755, May 2003.
[11] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," in IEEE Transactions on Industrial Electronics, vol. 50, no. 5, pp. 962-981, Oct. 2003, doi: 10.1109/TIE.2003.817609.
[12] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters-An Overview," IEEE Transactions on Industry Applications, vol. 50, no. 5, pp. 3569-3578, Sep. 2014.
[13] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage," IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1430-1443, May 2011.
[14] W. Chen and S. Y. R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC LightEmitting Diode (LED) Driver With High Input Power Factor and Constant Output Current," IEEE Transactions on Power Electronics, vol. 27, no. 3, pp. 1598-1607, March 2012.
[15] S. Lim, D. M. Otten and D. J. Perreault, "New AC-DC Power Factor Correction Architecture Suitable for High-Frequency Operation," in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 2937-2949, April 2016.
[16] A. Khaligh and M. D'Antonio, "Global Trends in High-Power On-Board Chargers for Electric Vehicles," in IEEE Transactions on Vehicular Technology, vol. 68, no. 4, pp. 33063324, April 2019.
[17] J. Rivas, "Radio frequency dc-dc power conversion," Sc.D. thesis, Massachusetts Institute of Technology, 2007.
[18] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd edition. Wiley-IEEE Press, 2011.
[19] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," IEEE Journal of Solid-State Circuits, vol. 10, no. 3, pp. 168176, June 1975.
[20] J. C. Hertel, Y. Nour, and A. Knott, "Integrated Very-High-Frequency Switch Mode Power Supplies: Design Considerations," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 526-538, June 2018.
[21] J. A. Pedersen, M. P. Madsen, A. Knott, and M. A. E. Andersen, "Self-oscillating galvanic isolated bidirectional Very High Frequency DC-DC converter," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2015, pp. 1974-1978.
[22] T. M. Andersen, S. K. Christensen, A. Knott, and M. A. E. Andersen, "A VHF class E DCDC converter with self-oscillating gate driver," in 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), March 2011, pp. 885891.
[23] J. A. Pedersen, M. P. Madsen, J. D. Mønster, T. Andersen, A. Knott and M. A. E. Andersen, "US mains stacked Very High Frequency self-oscillating resonant power converter with unified rectifier," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 1842-1846.
[24] H. Koizumi, M. Iwadare, S. Mori, and K. Ikeda, "A class D type high frequency tuned power amplifier with class E switching conditions," in Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94, vol. 5, May 1994, pp. 105-108 vol.5.
[25] D. C. Hamill, "Class DE inverters and rectifiers for DC-DC conversion," in PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, vol. 1, June 1996, pp. 854860.
[26] Y. Nour, A. Knott, and L. P. Petersen, "High frequency soft switching half bridge seriesresonant DC-DC converter utilizing gallium nitride FETs," in 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Sep. 2017, pp. P.1-P.7.
[27] M. P. Madsen, A. Knott, and M. A. E. Andersen, "Very high frequency half bridge DC/DC converter," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, March 2014, pp. 1409-1414.
[28] J. D. Mønster, M. P. Madsen, J. A. Pedersen and A. Knott, "Investigation, development and verification of printed circuit board embedded air-core solenoid transformers," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 133-139.
[29] I. Moon, M. K. Ranjram, S. Chakraborty, and D. J. Perreault, "A Wide Operating Range Converter Using a Variable-Inverter-Rectifier-Transformer with Improved Step-Down Capability," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1575-1582, 2019.
[30] Y.-C. Li, F. C. Lee, Q. Li, X. Huang, and Z. Liu, "A novel AC-to-DC adaptor with ultra-high power density and efficiency," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, mar 2016, pp. 1853-1860.
[31] Z. Liu, R. Yu, T. Chen, Q. Huang and A. Q. Huang, "Real-time adaptive timing control of synchronous rectifiers in high frequency GaN LLC converter," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2214-2220.
[32] L. Gu, K. Surakitbovorn, G. Zulauf, S. Chakraborty and J. Rivas-Davila, "High-Frequency Bidirectional Resonant Converter for High Conversion Ratio and Variable Load Operation," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[33] L. Gu, W. Liang, L. C. Raymond, and J. Rivas-Davila, "27.12 MHz GaN bi-directional resonant power converter," in Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on, June 2015.
[34] S. C. Moon, C. Chen, and D. Park, "Adaptive Dead Time Synchronous Rectification Control for High Efficiency LLC Resonant Converter," in 2019 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, mar 2019, pp. 2939-2946.
[35] J. C. Hertel, J. E. F. Overgaard, I. H. H. Jørgensen, T. M. Andersen, M. Rødgaard and A. Knott, "Synchronous Rectifier for High-Frequency Switch Mode Power Supplies using Phase Locked Loops," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[36] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "3.3kW CLLC converter with synchronous rectification for plug-in electric vehicles," in 2017 IEEE Industry Applications Society Annual Meeting. IEEE, oct 2017, pp. 1-6.
[37] X. Ren, Y. Zhou, D. Wang, X. Zou, and Z. Zhang, "A $10-\mathrm{MHz}$ isolated synchronous class- $\phi 2$ resonant converter," Power Electronics, IEEE Transactions on, vol. 31, no. 12, pp. 8317-8328, Jan 2016.
[38] L. Gu, W. Liang and J. R. Davila, "Design of very-high-frequency synchronous resonant DC-DC converter for variable load operation," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 3447-3454.
[39] L. Gu, K. Surakitbovorn and J. Rivas-Davila, "High-Frequency Resonant Converter with Synchronous Rectification for High Conversion Ratio and Variable Load

Operation," 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), Niigata, 2018, pp. 632-638.
[40] M. Kovacevic, "Advances in Very High Frequency Power Conversion," Ph.D. thesis, Technical University of Denmark, 2015.
[41] M. P. Madsen, "Very High Frequency Switch-Mode Power Supplies," Ph.D. thesis, Technical University of Denmark, 2015.
[42] J. A. Pedersen, "Very High Frequency Galvanic Isolated Offline Power Supply," Ph.D. thesis, Technical University of Denmark, 2017.
[43] Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement, ISO DS/EN 55 022/A2:2011, 2011.
[44] M. P. Madsen, J. A. Pedersen, A. Knott, and M. A. E. Andersen, "Self-oscillating resonant gate drive for resonant inverters and rectifiers composed solely of passive components," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, March 2014, pp. 2029-2035.
[45] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri and D. J. Perreault, "A High-Frequency Resonant Inverter Topology With Low-Voltage Stress," in IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1759-1771, July 2008.
[46] J. M. Rivas, O. Leitermann, Y. Han and D. J. Perreault, " A Very High Frequency DC-DC Converter Based on a Class $\Phi_{2}$ Resonant Inverter," in IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 2980-2992, Oct. 2011.
[47] M. P. Madsen, M. Kovacevic, J. D. Mønster, J. A. Pedersen, A. Knott, and M. A. E. Andersen, "Input-output rearrangement of isolated converters," in 2015 IEEE Power and Energy Conference at Illinois (PECI), Feb 2015, pp. 1-6.
[48] M. Kovacevic, A. Knott and M. A. E. Andersen, "VHF series-input parallel-output interleaved self-oscillating resonant SEPIC converter," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 2052-2056.
[49] C. Nwosu and M. Eng, "State-space averaged modeling of a nonideal boost converter," The pacific journal of science and Technology, vol. 2, no. 9, pp. 1-7, 2008.
[50] S. R. Sanders and G. C. Verghese, "Synthesis of averaged circuit models for switched power converters," IEEE Transactions on Circuits and systems, vol. 38, no. 8, pp. 905915, 1991.
[51] K. Mandal, S. Banerjee, C. Chakraborty, and M. Chakraborty, "Bifurcations in frequency controlled load resonant DC-DC converters," in 2012 IEEE International Symposium on Circuits and Systems, pp. 1135-1138, IEEE, 2012.
[52] O. Dranga, B. Buti, and I. Nagy, "Stability analysis of a feedback-controlled resonant DCDC converter," IEEE Transactions on Industrial Electronics, vol. 50, no. 1, pp. 141-152, 2003.
[53] P. C. Luk, S. Aldhaher, W. Fei, and J. F. Whidborne, "State-Space Modeling of a Class E2 Converter for Inductive Links," IEEE Transactions on Power Electronics, vol. 30, pp. 3242-3251, June 2015.
[54] J. Kwon, X. Wang, F. Blaabjerg, C. L. Bak, A. R. Wood, and N. R. Watson, "Linearized modeling methods of AC-DC converters for an accurate frequency response," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 15261541, 2017.
[55] R. Z. Scapini, L. V. Bellinaso, and L. Michels, "Stability analysis of half-bridge rectifier employing LTP approach," in IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society, pp. 780-785, IEEE, 2012.
[56] G. N. Love and A. R. Wood, "Harmonic state space model of power electronics," in 2008 13th International Conference on Harmonics and Quality of Power, pp. 1-6, IEEE, 2008.
[57] V. Salis, A. Costabeber, S. M. Cox, and P. Zanchetta, "Stability assessment of power-converter-based ac systems by LTP theory: eigenvalue analysis and harmonic impedance estimation," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1513-1525, 2017.
[58] V. Salis, A. Costabeber, S. M. Cox, A. Formentini, and P. Zanchetta, "Stability Assessment of High-Bandwidth DC Voltage Controllers in Single-Phase Active Front Ends: LTI Versus LTP Models," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 4, pp. 2147-2158, 2018.
[59] S. Sanders and J. Noworolski, "Generalized averaging method for power conversion circuits," IEEE Transactions on Power Electronics, vol. 6, no. 2, 1991.
[60] M. F. Menke, A'. R. Seidel, and R. V. Tambara, "LLC LED Driver Small-Signal Modeling and Digital Control Design for Active Ripple Compensation," IEEE Transactions on Industrial Electronics, vol. 66, no. 1, pp. 387-396, 2019.
[61] P. Wang, C. Liu, and L. Guo, "Modeling and simulation of full-bridge series resonant converter based on generalized state space averaging," in Applied Mechanics and Materials, vol. 347, pp. 1828-1832, Trans Tech Publ, 2013.
[62] C. Buccella, C. Cecati, H. Latafat, P. Pepe, and K. Razi, "Observer-Based Control of LLC DC/DC Resonant Converter Using Extended Describing Functions," IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5881-5891, 2015.
[63] C. Fei, F. Lee, and Q. Li, "Digital implementation of soft start-up and short-circuit protection for high-frequency LLC converters with optimal trajectory control (otc)," IEEE Transactions on Power Electronics, vol. PP, no. 99, pp. 1-1, 2016.
[64] W. Feng, F. C. Lee, and P. Mattavelli, "Simplified optimal trajectory control (sotc) for Ilc resonant converters," IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 24152426, May 2013.
[65] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for Ilc resonant converter," in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06., March 2006.
[66] M. Kovacevic and M. Madsen, "Burst mode control," 9 2015, wO2015128398; H02M 1/ 00 Al .
[67] M. Madsen and M. Kovacevic, "On and off controlled resonant dc-dc power converter," 9 2015, also published as: TW201607226 (A) ; WO2015128397; H03F 3/ 217 A I.
[68] M. Kovacevic, A. Knott, and M. A. E. Andersen, "A vhf interleaved self-oscillating resonant sepic converter with phase-shift burst-mode control," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, March 2014, pp. 1402-1408.
[69] M. P. Madsen, A. Knott, M. A. E. Andersen, and D. J. Perreault, "Outphasing control of gallium nitride based very high frequency resonant converters," in 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), July 2015, pp. 17.
[70] D. J. Perreault, "A new architecture for high-frequency variable-load inverters," in 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), June 2016, pp. 1-8.
[71] Y. Jang and M. M. Jovanovic, "A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization," in IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 85-93, Jan. 2009.
[72] R. Fernandes and O. Trescases, "A Multimode 1-MHz PFC Front End With Digital Peak Current Modulation," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 56945708, Aug. 2016.
[73] J. P. M. Figueiredo, F. L. Tofoli and B. L. A. Silva, "A review of single-phase PFC topologies based on the boost converter," 2010 9th IEEE/IAS International Conference on Industry Applications - INDUSCON 2010, Sao Paulo, 2010, pp. 1-6.
[74] L. Huber, L. Gang and M. M. Jovanovic, "Design-Oriented Analysis and Performance Evaluation of Buck PFC Front End," in IEEE Transactions on Power Electronics, vol. 25, no. 1, pp. 85-94, Jan. 2010.
[75] X. Wu, J. Yang, J. Zhang and M. Xu, "Design Considerations of Soft-Switched Buck PFC Converter With Constant On-Time (COT) Control," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3144-3152, Nov. 2011.
[76] X. Xie, C. Zhao, L. Zheng and S. Liu, "An Improved Buck PFC Converter With High Power Factor," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2277-2284, May 2013.
[77] Y. Ohnuma and J. Itoh, "A Novel Single-Phase Buck PFC AC-DC Converter With Power Decoupling Capability Using an Active Buffer," in IEEE Transactions on Industry Applications, vol. 50, no. 3, pp. 1905-1914, May-June 2014.
[78] M. A. Al-Saffar, E. H. Ismail and A. J. Sabzali, "Integrated Buck-Boost-Quadratic Buck PFC Rectifier for Universal Input Applications," in IEEE Transactions on Power Electronics, vol. 24, no. 12, pp. 2886-2896, Dec. 2009.
[79] Y. Li and C. Chen, "A Novel Primary-Side Regulation Scheme for Single-Stage High-Power-Factor AC-DC LED Driving Circuit," in IEEE Transactions on Industrial Electronics, vol. 60, no. 11, pp. 4978-4986, Nov. 2013.
[80] C. Zhao, J. Zhang and X. Wu, "An Improved Variable On-Time Control Strategy for a CRM Flyback PFC Converter," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 915-919, Feb. 2017.
[81] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," in IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 873-881, March-April 2011.
[82] B. Poorali and E. Adib, "Analysis of the Integrated SEPIC-Flyback Converter as a SingleStage Single-Switch Power-Factor-Correction LED Driver," in IEEE Transactions on Industrial Electronics, vol. 63, no. 6, pp. 3562-3570, June 2016.
[83] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1381-1390, May 2008.
[84] F. Musavi, W. Eberle, and W. G. Dunford, "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," IEEE Transactions on Industry Applications, vol. 47, no. 4, pp. 1833-1843, July 2011.
[85] W. Choi, J. Kwon, E. Kim, J. Lee, and B. Kwon, "Bridgeless Boost Rectifier With Low Conduction Losses and Reduced Diode Reverse-Recovery Problems," IEEE Transactions on Industrial Electronics, vol. 54, no. 2, pp. 769-780, April 2007.
[86] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 799807, Sep. 2016.
[87] A. J. Hanson and D. J. Perreault, "A high frequency power factor correction converter with soft switching," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2018, pp. 2027-2034.
[88] A. J. Hanson and D. J. Perreault, "A High-Frequency Power Factor Correction Stage with Low Output Voltage," IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1-1, 2019.
[89] N. Jain, P. K. Jain, and G. Joos, "A zero voltage transition boost converter employing a soft switching auxiliary circuit with reduced conduction losses," IEEE Transactions on Power Electronics, vol. 19, no. 1, pp. 130-139, Jan 2004.
[90] Y. Jang, M. M. Jovanovi, and D. L. Dillman, "Soft-Switched PFC Boost Rectifier With Integrated ZVS Two-Switch Forward Converter," IEEE Transactions on Power Electronics, vol. 21, no. 6, pp. 1600-1606, Nov 2006.
[91] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor correction techniques for high-power applications - an overview," IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 701-708, June 2005.
[92] Z. Liao, N. C. Brooks, Z. Ye, and R. C. N. Pilawa-Podgurski, "A high power density power factor correction converter with a multilevel boost front-end and a series-stacked energy decoupling buffer," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2018, pp. 7229-7235.
[93] S. Qin, Y. Lei, Z. Ye, D. Chou, and R. C. N. Pilawa-Podgurski, "A high-power-density power factor correction front end based on seven-level flying capacitor multilevel converter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1883-1898, Sep. 2019.
[94] E. Candan, A. Stillwell, N. C. Brooks, R. A. Abramson, J. Strydom, and R. C. N. PilawaPodgurski, "A 6-level flying capacitor multi-level converter for single phase buck-type power factor correction," in 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2019, pp. 1180-1187.
[95] J. Sasiluk and J. Kamon, "The electronic ballast using Class-E rectifier with tapped inductor for power factor correction," 2008 International Symposium on Intelligent Signal Processing and Communications Systems, Bangkok, 2009, pp. 1-4.
[96] S. Mangkalajan, C. Ekkaravarodome, K. Jirasereeamornkul, P. Thounthong, K. Higuchi and M. K. Kazimierczuk, "A Single-Stage LED Driver Based on ZCDS Class-E CurrentDriven Rectifier as a PFC for Street-Lighting Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8710-8727.
[97] K. Jirasereeamornkul, M. K. Kazimierczuk, I. Boonyaroonate and K. Chamnongthai, "Single-stage electronic ballast with class-E rectifier as power-factor corrector," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 53, no. 1, pp. 139-148, Jan. 2006.
[98] W. Chen, F. C. Lee and T. Yamauchi, "An improved "charge pump" electronic ballast with Iow THD and low crest factor," in IEEE Transactions on Power Electronics, vol. 12, no. 5, pp. 867-875, Sept. 1997.
[99] Jinrong Qian, F. C. Lee and T. Yamauchi, "Charge pump power-factor-correction dimming electronic ballast," in IEEE Transactions on Power Electronics, vol. 14, no. 3, pp. 461-468, May 1999.
[100] J. Qian, F. C. Lee and T. Yamauchi, "Analysis, design and experiments of a high power factor electronic ballast," Proceedings of APEC 97 - Applied Power Electronics Conference, Atlanta, GA, USA, 1997, pp. 1023-1029 vol.2.
[101] Jinrong Qian, F. C. Lee and T. Yamauchi, "Analysis, design, and experiments of a high-power-factor electronic ballast," in IEEE Transactions on Industry Applications, vol. 34, no. 3, pp. 616-624, May-June 1998.
[102] C. Ekkaravarodome, V. Chunkag, K. Jirasereeamornkul, and M. K. Kazimierczuk, "ClassD Zero-Current-Switching Rectifier as Power-Factor Corrector for Lighting Applications," IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4938-4948, 2014.
[103] C. Ekkaravarodome, K. Jirasereeamornkul, and M. K. Kazimierczuk, "Implementation of a DC-Side Class-DE Low-dv/dt Rectifier as a PFC for Electronic Ballast Application," IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5486-5497, 2014.
[104] R. Kathiresan, P. Das, T. Reindl and S. K. Panda, "A Novel ZVS DC-DC Full-Bridge Converter With Hold-Up Time Operation," in IEEE Transactions on Industrial Electronics, vol. 64, no. 6, pp. 4491-4500, June 2017.
[105] Y. Kim, K. Cho, D. Kim and G. Moon, "Wide-Range ZVS Phase-Shift Full-Bridge Converter With Reduced Conduction Loss Caused by Circulating Current," in IEEE Transactions on Power Electronics, vol. 28, no. 7, pp. 3308-3316, July 2013.
[106] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy and P. L. So, "A New ZVS Full-Bridge DC-DC Converter for Battery Charging With Reduced Losses Over Full-Load Range," in IEEE Transactions on Industry Applications, vol. 54, no. 1, pp. 571-579, Jan.-Feb. 2018.
[107] A. M. Garcia, M. J. Kasper, and M. Schlenk, "Asymmetrical flyback converter in high density SMPS," in PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management. VDE, 2018, pp. 1475-1479.
[108] L. Xue and J. Zhang, "Design Considerations of Highly-Efficient Active Clamp Flyback Converter Using GaN Power ICs," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 777-782, 2018.
[109] X. Huang, J. Feng, W. Du, F. C. Lee, and Q. Li, "Design consideration of MHz active clamp flyback converter with GaN devices for low power adapter application," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, mar 2016, pp. 23342341.
[110] Bo Yang, F. C. Lee, A. J. Zhang and Guisong Huang, "LLC resonant converter for front end DC/DC conversion," APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, USA, 2002, pp. 1108-1112 vol.2.
[111] M. Li, Z. Ouyang and M. A. E. Andersen, "High frequency LLC resonant converter with magnetic shunt integrated planar transformer," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2678-2685.
[112] W. Feng, P. Mattavelli, F. C. Lee, and D. Fu, "LLC converters with automatic resonant frequency tracking based on synchronous rectifier (SR) gate driving signals," Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, pp. 15, 2011.
[113] J. Deng, S. Li, S. Hu, C. C. Mi and R. Ma, "Design Methodology of LLC Resonant Converters for Electric Vehicle Battery Chargers," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1581-1592, May 2014.
[114] P. He and A. Khaligh, "Comprehensive Analyses and Comparison of 1 kW Isolated DCDC Converters for Bidirectional EV Charging Systems," in IEEE Transactions on Transportation Electrification, vol. 3, no. 1, pp. 147-156, March 2017.
[115] J. Jung, H. Kim, M. Ryu and J. Baek, "Design Methodology of Bidirectional CLLC Resonant Converter for High-Frequency Isolation of DC Distribution Systems," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1741-1755, April 2013.
[116] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen and J. Lai, "Design of Bidirectional DC-DC Resonant Converter for Vehicle-to-Grid (V2G) Applications," in IEEE Transactions on Transportation Electrification, vol. 1, no. 3, pp. 232-244, Oct. 2015.
[117] M. Ekhtiari, T. Andersen, M. A. E. Andersen and Z. Zhang, "Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 783-793, Jan. 2017.
[118] F. M. Spliid, "Efficient Resonant Converters for Power Factor Correction in Solid State Lighting Applications," Ph.D. thesis, Technical University of Denmark, 2020.
[119] 6.6 kW Bi-Directional EV On-Board Charger, Cree Power Applications, Application Note CPWR-AN25, Rev B, July 2018.
[120] B. Li, Q. Li, F. C. Lee, Z. Liu and Y. Yang, "A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1627-1636, Sept. 2018.
[121] A. Hopkins, N. McNeill, P. Anthony and P. Mellor, "Figure of merit for selecting superjunction MOSFETs in high efficiency voltage source converters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 3788-3793.
[122] F. Udrea, G. Deboy and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 713-727, March 2017.
[123] G. Deboy, O. Haeberlen and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 89-100, 2017.
[124] Y. Nour, Z. Ouyang, A. Knott and I. H. H. Jørgensen, "Design and implementation of high frequency buck converter using multi-layer PCB inductor," IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1313-1317.
[125] Y. Nour, A. Knott and I. H. H. Jørgensen, "Investigating enhancement mode gallium nitride power FETs in high voltage, high frequency soft switching converters," 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, 2016, pp. 1-5.
[126] Ferroxcube material datasheet https://www.ferroxcube.com/upload/media/design/FXCStainmetzCoefficients.xls.
[127] Micrometals material datasheet https://micrometalsarnoldpowdercores.com/pdf/mix/Mix-6-DataSheet.pdf.
[128] "Hitachi Metals Creates New Soft Ferrite Core Material with Outstanding HighFrequency Characteristics," Hitachi Metals Ltd., Press release, 2016.
[129] Bosheng Sun, "AC cycle skipping improves PFC light-load efficiency," Analog Applications Journal, Texas Instruments, 3Q 2014.
[130] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski, and P. K. Hanumolu, "A 4Phase $30-70 \mathrm{MHz}$ Switching Frequency Buck Converter Using a Time-Based Compensator," IEEE Journal of Solid-State Circuits, vol. 50, no. 12, December 2015.
[131] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High Frequency Buck Converter Design Using TimeBased Control Techniques," IEEE Journal of Solid State Circuits, vol. 50, no. 4, pp. 9901001, April 2015.
[132] S. J. Kim, W. Choi, R. Pilawa-Podgurski, and P. K. Hanumolu, "A $10 \mathrm{MHz} 2-800-\mathrm{mA} 0.5-$ 1.5-V 90\% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes," IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 814824, March 2018.
[133] J. C. Hertel, "High Efficiency Synchronous Rectifier using Phase Locked Loops," Ph.D. thesis, Technical University of Denmark, 2019.

## Appendix A

## Prototyping Setup

As resonant converters are built of separate compatible inverters and rectifiers blocks, as shown in Figure 2.1 it is of interest to experiment with different configurations for the switchnetwork, the resonant tank, and/or the rectifier network in the design phase, in order to conclude the gain of the different topologies for a specific application. For example, nine different converters can be built from a set of three inverters and three rectifiers. A practice employed in design and implementation process for the different prototypes in this thesis is to build mockups of different converters and obtain preliminary experimental results for a given set of specifications. Following, a custom PCB design with high power density is conducted for the optimal design choice based on the obtained measurement data.

In order to aid with this procedure, a modular prototyping setup is implemented with separate modules for the different converter peripherals, including the input filter, the switching network, the resonant tank, and the rectifier network. Figure A. 1 shows the modular resonant converter test platform, where daughter boards of the different modules are connected together on a mother board that hosts the testing terminals and connection to control signals. The control signals can be provided through connectors to a waveform generator or from a control daughter board.


Figure A.0.1: Modular resonant converter test platform.

The setup shown greatly facilitated the design and prototyping process, where different versions of each module are developed with variants of the switching devices, magnetic materials, rectifier diodes, and controller designs. That resulted in quick and educated design decisions based on experimental validation of different variants of the same converter through simple plug-and-play measurement process.

## Lab Setup



Figure A.2: Lab Setup.

Figure A. 2 shows the lab setup used for the validation of the different prototypes presented in this thesis. The case of testing AC-DC PFC converters is described here as it is the one with highest allocation of lab equipment. A thermal camera (Flir T650SC) continuously monitors the converter under test for validation of thermal stability and detection of failure mechanisms. A 1-GHz oscilloscope (LeCroy Wavesurfer 104MXS-B displays the switchingfrequency waveforms including the switching node voltage, resonant tank current, and gatesignals showing the implemented dead time, which provides in depth evaluation of ZVS operation and the different switching-loss modes. A $200-\mathrm{MHz}$ oscilloscope (LeCroy Wavesurfer 24 X s-A) is used to display the line-frequency waveforms, including the input voltage and current, the output voltage, and if needed the DC-bus voltage. This gives insight into PFC operation through the inspection of the input current waveform with respect to the input voltage in terms of the harmonic content and phase difference. In addition, the double-the-line frequency ripple can be determined, as well as the voltage stress on the energystorage capacitor in charge-pump-based converters. A low-voltage DC power supply (Rhode \& Schwartz HMP2020) supplies the driving circuit, and a high-voltage AC power supply (Keysight AC6802A) emulates the AC mains. A $120-\mathrm{MHz}$ dual-channel waveform generator (Keysight 33622A) generates the driving circuit signals. A DC electronic load (Itech IT8812B) acts as an active load for the converter under test. Finally, a precision power analyzer (N4L PPA5530) measures the efficiency, power factor, displacement factor, THD, and the magnitudes of the input current harmonics.

## Appendix [P1]

A. M. Ammar, Y. Nour, and A. Knott, "AC-DC Power Converter with Power Factor Correction", patent pending, December 2019.

## AC-DC POWER CONVERTER WITH POWER FACTOR CORRECTION

## FIELD OF THE INVENTION

The present invention relates to an AC-DC power converter which comprises a res- onant DC-DC converter and a charge pump circuit. The charge pump circuit is configured to perform power factor correction of the converter by drawing current pulses at a switching frequency of the converter from an AC line voltage such that electrical charges of the current pulses vary substantially proportionally to instantaneous amplitude of the AC line voltage.

## BACKGROUND OF THE INVENTION

The present AC-DC power converters may be applied to power factor correcting ACDC power converters in numerous applications. A high power factor is generally required or at least highly desirable in a power delivery system to reduce power losses and reduce distortion introduced to the AC grid by input current harmonics. In case the power system is loaded by a nonlinear load, e.g. switching converter, current drawn by the load is interrupted by a switching activity and therefore contains numerous higher frequency components that are multiples of the power system frequency. Such harmonic distortion reduces average power transferred to a load of the AC-DC power converter in addition to contaminating the AC grid. Power factor correction brings the power factor of a power circuit closer to 1 by making the load appear more resistive to the AC grid. Thus, achieving a close-to-sinusoidal line current that is substantially proportional to, and substantially in-phase with, the AC gridvoltage.

The skilled person will understand that the AC-DC power converters disclosed herein may be utilized in a wide range of applications and product categories, including laptop chargers, LED drivers, other adapters and power supplies for various industrial and consumer electronics. Thus, the AC-DC power converters disclosed herein meet an increasing demand for smaller, more power or energy efficient and longer living AC-DC converters. The present AC-DC power converter design solves these and other problems by a charge pump based Power Factor Correction (PFC). The present AC-DC converter may for example use soft-switching inverter topologies
and state-of-the-art devices such as wide bandgap semiconductors and relevant magnetic materials as discussed below in additional detail.

With the current trend towards smaller and highly portable electronic equipment for consumer and industrial applications it is important to minimize weight and size of the equipment without sacrificing performance. One application of the present ACDC converter with a great demand for miniaturization is offline power converters. Conventional offline converters are 2-stage architectures wherein the first stage is an AC-DC power factor correction (PFC) rectifier followed by an energy storage capacitor to filter the double-the-line frequency component on the output, while the second stage is a DC-DC converter providing the voltage and current levels conforms to load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current to limit the mains voltage distortion [1], [2].

Pulse-width-modulated (PWM) converters have been the primary candidate for the AC-DC stage in offline converters, including step-down converters, step-up converters, buck-boost converters, flyback converters and single-ended primary-inductor converter (SEPIC). These prior art converter topologies can provide high power factor, but generally suffer from several pronounced problems such as high conducted electromagnetic interference (EMI) from rectangular switching waveforms. Another problem associated with prior art converter topologies is hard-switching operation which typically leads to severe switching losses, low overall energy efficiency, severe EMI problems, relatively low switching frequencies and voltage stress, dv/dt, problems etc.

On the other hand, resonant inverters and converters typically have substantially lower switching losses than their PWM counterparts. The resonant inverters of ACDC power converters in accordance with the present invention may therefore be configured to provide zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) to provide high power conversion efficiencies at high switching frequencies for example switching frequencies above 750 kHz or above 1 MHz . That in turn results in reduced sizes of passive electrical components and thus higher power densities, higher loop-gain bandwidths and faster transient responses. The resonant
inverters and converters typically allow incorporation of high frequency transformers in the resonant tank or circuit. The latter allows galvanic isolation, in addition to offering different output voltages. That, in turn, can help combine the AC-DC with the following DC-DC stage for a single-stage solution for the present offline converters.

## SUMMARY OF THE INVENTION

A first aspect of the invention relates to an AC-DC power converter which comprises an AC rectification circuit configured to convert an AC line voltage into a rectified line voltage and a rectifying element connected between the rectified line voltage and a DC supply voltage of a resonant DC converter. The resonant DC converter comprises a resonant inverter configured to convert the DC supply voltage into a resonant inverter voltage at a fixed or controllable switching frequency and an output rectification circuit configured to generate a DC output voltage from the resonant voltage or generate a DC output current from the resonant voltage for supply to a converter load such as an LED lamp assembly. The AC-DC power converter additionally comprises a charge pump circuit connected to the rectified line voltage and the resonant inverter voltage. The charge pump circuit is configured to draw current pulses at the fixed or controllable switching frequency from the AC line voltage wherein electrical charges of the current pulses vary proportionally to, or at least substantially proportionality to, an instantaneous amplitude of the AC line voltage.

The skilled person will understand that the charge pump circuit may operate in an open loop manner and therefore does not require any separate regulation loop or mechanism to carry out the power factor correction of the line current drawn from the AC line voltage or mains voltage. Hence, the AC-DC power converter may comprise merely a single feedback regulation loop to adjust the DC output voltage or DC output current despite the integrated power factor correction (PFC) mechanism provided by the charge pump circuit. The AC-DC power converter may for example comprise a voltage or current regulation loop configured to adjust the DC output voltage or DC output current in accordance with a DC reference voltage or a DC reference current. The adjustment of the DC output voltage or DC output current may be achieved by controlling the switching frequency of the resonant inverter,
which is also the switching frequency of the resonant DC-DC converter, as discussed in additional detail below with reference to the appended drawings.

Other embodiments of the AC-DC power converter may have a substantially fixed switching frequency and the adjustment of the DC output voltage or DC output current may be achieved by duty cycle control, i.e. on/off control, of the switch control signal which may be PWM modulated.

The resonant inverter may comprise a series resonant network or tank, a parallel resonant network or tank or a combination of both. In each case, the resonant network or tank may comprise at least an inductor and a capacitor to set a resonance frequency. The resonance frequency may lie between 100 kHz and 300 MHz , for example above 750 kHz , and tuned to coincide with the switching frequency of the resonant DC-DC converter, which therefore also may lie between 100 kHz and 300 MHz . The skilled person will understand that properties of active components of the AC-DC power converter, such as transistors, and passive components, such as the inductor and capacitor of the resonant network, to may be tailored to a specific switching frequency or switching frequency range.

The skilled person will understand that the resonant inverter may have any of numerous well-known topologies such as a topology selected from the group \{class E , class F, class DE, class EF, LLC\}. Some embodiments of the AC-DC power converter may comprise a galvanic isolation barrier, e.g. a transformer with a certain conversion ratio, to step-up or step-down the resonant inverter voltage. The transformer may provide galvanic isolation between primary side circuitry and secondary side circuitry of the AC-DC power converter. The galvanic isolation barrier may be coupled between the resonant output voltage and an input voltage of the output rectification circuit.

According to one embodiment of the AC-DC power converter, the charge pump circuit comprises a smoothing capacitor connected to the DC supply voltage of the resonant inverter and a pump capacitor, or flying capacitor, connected from the resonant inverter voltage to the rectified line voltage. The circuit topology of the AC -DC power converter ensures that the charge variation of the pump capacitor, which is
proportional to the voltage variation across the pump capacitor, follows the AC line voltage across the $50 / 60 \mathrm{~Hz}$ line cycle. Accordingly, the average input or line current drawn by the AC-DC power converter substantially follows the AC line voltage and a unity power factor can ideally be obtained even though minor component and circuit imperfections may leave the power factor slightly below unity. The charge pump circuit may be configured such that the proportionality between the electrical charges of the current pulses and the instantaneous amplitude of the AC line voltage leads to a power factor exceeding 0.95 , and more preferably exceeds 0.98 , for example exceeding 0.99 as evidenced by the experimental results discussed in detail below with reference to the appended drawings.

According to certain embodiments of the invention, the electrical interconnection between the rectified line voltage and resonant inverter voltage is based on a capacitor only network, for example exclusively by the pump capacitor. This provides a compact and low-cost connection that may be based on standard, low cost and readily available capacitors. The electrical interconnection may therefore avoid the use of an inductive coupling or an inductive component of the below-discussed galvanic isolation transformer, such as a separate transformer winding, back to the rectified line voltage.

The charge pump circuit may be configured to, during a cycle of the switching frequency, sequentially cycle through states of:

- a first state where each of the rectifying element $\left(D_{p}\right)$ and AC rectification circuit $\left(\mathrm{D}_{\mathrm{B}}\right)$ is non-conducting/off and a voltage across the pump/flying capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$ remains substantially constant;
- a second state where AC rectification circuit $\left(D_{B}\right)$ is conducting/on and the rectifying element $\left(D_{p}\right)$ is non-conducting/off to charge the pump/flying capacitor $\left(C_{P}\right)$ by line current drawn from the AC line voltage;
- a third state where each of the rectifying element $\left(D_{p}\right)$ and $A C$ rectification circuit $\left(\mathrm{D}_{\mathrm{B}}\right)$ is non-conducting/off and the voltage across the pump/flying capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$ remains substantially constant;
- a fourth state where the AC rectification circuit $\left(D_{B}\right)$ is in a non-conducting/off state and the rectifying element $\left(D_{p}\right)$ is in a conducting/on state such that discharge current flows from the pump/flying capacitor $\left(\mathrm{C}_{P}\right)$ into the smoothing capacitor $\left(\mathrm{C}_{\mathrm{DC}}\right)$ to
increase the DC supply voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ of the resonant inverter and decrease the voltage across the pump/flying capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$.

The charge pump circuit may be configured to cycle through its second state during a rising edge of a waveform of the resonant inverter voltage; and cycle through its fourth state during a falling edge of the waveform of the resonant inverter voltage as discussed in additional detail below with reference to the appended drawings.

According to one embodiment, a capacitance of the smoothing capacitor and a capacitance of the pump/flying capacitor are selected such that the DC supply voltage of the resonant inverter is higher than the AC line voltage across every cycle of the AC line voltage. An advantage of the latter selection of respective capacitances of the smoothing capacitor and pump capacitor is that it prevents cross conduction between $A C$ line voltage source and the DC supply voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ of the resonant DC-DC converter.

The AC-DC power converter preferably comprises a voltage regulation loop or current regulation loop configured to adjust the DC output voltage (Vout) or DC output current, respectively, in accordance with a DC reference voltage or a DC reference current. The voltage or current regulation loop may be configured to:

- adjust the DC output voltage or DC output current by adjusting or controlling the switching frequency, i.e. frequency modulation control, and/or
- adjust the DC output voltage ( $\mathrm{V}_{\text {Out }}$ ) or DC output current by off/on modulation or duty cycle modulation of the switching frequency. Hence, in the latter embodiment, the switching frequency of AC-DC power converter may be fixed and the AC-DC power converter turned-on and turned-off at a certain control frequency.

According to one embodiment, the voltage or current regulation loop may be configured to adjust the switching frequency of the AC-DC power converter with more than +/- $5 \%$, or even more than +/- $10 \%$, relative to a nominal switching frequency of the AC-DC power converter. The nominal switching frequency may be identical to the resonance frequency of the resonant network or a predetermined off-set relative to resonance frequency of the resonant network.

The resonant inverter preferably comprises at least one semiconductor switch connected between the DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ) and a negative supply rail. The at least one semiconductor switch may comprise one or more wide bandgap transistors such as one or more gallium nitride FET(s). The resonant inverter may comprise controllable switch network such as a half-bridge driver comprising a pair of wide bandgap transistors. A switch signal, at the fixed or controllable switching frequency, may be applied to a control terminal, e.g. a gate terminal, of the least one semiconductor switch of the resonant inverter. An output terminal of the controllable switch network may be connected to a first end of the resonant network.

The resonant inverter may comprise a controllable switch network exhibiting a topology selected from a group of: class DE, Class E, class EF, LLC.

The resonant inverter may be configured for zero voltage switching (ZVS) and/or zero current switching (ZCS). The output rectification circuit of the DC-DC converter may be configured for zero voltage switching (ZVS) and/or zero current switching (ZCS).
The output rectification circuit of the DC-DC converter may comprise one or more passive diodes, such as silicon carbide Schottky diode(s), or one more active/controllable diodes such as one or more transistors such as at least one MOSFET.

A second aspect of the invention relates to a method of applying power factor correction to an AC-DC power converter using a charge pump circuit, said method comprising steps of: -converting an $A C$ line voltage into a rectified line voltage $\left(V_{B}\right)$; -applying the rectified line voltage $\left(\mathrm{V}_{B}\right)$ to a DC supply voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ of a resonant DC-DC converter through a rectifying element $\left(D_{p}\right)$, such as a semiconductor diode; -generating a resonant inverter voltage by switching a resonant inverter at a fixed or controllable switching frequency;
-rectifying the resonant inverter voltage to generate a DC output voltage or generate a DC output current;
-drawing charging pulses, at the switching frequency, from the AC line voltage into a pump or flying capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$ connected between the rectified line voltage $\left(\mathrm{V}_{\mathrm{B}}\right)$ and
the resonant inverter voltage, wherein electrical charges of the charging pulses vary substantially proportionally to an instantaneous amplitude of the AC line voltage; -discharging the pump or flying capacitor into a smoothing capacitor, connected to the DC supply voltage, by supplying current pulses, at the switching frequency, into the smoothing capacitor.

The skilled person will understand that present methodology may comprise that the charge pump circuit sequentially cycles through the previously discussed first, second, third and fourth states during every cycle of the switching frequency.

## BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention will be described in more detail in connection with the appended drawings, in which:

FIG. 1 is a top-level block diagram of AC-DC power converters in accordance with the invention,

FIG. 2 is a simplified electrical circuit diagram of a class-DE series resonant converter of the AC-DC power converter,
FIG. 2A shows block diagrams of various exemplary embodiments of AC-DC power converters in accordance with the invention,
FIG. 3 is a simplified equivalent diagram of the charge pump circuit of the AC-DC power converter,

FIG. 4 is a simplified electrical diagram of a first exemplary embodiment of the ACDC power converter based on a class-DE converter and a charge-pump circuit, FIG. 4A is a simplified electrical diagram of a second exemplary embodiment of the AC-DC power converter based on a class-DE converter and a charge-pump circuit, FIG. 5 shows low-frequency operation of the charge pump circuit across a half-line cycle, 50 Hz , of the mains line voltage inputted to the AC-DC power converter, FIG. 6 illustrates high frequency operation of an exemplary embodiment of the ACDC power converter across two switching cycles of the switching frequency of the class DE resonant converter,

FIG. 7 shows simulation results for the mains line current and mains voltage input of the exemplary embodiment of the AC-DC power converter,
FIG. 8 shows simulated waveforms of various internal voltages and currents of the exemplary embodiment of the AC-DC power converter,

FIG. 9 shows simulated losses of an exemplary inductor of a resonant network of the class-DE converter,

FIG. 10 simulated core losses at 1 MHz of the exemplary inductor of the resonant network of the class-DE converter

FIG. 11 - upper plot shows measured output power and conversion efficiency of an experimental prototype AC-DC power converter across its operational frequency range from 960 kHz to 1040 kHz ,
FIG. 11 - lower plot shows measured PFC results of the experimental prototype ACDC power converter across its operational frequency range from 960 kHz to 1040 kHz,

FIG. 12 shows measured harmonics distribution of the mains line current at full-load operation and half-load operation of the experimental prototype AC-DC power converter,
FIG. 13 shows line-frequency time domain waveforms of the experimental prototype AC-DC power converter; and
FIG. 14 shows measured harmonics distribution of the mains line current for the experimental prototype AC-DC power converter at 120 V_RMS and 230 V_RMS line voltage inputs.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following, various exemplary embodiments of the present AC-DC power converter are described with reference to the appended drawings. The skilled person will understand that the accompanying drawings are schematic and simplified for clarity and therefore merely show details which are essential to the understanding of the invention, while other details have been left out. Like reference numerals refer to like elements or components throughout. Like elements or components will therefore not necessarily be described in detail with respect to each figure. It will further be appreciated that certain actions and/or steps may be described or depicted in a particular order of occurrence while those skilled in the art will understand that such specificity with respect to sequence is not actually required.

FIG. 1 shows a simplified block diagram of the present AC/DC power converter 100. The AC/DC power converter 100 comprises an AC rectification circuit (101) which is coupled to an AC line voltage ( $\mathrm{V}_{\mathbb{I N}}$ ) which may deliver AC mains voltages like 230
$\mathrm{V} / 50 \mathrm{~Hz}$ or $110 \mathrm{~V} / 60 \mathrm{~Hz}$. The AC rectification circuit (101) may include a mains input filter as illustrated below. The AC rectification circuit (101) is configured to convert the AC line voltage $\mathrm{V}_{\text {IN }}$ into a rectified line voltage $\left(\mathrm{V}_{\mathrm{B}}\right)$. The AC/DC power converter 100 additionally comprises a charge pump circuit (103), which preferably included a smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ), and class DE resonant converter (105). The smoothing capacitor $\left(\mathrm{C}_{D C}\right)$ is connected to the DC supply voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ of the resonant inverter (101). The resonant converter (105) is configured to convert the DC supply voltage $\left(V_{D C}\right)$ firstly into a resonant inverter voltage (illustrated below) at a fixed or adjustable switching frequency. Secondly, an output rectification circuit (not shown) of the resonant converter (105) generates a DC output voltage ( $\mathrm{V}_{\text {OUT }}$ ) of the AC/DC power converter 100 by rectifying the resonant inverter voltage. A schematically illustrated converter load ( $R_{\mathrm{L}}$ ), such as a LED lamp assembly, is connected to the DC output voltage $\left(\mathrm{V}_{\text {Out }}\right)$. The converter load may generally exhibit inductive, capacitive or resistive impedance. The charge pump circuit (103) is configured to perform power factor correction (PFC) of the AC/DC power converter 100 by drawing charging pulses from the AC line voltage where electrical charges of the charging pulses vary substantially proportionally with an instantaneous amplitude of the AC line voltage as discussed in additional detail below.

FIG. 2 shows a simplified electrical circuit diagram of the resonant class DE power converter (105). The class DE power converter comprises a controllable switch network 212, a series resonant tank or network (214) comprising an inductor $L_{\text {RES }}$ and a capacitor $\mathrm{C}_{\text {Res. }}$. The skilled person will understand that other types of resonant tanks or tank circuits (214) may be used in alternative embodiments of the present AC/DC power converters as schematically illustrated on FIG. 2A. The class DE power converter comprises the previously discussed rectifier or rectification circuit 216. The skilled person will appreciate that alternative resonant power converter topologies such as Class E or LLC topologies may be employed in the present AC/DC power converter 100. The controllable switch network 212 is connected to positive and negative terminals or nodes of the DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ) to energize the converter 105. The resonant class DE power converter 105 typically comprises of two stages, wherein the first stage comprises the controllable switch network 212 and the resonant tank 214. The controllable switch network 212 converts a DC voltage input from the $D C$ supply voltage $\left(V_{D C}\right)$ into a high frequency $A C$ output, i.e. the
resonant inverter voltage $\mathrm{V}_{\text {REC }}$ and the series resonant tank 214 may perform an AC-AC gain. The second stage of the resonant converter 105 comprises the high frequency AC-DC rectification circuit 216 wherein energy/power supplied by the series resonant tank may be tapped off and delivered to the converter/output load ( $\mathrm{R}_{\mathrm{L}}$ ). The rectification circuit 216 may comprise SiC Schottky diodes $D_{R 1}$ and $D_{R 2}$ as discussed in additional detail below. The skilled person will understand that other types of AC-DC rectification circuits 216 may be used in alternative embodiments of the present AC/DC power converters, including rectification circuits that include an isolation transformer such as an center-tapped isolation transformer as schematically illustrated on FIG. 2A.

The utilization of a resonant power converter (105) allows utilization of soft-switching techniques through the intrinsic alternating behaviour of the currents and voltages through high-side and low-side semiconductor switches $Q_{H S}$ and $Q_{\text {Ls }}$ of the halfbridge 212, or controllable switch network, resulting in substantially lower switching losses. Driving signals (not shown) to the gate driver 213 are preferably synchronized with the same duty cycle and extended dead-time adjustment to avoid cross conduction between the semiconductor switches $Q_{H S}$ and $Q_{\text {LS }}$ switches and allow the resonant inductor current to charge or discharge the output capacitance of the halfbridge switches $Q_{H S}$ and $Q_{L S}$ so that their drain voltages reach the appropriate supply rail voltage before switching the gate. Therefore, ensuring zero voltage switching (ZVS) operating conditions of the half-bridge 212.

As discussed below in connection with the design of the charge pump stage, a gain of the class DE resonant inverter or stage should preferably be relatively high, e.g. a gain from about 0.5 to 1 to provide high power factor and low total harmonic distortion (THD) of the AC input current waveform. The inventors have found that a good approximation would be to design for 300 V of DC output voltage and assuming an input DC voltage to the half-bridge equal to the peak of the mains input voltage, e.g. 325 V . The design is preferably based on the well-known First Harmonic Approximation (FHA) approach even though alternative procedures may be used. The computation procedure or flow for an exemplary design of the AC/DC power converter with a target output power of 50 W may start by calculating a rectifier input resistance $R_{R E C}$ from the load resistance $R_{L}$ through impedance transformation via the resonant
rectifier as follows:

$$
\begin{align*}
& R_{L}=\frac{V_{\text {OUT }}{ }^{2}}{P_{\text {OUT }}}=1.8 \mathrm{k} \Omega  \tag{1}\\
& R_{R E C}=\frac{2 R_{L}}{\pi^{2}}=365 \Omega \tag{2}
\end{align*}
$$

The converter voltage conversion ratio is equal to:
$M_{V}=\frac{V_{\text {OUT }}}{V_{I N}}=0.923$

While gains of the half-bridge 212 and class-DE rectifier are equal to 0.45 and 2.22 respectively, the required gain of the series resonant tank 214 can be calculated by:
$M_{V_{-} R E S}=\frac{M_{V}}{M_{V_{-} H B} \cdot M_{V_{-} R E C}}=0.924$

The converter loaded quality factor is calculated using the following equation:
$Q_{L}=\frac{\sqrt{\frac{1}{M_{V-R E S}{ }^{2}}-1}}{f_{n}-\frac{1}{f_{n}}}$
where $f_{n}$ is the normalized switching frequency, equal to $f_{s w} / f_{o}-$ with $f_{o}$ being a resonant frequency of the series resonant tank 214. In order to ensure the validity of the above equations given the FHA approach, the loaded quality factor $Q_{L}$ of the resonant tank or circuit 214 needs to be high enough so that the resonant inverter current through the resonant tank 214 is substantially sinusoidal. A loaded quality factor of 2.5 is chosen for this design [5]. Using equation (5) to calculate the normalized switching frequency, and for a switching frequency of 1 MHz , the resonant frequency is calculated to 921 kHz . Therefrom, the resonant circuit component values may be calculated as:
$L_{R E S}=\frac{Q_{L} \cdot R_{R E C}}{\omega_{o}}=157 \mu H$
$C_{R E S}=\frac{1}{\omega_{o} \cdot Q_{L} \cdot R_{R E C}}=190 \mathrm{pF}$

Rectifier devices stresses are calculated as follows:
$V_{D_{-} \max }=V_{\text {OUT }}=300 \mathrm{~V}$
$I_{D_{-} \max }=\pi I_{\text {OUT }}=524 \mathrm{~mA}$
A voltage stress across the half-bridge switches:
$V_{S_{-} \max }=V_{I N}=325 \mathrm{~V}$

The current stresses of the half-bridge semiconductor switches $Q_{H s}$ and $Q_{\text {Ls }}$ and components of the series resonant network may be calculated from:
$I_{\text {RES_max }}=\pi P_{\text {OUT }}\left(\frac{2}{\eta \cdot V_{\text {IN_ } p k}}+\frac{1}{V_{\text {OUT }}}\right)$

FIG. 3 shows a simplified electrical equivalent circuit or diagram of an exemplary charge pump circuit 103 of the present AC-DC power converter 100. Through the addition of a capacitor, a diode and the previously discussed smoothing capacitor $\left(C_{D C}\right)$ to the resonant converter (105), mains input current drawn from the AC line voltage can be regulated to be substantially proportional to the instantaneous AC line voltage. The present embodiment of the resonant converter (105) comprises a series-resonant inverter circuit in conjunction with and a high-frequency rectification circuit to support LED driver applications. The smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ), or DC energy storage capacitor, is arranged at the converter input. The illustrated electrical equivalent circuit of the charge pump circuit 103 comprises a pump or flying capacitor $C_{p}$ and pump diode $D_{p}$. The AC rectification circuit (101) is schematically represented by diode $D_{B}$ and the rectifier input voltage ( $V_{R E C}$ ) is modelled by an independent high frequency square-wave voltage source 321 . The capacitor $C_{D C}$ is preferably designed in accordance with the pump capacitor $\mathrm{C}_{\mathrm{p}}$, such that the DC supply voltage $\mathrm{V}_{\mathrm{DC}}$ for power supply of the resonant inverter is always higher than the AC line voltage $V_{\mathbb{I N}}$ such that the $A C$ rectification circuit $D_{B}$ and the pump diode $D_{P}$ do not cross-conduct. Consequently, the input current $\mathrm{I}_{\mathbb{N}}$ drawn from the AC line voltage is equal to a positive charging current $I_{p}$ of the pump capacitor $C_{p}$. In other words the capacitance of the smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ) and the capacitance of the pump/flying capacitor ( $C_{P}$ ) are selected such that the $D C$ supply voltage $V_{D C}$ is high-
er than the AC line voltage across an entire cycle of the AC line voltage as discussed in additional detail below.

First, the pump/flying capacitor $\left(\mathrm{C}_{P}\right)$ is preferably large enough to store a maximum input charge from the AC mains, which input charge is function of the output power, the peak input voltage and the switching frequency of the power converter. Those constraints ensure the pump capacitor ( $\mathrm{C}_{\mathrm{P}}$ ) can store the maximum charge needed. This maximum charge occurs at the peak input current and voltage:

$$
\begin{equation*}
C_{P} \geq \frac{2 P_{\text {out }}}{\eta \cdot f_{s} \cdot V_{I N \_p k}{ }^{2}} \tag{12}
\end{equation*}
$$

Second, the capacitance of the smoothing capacitor ( $\mathrm{C}_{D C}$ ) is preferably dimensioned such that the voltage across it, which may correspond to the DC supply voltage $\left(V_{D C}\right)$ of the resonant inverter is higher than the $A C$ line voltage, or mains input voltage, across the entire cycle of the AC line voltage at least during steady state operation of the power converter 100. That constraints ensures the AC rectification circuit $\left(D_{B}\right)$ or diode bridge and the pump diode $\left(D_{P}\right)$ do not conduct at the same time. Hence, avoiding a direct current flow from the AC line voltage to the smoothing capacitor $\left(\mathrm{C}_{\mathrm{DC}}\right)$ and therefore providing control on the input current, which has to flow through the pump capacitor $\mathrm{C}_{\mathrm{p}}$.

$$
\begin{equation*}
C_{D C} \geq \frac{P_{\text {OUT }}}{2 \omega_{l} \cdot V_{D C_{-} \text {ripple }} \cdot V_{D C_{-} a v g}} \tag{13}
\end{equation*}
$$

As mentioned before, the class-DE stage is preferably designed with a high voltage gain (close to unity) which markedly reduces the dependence of the input current on the voltage across the smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ) and the output voltage and makes it a function of only the AC input voltage under steady state operation of the power converter 100.

FIG. 5 shows low-frequency operation of the charge pump circuit 103, where the pump capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$ gets charged and discharged within fall and rise times of the rectifier input voltage $V_{R E C}$, respectively. The electrical charge $\Delta Q_{P}$ is largely propor-
tional to a voltage difference across the pump capacitor $\mathrm{C}_{\mathrm{P}}$ and this voltage difference varies between a low-frequency high-value $\mathrm{V}_{\mathrm{P}_{\text {_high }}}$ and a constant low-value $V_{P \_ \text {_ow }}$ as indicated on the waveform plot 505 . The circuit ensures that the electrical charge variation of pump capacitor $\mathrm{C}_{\mathrm{P}}$, which is proportional to the voltage variation across $C_{p}$, i.e. $\mathrm{V}_{\mathrm{P}_{\text {_high }}}-\mathrm{V}_{\mathrm{P}_{\mathrm{I}} \text { low, }}$ follows, or varies proportionally with, the AC line voltage $\mathrm{V}_{\mathbb{N}}$ across the line cycle $50 / 60 \mathrm{~Hz}$. Accordingly, the average of the mains line current $\mathrm{I}_{\mathrm{IN}}$ follows or tracks instantaneous amplitude of the AC mains line voltage with high accuracy and consequently a power factor very close to unity can ideally be obtained. Experimental results described below illustrates that an impressively high power factor in the range $0.95-0.99$ is readily obtainable.

The skilled person will appreciate that the rectifier input voltage $\mathrm{V}_{\text {REC }}$ can be any kind of waveform with a substantially constant AC amplitude and that any DC bias of the rectifier input voltage $V_{\text {Rec }}$ has no effect on the line input current shape. This feature provides compatibility with different arrangements of the resonant tank circuit including the parallel-resonant, LCC, and LLC tank topologies or circuit arrangements.

FIG. 6 illustrates high frequency operation across two switching cycles of the switching frequency of the class DE resonant converter (105) and includes inter alia waveforms of the charging current $\mathrm{I}_{\mathrm{P}}$ and mains line current $\mathrm{I}_{\mathbb{N}}$ showing the AC-DC converter operation at a maximum power point ( $\omega t=\pi / 2$ ) to illustrate the charge pump circuit operation. The maximum power point corresponds to a resonant frequency of the series resonant tank. Across every switching cycle, at steady-state, the operation of the charge pump circuit spans over four intervals 1, 2, 3 and 4 or states as indicated along the time axis of the waveform plots on FIG. 6, as follows:

1) In a first interval, the rectified line voltage $V_{B}$ as shown on plot 621 is lower than the $D C$ supply voltage $V_{D C}$ and higher than the line input voltage $\mathrm{V}_{\mathrm{IN}}$ where the $\mathrm{V}_{\mathrm{IN}}$ waveform refers to the voltage on the node interfacing the LC-mains filter and the diode bridge $D_{B}$ so both diodes are off and no current flows through the pump capacitor $\mathrm{C}_{\mathrm{P}}$ and the voltage $\mathrm{V}_{\mathrm{P}}$ as shown on plot 623 is essentially constant at $\mathrm{V}_{\mathrm{P} \text { _low. }}$.
2) A second interval or states takes place during the fall time of the rectifier input voltage $\mathrm{V}_{\text {REC }}$ as shown on plot 622 . Once $\mathrm{V}_{\text {REC }}$ starts to decrease, $\mathrm{V}_{\mathrm{B}}$ has to decrease along until diode $D_{B}$ gets forward biased and the rectified line voltage $V_{B}$ gets pulled to $\mathrm{V}_{\text {IN }}$. While $\mathrm{V}_{\text {REc }}$ continues decreasing while $\mathrm{V}_{\mathrm{B}}$ remains substantially constant, because the $50 / 60 \mathrm{~Hz}$ grid frequency varies much slower, e.g. with a factor 1000 or more, than the switching frequency of $\mathrm{V}_{\mathrm{REC}}, \mathrm{V}_{\mathrm{P}}$ increases and the pump capacitor $C_{P}$ is charged by the mains line current $I_{I N}$ as shown on plot 627, until $V_{\text {REC }}$ reaches its low-value and $V_{P}$ reaches its high-value, where:
$V_{P_{-} \text {high }}=V_{I N}-V_{\text {REC_low }}$
3) $A$ third interval or state begins once $V_{R E C}$ settles at the low-value, where $C_{P}$ stops charging while diode $D_{P}$ still remains non-conducting or blocking. Similar to the first interval, no current flows through the pump capacitor and the voltage across the pump capacitor $C_{p}$ remains substantially constant.
4) Eventually, a fourth interval or state takes place during a rise time of $\mathrm{V}_{\text {REC }}$. Once $V_{\text {REC }}$ starts to increase, $V_{B}$ is forced increase along until pump diode $D_{P}$ gets forward biased or conducting and $V_{B}$ is pulled to the $D C$ supply voltage $V_{D C}$. While $V_{R E C}$ (622) continues increasing, with $D C$ supply voltage $V_{D C}$ constant, $V_{P}$ decreases and pump capacitor $C_{P}$ deliver a discharge current into the smoothing capacitor $C_{D C}$ to increase the $D C$ supply voltage $V_{D C}$ and decrease the voltage across pump capacitor $\mathrm{C}_{P}$ until $\mathrm{V}_{\text {REC }}$ reaches its high-value, $\mathrm{V}_{\text {REC_high, }}$, and $\mathrm{V}_{\mathrm{P}}$ reaches its lowvalue, where
$V_{P_{-} \text {low }}=V_{D C}-V_{\text {REC_high }}$

By the end of the fourth interval, the operation of the charge pump circuit reverts to interval or state 1) again and the cycle repeats.

This analysis shows that the mains line current $\mathrm{I}_{\mathrm{IN}}$ on plot 627 is discontinuous. The positive charging current $I_{p}$ on current waveform plot 625 is likewise discontinuous and only flows into the charge pump circuit during the second interval or state. As illustrated by the current waveform plot 627 of the mains line current $\mathrm{I}_{\mathrm{IN}}$ on FIG. 6, a charging current pulse having the electrical charge $\Delta Q_{P}$ is drawn from the $A C$ mains
line voltage during every interval 2 period and the electrical charge $\Delta Q_{P}$ varies substantially proportionally with the instantaneous amplitude of the AC line voltage. As illustrated by the current waveform plot 625 of the pump capacitor current $I_{P}$ on FIG. 6 , a corresponding charging current pulse, possessing an electrical charge $\Delta Q_{P}$, is drawn into the pump capacitor $\mathrm{C}_{\mathrm{P}}$ during every interval 2 ) state. However, a corresponding charging current pulse is drawn out of the pump capacitor $\mathrm{C}_{\mathrm{p}}$ during every interval 4) state and that electrical charge is supplied into the smoothing capacitor $C_{D C}$ to increase the $D C$ supply voltage $V_{D C}$.

FIG. 4 is a schematic electrical diagram of a first exemplary embodiment of the previously discussed AC-DC power converter 100 based on a class-DE series resonant inverter as schematically illustrated on FIG. 2. The AC-DC power converter 100 comprises an optional mains input filter including inductor $\mathrm{L}_{\mathrm{IN}^{N}}$ and capacitor $\mathrm{C}_{\mathrm{IN}}$ inserted between the mains voltage and the AC rectification circuit 401 which may comprise a diode bridge as illustrated. A class DE resonant inverter is configured to convert the $D C$ supply voltage $V_{D C}$ into the resonant inverter voltage $V_{R E C}$ at a fixed or adjustable switching frequency. The class DE resonant inverter 405 comprises high-side and low-side semiconductor switches $Q_{\text {Hs }}$ and $Q_{L s}$ which are driven in a non-overlapping manner by gate driving circuit 413 . The gate driving circuit 413 may comprise a digital isolator, such as Si8610BC by Silicon Labs, and an off-the-shelf type of gate driver such as UCC27611 by Texas Instruments, for each of the semiconductor switches $Q_{H s}$ and $Q_{L s}$. The output voltage $V_{s w}$ of the half-bridge driver comprising high-side and low-side semiconductor switches $Q_{H s}$ and $Q_{\text {Ls }}$ is applied to a series resonant tank 414 to produce a flow of resonant current $I_{\text {RES }}$ through the tank and a resonant inverter voltage $\mathrm{V}_{\mathrm{REC}}$ at the output of the tank 414.

The switching frequency or duty cycle may be adjusted or controlled by an output current or output voltage regulation loop or mechanism. The output current or output voltage regulation loop may comprise a switching frequency controller 440 or alternatively a duty cycle controller, i.e. using on/off control of the converter. One input of the controller 440 may be coupled to the output voltage $\mathrm{V}_{\text {OUT }}$ while another input is coupled to a voltage or current reference generator (not shown) which sets a target output voltage $\mathrm{V}_{\text {REF }}$ or target output current of the AC-DC power converter 100. The
frequency controller 440 generates a switch control signal $F_{\text {sw }}$ to an input of the gate driver 413 to adjust the switching frequency of the class DE resonant inverter 405 such that a target DC output voltage ( $\mathrm{V}_{\text {OUT }}$ ) or target DC output current is achieved as discussed in additional detail below in connection with experimental results of a

Table I shows target specifications of the AC-DC power converter 100 according to one embodiment:

| Parameter | Specification |
| :--- | :--- |
| Operational Volt- <br> age | $230 \mathrm{~V}_{\text {RMs }}$ |
| Line Frequency | 50 Hz |
| Output Power | 50 W |
| Power Factor | $>0.9$ |
| Table I |  | prototype AC-DC power converter. The AC-DC power converter 100 additionally comprises a high frequency AC-DC rectification circuit 416 which is configured to generate the DC output voltage ( $\mathrm{V}_{\text {out }}$ ) to the converter/output load $\left(\mathrm{R}_{\mathrm{L}}\right)$ by tapping off energy/power supplied by the series resonant tank 414 of the class DE inverter.

The AC-DC power converter 100 additionally comprises a charge pump circuit operating according to the principles discussed in connection with FIG. 3 above and which performs the previously discussed advantageous power factor correction (PFC) of the AC-DC power converter 100. The charge pump circuit comprises pump or flying capacitor $\mathrm{C}_{\mathrm{P}}$, a smoothing capacitor $\mathrm{C}_{\mathrm{DC}}$ and pump diode $\mathrm{D}_{\mathrm{P}}$. The rectifier input voltage which is equal to $\mathrm{V}_{\text {REC }}$ is applied at the junction node between output rectification diodes $D_{R 1}$ and $D_{R 2}$. The pump or flying capacitor $C_{P}$ is connected between the rectified line voltage $V_{B}$ and the rectifier input voltage $V_{\text {REC }}$ which is equal to the resonant inverter voltage produced by the class $D E$ resonant inverter.

The charge pump circuit 103 (FIG.3) is preferably designed such that the capaci- tance of the pump capacitor $\mathrm{C}_{\mathrm{P}}$ is large enough to store a maximum input current coming from the offline mains voltage. From the analysis above and considering that
for a series-resonant converter, the resonant inverter voltage $\bigvee_{\text {REC }}$ varies between $\mathrm{V}_{\text {OUt }}$ and 0 V and can be evaluated as follows:

$$
\begin{equation*}
V_{P_{-} \text {high }}=V_{I N}-V_{R E C_{-} \text {low }}=V_{I N}-0=V_{I N} \tag{11}
\end{equation*}
$$

$$
\begin{equation*}
V_{P_{-} \text {low }}=V_{D C}-V_{R E C_{-} \text {high }}=V_{D C}-V_{O U T} \tag{12}
\end{equation*}
$$

The equations (11), (12) show that the high values for the voltage across the pump capacitor $\mathrm{C}_{\mathrm{p}}$ take the envelope of the input voltage, while the low values take the envelope of the difference between the resonant converter's input and output voltages, which can be considered constant in high frequency converters.

Across one switching cycle, the variation of charge in the pump capacitor is equal to:
$\Delta Q_{P}=C_{P} \cdot \Delta V_{P}=C_{P}\left(V_{P_{\text {high }}}-V_{P_{\text {low }}}\right)=C_{P}\left(V_{I N}-V_{D C}+V_{\text {OUT }}\right)$ in a high power factor and low THD. In that case, the maximum current through the pump capacitor (averaged over a switching cycle) will be equal to the maximum input current, which can be calculated as follows. Assuming 90\% converter efficiency, the average input power is equal to:

Assuming a power factor of 1 , the input power is the product of two sinusoids, resulting in a peak input power of:

$$
\begin{equation*}
P_{I N_{-} \max }=2 P_{I N_{-} a v g}=111 \mathrm{~W} \tag{16}
\end{equation*}
$$

Accordingly, the maximum mains line current $\mathrm{I}_{\mathbb{N}}$ or input current is:
$I_{I N_{\_} \max }=\frac{P_{I N_{2} \max }}{V_{I N_{-} \max }}=\frac{111 \mathrm{~W}}{325 \mathrm{~V}}=342 \mathrm{~mA}=I_{P_{-} \max }$

By substituting those values in equation (14), the capacitance for the pump capacitor $\mathrm{C}_{\mathrm{P}}$ can be calculated as follows:
$C_{P}=\frac{I_{P_{\text {_max }}}}{f_{s} \cdot V_{I I_{-} \max }}=\frac{342 \mathrm{~mA}}{1 \mathrm{MHz} 325 \mathrm{~V}}=1.06 \mathrm{nF}$

The value for $\mathrm{C}_{\mathrm{p}}$ can be adjusted to account for the DE inverter stage gain not being exactly $1\left(V_{D C}-V_{\text {OUT }} \neq 0\right)$. In this design, a value of 1.3 nF is chosen. Whereas the maximum voltage seen by the pump capacitor $C_{P}$ is equal to:
$\Delta V_{P_{-} \max }=V_{\text {IN_max }}=325 \mathrm{~V}$

Based on the analysis and calculations outlined above, the exemplary embodiment of the present AC-DC power converter was simulated using LTspice. The switching frequency is set to 1.04 MHz for the simulation. The output power delivered to the converter load is 51 W and an average output voltage of 301 V . The power factor is determined to about 0.99 and total harmonic distortion (THD) of the mains line current is $5.4 \%$. FIG. 7 shows a mains line voltage waveform 750 of $230 \mathrm{~V}_{\text {RMS }}, 50 \mathrm{~Hz}$ inputted to the AC-DC converter for the LTspice circuit simulation. A current waveform 755 of the corresponding the mains line current $\mathrm{I}_{\mathrm{IN}} 7$ drawn by the AC-DC converter is also shown. It is evident that that the mains line current $\mathrm{I}_{\mathbb{N}}$ is largely inphase with the mains line voltage and distortion of the current waveform is relatively low.

Due to the charge pump circuit operation, the current in the resonant tank 414 peaks to the same value as pump capacitor current $I_{p}$, which takes place at the peak of the input power $(\omega, t=\pi / 2,3 \pi / 4)$. The current in the resonant tank 414 is further a function of the switching frequency, the output power, and a shape of the $\mathrm{V}_{\text {REC }}$ wave- form. The value is obtained from the simulation results, as shown in FIG. 8, which indicates that the resonant inductor current peaks to about 1.7A. This is also the maximum value of pump capacitor current $I_{p}$ at the maximum output power of the AC-DC power converter.

Error! Reference source not found. below summarizes specifications for the design of an exemplary inductor $L_{\text {RES }}$ of the series resonant tank (214) which are obtained from the circuit analysis and simulation results as described above.

| Parameter | Specifications |
| :--- | :--- |
| Inductance | $156 \mu \mathrm{H}$ |
| Current Fre- <br> quency | 1 MHz Sinus- <br> oid |
| Current Am- <br> plitude | 1.7 A |
| Table II |  |

When handling high frequency AC currents, a key factor to the inductor design is choosing the right core material. Several magnetic materials [6][7] are investigated and compared in terms of core losses at 1 MHz , as shown in Error! Reference source not found.IG. 10, wherein the 3F46 material (Ferroxcube) may be chosen as it shows the lowest core losses at the design operating conditions.

The following equation was used to estimate the inductor core loss. The peak flux density in the core can be calculated from:
$B_{p k}=\frac{1}{N} \cdot \frac{I_{p k} \cdot L}{A_{e}}$
where N is the number of turns, $\mathrm{I}_{\mathrm{pk}}$ is the amplitude of the resonant current, L is the inductance, and $A_{e}$ is the effective core area. Considering that the core loss is a function of the peak flux density for a chosen material, the loss for a given number of turns and core size can be estimated. The following calculation of the DC resistance of the windings gives an estimate of the winding losses.

The total cross-sectional area of the windings may be calculated from:
$A_{c}=n_{\text {wires }} \cdot \pi \cdot r_{\text {wire }}{ }^{2}$
where $\mathrm{n}_{\text {wires }}$ is the number of strands of Litz wire and $\mathrm{r}_{\text {wire }}$ is the wire radius. The DC resistance may then calculated from:
$R_{d c}=\rho_{c u} \cdot \frac{M L T \cdot N}{A_{c}}$
where $\rho_{c u}$ is the copper resistivity and MLT is the mean length of turn. For an EFD $25 / 13 / 9$ core size, with two parallel layers of $20^{*} 0.05 \mathrm{~mm}$ Litz wire, the DC resistance is $8.6 \mathrm{~m} \Omega \cdot \mathrm{~N}$. Next, AC resistance of the windings is calculated. The skin effect is negligible when using Litz wire at 1 MHz , but the proximity effect can have a significant influence on the closely wound wires. Modelling the AC resistance to be three times larger than the DC resistance estimates the winding losses to

$$
\begin{equation*}
P_{c u}=R_{a c} \cdot I_{r m s}^{2}=3 \cdot R_{d c} \cdot \frac{I_{p k}^{2}}{2}=37 \mathrm{~mW} \cdot \mathrm{~N} \tag{25}
\end{equation*}
$$

Based on these estimates, the inductor is designed with 52 turns, which helps distribute the losses evenly between the core and the windings and results in acceptable total losses. An airgap of 1.2 mm , distributed across the three legs of the core, adjusted the desired inductance.

FIG. 4A is a schematic electrical diagram of a second exemplary embodiment of the previously discussed AC-DC power converter 100a based on class-DE resonant inverter. Compared to the previously discussed first exemplary embodiment of the AC-DC power converter on FIG. 4, the present AC-DC power converter 101 additionally comprises a transformer T1 (no denotation) with a certain voltage conver-
sion ratio to step-up or step-down the resonant inverter voltage $\mathrm{V}_{\text {res }}$. The transformer T1 provides galvanic isolation between primary side circuitry and secondary side circuitry of AC-DC power converter 100a and is coupled between the resonant output voltage $\mathrm{V}_{\text {res }}$ and an input node 411a of the output rectification circuit 416a con- nected to diodes $D_{R 1}$ and $D_{R 2}$. As discussed above in connection with non-isolated AC-DC power converter 100a, the charge pump circuit comprises a pump capacitor $C_{P}$, a smoothing capacitor $C_{D C}$ and pump diode $D_{P}$. The pump capacitor $C_{P}$ is connected between the rectified line voltage $\mathrm{V}_{\mathrm{B}}$ and the resonant inverter voltage $\mathrm{V}_{\text {REC }}$ produced by the class DE resonant inverter. Preferably, the electrical interconnection between the rectified line voltage $\mathrm{V}_{\mathrm{B}}$ and resonant inverter voltage $\mathrm{V}_{\text {REC }}$ is based on capacitor only network, for example exclusively including the pump capacitor $\mathrm{C}_{\mathrm{P}}$. This provides a compact and low-cost connection that may be based on standard, low cost and readily available capacitors as discussed below. Hence, the electrical interconnection between the rectified line voltage $\mathrm{V}_{\mathrm{B}}$ and resonant inverter voltage $\mathrm{V}_{\text {REC }}$ is therefore preferably carried out without the use of any inductive coupling or component from the isolation transformer, T , such as a separate transformer winding, back to the rectified line voltage $\mathrm{V}_{\mathrm{B}}$.

FIG. 9 shows inductor losses in the inductor $L_{\text {RES }}$ of the series resonant tank (214) vs. number of turns. Based on these estimates, $L_{\text {RES }}$ is preferably designed with about 52 turns, which helps distribute the losses evenly between the core and the windings and results in acceptable total losses. An airgap of 1.2 mm , distributed across the three legs of the core may be utilized to adjust the desired inductance. An experimental prototype of the AC-DC converter was implemented and assembled on a printed circuit board. Because of the charge pump circuit operation, high frequency $A C$ current runs through the $A C$ rectification circuit, or input bridge, The latter is therefore preferably implemented using four fast recovery diodes as rectification elements. With respect to selection of the high-side and low-side semiconductor switches $Q_{H S}$ and $Q_{\text {LS }}$ of the half-bridge 412 the inventors found gallium nitride FETs to show superior performance compared to the silicon super-junction and silicon carbide counterparts. However, the skilled person will appreciate that semiconductor switches may be used for the purpose based on design constraints imposed on any specific embodiment of the present AC-DC power converter. For the rectification circuit 416 , including diodes $D_{R 1}$ and $D_{R 2}$, silicon carbide Schottky di-
odes may be employed because they show higher energy efficiency and thermal stability over the silicon counterparts.

Error! Reference source not found. shows a breakdown of the incorporated power stage components of the experimental prototype AC-DC power converter.

| Component | Simulated | Prototype | Type |
| :---: | :---: | :---: | :---: |
| $\mathrm{L}_{\text {IN }}$ | $100 \mu \mathrm{H}$ | $100 \mu \mathrm{H}$ <br> SLF7045 | Inductor |
| $\mathrm{C}_{\text {IN }}$ | 30 nF | 2*15 nF | Ceramic (COG) |
| Diode <br> Bridge |  | $\begin{aligned} & 4^{*} \text { ESH1GM } \\ & \text { RSG } \end{aligned}$ | Si Fast Recovery |
| $\mathrm{C}_{\mathrm{DC}}$ | $10 \mu \mathrm{~F}$ | $\begin{aligned} & 1 * 10 \mu \mathrm{~F} \\ & 3 * 0.1 \mu \mathrm{~F} \end{aligned}$ | Electrolytic <br> Ceramic (C0G) |
| $\mathrm{D}_{\mathrm{P}}$ |  | RF201LAM4S | Si Fast Recovery |
| $\mathrm{Cr}_{\mathrm{P}}$ | 1.36 nF | 2*680 pF | Ceramic (C0G) |
| $Q_{\text {HS }}, Q_{\text {LS }}$ |  | GS66502B | GaN <br> Switches |
| L ${ }_{\text {RES }}$ | $156 \mu \mathrm{H}$ | $152 \mu \mathrm{H}$ | Custom design |
| $\mathrm{C}_{\text {RES }}$ | 188 pF | 220 pF | Ceramic (C0G) |
| $\mathrm{D}_{\mathrm{R} 1}, \mathrm{D}_{\mathrm{R} 2}$ |  | $\begin{aligned} & \hline \text { GB01SLT06- } \\ & 214 \end{aligned}$ | SiC <br> Schottky |
| Cout | 30 nF | 2*15nF | Ceramic (C0G) |

Table III

The experimental prototype AC-DC power converter was tested for operation from a mains voltage of $230 \mathrm{~V}_{\text {RMS }}$ and running at converter switching frequencies between 0.96 MHz and 1.04 MHz . The latter frequency range lies within an inductive mode of operation for the resonant converter such that soft-switching operation, i.e. ZVS, of the class DC inverter was achieved.

FIG. 11 (top plot) shows the measured output power (left scale) and conversion efficiency (right scale) across the operational frequency range from 960 kHz to 1040 kHz of the experimental prototype AC-DC power converter. The depicted measurement results illustrate how output power modulation or control is achieved from 26 W to 50 W of output power through control of the switching frequency. At the same time a peak efficiency of $87.9 \%$ at 1.04 MHz switching frequency is achieved.

FIG. 11 (bottom plot) shows measured PFC results of the experimental prototype AC-DC power converter. The PFC results exhibit a peak power factor of 0.99 and minimum THD of 8.6 \% at an output power of 50 W and switching frequency of 960 kHz . The measured data shows that operation at lower frequencies, close to resonance of the series resonant tank with higher gain achieves higher power factor and lower THD. This is consistent with the analysis given in the previous sections.

FIG. 12 shows measured harmonics distribution of the mains line current at full-load operation and at half-load operation of the experimental prototype AC-DC power converter where THD figures of 8.6 \% and 17.4 \% are measured, respectively. Since one of the potential applications for the proposed converter is the rectifier or rectification circuit or stage in LED drivers, the figure illustrates the harmonics magnitudes against the IEC 61000-3-2 standard class-C device limits [1][2], where the histogram shows that the measured harmonics magnitudes are well-within the limits set by the IEC standard.

FIG. 13 shows line-frequency time domain waveforms of the experimental prototype AC-DC power converter. The experimental prototype AC-DC power converter is delivering an output or load power of 12.8 W and has a measured power factor of 0.99 and a THD of $9.1 \%$ for an average DC output voltage of 179 V with 20 V lowfrequency ripple as illustrated by the $\mathrm{V}_{\text {Out }}$ waveform.

FIG. 14 shows measured harmonics distribution of the mains line current for the experimental prototype AC-DC power converter at 120 V_RMS and 230 V_RMS line voltage inputs against the IEC 61000-3-2 standard class-C device limits [1][2]. FIGS. 13 and 14 illustrate that a high power factor and low THD of the prototype AC-DC power converter are achieved with different line input voltages as the charge pump circuit works in the same manner.

## References

[1] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[2] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[3] X. Xie, C. Zhao, L. Zheng and S. Liu, "An Improved Buck PFC Converter With High Power Factor," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 22772284, May 2013.
[4] X. Wu, J. Yang, J. Zhang and M. Xu, "Design Considerations of Soft-Switched Buck PFC Converter With Constant On-Time (COT) Control," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3144-3152, Nov. 2011.
[5] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd Edition ed., Wiley-IEEE Press, 2011.
[6] Ferroxcube material datasheet https://www.ferroxcube.com/upload/media/design/FXCStainmetzCoefficients.xls.
[7] Micrometals material datasheet https://micrometalsarnoldpowdercores.com/pdf/mix/Mix-6-DataSheet.pdf.

## CLAIMS

1. An AC-DC power converter comprising:

- an AC rectification circuit ( $\mathrm{D}_{\mathrm{B}}$ ) configured to convert an AC line voltage into a rectified line voltage $\left(V_{B}\right)$,
- a rectifying element $\left(D_{p}\right)$ connected between the rectified line voltage $\left(V_{B}\right)$ and a DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ) of a resonant DC converter; said resonant DC converter comprising:
- a resonant inverter (105) configured to convert the DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ) into a resonant inverter voltage at a fixed or controllable switching frequency, and - an output rectification circuit configured to generate a DC output voltage ( $\mathrm{V}_{\text {Out }}$ ) or DC output current from the resonant voltage for supply to a converter load $\left(R_{L}\right)$, - a charge pump circuit (103) connected to the rectified line voltage ( $\mathrm{V}_{\mathrm{B}}$ ) and the resonant inverter voltage, where said charge pump circuit (103) is configured to draw current pulses at the switching frequency from the AC line voltage, wherein electrical charges of the current pulses vary proportionally to instantaneous amplitude of the AC line voltage.

2. An AC-DC power converter according to claim 1, wherein the charge pump circuit comprises:

- a smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ) connected to the DC supply voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ of the resonant DC-DC converter;
- a pump or flying capacitor $\left(\mathrm{C}_{\mathrm{P}}\right)$ connected from the resonant inverter voltage to the rectified line voltage $\left(\mathrm{V}_{\mathrm{B}}\right)$.

3. An AC-DC power converter according to claim 2 , wherein the charge pump circuit is configured to, during a cycle of the switching frequency, sequentially cycle through states of:

- a first state where each of the rectifying element $\left(D_{p}\right)$ and AC rectification circuit $\left(D_{B}\right)$ is non-conducting/off and a voltage across the pump/flying capacitor $\left(C_{P}\right)$ remains substantially constant;
- a second state where AC rectification circuit $\left(D_{B}\right)$ is conducting/on and the rectifying element $\left(D_{p}\right)$ is non-conducting/off to charge the pump/flying capacitor $\left(C_{p}\right)$ by line current drawn from the AC line voltage;
- a third state where each of the rectifying element $\left(D_{p}\right)$ and $A C$ rectification circuit
$\left(D_{B}\right)$ is non-conducting/off and the voltage across the pump/flying capacitor $\left(C_{P}\right)$ remains substantially constant;
- a fourth state where the $A C$ rectification circuit $\left(D_{B}\right)$ is in a non-conducting/off state and the rectifying element $\left(D_{p}\right)$ is in a conducting/on state such that discharge cur- rent flows from the pump/flying capacitor $\left(C_{P}\right)$ into the smoothing capacitor $\left(\mathrm{C}_{\mathrm{DC}}\right)$ to increase the $D C$ supply voltage $\left(V_{D C}\right)$ of the resonant inverter and decrease the voltage across the pump/flying capacitor ( $\mathrm{C}_{\mathrm{P}}$ ).

4. An AC-DC power converter according to claim 3, wherein the charge pump circuit is configured to:

- cycle through its second state during a rising edge of a waveform of the resonant inverter voltage; and
- cycle through its fourth state during a falling edge of the waveform of the resonant inverter voltage.

5. An AC-DC power converter according to any of claims 2-4, wherein a capacitance of the smoothing capacitor $\left(C_{D C}\right)$ and a capacitance of the pump/flying capacitor $\left(\mathrm{C}_{P}\right)$ are selected such that the DC supply voltage $\left(V_{D C}\right)$ of the resonant inverter is higher than the $A C$ line voltage across an entire cycle of the AC line voltage.
6. An AC-DC power converter according to any of the preceding claims, further comprising:

- a voltage or current regulation loop configured to adjust the DC output voltage ( $\mathrm{V}_{\text {OUt }}$ ) or DC output current in accordance with a DC reference voltage or a DC reference current.

7. An AC-DC power converter according to claim 6 , wherein the voltage or current regulation loop is configured to:

- adjust the DC output voltage ( $\mathrm{V}_{\mathrm{OUT}}$ ) or DC output current by adjusting the controllable switching frequency, i.e. frequency modulation control, and/or
- adjust the DC output voltage ( $\mathrm{V}_{\text {OUt }}$ ) or DC output current by off/on duty cycle modulation of the fixed or controllable switching frequency for example a PWM switching or carrier frequency of the resonant inverter (105).

8. An AC-DC power converter according to any one of the preceding claims, wherein the resonant inverter comprises at least one semiconductor switch connected between the DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ) and a negative supply rail; said at least one semiconductor switch comprising one or more wide bandgap transistors such as one or more gallium nitride FET(s).
9. An AC-DC power converter according to claim 8, wherein a switch signal, at the fixed or controllable switching frequency, is applied to a control terminal, e.g. a gate terminal, of the least one semiconductor switch of the resonant inverter (105).
10. An AC-DC power converter according to anyone of the preceding claims, wherein the resonant inverter and/or the output rectification circuit of DC-DC converter is configured for zero voltage switching (ZVS) and/or zero current switching (ZCS).
11. An AC -DC power converter according to anyone of the preceding claims, wherein the output rectification circuit comprises one or more passive diodes, such as a silicon carbide Schottky diode(-s), or one more active/controllable diodes, such as MOSFETs.
12. An AC-DC power converter according to anyone of the preceding claims, wherein the resonant inverter comprises a series resonant network and/or a parallel resonant network having a predetermined resonance frequency, such as resonance frequency between 100 kHz and 300 MHz .
13. An AC-DC power converter according to anyone of the preceding claims, wherein the switching frequency is between 100 kHz and 300 MHz .
14. An AC-DC power converter according to anyone of the preceding claims, further comprising galvanic isolation barrier, such as an isolation transformer, coupled between the resonant output voltage and an input of the output rectification circuit.
15. A method of applying power factor correction to an AC-DC power converter using a charge pump circuit, said method comprising steps of:

- converting an $A C$ line voltage into a rectified line voltage $\left(V_{B}\right)$,
- applying the rectified line voltage $\left(V_{B}\right)$ to a $D C$ supply voltage $\left(V_{D C}\right)$ of a resonant DC-DC converter through a rectifying element ( $\mathrm{D}_{\mathrm{p}}$ ),
- generating a resonant inverter voltage by switching a resonant inverter at a fixed or controllable switching frequency,
- rectifying the resonant inverter voltage to generate a DC output voltage ( $\mathrm{V}_{\text {out }}$ ) or DC output current,
- drawing charging pulses, at the switching frequency, from the AC line voltage into a pump or flying capacitor ( $\mathrm{C}_{\mathrm{P}}$ ) connected between the rectified line voltage $\left(\mathrm{V}_{\mathrm{B}}\right)$ and the resonant inverter voltage, wherein electrical charges of the charging pulses vary proportionally to an instantaneous amplitude of the AC line voltage,
- discharging the pump or flying capacitor ( $\mathrm{C}_{\mathrm{P}}$ ) into a smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ), connected to the DC supply voltage ( $\mathrm{V}_{\mathrm{DC}}$ ), by supplying current pulses, at the switching frequency, into the smoothing capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ).


## ABSTRACT

The present invention relates to an AC-DC power converter which comprises a resonant DC-DC converter and a charge pump circuit. The charge pump circuit is configured to perform power factor correction of the AC-DC power converter by drawing current pulses at a switching frequency of the converter from an AC line voltage such that electrical charges of the current pulses vary substantially proportionally with instantaneous amplitude of the AC line voltage.


FIG. 1


FIG. 2

FIG. 2A

4/12


FIG. 3


FIG. 4


FIG. 4A


FIG. 5


FIG. 6

9/12


FIG. 7


FIG. 8


FIG. 9

## 11/12



FIG. 10


FIG. 11


FIG. 12


FIG. 13


FIG. 14

## Appendix [P2]

Y. Nour, A. M. Ammar, A. Knott, and C. K. Lumby, "Universal Mains High Power-Density ACDC Converter", patent pending, April 2020.

## Universal Mains High Power-Density AC-DC Converter

## Field of Invention

The invention relates to a high power-density universal-mains AC-DC Converter.

## Background of the Invention

Power factor correction (PFC) in AC-DC power converters is required in many applications. In the case of lighting equipment, the European Standard specifies power factor requirements for $>25 \mathrm{~W}$ rated solutions. At such low power levels, the PFC circuit is often a limiting factor for power density. Furthermore, universal offline power converters are required to adopt different variations of input RMS voltages ranging from 100 V to 240 V . As a result, universal PFC circuits must handle approximately double current or double voltage for the same power transfer at either of the input condition extremes compared to the opposite extreme. This variation results in difficulties in the optimization of key power processing components, which often lead to bulky circuit implementations.

## Summary of the Invention

Considering the prior art described above, it is an object of the present invention to present a PFC circuit, where the key power processing components can be optimized irrespective of the input voltage.

The object can be achieved by means of an AC-DC converter according to claim 1.

The second rectified AC signal has a voltage and a current, which have a phase shift. A purpose of the power factor correction (PFC) circuit is to minimize the phase shift of the current in relation to the phase of the voltage of the second rectified AC signal. When the phase shift of the voltage and the current is minimised and the voltage and the current are substantially in phase, the real power is almost equal to the apparent power and the reactive power is almost zero, reducing the amount of non-productive power, so that nearly all of the power provided can be utilised by the load.

Alternatively, the phase shift of the voltage of the second rectified AC signal can be minimized in relation to the phase of the current of the second rectified AC signal.

The voltage scaling circuit can be a voltage divider or a current multiplier when the first $\mathrm{V}_{\text {RMS }}$ is within a certain upper range, or the voltage scaling circuit can be a voltage multiplier or a current divider when the first $\mathrm{V}_{\mathrm{Rms}}$ is within a certain lower range. The purpose of the voltage scaling circuit is to expose the PFC circuit to similar conditions irrespective of whether the received AC signal on the first input is AC mains with a voltage of around $120 \mathrm{~V}_{\text {RMS }}$ or around $230 \mathrm{~V}_{\text {RMs. }}$. Either a first scaling factor above one is applied to the rectified lower voltage, like e.g. $120 \mathrm{~V}_{\mathrm{RMS}}$, and the rectified upper voltage, like e.g. $230 \mathrm{~V}_{\text {RMS }}$, is uninfluenced or at least substantially uninfluenced by the voltage scaling circuit, or the first scaling factor is below one and the first scaling factor is applied to the rectified upper voltage and the rectified lower voltage is uninfluenced or at least substantially uninfluenced by the voltage scaling circuit.

That the PFC circuit is exposed to similar conditions irrespective of the received AC signal on the first input means that the PFC circuit can be designed so that there will be lower voltage stresses on the whole circuit and particularly on the PFC circuit, and so that the PFC circuit can allow much higher switching frequency, and hence smaller magnetic components. The whole circuit comprises the rectifier, the voltage scaling circuit, and the PFC circuit, and maybe a control circuit.

The rectifier - if used without a PFC circuit - can distort the current waveform to a nonsinusoidal waveform so that unwanted harmonic currents and/or voltages are created in addition to the fundamental frequency of the signal. The harmonic currents are unwanted, since the high frequencies of the harmonic currents can be fatal to some electrical components in the circuit and, since the high frequencies can cause e.g. increased heating.

Another purpose of the power factor correction (PFC) circuit can be to change the shape of the current and/or voltage waveform to a sinusoidal waveform to remove the unwanted harmonic currents, e.g. by filters.

If the voltage scaling circuit can be a voltage divider or a current multiplier, a further advantage is that the whole circuit can be used to produce a lower output voltage depending on the voltage scaling circuit.

The AC-DC converter can be configured or suitable for receiving a high power AC signal and convert the high power AC signal to a DC signal, where high power AC signal can be at least $100 \mathrm{~V}_{\text {RMs }}$ or between $100-500 \mathrm{~V}_{\text {rms }}$ like e.g. AC mains. For an alternating electric voltage, $\mathrm{V}_{\text {RMs }}$, the root-mean-square voltage of the signal, can be equal to the value of the direct current that would produce the same average power dissipation in a resistive load.

The AC-DC converter according to the present disclosure reduces the PFC converter size by $30 \%$ compared to the state-of-the-art converters with a comparable efficiency and results in a simplification of the down-stream DC-DC converter.

The PFC circuit operation can be controlled, configured or designed to supply a constant DC voltage at its output. It is capable of supplying a constant output voltage while minimising voltage-current phase shift and reducing unwanted harmonic content as described above by utilising internal energy storage component(s). The PFC circuit can use sensing of the second signal voltage and current (after rectifier) or sensing of the third signal voltage and current (after voltage scaling) or sensing of the fourth signal (after PFC) voltage or any combination of these signals to control its operation.

In an embodiment, the voltage scaling circuit can be a switched-capacitor circuit.

Using switched-capacitor circuits is beneficial in terms of low energy consumption, and high power density.

In an embodiment, the first voltage range can be a certain lower range, which can be below a first limit, or a certain upper range, which can be above the first limit, wherein the first limit can be between 140 and 200 V $_{\text {RMs }}$, more preferably between 150 and 180 $V_{\text {RMS }}$.

AC mains are generally either $120 \mathrm{~V}_{\text {RMS }}$ or $230 \mathrm{~V}_{\text {RMS }}$, so that the first limit somewhere between 140 and $200 \mathrm{~V}_{\text {RMS }}$ will always distinguish between $A C$ mains of $120 \mathrm{~V}_{\text {RMS }}$ or $230 \mathrm{~V}_{\text {RMs. }}$. AC mains voltage has a tolerance. It is normal to have an input mains voltage lower or higher than the nominal values according to the specified range. To be on the safe side the first limit can be somewhere between 150 and $180 \mathrm{~V}_{\text {RMs. }}$.

In an embodiment, the voltage scaling circuit can be configured to scale the first rectified AC signal by a second scaling factor different from the first scaling factor, if the first $\mathrm{V}_{\text {RMs }}$ is within a second voltage range different from the first voltage range generating a third rectified AC signal.

By a second scaling factor different from the first scaling factor acting, wherein the first scaling factor and the second scaling factor are applied within two different ranges, two voltage ranges of the first rectified AC signal can be brought close to a third range, or two voltage ranges of the first rectified AC signal can be brought closer to each other, wherein for both voltage ranges of the first rectified AC signal the first rectified AC signal is lowered or increased.

In an embodiment, the second voltage range can be the certain upper range if the first voltage range is the certain lower range, and the second voltage range can be the certain lower range if the first voltage range is the certain upper range.

This way the whole range is covered and the certain lower range as well as the certain upper range will be scaled with either the first scaling factor or the second scaling factor. Irrespective of the voltage of the first rectified AC signal, the voltage of the first rectified AC signal can be lowered and/or increased.

In an embodiment, the first scaling factor and the second scaling factor can both be above one, or can both be below one, or the first scaling factor can be above one and the second scaling factor can be below one, or vice versa.

Such a voltage scaling circuit can e.g. be designed to lower the first rectified AC signal irrespective of whether the first $\mathrm{V}_{\text {RMS }}$ is in the certain lower range or in the certain upper range, wherein if the first $\mathrm{V}_{\mathrm{RMs}}$ is in the certain upper range the first rectified AC signal can e.g. be lowered more than if the first $\mathrm{V}_{\mathrm{Rms}}$ is in the certain lower range. In that way, the voltage supplied to the third input, i.e. to the input of the PFC circuit can be made much lower than the received AC signal reducing stress on the PFC circuit. Since AC mains is normally either around $120 \mathrm{~V}_{\text {RMS }}$ or around $230 \mathrm{~V}_{\text {RMS }}$ (for a single phase, but the ratio is one or two also for three phase systems) a ratio between the first scaling factor and the second scaling factor of around two will yield a voltage supplied to the
third input that is more or less the same irrespective of the AC mains being around 120 $V_{\text {RMs }}$ or around $230 \mathrm{~V}_{\text {RMs. }}$

In an embodiment, the AC-DC converter can comprise a control circuit for controlling the PFC circuit based on the first rectified AC signal of the second input and/or the DC signal of the third output.

The PFC circuit can have one control loop, even two control loops, or even three control loops. One loop can control the shape of the current of the first rectified AC signal, and for that, the voltage of the first rectified AC signal and/or the second rectified AC signal can be the controller input. The other loop can control the voltage of the output DC signal, and for that, the voltage of the output DC signal is a control input. The controller output can be a duty-cycle modulated signal to the power stage.

What is important is that the AC mains voltage and the current drawn by the whole circuit are in phase and have equal profiles, preferably sinus shapes, so that the active power equals or at least is close to the apparent power, the input power of the whole circuit. In other words, the power factor should preferably be as close to 1 as possible.

In an embodiment, the control circuit can control the power factor of the PFC circuit by minimising the phase shift between the voltage and the current of the second rectified AC signal.

Phase shift control and waveform shape control are both obtained by sensing the first rectified AC signal and/or the second rectified AC signal. In a simple PFC circuit, the current waveform is controlled to be an amplitude scaled version of the voltage, and hence both phase and shape can be corrected.

The exact method by which the control is implemented can vary and the skilled person will know how to design and implement the control. The present invention can utilise any PFC control method that would also work if connected directly to the AC mains.

In an embodiment, the first scaling factor of the scaling circuit can be two if the first $\mathrm{V}_{\text {RMS }}$ is within the certain lower range, or the first scaling factor can be one half if the first $\mathrm{V}_{\text {RMs }}$ is within the certain upper range.

Since the two dominating AC mains voltages are around $120 \mathrm{~V}_{\text {RMS }}$ and $230 \mathrm{~V}_{\text {RMs }}$ it is preferable either that the PFC circuit is dimensioned for a rectified 230 VRMS $^{\text {signal, in }}$ which case a voltage around $120 \mathrm{~V}_{\mathrm{Rms}}$ is multiplied by a factor 2 , while a voltage around $230 \mathrm{~V}_{\text {RMs }}$ is left uninfluenced, or that the PFC circuit is dimensioned for a rectified $120 \mathrm{~V}_{\text {RMS }}$ signal, in which case a voltage around $230 \mathrm{~V}_{\text {RMS }}$ is multiplied by a factor $1 / 2$, while a voltage around $120 \mathrm{~V}_{\text {RMS }}$ is left uninfluenced.

In an embodiment, the first scaling factor can be two if the first $\mathrm{V}_{\text {RMS }}$ is within the certain lower range, and the first scaling factor can be 1 otherwise, or the first scaling factor can be one half if the first $\mathrm{V}_{\text {Rмs }}$ is within the certain upper range, and the first scaling factor can be 1 otherwise.

In an embodiment, the AC-DC converter can comprise at least one switch for bypassing the voltage scaling circuit, where the voltage scaling circuit can be bypassed when the first $\mathrm{V}_{\mathrm{RMS}}$ is outside the certain lower range or the certain upper range.

If the voltage of the first rectified AC signal is below the certain upper range, the at least one switch bypasses the voltage scaling circuit so that the first rectified AC signal is uninfluenced by the voltage scaling circuit, while if the voltage of the first rectified AC signal is within the certain upper range, the at least one switch does not bypass the voltage scaling circuit so that the first rectified AC signal is influenced by the voltage scaling circuit, by a factor lower than one being applied on the first rectified AC signal.

Alternatively, if the voltage of the first rectified AC signal is above the certain lower range, the at least one switch bypasses the voltage scaling circuit so that the first rectified AC signal is uninfluenced by the voltage scaling circuit, while if the voltage of the first rectified AC signal is within the certain lower range, the at least one switch does not bypass the voltage scaling circuit so that the first rectified AC signal is influenced by the voltage scaling circuit, by a factor above one being applied on the first rectified AC signal.

This will be a simple and cost-effective way of exposing the PFC circuit to a similar signal irrespective of whether the received $A C$ signal on the first input is $120 V_{\text {RMS }}$ or $230 \mathrm{~V}_{\text {RMs }}$.

In an embodiment, the switched-capacitor circuit can comprise an out-capacitor, Cout, parallel over a second output and connecting a node 1 and a node 2, a first switch, Q1, and a second switch, Q2, in series, parallel with the out-capacitor, wherein the first switch and the second switch are connected in a node 3, wherein the node 3 is connected to the node 1 by the first switch and to the node 2 by the second switch, a fly-capacitor, Cfly, connecting the node 3 to a node 4, a third switch, Q3, connecting the node 2 to the node 4 , a fourth switch, Q4, connecting the node 4 to a node 5 , an incapacitor, Cin, parallel over the second input and connecting the node 5 and the node 1, wherein either Q1 and Q3 are conducting simultaneously or Q2 and Q4 are conducting simultaneously.

Design concepts of the art require many switching elements and impose challenges if traditional PFC control schemes would be combined with charge balancing of capacitors. These approaches are not suitable for low power designs, where component count by itself quickly becomes the limiting factor for power density. In contrast, the voltage scaling circuit in the proposed topology uses as few as four switches and three capacitors and operates in open-loop. With as few as four switches and three capacitors the power density can be kept high.

In an embodiment, the switched-capacitor circuit can comprise ten or less switches, preferably eight or less switches, more preferably six or less switches, and most preferably five or less switches.

The aforementioned switches can be integrated in one chip or module. Hence, the complexity of the scaling circuit can be reduced. Integration of the switches can also provide a way to optimize the efficiency.

As mentioned above, at low power designs component count by itself quickly becomes the limiting factor for power density. The fewer the number of components the better. Five or less switches will be advantageous.

In an embodiment, the voltage scaling circuit can be a step-down converter following the input voltage.

If the voltage scaling circuit is a step-down converter the first scaling factor of the voltage scaling circuit will be below 1 so that the second rectified AC signal will have a lower voltage than the first rectified AC signal. With a lower voltage supplied to the PFC circuit, the components can be chosen so that they only be exposed to lower voltages. The PFC circuit can be made more cost-effective.

In an embodiment, the voltage scaling circuit can be a step-up converter following the input voltage.

The PFC circuit must store energy during each period of the AC mains frequency to be capable of delivering power to the load, when the rectified input voltage is low. This storage is usually implemented with a bulk storage capacitor. The energy in a capacitor is proportional to the square of its charged voltage. Hence, more energy can be stored at a high capacitor voltage than a low capacitor voltage with the same capacitance.

Due to component limitations, the higher voltage rated capacitors provide less capacitance per volume, so there exists an optimal balance between capacitor voltage rating and capacitance value, which is determined by the component technology.

In general, whether to choose a step-up or step-down scaling is determined by development of component manufacturing technologies. Some components provide lower volume at high voltages and other at low voltages. In designing the AC-DC converter the voltage-volume relation must be considered/weighted for all components to decide between step-up and step-down. In either case, the nearly constant PFC input voltage due to adaptive voltage scaling results in reduction of overall volume from the reduced operating condition variation.

In some applications, the needed output voltage can be higher than the AC mains voltage (for example 600 V or 1200 V ). In these cases, it is beneficial to design the scaling circuit to "help" achieving the system requirements by scaling in the right direction - by stepping up the voltage.

In an embodiment, the voltage scaling circuit can be step up/down converter (for example buck-boost converter) which can step down or up the voltage, respectively, depending on the voltage of the AC signal or of the first rectified AC signal.

Since the two dominating AC mains voltages are around $120 \mathrm{~V}_{\text {RMs }}$ and around 230 $V_{\text {RMs }}$ it is preferable that the step-down converter or the step-up converter steps down $230 \mathrm{~V}_{\text {RMs }}$ by a factor of 2 and leaves $120 \mathrm{~V}_{\text {RMs }}$ uninfluenced or steps up $120 \mathrm{~V}_{\text {Rms }}$ by a factor of 2 and leaves $230 \mathrm{~V}_{\text {RMs }}$ uninfluenced, respectively. The amplitude of the voltage of the first rectified AC signal entering the step-down converter or the step-up converter can control the step-down converter or the step-up converter to step down the voltage or leave the voltage uninfluenced, or step up the voltage or leave the voltage uninfluenced, respectively. A control unit, like e.g. the control circuit for controlling the PFC circuit, can measure the voltage of the AC signal or the first rectified AC signal and control the step-down converter or the step-up converter.

With such a step-down converter or step-up converter, the same AC-DC converter can be used almost anywhere in the world. Since the electrical outlet varies between countries, AC-DC converter only needs to be adapted to have the plugs that fit the electrical outlets of the country, where the AC-DC converter is sold.

## Description of the Drawings

The invention will in the following be described in greater detail with reference to the accompanying drawings:

Fig. 1 a schematic view of a AC-DC converter
Fig. 2 a schematic view of an embodiment of a switched-capacitor circuit
Fig. 3 a simplified schematic to analyse the effect of the voltage scaling circuit/SC converter on the overall AC-DC converter power factor, where the SC converter is modelled as a DC transformer

Fig. 4 input and output current and voltage waveforms when the effective capacitance has an intermediate value

Fig. 5 shows the power factor and the current phase as a function of the effective capacitance of the switched-capacitor circuit shown in Fig. 2

Fig. 6 measured input and output current and voltage waveforms without a PFC circuit

Fig. 7 measured input and output current and voltage waveforms for the complete system with a PFC circuit

## Detailed Description of the Invention

Fig. 1 shows an AC-DC converter 1 comprising a rectifier 3, a voltage scaling circuit 5, a power factor correction (PFC) circuit 7, and a control circuit 9 for controlling the PFC circuit. An AC source 11 provides an AC signal applied over a first input 12 of the AC- DC converter 1. For illustrative reasons a load 13 is connected over the exit of the ACDC converter 1. The load 13 is provided with the generated DC signal from the AC-DC converter 1.

The AC signal from the AC source 11 is rectified by the rectifier 3 into a first rectified AC signal from a first output 14 of the rectifier 3 . The first rectified AC signal is applied over a second input 16 of the voltage scaling circuit 5 . The voltage scaling circuit 5 will apply a scaling factor above one to the first rectified AC signal only if the first rectified AC signal has a peak voltage within a certain lower range, or the voltage scaling circuit 5 will apply a scaling factor below one to the first rectified AC signal only if the first rectified AC signal has a peak voltage within a certain upper range.

The first rectified AC signal maybe boosted, reduced or left uninfluenced by the voltage scaling circuit 5 and applied as a second rectified AC signal over a second output 17 connected to a third input 18 of the PFC circuit 7.

However there is a gain to a lower range or an upper range is reduced, the result is that the PFC circuit 7 is exposed to a signal with more or less the same voltage irrespective of the voltage of the AC signal from the AC source 11, since the AC signal is in most cases either around $120 \mathrm{~V}_{\mathrm{RMs}}$ or around $230 \mathrm{~V}_{\mathrm{RMs}}$. That the PFC circuit 7 is exposed to a signal with more or less the same voltage means that the PFC circuit 7 can be made much more specific and does not need to be able to handle both 120 $\mathrm{V}_{\text {RMs }}$ and $230 \mathrm{~V}_{\text {RMs. }}$. The more specific PFC circuit can be made smaller, more efficient, and with a with a better power factor at a lower production cost.

The PFC circuit 7 will apply a DC voltage over the load 13.

The control circuit 9 has a first control circuit input 20 for reading the first rectified AC signal from the first output of the rectifier 3 and/or the second rectified AC signal from the second output of the voltage scaling circuit 5 as well as a second control circuit input 22 for reading the generated constant DC signal from the AC-DC converter 1.

The control circuit 9 also has a control circuit output 24 for controlling the PFC circuit 7 so that the power factor is close to 1 before the conversion to the DC voltage.

## Example

Fig. 2a shows an example of the voltage scaling circuit as a switched-capacitor circuit 32 with the second input 16 and the second output 17.

The switched-capacitor circuit 32 comprises
an out-capacitor ( $C_{\text {out }}$ ) 34 parallel over the second output 17 and connecting a node N1 and a node N2, a first switch 36 , a second switch 38 and the out-capacitor, wherein the first switch and the second switch are connected in a node N3, wherein the node N3 is connected to the node N1 by the first switch 36 and to the node N2 by the second switch 38 , a fly-capacitor ( $C_{\text {fiy }}$ ) 40 connecting the node N 3 to a node N4, a third switch 42 connecting the node N 2 to the node N 4 , a fourth switch 44 connecting the node N 4 to a node N 5 , and an in-capacitor ( $\left.C_{\text {in }}\right) 46$ parallel over the second input 16 and connecting the node N5 and the node N1.

In the switched-capacitor circuit 32, either the first switch 36 and the third switch 42 are conducting simultaneously or the second switch 38 and the fourth switch 44 are conducting simultaneously.

Fig. 2 b shows an example of the voltage scaling circuit as a buck converter 47 with features, which can be similar or the same as in features of Fig. 2a having the same reference numbers. The buck converter 47 has the second input 16, and the second output 17, wherein the voltage over the second output 17 is lower than the voltage over the second input 16. The buck converter can have a scaling factor with any number below one.

The buck converter 47 comprises
an out-capacitor ( $C_{\text {out }}$ ) 34 parallel over the second output 17 and connecting a node N 1 and a node N 2 , a first inductor 48 connecting the node N 2 to a node N 6 , a fifth switch 49 connecting the node N6 to the node N1,
a sixth switch 50 connecting the node N 6 to a node N 5 , and an in-capacitor $\left(C_{\text {in }}\right) 46$ parallel over the second input 16 and connecting the node N5 and the node N1.

The fifth switch 49 and the sixth switch 50 are closed interchangeably. When the sixth switch 50 is closed (conducting) and the fifth switch 49 is open (non-conducting), the voltage over the second input 16 will drive an increasing current through the first inductor 48 and the out-capacitor ( $C_{\text {out }}$ ) 34, increasing the voltage over the second output 17 . When the sixth switch 50 is open and the fifth switch 49 is closed, voltage over the second input 16 is removed from the circuit, and the current will decrease, decreasing the voltage over the second output 17.

The skilled person will understand that the buck converter can have different designs.

Fig. 2c shows an example of the voltage scaling circuit as a buck/boost converter 51 with features which can be similar or the same as in features of Figs. $2 a$ and $2 b$ having the same reference numbers. The buck/boost converter 51 has the second input 16 and the second output 17. The buck/boost converter can have a scaling factor with any number below one or above one.

The buck/boost converter 51 comprises
an out-capacitor ( $C_{\text {out }}$ ) 34 parallel over the second output 17 and connecting a node N 1 and a node N 2 , a seventh switch 52 connecting the node N 2 to a node N6, a second inductor 53 connecting the node N 6 to the node N 1 , a sixth switch 50 connecting the node N 6 to a node N 5 , and an in-capacitor ( $\left.C_{\text {in }}\right) 46$ parallel over the second input 16 and connecting the node N5 and the node N1.

The sixth switch 50 and the seventh switch 52 are closed interchangeably. The skilled person will understand that the buck/boost converter can have different designs.

Fig. 2d shows an example of the voltage scaling circuit as a forward converter 54 with features which can be similar or the same as in features of Figs. $2 \mathrm{a}, 2 \mathrm{~b}$ and/or 2 c having the same reference numbers. The forward converter 54has the second input 16
and the second output 17. The forward converter 54 can have a scaling factor with any number below one or above one.

The forward converter 54 comprises
an out-capacitor ( $C_{\text {out }}$ ) 34 parallel over the second output 17 and connecting a node N1' and a node N2, a third inductor 55 connecting the node N 2 to a node N 7 , a first diode 56 connecting the node N7 to the node N1' and allowing current to pass from the node N 1 ' to the node N7, a second diode 57 connecting the node N7 to a node N8 and allowing current to pass from the node N8 to the node N7, an in-capacitor $\left(C_{\text {in }}\right) 46$ parallel over the second input 16 and connecting the node N5 and the node N1", a third diode 58 connecting the node N1" to a node N9 and allowing current to pass from the node N1" to the node N9, a demagnetization winding 59 of a transformer 60 connecting the node N 9 to the node N5,
a seventh switch 61 connecting the node N 1 " to a node N 10 , a main primary winding 62 of the transformer 60 connecting the node N10 to the node N5, wherein the demagnetization winding 59 and the main primary winding 62 together make up a primary winding, and a secondary winding 63 of the transformer 60 connecting the node N8 to the node N1'.

The skilled person will understand that the forward converter can have different designs and how the forward converter works.

## Theoretical Approach

The proposed topology can use a switched-capacitor (SC) front-end to lower the input voltage of a PFC circuit in the case of high AC line voltage. In the case of low AC line voltage, the SC circuit or SC converter can instead be bypassed using internal switches $\left(Q_{3}\right.$ and $Q_{4}$ in Fig. 2) of the SC converter. The system is illustrated in Fig. 1. Using a 2:1 voltage step-down SC converter, this topology limits the maximum PFC circuit input RMS voltage to be $240 \mathrm{~V} / 2=120 \mathrm{~V}$. The range of PFC circuit input voltages is therefore greatly reduced compared to the conventional universal single-
stage solution. Furthermore, the PFC circuit output voltage, which is usually 400 V for a boost converter PFC, can be halved to 200 V and thereby reduce the voltage stress of any following DC-DC converter. Finally, control of the PFC circuit can be simplified due to the reduced input voltage range, and a properly designed frontend SC can in principle be added to any pre-existing PFC circuit without modification.

To analyse the effect of the front-end SC converter on the PFC circuit 7 in Fig. 1, the simplified schematic in Fig. 3 is utilized. The SC converter can be modelled as a DCDC transformer 70. For this analysis, an ideal converter with $100 \%$ efficiency is assumed, i.e. the output resistance is set to zero, and the PFC circuit is assumed to ensure ideal unity power factor. In addition, the PFC circuit is assumed to use the voltage at the second output from the SC converter as the sensing input for PFC control. A total effective capacitance C 71 seen at the output of the SC converter is included in the circuit, and a resistor $R_{p f c} 72$ models the load of the following PFC circuit. The forward drop of the rectifier diodes is assumed insignificant, but the series rectifier resistance 73 is included, since it is useful for the subsequent mathematical analyses.

In this model, the AC line voltage, $v_{a c}$, drives an AC current, $i_{a c}$. The AC current is rectified by the rectifier 3 so that a rectified current, $i_{\text {rect, }}$ flows on the other side of the rectifier. Likewise, the AC line voltage, $v_{a c}$, is rectified to $v_{\text {rect }}$, which drops over a series rectifier resistance, $R_{\text {rect, }}, 73$ down to a SC-input voltage, $v_{s c, i n}$, applied over the input of the DC-DC transformer 70. Since the DC-DC transformer 70 has been chosen in this case to have the ratio $2: 1$, a double rectified current, $2 i_{\text {rect, }}$, is driven by a capacitor voltage, $v_{c}$, which will be half of $v_{s c, \text { in }}$ in this case.

For large values of $C$, the circuit operates with narrow current pulses at the line voltage peak similar to the operation of a traditional AC-DC converter using a diode bridge and bulk capacitor. For small values of $C$, the current waveform approaches that of a purely resistive load. An intermediate effective capacitance can cause the circuit to operate with the input and output current and voltage waveforms shown in Fig. 4. During the interval $\phi_{1} \rightarrow \phi_{2}$, the diode bridge can be conducting and the output voltage can be scaled to half the input voltage by the SC converter. During the interval $\phi_{2} \rightarrow \pi+\phi_{1}$, the diodes can be reverse biased and the output voltage can be an exponential decay with
the time constant $\tau=R_{p f c} C$. The following analysis considers the boundaries between these two operating modes to determine the angles $\phi_{1}$ and $\phi_{2}$.

## A. Conduction Boundaries

First, the rectifier diodes are assumed to be conducting. The differential equation (1) is constructed to describe the current delivered to the PFC stage. A cosine is used for the AC source, as this simplifies the following derivation.

$$
\begin{align*}
\frac{v_{c}(t)}{R_{p f c}} & =2 i_{\text {rect }}(t)-C \frac{d v_{c}(t)}{d t}  \tag{1}\\
& =2 \frac{v_{a c} \cos (\omega t)-2 v_{c}(t)}{R_{\text {rect }}}-C \frac{d v_{c}(t)}{d t}
\end{align*}
$$

This equation is solved using the initial condition $v_{c}(0)=v_{a c}$, yielding the result in (2).

$$
\begin{gather*}
v_{c}(t)=\left(v_{a c}-a b\right) e^{-a t}+a b \cos (\omega t)+b \omega \sin (\omega t) \\
a=\left(R_{\text {rect }}+4 R_{p f c}\right) /\left(R_{\text {rect }} R_{p f c} C\right)  \tag{2}\\
b=2 v_{a c} /\left(R_{\text {rect }}\left(\omega^{2}+a^{2}\right) C\right)
\end{gather*}
$$

Utilizing the reasonable assumptions $R_{\text {rect }} \ll R_{p f c}$ and $R_{\text {rect }} C \ll 1$, it follows directly that $\alpha \gg 1$. Equation (2) can therefore be simplified to (3).

$$
\begin{equation*}
v_{c}(t) \approx a b \cos (\omega t)+b \omega \sin (\omega t) \tag{3}
\end{equation*}
$$

When the capacitor voltage of (3) is equal to half the AC voltage, as expressed in (4), the boundary between sinusoidal and exponentially decaying capacitor voltage is found.

$$
\begin{equation*}
a b \cos (\phi)+b \omega \sin (\phi)=\frac{v_{a c}}{2} \cos (\phi) \tag{4}
\end{equation*}
$$

From this equation an expression for the angle $\phi_{2}$ can be obtained, which is given in (5). Note that $\phi_{2}$ is the solution to (4) plus an additional $\pi / 2$, since a cosine was used in (1), while the angle $\phi_{2}$ is defined referenced to a sine, see Fig. 4.

$$
\begin{align*}
\phi_{2} & =\arctan \left[\left(v_{a c}-2 a b\right) /(2 b \omega)\right]+\pi / 2  \tag{5}\\
& \approx \arctan \left[\left(\omega R_{p f c} C\right)^{-1}\right]+\pi / 2
\end{align*}
$$

The approximation in (5) is valid for an ideal diode rectifier with zero series resistance 73 , i.e. $R_{\text {rect }}=0$.

Following the transition from sinusoidal to decaying voltage waveform after time $\phi_{2}$, the output voltage is given by (6), in which the time $t$ is referred to the transition point $\phi_{2}$.

$$
\begin{equation*}
v_{c}(t)=\frac{v_{a c}}{2} \sin \left(\phi_{2}\right) e^{-t /\left(R_{p f c} C\right)} \tag{6}
\end{equation*}
$$

The boundary $\phi_{1}$ where the rectifier diodes begin to conduct can be found by solving (7).

$$
\begin{gather*}
\frac{v_{a c}}{2} \sin \left(\phi_{2}\right) e^{-t_{1} /\left(R_{p f c} C\right)}=-\frac{v_{a c}}{2} \sin \left(\omega t_{1}+\phi_{2}\right)  \tag{7}\\
t_{1}=\left(\phi_{1}-\phi_{2}+\pi\right) / \omega
\end{gather*}
$$

Using the small angle approximation $\sin \left(\phi_{1}\right)=\phi_{1}$, it can be shown that $\phi_{1}$ is approximated by (8), where $W_{0}$ is the principal branch of the Lambert $W$ function.

$$
\begin{equation*}
\phi_{1} \approx W_{0}\left(\frac{\sin \left(\phi_{2}\right) e^{\left(\phi_{2}-\pi\right) /\left(\omega R_{p f c} C\right)}}{\omega R_{p f c} C}\right) \omega R_{p f c} C \tag{8}
\end{equation*}
$$

Note that the expressions (5) and (8) describing $\phi_{2}$ and $\phi_{1}$ respectively, are only functions of the effective capacitance seen at the output of the switched-capacitor (SC) converter, the equivalent load resistance of the PFC circuit and the AC mains frequency or line frequency.

## B. Power Factor

The total system Power Factor (PF) is of course the ratio of active to apparent power as seen from the AC supply, which is given by (9).

$$
\begin{equation*}
P F=P_{i n, a v g} /\left(v_{a c, r m s} i_{a c, r m s}\right) \tag{9}
\end{equation*}
$$

From the schematic in Fig. 3 and the current waveform in Fig. 4, it can be identified that the AC current is described by (10), in which the capacitor voltage

$$
v_{c}(t)=\left|v_{a c} / 2 \sin (\omega t)\right|
$$

for the time interval of non-zero AC current.

$$
\begin{align*}
&\left|i_{a c}(t)\right|=\frac{1}{2}\left(C \frac{d v_{c}(t)}{d t}+\frac{v_{c}(t)}{R_{p f c}}\right), \\
& i_{a c}=0 \quad, \phi_{1}+n \pi<\omega t<\phi_{2}+n \pi  \tag{10}\\
&, \text { otherwise }
\end{align*}
$$

From the symmetry of the positive and negative halves of the periodic current waveform, the instantaneous and RMS value of the AC current can be determined. Assuming the AC voltage to be sinusoidal, it is therefore trivial to calculate the PF in (9) for a given AC voltage, output load and effective capacitance.

## C. Effective Capacitance

The SC converter's effective output capacitance is a weighted sum of its input, output and flying capacitance. The output capacitance add directly to the effective capacitance, while the input capacitance is scaled by the squared 'turns ratio' of the DC transformer i.e. the ideal SC conversion ratio. The effect of the flying capacitance can in general be dependent on the topology and operation of the SC converter. In this work, a two-phase 2:1 conversion ratio SC as shown in Fig. 2 have been implemented. For this topology, the flying capacitance adds directly to the effective capacitance, and (11) is therefore the expression for calculating the effective capacitance.

$$
\begin{equation*}
C=C_{\text {out }}+\alpha_{s c} C_{f l y}+C_{i n} / N^{2}=C_{o u t}+C_{f l y}+C_{i n} / 4 \tag{11}
\end{equation*}
$$

where N is the voltage scaling factor of the SC converter, when the conversion ratio is described in the form $\mathrm{N}: 1$. For scaling factor of $1 / 2$, the ratio is $2: 1$, and hence $\mathrm{N}=2$
$\alpha_{s c}$ is a topology dependent weight factor used to model how much the flying capacitance adds to the effective capacitance 'seen' at the SC converter output.

## Implementation and Experimental Results

A high PF SC converter has been designed for nominal EU mains input ( 50 Hz , $230 V_{\text {rms }}$ ) and 50 W output power. The calculated relation between effective capacitance, power factor 78 and current displacement 79 for this specification is shown in Fig. 5. The current displacement is calculated from the first harmonic of the Fourier series decomposition of (10). As expected higher values of effective capacitance causes an increase in current displacement and decrease in PF.

By obtaining greater than 99\% PF it is shown that the SC converter can be designed to have negligible effect on PF. From Fig. 5 it is seen that such performance is expected with effective capacitance lower than $1,6 \mu \mathrm{~F}$. The schematic in Fig. 2 was implemented using the components in Table I. The converter was operated at 270 kHz . An input filter constructed from a $100 \mu \mathrm{H}$ inductor and 30 nF capacitor was also added, where the input filter was placed before the rectifier with the capacitor in parallel to the rectifier input and the inductor in series with one of the AC input wires.

TABLE I
Critical components used for implementation of SWITCHED-CAPACITOR CONVERTER.

|  | Manufacturer \& Part no. | Description | Amount |
| :---: | :--- | :---: | :---: |
| $Q_{1-4}$ | GaN Systems GS-065-004-1-L | GaN, $0.5 \Omega$ | 4 |
| $C_{\text {in }}$ | TDK C3216C0G2W153J160AA | 15 nF, C0G | 2 |
| $C_{f l_{y}}$ | TDK CKG45NC0G2W943J500JJ | $94 \mathrm{nF}, \mathrm{C0G}$ | 6 |
| $C_{\text {out }}$ | TDK CGA8P3X7T2E105K250KA | $1 \mu \mathrm{~F}$, X7T | 1 |

The measured line voltage, $v_{a c}, 80$ and current, $i_{a c}$, 82 as well as the output voltage 84 of the SC converter are shown in Fig. 6. In Fig. 6 measurements are without PFC circuit, i.e. only rectifier, SC converter and load are cascaded. This is directly comparable to the theoretical waveforms in Fig. 4. The current waveform is sinusoidal with small non-conducting intervals around the voltage zero crossing as expected. The performance was quantified using a Newtons4th PPA5530 power analyser at half and full power with the results in Table II. The 50W metrics are marked with circles in Fig. 5, where a circle around an " $x$ " means the measured PF and a circle around " + " means the measured current phase for the 50W metrics. The measured PF and measured current phase show good agreement between calculated and measured performance.

TABLE II
Measured performance of the switched-Capacitor converter at half and full output power.

|  | 25 W | 50 W |
| :--- | :---: | :---: |
| PF [\%] | 97.3 | 99.1 |
| PF (fundamental) [\%] | 97.8 | 99.3 |
| Current displacement [deg] | 12.1 | 6.7 |
| Current THD [\%] | 6.9 | 2.8 |
| Efficiency [\%] | 96.6 | 97.1 |

To further validate the developed model, $\mathrm{C}_{\text {fly }}$ was increased using $1 \mu \mathrm{~F}$ X7T capacitors, since COG capacitors became impractically large, and PF was again measured. The measured PF values and the measured current phase values are shown in Fig. 5 by the " $x$ " and " + " signs, respectively. The results are marked in Fig. 5 with their effective capacitance corrected for capacitance decrease with voltage bias at the transition time $\phi_{2}$. Even though the calculations assume ideal capacitors, the model and measurements are well correlated.

Finally, the SC converter was combined with a conventional PFC boost converter to verify the complete system functionality. The boost converter was based on a reference design for the Texas Instruments UCC28056 controller and slightly modified to output 210 V . Measured current 90 , line voltage, $\mathrm{vac}_{\mathrm{ac}}, 92$, and output voltage, $\mathrm{v}_{\mathrm{out}, \mathrm{sc}}, 94$ for the complete system are shown in Fig. 7. In Fig. 7 measurements are with all blocks including PFC circuit, i.e. rectifier, SC converter, PFC (boost converter in this proof-ofconcept implementation) and load are cascaded. The system performance at 50 W output is quantified in Table III.

TABLE III
MEASURED PERFORMANCE OF THE SWITCHED-CAPACITOR CONVERTER, BOOST CONVERTER AND COMPLETE SYSTEM AT 50 W OUTPUT POWER.

|  | SC | Boost | Total |
| :--- | :---: | :---: | :---: |
| PF [\%] | 99.1 | 98.7 | 94.3 |
| PF (fundamental) [\%] | 99.3 | 99.5 | 97.4 |
| Current displacement [deg] | 6.7 | 6.0 | 13.2 |
| Current THD [\%] | 2.8 | 12 | 10.5 |
| Efficiency [\%] | 97.1 | 95.0 | 92.5 |

The current displacement is only slightly affected by the addition of the boost converter as seen from the high fundamental PF. However, the boost contributes with a significant amount of distortion, which lowers the overall PF. Likewise, the boost converter is the bottleneck for system power efficiency. Hence, to improve the overall system performance, the boost converter should be optimized for the lower input and output voltage, but it is not an absolute necessity as is apparent from these results.

## Conclusion

A switched-capacitor front-end for universal PFC circuits has been presented and analysed. This front-end reduces the voltage stress of the PFC circuit and significantly limits the input voltage range, which allows for better optimization of the PFC circuit. Through circuit analysis, the front-end's effect on system power factor has been modelled. Experimental results for such front-end showed good correlation between calculated and measured performance. The implemented switched capacitor front-end by itself obtained $99,1 \%$ power factor at 50 W output power and $97,3 \%$ power factor at 25W output power. Finally, the switched-capacitor front-end was combined with a low voltage boost converter PFC circuit, which resulted in 94,3\% power factor and 92,5\% efficiency at full load with 230V RMS input. The implemented prototype shows that the
proposed topology is capable of providing good power factor without any additional control efforts. The full potential of the topology is still to be shown through optimization of the PFC circuit for reduced input voltage range.

## Claims

1. An AC-DC converter comprising

- a rectifier comprising
- a first input configured to receive an AC signal, and
- a first output, wherein the rectifier is configured to rectify the AC signal to a first rectified $A C$ signal having a first $\mathrm{V}_{\text {RMS }}$,
- a voltage scaling circuit comprising
- a second input connected to the first output, wherein the second input is configured to receive the first rectified AC signal, and
- a second output,
wherein the voltage scaling circuit is configured, if the first $V_{\text {RMS }}$ is within a first voltage range, to scale the first rectified AC signal by a first scaling factor generating a second rectified AC signal,
- a power factor correction (PFC) circuit for keeping the current in phase with and proportional to the voltage of the second rectified AC signal. the PFC circuit comprising
- a third input connected to the second output, and
- a third output configured to supply a DC signal on an AC-DC converter-output.

2. The AC-DC converter according to claim 1 , wherein the voltage scaling circuit is a switched-capacitor circuit.
3. The AC-DC converter according to any of the preceding claims, wherein the first voltage range is

- a certain lower range, which preferably is below a first limit, or
- a certain upper range, which preferably is above the first limit , wherein the first limit is between 140 and $200 \mathrm{~V}_{\mathrm{Rms}}$, more preferably between 150 and $180 \mathrm{~V}_{\text {RMs }}$.

4. The AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is configured to scale the first rectified AC signal by a second scaling factor different from the first scaling factor, if the first $\mathrm{V}_{\text {RMs }}$ is
within a second voltage range different from the first voltage range generating a third rectified AC signal.
5. The AC-DC converter according to claim 4, wherein the second voltage range is the certain upper range if the first voltage range is the certain lower range, and the second voltage range is the certain lower range if the first voltage range is the certain upper range.
6. The AC-DC converter according to claim 4 or 5 , wherein the first scaling factor and the second scaling factor

- are both above one, or
- are both below one, or
the first scaling factor is above one and the second scaling factor is below one, or vice versa.

7. The AC-DC converter according to any of the preceding claims, wherein the AC-DC converter comprises a control circuit for controlling the PFC circuit based on the first rectified AC signal of the second input and/or the second rectified AC signal of the second output and/or the DC signal of the third output.
8. The AC-DC converter according to claim 4, wherein the control circuit controls the power factor of the PFC circuit by minimising the phase shift between the voltage and the current of the second rectified AC signal.
9. The AC-DC converter according to any of the preceding claims, wherein the first scaling factor is 2 if the first $V_{\text {RMs }}$ is within the certain lower range, or
wherein the first scaling factor is $1 / 2$ if the first $V_{R M S}$ is within the certain upper range.
10. The AC-DC converter according to any of the preceding claims, wherein the first scaling factor is 2 if the first $\mathrm{V}_{\text {Rms }}$ is within the certain lower range, and the scaling factor is 1 otherwise, or wherein the first scaling factor is $1 / 2$ if the first $\mathrm{V}_{\text {RMs }}$ is within the certain upper range, and the first scaling factor is 1 otherwise
11. The AC-DC converter according to any of the preceding claims, wherein the AC-DC converter comprises at least one switch for bypassing the voltage scaling circuit, wherein the voltage scaling circuit is bypassed when the first $\mathrm{V}_{\text {RMs }}$ is outside the certain lower range or the certain upper range.
12. The AC-DC converter according to any of the preceding claims 2-11, wherein the switched-capacitor circuit comprises

- an out-capacitor, $\mathrm{C}_{\text {out }}$, parallel over the second output and connecting a node N1 and a node N2,
- a first switch, $Q_{1}$, a second switch, $Q_{2}$, and the out-capacitor, wherein the first switch and the second switch are connected in a node N3, wherein the node N 3 is connected to the node N1 by the first switch and to the node N 2 by the second switch,
- a fly-capacitor, $\mathrm{C}_{\text {fiy }}$, connecting the node N3 to a node N4,
- a third switch, $\mathrm{Q}_{3}$, connecting the node N 2 to the node N 4 ,
- a fourth switch, $\mathrm{Q}_{4}$, connecting the node N4 to a node N5,
- an in-capacitor, $\mathrm{C}_{\mathrm{in}}$, parallel over the second input and connecting the node N5 and the node N1,
wherein either $Q_{1}$ and $Q_{3}$ are conducting simultaneously or $Q_{2}$ and $Q_{4}$ are conducting simultaneously.

13. The $A C-D C$ converter according to any of the preceding claims $2-12$, wherein the switched-capacitor circuit comprises ten or less switches, preferably 8 or less switches, more preferably 6 or less switches, and most preferably 5 or less switches.
14. The high power density AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is

- a step-down converter, or
- step-up converter.

15. The high power density AC-DC converter according to any of the preceding claims, wherein the step-up/down converter steps down or up the voltage depending on the voltage of the AC signal or of the first rectified AC signal.

## Universal Mains High Power-Density AC-DC Converter


#### Abstract

The invention regards an AC-DC converter comprising a rectifier comprising a first input configured to receive an AC signal, and a first output, wherein the rectifier is configured to rectify the $A C$ signal to a first rectified $A C$ signal having a first $\mathrm{V}_{\text {RMs }}$, a voltage scaling circuit comprising a second input connected to the first output, wherein the second input is configured to receive the first rectified AC signal, and a second output, wherein the voltage scaling circuit is configured, if the first $\mathrm{V}_{\mathrm{RMS}}$ is within a first voltage range, to scale the first rectified AC signal by a first scaling factor generating a second rectified AC signal, a power factor correction (PFC) circuit for keeping the current in phase with and proportional to the voltage of the second rectified AC signal. the PFC circuit comprising a third input connected to the second output, and a third output configured to supply a DC signal on an AC-DC converter-output.




Fig. 1


Fig. 2a


Fig. 2d


Fig. 3


Fig. 4


Fig. 5


Fig. 6


Fig. 7

## Appendix [J1]

N. J. Dahl, A. M. Ammar, A. Knott and M. A. E. Andersen, "An Improved Linear Model for High Frequency Class-DE Resonant Converter using the Generalized Averaging Modeling Technique," in IEEE Journal of Emerging and Selected Topics in Power Electronics, October 2019.

# An Improved Linear Model for High Frequency Class-DE Resonant Converter using the Generalized Averaging Modeling Technique 

Nicolai J. Dahl, Student Member, IEEE, Ahmed M. Ammar, Student Member, IEEE, Arnold Knott, Michael A. E. Andersen, Member, IEEE


#### Abstract

As the operating frequency of power converters increases, the passive component values likewise decrease. This results in the effect of the parasitic components becoming more prominent, leading to significant modeling errors if not considered. For resonant converters this especially becomes a problem at high frequencies. This paper presents a reduced model for a class-DE series resonant converter based on generalized averaging that incorporates the relevant parasitics and uses multiple harmonics to obtain an accurate linear model. Comparison between the proposed model, prior art, and a prototype converter running at 1 MHz is conducted, and a PI-controller is designed based on each model and tested. The results show that the parasitics have a significant impact on the DC-gain and dynamics of the converter, and that the proposed model improves on the prior art by reducing the DC-gain error by more than 7 dB , and the error in the low frequency pole from $168 \%$ to 16.9 \%. Furthermore, the PI-controller designed on the prior art was found to have more than 40 times larger overshoot in the control signal when measured compared to the model prediction, while the controller based on the proposed model showed correct performance when simulated and measured.


Index Terms-Resonant converters, Modeling, PI control, State-space methods, DC-DC power converters.

## I. Introduction

TODAY, most electronic devices are powered with a Switch Mode Power Supply (SMPS) due to their small form factor and high efficiency. The majority of the SMPS are different types of hard switching PWM topologies. These supplies have high switching losses which limit the switching frequency that the supplies can handle. Nonetheless, higher switching frequencies allow for smaller passive components, and hence an overall smaller power supply, as well as higher bandwidth to better react to various load and line disturbances. Therefore, to improve on the switching frequencies, soft switching topologies have been receiving much attention in recent years [1-7]. One family of soft switching converters are the resonant converters [8]. Resonant converters work by having a resonant tank take care of charging and discharging the switching node before the switching event, and thus obtain Zero Voltage Switching (ZVS). This vastly reduces the switching losses, allowing for a higher operation frequency.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby (e-mail: nicoje@elektro.dtu.dk; ammma@elektro.dtu.dk; akn@elektro.dtu.dk; ma@elektro.dtu.dk)

The typical design and modeling procedures used for PWM converters do not apply to resonant converters. PWM converter models are fundamentally built on the small ripple hypothesis, meaning that the ripple can be averaged and only the underlying linear dynamics need to be considered [9, 10]. This is not applicable with resonant converters as it would average out the resonance in the resonance tank to zero. To resolve this, models that are able to capture the periodic behavior have been developed. One modeling approach is to model the converter using multiple subsystems connected with a reset map [11-13]. This method maintains all the information of the converter, but is not very pratical for most analysis and control design. Another modeling approach which has recieved a lot of attention in the modeling of active front ends is the Linear Time-Varying Periodic (LTP) model [14-18]. This method uses a harmonic state space model to descripe how each of the harmonic components of the input impact each of the harmonic components of the output. Lastly, there are the modeling approaches based on the generalized averaging model [19-22]. This modeling approach extends the original averaging model method by describing the periodic behavior of the system using a Fourier series. Many of these modeling approaches come with a set of assumptions to simplify the problem. These assumptions are typical about purely sinusoidal signals or fast decaying harmonics, resulting in solutions which are only valid in a limited range if not fulfilled. Furthermore, the prior art, that uses the modeling techniques presented above, only considers converters operating at frequencies up to 200 kHz . At these frequencies, the parasitic components are negligible, and for that reason not included in the models. However, with the increase in operating frequency, this is no longer the case and the models breaks down.

This paper presents a model of a class-DE Series Resonant Converter (SRC) where the effect of the parasitics is included to make the model valid for high-frequency operation. The model is based on the generalized averaging method, and considers multiple harmonics to obtain a precise representation of the converter behavior. The resulting model is of a high-order, so a model reduction approach is applied to simplify the model to a low order, high precision, and computational robust linear model which is valid for a wide operation range. The proposed reduced model is validated against a 1 MHz class-DE SRC and compared to prior art. Lastly, a PI-controller is designed
based on both the proposed model and prior art, and tested to assess the performance improvement. Although the presented model is for a class-DE SRC, the presented modeling method with the same parasitics can also be used to model variations of the class-DE resonant network, like the LLC, LCC, and parallel resonant converter.

## II. Large Signal Model

Using Kirchoff's current and voltage laws, the discontinuous differential equations governing the behavior of the class-DE converter shown in Fig. 1 are established. Equation (1) shows the derived equations which are similar to the findings in [21], but also include the equivalent series resistance for the capacitor and inductor, here lumped together in $R_{e s r}$ (not shown in the circuit).

$$
\begin{align*}
& \dot{I}_{r}=\frac{V_{s w}}{L_{r}}-\frac{V_{r}}{L_{r}}-I_{r} R_{e s r}-\frac{V_{h b}}{L_{r}}  \tag{1a}\\
& \dot{V}_{r}=\frac{I_{r}}{C_{r}}  \tag{1b}\\
& \dot{V}_{o}=\frac{I_{h b}}{C_{f}}-\frac{V_{o}}{C_{f} R_{f}} \tag{1c}
\end{align*}
$$

where $I_{r}$ is the periodic current in the resonance tank, $V_{r}$ is the voltage across the resonance tank capacitor $C_{r}$, and $V_{o}$ is the output voltage of the converter. $V_{s w}, V_{h b}$, and $I_{h b}$ are the switching node voltage, the voltage at the rectifier, and the current through the rectifier to the output, respectively, and are all piece-wise continuous functions. In reported work [20, 21] these piece-wise continuous functions are assumed to be ideal, e.g. the effect of parasitic components is disregarded. This is a fair assumption for medium frequency operation ( $<500 \mathrm{kHz}$ ) where it provides satisfactory results. However, as the switching frequency is increased, the capacitor and inductor sizes in the resonance tank decrease and the parasitic components of the switching devices start to become significant and interact with the converter. The parasitics, among other factors, cause a change in the resonance frequency and delaying of charge transfer in the rectifier. Therefore, to obtain an accurate model of the converter at high frequency switching, the relevant parasitics need to be identified and included in the model.

The dominant parasitics come from the switching devices in the converter, i.e. the FETs and the diodes, and are capacitive by nature. Thus the output capacitance of the FETs, $C_{o s s}$, and the capacitance of the diodes, $C_{d}$ are added to the model. Both of these capacitors are nonlinear dependent of the voltage across the device, and will change in value during charging/discharging. Hence, the capacitor values are approximated by the time related capacitors to give an equivalent behavior. The parasitics in the resonant tank are, in the MHz range, usually insignificant in size, and thus not considered in the model. Fig. 1 shows the class-DE series resonant converter with the relevant parasitics.


Fig. 1: The class-DE series resonant converter with the parasitic capacitance for the FET's and diodes. The ESR resistances of $L_{r}$ and $C_{r}$ are not explicitly shown in the circuit, but still included in the calculations.

Looking at Fig. 1 it is seen that all the parasitic components are connected to nodes that are discontinuous and hence need to be described by piece-wise functions. To work out the exact behavior of these piece-wise functions, a transient simulation of the converter is performed. Fig. 2 shows the steady state operation of the discontinuous nodes $V_{h b}, I_{h b}$ and $V_{s w}$ in normalized time.


Fig. 2: The discontinuous waveforms of the converter. The dashed lines indicate the conduction time of the rectifier.

From Fig. 2, the effects of the added parasitics are observed. Once the resonance current $I_{r}$ becomes positive (about $\pi / 4$ ), the diode capacitance $C_{d}$ starts charging hence increasing the voltage in $V_{h b}$. This prevents the charge transfer in the rectifier to the output since the forward voltage of the diodes is yet to be reached. Then, when $V_{h b}=V_{o}$ the diode can start conducting and will keep on conducting until the resonance current becomes negative. At that point, the diode capacitance will be discharging. In the ideal case, $V_{h b}$ would ramp up instantaneously, allowing the current to be passed to the output for the entire positive half-cycle. However, due to the parasitic
capacitance in the rectifier diodes, this is no longer the case.
Regarding the switching node, $V_{s w}$, it resembles a square waveform, however, with a small slope on the edges. The slopes come from the charging and discharging of the $C_{\text {oss }}$ during the dead time of the gate signals when none of the FETs are conducting. This leads to the system being in its unforced stage, and the resonance current will charge/discharge $C_{\text {oss }}$. The length of the dead time is given by $\pi(1-2 D)$ where $D$ is the positive duty cycle of the gate signals to the FETs. Ideally, it is desired to tune the duty cycle such that $C_{o s s}$ is charged to $V_{s}$ and zero voltage switching occurs. In case $C_{o s s}$ is over charged, diodes in parallel with $C_{o s s}$ will start conducting, limiting the voltage. However, these diodes are not included in Fig. 1 and neither in the presented model since it would lead to $V_{s w}$ being piece-wise in both time and voltage. Functions that are piece-wise in more than one variable are increasingly difficult to model and approximate as the problem becomes multidimensional. Hence the complete model is only valid in operation modes where these diodes are not conducting, i.e. partial and full ZVS. In operation modes where the diodes are conducting, the model will over charge the voltage in the switching node, $V_{s w}$ to maintain the resonant current. Thus the resonant current and output voltage remain valid in this operation mode, and only $V_{s w}$ will differ from the expected behavior.

From the behavior described above the piece-wise equations are formalized. Equation (2) to (4) shows the piece-wise functions. Each equation is periodic, i.e. $f(t)=f(t+2 \pi)$, and $\phi$ represents the phase shift observed in Fig. 2.

$$
\begin{align*}
& V_{h b}(t-\phi)= \begin{cases}\frac{\int I_{r} \mathrm{~d} t}{2 C_{d} \omega} & 0 \leq t<t_{o n} \\
V_{o} & t_{o n} \leq t<\pi \\
\frac{\int I_{r} \mathrm{~d} t}{2 C_{d} \omega}+V_{o} & \pi \leq t<\pi+t_{o n} \\
0 & \pi+t_{o n} \leq t<2 \pi\end{cases}  \tag{2}\\
& I_{h b}(t-\phi)= \begin{cases}0 & 0 \leq t<t_{o n} \\
I_{r} & t_{o n} \leq t<\pi \\
0 & \pi \leq t<2 \pi\end{cases}  \tag{3}\\
& V_{s w}(t)= \begin{cases}\frac{\int-I_{r} \mathrm{~d} t}{2 C_{o s} \omega} & 0 \leq t<\pi(1-2 D) \\
V_{s} & \pi(1-2 D) \leq t<\pi \\
\frac{\int-I_{r} \mathrm{~d} t}{2 C_{o s} \omega}+V_{s} & \pi \leq t<2 \pi(1-D) \\
0 & 2 \pi(1-D) \leq t<2 \pi\end{cases} \tag{4}
\end{align*}
$$

where $\omega$ is the switching frequency $f_{s w}$ in $\mathrm{rad} / \mathrm{sec}$, and $t_{o n}$ is the point where $I_{h b}$ becomes non-zero. If $\omega$ is assumed to be constant, the equations become piece-wise linear. $t_{o n}$ is found as the time it takes to charge both $C_{d}$ to $V_{o}$ using a sinusoidal current with magnitude $I_{m}$. Thus the calculation of $t_{o n}$ assumes an ideal resonance current. Equation (5) shows the function for $t_{o n}$.

$$
\begin{equation*}
t_{o n}=\arccos \left(1-\frac{2 \omega C_{d} V_{o}}{I_{m}}\right) \tag{5}
\end{equation*}
$$

With (1) through (5), we obtain a complete piece-wise mathematical representation of the converter with the described parastics.

## III. Harmonic Approximation

The mathematical model developed in section II can be expressed as multiple models, all connected through switching surfaces [12]. This allows for a precise discontinuous description of the system which is suited for simulation. However, the model is impractical for further analysis and control design where a single Linear Time Invariant (LTI) model is preferred. Thus the model needs to be linearized. The resonance converter exhibits a limit cycle in its steady-state operation, making the conventional averaging linearization methods inapplicable, and other more generalized methods are needed. One such method, and the method used in prior art, is the harmonic balance method. This method approximates each state with a Fourier series, where the magnitude for each term becomes the new state of the system. The approximation will result in a loss of information as the Fourier series will at some point be truncated. Equation (6) shows the approximation of the states by the Fourier series to the arbitrary order $N$. Equation (7) shows the same but for the state derivatives.

$$
\begin{align*}
& I_{r} \approx I_{r_{D C}}+\sum_{n=1}^{N} I_{r_{s n}} \sin (n \omega t)+I_{r_{c n}} \cos (n \omega t)  \tag{6a}\\
& V_{r} \approx V_{r_{D C}}+\sum_{n=1}^{N} V_{r_{s n}} \sin (n \omega t)+V_{r_{c n}} \cos (n \omega t)  \tag{6b}\\
& V_{o} \approx V_{o_{D C}}+\sum_{n=1}^{N} V_{o_{s n}} \sin (n \omega t)+V_{o_{c n}} \cos (n \omega t)  \tag{6c}\\
& \dot{I}_{r} \approx \dot{I}_{r_{D C}}+\sum_{n=1}^{N}\left(\dot{I}_{r_{s n}}-\omega n I_{r_{c n}}\right) \sin (n \omega t)+ \\
& \left(\dot{I}_{r_{c n}}+\omega n I_{r_{s n}}\right) \cos (n \omega t)  \tag{7a}\\
& \dot{V}_{r} \approx \dot{V}_{r_{D C}}+\sum_{n=1}^{N}\left(\dot{V}_{r_{s n}}-\omega n V_{r_{c n}}\right) \sin (n \omega t)+ \\
& \left(\dot{V}_{r_{c n}}+\omega n V_{r_{s n}}\right) \cos (n \omega t)  \tag{7b}\\
& \dot{V}_{o} \approx \dot{V}_{o_{D C}}+\sum_{n=1}^{N}\left(\dot{V}_{o_{s n}}-\omega n V_{o_{c n}}\right) \sin (n \omega t)+ \\
& \left(\dot{V}_{o_{c n}}+\omega n V_{o_{s n}}\right) \cos (n \omega t) \tag{7c}
\end{align*}
$$

With the approximation of the states, the state vector goes from being of order 3 to order $3+6 N$, where $N$ is the order of the Fourier series. Equation (8) shows the new state vector. Here $I_{r_{c n}}, I_{r_{s n}}$, etc. are vectors of length $N$ containing the states for each harmonic.

$$
x=\left[\begin{array}{c}
I_{r}  \tag{8}\\
V_{r} \\
V_{f}
\end{array}\right] \mapsto\left[\begin{array}{c}
I_{r_{D C}} \\
V_{r_{D C}} \\
V_{o_{D C}} \\
I_{r_{c n}} \\
V_{r_{c n}} \\
V_{o_{c n}} \\
I_{r_{s n}} \\
V_{r_{s n}} \\
V_{o_{s n}}
\end{array}\right]
$$

Besides the states, the piece-wise functions (2)-(4) each needs to be approximated by a single continuous function. Since the piece-wise functions are periodic, a Fourier series can likewise be used. The Fourier series are calculated through conventional methods, and then rewritten to simplify the computation. The Appendix presents the used rewritten Fourier series. Fig. 3 shows the normalized magnitudes of the Fourier coefficients for each of the constructed series.


Fig. 3: Normalized magnitudes of the harmonic content for each Fourier series.

Fig. 3 shows that $V_{h b}$ and $V_{s w}$ are described purely by the odd harmonics in the Fourier series. This results in all the even terms, except zero, in the states $I_{r_{c n}}, I_{r_{s n}}, V_{r_{c n}}$, and $V_{r_{s n}}$ evaluate to zero and the states can be discarded as they provide no information. This reduces the size of the system to $3+4 N$ for an even $N$. Furthermore, from Fig. 1 it can also be concluded that $I_{r_{D C}}$ will always be zero in steady state due to the resonance tank capacitor $C_{r}$ blocking DC current flow. However, $I_{r_{D C}}$ is non-zero during transients. Thus it still provides some information.

## A. Harmonic Balancing

With the Fourier approximation of both the states and the piece-wise functions completed, the approximations are inserted in (1). This creates a set of partial differential equations (PDEs). However, by collecting the trigonometric terms, the partial differential equation can be separated into a set of first order ordinary differential equations (ODEs), where the trigonometric term can be canceled out. Equation (9) shows the resulting three equations for (1c) when the described method is applied. Here a 1st order Fourier series is used, and $I_{h b_{D C}}, I_{h b_{s}}$, and $I_{h b_{c}}$ are the calculated Fourier coefficients.

$$
\begin{align*}
\dot{V}_{o_{D C}} & =\frac{I_{h b_{D C}}}{C_{f}}-\frac{V_{o_{D C}}}{C_{f} R_{f}}  \tag{9a}\\
\dot{V}_{o_{s}} & =\frac{I_{h b_{s}}}{C_{f}}-\frac{V_{o_{s}}}{C_{f} R_{f}}+\omega V_{o_{c}}  \tag{9b}\\
\dot{V}_{o_{c}} & =\frac{I_{h b_{c}}}{C_{f}}-\frac{V_{o_{c}}}{C_{f} R_{f}}-\omega V_{o_{s}} \tag{9c}
\end{align*}
$$

The Fourier coefficients will be nonlinear expressions dependent on one or more of the states, making the system of firstorder ODEs nonlinear. Due to the Fourier series, the resulting system is a continuous approximation of the discontinuous system in (1) where the discontinuities have been eliminated at the expense of an increased number of states. The nonlinear approximation obtained from the Fourier series (17)-(19) is not accurate in transient simulations due to simplifications. However, other realizations of the Fourier series will result in accurate transient simulations but at the expense of increased computation time. Nonetheless, the operating point for all the states of the resonant converter can be determined by inserting the desired duty cycle and frequency into the system, and solve for the steady-state using a numerical solver.

## IV. Linear State Space Model

With the nonlinear approximation model constructed and a suitable operation point found, linearization of the model is done to obtain a state space model of the form

$$
\begin{align*}
\dot{x} & =A x+B u  \tag{10a}\\
y & =C x \tag{10b}
\end{align*}
$$

where $A$ is the system matrix, $B$ is the input matrix, and $C$ is the output matrix. The state vector $x$ will contain the Fourier expanded variables as presented in (8). Since the even harmonics of the resonant voltage and current turned out to be redundant, the differential equations describing these can be removed prior to linearization without any loss of information. The input vector $u$ consist of the switching frequency, $f_{s w}$, the duty cycle, $D$, and the supply voltage, $V_{s}$, where the latter is used to include potential disturbances from the supply. Lastly, the output vector $y$ consists of the DC output voltage, $V_{o_{D C}}$. The obtained state space model will only be valid up to the Nyquist frequency due to the selected modeling approach. Nonetheless, this still results in an accurate model for controller design and general analysis. For cases where dynamic content above the Nyquist frequency is needed, the modeling approach presented in [23] can be used. This modeling method provides an extended range of the model but at the expense of beings computationally more expensive.

## A. Model Reduction

The created state space model contain both a large portion of zero elements and some large values in the system matrix. This leads to a high condition number of the model, indicating that the model has poor numerical properties and may produce numerical errors in further computations. Furthermore, because
of the large size of the state space model, the model is not practical for control design. Also, conversion to transfer functions are discouraged due to the reduction of the numerical precision inherent in the conversion process. Thus to address these problems, the state space model needs to be adjusted and reduced in order to maintain reliability for later computations. The reduction is also necessary from a control perspective where a smaller number of states needs to be considered, making observer designs and complex control strategies simpler and faster to implement and execute.

One procedure to prepare the system for a model reduction that also tend to improve the condition number of the state space model is to balance the system. A balanced system is a system where the states are selected in such a way that each state is as controllable as it is observable. Then the relative impact of each state is given by the Hankel Singular Values (HSV). The HSV is defined as $\lambda^{\frac{1}{2}}(P Q)$, where $P$ and $Q$ are the controllability and observability Gramians respectively. For linear systems $P$ and $Q$ can be determined using the two Lyapunov equations in (11) [24, 25].

$$
\begin{align*}
& A P+P A^{T}+B B^{T}=0  \tag{11a}\\
& A^{T} Q+Q A+C^{T} C=0 \tag{11b}
\end{align*}
$$

If $P$ and $Q$ are both diagonal matrices containing the HSVs sorted from highest to lowest, the states in $A$ are balanced and, likewise, sorted. Hence the first states are those with the largest impact on the system dynamics down to the last state which has the least impact. Moreover, all the elements in the matrices will be non-zero, and the numerical values will be closer, thereby improving the condition number.

With the system balanced, model reduction can be achieved easily. Since the states are already sorted by their dynamical impact, the state space system can be partitioned into the parts to keep, denoted ( $A_{11}, B_{1}, C_{1}$ ), and the parts to discard, as shown in (12). The exact number of states to keep can usually be determined by inspecting the HSVs and observing if any state has a large decrease in it HSV. Lastly, the reduced model is derived using a residualization based reduction (13). The residualization technique sets $\dot{x}_{2}=0$, thereby assuming steady state, and solves for $x_{2}$ in terms of $x_{1}$ and $u$. The result is backsubstituted into the equation for $x_{1}$ resulting in the matrices in (13). This method ensures that the information regarding the DC-gain in the discarded states is preserved in the reduced model thus improving the overall precision at low frequencies which is critical for power converters.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{x}_{1} \\
\dot{x}_{2}
\end{array}\right]=\left[\begin{array}{ll}
A_{11} & A_{12} \\
A_{21} & A_{22}
\end{array}\right]\left[\begin{array}{l}
x_{1} \\
x_{2}
\end{array}\right]+\left[\begin{array}{l}
B_{1} \\
B_{2}
\end{array}\right] u}  \tag{12a}\\
& {\left[\begin{array}{l}
y_{1} \\
y_{2}
\end{array}\right]=\left[\begin{array}{ll}
C_{1} & C_{2}
\end{array}\right]\left[\begin{array}{l}
x_{1} \\
x_{2}
\end{array}\right]} \tag{12b}
\end{align*}
$$

$$
\begin{align*}
& A_{r}=A_{11}-A_{12} A_{22}^{-1} A_{21}  \tag{13a}\\
& B_{r}=B_{1}-A_{12} A_{22}^{-1} B_{2}  \tag{13b}\\
& C_{r}=C_{1}-C_{2} A_{22}^{-1} A_{21} \tag{13c}
\end{align*}
$$

## V. Experimental Validation

To verify the presented theory, we construct a class-DE SRC with the specifications and bill of material presented in Table I. These values are also used in the model such that a comparison with the implemented converter can be made.

TABLE I: Test conditions of the converter and the corresponding bill of materials.

|  | Value | Unit | Acquired |
| :---: | :---: | :--- | :---: |
| Test Conditions |  |  |  |
| $V_{s}$ | 348 | V | Measured |
| $V_{o}$ | 210 | V | Measured |
| $D$ | 47.9 | $\%$ | Known |
| $f_{s w}$ | 1.01 | MHz | Known |
| $f_{r}$ | 865 | kHz | Calculated |
|  |  |  |  |
| Bill of Materials |  |  |  |
| $L_{r}$ | 150 | $\mu \mathrm{H}$ | Measured |
| $C_{r}$ | 240 | pF | Estimated |
| $C_{o s s}$ | 53 | pF | Datasheet [26] |
| $C_{d}$ | 20 | pF | Datasheet [27] |
| $R_{e s r}$ | 1.5 | $\Omega$ | Measured |
| $R_{L}$ | 1000 | $\Omega$ | Known |
| $C_{L}$ | 30 | nF | Measured |

For the resonance tank capacitor, $C_{r}$, a 220 pF capacitor with a $10 \%$ tolerance is used. However, the value is increased slightly to account for parasitic capacitance in the resonance tank. For $C_{o s s}$ and $C_{d}$, the capacitance is found from the datasheets by calculating the average capacitance for the voltage range each device experiences.

## A. Deriving the Model

Using the specifications in Table I and the theory presented in section III, an approximative nonlinear dynamical model using a 5th order Fourier series is constructed. A Fourier series of order 5 is found to be a good compromise between sufficient convergence of the Fourier series and needed computation time. For orders lower than 5, the precision of the model decreases rapidly, while for higher orders, the numerical issues become worse without adding much to the precision. To illustrate the increase in precision with the order of the Fourier series, the operation point is calculated for every second order going from order 1 through 9. Table II shows the computed DC output voltage, $V_{O_{D C}}$ for each operation point with the stepwise change in the result, $\Delta V$. The stepwise change illustrates the convergence of the model for the given order of the Fourier series, by considering the difference in the output voltage between the models.

TABLE II: Computed output voltage for different order Fourier series. $\Delta V$ shows the change in the output voltage in volt and percent between the associated order model and the model to the left.

| Order | 1 | 3 | 5 | 7 | 9 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{O_{D C}}$ | 220.57 V | 212.55 V | 212.44 V | 212.42 V | 211.92 V |
| $\Delta V$ |  | -8.02 V | -0.11 V | -0.02 V | -0.5 V |
|  |  | $-3.6 \%$ | $-0.052 \%$ | $-0.009 \%$ | $-0.234 \%$ |

The computed operation point is inserted into the state space model to obtain the linear model. The resulting model is a 25 states model with a condition number of $1.5 \cdot 10^{6}$. By balancing the model, the condition number is reduced to 855 thus providing a numerical improvement of roughly 3 decimals. Finally, the model reduction is performed using the method described in Section IV-A. The HSVs are extracted to determine each states impact on the dynamics of the converter. Fig. 4 shows the value of the HSV related to each state in the balanced high-order state space model.


Fig. 4: The Hankel Singular Values corresponding to each state of the balanced high-order state space model of the resonant converter.

A large drop in the HSV is observed when going from 1 state to 2 states and when going from 3 states to 4 states. Above 4 states, the HSVs are so small that the dynamical impact is negligible. This suggest that a 3rd order model is sufficient to describe the behavior of the converter. Equation (14) shows the reduced 3rd order state space model of the system.

$$
\begin{align*}
& A_{r}=\left[\begin{array}{ccc}
-4.12 & -1.08 & -10.2 \\
-1.21 & -1.78 & 104 \\
10.2 & -103 & -69.3
\end{array}\right] 10^{4}  \tag{14a}\\
& B_{r}=\left[\begin{array}{cc}
0.214 & -160 \\
0.171 & -26.0 \\
-0.239 & 157
\end{array}\right]  \tag{14b}\\
& C_{r}=\left[\begin{array}{ccc}
-160 & -23.7 & -157
\end{array}\right] \tag{14c}
\end{align*}
$$

To ensure that the reduction removes only non-essential state information, the frequency and time information between the high-order model and the reduced model is compared. Fig. 5 shows the frequency response for the reduced and
high-order model, and Fig. 6 shows the step responses.
Looking at Fig. 5 we find that the DC and low frequency content is preserved in the reduced model thanks to the residualization method used. From 800 kHz and above, the high-order model contains information regarding the switching behavior which is not preserved in the reduced model. Since the converter operates with a switching frequency of 1 MHz , the reduced model is more than adequate to describe the low frequency dynamics of the converter. This is also clearly illustrated in the step responses in Fig. 6 where the reduced model precisely matches the high-order model. The reduction of the model further reduces the condition number down to 33.

## B. Measurements

Fig. 7 shows the implemented class-DE converter prototype that has been tested in the laboratory. The switching frequency of the prototype is controlled by a voltage controlled oscillator (VCO). To get a good comparison between the models, the prototype, and existing models, multiple measurements are conducted. First, the steady state output voltage is obtained


Fig. 5: Calculated frequency response of the high-order and the reduced state space models for the switching frequency, $f_{s w}$, and the supply voltage, $V_{s}$, to the output, $V_{o}$.


Fig. 6: Calculated step response of the high-order and the reduced state space models. The switching frequency, $f_{s w}$, is stepped 1 kHz and the supply voltage, $V_{s}$, is stepped 1 V . All signals are offset to zero.


Fig. 7: The implemented Class-DE SR Converter.
for the prototype, the proposed model, and prior art [20, 21]. Second, measurements of the frequency response from the switching frequency to the output voltage is taken for the prototype and calculated for the models. The frequency response is measured using a frequency response analyser which superimposes a small sinosoidal signal on the input of the VCO through an injection transformer. The input voltage of the VCO and the output voltage of the prototype are measured from where the frequency response is calculated.Lastly, step responses from both the supply voltage and the switching frequency to the output voltage are conducted. For the step responses, all the steps are offset to 0 V at $t=0$ to better compare the transient behavior and the gain. The prior art with which the proposed model is compared to is built on the work reported in [20,21] where a 5th order state space model is constructed from a 1st order Fourier series with no parasitic capacitors included.

Table III shows the measured DC output voltage of the prototype converter, and the calculated DC output voltage for the two models with the difference from the voltage measured on the prototype, $\Delta V$. Inspecting the table, it is found that the proposed model is closer to the measured results than what has been accomplished with the prior art. The proposed model has its steady state output voltage within $1.1 \%$ of the measured output voltage, while the prior art is within $8.5 \%$.

Fig. 8 shows the measured and calculated frequency responses from the switching frequency to the output voltage of the converter. Observing the figure, we find a strong correlation between the proposed model and the implemented prototype up to 600 kHz from which the magnitude of the measurement increases due to the resonance and switching frequency. Thus the measurements diverge from the model that is no longer valid due to the exceeding of the Nyquist frequency. The measured frequency response has a DC-gain of -60.6 dB , followed by a first order low pass filter response at 5.9 kHz , followed again by the beat frequency which causes a

TABLE III: DC output voltage of the resonant converter in steady state for the prototype (measured) and the two models (calculated).

|  | Prototype | Proposed | Prior Art |
| :---: | :---: | :---: | :---: |
| $V_{o D C}$ | 210 V | 212.4 V | 192.2 V |
| $\Delta V$ |  | $2.4 \mathrm{~V}(1.1 \%)$ | $-17.8 \mathrm{~V}(-8.5 \%)$ |



Fig. 8: Frequency response for $V_{o} / f_{s w}$ measured and calculated for the reduced model.


Fig. 9: Step response for $V_{o} / f_{s w}$ measured and calculated for the reduced model. All signals are offset to zero, and the step goes from 1.01 MHz to 1.03 MHz .
second order low pass filter response at about 162 kHz . The DC-gain of the proposed model is off by 0.9 dB , and the model matches the damping and cutoff frequencies of the two low pass filter responses. The small observed differences between the proposed model and the measurements are caused by minor discrepancies in the expected and actual component values leading to a slight difference in the response. On the other hand, the prior art is off by 8.3 dB , and has the cutoff frequency of the first low pass filter at 15.8 kHz . However, the location of the beat frequency matches the measurement but the response is too damped.

Fig. 9 shows the response of the output voltage for the prototype converter and the two models when stepping the switching frequency, $f_{s w}$, up 20 kHz . The increase in frequency moves the switching frequency further away from the resonance frequency $f_{r}$, causing a voltage reduction on the output. The output voltage of the prototype falls by 18 V and settles to within $2 \%$ of the final voltage after about $100 \mu \mathrm{~s}$ with no overshoot. The proposed model has a smaller step of -16.9 V and a faster settling time of about $91 \mu \mathrm{~s}$. Meanwhile the prior art steps to -7.2 V with a settling time of $41 \mu \mathrm{~s}$. Hence the gains of the models for the steps correspond to the gain differences found in the frequency response in Fig. 8.


Fig. 10: Response for a 20 V step in the supply voltage measured and calculated for the reduced model. All signals are offset to zero, and the step steps from 348 V to 328 V .

Lastly, Fig. 10 shows a 20 V step in the power supply for the prototype and the two models. The step was conducted by shorting out a 20 V supply hence creating a sudden drop in the supply voltage. However, the lab induced voltage drop contains damped oscillations that influence the step behavior. To obtain the best possible comparison between the models and the prototype, the actual voltage drop was logged and used as the step for the models. Observing Fig. 10 we see that the 20 V step causes the output of the converter to fall with 11.3 V in a well damped fashion. Both of the models also fall to approximately the same value with the prior art falling to -10.8 V and the proposed model -11.8 V . However, the transient of the proposed model follows the measured response more precisely than the prior art which falls faster and has a slight undershoot.

To finalize this section, Table IV summarizes the results from the conducted measurements. From the table it is found that the proposed model is closer to the prototype converter for all the measurement. Especially the signal path from $f_{s w}$ to the output receives a significant improvement with the proposed model. The DC-gain error is improved with 7.4 dB and the error in the low frequency pole, $f_{l p}$ is reduced to less than $16.9 \%$ from $168 \%$ when comparing the prior art to the proposed reduced model.


Fig. 11: Block diagram of the closed loop configuration of the class-DE converter.

TABLE IV: Summary of the measurement results.

| Model | Prototype | Proposed | Prior Art |
| ---: | :---: | :---: | :---: |
| Steady State |  |  |  |
| $V_{o_{D}}$ | 210 V | 212.4 V | 192.2 V |
| $\Delta V$ |  | $2.4 \mathrm{~V}(1.1 \%)$ | $-17.8 \mathrm{~V}(-8.5 \%)$ |
|  |  |  |  |
| Frequency Response |  | -68.9 dB |  |
| DC-Gain | -60.6 dB | -61.5 dB | 15.8 kHz |
| $f_{l p}$ | 5.9 kHz | 6.9 kHz | 169 kHz |
| $f_{\text {beat }}$ | 162 kHz | 166 kHz |  |
| Step Response $\left(f_{s w}\right)$ |  |  | $41 \mu \mathrm{~s}$ |
| Settling time | $100 \mu \mathrm{~s}$ | $91 \mu \mathrm{~s}$ | -7.2 V |
| Final value | -18 V | -16.9 V | $10.8 \mathrm{~V}(60 \%)$ |
| $\Delta V$ |  | $1.1 \mathrm{~V}(6.1 \%)$ |  |
|  |  |  | -10.8 V |
| Step Response $\left(V_{s}\right)$ | -11.3 V | -11.8 V | $0.5 \mathrm{~V}(4.4 \%)$ |
| Final value | $-0.5 \mathrm{~V}(-4.4 \%)$ |  |  |
| $\Delta V$ |  |  |  |

## VI. Control Example

This section presents the design of a PI-controller for the SRC Class-DE converter based on the proposed model and prior art. The closed-loop responses of the two controllers are compared to assess the improvement by the proposed model.

## A. Design

The objective of the controllers is to regulate the output voltage of the converter by adjusting the switching frequency. Fig. 11 shows the closed loop configuration of the converter where $A$ is an attenuation factor of $1 / 70$. To obtain comparable controllers for the two models, numerical optimization is utilized. The numerical optimization is set to minimize the Integral Absolute Error (IAE) of the output, and the Integral Square Error (ISE) of the control signal by changing the integral and proportional gain of the PI-controller. Equation (15) shows the cost function.

$$
\begin{equation*}
J=\int\left|V_{r e f}-V_{o}(t)\right|+R\left(u_{r e f}-u(t)\right)^{2} \mathrm{~d} t \tag{15}
\end{equation*}
$$

In (15), $V_{o}(t)$ is the change in the voltage output of the converter due to a step in the frequency, and $V_{r e f}$ is the reference output voltage. In this case, the DC-gain of the model. Likewise, $u(t)$ is the control signal from the PI-controller and $u_{r e f}$ is the final value after the step. Lastly, $R$ is a tuning parameter used to control how aggressive the response should be. $R$ is selected to be 0.01 which results in a fast response with a limited overshoot in $u(t)(<10 \%)$ for both models. Running the optimization results in the controller parameters found in Table V, where $J^{*}$ is the final cost.

TABLE V: Controller parameters

| Model | $K_{p}$ | $K_{i}$ | $J^{*}$ |
| ---: | :---: | :---: | :---: |
| Proposed | 1.24 | 61290 | 0.8443 |
| Prior Art | 2.66 | 274392 | 0.2384 |

From Table V, we find that the controller designed on the prior art model is more aggressive and has a lower final cost compared to the controller designed on the proposed model.


Fig. 12: Closed-Loop step response of the implemented converter with the controller designed with the proposed model and the prior art. (a) shows the movement in the output voltage, and (b) the control signal from the PI-controller.

This suggest that the prior art controller should provide a faster response with less overshoot in the control signal. However, based on the findings in Section V-B this will not be the case when tested on the prototype.

## B. Closed-Loop Step Response

To verify the performance of the two designed controllers, the controllers are connected to the prototype resonant converter. A step of 1 V on the reference, equating to 50 V on the output, is applied. Fig. 12 shows the resulting steps for the two controllers. Fig. 12a shows the output voltage and Fig. 12b shows the control signal from the PI-controller.

The responses in Fig. 12 clearly shows that the overshoot for the controller based on the prior art is significantly larger than the expected ( $<10 \%$ ), indicating that the model is not representative for the actual converter. The controller based on the prior art has a faster rise time on the output than the controller based on the proposed model. However, the faster rise time results in an overshoot, and the settling time for both controllers ends up being about $90 \mu \mathrm{~s}$. The response of the system with the controller based on the proposed model behaves similar to what is expected from the control design, indicating that the proposed model is a good representation
of the actual converter. The initial overshoot observed in the control signal in Fig. 12b at $t=0$ is caused by a large ground loop creating high-frequency oscillations.

Finally, Fig. 13 shows the measured and expected overshoots in the output voltage and the control signal for both of the controllers. From the figure, more than 40 times difference in the overshoot in the control signal of the prior art is evident, while almost no change is observed between the expected overshoot and the measured overshoot for the system based on the proposed model.


Fig. 13: Comparison of expected and measured overshoot for both models. The expected value for $y(t)$ prior art is zero and the overshoot for both the expected and measured $y(t)$ for the proposed model is less than $1 \%$.

## VII. Conclusion

This paper presents an improved model for class-DE series resonant converters operating at high frequencies. It is identified that the parasitic capacitances of the switching devices in the converter have a significant impact on the converter behavior and output voltage, and should be included in models once high frequency operation is considered. Using the generalized averaging modeling technique, a model incorporating parasitics is derived. The model is a high order model since multiple harmonics need to be considered to capture the influence of the parasitic components adequately. To mitigate the difficulties of working with high order models, a reduction method that retains all the relevant dynamics is presented. The reduced model is compared against a prototype class-DE SRC as well as prior art, and it is found that the reduced model is able to model the prototype accurately. The gain error is improved with more than 7 dB , and the error in the low frequency pole is reduced to less than $16.9 \%$ from $168 \%$ when comparing the proposed reduced model with the prior art. A PI-controller is designed for the prior art and the proposed model, and tested on the prototype. It is found that the desired control behavior and the measured behavior matched for the proposed model while the prior art resulted in more than 40 times larger overshoot in the measurements compared to what was expected from the prior art model, showing the discrepancy that exists between the prior art model and the measurement.

## APPENDIX

The Appendix presents the equations used to calculate the coefficients for the Fourier series used in this work. To shorten the equations, the following substitution is applied:

$$
\begin{equation*}
C_{b}(t)=\int I_{r}(t) \mathrm{d} t \tag{16}
\end{equation*}
$$

A. Fourier series for the voltage node $V_{h b}$

$$
\begin{align*}
a_{V_{h b}}= & \frac{1}{\pi C_{d} \omega}\left(\int_{-\phi}^{t_{o n}-\phi} C_{b}(t) \sin (n t) \mathrm{d} t\right.  \tag{17a}\\
& \left.-C_{b}(-\phi) \int_{-\phi}^{t_{o n}-\phi} \sin (n t) \mathrm{d} t\right) \\
& +\frac{1}{\pi} \int_{t_{o n}-\phi}^{t_{o n}+\pi-\phi} V_{o}(t) \sin (n t) \mathrm{d} t \\
b_{V_{h b}}= & \frac{1}{\pi C_{d} \omega}\left(\int_{-\phi}^{t_{o n}-\phi} C_{b}(t) \cos (n t) \mathrm{d} t\right.  \tag{17b}\\
& \left.-C_{b}(-\phi) \int_{-\phi}^{t_{o n}-\phi} \cos (n t) \mathrm{d} t\right) \\
& +\frac{1}{\pi} \int_{t_{o n}-\phi}^{t_{o n}+\pi-\phi} V_{o}(t) \cos (n t) \mathrm{d} t \\
b_{0}= & \frac{V_{o D C}}{2} \tag{17c}
\end{align*}
$$

Valid for: $n=1,3, \ldots N$.
B. Fourier series for the current $I_{h b}$

$$
\begin{align*}
a_{I_{h b}} & =\frac{1}{\pi} \int_{t_{o n}-\phi}^{\pi-\phi} I_{r}(t) \sin (n t) \mathrm{d} t  \tag{18a}\\
b_{I_{h b}} & =\frac{1}{\pi} \int_{t_{o n}-\phi}^{\pi-\phi} I_{r}(t) \cos (n t) \mathrm{d} t  \tag{18b}\\
b_{0} & =\frac{1}{2 \pi} \int_{t_{o n}-\phi}^{\pi-\phi} I_{r}(t) \mathrm{d} t \tag{18c}
\end{align*}
$$

C. Fourier series for the voltage node $V_{s w}$

$$
\begin{align*}
a_{V_{s w}}= & \frac{1}{\pi}\left(\frac{-1}{C_{o s s} \omega} \int_{0}^{\pi(1-2 D)} C_{b}(t) \sin (n t) \mathrm{d} t\right.  \tag{19a}\\
& +\left(\frac{C_{b}(0)}{C_{o s s} \omega}-V_{s}\right) \int_{0}^{\pi(1-2 D)} \sin (n t) \mathrm{d} t \\
& \left.+V_{s} \int_{\pi(1-2 D)}^{\pi} \sin (n t) \mathrm{d} t\right) \\
b_{V_{s w}}= & \frac{1}{\pi}\left(\frac{-1}{C_{o s s} \omega} \int_{0}^{\pi(1-2 D)} C_{b}(t) \cos (n t) \mathrm{d} t\right.  \tag{19b}\\
& +\left(\frac{C_{b}(0)}{C_{o s s} \omega}-V_{s}\right) \int_{0}^{\pi(1-2 D)} \cos (n t) \mathrm{d} t \\
& \left.+V_{s} \int_{\pi(1-2 D)}^{\pi} \cos (n t) \mathrm{d} t\right) \tag{19c}
\end{align*}
$$

Valid for: $n=1,3, \ldots N$.

## REFERENCES

[1] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1-14, Feb 2009.
[2] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. Andersen, "Evolution of very high frequency power supplies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, 2014.
[3] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," in Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE, pp. 1-11, IEEE, 2006.
[4] N. Bertoni, G. Frattini, R. G. Massolini, F. Pareschi, R. Rovatti, and G. Setti, "An Analytical Approach for the Design of Class-E Resonant DC-DC Converters," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7701-7713, 2016.
[5] X. Gao, H. Wu, and Y. Xing, "A Multioutput LLC Resonant Converter With Semi-Active Rectifiers," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1819-1827, 2017.
[6] M. Noah, S. Endo, H. Ishibashi, K. Nanamori, J. Imaoka, K. Umetani, and M. Yamamoto, "A Current Sharing Method Utilizing Single Balancing Transformer for a Multiphase LLC Resonant Converter With Integrated Magnetics," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 977-992, 2018.
[7] H. Ma, Y. Li, Q. Chen, L. Zhang, and J. Xu, "A Single-Stage Integrated Boost-LLC AC-DC Converter

Valid for: $n=1,2, \ldots N$.

With Quasi-Constant Bus Voltage for Multichannel LED Street-Lighting Applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1143-1153, 2018.
[8] M. K. Kazimierczuk and D. Czarkowski, Resonant power converters. John Wiley \& Sons, 2012.
[9] C. Nwosu and M. Eng, "State-space averaged modeling of a nonideal boost converter," The pacific journal of science and Technology, vol. 2, no. 9, pp. 1-7, 2008.
[10] S. R. Sanders and G. C. Verghese, "Synthesis of averaged circuit models for switched power converters," IEEE Transactions on Circuits and systems, vol. 38, no. 8, pp. 905-915, 1991.
[11] K. Mandal, S. Banerjee, C. Chakraborty, and M. Chakraborty, "Bifurcations in frequency controlled load resonant DC-DC converters," in 2012 IEEE International Symposium on Circuits and Systems, pp. 1135-1138, IEEE, 2012.
[12] O. Dranga, B. Buti, and I. Nagy, "Stability analysis of a feedback-controlled resonant DC-DC converter," IEEE Transactions on Industrial Electronics, vol. 50, no. 1, pp. 141-152, 2003.
[13] P. C. Luk, S. Aldhaher, W. Fei, and J. F. Whidborne, "State-Space Modeling of a Class $E^{2}$ Converter for Inductive Links," IEEE Transactions on Power Electronics, vol. 30, pp. 3242-3251, June 2015.
[14] J. Kwon, X. Wang, F. Blaabjerg, C. L. Bak, A. R. Wood, and N. R. Watson, "Linearized modeling methods of AC-DC converters for an accurate frequency response," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1526-1541, 2017.
[15] R. Z. Scapini, L. V. Bellinaso, and L. Michels, "Stability analysis of half-bridge rectifier employing LTP approach," in IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society, pp. 780-785, IEEE, 2012.
[16] G. N. Love and A. R. Wood, "Harmonic state space model of power electronics," in 2008 13th International Conference on Harmonics and Quality of Power, pp. 1-6, IEEE, 2008.
[17] V. Salis, A. Costabeber, S. M. Cox, and P. Zanchetta, "Stability assessment of power-converter-based ac systems by LTP theory: eigenvalue analysis and harmonic impedance estimation," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1513-1525, 2017.
[18] V. Salis, A. Costabeber, S. M. Cox, A. Formentini, and P. Zanchetta, "Stability Assessment of High-Bandwidth DC Voltage Controllers in Single-Phase Active Front Ends: LTI Versus LTP Models," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 4, pp. 2147-2158, 2018.
[19] S. Sanders and J. Noworolski, "Generalized averaging method for power conversion circuits," IEEE Transactions on Power Electronics, vol. 6, no. 2, 1991.
[20] M. F. Menke, Á. R. Seidel, and R. V. Tambara, "LLC LED Driver Small-Signal Modeling and Digital Control Design for Active Ripple Compensation," IEEE Transactions on Industrial Electronics, vol. 66, no. 1, pp. 387-396, 2019.
[21] P. Wang, C. Liu, and L. Guo, "Modeling and simulation of full-bridge series resonant converter based on generalized state space averaging," in Applied Mechanics and Materials, vol. 347, pp. 1828-1832, Trans Tech Publ, 2013.
[22] C. Buccella, C. Cecati, H. Latafat, P. Pepe, and K. Razi, "Observer-Based Control of LLC DC/DC Resonant Converter Using Extended Describing Functions," IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5881-5891, 2015.
[23] J. Groves, "Small-signal analysis using harmonic balance methods," in Power Electronics Specialists Conference, 1991. PESC'91 Record., 22nd Annual IEEE, pp. 74-79, IEEE, 1991.
[24] S. Skogestad and I. Postlethwaite, Multivariable feedback control: analysis and design, vol. 2. Wiley New York, 2007.
[25] P. Benner, "Numerical linear algebra for model reduction in control and simulation," GAMM-Mitteilungen, vol. 29, no. 2, pp. 275-296, 2006.
[26] GaNSystems, "GaN transistor GS66502B," 2017.
[27] GeneSiC, "Silicon Carbide Power Schottky Diode GB01SLT06-214," 2014.


Nicolai J. Dahl Nicolai J. Dahl (S'19) is a Ph.D. student at the electronics group at the Technical University of Denmark, Kongens Lyngby, Denmark. He received both his B.Sc. degree and M.Sc. degree from the Technical University of Denmark in June 2016 and August 2018 respectively. His research interest include control theory, system modeling, signal processing, and optimization, which he has applied in the fields of switch-mode power amplifiers, resonant converters, and his current research topic, time-based control.


Ahmed M. Ammar Ahmed M. Ammar (S'11) received his B.Sc. and M.Sc. degrees in electrical engineering from Mansoura University and Nile University, Egypt, in 2011 and 2014, respectively. His experience includes positions at different industries including Intel Corporation, Imec, and Mentor Graphics (now Mentor, a Siemens Business). He is currently working as a graduate research and teaching assistant at the Department of Electrical Engineering in the Technical University of Denmark towards his Ph.D. Degree. His current research interests include power electronics, integrated power converters, and power management and delivery circuits and systems.


Arnold Knott Arnold Knott (M'10) received the DiplomIngenieur (FH) degree from the University of Applied Sciences in Deggendorf, Germany, in 2004. From 2004 until 2009 he has been working with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications. In 2010 he earned the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark working on a research project under the title "Improvement of out-of band Behavior in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology". From 2010 to 2013 he was Assistant Professor and since 2013 Associate Professor at the Technical University of Denmark. His interests include switchmode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility and communication systems.


Michael A. E. Andersen Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark, where since 2009, he has been the Deputy Head of the Department of Electrical Engineering. He is the author or coauthor of more than 300 publications. His research interests include switchmode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.

## Appendix [J2]

F. M. Spliid, A. M. Ammar, and A. Knott, "Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, December 2019.

# Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications 

Frederik M. Spliid, Student Member, IEEE, Ahmed M. Ammar, Student Member, IEEE, and Arnold Knott


#### Abstract

Resonant converter topologies have the ability to eliminate switching losses through zero-voltage switching, making them well-suited for switching operation in the MHz frequency range. However, these types of converters are traditionally very sensitive to changes in input voltage and power level, making them unsuitable as power factor correcting AC-DC converters. This paper present a throughout analysis of the operation of a class DE converter in order to derive a set of conditions, under which it can achieve constant input impedance over a wide input voltage range ( $60-325 \mathrm{~V}$ DC) with constant output voltage ( 450 V DC) and thus be operated as a PFC converter, while maintaining zero voltage switching across the full range. The operation is experimentally verified under DC-DC operation for different power levels at a series of input voltages within the specified range. The implemented prototype achieves conversion efficiencies of up to $94 \%$ and handles up to 105 W of power at switching frequencies of 2 MHz and above, while achieving constant input impedance over the full input voltage range, enabling its use as a power factor correcting converter.


Index Terms-AC-DC power conversion, power factor correction, resonant converters, zero voltage switching, wide-bandgap semiconductors

## I. Introduction

The recent years have seen many advances in the field of power converters operating at switching frequencies in the high frequency (HF, $3-30 \mathrm{MHz}$ ), or very high frequency (VHF, 30-300 Mhz) ranges [1]-[4]. By the use of resonant converter topologies [5], the converter switching losses are mostly eliminated, allowing converters to be operated at much higher frequencies than previously feasible, greatly reducing the size and cost of passive energy storage components [6], [7]. Popular resonant converter topologies include the Class E [8], [9], Class DE [10], [11] and Class $\Phi_{2}$ converters [12]. Through the use of self-oscillating passive gate drivers [13], the need for active gate drivers is eliminated, enabling power converters operating in the range of 30 MHz [14], [15] or even 100 MHz [16]. With the emergence of wide bandgap technologies such as Gallium Nitride (GaN) transistors, this development is further enabled by the improved figures of merit of new switching devices [17], [18], and previous publications have demonstrated active-driven GaN-based switch-

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark (e-mail: frmsp@elektro.dtu.dk; ammma@elektro.dtu.dk; akn@elektro.dtu.dk).
mode converters operating at switching frequencies of 10 MHz [19] and even 100 MHz [20].
While resonant converter topologies have enabled increased switching frequencies compared to traditional hard-switched topologies, their control is complicated. Through their ability to operate with zero-voltage switching (ZVS), they can achieve high efficiency under the right operating conditions, but they are very sensitive to changes in loading conditions [21], [22]. As the diode-based rectifiers used in resonant converter topologies are inherently non-linear in their input impedance, this means that these topologies are very sensitive to changes in voltage and power levels, giving them a low dynamic range and making them a less obvious choice for AC/DC applications as power factor correctional (PFC) converters. Methods compensating for these non-linearities in order to achieve zero-voltage switching over a wider voltage range has previously been described for the class E converter [23]-[26] and LLC converters [27].
Other work describing soft-switching PFC converters with resonant and non-resonant converter topologies include [28][34]. In order to function as a PFC converter, a converter must draw an input current proportional to its instantaneous input voltage - meaning that the input impedance of the converter must emulate a constant resistor, $R_{i n}$, over a desired voltage range and that the input power must be defined by (1) in this range.

$$
\begin{equation*}
P_{i n}=\frac{V_{i n}^{2}}{R_{i n}} \tag{1}
\end{equation*}
$$

This paper presents a throughout analysis of the operation of a class DE converter, in order to derive a set of conditions required for the converter to achieve constant input impedance


Fig. 1: The presented converter as part of 2-stage AC/DC power supply


Fig. 2: Input power vs. input voltage for three different impedance levels.
and zero voltage switching over a desired voltage range. This enables the class DE converter to be used as a PFC converter in a system as the one shown in fig. 1. Through careful control of frequency and duty cycle, it is shown that is it possible to use the topology as a PFC converter without the need for any additional components. Open-loop DC-DC operation is demonstrated for a series of operating points with varying input voltage and power levels. The specifications of the lab prototype is shown in table I and the relation between input voltage and power for three different values of input resistance is shown in fig. 2.

| Quantity | Symbol | Value |
| :---: | :---: | :---: |
| Input voltage | $V_{i n}$ | $60 \mathrm{~V}-325 \mathrm{~V}$ |
| Output voltage | $V_{o}$ | $450 V_{D C}$ |
| Input resistance | $R_{i n}$ | $1000-10,000 \Omega$ |

TABLE I: Prototype specifications.

## II. TOPOLOGY ANALYSIS

The converter is designed as a class DE resonant converter consisting of a class DE inverter [10], [11] and a class DE rectifier [10], [35] connected through a series resonant tank as shown in fig. 3. Compared to other resonant converter topologies, the class DE converter has the benefits of lower voltage stresses on the semiconductor devices, and that it incorporates only a single magnetic component. As magnetic components are often bulky, this allows for a more compact design. The primary disadvantage of the topology is the floating high-side switch on the inverter side, which complicates the driving of the switches.


Fig. 3: Block diagram of resonant converter


Fig. 4: Class DE inverter schematic
By performing a throughout mathematical analysis of the ideal converter operation, the conditions that must be met for the converter to function in the desired voltage and power range are determined. By first analyzing the operation of inverter and rectifier separately, the conditions can be determined by assuming conservation of power.
Both circuits have been analyzed in detail in previous literature [11], [36]. However, as the intended converter application in this work is power factor correction, the following analysis will be more focused on quantities related to this application, with most operational parameters being referred to the input voltage and resistance, rather than output power. Furthermore, this analysis sacrifices the traditional requirement of zero- $\frac{d v}{d t}$ switching in the inverter in exchange for the option to achieve constant input resistance over a wide input range.

## A. Inverter analysis

The mathematical analysis starts with the inverter circuit, in order to determine its required load impedance, which is later needed for impedance matching of the rectifier.
The class DE inverter (fig. 4) consists of a transistor halfbridge with shunt capacitors across the transistors. During analysis the two switches are assumed to be driven with an equal duty cycle, $D_{i}$, and 180 degrees of phase shift between them while the inverter output current is a pure sine wave at the switching frequency. Traditionally the inverter is designed for the resonant current to be in phase with the driving signal for the high-side switch in order to achieve zero- $\frac{d v}{d t}$ switching. However, this design introduces a phase lag, $\varphi$, in order to give an additional degree of freedom. Throughout analysis, the parameter $C_{s}$ is introduced as an expression for the total capacitance on the switch node, i.e. the sum of capacitors $C_{Q 1}$ and $C_{Q 2}$, where $I_{m}$ is the resonant current amplitude and $\omega_{s w}$ is the switching frequency in radians per second.
The inverter has four states of operation as described in table II: one conducting state for each switch (states 1 and 3 ) and two charge/discharge states for the shunt capacitors (states 2 and 4 ), in order to achieve zero voltage switching.

| State | Conducting <br> switch | $i_{Q 1}$ | $i_{C 2}-i_{C 1}$ |
| :---: | :---: | :---: | :---: |
| 1 | Q 1 | $I_{m} \cdot \sin \left(\omega_{s w} t-\varphi\right)$ | 0 |
| 2 | - | 0 | $-I_{m} \cdot \sin \left(\omega_{s w} t-\varphi\right)$ |
| 3 | Q 2 | 0 | 0 |
| 4 | - | 0 | $-I_{m} \cdot \sin \left(\omega_{s w} t-\varphi\right)$ |

TABLE II: Operating states of class DE inverter.

The DC input current of the inverter, $I_{i n}$, is found by calculating the average current drawn from the input voltage source, $V_{i n}$, over a full switching cycle. In steady state operation, the average current through capacitors $C_{i n}$ and $C_{Q 1}$ will be zero, and the DC input current will be equal to the average value of the current in the high side switch, $Q 1$. An expression for the DC input current, $I_{i n}$, is found by calculating the average value of $i_{Q 1}$ over a full switching cycle. As this switch is only conducting in state 1 , the switch current only needs to be integrated over this state.

$$
\begin{gather*}
I_{i n}=\frac{1}{T_{s w}} \int_{0}^{T_{s w}} i_{Q 1} d t  \tag{2}\\
=\frac{I_{m}}{T_{s w}} \int_{0}^{D_{i} \cdot T_{s w}} \sin \left(\omega_{s w} t-\varphi\right) d t \Leftrightarrow \\
I_{i n}=\frac{I_{m}}{2 \pi} \cdot\left(\cos (\varphi)-\cos \left(2 \pi D_{i}-\varphi\right)\right) \tag{3}
\end{gather*}
$$

The voltage at the switch node, $V_{s}$, is equal to either the input voltage or zero when switches $Q 1$ and $Q 2$ are turned on in states 1 and 3, respectively. During the dead-time in states 2 and 4 , the resonant current charges and discharges the voltage across capacitors $C_{1}$ and $C_{2}$.
$V_{s}(t)=\left\{\begin{array}{cc}V_{i n} & \text { in state } 1 \\ V_{i n}-\frac{I_{m}}{C_{s}} \int_{D_{i} T_{s w}}^{t} \sin \left(\omega_{s w} t-\varphi\right) d t & \text { in state 2 } \\ 0 & \text { in state 3 } \\ -\frac{I_{m}}{C_{s}} \int_{\frac{T_{s w}}{2}+D_{i} T_{s w}}^{t} \sin \left(\omega_{s w} t-\varphi\right) d t & \text { in state 4 }\end{array}\right.$
An expression for the input voltage is found by determining the state 4 value of $V_{s}$ at time $t=T_{s w}$. Assuming ZVS, the value at this time should be equal to $V_{i n}$ :

$$
\begin{equation*}
V_{i n}=V_{s}\left(T_{s w}\right)=\frac{I_{m}}{\omega_{s w} C_{s}} \cdot\left(\cos (\varphi)+\cos \left(2 \pi D_{i}-\varphi\right)\right) \tag{5}
\end{equation*}
$$

Combining (4) and (5) gives a simpler expression for the switch node voltage.

$$
V_{s}(t)=\left\{\begin{array}{cl}
V_{i n} & \text { in state } 1  \tag{6}\\
V_{i n} \cdot \frac{\cos \left(\omega_{s w} t-\varphi\right)+\cos (\varphi)}{\cos \left(2 \pi D_{i}-\varphi\right)+\cos (\varphi)} & \text { in state } 2 \\
0 & \text { in state } 3 \\
V_{i n} \cdot \frac{\cos \left(\omega_{s w} t-\varphi\right)+\cos \left(2 \pi D_{i}-\varphi\right)}{\cos \left(2 \pi D_{i}-\varphi\right)+\cos (\varphi)} & \text { in state 4 }
\end{array}\right.
$$

Fig. 5 shows normalised waveforms for $V_{s}, i_{r}$ (resonant current) and $i_{Q 1}$. Combining and rewriting (3) and (5) gives expressions that can be used to find $\varphi$ and $D_{i}$ for a given set of parameters:

$$
\begin{gather*}
\cos (\varphi)=\frac{\pi f_{s w} C_{s} V_{i n}+\pi I_{i n}}{I_{m}}  \tag{7}\\
\cos \left(2 \pi D_{i}-\varphi\right)=\frac{\pi f_{s w} C s V_{i n}-\pi I_{i n}}{I_{m}} \tag{8}
\end{gather*}
$$

Lastly, the required impedance at the inverter output is determined, in order to achieve the desired resonant current amplitude and phase. This is done through a first harmonic analysis of the switch-node voltage $V_{s}(t)$, which is considered in two parts - an active part in phase with the resonant current, labelled $V_{s, R}$, and a reactive part leading the resonant


Fig. 5: Class DE inverter waveforms, for $D_{i}=40 \%$ and $\varphi=\frac{\pi}{5}$
current by 90 degrees, labelled $V_{s, X}$. The active and reactive components of the switch-node voltage (6) are determined from Fourier analysis:

$$
\begin{align*}
V_{s, R} & =\frac{2}{T_{s w}} \cdot \int_{0}^{T_{s w}} V_{s}(t) \cdot \sin \left(\omega_{s w} \cdot t-\varphi\right) d t  \tag{9}\\
& =\frac{V_{i n}}{\pi} \cdot\left(\cos (\varphi)-\cos \left(2 \pi D_{i}-\varphi\right)\right)
\end{align*}
$$

$$
\begin{equation*}
V_{s, X}=\frac{2}{T_{s w}} \cdot \int_{0}^{T_{s w}} V_{s}(t) \cdot \cos \left(\omega_{s w} \cdot t-\varphi\right) d t \Leftrightarrow \tag{10}
\end{equation*}
$$

$$
\begin{equation*}
V_{s, X}=\frac{V_{i n}}{2 \pi} \cdot\left(\frac{K_{1}+K_{2}+\pi-2 \pi D_{i}}{\cos (\varphi)+\cos \left(2 \pi D_{i}-\varphi\right)}\right) \tag{11}
\end{equation*}
$$

where the expressions $K_{1}$ and $K_{2}$ are functions of $\varphi$ and $D_{i}$ :

$$
\begin{gather*}
K_{1}=\sin (\varphi) \cdot \cos (\varphi)  \tag{12}\\
K_{2}=\sin \left(2 \pi D_{i}-\varphi\right) \cdot \cos \left(2 \pi D_{i}-\varphi\right) \tag{13}
\end{gather*}
$$

The required active and reactive load impedances, $R_{i n v}$ and $X_{i n v}$ respectively, are calculated by dividing the voltage components by the resonant current amplitude $I_{m}$. Through (3), the impedances can be expressed in terms of input voltage and current, as well as $\varphi$ and $D_{i}$.

$$
\begin{align*}
& R_{i n v}=\frac{V_{s, R}}{I_{m}}=\frac{V_{i n}}{2 \pi^{2} I_{i n}} \cdot\left(\cos (\varphi)-\cos \left(2 \pi D_{i}-\varphi\right)\right)^{2}  \tag{14}\\
& X_{i n v}=\frac{V_{s, X}}{I_{m}}=\frac{V_{i n}}{4 \cdot \pi^{2} \cdot I_{i n}} \cdot\left(K_{1}+K_{2}+\pi-2 \pi D_{i}\right) \cdot K_{3} \tag{15}
\end{align*}
$$

where the expressions $K_{3}$ is a function of $\varphi$ and $D_{i}$ :

$$
\begin{equation*}
K_{3}=\frac{\cos (\varphi)-\cos \left(2 \pi D_{i}-\varphi\right)}{\cos (\varphi)+\cos \left(2 \pi D_{i}-\varphi\right)} \tag{16}
\end{equation*}
$$



Fig. 6: Class DE rectifier schematic

## B. Rectifier analysis

A similar analysis is applied to the class DE rectifier. The class DE rectifier (fig. 6) consists of a diode half bridge with shunt capacitors connected across the diodes. The shunt capacitors include any parasitic capacitance of the diodes, as well as any externally added capacitance. By assuming a constant output voltage and a purely sinusoidal input current, the rectifier can be analysed with equal diode conduction duty cycles, denoted $D_{r}$. The sinusoidal input current source represents an ideal resonant inverter, and is replaced by a class DE inverter in the full converter.

Previous work [36] has analyzed the topology in detail with its output power described as functions of input current amplitude and diode duty cycle, but in this case it is more desirable to calculate the required current amplitude as a function of power and switching frequency, as the primary quantity of interest for PFC applications is the input current, or input impedance, of the full converter.
The input current $i_{r}$ is a perfect sine wave with amplitude $I_{m}, i_{r}=I_{m} \cdot \sin \left(\omega_{s w} t\right)$, and the rectifier operation can be divided into 4 different states, as shown in table III. Each diode conducts for a duty cycle $D_{r}$, while the shunt capacitors charge and discharge in the remaining time. As the net average current through the shunt capacitors over a switching cycle is zero, any charge carried to the output is flowing through the diode $D 2$.

Fig. 7 shows waveforms for input current and voltage, as well as the current through the high-side diode, $D 2$.
The amplitude of the resonant current, $I_{m}$ can be expressed as a function of output voltage, output current, switching frequency and the sum of the two shunt capacitors, denoted $C_{r}$, by looking at the charge transfer for the positive half cycle of the resonant current, states A and B.
In state A, before the diode $D 2$ starts conducting, the resonant current transfers the amount of charge needed to raise the

| State | Conducting diode | $i_{D 2}$ | $i_{C 1}+i_{C 2}$ |
| :---: | :---: | :---: | :---: |
| A | - | 0 | $i_{r}$ |
| B | D2 | $i_{r}$ | 0 |
| C | - | 0 | $i_{r}$ |
| D | D1 | 0 | 0 |

TABLE III: Operating states of class DE rectifier.


Fig. 7: Class DE rectifier waveforms, for $D_{r}=30 \%$
voltage $v_{r}$ to the level of the output voltage $V_{o}$. The shunt capacitors store this charge during diode conduction in state B.

$$
\begin{equation*}
\int_{0}^{T_{s w} \cdot\left(\frac{1}{2}-D_{r}\right)} I_{m} \cdot \sin \left(\omega_{s w} t\right) d t=C_{r} \cdot V_{o} \tag{17}
\end{equation*}
$$

In state B , the diode $D 2$ is conducting and the resonant current transfers an amount of charge to the rectifier output. This charge is equal to the average output current multiplied by the switching period, $T_{s w}$.

$$
\begin{equation*}
\int_{T_{s w} \cdot\left(\frac{1}{2}-D_{r}\right)}^{T_{s w} \cdot \frac{1}{2}} I_{m} \cdot \sin \left(\omega_{s w} t\right) d t=I_{o} \cdot T_{s w}=\frac{2 \cdot \pi \cdot I_{o}}{\omega_{s w}} \tag{18}
\end{equation*}
$$

Combining (17) and (18), an expression for the required resonant current amplitude as a function of $V_{o}, I_{o}, C_{r}$ and the switching frequency is obtained:

$$
\begin{gather*}
\int_{0}^{\frac{T_{s w}}{2}} I_{m} \cdot \sin \left(\omega_{s w} t\right) d t=\frac{2 \cdot I_{m}}{\omega_{s w}} \Leftrightarrow  \tag{19}\\
\frac{2 \cdot I_{m}}{\omega_{s w}}=C_{r} \cdot V_{o}+\frac{2 \cdot \pi \cdot I_{o}}{\omega_{s w}} \Leftrightarrow  \tag{20}\\
I_{m}=\pi \cdot f_{s w} \cdot C_{r} \cdot V_{o}+\pi \cdot I_{o} \tag{21}
\end{gather*}
$$

At the switching frequency, the input impedance of the rectifier resembles an RC-series circuit, with resistance $R_{\text {rect }}$ and capacitance $C_{\text {rect }}$ depending on the output power.
The equivalent input resistance of the rectifier for a given output current can be determined from (21) by assuming $100 \%$ efficiency.

$$
\begin{equation*}
R_{\text {rect }} \cdot \frac{I_{m}^{2}}{2}=I_{o} \cdot V_{o} \Leftrightarrow \tag{22}
\end{equation*}
$$

$$
\begin{equation*}
R_{r e c t}=\frac{2 \cdot I_{o} \cdot V_{o}}{I_{m}^{2}}=\frac{2 \cdot I_{o} \cdot V_{o}}{\left(\pi \cdot f_{s w} \cdot C_{r} \cdot V_{o}+\pi \cdot I_{o}\right)^{2}} \tag{23}
\end{equation*}
$$

The equivalent input capacitance can be determined using fourier analysis, and a general expression dependent on the diode duty cycle was derived in [36].

$$
\begin{equation*}
C_{r e c t}=\frac{\pi \cdot C_{r}}{\pi \cdot\left(1-2 D_{r}\right)+K_{r}} \tag{24}
\end{equation*}
$$

Where $K_{r}$ is a function of diode duty cycle:

$$
\begin{equation*}
K_{r}=\sin \left(2 \pi D_{r}\right) \cdot \cos \left(2 \pi D_{r}\right) \tag{25}
\end{equation*}
$$

The duty cycle is described as a function of the other parameters by re-evaluating (17) and combining with (21):

$$
\begin{gather*}
\int_{0}^{T_{s w} \cdot\left(\frac{1}{2}-D_{r}\right)} \sin \left(\omega_{s w} t\right) d t=\frac{C_{r} \cdot V_{o}}{I_{m}}=\frac{1+\cos \left(2 \pi D_{r}\right)}{\omega_{s w}} \Leftrightarrow  \tag{26}\\
D_{r}=\frac{1}{2 \pi} \cdot \cos ^{-1}\left(\frac{f_{s w} \cdot C_{r} \cdot V_{o}-I_{o}}{f_{s w} \cdot C_{r} \cdot V_{o}+I_{o}}\right) \tag{27}
\end{gather*}
$$

Equations (23), (24) and (27) express the equivalent input resistance and capacitance of the class DE rectifier for any combination of $V_{o}, I_{o}, C_{r}$ and $f_{s w}$.

## C. Full converter

The class DE rectifier is connected to the output of the class DE inverter through a series resonant tank, sized to meet the reactance requirement of the inverter.
With the two circuits connected, the current sources in fig. 4 and 6 are replaced by the other half-circuit and the resonant tank, with the inverter output current being equal to the rectifier input current.
By inserting (21) into (7), an expression for the phase angle, $\varphi$, can be written:

$$
\begin{equation*}
\cos (\varphi)=\frac{\pi f_{s w} C_{s} V_{i n}+\pi I_{i n}}{\pi f_{s w} C_{r} V_{o}+\pi I_{o}} \tag{28}
\end{equation*}
$$

For the topology to function as a PFC converter, it must achieve a constant input impedance $R_{i n}$ over the full input voltage range, in order to ensure a proportional relationship between the input voltage and current. The input current can be expressed in terms of input voltage and resistance:

$$
\begin{equation*}
I_{i n}=\frac{V_{i n}}{R_{i n}} \tag{29}
\end{equation*}
$$

Since the resonant topology has negligible switching losses, considering ZVS operation, the losses in the converter are assumed to be dominated by the losses in the resonant tank. With an efficiency $\eta_{\text {res }}$ in the resonant circuit, the output current can be expressed as:

$$
\begin{equation*}
I_{o}=\eta_{\text {res }} \cdot \frac{V_{\text {in }} I_{\text {in }}}{V_{o}}=\eta_{\text {res }} \cdot \frac{V_{\text {in }}^{2}}{V_{o} \cdot R_{i n}} \tag{30}
\end{equation*}
$$

Where $\eta_{\text {res }}$ is determined by the ratio of the rectifier input resistance and the equivalent series resistance (ESR) of the resonant tank:

$$
\begin{equation*}
\eta_{\text {res }}=\frac{R_{\text {rect }}}{R_{\text {rect }}+E S R} \tag{31}
\end{equation*}
$$

The ESR of the resonant tank includes ESR of the resonant capacitor as well as winding and core losses in the resonant inductor.
Equation (28) can now be rewritten.

$$
\begin{equation*}
\cos (\varphi)=\frac{f_{s w} C_{s} R_{i n} V_{i n} V_{o}+V_{i n} V_{o}}{f_{s w} C_{r} R_{i n} V_{o}^{2}+\eta_{\text {res }} \cdot V_{i n}^{2}} \tag{32}
\end{equation*}
$$

In order for $\varphi$ to be a real number, it is required that $\cos (\varphi) \leq$ 1. By rearranging (32), a constraint for the converter operation can be written:

$$
\begin{equation*}
f_{s w} \cdot R_{i n} \geq \frac{V_{i n} V_{o}-\eta_{\text {res }} \cdot V_{i n}^{2}}{V_{o} \cdot\left(C_{r} V_{o}-C_{s} V_{i n}\right)} \tag{33}
\end{equation*}
$$

For a given set of voltages and capacitances this gives a minimum achievable input resistance for a specific switching frequency. An increase in $\eta_{\text {res }}$ will reduce the minimum input resistance.
Equations (21), (29) and (30) are inserted into (8) in order to determine the inverter duty cycle:

$$
\begin{equation*}
\cos \left(2 \pi D_{i}-\varphi\right)=\frac{f_{s w} C_{s} R_{i n} V_{i n} V_{o}-V_{i n} V_{o}}{f_{s w} C_{r} R_{i n} V_{o}^{2}+\eta_{\text {res }} \cdot V_{i n}^{2}} \tag{34}
\end{equation*}
$$

Combining (32) and (34) makes it possible to reduce (16).

$$
\begin{equation*}
K 3=\frac{1}{f_{s w} C_{s} R_{i n}} \tag{35}
\end{equation*}
$$

Inserting (35) and (29) into (15) gives a simpler expression for the required load reactance seen from the inverter side.

$$
\begin{equation*}
X_{i n v}=\frac{1}{4 \cdot \pi^{2} \cdot f_{s w} C_{s}} \cdot\left(K_{1}+K_{2}+\pi-2 \pi D_{i}\right) \tag{36}
\end{equation*}
$$

Expressions for the current phase angle, $\varphi$, and inverter duty cycle, $D_{i}$, are derived from (32) and (34).

$$
\begin{gather*}
\varphi=\cos ^{-1}\left(\frac{f_{s w} C_{s} R_{i n} V_{i n} V_{o}+V_{i n} V_{o}}{f_{s w} C_{r} R_{i n} V_{o}^{2}+\eta_{\text {res }} \cdot V_{i n}^{2}}\right)  \tag{37}\\
D_{i}=\left(\cos ^{-1}\left(\frac{f_{s w} C_{s} R_{i n} V_{i n} V_{o}-V_{i n} V_{o}}{f_{s w} C_{r} R_{i n} V_{o}^{2}+\eta_{r e s} \cdot V_{i n}^{2}}\right)+\varphi\right) \cdot \frac{1}{2 \pi} \tag{38}
\end{gather*}
$$

The expression for the rectifier diode duty cycle (27) can be rewritten using (30)

$$
\begin{equation*}
D_{r}=\frac{1}{2 \pi} \cdot \cos ^{-1}\left(\frac{f_{s w} \cdot C_{r} \cdot R_{i n} \cdot V_{o}^{2}-\eta_{r e s} \cdot V_{i n}^{2}}{f_{s w} \cdot C_{r} \cdot R_{i n} \cdot V_{o}^{2}+\eta_{r e s} \cdot V_{i n}^{2}}\right) \tag{39}
\end{equation*}
$$

The reactance of the resonant tank needs to cancel out the reactance of the rectifier input capacitance found in (24) and provide the required load reactance for the inverter as found in (36). For any set of input- and output voltages, input resistance, node capacitances, switching frequency and resonant tank efficiency, a required reactance can be calculated.

$$
\begin{gather*}
X_{\text {tank }}=X_{i n v}+\frac{1}{\omega_{s w} \cdot C_{r e c t}} \Leftrightarrow  \tag{40}\\
X_{\text {tank }}=\frac{K_{1}+K_{2}+\pi \cdot\left(1-2 D_{i}\right)}{4 \pi^{2} f_{s w} C_{s}}+\frac{K_{r}+\pi \cdot\left(1-2 D_{r}\right)}{2 \pi^{2} f_{s w} C_{r}} \tag{41}
\end{gather*}
$$

The inverter and rectifier circuits of the class DE converter are connected through a series resonant tank consisting of an inductor, $L_{\text {tank }}$, and a capacitor $C_{\text {tank }}$. In order to achieve zero-voltage switching and constant input resistance, the switching frequency and duty cycle of the class DE inverter must be controlled in order to achieve a match between the required reactance determined by (41) and the reactance of the resonant tank:

$$
\begin{equation*}
\omega_{s w} \cdot L_{t a n k}-\frac{1}{\omega_{s w} \cdot C_{t a n k}}=X_{t a n k} \tag{42}
\end{equation*}
$$

## III. CALCULATION OF OPERATING POINT

Due to the highly nonlinear nature of (42), generic, symbolic solutions are difficult to calculate. Instead, numerical solutions are found for a specific application, based on the specifications in table I. A Class DE converter is designed to meet the specs and a series of operating points are calculated.

## A. Semiconductors

The first step is to select suitable switches and diodes for the two half-bridges in the converter. For the switches in the inverter half bridge, the devices must have a voltage rating higher than the peak input voltage, 325 V , and a current ranting higher than the peak input current of converter. The peak input current is found at the maximum input voltage and lowest input resistance, $I_{\text {in,max }}=\frac{325 \mathrm{~V}}{1000 \Omega}=325 \mathrm{~mA}$. Furthermore, it is desirable to select devices with low parasitic shunt capacitance, in order to allow for fast switching of the inverter bridge.
For these reasons, the selected switches are the GS66502B GaN transistors from GaN Systems [37]. With voltage and current ratings of 650 V and 7.5 A respectively, these devices satisfy the requirements, with a parasitic shunt capacitance, $C_{\text {oss }}$, in the range of tens of pF . In order to estimate the timerelated effective shunt capacitance of the devices, a simulation is performed in LTSpice, using the testbench shown in fig. 8. A current source is connected to the device under test in parallel with an ideal diode connected to a voltage source with the desired test voltage. Once the voltage across the switch is charged to the level of the bias voltage, the diode will start conducting the full input current. The time when this occurs is denoted $t_{\text {charge }}$. By knowing the charging time, the bias voltage and the test current, the effective capacitance is calculated using (43).

$$
\begin{equation*}
C_{Q}=\frac{t_{\text {charge }} \cdot I_{\text {test }}}{V_{\text {test }}} \tag{43}
\end{equation*}
$$

For the selected switch, the effective capacitance for charging from $0-325 \mathrm{~V}$ is found to be 54 pF . For lower voltage levels this value will be higher due to nonlinearities in the device capacitance, and this is taken into account for lower input voltages.
A graph of the time-related effective value of $C_{s}$ vs. input voltage, using two GS66502B GaNFETs is shown in fig. 9. It is seen that the effective value of $C_{s}$ is varying by a factor of two over the range of operation.
For the rectifier bridge, the chosen diodes are GB01SLT06 from GeneSiC Semiconductor [38]. These devices are rated for 650 V and 2.5 A , making them suitable for the design.


Fig. 8: LTSpice test bench for determination of switch shuntcapacitance


Fig. 9: Simulated values of $C_{s}$ vs. input voltage using two GS66502B GaNFETs

Through simulations similar to the ones performed on the switches, the effective shunt capacitance of the diodes is found to be around 21 pF when charging from $0-450 \mathrm{~V}$. As the output voltage is considered constant for all operating points, this capacitance value is assumed to be constant as well.

The simulated values for parasitic capacitances are used to calculate theoretical solutions for the switching frequency and duty cycle at different operating points. As the parasitics of the physical components may deviate from those in the simulation models, the switching frequency and duty cycle might need slight adjustments from the calculated values in order to ensure zero-voltage switching and constant input resistance of the converter. Parameter mismatches between the switching devices in the circuit are of no consequence to the converter operation, as the important parameter is the total capacitance on the switch node, $C_{s}$, and not its distribution between the devices.

## B. Shunt capacitors

Rearranging (33) gives a minimum value of the rectifier shunt capacitance, $C_{r}$, based on the choice of inverter switches. This minimum value depends on the switching frequency, input voltage and efficiency of the converter, and the choice of capacitance affects the solution space of (42). As a starting point, the minimum capacitance is calculated at the peak input power (peak input voltage and minimum input resistance) and a switching frequency of 2 MHz , as this has previously been found to be the optimum frequency in terms of magnetic components sizes [39]. For this calculation the resonant tank efficiency, $\eta_{\text {res }}$, is assumed to be $95 \%$ under the specified conditions. If the efficiency turns out to be lower than this, the switching frequency might have to be increased slightly to compensate.

$$
\begin{equation*}
C_{r} \geq \frac{V_{i n} V_{o}-\eta_{\text {res }} \cdot V_{i n}^{2}}{f_{s w} R_{i n} V_{o}^{2}}+C_{s} \frac{V_{i n}}{V_{o}} \Leftrightarrow \tag{44}
\end{equation*}
$$

$$
\begin{gather*}
C_{r} \geq \frac{325 \mathrm{~V} \cdot 450 \mathrm{~V}-0.95 \cdot(325 \mathrm{~V})^{2}}{2 M H z \cdot 1 k \Omega \cdot(450 \mathrm{~V})^{2}}+108 \mathrm{pF} \cdot \frac{325 \mathrm{~V}}{450 \mathrm{~V}} \\
=191 \mathrm{pF} \tag{45}
\end{gather*}
$$

Since the combined parasitic capacitance of the two diodes is only 42 pF , it is evident that external capacitance is required for the converter to function under these conditions. For this reason, a external shunt capacitor, $C_{r, e x t}$, of 150 pF is added, bringing the total size of $C_{r}$ to 192 pF .
Decoupling capacitors are placed at the inverter input and rectifier output in order to filter out the residuals at the switching frequency.

## C. Resonant tank

Knowing the capacitances $C_{s}$ and $C_{r}$, the requried resonant tank reactance, $X_{\text {tank }}$, can be plotted as a function of the input voltage and switching frequency, as shown in fig. 10.
The resonant tank needs to be able to meet the reactance requirement at any input voltage by only adjusting the switching frequency. In order to choose a size for the resonant inductor, the input resistance of the rectifier is calculated at peak power an 2 MHz . This is done using (23) and (30):

$$
\begin{equation*}
R_{r e c t}=\frac{2 \eta_{\text {res }} V_{i n}^{2} V_{o}^{2} R_{\text {in }}}{\left(\pi f_{s w} C_{r} R_{i n} V_{o}^{2}+\pi \eta_{r e s} V_{i n}^{2}\right)^{2}}=130 \Omega \tag{46}
\end{equation*}
$$

According to [5], the resonant current can be assumed to have a sinusoidal shape when the loaded quality factor of the resonant tank relative to the rectifier input resistance is larger than 2.5 . In this converter, the inductor is chosen to be approximately 50 percent larger than this, in order to have higher harmonic suppression in the resonant tank and make the comparison between the theory and measurements easier.
$L_{\text {tank }}=1.5 \cdot 2.5 \cdot \frac{R_{\text {rect }}}{\omega_{\text {sw }}}=2.5 \cdot 1.5 \cdot \frac{130 \Omega}{2 \pi \cdot 2 \mathrm{MHz}}=39 \mu \mathrm{H}$
Based on this inductor, the resonant tank capacitor is sized to meet the reactance requirement for all input voltages. In Fig. 11 the calculated reactance requirement from (41) is plotted for a series of different input voltages over a wide frequency range. It is seen that the $40 \mu H$ inductor in series with a 340 pF capacitor is able to meet the reactance requirement for all input levels.


Fig. 10: Required resonant tank reactance vs. $V_{i n}$ and $f_{s w}$


Fig. 11: Calculated values for required resonant tank reactance vs. reactance of the selected resonant tank.

Once again assuming a switching frequency of 2 MHz and a resonant tank efficiency of $95 \%$, the inductor current amplitude at the peak input voltage is calculated by combining (21) and (30).

$$
\begin{gathered}
I_{m, \max }=\pi \cdot 2 \mathrm{MHz} \cdot 192 \mathrm{pF} \cdot 450 \mathrm{~V}+\frac{0.95 \cdot \pi \cdot(325 \mathrm{~V})^{2}}{1 \mathrm{k} \Omega \cdot 450 V_{(48)}} \\
=1.24 \mathrm{~A}
\end{gathered}
$$

Based on the same parameters, the peak AC voltage across the resonant capacitor is calculated:

$$
\begin{align*}
& V_{C_{\text {tank }, \text { max }}}=I_{m, \text { max }} \cdot \frac{1}{\omega_{s w} \cdot C_{t a n k}}  \tag{49}\\
& =\frac{1.24 \mathrm{~A}}{2 \cdot \pi \cdot 2 M H z \cdot 340 \mathrm{pF}}=290 \mathrm{~V}
\end{align*}
$$

In addition to this, the capacitor needs to store a DC voltage of up to $V_{o}$, resulting in a maximum voltage of around 740 V . A $40 \mu H$ inductor with an equivalent large-signal AC series resistance of $6 \Omega$ at 2 MHz is wound using a $40 \times 50 \mu \mathrm{~m}$ copper litz-wire and an EFD 15/8/5 core made of Ferroxcube 3F46 material. Based on this ESR, and the rectifier input resistance calculated in (46), the expected $\eta_{\text {res }}$ at peak power is calculated from (31).

$$
\begin{equation*}
\eta_{\text {res }}=\frac{130 \Omega}{130 \Omega+6 \Omega}=95.6 \% \tag{50}
\end{equation*}
$$

This value is seen to be close to the assumed value of $95 \%$. Fig. 12 shows the circuit diagram for power stage of the implemented converter, and table IV shows a list of the selected components.


Fig. 12: Converter power stage


Fig. 13: Calculated switching frequency and duty cycle vs. input voltage

For the chosen resonant tank, the required switching frequencies and duty cycles within the input voltage range are calculated for a number of different input resistances. The calculated operating points are shown in fig. 13. It should be noted that these operating points assume a resonant tank efficiency, $\eta_{\text {res }}$, of $95 \%$, which might not be the case under all conditions. Due to this, and any non-linearities in the resonant tank, the operating points of a physical converter will need fine-tuning in order to achieve the desired input impedance.

| Component | Model/Size |
| :---: | :---: |
| Q1, Q2 | GaN Systems GS66502B |
| $\mathrm{D} 1, \mathrm{D} 2$ | GeneSiC GB01SLT06 |
| $C_{\text {in }}$ | 50 nF |
| $C_{\text {tank }}$ | 340 pF |
| $C_{o}$ | 25 nF |
| $C_{r, \text { ext }}$ | 150 pF |
| $L_{\text {tank }}$ | $40 \mu H$ |

TABLE IV: Selected components for the prototype.

## IV. EXPERIMENTAL VERIFICATION

A converter prototype is built (fig. 14) and tested in the laboratory. Converter operation is verified at a number of different input voltages for input resistances of 1,5 and $10 \mathrm{k} \Omega$. Across the measurements, the converter output is connected to


Fig. 14: Converter prototype with marked subcircuits. Gate driver (red), input filter (white), inverter (black), rectifier (green) and resonant tank ${ }^{1}$ (cyan).
a constant voltage load of 450 V representing a large DC bus capacitor. Gate signals for the inverter switches are generated externally by a Rigol DG1062 signal generator and fed through a set of Si8610 digital isolators from silicon labs and a set of UCC27611 gate drivers from Texas Instruments. The current, voltage and power at the converter input and output is measured using a N4L PPA 5530 Precision Power Analyzer, and the input impedance of the converter is calculated from these values.
A schematic of the experimental setup including test points is shown in fig. 15.

Starting from the calculated values, the switching frequency is tuned in order to achieve the desired input impedance. A comparison between the calculated switching frequencies and the ones used in the measurements is shown in fig. 16.
Three sets of measured waveforms are shown in fig. 17. The measurements are performed at $V_{i n}=325 \mathrm{~V}$ for 3 different input impedances. As the impedance level increase, the resonant current is seen to drop in amplitude and increase in frequency while the duty cycle of the rectifier diodes are reduced.

[^1]

Fig. 15: Diagram of the measurement setup.


Fig. 16: Comparison of calculated (lines) and experimental (dots) switching frequencies for different input impedances.

The measured input impedances relative to the ideal values are shown in fig. 18, and is seen to be within 2 percent deviation of the target values.
From the measured values of the input impedance, an input current waveform is extrapolated for a European mains AC input voltage (fig. 19), assuming a diode rectifier bridge is placed at the converter input and that a control loop sets the


Fig. 17: Measured waveforms for $V_{s}$ (red), $V_{r}$ (green), $V_{o}$ (orange) and $i_{r}$ (blue) for $V_{i n}=325 \mathrm{~V}$. Scaling is $100 \mathrm{~V} / \mathrm{div}$ and $500 \mathrm{~mA} / \mathrm{div}$ on the y -axis and $200 \mathrm{~ns} /$ div on the x -axis.


Fig. 18: Measured values for converter input resistance relative to target values.
switching frequency to the values used in the measurements, with the converter being operational when the input voltage exceeds 60 V . Using an adaptive dead-time control technique [40], the duty cycle can be adjusted accordingly such that zero-voltage switching is ensured along the line cycle. From the waveforms in fig. 19, the input current THD and power factor of the converter can be calculated for the different impedance levels. the calculated values are shown in table V. The calculated values assume an ideal input filter, which completely filters out the switching frequency and its higher harmonics while providing no attenuation or phase shift at lower frequencies. A practical filter would introduce a small phase shift in the input current and reduce the power factor of the converter, so such a filter should be designed to ensure that the power factor requirement of the converter is met.

| $R_{\text {in,taret }}$ | THD | Power factor |
| :---: | :---: | :---: |
| $1 k \Omega$ | $5.25 \%$ | $99.9 \%$ |
| $5 k \Omega$ | $5.2 \%$ | $99.9 \%$ |
| $10 k \Omega$ | $5.22 \%$ | $99.9 \%$ |

TABLE V: Extracted THD and Power factor values.
The efficiency of the prototype at different load levels and input voltages is measured using the power analyzer connected to the converter input and output terminals (see fig. 15). The efficiency is defined as $\eta=\frac{P_{o u t}}{P_{\text {in }}}$, and the measured vales are shown in fig. 20. The converter is seen to achieve efficiencies of up to 94 percent at the peak output power.


Fig. 19: Extrapolated input waveforms for european mains input.


Fig. 20: Measured converter efficiency vs. input voltage for different input resistances.

## V. Conclusion

Through mathematical analysis, a set of conditions has been derived for a class DE resonant converter to be operated with a constant input impedance over a wide input voltage range, enabling its use in power factor correction applications. A constructed prototype is tested at various input voltages between 60 and 325 V for input resistances of 1,5 and 10 $k \Omega$, with measured input impedances within a few percent of the desired values.
With conversion efficiencies reaching as high as $94 \%$, the prototype is able to convert more than 100 W of power in DC/DC operation without the need for bulky heatsinks. If implemented as an AC/DC converter with a microcontroller generating the gate-signals, the converter can function as a PFC converter with zero voltage switching and small passive components. Based on extrapolation from measured values, the converter is expected to achieve a THD as low as $5.2 \%$ and a power factor of 0.999 before the input filter for European mains AC input.

## REFERENCES

[1] A. Knott et al., "Evolution of very high frequency power supplies," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sept. 2014.
[2] J. C. Hertel et al., "Integrated Very-High-Frequency Switch Mode Power Supplies: Design Considerations," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 526-538, 2018.
[3] J. M. Rivas et al., "New Archtectures for Radio-Frequency DC-DC Power Conversion," in IEEE Transaction on Power Electronics, vol. 21, no. 2, pp. 380-393, 2006.
[4] D. J. Perrault et al., "Opportunities and Challenges in Very High Frequency Power Conversion," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 1-14.
[5] M. K. Kazimierczuk and D. Czarkowski, Resonant Power Converters. Wiley, 2011.
[6] M. P. Madsen, "Very High Frequency Switch-Mode Power Supplies," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 2015.
[7] M. Kovacevic, "Advances in Very High Frequency Power Conversion," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 2015.

8] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," in IEEE Journal of Solid-State Circuits, Vol. 10, no. 3, pp. 168-176, 1975.
[9] M. K. Kazimierczuk, "Analysis of class E zero-voltage-switching rectifier," in IEEE Transactions on Circuits and Systems, Vol. 37, no. 6, pp. 747-755, 1990.
[10] D. C. Hamill, "Class DE inverters and rectifiers for DC-DC conversion," in Proc. IEEE Power Electronics Specialists Conference, 1996.
[11] H. Sekiya et al., "Steady-State Analysis and Design of Class-DE Inverter at Any Duty Ratio," in IEEE Transaction on Power Electronics, vol. 30, no. 7, pp. 3685-3694, 2014.
[12] J. Rivas, "Radio Frequency dc-dc Power Conversion," Doctoral thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, USA, 2006.
[13] M. P. Madsen et al., "Self-oscillating resonant gate drive for resonant inverters and rectifiers composed solely of passive components," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2014, pp. 2029-2035.
[14] M. P. Madsen et al., "Very high frequency half bridge DC/DC converter," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2014, pp. 1409-1414.
[15] M. P. Madsen et al., "Low Power Very High Frequency Switch-Mode Power Supply With 50 V Input and 5 V Output," in IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6569-6580, 2014.
[16] T. M. Andersen et al., "A VHF class E DC-DC converter with selfoscillating gate driver," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2011, pp. 885-891.
[17] J. Millán et al., "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, 2014.
[18] G. Zulauf et al., "Considerations for Active Power Device Selection in High- and Very-High-Frequency Power Converters," in Proc. Workshop on Control and Modeling for Power Electronics, 2018.
[19] W. Liang et al., "Low-Mass RF Power Inverter for CubeSat Applications Using 3-D Printed Inductors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 2, pp. 880-890, 2017.
[20] Y. Zhang et al., "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," in IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7926-7942, 2016.
[21] D. J. Kessler and M. K. Kazimierczuk, "Power losses and efficiency of class-E power amplifier at any duty ratio," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1675-1689, 2004.
[22] F. H. Raac, "Effects of circuit variations on the class E tuned power amplifier," in IEEE Journal of Solid-State Circuits, vol. 13, no. 2, pp. 239-247, 1978.
[23] Y. Han et al., "Resistance compression networks for radio-frequency power conversion," in IEEE Transactions on Power Electronics, vol. 22, no. 1, pp. 41-53, 2007.
[24] L. Roslaniec et al., "Design of Single-Switch Inverters for Variable Resistance/Load Modulation Operation," in IEEE Transactions of Power Electronics, vol. 30, no. 6, pp. 3200-3214, 2014.
[25] S. Park and J. Rivas-Davila, "Duty Cycle and Frequency Modulations in Class-E DC-DC Converters for a Wide Range of Input and Output Voltages," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10524-10538, 2018.
[26] J. A. Santiago-Gonzáles et al., "Design of resistive-input class E resonant rectifiers for variable-power operation," in Proc. Workshop on Control and Modeling for Power Electronics, 2013.
[27] R. Elferich, "ZVS modelling of the LLC converter operating as unity power factor front end," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, 2018, pp. 1-7.
[28] A. J. Hanson and D. J. Perrault,"A high frequency power factor correction converter with soft switching," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonia, TX, 2018, pp. 2027-2034.
[29] J. A. Santiago-Gonzales et. al, "Single phase universal input PFC converter operating at HF," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2018, pp. 2062-2069.
[30] A. M. Ammar et al., "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," 2019 IEEE 20th Workshop on Control and Modelling for Power Electronics (COMPEL), Toronto, 2019.
[31] H. Ma et al., "A Single-Stage Integrated Boost-LLC AC-DC Converter With Quasi-Constant Bus Voltage for Multichannel LED Street-Lighting Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1143-1153, Sept. 2018.
[32] H. Valipour et al., "Resonant Bridgeless AC/DC Rectifier with High Switching Frequency and Inherent PFC Capability," in IEEE Transactions on Power Electronics, 2019.
[33] G. Li et al., "A Single-Stage Interleaved Resonant Bridgeless Boost Rectifier with High-Frequency Isolation," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.
[34] S. Mangkalajan et al., "A Single-Stage LED Driver Based on ZCDS Class-E Current-Driven Rectifier as a PFC for Street-Lighting Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp 8710-8727, 2018.
[35] K. Fukui and H. Koizumi, "Half-wave class DE low dv/dt rectifier," in 2012 IEEE Asia Pacific Conference on Circuits and Systems, pp. 854860, 1996.
[36] K. Fukui and H. Koizumi, "Analysis of half-wave class DE low dv/dt rectifier at any duty cycle," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 234-245, 2014.
[37] GaNSystems, GS66502B datasheet, 2018, https://gansystems.com/wp-content/uploads/2018/04/GS66502B-DS-Rev-180420.pdf
[38] GeneSiC-Semiconductor, GB01SLT06 datasheet, 2014, http://www.genesicsemi.com/images/products_sic/rectifiers/GB01SLT06214.pdf.
[39] B. X. Foo et al., "Can higher frequencies reduce magnetics size? An exploration of the impact of frequency on optimized flyback transformers," in Proc. Workshop on Control and Modeling for Power Electronics, 2017.
[40] M. Ekhtiari et. al, "Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 783-793, Jan. 2017.

## Appendix [J3]

A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Analysis and Design of a Charge-PumpBased Resonant AC-DC Converter with Inherent PFC Capability," in IEEE Journal of Emerging and Selected Topics in Power Electronics, January 2020.

# Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability 

Ahmed M. Ammar, Student Member, IEEE, Frederik M. Spliid, Student Member, IEEE, Yasser Nour, Senior Member, IEEE, and Arnold Knott


#### Abstract

This paper presents the analysis and design of a resonant power factor correction (PFC) rectifier for the first stage in single-phase front-end offline converters targeting low-power applications (up to 100 W ). With the addition of a charge pump circuit comprised of a capacitor and a diode to a class-DE resonant converter, PFC functionality is achieved inherently. The operation is based on soft switching, allowing for increased switching frequencies with reduced switching losses. A 1 MHz prototype employing wide-bandgap (WBG) switching devices is built and tested to validate the analysis and proposed design method. The prototype achieves up to 50 W of output power with a power factor of 0.99 , a total harmonic distortion (THD) of $8.6 \%$, and an efficiency of up to $88 \%$; with harmonic magnitudes well-within the IEC 61000-3-2 standard class-C device limits, making it suitable for use as the rectifier stage in LED drivers. Despite the additional circuit stresses from the charge pump operation, the proposed converter offers simplicity and low component overhead, with the potential for higher frequency operation towards higher power densities.


Index Terms- AC-DC power conversion, power factor correction, resonant power conversion, charge pump, widebandgap semiconductors.

## I. Introduction

WITH the current trend towards smaller and highly portable consumer electronics and other industrial applications, research has been investigating the opportunities for minimizing the weights and sizes of products form factors, while achieving the same performance. The main hinder has been the power supplies due to their bulky passive components, where the passive components sizes are inversely proportional to the switching frequencies of the converters. One such application with a great demand for miniaturization is offline converters.
The typical solution for offline converters is a two-stage architecture, as shown in Fig. 1. The first stage is an AC-DC power factor correction (PFC) rectifier followed by an energystorage capacitor to filter the double-the-line $100 / 120 \mathrm{~Hz}$ frequency component. The second stage is a DC-DC converter

[^2]

Fig. 1. Offline converter structure. The red box outlines the focus of this work. providing the voltage and current levels that apply to the load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current to limit the mains voltage distortion [1][2].

Pulse-width-modulated (PWM) converters have been the primary candidate for the AC-DC stage in offline converters, including buck [3]-[6], boost [7][8], buck-boost [9][10], flyback [11], and SEPIC [12][13] converters. They can provide high power factor and are easy to control. However, their operation is based on hard switching. Accordingly, they typically operate at low frequencies in order to limit the switching losses. This in turn results in large sizes for the passive components needed to store and process the energy transferred to the load every switching cycle. On the other hand, high-frequency designs have less efficiency and may incorporate a heat sink for thermal management, which counteracts the gain in power density.

Accordingly, soft-switching resonant converters have been receiving much attention in the recent years [14]-[17]. Resonant converters have substantially lower switching losses than their PWM counterparts. Thanks to their zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) characteristics, which make them a good candidate for achieving high efficiencies at high frequencies. That in turn results in reduced sizes for the passive components, and thus higher power densities, higher loop-gain bandwidths, and faster transient responses. This has led to the investigation of their adoption into different applications conventionally dominated by PWM converters, including DC-DC [18]-[29] and AC-DC conversion [30]-[35].

[^3]In this paper, the analysis and design flow for a resonant PFC rectifier for single-phase offline converters are presented. The system, shown in Fig. 2, incorporates an input filter and bridge, a charge pump circuit, a DC energy-storage capacitor, and a class-DE converter. The proposed converter can achieve PFC inherently, where the operation is based on soft switching, allowing for high-frequency design with reduced passives sizes, in addition to freedom from the limited bandwidths of the PFC controllers available on the market.

This paper is organized as follows: section II illustrates the principle of operation of the proposed converter. Circuit analysis is presented in section III. Section IV covers the design process of the converter. Prototype implementation and experimental results are shown in section V. Finally, conclusion is provided in section VI.

## II. Principle of operation

This section describes the principle of operation of the charge pump PFC converter. A charge pump electronic ballast circuit is reported in [36]. With the addition of an auxiliary circuit comprised of a capacitor and a diode to a conventional highfrequency inverter circuit, the input current can be regulated to follow the input voltage. In this work, the charge pump circuit is incorporated into a class-DE series-resonant converter, as shown in Fig. 3, where the inverter circuit is cascaded by a highfrequency rectifier for enabling use in AC-DC converters [37].

The driving signals to the switches are synchronized with a switching frequency that guarantees operation above resonance, with the same duty cycle and extended dead time. This allows the resonant tank current to charge and discharge the halfbridge switches output capacitances, so that their voltages reach the appropriate rail voltage before switching the gate, thus ensuring ZVS. Additionally, the DC energy-storage capacitor $C_{D C}$ is placed at the inverter input, thus helping to achieve softswitching operation along the constantly varying AC input line voltage, with no effect on the power factor and input current shape.

Fig. 4 shows a simplified circuit diagram for the power converter, where the input filter is omitted and a diode $D_{B}$ models the input bridge for simplicity. The figure also shows


Fig. 2. Proposed PFC stage architecture.


Fig. 3. Proposed PFC converter.
the voltages and currents signs convention used throughout the analysis and rest of figures.

The DC energy-storage capacitor $C_{D C}$ is designed in accordance with the pump capacitor $C_{P}$ such that the voltage $V_{D C}$ is always higher than the input voltage $V_{I N}$, and thus the diode bridge $D_{B}$ and the pump diode $D_{P}$ do not cross-conduct. As a result, the input current $I_{I N}$ is equal to the charging current of the pump capacitor (positive $I_{P}$ ).

## A. Operation across Line Cycle

Fig. 5 shows the behavioral circuit operation across half an input line cycle. As the charge pump capacitor is connected between a low-frequency voltage node $V_{B}$ and a high-frequency voltage node $V_{R E C}$, charge flows through $C_{P}$ only during voltage changes on the high-frequency node. This results in voltage changes across $C_{P}$, as the other node is relatively constant with respect to high-frequency voltage changes. The pump capacitor charge $Q_{P}$ is proportional to the capacitor value $C_{P}$ and the voltage across it, $V_{P}$, where the latter varies between a lowfrequency high-value $V_{P_{-} \text {high }}$ and a constant low-value $V_{P_{-} \text {low }}$. The circuit design ensures that the voltage variation across the pump capacitor $V_{P}$ follows the input voltage $V_{I N}$ across the line cycle, resulting in a charge variation $Q_{P}$, and accordingly an input current, proportional to the input voltage, and a unity power factor can ideally be obtained.

It is noted that the $V_{R E C}$ voltage can be any kind of waveform with a constant AC amplitude, and the DC bias of $V_{R E C}$ has no effect on the input current shape, which makes the proposed converter architecture, shown in Fig. 2, compatible with different arrangements for the resonant tank, including the parallel-resonant, LCC, and LLC arrangements.


Fig. 4. Simplified circuit diagram for half-line cycle operation.


Fig. 5. Behavioral circuit operation across half a line cycle ( 50 Hz ).

## B. Operation across Switching Cycle

Fig. 6 shows waveforms for several circuit currents and voltages across two switching cycles, where the circuit and devices parasitics are ignored for simplicity. The circuit operation spans six intervals, where energy is exchanged between the line input, the pump capacitor, the resonant tank, the DC capacitor, and the load. The converter operates in the inductive mode of operation, where the resonant tank current $I_{R E S}$ lags the switching node voltage $V_{S W}$, and thus ZVS can be achieved. Fig. 7 shows the equivalent circuits and resonant tank current paths across the different intervals of operation.

In interval 1 (including 1A and 1B), the voltage $V_{B}$ is lower than $V_{D C}$ and higher than $V_{I N}$, so both the diodes $D_{B}$ and $D_{P}$ are off, and no current flows through the pump capacitor. Meanwhile, the energy stored in the circuit is transferred to the output through $D_{R I}$. Fig. 7 (a) shows the resonant inductor current direction in interval 1 A , where the high side switch is on and the low side switch is off, and charge flows from the DC capacitor through the resonant tank to the load. In interval 1B, the switching node voltage toggles, and the energy stored in the resonant tank is transferred to the output, as shown in Fig. 7 (b).
Interval 2 takes place across the fall time of $V_{R E C}$. Once $V_{R E C}$ starts to decrease, $V_{B}$ has to decrease along, until $D_{B}$ is forward biased and $V_{B}$ is pulled to $V_{I N}$. While $V_{R E C}$ continues to decrease, with $V_{B}$ almost constant (as the grid frequency is significantly lower than the switching frequency), $V_{P}$ increases and $C_{P}$ is charged by the line current $I_{I N}$, as shown in Fig. 7 (c), until $V_{R E C}$ reaches its low value and $V_{P}$ reaches its high value, where

$$
\begin{equation*}
V_{P_{-} \text {high }}=V_{I N}-V_{\text {REC_low }} \tag{1}
\end{equation*}
$$

Meanwhile, $V_{S W}$ is low, so $C_{P}$ charges through the resonant tank and low-side switch, and the load is supplied by Cout.

The third interval (including 3A and 3B) begins once $V_{R E C}$ settles at the low-value, when $C_{P}$ stops charging and while $D_{P}$ still blocks. Similar to interval 1, no current flows through the pump capacitor and $V_{P}$ is constant. Fig. 7 (d) shows the resonant tank current direction in interval 3A, where the current


Fig. 6. Circuit operation across two switching cycles (Arrows on the pump capacitor current $I_{P}$ waveform reflect the variation of the capacitor charge $Q_{P}$ across line cycle).
freewheels in $D_{R 2}$ and $Q_{L S}$. In interval 3B, the switching node voltage toggles, and energy is transferred from the resonant tank to the DC capacitor through $Q_{H S}$ and $D_{R 2}$, as shown in Fig. 7 (e). Throughout the interval, the load is supplied by Cout.
Interval 4 takes place across the rise time of $V_{R E C}$. Once $V_{R E C}$ starts to increase, $V_{B}$ has to increase along until $D_{P}$ is forward biased and $V_{B}$ is pulled to $V_{D C}$. While $V_{R E C}$ continues


Fig. 7. Equivalent circuits with resonant tank current paths (dashed arrows) across different intervals of operation.
decreasing, with $V_{D C}$ almost constant, $V_{P}$ decreases and energy transfers from $C_{P}$ to resonant tank, as shown in Fig. 7 (f), until $V_{R E C}$ reaches its high value, and $V_{P}$ reaches its low value, where

$$
\begin{equation*}
V_{P_{-} \text {low }}=V_{D C}-V_{R E C \_h i g h} \tag{2}
\end{equation*}
$$

Meanwhile, the load is supplied by Cout. $^{\text {. By }}$ the end of the fourth interval, operation enters interval 1 again and the cycle repeats.
The analysis shows that the input current is discontinuous, only flows into the circuit during the second interval, and is equal to the charging pump capacitor current (positive $I_{P}$ shown in Fig. 6), where the charge $Q_{P}$ is equal to the charge taken from the line input $Q_{I N}$.
Depending on the value for the input line voltage $V_{I N}$ across the line cycle, the length of intervals 2 and 4 gets extended or narrowed with respect to the amount of charge taken from the input AC mains, which is shown by the arrows on the $I_{P}$ waveform in Fig. 6. When $V_{I N}$ is high, the majority of the load energy comes from the line, thus $Q_{I N}$ increases, extending the lengths of intervals 2 and 4 , which reach their maximum at the peak input AC mains voltage ( $\omega_{l} t=\pi / 2,3 \pi / 4$ ). On the other hand, when the $V_{I N}$ is low, the majority of the load energy comes from the DC capacitor $C_{D C}$, with reduced charge taken from the input AC mains. That, in turn, narrows the lengths for intervals 2 and 4 , which reach zero value at the zero crossings of the input AC mains voltage ( $\omega_{l} t=\pi, 2 \pi$ ), then the charge $Q_{P}$ equals zero, as shown in Fig. 5, and all of load energy then comes from $C_{D C}$. Therefore, at the zero-crossings of the input voltage, the classDE stage operates in a conventional nature, with no effect from the charge-pump circuit. While at the peaks of $V_{I N}$, the chargepump capacitor is at full capacity, loading the resonant tank and DC capacitor with the peak charge taken from the line, resulting in additional circuit stresses that are analyzed as follows.

## III. Circuit Analysis

In this section, the circuit analysis is presented. The analysis is based on the First Harmonic Approximation (FHA) approach for modelling resonant converters, which assumes the resonant tank current to be sinusoidal. That is ensured through the design for a high loaded quality factor in the resonant tank. With that assumption, a simple analysis and design flow is presented, sparing the need for an accurate model that takes into account the high-order harmonics in the resonant tank and pump circuit, thus simplifying the design process.
Two conditions for proper functionality of the circuit are illustrated. These conditions set the basis for the design process covered in the following section. In addition, the different circuit stresses that result from the incorporation of the chargepump circuit into the class-DE resonant stage are analyzed. The stresses include the resonant tank peaking current and the DC capacitor peaking voltage. The section starts with finding the first condition for achieving high power factor based on the principle of operation illustrated in section II, which sets the basis for the class-DE stage design. That is followed by two analyses for the voltage across the DC capacitor, including the average voltage value, which is a function of the pump capacitor $C_{P}$ size, and the low-frequency voltage ripple, which is a function of the $C_{D C}$ size. Another condition for ensuring full
control over the input current is then illustrated, which sets the requirement for the design of the two capacitors. Eventually, an analysis of the maximum resonant tank peak current across line cycle is presented, which defines the specifications for the resonant inductor design.

## A. First Condition for Obtaining High Power Factor

From the circuit operation covered in section II-B, and considering that for a series-resonant tank the rectifier input voltage $V_{\text {REC }}$ swings between zero volts and the output voltage, as shown in Fig. 6, (1) and (2) can be re-evaluated as follows

$$
\begin{align*}
V_{P_{\_} \text {high }} & =V_{I N}-V_{R E C \_ \text {low }}=V_{I N}-0=V_{I N}  \tag{3}\\
V_{P_{-} \text {low }} & =V_{D C}-V_{R E C \_h i g h}=V_{D C}-V_{O U T} \tag{4}
\end{align*}
$$

The equations show that the envelope of the high values for the voltage across the pump capacitor takes the shape of the input voltage, while the low-values envelope takes the value of the difference between the resonant converter's input and output voltages, which is almost constant in high frequency. Across one switching cycle, the variation of charge in the pump capacitor is equal to

$$
\begin{equation*}
Q_{P}=C_{P}\left(V_{P_{-} \text {high }}-V_{P_{-} \text {low }}\right)=C_{P}\left(V_{I N}-V_{D C}+V_{\text {OUT }}\right) \tag{5}
\end{equation*}
$$

The pump capacitor charging current, which is equal to the input current, averaged over one switching cycle is equal to

$$
\begin{equation*}
I_{I N}=\frac{Q_{P}}{T_{s}}=f_{s} \cdot Q_{P}=f_{s} \cdot C_{P}\left(V_{I N}-V_{D C}+V_{O U T}\right) \tag{6}
\end{equation*}
$$

where $f_{s}$ is the converter switching frequency. Considering the class-DE stage is designed to operate near resonance, with a high gain close to unity, the difference between $V_{D C}$ and $V_{O U T}$ gets to be very small. Assuming $V_{D C} \approx V_{O U T}$, (6) is re-evaluated to

$$
\begin{equation*}
I_{I N} \approx f_{s} \cdot C_{P} \cdot V_{I N} \tag{7}
\end{equation*}
$$

Therefore, in steady state, the input current becomes proportional to the input voltage, resulting in a high power factor and low total harmonic distortion (THD). Accordingly, this condition sets the specification for the class-DE stage design.

## B. Energy-Storage Capacitor Average Voltage Analysis

From (6), the input power averaged over a switching cycle is obtained by

$$
\begin{equation*}
P_{I N}=V_{I N} \cdot I_{I N}=f_{S} \cdot C_{P} \cdot V_{I N}\left(V_{I N}+V_{\text {OUT }}-V_{D C}\right) \tag{8}
\end{equation*}
$$

And knowing that

$$
\begin{equation*}
V_{I N}=V_{I N_{-} p k} \sin \left(\omega_{l} t\right) \tag{9}
\end{equation*}
$$

The input power averaged over a line cycle is found by

$$
\begin{equation*}
P_{I N \_a v g}=\frac{1}{T_{l}} \int_{0}^{T_{l}} P_{I N} d t=\frac{2}{T_{l}} \int_{0}^{\frac{T_{l}}{2}} P_{I N} d t \tag{10}
\end{equation*}
$$

Substituting (8) in (10), the integral is evaluated to
$P_{I N \_a v g}=f_{S} \cdot C_{P} \cdot V_{I N_{-} p k}\left[\frac{V_{I N \_p k}}{2}+\frac{2}{\pi}\left(V_{\text {OUT }}-V_{D C_{-} a v g}\right)\right]$

Equating to $P_{\text {OUT }} / \eta$ and rearranging to find $V_{D C_{-} \text {avg }}$

$$
\begin{equation*}
V_{D C_{\_} a v g}=V_{O U T}+\frac{\pi}{2}\left(\frac{V_{I N \_p k}}{2}-\frac{P_{\text {OUT }}}{\eta \cdot f_{s} \cdot C_{P} \cdot V_{I N_{\_} p k}}\right) \tag{12}
\end{equation*}
$$

where $\eta$ is the converter efficiency. Therefore, the charge-pump circuit results in a stress on the DC capacitor voltage, where a larger pump capacitor results in a higher voltage stress across the DC capacitor.

## C. Energy-Storage Capacitor Voltage Ripple Analysis

For an AC-DC rectifier, the difference between the instantaneous input power and the constant output power needs to be stored within a circuit element. In case of the proposed converter, that element is the DC energy-storage capacitor $C_{D C}$. As discussed in section II-B, when the input voltage is high, so is the input power, and the majority of the energy comes from the line and gets stored in the pump capacitor $C_{P}$, which then charges the DC bus capacitor $C_{D C}$, increasing the voltage across it. On the other hand, when the input voltage is low, $C_{D C}$ expends more energy to the load than what it stores from the line, decreasing the voltage $V_{D C}$. Further, when the input voltage is zero, all energy comes from the DC capacitor and it does not store any charge. This results in a double-the-linefrequency voltage ripple across the DC capacitor, as shown in Fig. 8, which is evaluated from the energy of the DC capacitor as follows. The power flowing into the DC capacitor is

$$
\begin{equation*}
P_{D C}=P_{I N}-P_{O U T} \tag{13}
\end{equation*}
$$

Assuming a power factor of one, where the input voltage and current are sinusoids and in phase, and rewriting (8), the input power is calculated to

$$
\begin{align*}
& P_{I N}=V_{I N_{p k}} \cdot I_{I N_{p k}} \sin ^{2}\left(\omega_{l} t\right) \\
= & \frac{V_{I N_{\_} p k} \cdot I_{I N_{-} p k}}{2}\left[1-\cos \left(2 \omega_{l} t\right)\right] \tag{14}
\end{align*}
$$

For simplicity, assuming $100 \%$ efficiency

$$
\begin{equation*}
P_{\text {OUT }}=P_{I N_{\_} a v g}=\frac{V_{I N \_p k} \cdot I_{I N \_p k}}{2} \tag{15}
\end{equation*}
$$

Substituting (14) and (15) in (13) gives

$$
\begin{equation*}
P_{D C}=-P_{O U T} \cos \left(2 \omega_{l} t\right) \tag{16}
\end{equation*}
$$

Finding the energy


Fig. 8. The input power and DC capacitor voltage waveforms.

$$
\begin{gather*}
E_{D C}=\int_{0}^{T_{l}} P_{D C} d t=E_{D C}(0)-\frac{P_{\text {OUT }} \sin \left(2 \omega_{l} t\right)}{2 \omega_{l}} \\
=\frac{1}{2} C_{D C} \cdot V_{D C}{ }^{2} \tag{17}
\end{gather*}
$$

Rearranging for $V_{D C}$ and knowing that $V_{D C}(0)$ is equal to the rms voltage [38]

$$
\begin{equation*}
V_{D C}=V_{D C_{\_} r m s} \sqrt{1-\frac{P_{O U T}}{\omega_{l} \cdot C_{D C} \cdot V_{D C_{-} r m s}}{ }^{2}} \sin \left(2 \omega_{l} t\right) \tag{18}
\end{equation*}
$$

With the AC ripple being sufficiently smaller than $V_{D C_{-} r m s, ~ t h e ~}^{\text {en }}$ ripple amplitude can be evaluated by

$$
\begin{equation*}
V_{D C_{-} \text {ripple }} \approx \frac{P_{O U T}}{2 \omega_{l} \cdot C_{D C} \cdot V_{D C_{-} r m s}} \tag{19}
\end{equation*}
$$

Therefore, the low-frequency ripple on the DC capacitor voltage is a function of the output power and the DC capacitor $C_{D C}$ size.

## D. Second Condition for Obtaining High Power Factor

From the analyses for the average DC capacitor voltage and its low frequency ripple, the pump and DC capacitors should be designed such that the minimum DC capacitor voltage is higher than the peak input voltage. That guarantees no crossconduction occurs through the diode bridge and the pump diode, the case allowing current to flow directly from the line input to the DC capacitor, which reduces the power factor. Therefore, for a high power factor, the following condition needs to be satisfied

$$
\begin{equation*}
V_{D C_{-} \text {ripple }}<V_{D C_{\_} a v g}-V_{I N_{-} p k} \tag{20}
\end{equation*}
$$

Therefore, equation (20) sets a design specification for the maximum ripple on the DC capacitor voltage, and accordingly the minimum size of the DC capacitor for a given average voltage across it, where the latter is a function of the pump capacitor size.

## E. Resonant Tank Maximum Current Amplitude Analysis

From the circuit operation illustrated in section II-B, it is shown that the resonant tank carries both the charge pump circuit current as well as the current to the output load. The input charge $Q_{I N}$ stored in the charge pump capacitor is transferred to the resonant tank in interval 4, while the output charge $Q_{\text {out }}$ is supplied to the load by the DC capacitor and the resonant tank in intervals 1A and 1B respectively. Accordingly, a total charge of $Q_{\text {тот }}$ gets stored then depleted from the resonant tank within one half of a switching cycle, as shown in Fig. 6 (shadowed area), where

$$
\begin{equation*}
Q_{T O T}=Q_{I N}+Q_{O U T}=\int_{0}^{\frac{T_{S}}{2}} I_{R E S}(t) d t \tag{21}
\end{equation*}
$$

With the assumption that the resonant tank has a high-enough loaded quality factor $Q_{L}$ with near-resonance operation, the resonant tank current is a sinusoidal waveform that can be described by

$$
\begin{equation*}
I_{R E S}(t)=I_{R E S_{-} p k} \sin \left(\omega_{s} t\right) \tag{22}
\end{equation*}
$$

Accordingly, (21) is evaluated to

$$
\begin{equation*}
Q_{\text {IN }}+Q_{\text {OUT }}=\frac{T_{S}}{\pi} I_{\text {RES_} \_p k} \tag{23}
\end{equation*}
$$

Dividing both sides of (23) by $T_{s}$ gives the average currents across the switching cycle

$$
\begin{equation*}
I_{I N}+I_{O U T}=\frac{I_{\text {RES_pk }}}{\pi} \tag{24}
\end{equation*}
$$

Assuming $I_{\text {OUT }}$ is constant and $I_{I N}$ is a sinusoid in phase with the input voltage $V_{I N}$ (unity power factor), the maximum values for both currents are evaluated to

$$
\begin{gather*}
I_{\text {OUT }}=\frac{P_{\text {OUT }}}{V_{\text {OUT }}}  \tag{25}\\
I_{I N_{-} p k}=\frac{P_{I N_{\_} p k}}{V_{I N_{-} p k}}=\frac{2 P_{I N_{\_} a v g}}{V_{I N_{-} p k}}=\frac{2 P_{\text {OUT }}}{\eta \cdot V_{I N_{-} p k}} \tag{26}
\end{gather*}
$$

The maximum value for the resonant tank current amplitude across a line cycle, which occurs at the peak input voltage, is then evaluated to be

$$
\begin{equation*}
I_{\text {RES_max }}=\pi P_{\text {OUT }}\left(\frac{2}{\eta \cdot V_{I N_{-} p k}}+\frac{1}{V_{\text {OUT }}}\right) \tag{27}
\end{equation*}
$$

Accordingly, the charge pump circuit results in a stress in the resonant tank current, which is a function of the input voltage and output power of the converter.

## IV. Design

This section illustrates the design process for the proposed converter based on the analyses and design conditions covered in section III. The design criteria covers the design for a given set of specifications while satisfying the conditions for obtaining a high power factor. First, the pump capacitor needs to be large enough to store the maximum input charge from the AC mains, which is function of the output power, the peak input voltage, and the switching frequency. Second, the energystorage DC capacitor needs to be designed such that the voltage across it, $V_{D C}$, is always higher than the input voltage $V_{I N}$ across the line cycle in steady state. That ensures the diode bridge and the pump diode cannot conduct at the same time, and no direct current flow from the line input to the DC capacitor, thus providing full control on the input current, which has to flow through the pump capacitor. Lastly, the class-DE stage is designed based on the analysis in section III-A, which sets a condition for the stage voltage gain to be high (close to unity). That ideally eliminates the dependence of the input current on the DC capacitor voltage $V_{D C}$ and the output voltage $V_{O U T}$, and makes it function of only the input voltage in steady state, as shown by (7).

## A. Charge Pump Capacitor Design

The maximum current through the pump capacitor (averaged over a switching cycle) is equal to the peak input current, which takes place at the peak input voltage and is calculated from (26). Substituting in (7) and rearranging for $C_{P}$

$$
\begin{equation*}
C_{P} \geq \frac{2 P_{\text {OUT }}}{\eta \cdot f_{s} \cdot V_{\text {IN_pk }}{ }^{2}} \tag{28}
\end{equation*}
$$

To account for the power stage gain not being one ( $V_{D C}-V_{\text {OUT }}$ $\neq 0$ ), the value for $C_{P}$ can be adjusted to be marginally larger than that obtained from (28), while keeping in mind that a larger $C_{P}$ results in higher voltage stress across $C_{D C}$.

## B. Energy-Storage DC Capacitor Design

From (12) and (20), a specification is found for the maximum allowed ripple on the DC capacitor voltage in order to guarantee proper operation and high power factor. From (19), rearranging for $C_{D C}$, and considering a conservative substitution of $V_{D C \_a v g}$ for $V_{D C_{-} r m s}$, the sizing for the DC capacitor for a given ripple is found from

$$
\begin{equation*}
C_{D C} \geq \frac{P_{\text {OUT }}}{2 \omega_{l} \cdot V_{\text {DC_ripple }} \cdot V_{D C_{\_} \text {avg }}} \tag{29}
\end{equation*}
$$

For applications with relaxed requirements for power factor and THD, some cross-conduction can be allowed to occur without violating the specifications, where some charge will flow directly from the input line to the DC capacitor, resulting in a short notch in the input current waveform. Thus, the sizing for both capacitors constitutes a design trade-off between circuit stresses, power quality and power density.

## C. Class-DE Stage Design

The design procedure given in [14] is used for the class-DE stage design. The procedure starts by calculating the rectifier input resistance $R_{R E C}$ from the load resistance $R_{L}$ through impedance transformation via the resonant rectifier as follows

$$
\begin{equation*}
R_{R E C}=\frac{2 R_{L}}{\pi^{2}}=\frac{2 V_{\text {OUT }}{ }^{2}}{\pi^{2} \cdot P_{\text {OUT }}} \tag{30}
\end{equation*}
$$

The voltage conversion ratio is equal to

$$
\begin{equation*}
M_{V}=\frac{V_{\text {OUT }}}{V_{D C_{\_} a v g}} \tag{31}
\end{equation*}
$$

Considering a half bridge for the inverter switching network and a class-D rectifier, the overall converter gain becomes approximately equal to the resonant tank gain. The converter loaded quality factor is then calculated using the following equation

$$
\begin{equation*}
Q_{L}=\frac{\sqrt{\frac{1}{M_{V}^{2}}-1}}{f_{n}-\frac{1}{f_{n}}} \tag{32}
\end{equation*}
$$

where $f_{n}$ is the normalized switching frequency, equal to $f_{s} / f_{o}$, with $f_{o}$ being the resonant frequency. In order to ensure the validity of the above analysis based on the FHA approach, the loaded quality factor $Q_{L}$ of the resonant circuit needs to be high enough so that the current through the resonant circuit is sinusoidal. A loaded quality factor of $\sim 2.5$ is sufficient [14]. The normalized switching frequency is then obtained from (32). Following, and for a specified switching frequency $f_{s}$, the resonant tank component values are calculated

$$
\begin{equation*}
f_{o}=\frac{f_{s}}{f_{n}} \tag{33}
\end{equation*}
$$

$$
\begin{gather*}
L_{R E S}=\frac{Q_{L} \cdot R_{R E C}}{\omega_{o}}  \tag{34}\\
C_{R E S}=\frac{1}{\omega_{o} \cdot Q_{L} \cdot R_{R E C}} \tag{35}
\end{gather*}
$$

It is worth mentioning that a higher $Q_{L}$ value would not affect the power factor, as it guarantees a more sinusoidal resonant tank current with lower harmonic content. However, it can complicate the magnetic devices design, see (34), which is a challenge for this topology with the high current stress in the inductor, as shown by (27), and can result in low efficiency. On the other hand, a lower value for $Q_{L}$ can result in mismatch between the proposed design flow and the realized values, as the current in the tank is no longer sinusoidal, and an accurate model taking into account the high-order harmonics in the resonant tank and the pump circuit is then needed, which complicates the design.

The rectifier devices stresses are calculated as follows

$$
\begin{gather*}
V_{D_{\_} \max }=V_{\text {OUT }}+V_{\text {OUT_ripple }}  \tag{36}\\
I_{D_{\_} \max }=\pi I_{\text {OUT }} \tag{37}
\end{gather*}
$$

while the voltage stress for the half-bridge switches is the same as the DC and pump capacitors voltage stresses, and is equal to

$$
\begin{equation*}
V_{S_{-} \max }=V_{D C_{-} a v g}+V_{D C_{-} \text {ripple }} \tag{38}
\end{equation*}
$$

and the current stress in the half bridge is equal to that of the resonant tank obtained from (27).

## V. 1 MHz 50 W PRototype

This section covers the design and implementation of a 1 MHz 50 W prototype based on the analysis and design conditions obtained from sections III and IV. Starting from the design specifications, the design procedure for the presented specifications is illustrated, followed by a presentation of the simulation results used for functional verification. The resonant inductor design process is then covered, followed by a description of the implementation of the overall prototype. Eventually, experimental results are presented and compared against the analysis and circuit simulation results.

## A. Design Specifications

Table I lists the specifications for the designed prototype, which is proposed for PFC rectifiers supplied from European mains for low-power range applications. A switching frequency of 1 MHz is specified for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. As discussed in section IV-A, the gain of the class-DE stage has to be high to allow for a high power factor and low THD. A good approximation is to design for 300 V output voltage for a peak input voltage of 325 V . It is,

TABLE I. DESIGN SPECIFICATIONS.

| Specifications | Input Voltage | $230 \mathrm{~V}_{\mathrm{rms}}$ |
| :---: | :---: | :---: |
|  | Line Frequency | 50 Hz |
|  | Output Power | 50 W |
| Design | Switching Frequency | 1 MHz |
| Considerations | Output Voltage | 300 V |

however, possible to design for lower output voltages through the insertion of a high-frequency transformer in the rectifier circuit. As long as the pump capacitor is coupled to a highfrequency node with high voltage gain, inherent PFC functionality is achieved.

## B. Prototype Design Procedure

From the design specifications, the design process starts by sizing the pump capacitor according to the output power, the input voltage, and switching frequency. Finding the minimum value for $C_{P}$ from (28), a marginally higher value is chosen to account for the non-unity gain of the class-DE stage. The DC capacitor voltage stress is then calculated from (12). Following, the specification for the double-the-line-frequency ripple on the DC capacitor voltage is evaluated from (20) in order to guarantee high power factor. The DC capacitor is then designed for the specified low-frequency ripple according to (29). Eventually, the class-DE stage design takes place according to the procedure given in section IV-C, using (30-38), where the resonant tank current stress is calculated from (27).

It is worth noting that this design procedure is a first pass approach, as numerous issues have been neglected for simplicity, including parasitics and other non-idealities. A design decision is made for power quality, where a design iteration with respect to a larger pump capacitor and/or a larger DC capacitor can be needed. Another decision is then made on whether the design specifications with respect to power density and efficiency are met. If not, a design iteration with respect to class-DE stage design is conducted for a different output voltage and/or resonant tank quality factor.
Table II lists the obtained design values according to the specifications given in Table I, with a resonant tank quality factor of 2.4 and assuming $90 \%$ efficiency.

## C. Simulation Results

Based on the analysis and calculated values, the circuit is simulated in LTspice for functional verification. Fig. 9 shows the simulation results at full-load operation. Fig. 9 (a) shows the line-frequency waveforms at an output power of 50.6 W and an average output voltage of 300 V , with a power factor of 0.99 and a THD of $5.5 \%$. Fig. 9 (b) shows the switching-frequency waveforms at the peak input power ( $\omega_{t} \mathrm{t}=\pi / 2,3 \pi / 4$ ), where ZVS operation is observed on the $V_{S W}$ waveform, which peaks to $\sim$ 370 V , while a sinusoidal resonant tank current with a peak value of 1.6 A is observed. Thus, the results go in accordance with the analysis in section IV and the calculated values in section V-B.

## D. Resonant Inductor Design

Table III summarizes the specifications for the resonant inductor design, which are obtained from the circuit analysis

TABLE II. DESIGN VALUES CALCULATED FROM CIRCUIT ANALYSIS.

| Parameter | Calculated |
| :---: | :---: |
| $C_{P}$ (min.) | 1.05 nF |
| $V_{D C \text { avg }}$ | 349 V |
| $C_{D C}$ (min.) | $9.6 \mu \mathrm{~F}$ |
| $L_{R E S}$ | $158 \mu \mathrm{H}$ |
| $C_{R E S}$ | 206 pF |
| $I_{R E S \text { max }}$ | 1.6 A |



Fig. 9. Simulation results at full-load operation.
and verified with simulation results, where the peak current amplitude and the inductance specifications are obtained from (27) and (34) respectively.

When handling high-frequency AC currents, a key factor to the inductor design is choosing the right core material. Several magnetic materials [39][40] are investigated and compared in terms of core losses at 1 MHz , as shown in Fig. 10, where the 3F46 material is chosen, as it shows the lowest core losses at the design operating conditions. The following equation is used to estimate the inductor core losses. The peak flux density in the core can be calculated from [38]

$$
\begin{equation*}
B_{\max }=\frac{1}{N} \cdot \frac{I_{R E S \_\max } \cdot L}{A_{e}} \tag{39}
\end{equation*}
$$

where $N$ is the number of turns, $L$ is the inductance, and $A_{e}$ is the effective core cross-sectional area. Considering that the core

TABLE III. RESONANT INDUCTOR DESIGN SPECIFICATIONS.

| Parameter | Specification |
| :---: | :---: |
| Inductance | $158 \mu \mathrm{H}$ |
| Current Frequency | 1 MHz sinusoid |
| Current Peak Amplitude | 1.6 A |



Fig. 10. Core power-loss density (Pv) vs. magnetic flux density (B) for different magnetic materials at 1 MHz .
losses are a function of the peak flux density for a chosen material, the losses for a given number of turns and core size can be estimated. The following calculation of the DC resistance of the windings gives an estimate of the winding losses. The total cross-sectional area of the windings $A_{c}$ is calculated from

$$
\begin{equation*}
A_{c}=n_{\text {wires }} \cdot \pi \cdot r_{\text {wire }}{ }^{2} \tag{40}
\end{equation*}
$$

where $n_{\text {wires }}$ is the number of strands of Litz wire and $r_{\text {wire }}$ is the wire radius. The DC resistance is then calculated from

$$
\begin{equation*}
R_{d c}=\rho_{c u} \cdot \frac{M L T \cdot N}{A_{c}} \tag{41}
\end{equation*}
$$

where $\rho_{c u}$ is the copper resistivity and $M L T$ is the mean length of turn. For an EFD 25/13/9 core size, with two parallel layers of $20 \times 0.05 \mathrm{~mm}$ Litz wire, the DC resistance is calculated to $8.6 \mathrm{~m} \Omega \cdot \mathrm{~N}$.

Next, the AC resistance of the windings is calculated. The skin effect is negligible when using Litz wire at 1 MHz , but the proximity effect can have a significant influence on the closely wound wires. Modelling the AC resistance to be three times larger than the DC resistance (based on empirical tuning), the winding losses are estimated to

$$
\begin{equation*}
P_{c u}=R_{a c} \cdot I_{r m s}^{2}=3 \cdot R_{d c} \cdot \frac{I_{\text {RES_max }}{ }^{2}}{2}=33 \mathrm{~mW} \cdot \mathrm{~N} \tag{42}
\end{equation*}
$$

Fig. 11 shows the inductor losses vs. number of turns. Based on these estimates, the inductor is designed with 52 turns, which helps to distribute the losses evenly between the core and the winding, and results in acceptable total losses. An airgap of 1.2 mm , distributed across the three legs of the core, adjusted the desired inductance. Fig. 12 shows the small signal characteristics of the implemented inductor measured using a $40 \mathrm{~Hz}-110 \mathrm{MHz}$ precision impedance analyzer (Agilent Technologies 4294A). At 1 MHz , an inductance of $152.3 \mu \mathrm{H}$ and an ESR of $2.5 \Omega$ are obtained, corresponding to a $Q$-value of 380 and 3.2 W of losses when excited with a 1.6 A sinusoidal current. This is a first-pass approach for the resonant inductor design, which assumes room temperature for inductor core and


Fig. 11. Inductor losses vs. number of turns.


Fig. 12. Resonant inductor inductance and ESR measurements.
windings, and does not take into account the impact of the nonideal field distribution in the core and the windings self-heating.

## E. Implementation

Fig. 13 shows a photograph of the implemented prototype power stage. The converter is implemented and assembled on a two-layer printed circuit board (PCB). Because of the chargepump circuit operation, a high-frequency AC current runs through the input bridge, which is implemented using four fastrecovery diodes. With respect to selection of switches, Fig. 14 shows a comparison based on datasheet parameters between the best in-class switches figures of merit [41]-[44], where gallium nitride ( GaN ) FETs show superior performance compared to the silicon superjunction and silicon carbide ( SiC ) counterparts.

Device 6 in Fig. 14 is used for the inverter design. The switches gate-driving circuit is comprised of a digital isolator (Si8610BC by Silicon Labs) and a gate driver (UCC27611 by Texas Instruments) for each of the high-side and low-side switches. For the high-side driver supply, a bootstrap network of a diode (GB01SLT06-214, SiC Schottky) and a capacitor (1 $\mu \mathrm{F}$, ceramic X 7 R ) is used, in addition to a peripheral solution comprised of isolated power supplies (MTE1S0506MC by Murata), and both circuits are equally operational.

In order to control noise coupling from the power loop to gate-drive loop, the gate driver packages are placed as close as possible to the devices gate terminals to minimize the gate parasitic inductance. Another layout consideration taken is the separation of the source terminal to the driving and power loops


Fig. 13. Prototype power stage.


Fig. 14. Summary of best in-class switches' figures of merit.
in a star-connected fashion. That helps alleviate the gate ringing resulting from the common-source inductance. As the selected gate driver offers separate source/sink outputs, a separate 0402 SMD gate resistor is added to each path to control the miller effect. A source gate resistor of $30 \Omega$ is chosen to reduce the turn-on dv/dt slew rate and limit gate oscillation. On the other hand, a sink gate resistor of $4 \Omega$ is chosen to provide a strong pull-down during turn-off, hence preventing the false turn-on events with the low threshold voltage of GaN FETs.

For the rectifier side, SiC Schottky diodes are employed, as they show higher efficiency compared to the silicon high-

TABLE IV. PROTOTYPE POWER-STAGE BOM.

| Component | Calculated | Simulated | Prototype | Type |
| :---: | :---: | :---: | :---: | :---: |
| $L_{I N}$ |  | $100 \mu \mathrm{H}$ | $100 \mu \mathrm{H} / 0.5 \mathrm{~A}$ | Inductor |
| $C_{I N}$ |  | 30 nF | $2 * 15 \mathrm{nF} / 450 \mathrm{~V}$ | Ceramic (C0G) |
| Diode Bridge |  |  | $4 * \mathrm{ESH} 1 \mathrm{GM}$ RSG | Si Fast Recovery |
| $C_{D C}$ | $9.6 \mu \mathrm{~F}$ | $10 \mu \mathrm{~F}$ | $* * 10 \mu \mathrm{~F} / 450 \mathrm{~V}$ <br> $3 * 0.1 \mu \mathrm{~F} / 450 \mathrm{~V}$ | Electrolytic <br> Ceramic (C0G) |
| $D_{P}$ |  |  | RF 201 LAM 4 S | Si Fast Recovery |
| $C_{P}$ | 1.05 nF | 1.3 nF | $2 * 680 \mathrm{pF} / 500 \mathrm{~V}$ | Ceramic (C0G) |
| $Q_{H S}, Q_{L S}$ |  |  | GS 66502 B | GaN Switches |
| $L_{R E S}$ | $158 \mu \mathrm{H}$ | $158 \mu \mathrm{H}$ | $152 \mu \mathrm{H} / 1.6 \mathrm{~A}$ | Custom design |
| $C_{R E S}$ | 206 pF | 200 pF | $220 \mathrm{pF} / 3 \mathrm{kV}$ | Ceramic (C0G) |
| $D_{R I}, D_{R 2}$ |  |  | $\mathrm{~GB} 01 \mathrm{SLT} 06-214$ | SiC Schottky |
| $C_{O U T}$ |  | 30 nF | $2 * 15 \mathrm{nF} / 450 \mathrm{~V}$ | Ceramic (C0G) |

voltage counterparts. Table IV shows a breakdown of the incorporated power stage bill-of-materials (BoM) for the proposed design.

## F. Experimental Results

The converter is tested for operation from $230 \mathrm{~V}_{\text {rms }}$ at switching frequencies between 0.96 MHz and 1.04 MHz , which are within the inductive mode of operation for the resonant converter, and accordingly, soft-switching operation can be achieved. Fig. 15 (a) shows the output power and efficiency across the operational frequency range for the proposed converter. Results illustrate that an output power ranging from 26.6 to 50 W is obtained through frequency modulation, while achieving a peak efficiency of $87.8 \%$. Fig. 15 (b) shows the power quality results. The converter achieves a peak power factor of 0.99 and minimum THD of $8.6 \%$, at an output power of 50 W and switching frequency of 0.96 MHz . Results show that operation at lower frequencies, close to resonance with higher gain, achieves higher power factor and lower THD, which goes in accordance with the analysis given in section III.

(a) Output power and efficiency.

(b) Power factor and THD.

Fig. 15. Obtained prototype measurements across operational frequency range.

Fig. 16 shows scope captures for the implemented prototype waveforms at full-load operation. Fig. 16 (a) shows the low frequency waveforms, including the input voltage and current as well as the output voltage. The input voltage is displayed using a high-voltage differential probe (Testec SI 9001), while the input current is measured using a 50 MHz current probe (Hioki CT6700), and the output voltage is measured using a 500 MHz 10x voltage probe with 9 pF capacitance. The figure shows an almost-sinusoidal input current with a phase difference of $5.7^{\circ}$ with the input voltage, and an average output voltage of 300 V , which matches the circuit analysis and the simulation results shown in Fig. 9 (a). A 100 Hz ripple of 40 V is measured on the output voltage, which is about $13 \%$ of the DC voltage and can be reduced through the incorporation of a larger DC capacitor. Fig. 16 (b) shows a scope capture for the high-frequency signals at full-load operation. The capture is taken with infinite persistence to visualize the variations across the input voltage range, which is the low-frequency ripple on the DC capacitor voltage. The resonant circuit current $I_{\text {RES }}$ is measured using a 50 MHz current probe (LeCroy AP015). The current is seen to be sinusoidal, thus ensuring the validity of the design process given in section IV-C, which is based on the FHA approach. The resonant tank current peaking effect matches the 1.6 A value obtained from the analysis in section III-E and the simulations results shown in Fig. 9 (b). The

(a) Line-frequency waveforms ( $V_{I N} 100 \mathrm{~V} /$ div, $I_{I N} 100 \mathrm{~mA} / \mathrm{div}$, $V_{\text {OUT }} 100 \mathrm{~V} / \mathrm{div}$ with $5 \mathrm{~ms} / \mathrm{div}$ ).

(b) Switching-frequency waveforms in infinite-persistence mode ( $V_{S W} 100$ V/div, $I_{R E S} 1 \mathrm{~A} /$ div, $H S G / L S G 5 \mathrm{~V} /$ div with $200 \mathrm{~ns} /$ div).

Fig. 16. Scope images for the implemented prototype waveforms at full-load operation.
switching node voltage waveform $V_{S W}$ is measured using a 500 MHz 10x voltage probe with 9 pF capacitance and shows that soft switching is obtained across the input voltage range.

Fig. 17 shows scope captures for the implemented prototype waveforms at half-load operation. As expected, operation at higher frequencies, away from resonance, results in lower power factor and higher THD, as observed from Fig. 17 (a), which are quantified in Fig. 15 (b). On the other hand, Fig. 17 (b) shows a reduced resonant tank current stress, resulting in higher efficiency at lower loads, as shown by Fig. 15 (a).
The driving signals to the switches are synchronized with the same duty cycle and extended dead time. For the full-load operation shown in Fig. 16 (b), the driving signals duty cycle is adjusted and fixed at $37 \%$, where ZVS is achieved and the average devices temperature is minimal, resulting in a dead time of 135 ns . Considering that the input voltage for the halfbridge is not dc, where it has the double-the-line-frequency ripple on top of the average DC capacitor voltage, see (38), full ZVS is achieved for the mid-range of $V_{D C}$. Whereas partial soft switching is observed at the lower end of that range, as longer dead time is needed. On the other hand, a short interval with GaN-FETs reverse conduction is noticed at the higher end of the range, for which a shorter dead time can achieve full ZVS.

Considering that the GaN device has zero reverse recovery charge $\left(Q_{R R}\right)$, the worst-case power loss due to reverse

(a) Line-frequency waveforms ( $V_{I N} 100 \mathrm{~V} / \mathrm{div}, I_{I N} 100 \mathrm{~mA} / \mathrm{div}, V_{\text {OUT }} 100 \mathrm{~V} / \mathrm{div}$ with $5 \mathrm{~ms} /$ div).

(b) Switching-frequency waveforms in infinite-persistence mode ( $V_{S W} 100$ V/div, $I_{R E S} 1$ A/div, $H S G / L S G 5 \mathrm{~V} /$ div with $200 \mathrm{~ns} /$ div).
Fig. 17. Scope images for the implemented prototype waveforms at half-load operation.
conduction can be estimated as follows. Fig. 18 shows measurement results for the reverse conduction characteristics of the employed GaN device across different temperatures with zero gate-source voltage (obtained using a Keysight B1505A curve tracer). Assuming an average reverse current $I_{\text {rev }}$ equal to the maximum resonant tank current, 1.6 A , a voltage drop of about 2.2 V is developed across the GaN device $\left(V_{\text {rev }}\right)$. From Fig. 16 (b), a reverse conduction interval $T_{\text {rev }}$ of 80 ns is observed for each device. The power loss due to reverse conduction $P_{\text {rev }}$ is then calculated to

$$
\begin{equation*}
P_{\text {rev }}=2 \cdot I_{\text {rev }} \cdot V_{\text {rev }} \cdot T_{\text {rev }} \cdot f_{s}=0.54 \mathrm{~W} \tag{43}
\end{equation*}
$$

Considering that reverse conduction occurs only for the high end of the voltage range across the half-bridge, the value obtained from (43) represents a pessimistic case that assumes that reverse conduction occurs across the entirety of the linecycle, with the same reverse current. Accordingly, the actual contribution of the reverse conduction loss to the total power loss is of less concern.
For achieving the best efficiency across line and load ranges, an adaptive dead-time adjustment circuit can be incorporated [45]. A less-effective but lower-cost method to alleviate that effect is through the incorporation of a larger capacitor $C_{D C}$, which results in reduced ripple across the DC capacitor and half-bridge, see (19).

Fig. 19 shows the input current harmonics distribution at full and half-load operations, where THD figures of $8.6 \%$ and 17.4 $\%$ are measured respectively. Since one of the potential applications for the proposed converter is the rectifier stage in LED drivers, the figure illustrates the harmonics magnitudes against IEC 61000-3-2 standard class-C device limits [1][2],where it is shown that the measured harmonics magnitudes are well-within the limits set by the standard.


Fig. 18. Measured GaN device reverse characteristics across different temperatures for $V_{G S}=0 \mathrm{~V}$.


Fig. 19. Input Current harmonics distribution.


Fig. 20. Thermal image for converter at full-load.
Fig. 20 shows a thermal photograph for the prototype under full-load operation, where the inductor windings are the hottest element in the circuit, with a maximum temperature of $84.5^{\circ} \mathrm{C}$ (with airflow).

Table V shows a comparison of the proposed work with several reported solutions for the PFC front-end in single-phase offline converters for low-power applications. While the majority of the reported converters operate at low frequencies to limit the switching losses, the proposed converter operates at 1 MHz with soft switching. The proposed converter also has the
potential for operation at higher frequencies, as all of the circuit components scale with frequency (other than the DC energystorage capacitor size, which is dictated by the $50 / 60 \mathrm{~Hz}$ standard line frequency). In addition, different PFC control techniques are employed in the reported solutions, while the proposed converter achieves PFC inherently, where the circuit overhead is only an extra diode and a capacitor. That simplifies the design and provides freedom from the limited frequency range for available PFC controllers, which is another factor allowing for high-frequency operation. The output-voltage control can be achieved with switching frequency modulation and/or burst-mode operation, depending on the requirements of the following DC-DC stage, where results has shown that high power factor and low THD are achieved across the load range.

Similar to most of the reported solutions, the proposed structure is compatible with universal input mains, as the charge pump circuit is able to achieve inherent PFC regulation, regardless of the input voltage, where the analysis and principle of operation of the pump circuit is the same across any input voltage that can range between $85-265 \mathrm{~V}_{\text {rms. }}$. However, in order to achieve the same output power across both ends of the input voltage range, two aspects need to be taken into consideration. First, the resonant tank needs to be designed for the worst-case conditions, with respect to the input rms voltage and output power. More specifically, the resonant tank inductor needs to be designed to handle the worst-case current, which comes with the minimum input rms voltage and maximum output power, as can be seen from (27). Second, in order to satisfy the first condition for obtaining high power factor, given in section IIIA, which entitles the class-DE stage to operate near resonance with a near-unity gain, the output voltage will change across the range of the input rms voltage. That in turn will require the following DC-DC stage to have a wide-input line regulation capability. Fig. 21 shows a scope capture for the implemented prototype line-frequency waveforms with $120 \mathrm{~V}_{\text {rms }}$ input, delivering an output power of 12.8 W , a power factor of 0.99 , and a THD of $9.1 \%$ for an average output voltage of 179 V with 20 V low-frequency ripple. Fig. 22 shows the input current harmonics magnitudes for 120 and $230 \mathrm{~V}_{\mathrm{rms}}$ inputs. The figures show that high power factor and low THD are achieved with different input voltages, as the charge pump circuit works in the same manner. Yet, to achieve the full-load operation for the low

TABLE V. COMPARISON WITH REPORTED LITERATURE.

| Reference | [4] | [5] | [8] | [10] | [11] | [12] | [13] | This Work |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Year | 2011 | 2013 | 2016 | 2013 | 2017 | 2011 | 2016 | 2019 |
| Topology | Buck | Buck | Boost | Buck-Boost | Flyback | SEPIC | SEPIC | Resonant |
| Aux. Circuits | None | $\begin{gathered} \text { Switch and } 2 \\ \text { diodes } \end{gathered}$ | None | None | None | None | None | Capacitor and diode |
| Mains Compatibility | Universal | Universal | Universal | Universal | Universal | $100 \mathrm{~V}_{\text {rms }}$ | $220 \mathrm{~V}_{\text {rms }}$ | Universal |
| Output Power [W] | 100 | 100 | 150 | 12 | 60 | 65 | 21 | 50 |
| Output voltage [V] | 90 | 80 | $250 / 450$ | 112 / 350 | 24 | 48 | 30 | 300 |
| Power Factor | 0.98 | 0.96 | --- | 0.98 | 0.99 | --- | 0.99 | 0.99 |
| THD [\%] | --- | 18 | 5 | 8.7 | 8 | 1.6 | 12.6 | 8.6 |
| Efficiency [\%] | 96.5 | 95.5 | 95 | 88 | 90.8 | 92.8 | 91.6 | 88 |
| Semiconductors (switches) | Si | Si | Si | Si | Si | Si | Si | GaN |
| Semiconductors (diodes) | Si | Si | SiC | Si | Si | Si | Si | SiC |
| Switching freq. [kHz] | 25-425 | --- | 125-1000 | 65 | 45-300 | 50 | 50 | 1000 |
| PFC Control | Constant ON-time | $\begin{aligned} & \text { Constant ON- } \\ & \text { time } \\ & \hline \end{aligned}$ | PWM / PFM | PWM | $\begin{aligned} & \text { Variable ON- } \\ & \text { time } \end{aligned}$ | PWM | PWM | Inherent |
| Output Voltage Control | Constant ON-time | $\begin{gathered} \text { Constant ON- } \\ \text { time } \end{gathered}$ | PWM / PFM | PWM | $\begin{gathered} \text { Variable ON- } \\ \text { time } \\ \hline \end{gathered}$ | PWM | PWM | PFM |

line voltage, the resonant tank needs to be redesigned for the high current that will result from (27), while the current prototype was designed for the $230 \mathrm{~V}_{\mathrm{rms}}$ mains input as given in the design specifications in Table I.

Even though the inherently achieved power factor and THD figures fall within the reported ranges, it is noted that the proposed solution has lower efficiency compared to several reported ones. This comes from two main factors. The first being the added stress on the resonant-tank, as the pump circuit operation entitles the resonant tank to store the energy from the input line as well as the energy to the load every switching cycle, which is the main reason for the current peaking effect analyzed in section III-E and evaluated by (27). With the employed high-frequency magnetic material for the given operation frequency range, the core losses scale with ~ $f_{s}^{2.5} \cdot I_{\text {RES }}{ }^{2.34}[39]$, while the winding losses scale with $\sim f_{s} \cdot I_{\text {RES }}{ }^{2}$. Accordingly, in addition to the high frequency design, the current stress in the resonant tank results in high losses in the resonant inductor. A way to alleviate that effect is through the incorporation of a larger core or a better-suited magnetic material. The second factor is the partial soft switching of the converter with the implemented fixed dead time, which can be alleviated through the incorporation of an adaptive dead-time adjustment technique and/or a larger energy-storage capacitor $C_{D C}$. On the other hand, a lower frequency design would mitigate both effects while sacrificing the power density. These factors together constitute a trade-off between efficiency, power density and power quality (power factor and THD).


Fig. 21. Line-frequency waveforms for $120 \mathrm{~V}_{\mathrm{rms}}$ input ( $V_{I N} 50 \mathrm{~V} /$ div, $I_{I N} 100$ $\mathrm{mA} / \mathrm{div}$, $V_{\text {OUT }} 50 \mathrm{~V} /$ div with $5 \mathrm{~ms} /$ div).


Fig. 22. Input current harmonics distribution for different line voltages against the standard.

It is worth mentioning that while the proposed architecture is tested and implemented with a series-resonant tank, the chargepump circuit is functional with other arrangements for the resonant tank, including the parallel-resonant, LLC, and LCC circuits. In addition, resonant converters allow for galvanic isolation through the addition of a high-frequency transformer to the resonant tank. These features allow for different output voltages that can be higher or lower than the input voltage, which gives additional flexibility for the following DC-DC stage design based on the application and system requirements.

## VI. Conclusion

The analysis and design flow of a charge-pump-based resonant PFC rectifier for low-power single-phase offline converters is presented. The system incorporates an input bridge, a charge-pump circuit, a DC energy-storage capacitor, and a class-DE resonant converter. Although the circuit is subject for additional stresses from the incorporation of the charge pump circuit, which result in added losses in the resonant tank, the converter achieves PFC functionality inherently. At the same time, the operation is based on soft switching, allowing for increased switching frequencies with reduced switching losses. A prototype is built and tested to validate the presented analysis and design procedure. The prototype achieves up to 50 W of power, with a power factor of 0.99 , a THD of $8.6 \%$, and an efficiency of up to $88 \%$, with harmonic magnitudes well-within the IEC 61000-3-2 standard class-C device limits, making it suitable for use as the rectifier stage in LED drivers.

## References

[1] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[2] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[3] L. Huber, L. Gang and M. M. Jovanovic, "Design-Oriented Analysis and Performance Evaluation of Buck PFC Front End," in IEEE Transactions on Power Electronics, vol. 25, no. 1, pp. 85-94, Jan. 2010.
[4] X. Wu, J. Yang, J. Zhang and M. Xu, "Design Considerations of SoftSwitched Buck PFC Converter With Constant On-Time (COT) Control," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 31443152, Nov. 2011.
[5] X. Xie, C. Zhao, L. Zheng and S. Liu, "An Improved Buck PFC Converter With High Power Factor," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2277-2284, May 2013.
[6] Y. Ohnuma and J. Itoh, "A Novel Single-Phase Buck PFC AC-DC Converter With Power Decoupling Capability Using an Active Buffer," in IEEE Transactions on Industry Applications, vol. 50, no. 3, pp. 19051914, May-June 2014.
[7] Y. Jang and M. M. Jovanovic, "A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization," in IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 85-93, Jan. 2009.
[8] R. Fernandes and O. Trescases, "A Multimode 1-MHz PFC Front End With Digital Peak Current Modulation," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5694-5708, Aug. 2016.
[9] M. A. Al-Saffar, E. H. Ismail and A. J. Sabzali, "Integrated Buck-BoostQuadratic Buck PFC Rectifier for Universal Input Applications," in IEEE Transactions on Power Electronics, vol. 24, no. 12, pp. 2886-2896, Dec. 2009.
[10] Y. Li and C. Chen, "A Novel Primary-Side Regulation Scheme for SingleStage High-Power-Factor AC-DC LED Driving Circuit," in IEEE Transactions on Industrial Electronics, vol. 60, no. 11, pp. 4978-4986, Nov. 2013.
[11] C. Zhao, J. Zhang and X. Wu, "An Improved Variable On-Time Control Strategy for a CRM Flyback PFC Converter," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 915-919, Feb. 2017.
[12] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," in IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 873-881, March-April 2011.
[13] B. Poorali and E. Adib, "Analysis of the Integrated SEPIC-Flyback Converter as a Single-Stage Single-Switch Power-Factor-Correction LED Driver," in IEEE Transactions on Industrial Electronics, vol. 63, no. 6, pp. 3562-3570, June 2016.
[14] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd edition. Wiley-IEEE Press, 2011.
[15] D. J. Perreault et al., "Opportunities and Challenges in Very High Frequency Power Conversion," 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, 2009, pp. 1-14.
[16] A. Knott, T. M. Andersen, P. Kamby, M. P. Madsen, M. Kovacevic and M. A. E. Andersen, "On the ongoing evolution of very high frequency power supplies," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2013, pp. 2514-2519.
[17] A. Knott et al., "Evolution of Very High Frequency Power Supplies," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sept. 2014.
[18] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," 2006 37th IEEE Power Electronics Specialists Conference, Jeju, 2006, pp. 1-11.
[19] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson and D. J. Perreault, "Very High Frequency Resonant Boost Converters," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, 2007, pp. 2718-2724.
[20] M. P. Madsen, A. Knott and M. A. E. Andersen, "Very high frequency resonant DC/DC converters for LED lighting," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2013, pp. 835-839.
[21] J. M. Rivas, R. S. Wahby, J. S. Shafran and D. J. Perreault, "New Architectures for Radio-Frequency DC-DC Power Conversion," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 380-393, March 2006.
[22] M. P. Madsen, A. Knott and M. A. E. Andersen, "Very high frequency half bridge DC/DC converter," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 1409-1414.
[23] Y. Nour, A. Knott and L. P. Petersen, "High frequency soft switching half bridge series-resonant DC-DC converter utilizing gallium nitride FETs," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, 2017, pp. P.1-P.7.
[24] X. Gao, H. Wu and Y. Xing, "A Multioutput LLC Resonant Converter With Semi-Active Rectifiers," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1819-1827, Dec. 2017.
[25] M. Noah et al., "A Current Sharing Method Utilizing Single Balancing Transformer for a Multiphase LLC Resonant Converter With Integrated Magnetics," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 977-992, June 2018
[26] T. Mishima, "A Time-Sharing Current-Fed ZCS High Frequency Inverter-Based Resonant DC-DC Converter with Si-IGBT / SiC-SBD Hybrid Module for Inductive Power Transfer Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[27] M. Vasić, D. Serrano, V. Toral, P. Alou, J. A. Oliver and J. A. Cobos, "Ultraefficient Voltage Doubler Based on a GaN Resonant SwitchedCapacitor Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 622-635, June 2019.
[28] Y. Wang, H. Song and D. Xu, "Soft-Switching Bidirectional DC/DC Converter With an LCLC Resonant Circuit," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 851-864, June 2019.
[29] X. Zhao, C. Chen, J. Lai and O. Yu, "Circuit Design Considerations for Reducing Parasitic Effects on GaN-Based 1-MHz High-Power-Density High-Step-Up/Down Isolated Resonant Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 695-705, June 2019.
[30] H. Ma, Y. Li, Q. Chen, L. Zhang and J. Xu, "A Single-Stage Integrated Boost-LLC AC-DC Converter With Quasi-Constant Bus Voltage for Multichannel LED Street-Lighting Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1143-1153, Sept. 2018.
[31] R. Elferich, "ZVS modelling of the LLC converter operating as unity power factor front end," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, 2018, pp. 1-7.
[32] A. J. Hanson and D. J. Perreault, "A high frequency power factor correction converter with soft switching," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2027-2034.
[33] H. Valipour, M. Mahdavi and M. Ordonez, "Resonant Bridgeless AC/DC Rectifier with High Switching Frequency and Inherent PFC Capability," in IEEE Transactions on Power Electronics.
[34] G. Li, J. Xia, K. Wang, Y. Deng, X. He and Y. Wang, "A Single-Stage Interleaved Resonant Bridgeless Boost Rectifier with High-Frequency Isolation," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[35] S. Mangkalajan, C. Ekkaravarodome, K. Jirasereeamornkul, P. Thounthong, K. Higuchi and M. K. Kazimierczuk, "A Single-Stage LED Driver Based on ZCDS Class-E Current-Driven Rectifier as a PFC for Street-Lighting Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8710-8727, Oct. 2018.
[36] W. Chen, F. C. Lee and T. Yamauchi, "An improved "charge pump" electronic ballast with low THD and low crest factor," in IEEE Transactions on Power Electronics, vol. 12, no. 5, pp. 867-875, Sept. 1997.
[37] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," 2019 IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, 2019.
[38] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, $2^{\text {nd }}$ edition. Kluwer Academic Publishers, 2001.
[39] Ferroxcube material datasheet https://www.ferroxcube.com/upload/media/design/FXCStainmetzCoeffi cients.xls.
[40] Micrometals material datasheet https://micrometalsarnoldpowdercores.com/pdf/mix/Mix-6DataSheet.pdf.
[41] A. Hopkins, N. McNeill, P. Anthony and P. Mellor, "Figure of merit for selecting super-junction MOSFETs in high efficiency voltage source converters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 3788-3793.
[42] Y. Nour, Z. Ouyang, A. Knott and I. H. H. Jørgensen, "Design and implementation of high frequency buck converter using multi-layer PCB inductor," IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1313-1317.
[43] F. Udrea, G. Deboy and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 713-727, March 2017.
[44] G. Deboy, O. Haeberlen and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 89-100, 2017.
[45] M. Ekhtiari, T. Andersen, M. A. E. Andersen and Z. Zhang, "Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 783-793, Jan. 2017.

## Appendix [J4]

F. M. Spliid, A. M. Ammar, Y. Nour, and A. Knott, "A Series-Resonant Charge-Pump-Based Power Factor Correction Port for Single-Phase Mains Rectification," under revision in IEEE Journal of Emerging and Selected Topics in Power Electronics.

# A Series-Resonant Charge-Pump-Based Power Factor Correction Port for Single-Phase Mains Rectification 

Frederik M. Spliid, Student Member, IEEE, Ahmed M. Ammar, Student Member, IEEE, Yasser Nour, Senior Member, IEEE, and

Arnold Knott

Corresponding author: Frederik M. Spliid<br>Elektrovej 325, room 254<br>2800 Kongens Lyngby, Denmark<br>Phone: +45 40515418<br>E-mail: frmsp@elektro.dtu.dk


#### Abstract

In electronic applications supplied from the AC mains, the power factor and harmonic content of the input currents is bound by international standards, and power factor correction (PFC) converters are often needed in order to comply with these standards. State-of-the-art AC-DC converters are based on a cascaded architecture, requiring the power factor correction (PFC) stage to process both the active power delivered to the load as well as the reactive power required to maintain a high power factor. This paper presents the concept of a power factor port connected in parallel with the load rather than the cascaded connection. Through this architecture, the stresses and losses in the PFC converter are reduced as it only needs to supply the reactive power required for power factor correction, and not the active power for the load itself. A converter is designed as a modified class-DE series-resonant converter and achieves partial soft-switching, allowing it to be operated at high switching frequencies. A $50-\mathrm{W}$ prototype for European mains is implemented and shown to achieve a power factor of 0.99 , input harmonic magnitudes well below the limits of the IEC 61000-3-2 standard, and an efficiency of up to $92.2 \%$, an 8 pp efficiency improvement compared to similar converters in cascaded connection.


## Index Terms

AC-DC power conversion, power factor correction, resonant converters, charge pump

[^4]
## I. Introduction

In the pursuit of increasing power density, the recent years have seen a significant research interest in the field of resonant power converters [1], with switching frequencies taken into the high-frequency (HF, 3-30 MHz) or even very-high-frequency (VHF, 30-300 MHz) ranges [2]-[6]. Under ideal operation, resonant converter topologies have the benefit of being able to achieve zero voltage switching (ZVS) [7]. This mostly eliminates the switching losses in active components and allows the converter to be operated at higher frequencies than otherwise possible. Increased switching frequencies come with many benefits, including reduced size and cost of passive energy storage and filter components [8], [9]. With the emergence of wide bandgap technologies such as Gallium Nitride (GaN) transistors, this development is further enabled by the improved figures of merit of new switching devices [10], [11], and previous publications have demonstrated active-driven GaN-based switch-mode converters operating at switching frequencies of 10 MHz [12], [13] and even 100 MHz [14].

Popular resonant converter topologies include the Class-E [15], [16], Class-DE [17], [18] and Class- $\Phi_{2}$ converters [19]. While the Class-E topology has the benefit of employing only a single low-side switching component, the Class-DE topology has the benefit of greatly reduced voltage stresses and the Class- $\Phi_{2}$ topology combines the use of a single low-side switch with a moderate voltage stress at the cost of higher complexity and component count. One application where the demand for compact power converters is rising is in the field of solid-state lighting, where power electronic drivers are needed to convert an AC mains input voltage into a low-ripple DC output current for a load consisting of light-emitting diodes (LEDs). For power levels above 25 W , these converters need to provide power factor correction (PFC) according to international standards [20], [21], which requires active rectification of the AC input voltage. This type of driver is often implemented with a two-stage architecture as shown in Fig. 1 , where the first stage provides power factor correction of the input current, while the second stage is a DC-DC converter responsible for converting the intermediate bus voltage into the DC level required for the load, while removing the double-line-frequency $100 / 120 \mathrm{~Hz}$ voltage ripple.

While resonant converters have successfully been put to use as DC-DC converters applicable as the second stage in this architecture, their use as power factor correctional converters are limited at this point. A reason for this is that while resonant converters can be very efficient under the right operating conditions, they are very sensitive to load changes [22], [23], as their rectifier stages have a highly non-linear input-impedance. Several methods have been demonstrated to compensate for these non-linearities in order to ensure a wider range of operation for Class-E


Fig. 1: Traditional two-stage cascaded PFC AC/DC converter.


Fig. 2: Proposed parallel PFC stage architecture.
[24]-[27], Class-DE [28], and LLC resonant topologies [29]. In order to operate as a power factor correctional stage, a converter must draw an input current proportional to the input voltage over the full line cycle, and soft switching PFC converters with both resonant and non-resonant converter topologies have been demonstrated in literature [30]-[37].

The work presented in [30], [31] demonstrates a modified Class-DE resonant converter driving a power factor correcting charge-pump circuit from a 230 V AC input voltage. The converter introduced in this paper is an enhanced configuration based on this previous work, which achieves higher efficiency and lower total harmonic distortion (THD) by modifying the power flow and reducing the stresses on the resonant converter. Whereas the previously presented work is implemented as a traditional cascaded AC-DC converter with the resonant converter supplying the load directly, the proposed design in this work utilizes a parallel architecture. Fig. 2 shows the proposed architecture, where the resonant converter acts as a power factor port, driving only the charge-pump circuit, while the load or second converter stage is connected in parallel with this resonant converter. A prototype is constructed and used to demonstrate the PFC operation of the topology. The specifications of the prototype converter is given in Table I.

## II. Topology

The proposed converter is designed as a modified class DE converter, with a class D inverter half bridge connected to a class DE rectifier [17], [38] through a resonant tank. The class D/DE topology is chosen as it has the benefit of reduced voltage stresses on the switching components, compared to other resonant converter topologies. The class DE rectifier circuit has been equipped with an additional diode bridge and a charge pump capacitor which ensures power factor correction operation of the converter. A schematic of the full converter is shown in Fig. 3.

| Input voltage | $230 \mathrm{~V}_{\mathrm{AC}}$ |
| :---: | :---: |
| Output voltage | $400 \mathrm{~V}_{\mathrm{DC}}$ |
| Output power | 50 W |

TABLE I: Prototype specifications


Fig. 3: Schematic of full converter.

Previous literature [18], [39] have presented throughout analyses of the traditional class-DE rectifier circuit, but as the addition of the charge-pump capacitor changes the behavior of the circuit, an analysis of the modified topology is performed.

## A. Charge pump

The basic operation of the charge pump circuit is illustrated in Fig. 4. As the converter switches at a frequency significantly faster than the AC input voltage, $V_{\text {in }}$ and $V_{\text {rect }}$ are assumed constant over a switching cycle. During intervals $1 \mathrm{a}, 1 \mathrm{~b}, 3 \mathrm{a}$ and 3 b , the charge pump capacitor $C_{p}$ is discharged and charged respectively through the resonant tank of the converter. In intervals $1 \mathrm{~b}, 2,3 \mathrm{~b}$ and 4 , energy is transferred from the resonant tank to the load. When the charge pump capacitor is fully charged, at the boundary between intervals 3 b and 4 , the voltage at node $V_{r}$ is zero and the charge pump voltage $V_{p}$ is equal to the rectified input voltage $V_{\text {rect }}$. Ignoring any losses in the input filter and diode bridge, this voltage is equal to the absolute value of the input voltage $V_{i n}$. By the end of interval 1 b , the capacitor is discharged to zero volts, with diodes $D_{2}$ and $D_{4}$ preventing discharging to negative voltage.

Since the capacitor is charged and discharged every switching cycle, the amount of charge passing through diode $D_{1}$ every cycle is

$$
\begin{equation*}
Q_{D 1}=C_{p} \cdot V_{p, \max }=C_{p} \cdot\left|V_{i n}\right| \tag{1}
\end{equation*}
$$

Ignoring any leakage currents in the input filter and diode bridge, this is the net charge drawn from the input every cycle. This gives an input current of

$$
\begin{equation*}
I_{i n}=Q_{D 1} \cdot f_{s w}=f_{s w} \cdot C_{p} \cdot V_{i n} \tag{2}
\end{equation*}
$$

Equation (2) indicates that the average input current over a switching cycle is proportional to the instantaneous input voltage of the converter, and this is the case for any value of $V_{i n}$, assuming that the switching frequency is constant over the AC line cycle and that the current in the resonant tank is sufficient to completely charge and


Fig. 4: Charge pump operation.
discharge $C_{p}$ in every switching cycle. With the input current being proportional to the input voltage over the full line cycle a high power factor is achieved.

Using (2), the relationship between $C_{p}, f_{s w}$ and the input power can be derived.

$$
\begin{equation*}
P_{i n}=I_{i n} \cdot V_{i n}=f_{s w} \cdot C_{p} \cdot V_{i n}^{2} \tag{3}
\end{equation*}
$$

This means that the input power (and output power, assuming constant efficiency) of the converter scales linearly with the switching frequency, allowing control of the output power through frequency modulation.

## B. Rectifier

The schematic of the modified rectifier circuit with the charge-pump circuit is shown in Fig. 5. The circuit consists of four diodes, $D_{1-4}$ and a capacitor $C_{p}$. As the system is assumed to be dominated by the capacitance of $C_{p}$, any parasitic shunt capacitance of the diodes are ignored for the purpose of this analysis.


Fig. 5: Schematic of modified class-DE rectifier with charge-pump circuitry.

The rectifier is supplied by a current $i_{\text {res }}$, which is assumed to be an ideal sine wave with frequency $\omega_{s w}$ and amplitude $I_{r}$.

$$
\begin{equation*}
i_{r e s}=I_{r} \cdot \sin \left(\omega_{s w} t\right) \tag{4}
\end{equation*}
$$

The operation of the rectifier can be characterized by the 4 states shown in Table II, with each diode conducting in one state. The duty cycle $D_{r}$ denotes the fraction of the the switching cycle, $T_{s w}$, in which diodes $D_{3}$ or $D_{4}$ are conducting. The voltage at node $V_{b}$ is equal to either $V_{b u s}$ or $V_{\text {rect }}$, depending on the instantaneous direction of current $i_{\text {res }}$

During state 1 , current is flowing through the charge pump capacitor, $C_{p}$, and diode $D_{2}$, discharging the capacitor and raising the voltage $V_{r}$ until it reaches the level of $V_{\text {bus }}$ and the capacitor is fully discharged. At this point in time, the rectifier enters state 2 and diode $D_{4}$ starts conducting, while no current flows in the capacitor. When the direction of the resonant current changes, the diode $D_{4}$ blocks the current and the circuit enters state 3 , where current flows through diode $D_{1}$, charging the capacitor and decreasing the voltage $V_{r}$. When $V_{r}$ is reduced to 0 V , and the voltage $V_{p}$ is equal to the rectified input voltage $V_{\text {rect }}$, the capacitor stops charging and current flows through $D_{3}$ in state 4 . Once the current changes its direction again, the circuits reverts to state 1 .

| State | Conducting diode | $V_{b}$ | $i_{C p}$ | Time |
| :---: | :---: | :---: | :---: | :---: |
| 1 | $D_{2}$ | $V_{b u s}$ | $-I_{r} \cdot \sin \left(\omega_{s w} t\right)$ | $0<t \leq T_{s w} \cdot\left(0.5-D_{r}\right)$ |
| 2 | $D_{4}$ | $V_{\text {bus }}$ | 0 | $T_{s w} \cdot\left(0.5-D_{r}\right)<t \leq T_{s w} \cdot 0.5$ |
| 3 | $D_{1}$ | $V_{\text {rect }}$ | $-I_{r} \cdot \sin \left(\omega_{s w} t\right)$ | $T_{s w} \cdot 0.5<t \leq T_{s w} \cdot\left(1-D_{r}\right)$ |
| 4 | $D_{3}$ | $V_{\text {rect }}$ | 0 | $T_{s w} \cdot\left(1-D_{r}\right)<t \leq T_{s w}$ |

TABLE II: States of modified class DE rectifier.

This means that the current through the charge pump capacitor over a full cycle can be described as

$$
i_{C p}(t)=\left\{\begin{array}{cc}
-I_{r} \cdot \sin \left(\omega_{s w} t\right) & \text { for state } 1  \tag{5}\\
0 & \text { for state } 2 \\
-I_{r} \cdot \sin \left(\omega_{s w} t\right) & \text { for state } 3 \\
0 & \text { for state } 4
\end{array}\right.
$$

At the start of each cycle the charge pump voltage $V_{p}$ is charged to $V_{\text {rect }}$. Over a cycle, the voltage is

$$
V_{p}(t)=V_{r e c t}+\frac{1}{C_{p}} \int_{0}^{t} i_{C p} d t=\left\{\begin{array}{cl}
V_{r e c t}-\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(1-\cos \left(\omega_{s w} t\right)\right) & \text { for state } 1  \tag{6}\\
0 & \text { for state } 2 \\
\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(\cos \left(\omega_{s w} t\right)+1\right) & \text { for state } 3 \\
V_{\text {rect }} & \text { for state } 4
\end{array}\right.
$$

Knowing that the voltage across the capacitor must be continuous across the transitions between the states, a relationship between current amplitude $I_{r}$ and diode duty cycle $D_{r}$ can be derived:

$$
\begin{gather*}
V_{p}\left(T_{s w} \cdot\left(0.5-D_{r}\right)\right)=0 \Leftrightarrow  \tag{7}\\
V_{r e c t}-\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(1+\cos \left(2 \pi D_{r}\right)\right)=0 \tag{8}
\end{gather*}
$$

By rearranging and isolating for $D_{r}$ we get

$$
\begin{gather*}
\cos \left(2 \pi D_{r}\right)=\frac{V_{\text {rect }} \omega_{s w} C_{p}}{I_{r}}-1  \tag{9}\\
D_{r}=\frac{1}{2 \pi} \cos ^{-1}\left(\frac{V_{\text {rect }} \omega_{s w} C_{p}}{I_{r}}-1\right) \tag{10}
\end{gather*}
$$

Using (9), the charge pump voltage can now be expressed as

$$
V_{p}(t)=\left\{\begin{array}{cc}
V_{r e c t} \frac{\cos \left(2 \pi D_{r}\right)+\cos \left(\omega_{s w} t\right)}{\cos \left(2 \pi D_{r}\right)+1} & \text { for state } 1  \tag{11}\\
0 & \text { for state } 2 \\
V_{\text {rect }} \frac{1+\cos \left(\omega_{s w} t\right)}{1+\cos \left(2 \pi D_{r}\right)} & \text { for state } 3 \\
V_{\text {rect }} & \text { for state } 4
\end{array}\right.
$$

The voltage at the input of the rectifier, $V_{r}$ is calculated as $V_{r}=V_{b}-V_{p}$, and $V_{b}$ is equal to $V_{b u s}$ and $V_{\text {rect }}$ for the positive and negative half-cycles of $i_{\text {res }}$ respectively, this gives the following expression for $V_{r}$.

$$
V_{r}(t)=\left\{\begin{array}{cc}
V_{\text {bus }}-V_{\text {rect }} \frac{\cos \left(2 \pi D_{r}\right)+\cos \left(\omega_{s w} t\right)}{\cos \left(2 \pi D_{r}\right)+1} & \text { for state } 1  \tag{12}\\
V_{\text {bus }} & \text { for state } 2 \\
V_{\text {rect }} \frac{\cos \left(2 \pi D_{r}\right)-\cos \left(\omega_{s w} t\right)}{\cos \left(2 \pi D_{r}\right)+1} & \text { for state } 3 \\
0 & \text { for state } 4
\end{array}\right.
$$

A set of waveforms for the rectifier is shown in Fig. 6. From (10), it is seen that an increase in resonant current amplitude will result in faster charging and discharging of $C_{p}$ and an increased duty cycle for diodes $D_{3}$ and $D_{4}$. As charging and discharging of $C_{p}$ is the only part of the operation that transfers power from the input to output of the converter, any current in diodes $D_{4}$ and $D_{3}$ is just energy being cycled in the converter causing extra power loss. However, these diodes are necessary in order to limit the voltage swing of $V_{r}$ for large resonant currents. This


Fig. 6: Waveforms of $V_{p}, V_{r}$ and $V_{b}$ for $V_{\text {rect }}=325 \mathrm{~V}$ and $V_{b u s}=400 \mathrm{~V}$. Solid lines for optimal operation with $I_{r}=I_{r, \text { ideal }}$, dashed lines for suboptimal case with $I_{r}=\frac{4}{3} \cdot I_{r, \text { ideal }}$.
means that the ideal amplitude of resonant current $i_{\text {res }}$ is the one that is sufficient to fully charge and discharge $C_{p}$ over a switching cycle, while causing zero conduction in diodes $D_{3}$ and $D_{4}$. This amplitude is calculated by rewriting (9):

$$
\begin{gather*}
I_{r}=\frac{V_{\text {rect } t} \omega_{s w} C_{p}}{1+\cos \left(2 \pi D_{r}\right)} \Leftrightarrow  \tag{13}\\
I_{r, \text { ideal }}=\frac{V_{\text {rect }} \omega_{s w} C_{p}}{1+\cos (2 \pi \cdot 0)}=\frac{V_{\text {rect }} \omega_{s w} C_{p}}{2} \tag{14}
\end{gather*}
$$

With the expression from (13), $V_{\text {rect }}$ can be expressed in terms of $I_{r}$ :

$$
\begin{equation*}
V_{r e c t}=\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(1+\cos \left(2 \pi D_{r}\right)\right) \tag{15}
\end{equation*}
$$

With the expression from (15), the waveform for $V_{r}$ can be rewritten as a function of current amplitude:

$$
V_{r}(t)=\left\{\begin{array}{cl}
V_{b u s}-\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(\cos \left(2 \pi D_{r}\right)+\cos \left(\omega_{s w} t\right)\right) & \text { for state } 1  \tag{16}\\
V_{b u s} & \text { for state } 2 \\
\frac{I_{r}}{\omega_{s w} C_{p}} \cdot\left(\cos \left(2 \pi D_{r}\right)-\cos \left(\omega_{s w} t\right)\right) & \text { for state } 3 \\
0 & \text { for state } 4
\end{array}\right.
$$

Using Fourier analysis, the voltage waveform is separated into in-phase and quadrature components relative to the current in order to determine the equivalent input impedance of the rectifier at the switching frequency.

$$
\begin{gather*}
V_{r, i}=2 f_{s w} \cdot \int_{0}^{T_{s w}} V_{r}(t) \cdot \sin \left(\omega_{s w} t\right) d t=V_{b u s} \cdot \frac{2}{\pi}-2 f_{s w} C_{p} \frac{V r e c t}{}{ }^{2}  \tag{17}\\
I_{r}  \tag{18}\\
V_{r, q}=2 f_{s w} \cdot \int_{0}^{T_{s w}} V_{r}(t) \cdot \cos \left(\omega_{s w} t\right) d t=\sin \left(2 \pi D_{r}\right)\left(\frac{1}{\pi} \frac{I_{r}}{\omega_{s w} C_{p}}-\frac{1}{\pi} V_{r e c t}\right)+\frac{I_{r}}{\omega_{s w} C_{p}}\left(2 D_{r}-1\right)
\end{gather*}
$$

The input impedance of the rectifier at the switching frequency can be modelled as a resistor in series with a capacitor. The two components are calculated from the two voltage components.

$$
\begin{equation*}
R_{\text {rect }}=\frac{V_{r, i}}{I_{r}}=\frac{2}{\pi} \cdot \frac{V_{b u s}}{I_{r}}-2 f_{s w} C_{p}\left(\frac{V_{\text {rect }}}{I_{r}}\right)^{2} \tag{19}
\end{equation*}
$$



Fig. 7: Equivalent input capacitance and resistance of rectifier for $V_{\text {rect }}=325 \mathrm{~V}$ and $V_{\text {bus }}=400 \mathrm{~V}$

$$
\begin{equation*}
C_{r e c t}=-\frac{I_{r}}{\omega_{s w} V_{r, q}}=\frac{\pi C_{p}}{\sin \left(2 \pi D_{r}\right) \cdot\left(\frac{V_{r e c t}}{I_{r}} \omega_{s w} C_{p}-1\right)+\pi-2 \pi D_{r}} \tag{20}
\end{equation*}
$$

Normalized graphs of the the equivalent input resistance and capacitance of the rectifier at the peak input voltage are shown in Fig. 7. Knowing this input impedance, the resonant tank can be designed to match the impedance between the rectifier and inverter.

The presence of higher harmonics in the resonant current might affect the calculated values for input impedance, but the basics of the operation are still valid. Harmonic content is likely to change the ideal current amplitude, $I_{r, \text { ideal }}$, and some tuning might be required to achieve ideal operation.

## C. Inverter

The inverter circuit consist of a transistor half-bridge driving an AC current through a resonant tank into the rectifier. A schematic of the inverter is shown in Fig. 8. For the purpose of this analysis, the parasitic shunt capacitance of the switching devices are neglected, as the charge pump capacitor is still assumed to dominate the system. Soft switching is achieved through manual tuning of the dead-time between the gate signals for the inverter switches. For improved efficiency, adaptive dead-time techniques [40]-[43] might be applied.

Ignoring the dead-time, the voltage waveform at the switch node $V_{s}$ can be approximated as a square wave with duty cycle $D_{i}$, switching between the bus voltage $V_{\text {bus }}$ and ground. The high side switch $Q_{1}$ is driven with duty cycle $D_{i}$, while the low side is operated with duty cycle $1-D_{i}$.

$$
V_{s}(t)=\left\{\begin{array}{cl}
V_{b u s} & \text { for } 0<t \leq D_{i} T_{s w}  \tag{21}\\
0 & \text { for } T_{s w}<t \leq T_{s w}
\end{array}\right.
$$



Fig. 8: Schematic of class D inverter with load

By modulating the duty cycle $D_{i}$, the fundamental amplitude of the switch-node voltage can be changed. An expression for the fundamental amplitude as a function of duty cycle is derived using Fourier analysis.

$$
\begin{gather*}
V_{s, \text { fund }}=2 f_{s w} \sqrt{\left(\int_{0}^{T} V_{s}(t) \sin \left(\omega_{s w} t\right)\right)^{2}+\left(\int_{0}^{T} V_{s}(t) \cos \left(\omega_{s w} t\right)\right)^{2}} \Leftrightarrow  \tag{22}\\
V_{s, \text { fund }}=V_{\text {bus }} \frac{\sqrt{2}}{\pi} \sqrt{1-\cos \left(2 \pi D_{i}\right)} \tag{23}
\end{gather*}
$$

The normalized fundamental amplitude of the switch node voltage vs. duty cycle $D_{i}$ is shown in Fig. 9. The voltage needed at the switch node is found by multiplying the current amplitude by the combined impedance of the rectifier and the resonant tank. The minimum applicable duty cycle is the one that results in the ideal current amplitude, and any value between this and $50 \%$ will work. For duty cycles above $50 \%$, the fundamental amplitude of $V_{s}$ will start decreasing according to (23).
The total impedance of the resonant tank and the rectifier at the switching frequency is given by the following


Fig. 9: Fundamental amplitude of switch-node voltage (normalized) vs. inverter duty cycle.
expression:

$$
\begin{equation*}
Z_{l o a d}=\sqrt{\left(\omega_{s w} L_{r e s}-\frac{1}{\omega_{s w} C_{r e s}}-\frac{1}{\omega_{s w} C_{r e c t}}\right)^{2}+R_{r e c t}^{2}} \tag{24}
\end{equation*}
$$

And the voltage amplitude at the switch node is:

$$
\begin{equation*}
V_{s, a m p}=I_{r} \cdot Z_{\text {load }} \tag{25}
\end{equation*}
$$

By combining (23) and (25) an expression for determining the duty cycle for the inverter can be written:

$$
\begin{equation*}
D_{i}=\frac{1}{2 \pi} \cos ^{-1}\left(1-\frac{\pi^{2}}{2}\left(\frac{I_{r} Z_{\text {load }}}{V_{b u s}}\right)^{2}\right) \tag{26}
\end{equation*}
$$

Once the resonant tank is designed, it is possible to calculate the required duty cycles at the different levels of $V_{\text {rect }}$.

## III. Implementation

A prototype is designed for the specifications given in Table I. The switching frequency is chosen as 200 kHz , since synchronous half-bridge gate drivers for this frequency and voltage range are easily commercially available.

## A. Rectifier and charge pump

The size of the charge pump capacitor $C_{p}$ is calculated by rearranging (3) and referring it to the output power rather than the input power. A conversion efficiency, $\eta$ of $90 \%$ is assumed at this point.

$$
\begin{equation*}
C_{p}=\frac{P_{\text {in }}}{f_{s w} V_{i n}^{2}}=\frac{P_{\text {out }}}{f_{s w} V_{\text {in }}^{2} \eta}=\frac{50 \mathrm{~W}}{200 \mathrm{kHz} \cdot(230 \mathrm{~V})^{2} \cdot 0.9}=5.4 \mathrm{nF} \tag{27}
\end{equation*}
$$

At the peak input voltage, this gives an ideal resonant current amplitude of

$$
\begin{equation*}
I_{r, \text { ideal }}=\frac{V_{\text {rect }} \omega_{s w} C_{p}}{2}=\frac{325 \mathrm{~V} \cdot 2 \pi \cdot 200 \mathrm{kHz} \cdot 5.4 \mathrm{nF}}{2}=1.1 \mathrm{~A} \tag{28}
\end{equation*}
$$

The diodes in the rectifier circuits need to be able to hande a current larger than this and a reverse voltage larger than the 400 V bus voltage. Furthermore, the diodes need to have a paracitic capacitance that is much smaller than the size of the charge pump capacitor in order for the assumptions made in the topology section to be valid.

The chosen diodes are the GB01SLT06 silicon carbide Schottky diodes from GeneSiC Semiconductor with a voltage rating of 650 V and an effective shunt capacitance of around 20 pF [44].

With a switching frequency of 200 kHz and a charge pump capacitor of 5.4 nF , the equivalent input resistance of the rectifier at ideal current amplitude is calculated at peak input voltage by combining (14) and (19). The input capacitance (20) at this current amplitude is equal to the charge pump capacitor.

$$
\begin{gather*}
R_{\text {rect }, \text { ideal }}=\frac{2}{\pi} \cdot \frac{V_{\text {bus }}}{I_{r, \text { ideal }}}-2 f_{\text {sw }} C_{p}\left(\frac{V_{\text {rect }}}{I_{r, \text { ideal }}}\right)^{2}=\frac{4}{\pi \omega_{\text {sw }} C_{p}} \cdot\left(\frac{V_{\text {bus }}}{V_{\text {rect }}}-1\right)  \tag{29}\\
R_{\text {rect }, \text { ideal }}=\frac{4}{\pi 2 \pi \cdot 200 k H z \cdot 5.4 \mathrm{nF}} \cdot\left(\frac{400 \mathrm{~V}}{325 \mathrm{~V}}-1\right)=43.3 \Omega \tag{30}
\end{gather*}
$$

## B. Resonant tank

In order to design the resonant tank, the input impedance of the rectifier needs to be known. As a starting point, the values at ideal current amplitude are used. According to [7], the current in the resonant tank can be assumed to have a sinusoidal shape if the Q -factor of the resonant inductor relative to the input resistance of the rectifier is larger than 2.5 . However, this is based on the assumption that the inverter is of a class DE topology with symmetric gate signals, where the second harmonic of the switch node voltage is largely suppressed. For the class D inverter, the on-time switching waveform can be asymmetrical, and significant second harmonic content can appear in the waveform. To ensure significant suppression of the second harmonic, the inductor is sized to have a loaded Q-factor of 6 .

$$
\begin{equation*}
L_{\text {res }}=\frac{Q R_{\text {rect }}}{\omega_{s w}}=\frac{6 \cdot 43.3 \Omega}{2 \pi \cdot 200 \mathrm{kHz}}=210 \mu \mathrm{H} \tag{31}
\end{equation*}
$$

The inductor is wound using 66 turns of $20 \times 50 \mu \mathrm{~m}$ Litz wire on an EFD15 core with 3F46 material from Ferroxcube. The ESR at 200 kHz is measured to be $870 \mathrm{~m} \Omega$ with an inductance of $220 \mu \mathrm{H}$. In order to have some design overhead, and consider non-ideal operation, the inductor is designed for a peak current of $1.7 \mathrm{~A}, 50 \%$ larger than the ideal amplitude calculated in (14). Combining the inductance with the input impedance of the rectifier gives an equivalent impedance of:

$$
\begin{equation*}
Z_{e q}=\sqrt{\left(\omega_{s w} \cdot L_{r e s}-\frac{1}{\omega_{s w} C_{p}}\right)^{2}+R_{r e c t}^{2}}=136 \Omega \tag{32}
\end{equation*}
$$

Multiplying by the ideal resonant current amplitude calculated in (28) gives a required switch node voltage amplitude of 150 V or $0.375 \cdot V_{\text {bus }}$, which is within the achievable range seen in Fig. 9. This means that there are no strict requirements on the size of the resonant capacitor $C_{r e s}$, as no decrease in reactive impedance is required, and it is only needed to block the DC voltage between the switch node and the rectifier input. A capacitor of 44 nF is chosen, and the resulting load impedance on the inverter is calculated.

$$
\begin{equation*}
Z_{\text {load }}=\sqrt{\left(\omega_{s w} \cdot L_{r e s}-\frac{1}{\omega_{s w} C_{p}}-\frac{1}{\omega_{s w} C_{r e s}}\right)^{2}+R_{r e c t}^{2}}=119 \Omega \tag{33}
\end{equation*}
$$

Based on the assumed 1.7 A peak current in the inductor, the maximum voltage across the resonant capacitor is calculated. Using a convservative approach, the voltage is calculated as the resulting AC voltage from the current added to a DC voltage equal to $V_{b u s}$.

$$
\begin{equation*}
V_{C, \max }=1.7 \mathrm{~A} \cdot \frac{1}{2 \pi \cdot 200 \mathrm{kHz} \cdot 44 \mathrm{nF}}+400 \mathrm{~V}=430 \mathrm{~V} \tag{34}
\end{equation*}
$$

The resulting resonant frequency of the resonant tank is calculated. The resonant tank will appear inductive above this frequency. As an inductive load is a requirement in order to achieve full or partial soft switching in the inverter bridge, the converter should be operated above this frequency.

$$
\begin{equation*}
f_{\text {res }}=\frac{1}{2 \pi} \frac{1}{\sqrt{C_{r e s} L_{r e s}}}=51.2 \mathrm{kHz} \tag{35}
\end{equation*}
$$

## C. Inverter

The switching devices in the inverter needs to handle the resonant current amplitude and the bus voltage while having a low parasitic shunt capacitance in order to make soft switching more easy to obtain. The chosen devices are the GS-065-004-1-L GaN transistors from GaN Systems [45], with a voltage rating of 650 V , a current rating of 3.5 A and an effective shunt capacitance of around 18 pF . The half bridge is driven by a Si8274 half bridge gate driver from Silicon Labs, and the optimal dead time is found through empirical tuning.

The required inverter duty cycle is calculated using (26) with the ideal resonant current amplitude calculated in (28) and the load impedance found in (33).

$$
\begin{equation*}
D_{i}=\frac{1}{2 \pi} \cdot \cos ^{-1}\left(1-\frac{\pi^{2}}{2}\left(\frac{I_{r, i d e a l} Z_{\text {load }}}{V_{\text {bus }}}\right)^{2}\right)=17.2 \% \tag{36}
\end{equation*}
$$

This duty cycle will ensure sufficient current amplitude at the peak input voltage. And since the load impedance of the rectifier is seen from (19) and (20) to decrease with decreasing input voltage, it should also ensure sufficient current for lower input levels. In a more advanced configuration, the duty cycle could be modulated along the line cycle to ensure more efficient operation, but as a proof of concept, the converter is chosen to operate with a constant on-time for all input levels. A list of all the component values used in the power stage is shown in Table III.

| Component | Value |
| :---: | :---: |
| $D_{1-4}$ | GB01SLT06 |
| $Q_{1-2}$ | GS-065-004-1-L |
| $L_{\text {res }}$ | $220 \mu \mathrm{H}$ |
| $C_{\text {res }}$ | $2 \times 22 \mathrm{nF}$ |
| $C_{p}$ | $2 \times 2.7 \mathrm{nF}$ |
| $C_{\text {bus }}$ | $10 \mu \mathrm{~F}+4 \times 100 \mathrm{nF}$ |
| $C_{\text {rect }}$ | 100 nF |
| Gate driver | Si8274 |

TABLE III: Components in prototype power stage

## D. Control loop

Since the input power (3) of the converter scales proportionally with the switching frequency, the converter can be controlled by modulating this parameter. In order to comply with the IEC 61000-3-2 standard [20], the converter must be capable of performing power factor correction down to a power level of 25 W . When processing less power than this, the output voltage can be controlled by simple hysteresis control.
The minimum switching frequency is calculated:

$$
\begin{equation*}
f_{s w, \min }=\frac{P_{\min }}{C_{p} V_{i n}^{2}}=\frac{25 \mathrm{~W}}{5.4 \mathrm{nF} \cdot(230 \mathrm{~V})^{2}}=87.5 \mathrm{kHz} \tag{37}
\end{equation*}
$$

Since this frequency is higher than the calculated resonance frequency of the resonant tank in (35), the converter should be capable of operating at this point. Using an LTC6990 Voltage-controlled oscillator (VCO) from Analog


Fig. 10: Block diagram of the control loop for PFC operation.

Devices, which is capable of operating in the desired region, a control loop is designed using a PI-controller. In order to maintain a low input current THD, the bandwidth of the control loop must be lower than the double-linefrequency of 100 Hz so that the switching frequency, and power level, is being kept constant through the line cycle. Through simulations it was found that a PI controller with a gain of 0.042 and a time constant of $21 \mu \mathrm{~s}$, resulting in a system bandwidth of 50 Hz is sufficient. A block-level diagram is shown in Fig. 10.

For power levels below 25 W , the converter output voltage is controlled by a hysteresis controller that turns off the power stage when the output voltage reaches 450 V and turns it on again at full power when the voltage drops to 350 V .

## IV. Experimental results

A prototype of the presented converter is built (Fig. 11) and tested in the laboratory. Converter operation is verified at output power levels ranging from $20-50 \mathrm{~W}$ for an AC input voltage of $230 \mathrm{~V}_{\mathrm{RMS}}$ at 50 Hz . The output of the converter is connected to an ITECH IT8812B electronic load set up to behave as a resistor and the output power, efficiency, power factor and input current THD is measured using a N4L PPA 5530 Precision Power Analyzer. Fig. 12 shows a schematic of the experimental setup includng test points.

The power level is adjusted by controlling the resistance of the electronic load. A set of measured high-frequency switching waveforms at the peak input voltage ( 325 V ) and an output power of 50 W is shown in Fig. 13. Fig. 14


Fig. 11: Converter prototype


Fig. 12: Diagram of the measurement setup


Fig. 13: Measured high-frequency waveforms of $V_{r}$ (yellow), $V_{b u s}$ (red), $V_{s}$ (green) and $i_{r e s}$ (blue) at peak input voltage. scaling is $100 \mathrm{~V} / \mathrm{div}$ and $500 \mathrm{~mA} /$ div on the y -axis and $2 \mu \mathrm{~s} / \mathrm{div}$ on the x -axis.
shows low frequency waveforms at 50 W output power. The converter is tuned to start operation at an input level of 50 V and the input current waveform is seen to resemble a sine wave, indicating a high power factor.

The converter efficiency, power factor and input current THD is measured using the connected power analyzer, and the power factor is found to be above 0.99 across the full power range. The results for efficiency and THD are shown in Fig. 15 and are seen to be above $90 \%$ and below $8 \%$ respectively across the full range with more than $92 \%$ efficiency and less than $6 \%$ THD at full power. The results are compared to those from [31], which is a cascaded configuration of the same topology. The presented converter is shown to have a lower THD and higher efficiency across the full range, with up to 8 pp of efficiency increase. A harmonics breakdown comparing the amplitude of individual harmonics at full load to the limits of the IEC 61000-3-2 standard [20] is shown in Fig. 16. The harmonics are seen to be well within the limits.


Fig. 14: Measured waveforms of $V_{i n}$ (green), $V_{\text {bus }}$ (yellow) and $i_{\text {in }}$ (blue) at peak input voltage. scaling is 100 $\mathrm{V} /$ div and $200 \mathrm{~mA} / \mathrm{div}$ on the y -axis and $10 \mathrm{~ms} /$ div on the x -axis.


Fig. 15: Measured efficiency and input current THD vs. Output power. Compared with results from [31].


Fig. 16: Harmonics distribution at full load.

## V. Conclusion

The concept of using a resonant "power factor port" in order to drive a charge-pump power factor correctional converter has been presented, and a prototype has been been constructed and tested to verify the operation. The prototype is capable of processing 50 W of power from a 230 V AC input voltage to a 400 V DC output voltage with a power factor of 0.99 , an efficiency of up to $92 \%$ and a THD of less than $6 \%$ at full load with harmonic amplitudes well within the limits of the IEC 61000-3-2 standard [20]. Through frequency control, the prototype is capable to operate over a wide power range with conversion efficiencies above $90 \%$ making it useful for applications with varying load power. The constructed prototype operates at frequencies of up to 200 kHz , but with its large degree of soft-switching and GaN switching devices with low gate charge, the concept should be feasible at higher frequencies as well, with the most immediate constraint being the need for a half-bridge gate driver capable of switching at these frequencies while having the necessary voltage rating.

## REFERENCES

[1] A. Knott et al., "Evolution of very high frequency power supplies," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sept. 2014.
[2] J. C. Hertel et al., "Integrated Very-High-Frequency Switch Mode Power Supplies: Design Considerations," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 526-538, 2018.
[3] J. M. Rivas et al., "New Archtectures for Radio-Frequency DC-DC Power Conversion," in IEEE Transaction on Power Electronics, vol. 21, no. 2, pp. 380-393, 2006.
[4] D. J. Perrault et al., "Opportunities and Challenges in Very High Frequency Power Conversion," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 1-14.
[5] M. P. Madsen et al., "Low Power Very High Frequency Switch-Mode Power Supply With 50 V Input and 5 V Output," in IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6569-6580, 2014.
[6] M. P. Madsen et al., "Very high frequency half bridge DC/DC converter," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2014, pp. 1409-1414.
[7] M. K. Kazimierczuk and D. Czarkowski, Resonant Power Converters. Wiley, 2011.
[8] M. P. Madsen, "Very High Frequency Switch-Mode Power Supplies," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 2015.
[9] M. Kovacevic, "Advances in Very High Frequency Power Conversion," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 2015.
[10] J. Millán et al., "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, 2014.
[11] G. Zulauf et al., "Considerations for Active Power Device Selection in High- and Very-High-Frequency Power Converters," in Proc. Workshop on Control and Modeling for Power Electronics, 2018.
[12] W. Liang et al., "Low-Mass RF Power Inverter for CubeSat Applications Using 3-D Printed Inductors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 2, pp. 880-890, 2017.
[13] H. Thanh Le et al., "Microfabricated Air-Core Toroidal Inductor in Very High-Frequency Power Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 604-613, 2018.
[14] Y. Zhang et al., "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," in IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7926-7942, 2016.
[15] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," in IEEE Journal of Solid-State Circuits, Vol. 10, no. 3, pp. 168-176, 1975.
[16] M. K. Kazimierczuk, "Analysis of class E zero-voltage-switching rectifier," in IEEE Transactions on Circuits and Systems, Vol. 37, no. 6, pp. 747-755, 1990.
[17] D. C. Hamill, "Class DE inverters and rectifiers for DC-DC conversion," in Proc. IEEE Power Electronics Specialists Conference, 1996.
[18] H. Sekiya et al., "Steady-State Analysis and Design of Class-DE Inverter at Any Duty Ratio," in IEEE Transaction on Power Electronics, vol. 30, no. 7, pp. 3685-3694, 2014.
[19] J. Rivas, "Radio Frequency dc-dc Power Conversion," Doctoral thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, USA, 2006.
[20] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[21] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[22] D. J. Kessler and M. K. Kazimierczuk, "Power losses and efficiency of class-E power amplifier at any duty ratio," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1675-1689, 2004.
[23] F. H. Race, "Effects of circuit variations on the class E tuned power amplifier," in IEEE Journal of Solid-State Circuits, vol. 13, no. 2, pp. 239-247, 1978.
[24] Y. Han et al., "Resistance compression networks for radio-frequency power conversion," in IEEE Transactions on Power Electronics, vol. 22, no. 1, pp. 41-53, 2007.
[25] L. Roslaniec et al., "Design of Single-Switch Inverters for Variable Resistance/Load Modulation Operation," in IEEE Transactions of Power Electronics, vol. 30, no. 6, pp. 3200-3214, 2014.
[26] S. Park and J. Rivas-Davila, "Duty Cycle and Frequency Modulations in Class-E DC-DC Converters for a Wide Range of Input and Output Voltages," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10524-10538, 2018.
[27] J. A. Santiago-Gonzáles et al., "Design of resistive-input class E resonant rectifiers for variable-power operation," in Proc. Workshop on Control and Modeling for Power Electronics, 2013.
[28] F. Spliid et. al, "Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020.
[29] R. Elferich, "ZVS modelling of the LLC converter operating as unity power factor front end," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, 2018, pp. 1-7.
[30] A. M. Ammar et al., "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability" 2019 IEEE 20th Workshop on Control and Modelling for Power Electronics (COMPEL), Toronto, 2019.
[31] A. M. Ammar et. al, "Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020.
[32] A. J. Hanson and D. J. Perreault, "A High-Frequency Power Factor Correction Stage with Low Output Voltage," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020.
[33] J. A. Santiago-Gonzales et. al, "Single phase universal input PFC converter operating at HF," in Proc. IEEE Applied Power Electronics Conference and Exposition, 2018, pp. 2062-2069.
[34] H. Ma et al., "A Single-Stage Integrated Boost-LLC AC-DC Converter With Quasi-Constant Bus Voltage for Multichannel LED StreetLighting Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1143-1153, Sept. 2018.
[35] H. Valipour et al., "Resonant Bridgeless AC/DC Rectifier with High Switching Frequency and Inherent PFC Capability," in IEEE Transactions on Power Electronics, 2019.
[36] G. Li et al., "A Single-Stage Interleaved Resonant Bridgeless Boost Rectifier with High-Frequency Isolation," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.
[37] S. Mangkalajan et al., "A Single-Stage LED Driver Based on ZCDS Class-E Current-Driven Rectifier as a PFC for Street-Lighting Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp 8710-8727, 2018.
[38] K. Fukui and H. Koizumi, "Half-wave class DE low dv/dt rectifier," in 2012 IEEE Asia Pacific Conference on Circuits and Systems, pp. 854-860, 1996.
[39] K. Fukui and H. Koizumi, "Analysis of half-wave class DE low dv/dt rectifier at any duty cycle," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 234-245, 2014.
[40] M. Ekhtiari et. al, "Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 783-793, Jan. 2017.
[41] S. C. Moon et. al, "Adaptive Dead Time Synchronous Rectification Control for High Efficiency LLC Resonant Converter," Proc. IEEE Applied Power Electronics Conference and Exposition, 2019, pp. 2939-2946.
[42] Y. Nour, "Miniturization of High Frequecny Power Converters," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 2018.
[43] J. C. Hertel et. al, "Synchronous Rectifier for High-Frequency Switch Mode Power Supplies using Phase Locked Loops," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020.
[44] GeneSiC-Semiconductor, GB01SLT06 datasheet, 2014, http://www.genesicsemi.com/images/products_sic/rectifiers/GB01SLT06-214.pdf.
[45] GaNSystems, GS66502B datasheet, 2018, https://gansystems.com/wp-content/uploads/2018/04/GS66502B-DS-Rev-180420.pdf

## Appendix [J5]

H. Mahdi, A. M. Ammar, Y. Nour, and M. A. E. Andersen, "A Class-E-Based Resonant AC-DC Converter with Inherent PFC Capability," under revision in IEEE Journal of Emerging and Selected Topics in Power Electronics.

# A Class-E-Based Resonant AC-DC Converter with Inherent PFC Capability 

Hussein Mahdi, Student member, IEEE, Ahmed M. Ammar, Student member, IEEE, Yasser Nour, Senior Member, IEEE, and Michael A. E. Andersen, Member, IEEE

## Corresponding author:

Ahmed M. Ammar
Elektrovej 325, Room 216
2800 Kongens Lyngby, Denmark
Phone: +45 45253697
E-mail: ammma@elektro.dtu.dk


#### Abstract

This paper investigates the use of the class-E inverter for power factor correction (PFC) applications. Analytical and statespace models are derived showing the class-E inverter's capability of achieving inherent PFC operation with a constant duty cycle. A converter incorporating a diode bridge, a class-E inverter, and a class-D rectifier is presented for the PFC stage in singlephase offline converters. A prototype is designed to validate the analysis and presented design method. The prototype operates with zero-voltage switching (ZVS) across the load range and achieves up to 211 W of output power at an efficiency of $88 \%$, with an inherent power factor of 0.99 and a total harmonic distortion (THD) of $8.8 \%$. The measured input current harmonic magnitudes are well-within the limits of the IEC 61000-3-2 standard limits for class-C devices, making the converter relevant for LED driver applications. Frequency modulation is used to achieve lower output power down to 25 W , with a power factor of 0.95 , THD of $28 \%$, and an efficiency of $88 \%$.


## Index Terms

AC-DC power conversion, power factor correction, resonant power conversion, class-E inverter, zero-voltage switching.

## I. INTRODUCTION

Large-scale deployment of switch-mode power supplies to the utility introduces line current harmonics. The injected current harmonics result in voltage distortion and reduce the reliability of the grid [1, 2]. As a result, several international standards, such as the IEC 61000-3-2, expressly limit the magnitudes of input current harmonics and set a limit for the minimum power factor. Thus, a power factor correction (PFC) converter needs to be employed in offline converters for different applications to comply with these standards.

The typical solution for offline converters is a two-stage structure that is illustrated in Fig. 1. A front-end stage ac-dc PFC converter rectifies the ac voltage to a relatively smooth dc voltage while regulating the input current to follow the ac line voltage. A following dc-link capacitor filters the double-the-line frequency component. Finally, a dc-dc converter provides the current and voltage levels that apply to the load. This work's focus is on the PFC front-end stage of the offline converter.

Conventionally, pulse width modulation (PWM) converters are employed for the PFC stage, including boost [3-6], buck [7-9], buck-boost [10-12], SEPIC [13, 14], Cuk [15], and flyback [16] topologies. They offer high power quality and efficiency [17]. However, their hard-switching nature results in high switching losses, which sets an upper limit for the switching frequency and, in turn, the power density. In addition, their sharp switching current and voltage waveforms have high-frequency harmonic components, complicating electromagnetic interference (EMI) filters design. On the other hand, resonant converters operation is based on soft switching, which results in substantially lower switching losses and EMI noise at higher switching frequencies [18, 19]. As a result, resonant converters have been investigated for use in many applications, one of which is offline converters, where prior art reported their use in the ac-dc stage [20-23], dc-dc stage [24, 25], or both stages [26-28].

This paper investigates the feasibility of employing the class-E inverter for the PFC stage in single-phase offline converters. Mathematical models are derived for the circuit showing inherent PFC capability with a constant duty-cycle operation. A converter comprising an input bridge, a class-E inverter, and a class-D rectifier is presented. Fig. 2 shows the proposed converter block diagram. The converter operation is based on zero-voltage switching (ZVS) and achieves PFC inherently, which provides freedom from the limited bandwidths of the commercially available PFC controllers.

FOCUS OF THIS WORK


Fig. 1. Offline converter structure.


Fig. 2. The architecture of the proposed converter.
This paper is organized as follows: Section II describes the principle of operation of the presented converter. Mathematical models based on analytical and state-space approaches are covered in Section III. Section IV presents the design procedure and simulation results. Prototype implementation and experimental verification results are illustrated in Section V. Finally, conclusion is provided in Section VI.

## II. PRINCIPLE OF OPERATION

The schematic of the presented converter is shown in Fig. 3, which comprises a front-end diode bridge rectifier $D_{l}$ - $D_{4}$, a class-E inverter, and a class-D current-driven rectifier. The diode bridge rectifies the ac input voltage. A capacitor $C_{i n}$ is connected in parallel with the bridge to suppress the EMI and absorb the reverse current from the inverter. A class-E ZVS inverter drives the resonant tank with a current $i_{r}(t)$, where the shape of the waveform depends on the loaded quality factor of the tank $Q_{L}$ and the dutycycle $D$. A class-D rectifier converts the high-frequency current into a dc output voltage, where the voltage stress across the rectifier diodes equals the output voltage.

Considering that the switching frequency $f_{s}$ is much higher than the line frequency $f_{l}$, the input voltage to the inverter $v_{\text {rec }}(t)$ is assumed constant across the switching cycle. With a high-enough quality factor for the resonant tank, the first-harmonic approximation (FHA) approach for modeling resonant converters is valid, and the resonant current is a sinewave with the form

$$
\begin{equation*}
i_{r}\left(\theta_{s}\right)=I_{r} \sin \left(\theta_{s}+\varphi\right) \tag{1}
\end{equation*}
$$

where $I_{r}$ is the current amplitude, $\theta_{s}=\omega_{s} t$ is the current angle across the switching cycle, and $\varphi$ is the phase shift with the switching node voltage.


Fig. 3. Class-E converter for PFC applications.

The switching cycle is divided into four intervals, as shown in Fig. 4, with the corresponding voltage and current waveforms illustrated in Fig. 5.

In interval $\mathrm{I}\left(t_{0}-t_{l}\right)$, the switch is on and the rectified voltage $v_{\text {rec }}(t)$ is higher than the switching node voltage, thus the input current $i_{i n}(t)$ increases linearly, charging the input inductor $L_{i n}$. The resonant current is positive and flows in $D_{6}$, while $D_{5}$ is in reverse bias. Accordingly, the current flowing through the switch is the difference between $i_{i n}(t)$ and $i_{r}(t)$.

In interval II $\left(t_{1}-t_{2}\right)$, the switch is still on, and the input current $i_{i n}(t)$ keeps charging the input inductor $L_{i n}$, while the resonant current reverses its direction and flows in $D_{5}$ with $D_{6}$ in reverse bias.

In interval III $\left(t_{2}-t_{4}\right)$, the switch is turned off and the capacitor $C_{s}$ starts charging with the input current. Thus, $v_{s}(t)$ begins to increase, yet it is still less than the $v_{\text {rec }}(t)$. As a result, $i_{\text {in }}(t)$ keeps increasing until it reaches its maximum at $t_{3}$ when $v_{\text {rec }}(t)$ equals $v_{s}(t)$. Afterwards, the input inductor $L_{i n}$ starts discharging in the capacitor $C_{s}$, resulting in increasing of the voltage stress across the switch to its maximum value by the end of this interval. Theoretically, the voltage stress across the switch $v_{s}(t)$ in a class-E inverter


Interval I


Interval II


Interval III


Interval IV
Fig. 4. Simplified circuit diagram for half-line cycle operation.


Fig. 5 Voltage and current waveforms across two switching cycle.
reaches about 3.6 times the input voltage with $50 \%$ duty cycle [29]. However, in practice, this stress could reach more than four times the input voltage due to the nonlinearity of the switch node capacitance $C_{s}[30,31]$.

In interval IV $\left(t_{4}-T\right)$, the switch is still turned off, the resonant current reverses its direction, turning $D_{5}$ off and $D_{6}$ on. The capacitor $C_{s}$ starts discharging, and the switch voltage reduces until $v_{\text {rec }}(t)$ equals $v_{s}(t)$ at $t_{5}$, with the inductor $L_{\text {in }}$ is discharging as $v_{\text {rec }}(t)<$ $v_{s}(t)$. From $t_{5}$ to the end of the interval, the inductor $L_{i n}$ is charging, and the capacitor $C_{s}$ continues discharging until full depletion. By the end of this interval, the switch is turned on by the gate driver, and a new cycle begins.

## III. Mathematical Modelling

In this section, the mathematical models for the class-E inverter are investigated with respect to the input impedance. The conventional analytical and state-space approaches are considered. In the former approach, the design procedure derives the equations from the waveforms, while the latter is based on the basic circuit equations from Ohm's and Kirchhoff's laws. The principle of operation of the Class-E rectifier as an input current shaping stage is explained in [27,28] and is adopted in this work.

## A. Analytical Approach

The analysis of the proposed topology is carried out across the switching cycle and using the approach given in [29], which assumes ideal semiconductor switches, a high-enough input inductance such that the DC component of the input current $I_{i n}$ is only considered. From the principle of operation given in Section II and the $V_{s}$ waveform in Fig. 5, the capacitor $C_{s}$ current can be written as follows

$$
i_{C_{s}}\left(\theta_{s}\right)= \begin{cases}0 & , 0<\theta_{s} \leq 2 \pi D  \tag{2}\\ I_{i n}-I_{r} \sin \left(\theta_{s}+\varphi\right), 2 \pi D<\theta_{s} \leq 2 \pi\end{cases}
$$

The voltage across the switch is then calculated

$$
v_{s}\left(\theta_{s}\right)=\frac{1}{\omega_{s} C_{s}} \int_{0}^{\theta_{s}} i_{C_{s}}(\theta) d \theta=\left\{\begin{array}{c}
0, \quad 0<\theta_{s} \leq 2 \pi D  \tag{3}\\
\frac{1}{\omega_{s} C_{s}}\left[\begin{array}{c}
I_{r}\left[\theta_{s}-2 \pi D\right) \\
\left.+\cos \left(\theta_{s}+\varphi\right)-\cos (2 \pi D+\varphi)\right]
\end{array}\right], 2 \pi D<\theta_{s} \leq 2 \pi
\end{array}\right.
$$

where $\theta$ is the variable of integration. Under optimal operation conditions, where ZVS is achieved, the voltage across the switch equals zero by the end of the switching period. Substituting $\theta_{s}=2 \pi$ in (3) and equating to zero, the following expression for the resonant current amplitude is derived.

$$
\begin{equation*}
I_{r}=I_{i n} \frac{2 \pi(1-D)}{\cos (2 \pi D+\varphi)-\cos (\varphi)} \tag{4}
\end{equation*}
$$

Considering zero-derivative voltage switching $\left(\mathrm{ZdVS}, d v_{s}(2 \pi) / d \theta=0\right)$ is also achieved, taking the derivative for (3) with $\theta_{s}=2 \pi$ and equating to zero, the following expressions for the phase shift $\varphi$ is derived.

$$
\begin{equation*}
\tan (\varphi)=\frac{\cos (2 \pi D)-1}{2 \pi(1-D)+\sin (2 \pi D)} \tag{5}
\end{equation*}
$$

It can be seen that $\varphi$ is a function of the duty ratio $D$. Following, the rectified voltage can be written as follows

$$
\begin{equation*}
V_{\text {rec }}=\frac{1}{2 \pi} \int_{0}^{2 \pi} v_{L_{\text {in }}}(\theta) d \theta+\frac{1}{2 \pi} \int_{0}^{2 \pi} v_{s}(\theta) d \theta \tag{6}
\end{equation*}
$$

As the average voltage across the input inductor is zero, eliminating the first term and substituting (3) in (6) then evaluating the integration gives

$$
\begin{equation*}
V_{\text {rec }}=\frac{I_{\text {in }}}{\omega_{s} C_{s}}\left[\frac{(1-D)[\pi(1-D) \cos (\pi D)+\sin (\pi D)]}{\tan (\pi D+\varphi) \sin (\pi D)}\right] \tag{7}
\end{equation*}
$$

Dividing (7) by $I_{i n}$ gives the following expression for the input resistance.

$$
\begin{equation*}
R_{i n}=\frac{1}{\omega_{s} C_{s}}\left[\frac{(1-D)[\pi(1-D) \cos (\pi D)+\sin (\pi D)]}{\tan (\pi D+\varphi) \sin (\pi D)}\right] \tag{8}
\end{equation*}
$$

Since (8) is a function of the duty ratio $D$ and phase shift $\varphi$, which is itself a function of duty ratio as shown in (5), then operating at constant duty ratio results in a constant input resistance that is independent of line changes. As a result, the converter is seen as a resistor from the bridge side across the line cycle and power factor correction is achieved.

## B. State-Space Approach

While the analytical approach assumes an ideal switching device and a sinusoidal resonant current to ensure the validity of the FHA approach, in the state-space approach, the design parameters are computed numerically. The state-space approach is used in prior art [32-34] to design class-E dc-dc converters with any loaded quality factor of the resonant tank and any size for the input inductor. Accordingly, it is considered in this section for flexibility across different designs.

By adding the switch on resistance to the model, the switch is replaced with a resistor as follows

$$
r_{s}= \begin{cases}r_{o n} & , 0<\theta_{s} \leq 2 \pi D  \tag{9}\\ r_{\text {off }} & , 2 \pi D<\theta_{s} \leq 2 \pi\end{cases}
$$

where $r_{o n}$ and $r_{o f f}$ are the equivalent resistances of the switch in on and off states, respectively. The circuit has four energy storage components ( $L_{i n}, L_{r}, C_{s}$ and $C_{r}$ ), which define the dimension of the state vector. The following expressions are obtained by applying Kirchhoff voltage and current laws.

$$
\begin{gather*}
\omega_{s} L_{i n} \frac{d i_{i n}\left(\theta_{s}\right)}{d \theta_{s}}=v_{r e c}\left(\theta_{s}\right)-v_{s}\left(\theta_{s}\right)  \tag{10a}\\
\omega_{s} C_{r} \frac{d v_{C_{r}}\left(\theta_{s}\right)}{d t}=i_{r}\left(\theta_{s}\right)  \tag{10b}\\
\omega_{s} L_{r} \frac{d i_{r}\left(\theta_{s}\right)}{d t}=v_{s}\left(\theta_{s}\right)-v_{C_{r}}\left(\theta_{s}\right)-i_{r}\left(\theta_{s}\right) R_{e f f}  \tag{10c}\\
\omega_{s} C_{s} \frac{d v_{s}\left(\theta_{s}\right)}{d t}=i_{i n}\left(\theta_{s}\right)-\frac{v_{s}\left(\theta_{s}\right)}{r_{s}}-i_{r}\left(\theta_{s}\right) \tag{10d}
\end{gather*}
$$

Where $v_{C r}(\theta s)$ is the voltage across the resonant tank capacitor $C_{r}$ and $R_{e f f}$ is the class-D rectifier effective resistance. By normalizing the impedances in (10) with the effective resistances, it can be rearranged and rewritten in the following matrix form

$$
\begin{align*}
& \dot{x}=A \cdot x+B \cdot u  \tag{11a}\\
& A=\left[\begin{array}{cccc}
\frac{1}{\omega_{s} C_{s} r_{s}} & 0 & \frac{1}{\omega_{s} R_{e f f} C_{s}} & \frac{-1}{\omega_{s} R_{e f f} C_{s}} \\
0 & 0 & 0 & \frac{1}{\omega_{s} R_{e f f} C_{r}} \\
\frac{-R_{e f f}}{\omega_{s} L_{i n}} & 0 & 0 & 0 \\
\frac{1}{Q_{L}} & 0 & \frac{-1}{Q_{L}} & \frac{-1}{Q_{L}}
\end{array}\right]  \tag{11b}\\
& B=\left[\begin{array}{c}
0 \\
0 \\
\frac{R_{e f f}}{\omega_{s} L_{i n}} \\
0
\end{array}\right]  \tag{11c}\\
& x=\left[\begin{array}{c}
v_{s}\left(\theta_{s}\right) \\
v_{C_{r}}\left(\theta_{s}\right) \\
i_{\text {in }}\left(\theta_{s}\right) \\
i_{r}\left(\theta_{s}\right)
\end{array}\right]  \tag{11d}\\
& Q_{L}=\frac{\omega_{s} \cdot L_{r}}{R_{e f f}} \tag{11e}
\end{align*}
$$

Where $x$ is the state vector, $A$ is the system matrix, $B$ is the control matrix, and $u$ is the input vector. From (11), the number of parameters is nine, i.e. $\omega_{s}, D, Q_{L}, L_{i n}, L_{r}, C_{r}, C_{s}, R_{e f f}, r_{s} \in \mathbb{R}^{9}$ and the solution of the equation is

$$
\begin{equation*}
x\left(\theta_{s}\right)=x_{n}\left(\theta_{s}\right)+x_{F}\left(\theta_{s}\right) \tag{12}
\end{equation*}
$$

Where $x_{n}\left(\theta_{s}\right)$ is the natural response of the system and $x_{F}\left(\theta_{s}\right)$ is the forced response. These two terms can be calculated as follows [35].

$$
\begin{gather*}
x_{n}\left(\theta_{S}\right)=e^{A \theta_{S}} \cdot x\left(0^{-}\right)  \tag{13}\\
x_{F}\left(\theta_{S}\right)=A^{-1} \cdot\left(e^{A \theta_{S}}-I\right) \cdot B \cdot u \tag{14}
\end{gather*}
$$

Where $e^{4 \theta s}$ is the exponential matrix, $x\left(\theta^{-}\right)$is the initial condition vector, and $I$ is the identity matrix, while the currents are normalized with the input current and the voltages are normalized with the input voltage. Since the waveforms are continuous and periodic, the initial conditions can be found by applying the continuity condition of the waveforms such that

$$
\begin{gather*}
x_{o n}\left(0^{-}\right)=\left.x_{o f f}(\theta)\right|_{\theta=2 \pi(1-D)}  \tag{15a}\\
x_{o f f}\left(0^{-}\right)=\left.x_{o n}(\theta)\right|_{\theta=2 \pi D} \tag{15b}
\end{gather*}
$$

Substituting (12)-(14) in (11) gives

$$
\left[\begin{array}{c}
x_{o n}(2 \pi)  \tag{16}\\
x_{o f f}(2 \pi)
\end{array}\right]=\left[\begin{array}{cc}
-e^{2 \pi D A_{o n}} & I \\
I & -e^{2 \pi(1-D) A_{o f f}}
\end{array}\right]^{-1} \cdot\left[\begin{array}{c}
A_{o n}^{-1}\left(e^{2 \pi D A_{o n}}-I\right) \\
A_{o f f}^{-1}\left(e^{2 \pi(1-D) A_{o f f}}-I\right)
\end{array}\right] \cdot B
$$

Where $A_{o n}$ and $A_{o f f}$ are the system matrices in (11) when $r_{s}$ is equal to $r_{o n}$ and $r_{o f f}$, respectively. Under optimal operation conditions, where ZVS and ZdVS are achieved, (16) can be re-evaluated and solved numerically using the Matlab fsolve solver. However, there are nine parameters and two optimum operation conditions. Therefore, $\omega_{s}, D, Q_{L}, L_{i n}, L_{r}, R_{e f f}, r_{s} \in \mathbb{R}^{7}$ are chosen as the design parameters, while $C_{r}, C_{s}$ are solved as unknown parameters. Since (11) is in the form of a first-order differential equation, the solution with oscillating input can also be written as

$$
\begin{gather*}
x\left(\theta_{l}\right)=M \cdot \cos \left(\theta_{l}\right)+N \cdot \sin \left(\theta_{l}\right)=G \cdot \sin \left(\theta_{l}-\alpha\right)  \tag{17a}\\
G=\sqrt{M^{2}+N^{2}}=\frac{B}{\sqrt{2}}  \tag{17b}\\
\alpha=\tan ^{-1}\left(\frac{N}{M}\right)=\frac{\omega_{l}}{A} \tag{17c}
\end{gather*}
$$

Where $M$ and $N$ are solution parameters that are found from the initial conditions, $\theta_{l}=\omega_{l} t$ is the input current angle across the line cycle, $G$ is the gain vector, and $\alpha$ is the phase shift matrix. Equation (17a) mathematically shows that the response of the system, $i_{i n}\left(\theta_{l}\right)$ which is the main interest, to the oscillating input voltage has the same frequency of the input and phase-shifted by $\alpha$. From $(17 \mathrm{c})$, it can be proven that the input current is in phase with the input voltage (i.e. $\alpha \approx 0$ ), and hence the converter emulates a resistor.

TABLE I
DESIGN SPECIFICATIONS OF THE PROPOSED TOPOLOGY

| Parameters | Specifications |
| :---: | :---: |
| RMS Input Voltage [V] | 120 |
| Line Frequency [Hz] | 60 |
| Output Power [W] | 300 |
| Output Voltage [V] | 200 |
| Switching Frequency [kHz] | 90 |

## IV. CONVERTER DESIGN

This section describes the design procedure of the presented converter. Table I summarizes the converter design specifications. The converter is designed to operate from US mains input voltage for a rated output power of 300 W and an output voltage of 200 V. A $90-\mathrm{kHz}$ switching frequency is chosen for this design which is intended to prove the analysis and inherent PFC capability. A duty cycle of $40 \%$ is chosen as a good trade-off between the power output capability of the converter and the maximum voltage stress on the switch.

In the analytical approach, the design procedure based on the FHA approach and given in [29] is followed here. To ensure the validity of the FHA approach, a high-quality factor of seven is chosen for this design. The procedure begins with the calculation of the class-D rectifier effective input resistance.

$$
\begin{equation*}
R_{e f f}=\frac{2 R_{L}}{\pi^{2}}=\frac{2 V_{o}^{2}}{\pi^{2} \cdot P_{o}} \tag{18}
\end{equation*}
$$

Where $R_{L}$ is the load resistance, $V_{0}$ is the output voltage, and $P_{0}$ is the output power. The phase angle of the resonant current can be written as

$$
\begin{equation*}
\varphi=\pi+\arctan \left(\frac{\cos (2 \pi D)-1}{2 \pi(1-D)+\sin (2 \pi D)}\right) \tag{19}
\end{equation*}
$$

The capacitor $C_{s}$ is calculated from

$$
\begin{equation*}
C_{s}=\frac{\cos (\pi D+\varphi)[(1-D) \pi \cos (\pi D)+\sin (\pi D)] \cdot 2 \sin (\pi D) \sin (\pi D+\varphi)}{\pi^{2}(1-D) \omega_{s} R_{e f f}} \tag{20}
\end{equation*}
$$

The switching frequency is chosen to be higher than the resonant frequency such that the net impedance of the tank is inductive. The inductor $L_{r}$ can be divided into two series inductances, such that $L_{r l}$ resonates with the capacitor $C_{r}$ at the switching frequency, while $L_{r 2}$ is responsible for the phase lagging shown in (19) and can be calculated from

$$
\begin{equation*}
L_{r 2}=\frac{R_{e f f}}{\omega_{s}} \cdot \frac{2(1-D)^{2} \pi^{2}-1+2 \cos (\varphi) \cos (2 \pi D+\varphi)-\cos (2(\pi D+\varphi))[\cos (2 \pi D)-\pi(1-D) \sin (2 \pi D)]}{4 \sin (\pi D) \sin (\pi D+\varphi) \cos (\pi D+\varphi)[(1-D) \pi \cos (\pi D)+\sin (\pi D)]} \tag{21}
\end{equation*}
$$

Then, the resonant capacitor can be found as follows

TABLE II
Calculated Component Values

| Component | Analytical <br> Model | State- <br> space <br> Model | Differences <br> [\%] |
| :---: | :---: | :---: | :---: |
| $\boldsymbol{L}_{\boldsymbol{i n}}[\boldsymbol{\mu H}]$ | 205.8 | 205.8 | 0 |
| $\boldsymbol{L}_{\boldsymbol{r}}[\boldsymbol{\mu} \boldsymbol{H}]$ | 350.6 | 350.6 | 0 |
| $\boldsymbol{C}_{\boldsymbol{s}}[\boldsymbol{n F}]$ | 15.2 | 15.2 | 0.3 |
| $\boldsymbol{C}_{\boldsymbol{r}}[\boldsymbol{n F}]$ | 11.7 | 12.3 | 7 |

$$
\begin{equation*}
C_{r}=\frac{1}{\omega_{s}^{2} L_{r 1}}=\frac{1}{\omega_{s}^{2}\left(L_{r}-L_{r 2}\right)}=\frac{1}{\omega_{s}\left(Q_{L} \cdot R_{e f f}-\omega_{s} \cdot L_{r 2}\right)} \tag{22}
\end{equation*}
$$

The input inductance ( $L_{i n}$ ) should be large enough to ensure a small ripple current through the choke ( $10 \%$ of dc current), and calculated as follows [29]

$$
\begin{equation*}
L_{i n} \geq \frac{7 R_{e f f}}{f_{s}} \tag{23}
\end{equation*}
$$

Regarding the output capacitor $C_{f}$, it needs to be large enough to filter the double-the-line frequency in single-phase PFC applications, and it is calculated from the following expression, with $\eta$ being the efficiency [28]

$$
\begin{equation*}
C_{f} \geq \frac{\eta \cdot P_{o}}{0.04 V_{0}^{2} \cdot \omega_{l}} \tag{24}
\end{equation*}
$$

The state-space approach is carried out numerically in MATLAB. Table II lists the calculated values of the components from both models. It can be observed that the values obtained from both models are highly correlated.

## V. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

This section covers the implementation procedure for a prototype built based on the analysis and design procedure. Experimental results are then presented and discussed.

## A. Implementation

The prototype of the proposed topology is assembled on a two-layer PCB. Table III lists the prototype bill of materials based on the parameters obtained from the design procedure given in Section IV. Compared with silicon devices, wide-bandgap devices have reduced reverse-recovery charge and better figures of merit [36-38]. A Silicon Carbide ( SiC ) device is used for the converter single switch, which is driven using a single-channel isolated gate driver (UCC5350SBD by Texas Instruments).

## B. Experimental Results

Fig. 6 shows the prototype testing lab setup. The converter is tested from US-mains input voltage, delivering up to 211 W of power at 89.5 kHz and $55 \%$ duty ratio, where thermal considerations limited the delivery for a higher power.

TABLE III

| BILL OF MATERIALS |  |  |
| :---: | :---: | :---: |
| Component | Value | Type |
| $\boldsymbol{D}_{\mathbf{1}}-\boldsymbol{D}_{\mathbf{4}}$ | GBU10A | Bridge Rectifier |
| $\boldsymbol{C}_{\boldsymbol{D} \boldsymbol{C}}[\boldsymbol{\mu} \boldsymbol{F}]$ | 1 | SMD Film Capacitor |
| $\boldsymbol{L}_{\mathbf{1}}[\boldsymbol{m} \boldsymbol{H}]$ | 1.3 | 3C97 ETD49/25/16 |
| $\boldsymbol{L}_{\boldsymbol{2}}[\boldsymbol{\mu} \boldsymbol{H}]$ | 342.9 | 3C97 ETD59/31/22 |
| $\boldsymbol{C}_{\boldsymbol{s}}[\boldsymbol{n} \boldsymbol{F}]$ | 15 | SMD Ceramic Capacitor |
| $\boldsymbol{Q}_{\boldsymbol{1}}$ | C3M0075120D | 1200 V SiC MOSFET |
| $\boldsymbol{C}[\boldsymbol{n F}]$ | $2 \times 5.6$ | SMD Ceramic Capacitor |
| $\boldsymbol{D}_{5} \& \boldsymbol{D}_{\mathbf{6}}$ | C3D10065A | SiC Schottky Diode |



Fig. 6. Topology under testing.
Fig. 7 shows the line-frequency waveforms at 211 W load. The input and output voltages are measured using high-voltage differential probes (LeCroy ADP305 and Testec SI 9001), and the current is displayed using a clamp-on current probe (Siemens $7 \mathrm{KA} 1412-8 \mathrm{AA}$ ). The figure shows the input current to be proportional to the input voltage, with a minor phase difference, achieving a power factor of 0.99 inherently. The dashed waveform is the input current filtered by the moving-average function in MATLAB and shown for clarity.

Fig. 8 shows the switching-frequency waveforms at 211 W . The resonant current has a sinusoidal waveform, which goes in accordance with the analysis and design procedure based on the FHA approach, and it is about 15 A peak-to-peak. While the input current in the inductor $\left(L_{i n}\right)$ is mainly a dc component with 0.4 A peak-to-peak ripple. The figure illustrates the inductive mode of operation, where the resonant current lags the switch node voltage and the switch voltage return to zero before the switch is turned on, achieving ZVS. A short interval on reverse conduction of the FET is observed, where the switch-node capacitance is fully depleted before the switch turns on. However, with the reduced reverse recovery charge in SiC devices, the contribution of reverse


Fig. 7. Experimental line-frequency waveforms of the proposed converter at full load.


Fig. 8. Experimental switching-frequency waveforms of the proposed converter at 211 W .
conduction to the overall power loss is insignificant and can be eliminated with a precise adjustment of the switch driving signal duty cycle.

Fig. 9 and Fig. 10 show the line-frequency and switching-frequency waveforms at 25 W , which is the minimum power required to achieve PFC according to the IEC 61000-3-2 standard for class-C devices. The figures show that a high-power factor is still achieved at the light load, where the ZVS operation is maintained through the adjustment of the switch duty ratio.

Fig. 11 shows the obtained efficiency and employed switching frequency across the load range. The results show that the output power can be regulated from 211 W down to 25 W with switching frequency modulation between 89.5 kHz to 104.3 kHz , respectively. The peak obtained efficiency is $88.3 \%$ at 90 W with 96 kHz and a duty ratio of 0.5 . The small dips in the efficiency curve are attributed to the partial loss of ZVS , which is corrected by adjusting the duty ratio.


Fig. 9. Experimental line-frequency waveforms of the proposed converter at 25 W .
High Frequency Waveforms at 25 W



Fig. 10. Experimental switching-frequency waveforms of the proposed converter at 25 W .

The power quality results are shown in Fig. 12, where a power factor of 0.99 and a total harmonic distortion (THD) of $8.8 \%$ are achieved at full load, while the minimum power factor is 0.95 at 25 W with a THD of $28 \%$. Considering solid-state lighting drivers as one of the potential applications of the proposed converter, Fig. 13 shows the input current harmonics magnitudes at 211 W and 25 W against the IEC 61000-3-2 standard class-C device limits. The figure depicts that the obtained harmonics are well within the limits set by the standard at full-load, while the $5^{\text {th }}$ harmonic marginally exceeds the limit at light-load.


Fig. 11. The efficiency and Switching Frequencies of the proposed converter in different output power levels.


Fig. 12. The obtained power factor and THD across load range.


Fig. 13. Harmonic spectrum for input line current of the Class-E circuit compared to IEC 61000-3-2 class C standard. At 211 W and 25 W .

TABLE V
COMPARISON WITH REPORTED LETRATURE

| Reference | [3] | [7] | [10] | [13] | [15] | [16] | [26] | [20] | [27] | [23] | [21] | This work |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Year | 2019 | 2015 | 2018 | 2016 | 2017 | 2017 | 2013 | 2019 | 2009 | 2014 | 2020 | 2020 |
| Type | PWM | PWM | PWM | PWM | PWM | PWM | Resonant | Resonant | Resonant | Resonant | Resonant | Resonant |
| Topology | Boost | Buck | BuckBoost | SEPIC | Cuk | Flyback | Class-D <br> Rectifier | Class-D Converter | Class-E <br> Rectifier | Class-D <br> Rectifier | Class-D Inverter | Class-E <br> Inverter |
| Aux. circuit | None | Filter | None | None | Filter | Filter | Matching Network | None | Matching Network | Matching Network | Charge Pump | None |
| $\mathrm{V}_{\mathrm{IN}}\left[\mathrm{V}_{\mathrm{rms}}\right]$ | Universal | Universal | 220 | 120 | Universal | Universal | 220 | 230 | 220 | 220 | 230 | 120 |
| Power [W] | 1000 | 300 | 245 | 200 | 300 | 60 | 36 | 105 | 36 | 36.4 | 50 | 211 |
| Vout [V] | 400 | 80 | 245 | 400 | 300 | 24 | 327 | 450 | 343 | 342 | 300 | 165 |
| Power Factor | 0.99 | 0.94 | 0.99 | 0.97 | 0.99 | 0.99 | 0.99 | 0.99 | 0.99 | 0.98 | 0.99 | 0.99 |
| THD [\%] | - | 25.7 | <10 | 27.2 | <6 | 8 | 1.4 | 5.2 | 5.6 | 20 | 8.6 | 8.8 |
| $\begin{gathered} \hline \text { Efficiency } \\ {[\%]} \\ \hline \end{gathered}$ | 96 | 97 | 97 | 96 | N/A | 91 | 90 | 94 | 86 | 94 | 88 | 88 |
| Switching Frequency [kHz] | 550 | 65 | 4000 | 50 | 500 | 300 | 84 | 2000 | 61 | 50 | 1000 | 90 |
| PFC functionality | Inherent | Controlled | Controlled | Controlled | Controlled | Controlled | Inherent | Controlled | Inherent | Inherent | Inherent | Inherent |
| Components count* | 18 | 14 | 13 | 15 | 9 | 8 | 16 | 12 | 14 | 9 | 12 | 10 |

Table V compares the proposed work with a number of reported solutions for PFC applications for the low-mid power range. It can be observed that the obtained power factor and THD figures fall within the ranges reported by prior art. In addition, the proposed converter achieves PFC inherently across a wide load range. That provides freedom from the limited bandwidths of commercial PFC controllers and is cost-competitive, with low component overhead. Compared with the reported resonant PFC converters, the class-E inverter topology offers a simpler driving circuitry, as it incorporates a single switch referenced to ground, with no need for additional circuit or matching network, reducing the overall system bill of materials. In addition, as the topology features an input inductor, it requires simpler input filter and diode bridge implementations, as the input current is not pulsating such as the case in [21]. It is noted that the proposed converter's efficiency is lower than that reported by PWM converters, yet it is on par with several reported resonant converter solutions. As the target of the presented prototype was to prove the inherent PFC capability, there is a space for improvement with an optimized high-frequency design that takes benefit of the ZVS capabilities of the proposed work towards high-power-density implementations with higher efficiencies.

## VI. CONCLUSION

This paper investigates the use of the class-E inverter for PFC applications. The circuit analytical model proves that the converter emulates a resistance to the input when operating with a fixed duty ratio. That is asserted from the obtained state-space model, where the phase shift between the input current and voltage is shown to equal almost zero. A resonant converter incorporating a class-E inverter with a class-D rectifier is designed and implemented for the front-end AC-DC stage in a two-stage offline converter. A prototype is built and tested to prove the concept. The prototype achieves zero-voltage switching and inherent PFC along the load
range between 25 W and 211 W , with a peak efficiency of $88 \%$, a peak power factor of 0.99 and mimimum THD of $8.8 \%$ at full load. The input current harmonic magnitudes are well-within the limits of the IEC 61000-3-2 standard limits for class-C devices, making it relevant LED driver applications.

## References

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," IEEE Transactions on Industrial Electronics, vol. 50, no. 5, pp. 962-981, 2003.
[2] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase PFC topologies based on the boost converter," in 2010 9th IEEE/IAS International Conference on Industry Applications - INDUSCON 2010, 8-10 Nov. 2010 2010, pp. 1-6.
[3] R. T. Ryan, D. N. Hogan, R. J. Morrison, and J. G. Hayes, "Digital Closed-Loop Control Strategy to Maintain the Phase Shift of a Multi-Channel BCM Boost Converter for PFC Applications," IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 7001-7012, 2019.
[4] A. Jha and B. Singh, "A bridgeless boost PFC converter fed LED driver for high power factor and low THD," in 2018 IEEMA Engineer Infinite Conference (eTechNxT), 13-14 March 2018 2018, pp. 1-6.
C. Xue, Y. Zhou, and W. Xu, "Modeling and stability analysis of parallel-connected PFC Boost converter," in 2019 Chinese Control And Decision Conference (CCDC), 3-5 June 2019 2019, pp. 1775-1779.
[6] H. Xu, D. Chen, F. Xue, and X. Li, "Optimal Design Method of Interleaved Boost PFC for Improving Efficiency from Switching Frequency, Boost Inductor, and Output Voltage," IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6088-6107, 2019.
[7] C. Yang, Y. Liu, P. Tseng, T. Pan, H. Chiu, and Y. Lo, "DSP-Based Interleaved Buck Power Factor Corrector With Adaptive Slope Compensation," IEEE Transactions on Industrial Electronics, vol. 62, no. 8, pp. 4665-4677, 2015.
[8] Y. Liu, F. Syu, H. Hsieh, K. A. Kim, and H. Chiu, "Hybrid Switched-Inductor Buck PFC Converter for High-Efficiency LED Drivers," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 8, pp. 1069-1073, 2018.
[9] C. Lin et al., "Study on an interleaved buck power factor corrector with gallium nitride field effect transistor and integrated inductor," IET Power Electronics, vol. 7, no. 10, pp. 2506-2516, 2014.
[10] A. J. Hanson and D. J. Perreault, "A high frequency power factor correction converter with soft switching," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), 4-8 March 2018 2018, pp. 2027-2034.
[11] B. Zhao, A. Abramovitz, and K. Smedley, "Family of Bridgeless Buck-Boost PFC Rectifiers," IEEE Transactions on Power Electronics, vol. 30, no. 12, pp. 6524-6527, 2015.
[12] M. O. Badawy, Y. Sozer, and J. A. D. Abreu-Garcia, "A Novel Control for a Cascaded Buck-Boost PFC Converter Operating in Discontinuous Capacitor Voltage Mode," IEEE Transactions on Industrial Electronics, vol. 63, no. 7, pp. 4198-4210, 2016.
[13] A. M. A. Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless PFC-Modified SEPIC Rectifier With Extended Gain for Universal Input Voltage Applications," IEEE Transactions on Power Electronics, vol. 30, no. 8, pp. 4272-4282, 2015.
[14] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 873-881, 2011.
[15] A. Jha and B. Singh, "Cuk PFC converter for high brightness LED driver with brightness control," in 2016 IEEE 7th Power India International Conference (PIICON), 25-27 Nov. 2016 2016, pp. 1-6.
[16] C. Zhao, J. Zhang, and X. Wu, "An Improved Variable On-Time Control Strategy for a CRM Flyback PFC Converter," IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 915-919, 2017.
[17] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics. Boston: Boston: Springer, 2007.
[18] L. S. Mendonça, T. C. Naidon, G. G. d. Freitas, M. L. d. S. Martins, and F. E. Bisogno, "Energy-Based Normalization for Resonant Power Converters," IEEE Transactions on Power Electronics, vol. 33, no. 8, pp. 6526-6536, 2018.
[19] M. Salem, A. Jusoh, N. R. N. Idris, Himadry S. Das, and I. Alhamrouni, "Resonant power converters with respect to passive storage (LC) elements and control techniques - An overview," Renewable and Sustainable Energy Reviews, vol. 91, pp. 504-520, 2018.
[20] F. M. Spliid, A. M. Ammar, and A. Knott, "Analysis and Design of a Resonant Power Converter with Wide Input Voltage Range for AC/DC Applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1-1, 2019.
[21] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability," IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1-1, 2020.
[22] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," in 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 17-20 June 2019 2019, pp. 1-5.
[23] C. Ekkaravarodome, V. Chunkag, K. Jirasereeamornkul, and M. K. Kazimierczuk, "Class-D Zero-Current-Switching Rectifier as Power-Factor Corrector for Lighting Applications," IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4938-4948, 2014.
[24] A. M. Ammar, Y. Nour, and A. Knott, "A High-Efficiency 1 MHz 65 W GaN-Based LLC Resonant DC-DC Converter," in 2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE), 23-25 Oct. 2019 2019, pp. 448-452.
[25] Y. Wang, F. Li, Y. Qiu, S. Gao, Y. Guan, and D. Xu, "A Single-Stage LED Driver Based on Flyback and Modified Class-E Resonant Converters With Low-Voltage Stress," IEEE Transactions on Industrial Electronics, vol. 66, no. 11, pp. 8463-8473, 2019.
[26] C. Ekkaravarodome, K. Jirasereeamornkul, and M. K. Kazimierczuk, "Implementation of a DC-Side Class-DE Low- $d v / d t$ Rectifier as a PFC for Electronic Ballast Application," IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5486-5497, 2014.
[27] J. Sasiluk and J. Kamon, "The electronic ballast using Class-E rectifier with tapped inductor for power factor correction," in 2008 International Symposium on Intelligent Signal Processing and Communications Systems, 8-11 Feb. 2009 2009, pp. 1-4.
[28] K. Jirasereeamornkul, M. K. Kazimierczuk, I. Boonyaroonate, and K. Chamnongthai, "Single-stage electronic ballast with class-E rectifier as powerfactor corrector," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 53, no. 1, pp. 139-148, 2006.
[29] M. Kazimierczuk and D. Czarkowski, Resonant Power Converters, 2nd Edition ed. Wily, 2012.
[30] M. J. Chudobiak, "The use of parasitic nonlinear capacitors in class E amplifiers," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 41, no. 12, pp. 941-944, 1994.
[31] T. M. Andersen, S. K. Christensen, A. Knott, and M. A. E. Andersen, "A VHF class E DC-DC converter with self-oscillating gate driver," in 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 6-11 March 2011 2011, pp. 885-891.
[32] H. Sekiya, I. Sasase, and S. Mori, "Computation of design values for Class E amplifiers without using waveform equations," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 49, no. 7, pp. 966-978, 2002, doi: 10.1109/TCSI.2002.800474.
[33] J. Lu and T. Yahagi, "Design of generalized class E2 dc/dc converter," International Journal of Circuit Theory and Applications, vol. 31, pp. 229-248, 05/01 2003.
[34] P. C. Luk, S. Aldhaher, W. Fei, and J. F. Whidborne, "State-Space Modeling of a Class E ${ }^{2}$ Converter for Inductive Links," IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 3242-3251, 2015.
[35] G. Strang, Differential Equations and Linear Algebra. Wellesley-Cambridge Press,U.S., 2015, p. 510.
[36] F. F. Wang and Z. Zhang, "Overview of silicon carbide technology: Device, converter, system, and application," CPSS Transactions on Power Electronics and Applications, vol. 1, no. 1, pp. 13-32, 2016.
[37] J. Millán, "A review of WBG power semiconductor devices," in CAS 2012 (International Semiconductor Conference), 15-17 Oct. 2012 2012, vol. 1, pp. 57-66.
[38] J. Tsao et al., "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," Advanced Electronic Materials, $12 / 01$ 2017.

## Appendix [J6]

A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A 1-MHz 1.5-Stage LED Driver with Charge-Pump-Based Power Factor Correction," draft for IEEE Journal of Emerging and Selected Topics in Power Electronics.

# A 1-MHz 1.5-Stage LED Driver with Charge-PumpBased Power Factor Correction 

Ahmed M. Ammar, Student Member, IEEE, Frederik M. Spliid, Student Member, IEEE, Yasser Nour, Senior<br>Member, IEEE, and Arnold Knott

## Corresponding author:

Ahmed M. Ammar
Elektrovej 325, Room 216
2800 Kongens Lyngby, Denmark
Phone: +45 45253697
E-mail: ammma@elektro.dtu.dk


#### Abstract

This paper presents the design and implementation of a 1.5 -stage LED driver. The driver structure comprises a charge-pumpbased power factor correction (PFC) converter and a class-DE dc-dc converter. The PFC converter employs an improved chargepump circuit that achieves PFC inherently. The class-DE converter comprises a series-resonant tank and a high-frequency transformer. Both converters share the same half-bridge and gate-driving circuit. The overall converter operates with zero-voltage switching across the entire load range, allowing for increased switching frequencies with reduced switching losses. A $1-\mathrm{MHz}$ prototype employing wide bandgap (WBG) switching devices is built and tested. The prototype delivers up to 42 W of output power, with a power density of $2 \mathrm{~W} / \mathrm{cm}^{3}$, and achieves a power factor of 0.99 , a total harmonic distortion (THD) of $6 \%$, and an efficiency of $90 \%$ at full load, with harmonic magnitudes well-within the IEC $61000-3-2$ standard limits for class-C devices. Burstmode (on/off) modulation is used for output current regulation between 20 and 900 mA .


## Index Terms

LED drivers, power factor correction, resonant power conversion, charge pump, wide bandgap semiconductors.

[^5]
## I. INTRODUCTION

The majority of current light systems are using high-brightness light-emitting diodes (LEDs) as the light source, for many reasons that include their longer lifetime, higher energy savings, smaller form factors, as well as higher quality and durability compared to other technologies [1][2]. The complete system comprises the electrical part (light engine), the mechanical part (luminaire), and the optical part (reflector and lens). The bottleneck for the size, weight, and cost reduction, as well as higher reliability and efficiency, is the light engine, which consists of an LED module (the LED array and the substrate material it is mounted on) and a driver (electrical engine). While the LED module is responsible for the limit in energy efficacy ( $1 \mathrm{~m} / \mathrm{W}$ ), the driver is the limiting factor for size, weight, cost and reliability.

The conventional solution for LED drivers is a two-stage converter, as shown in Fig. 1, where the first stage is an ac-dc rectifier with power factor correction (PFC) followed by an energy-storage capacitor to filter the double-the-line $100 / 120 \mathrm{~Hz}$ frequency component on the output, while the second stage is a dc-dc converter providing the voltage and current levels that apply to the LED load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current to limit the mains voltage distortion [3][4].

Pulse-width-modulated (PWM) converters have been the primary candidate for both driver stages. They can provide high power factor and efficiency, and are easy to control. However, in addition to the high conducted electromagnetic interference (EMI) from the rectangular waveforms, their operation is based on hard switching. Accordingly, they typically operate at low frequencies in order to limit the switching losses. This, in turn, results in larger sizes for the passive components needed to store and process the power transferred to the load every switching cycle.

Consequently, there is an increasing demand for smaller and highly efficient LED drivers. Through the use of soft-switching circuit topologies, combined with the employment of the state-of-the-art devices, such as wide bandgap semiconductors and highfrequency magnetic materials, circuits can operate at higher switching frequencies, which allows for using smaller passive devices, and thus overall less weight and size for the whole converter.

This paper presents a resonant-converter-based LED driver. The structure, shown in Fig. 2, integrates a charge-pump-based PFC converter and a class-DE converter in a 1.5 -stage architecture, where the semiconductor switches and their driving circuit are shared


Fig. 1. Conventional LED driver structure.


Fig. 2. Proposed LED driver structure.
between both stages. The PFC converter employs an improved charge-pump circuit that achieves PFC inherently, which provides simplicity and freedom from the limited bandwidths of commercially available PFC controllers. The class-DE converter provides the voltage and current scaling for the LED load.

This paper is organized as follows. Section II outlines the principle of operation of the proposed converter. The design flow is illustrated in Section III. Section IV describes the implementation process for a $1-\mathrm{MHz}$ prototype. Experimental results are then shown in Section V. Finally, Section VI concludes the achieved results.

## II. Principle of Operation

## A. Charge-pump PFC Circuit

The use of charge-pump-based technique for PFC applications was reported in the 90 's for the use in electronic ballast circuits [5]-[8]. Fig. 3 shows an equivalent circuit for the charge-pump PFC converter, where a single diode $D_{B}$ represents the input bridge that rectifies the ac mains, and the dc-dc converter stage is modelled with a resistor $R_{D C}$. The variable voltage source $V_{H F}$ is equivalent to a high-frequency voltage node in the converter circuit. The energy-storage capacitor $C_{D C}$ is designed in accordance with the pump capacitor $C_{P}$ such that the voltage $V_{D C}$ is higher than $V_{I N}$ across the entire line cycle, and accordingly the diode bridge $D_{B}$ and the pump diode $D_{P}$ do not cross-conduct. Consequently, the input current is equal to the positive charging current of the pump capacitor.


Fig. 3. Basic charge-pump circuit.


Fig. 4. Charge-pump circuit operation across half a line cycle.
Fig. 4 shows representative waveforms for circuit operation across one half of a line cycle. The pump capacitor is charged and discharged within the rise and fall times of $V_{H F}$, respectively. The capacitor charge $\Delta Q_{P}$ is proportional to the voltage difference across the capacitor $V_{P}$, which varies between a low-frequency high value $V_{P_{\text {_high }}}$ and a constant low value $V_{P_{-} l o w . ~ T h e ~ c i r c u i t ~ d e s i g n ~}^{\text {. }}$ ensures that the charge variation of $C_{P}$, which is proportional to the voltage variation across it ( $V_{P}$ high $-V_{P}$ low), follows the input voltage $V_{I N}$ across the line cycle $(50 / 60 \mathrm{~Hz})$. Accordingly, the average input current follows the input voltage and a unity power factor can ideally be obtained. From circuit analysis, the voltage variation across $C_{P}$ in one switching cycle is evaluated as

$$
\begin{equation*}
\Delta V_{P}=V_{P_{-} \text {high }}-V_{P_{-} \text {low }}=V_{I N}-V_{D C}+\left(V_{H F_{-} \text {high }}-V_{H_{-} \text {low }}\right) \tag{1}
\end{equation*}
$$

From (1), in a converter circuit where the voltage $V_{H F}$ has a peak-to-peak amplitude equal to $V_{D C}$, the voltage variation across the $C_{P}$ becomes equal to the input voltage, and the variation of the pump capacitor charge is calculated as

$$
\begin{equation*}
\Delta Q_{P}=C_{P} \cdot \Delta V_{P}=C_{P} \cdot V_{I N} \tag{2}
\end{equation*}
$$

The pump capacitor charging current, which is equal to the input current, averaged across one switching cycle, is then equal to

$$
\begin{equation*}
I_{I N}=\frac{\Delta Q_{P}}{T_{S}}=f_{s} \cdot C_{P} \cdot V_{I N} \tag{3}
\end{equation*}
$$

Where $f_{s}$ is the converter switching frequency. Therefore, in steady state operation with a constant switching frequency, the input current becomes proportional to the input voltage, and unity power factor can be obtained.

## B. Charge-pump-based Class-DE Series-Resonant Converter

In [9][10], the charge-pump circuit is added to a class-DE series-resonant converter, where the pump capacitor is coupled to the node interfacing the inverter and the rectifier, $V_{R E C}$, as shown in Fig. 5. That results in the sharing of the converter switches and resonant tank between the pump circuit and the dc-dc stage, which reduces the component count and cost. However, that comes


Fig. 5. Charge-pump-based converter reported in [9][10].
with two drawbacks. First, the power factor of the converter becomes dependent on the resonant tank gain, as coupling to the $V_{\text {REC }}$ node results in the following expression for the input current after re-evaluating (1)

$$
\begin{equation*}
I_{I N}=\frac{\Delta Q_{P}}{T_{s}}=f_{s} \cdot \Delta Q_{P}=f_{s} \cdot C_{P} \cdot\left(V_{I N}-V_{D C}+V_{O U T}\right) \tag{4}
\end{equation*}
$$

From (4), it is seen that operation close to resonance with a high resonant tank gain (close to unity) is a condition for eliminating the $V_{O U T}-V_{D C}$ term and achieving a high power factor. Accordingly, with the use of frequency modulation for output voltage/current regulation, low power factor is obtained at low-load operation owing to the lower tank gain. Second, high current stress is imposed on the resonant tank components, as the charge-pump circuit operation entitles the resonant tank to store the energy from the input line as well as the energy to load every switching cycle. That complicates the resonant inductor design and results in limited efficiency.

## C. Splitting the resonant tank

By moving the charge-pump coupling from the $V_{R E C}$ node to the switching node $V_{S W}$, the resonant tank only processes the power to the load and the current stress is reduced. However, the circuit becomes impractical for high-frequency operation, as the charge pump circuit capacitively loads the half-bridge, resulting in loss of ZVS. In addition, the pump capacitor charges and discharges with a low time constant, owing to the low switch on-resistance $R_{d s(o n)}$. That results in high current spikes that can reach tens of amperes through the bridge and pump diodes and switches. Therefore, to allow for operation at high frequencies, an inductor needs to be placed in the input current path to smooth the pump capacitor high-frequency current.

## D. Modified Charge-pump PFC Circuit

Fig. 6 shows the modified charge-pump circuit, where an inductor $L_{P}$ is added in series with the charge pump capacitor $C_{P}$ to
smooth the capacitor current. That, however, results in reduction of the power factor, as the voltage change across the capacitor is no longer equal to the input voltage with the voltage drop across the inductor. To bind the voltage across the capacitor to the input voltage, two clamping diodes $D_{C 1}$ and $D_{C 2}$ are added to clamp $V_{C}$ to a maximum voltage of $V_{D C}$ and minimum voltage of zero [5]. The circuit operation spans six intervals every switching cycle. Fig. 7 shows waveforms for several circuit currents and voltages across two switching cycles, where the circuit and devices parasitics are ignored for simplicity. Fig. 8 shows the equivalent circuits and current paths across the different intervals of operation.

Interval 1 starts once the half-bridge switches, with the high-side switching off and low-side on. The energy stored in the pump


Fig. 6. Modified charge-pump circuit.


Fig. 7. Circuit operation across two switching cycles (patterned areas illustrate the charge flow in the charge-pump capacitor as well as the clamping diodes).


Fig. 8. Equivalent circuits with charge-pump circuit current paths (red dashed arrows) and load current paths (blue dashed arrows) across different intervals of operation. (a) Interval 1, (b) interval 2, (c) interval 3, (d) interval 4, (e) interval 5, and (f) interval 6 equivalent circuits.
capacitor is discharged in $C_{D C} . I_{L P}$ decreases linearly, with the voltage across the pump capacitor decreasing until it reaches zero, while $V_{C}$ keep increasing until it reaches $V_{D C}$. At that point, interval 2 starts, where $D_{C l}$ turns on and $V_{C}$ is clamped to $V_{D C}$, while $I_{L P}$ continues decreasing until it reaches zero. Meanwhile, no current flows in $C_{P}$. Interval 3 starts once the energy in the chargepump tank gets depleted. $D_{C l}$ stops conducting and $D_{B}$ turns on to charge $C_{P}$ by the line input current. This interval terminates when the half-bridge switches again and interval 4 begins. In that interval, the high-side switch is on and the low-side is off. $D_{B}$ continues to conduct until $C_{P}$ is charged to $V_{I N}$, while $V_{C}$ decreases to zero. At that point, interval 5 starts and $D_{C 2}$ turns on, clamping $V_{C}$ to zero. $I_{L P}$ linearly increases as a positive voltage of $V_{D C}$ is applied across it and the interval ends once it reaches zero. Interval 6 then starts, where part of the energy stored in $C_{P}$ is released into $L_{P}$ while the charge-pump tank current freewheels through $D_{P}$ and $Q_{H S}$. By the end of that interval, $Q_{H S}$ turns off, and the next switching cycle begins.

The analysis shows that the ac line input current is discontinuous and equal to the pump capacitor charging current, which is equal to $I_{L P}$ in intervals 3 and 4. In addition, the voltage across the pump capacitor is changing between $V_{I N}$ and zero every switching cycle, as seen in Fig. 7, and accordingly (2) and (3) hold for this circuit and unity power factor is achieved.

## E. Proposed Converter

Fig. 9 shows the proposed converter schematic, where the $R_{D C}$ load in Fig. 6 is replaced with a class-DE resonant converter for the dc-dc stage. The half-bridge switch network and its driving circuit are shared between the two converters, resulting in what can be described as a 1.5 -stage architecture, where the current paths to the PFC and class-DE stages are split from the switching node. Compared to the two-stage conventional architecture, the proposed converter offers lower components count, and thus higher power


Fig. 9. Proposed 1.5 -stage structure, with shared switch network and driving circuit.
density and lower cost. Compared to the prior art in [9][10], by sharing only the switches between the two paths and splitting the single resonant tank into two, the current stress in each tank is reduced and the design of magnetic devices becomes simpler. Additionally, higher design flexibility is achieved for the dc-dc stage that is decoupled from the charge-pump circuit operation, with no dependence of the power factor on the dc-dc stage gain.

## III. Circuit Analysis and Design

## A. Charge-Pump Capacitor Design

The charge pump capacitor needs to be designed for handling the maximum line input current. From (3), the input power averaged over a switching cycle is given by

$$
\begin{equation*}
P_{I N}=V_{I N} \cdot I_{I N}=f_{s} \cdot C_{P} \cdot V_{I N}^{2} \tag{5}
\end{equation*}
$$

Where the input voltage is a sinusoid of the line frequency

$$
\begin{equation*}
V_{I N}=V_{I N_{\_} p k} \sin \left(\omega_{l} t\right) \tag{6}
\end{equation*}
$$

The input power averaged over a line cycle is obtained as follows

$$
\begin{equation*}
P_{\text {IN_avg }}=\frac{1}{T_{l}} \int_{0}^{T_{l}} P_{I N} d t=\frac{2}{T_{l}} \int_{0}^{\frac{T_{l}}{2}} P_{I N} d t \tag{7}
\end{equation*}
$$

With the substitution of (5) and (6) in (7), the integral is evaluated to

$$
\begin{equation*}
P_{I N_{-} a v g}=\frac{1}{2} f_{S} \cdot C_{P} \cdot V_{I N_{-} p k}^{2} \tag{8}
\end{equation*}
$$

Equating to $P_{\text {OUT }} / \eta$ and rearranging for $C_{P}$

$$
\begin{equation*}
C_{P}=\frac{2 P_{\text {OUT }}}{\eta \cdot f_{s} \cdot V_{I N \_p k}{ }^{2}} \tag{9}
\end{equation*}
$$

## B. Charge-Pump Inductor Design

The size of the charge pump inductor determines the length of intervals 2 and 5 in Fig. 7, during which the clamping diodes conduct to clamp the voltage on the charge-pump capacitor and achieve high power factor. A low value for $L_{P}$ results in higher conduction times of the clamping diodes and less efficiency. While a high value for $L_{P}$ results in loss of power factor and high THD. The optimal value of $L_{P}$ is the one that is sized to store the exact energy stored in the pump capacitor, as follows.

$$
\begin{equation*}
\frac{1}{2} C_{P} \cdot V_{P}^{2}=\frac{1}{2} L_{P} \cdot I_{L_{P}}^{2} \tag{10}
\end{equation*}
$$

Assuming a triangular current in the pump circuit, $I_{L P}$ can be calculated from the total charge $Q_{P}$ (area of triangle shown in Fig. 7, assuming $Q_{C}=0$ ) as follows

$$
\begin{gather*}
Q_{P}=C_{P} \cdot V_{P}=\frac{1}{2} \cdot \frac{T_{s}}{2} \cdot I_{L_{P}}  \tag{11}\\
I_{P_{-} p k}=4 \cdot \frac{C_{P} \cdot V_{P}}{T_{s}}=4 \cdot f_{s} \cdot C_{P} \cdot V_{P} \tag{12}
\end{gather*}
$$

Substituting (12) in (10) and arranging for $L_{P}$

$$
\begin{equation*}
L_{P}=\frac{1}{16 \cdot C_{P} \cdot f_{s}^{2}} \tag{13}
\end{equation*}
$$

## C. Energy-Storage Capacitor Design

The energy-storage capacitor needs to store the difference between the instantaneous input power and the constant output power, as follows.

$$
\begin{equation*}
P_{D C}=P_{I N}-P_{O U T} \tag{14}
\end{equation*}
$$

Rewriting (5) as the product of two sinusoids

$$
\begin{equation*}
P_{I N}=V_{I N_{-} p k} \cdot I_{I N_{-} p k} \sin ^{2}\left(\omega_{l} t\right)=\frac{V_{I N_{-} p k} \cdot I_{I N_{\_} p k}}{2}\left[1-\cos \left(2 \omega_{l} t\right)\right] \tag{15}
\end{equation*}
$$

For simplicity, assuming $100 \%$ efficiency, the output power is evaluated to

$$
\begin{equation*}
P_{\text {OUT }}=P_{I N_{\text {avg }}}=\frac{V_{I N_{-} p k} \cdot I_{I N_{-} p k}}{2} \tag{16}
\end{equation*}
$$

Substituting (15) and (16) in (14) gives

$$
\begin{equation*}
P_{D C}=-P_{\text {OUT }} \cos \left(2 \omega_{l} t\right) \tag{17}
\end{equation*}
$$

Finding the energy

$$
\begin{equation*}
E_{D C}=\int_{0}^{T_{l}} P_{D C} d t=E_{D C}(0)-\frac{P_{\text {OUT }} \sin \left(2 \omega_{l} t\right)}{2 \omega_{l}}=\frac{1}{2} C_{D C} \cdot V_{D C}{ }^{2} \tag{18}
\end{equation*}
$$

Rearranging for $V_{D C}$ and knowing that $V_{D C}(0)$ is equal to the rms voltage [11]

$$
\begin{equation*}
V_{D C}=V_{D C_{-} r m s} \sqrt{1-{\frac{P_{O U T}}{\omega_{l} \cdot C_{D C} \cdot V_{D C_{-} r m s}}{ }^{2}}^{2} \sin \left(2 \omega_{l} t\right)} \tag{19}
\end{equation*}
$$

With the ac ripple being sufficiently smaller than the rms voltage, the ripple amplitude can be evaluated by

$$
\begin{equation*}
V_{D C_{\_} \text {ripple }} \approx \frac{P_{\text {OUT }}}{2 \omega_{l} \cdot C_{D C} \cdot V_{D C \_r m s}} \tag{20}
\end{equation*}
$$

The energy-storage capacitor $C_{D C}$ needs to be sized such that the voltage across it is higher than the peak input voltage across the line cycle. That guarantees that no cross-conduction occurs through the diode bridge and the pump diode, and accordingly the input current is forced into the pump circuit that achieves PFC. Accordingly, for a high power factor, the following condition needs to be satisfied.

$$
\begin{equation*}
V_{D C_{-} \text {ripple }}<V_{D C}-V_{I N_{-} p k} \tag{21}
\end{equation*}
$$

By substitution of (21) in (20), rearranging for $C_{D C}$, and considering a conservative substitution of the average voltage for the rms, the sizing of the energy-storage capacitor for a given average bus voltage is found from

$$
\begin{equation*}
C_{D C} \geq \frac{P_{O U T}}{2 \omega_{l} \cdot V_{D C} \cdot\left(V_{D C}-V_{I N \_p k}\right)} \tag{22}
\end{equation*}
$$

## D. Class-DE Stage Design

The design procedure given in [12] based on the first-harmonic approximation (FHA) approach for the analysis and design of resonant converters is used for the class-DE converter design. The procedure starts by the calculation of the load resistance $R_{L}$ referred to the rectifier input, as follows.

$$
\begin{equation*}
R_{R E C}=\frac{8 \cdot R_{L}}{\pi^{2} \cdot n^{2}}=\frac{8 \cdot V_{O U T}^{2}}{\pi^{2} \cdot n^{2} \cdot P_{O U T}} \tag{23}
\end{equation*}
$$

Where $n$ is the transformer turns ratio $\left(N_{S} / N_{P}\right)$. The converter voltage gain is the product of the half-bridge gain $M_{H B}$, the resonant tank gain $M_{R E S}$, and $n$.

$$
\begin{equation*}
M=\frac{V_{O U T}}{V_{D C}}=M_{H B} \cdot M_{R E S} \cdot n \tag{24}
\end{equation*}
$$

Knowing that the half-bridge gain is equal to one half and rearranging to evaluate the required resonant tank gain

$$
\begin{equation*}
M_{R E S}=\frac{2 \cdot V_{O U T}}{n \cdot V_{D C}} \tag{25}
\end{equation*}
$$

The resonant tank gain is the magnitude of the resonant tank transfer function and can be expressed as a function of the loaded quality factor $Q_{L}$ and the normalized switching frequency $f_{n}$ as follows.

$$
\begin{equation*}
M_{R E S}=\frac{f_{n}}{\sqrt{\left[Q_{L} \cdot\left(f_{n}{ }^{2}-1\right)\right]^{2}+f_{n}{ }^{2}}} \tag{26}
\end{equation*}
$$

From the value obtained in (25), and with a proper choice of $Q_{L}$, the normalized switching frequency is obtained from (26). Following, for a specified switching frequency, the resonant frequency and tank components are calculated as follows.

$$
\begin{gather*}
f_{o}=\frac{f_{S}}{f_{n}}  \tag{27}\\
L_{R E S}=\frac{Q_{L} \cdot R_{R E C}}{\omega_{o}}  \tag{28}\\
C_{R E S}=\frac{1}{\omega_{o} \cdot Q_{L} \cdot R_{R E C}} \tag{29}
\end{gather*}
$$

## E. Circuit Stresses

Starting with the energy-storage capacitor, the maximum voltage across the capacitor is equal to the maximum allowed voltage ripple on top of the average value.

$$
\begin{equation*}
V_{D C_{-} \max }=V_{D C}+\left(V_{D C}-V_{I N_{-} p k}\right)=2 \cdot V_{D C}-V_{I N_{\_} p k} \tag{30}
\end{equation*}
$$

With respect to the charge-pump circuit, the voltage stress across the pump capacitor is clamped to the input voltage, and accordingly the voltage stress across the capacitor is

$$
\begin{equation*}
V_{P_{-} \max }=V_{I N_{-} p k} \tag{31}
\end{equation*}
$$

Substituting (31) in (12), the current stress in the pump circuit inductor is

$$
\begin{equation*}
I_{P_{-} \max }=4 \cdot f_{s} \cdot C_{P} \cdot V_{I N_{-} p k} \tag{32}
\end{equation*}
$$

The pump diodes stresses are equal to

$$
\begin{gather*}
V_{D P \_\max }=V_{D C_{\_} \max }  \tag{33}\\
I_{D P_{\_} \max }=I_{P \_\max } \tag{34}
\end{gather*}
$$

Where the clamping diodes are rated for the same voltage as the pump diode, yet for a lower current stress, which depends on the accuracy of the design of the pump inductor.

The class-DE resonant tank components stresses are calculated from the following formula (with a conservative assumption of operation at resonance).

$$
\begin{gather*}
V_{R E S_{-} \max }=\frac{2 \cdot V_{D C_{-} \max } \cdot Q_{L}}{\pi}  \tag{35}\\
I_{\text {RES_max }}=\frac{2 \cdot V_{D C_{-} \max }}{\pi \cdot R_{R E C}} \tag{36}
\end{gather*}
$$

The class-DE stage rectifier diodes stresses are calculated as follows

$$
\begin{gather*}
V_{D R_{-} \max }=V_{\text {OUT }}  \tag{37}\\
I_{D R_{-} \max }=\frac{\pi \cdot I_{\text {OUT }}}{2}=\frac{\pi \cdot P_{\text {OUT }}}{2 \cdot V_{\text {OUT }}} \tag{38}
\end{gather*}
$$

The voltage stress across the half-bridge switches and the energy storage capacitor is calculated

$$
\begin{equation*}
V_{S_{-} \max }=V_{D C_{-} \max } \tag{39}
\end{equation*}
$$

While the current in the switches is equal to the sum of the pump-circuit inductor and the class-DE resonant tank currents. With a conservative assumption of zero phase difference between the two currents, the current stress in the switches is equal to

$$
\begin{equation*}
I_{S_{-} \max }=I_{P_{-} \max }+I_{\text {RES_} \max } \tag{40}
\end{equation*}
$$

## F. Achieving ZVS Operation

Assuming operation at the class-DE stage tank resonant frequency, the resonant tank voltage gain is unity. Substituting that in (25) gives the following expression for the turns ratio

$$
\begin{equation*}
n=\frac{2 \cdot V_{\text {OUT }}}{V_{D C}} \tag{41}
\end{equation*}
$$

Substituting (23) and (41) in (36) gives

Table I. LED Driver Design Specifications

| Input Voltage | $230 \mathrm{~V}_{\mathrm{rms}}$ |
| :---: | :---: |
| Line Frequency | 50 Hz |
| Output Power | 40 W |
| Output Voltage | 45 V |
| Power Factor | $>0.9$ |
| THD | $<10 \%$ |
| Efficiency | $>90 \%$ |
| Switching Frequency | 1 MHz |

$$
\begin{equation*}
I_{\text {RES_max }}=\frac{\pi \cdot P_{O U T}}{V_{D C}} \tag{42}
\end{equation*}
$$

By dividing (32) by (42) and substitution of (9)

$$
\begin{equation*}
I_{P_{-} \max }=\frac{8 \cdot V_{D C_{\_} \max }}{\eta \cdot \pi \cdot V_{I N_{-} p}} \cdot I_{R E S_{-} \max } \tag{43}
\end{equation*}
$$

With a conservative assumption of $V_{D C_{-} \max }$ being equal to $V_{I N \_p k}$ and $100 \%$ efficiency, the pump-circuit branch current amplitude is at least 2.5 times the class-DE stage branch current amplitude. Accordingly, the pump-circuit branch current is the one defining the criteria for achieving ZVS operation for most of the line cycle. From (9) and (13), the resonant frequency of the pump-circuit tank can be obtained as follows.

$$
\begin{equation*}
f_{P}=\frac{1}{2 \cdot \pi \cdot \sqrt{L_{P} \cdot C_{P}}}=\frac{2 f_{s}}{\pi} \tag{44}
\end{equation*}
$$

Accordingly, the switching frequency is sufficiently higher than the pump tank resonant frequency, which goes in accordance with the assumption of the triangular pump inductor current shown in Fig. 7, and results in inductive-mode of operation for the pump circuit branch and ZVS operation is achieved.

## IV. 1-MHz PRototype

## A. Design Specifications

Table I lists the specifications for the designed prototype, which is proposed for LED drivers supplied from European mains for low-mid power applications. A switching frequency of 1 MHz is specified for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. An output voltage of 45 V is common for LED modules in the specified power range.

## B. Prototype Design Procedure

From the design specifications, the design process starts by the design of the energy-storage capacitor using (22) and (30). The charge-pump circuit is then designed using (9) and (31) for the pump capacitor, (13) and (32) for the pump inductor, and (33) and (34) for the pump diode. Following, the class-DE stage design takes place using (28)-(29) and (35)-(38). Eventually, the shared half-bridge switches stresses are calculated from (39)-(40).

The choice of the loaded quality factor $Q_{L}$ for the class-DE stage constitutes a trade-off between accuracy and implementation complexity. A higher $Q_{L}$ guarantees a more sinusoidal resonant tank current with lower harmonic content, and thus additional validity for the design equations based on the FHA approach. However, it complicates the magnetic devices design with the need for a higher value for the resonant inductor. In this work, a low $Q_{L}$ value is chosen in order to enable the integration of the resonant inductor into the transformer through the transformer leakage inductance. That results in the reduction of component count and increased power density. Table II lists the obtained design values according to the specifications given in Table I, with a loaded quality factor of 0.3 and a transformer turns-ratio of $4: 1$ for the class-DE stage, and assuming 360 V for $V_{D C}$ and $95 \%$ efficiency.

## C. Implementation

Fig. 10 shows a photograph of the implemented prototype. The converter is assembled on a four-layer printed circuit board, which is mounted on a test-bench board with terminals for testing. Because of the charge-pump circuit operation, a high-frequency ac current runs through the input bridge, which is implemented using four fast-recovery diodes. Gallium nitride (GaN) FET switches are employed for the half-bridge, as they show superior performance over the silicon and silicon carbide ( SiC ) counterparts for that voltage range. SiC Schottky diodes are employed for the pump circuit diodes, namely $D_{P}, D_{C 1}$, and $D_{C 2}$. They show higher efficiency compared with the silicon high-voltage alternatives. On the other hand, silicon Schottky diodes are employed in the high-frequency

Table II. Design Values Calculated from Circuit Analysis Equations

| Parameter | Calculated |
| :---: | :---: |
| $C_{D C}$ min | $6.32 \mu \mathrm{~F}$ |
| $V_{D C}$ max | 395 V |
| $C_{P}$ | 0.99 nF |
| $V_{P}$ | 325.3 V |
| $L_{P}$ | $63.13 \mu \mathrm{H}$ |
| $I_{L P}$ | 1.29 A |
| $V_{D P \text { max }}$ | 395 V |
| $I_{D P \text { max }}$ | 1.29 A |
| $L_{R E S}$ | $25.08 \mu \mathrm{H}$ |
| $C_{R E S}$ | 1.01 nF |
| $V_{R E S \text { max }}$ | 75.44 V |
| $I_{R E S}$ max | 0.48 A |
| $V_{D R \text { max }}$ | 45 V |
| $I_{D R \text { max }}$ | 1.75 A |
| $V_{S_{\text {max }}}$ | 395 V |
| $I_{S_{\text {max }}}$ | 1.77 A |



Fig. 10. Prototype Picture.
rectifier full bridge. Table III shows a breakdown of the incorporated power stage bill-of-materials (BoM) for the proposed converter.

A half-bridge gate driver (Si8274 by Silicon Labs, Austin, TX, USA) drives the half-bridge switches. The dead time is set using a fixed resistor and adjusted to achieve ZVS with minimal reverse-conduction through the switches. The gate driver package is placed adjacent to the devices gate terminal in order to control noise coupling from the power loop to the gate-drive loop. Another layout consideration taken is the separation of the source terminal to the gate-driving and power loops in a star-connected fashion, which is allowed with the source-sense pad of the GS-065-004-1-L device package. That helps alleviate the gate ringing resulting from the common-source inductance. The driving signal is generated from a voltage controlled oscillator (LTC6990 by Analog Devices) and the $1-\mathrm{MHz}$ frequency is set by fixed resistors.

It should be noted that the effect of switching frequency modulation on both stages is not monotonic. An increase in $f_{s}$ leads to higher input power, as per (3). On the other hand, the higher $f_{s}$ is, the lower the resonant tank gain for the dc-dc stage, and accordingly lower output power. The difference in the input and output powers can lead to a stress on the energy-storage capacitor if not modeled. Accordingly, switching frequency modulation is not preferable for this architecture, and burst-mode operation prevails. To enable dimming functionality, a $20-\mathrm{kHz}$ PWM signal is applied to the gate driver enable input for on/off modulation of the converter,

Table III. Prototype power-stage BoM.

| Component | Prototype | Type |
| :---: | :---: | :---: |
| $L_{I N}$ | $100 \mu \mathrm{H}$ | Inductor |
| $C_{I N}$ | $2 * 15 \mathrm{nF}$ | Ceramic |
| Diode Bridge | $4 * \mathrm{ESH1GM} \mathrm{RSG}$ | Si Fast Recovery |
| $C_{D C}$ | $1 \times 10 \mu \mathrm{~F}$ | Electrolytic |
|  | $2 \times 0.1 \mu \mathrm{~F}$ | Ceramic |
| $D_{P,} D_{C 1}, D_{C 2}$ | GB01SLT06-214 | SiC Schottky |
| $C_{P}$ | $1 \times 470 \mathrm{pF}$ | Ceramic (C0G) |
|  | $1 \times 560 \mathrm{pF}$ | Ceramic (C0G) |
| $L_{P}$ | $68 \mu \mathrm{H}$ | Custom design |
| $Q_{H S,} Q_{L S}$ | GS-065-004-1-L | GaN Switches |
| $C_{R E S}$ | $3 \times 330 \mathrm{pF}$ | Ceramic (C0G) |
| $L_{R E S}$ | $26 \mu \mathrm{H}$ | Custom design |
| $D_{R 1}-D_{R 4}$ | PMEG60T20ELP | Si Schottky |
| $C_{O U T}$ | $1 \times 100 \mu \mathrm{~F}$ | Electrolytic |
|  | $2 \times 1 \mu \mathrm{~F}$ | Ceramic |

where the output power is modulated using the PWM signal duty-cycle. To suppress the PWM signal noise on the input current, an LC filter of $10-\mathrm{mH}$ choke and $100-\mathrm{nF}$ shunt capacitor is incorporated on the test-bench board.

Custom magnetic components are implemented for the charge-pump circuit inductor $L_{P}$ and the class-DE converter transformer. The 3F46 material from Ferroxcube is selected for both devices, as it has low losses at the design switching frequency. EFD 15/8/5 cores are used for both devices. The class-DE converter transformer primary and secondary windings are divided between the core halves and separated in order to achieve a low coupling coefficient, which enables the integration of the resonant tank series inductance $L_{R E S}$ in the transformer leakage inductance, thus saving the space and cost for an additional magnetic device. The magnetic components small-signal characterization is conducted using a $40 \mathrm{~Hz}-110 \mathrm{MHz}$ precision impedance analyzer (Agilent Technologies 4294A). At 1 MHz , an inductance of $68 \mu \mathrm{H}$ and ESR of $0.7 \Omega$ are measured for the pump circuit inductor $L_{P}$, whereas a total primary side inductance of $139 \mu \mathrm{H}$ and an ESR of $1.5 \Omega$ are obtained for the class-DE transformer, with $26 \mu \mathrm{H}$ measured leakage inductance used towards the resonant tank inductance $L_{\text {RES }}$. A secondary side inductance of $7.2 \mu \mathrm{H}$ is measured, which results in an effective transformer turns ratio of 3.96:1.

## D. Experimental Results

The converter is tested for operation from $230 \mathrm{~V}_{\mathrm{rms}}$ across the burst signal duty-cycle modulation between 1-100 \%. The prototype is loaded with an industrial LED lamp (RRC03645-01 by ROBUS) with 105 LEDs connected in a $7 \times 15$ array. Fig. 11 shows the obtained results across operational range. The prototype delivers up to 42 W of output power. The reduced output power at 1 MHz is the result of offsets in components implemented values compared to calculations, and increased by increasing the pump capacitor size or the switching frequency. The efficiency across the output power range is shown in Fig. 11(a), where a peak efficiency of $90.4 \%$ is achieved at full-load, with an efficiency of $88 \%$ at half-load. The figure also shows the correspondent burst signal duty cycle across the load range. Fig. 11(b) shows the output voltage and current across the operational range, where an output current range of $20-900 \mathrm{~mA}$ is achieved with an almost linear dependence on the burst signal duty-cycle, which simplifies the dimming control and enables the fine-tuning of the current with a PWM burst signal of high resolution. The power quality results are shown in Fig. 11(c), where a power factor higher than 0.98 and a THD lower than $10 \%$ are obtained across the power range where power factor correction is demanded by the IEC 61000-3-2 standard for class-C devices.

Fig. 12 shows scope captures for the implemented prototype waveforms at full-load operation. Fig. 12(a) shows the linefrequency waveforms, including the input voltage and current, output voltage and the voltage across the energy-storage capacitor $C_{D C}$. The input and output voltages are measured using high-voltage differential probes (Testec SI 9001), the input current using a $50-\mathrm{MHz}$ current probe (LeCroy AP015), while the dc capacitor voltage is measured using a $500-\mathrm{MHz} 10 \mathrm{x}$ voltage probe with $9-\mathrm{pF}$
capacitance. The figure shows an almost-sinusoidal input current in phase with the input voltage, and an average output voltage of 47 V. Fig. 12(b) shows the switching-frequency signals at full-load operation. The pump-circuit inductor and transformer-secondary currents are measured using 50-MHz current probes (LeCroy CP030 and AP015, respectively). The transformer-secondary current is seen to be sinusoidal owing to the operation at resonance, thus ensuring the validity of the design process of the class-DE stage


Fig. 11. Obtained prototype measurements across operational range. (a) Output power and efficiency. (b) Output voltage and current. (c) Power factor and input current THD.


Fig. 12. Scope images for the implemented prototype waveforms at full-load operation. (a) Line-frequency waveforms ( $100 \mathrm{~V} / \mathrm{div}, 200 \mathrm{~mA} / \mathrm{div}$, with 5 $\mathrm{ms} /$ div). (b) Switching-frequency waveforms ( $100 \mathrm{~V} / \mathrm{div}, 1 \mathrm{~A} / \mathrm{div}$, with $200 \mathrm{~ns} / \mathrm{div}$ ).
which is based on the FHA approach. On the other hand, the pump-circuit inductor current is seen to be triangular, as the switching frequency is considerably higher than the charge-pump tank resonant frequency. The pump inductor current has an amplitude that is larger than the class-DE resonant tank current primary, which is $1 / n$ times the transformer secondary current. The switching-node voltage waveform $V_{S W}$ is measured using a $500-\mathrm{MHz} 10 \mathrm{x}$ voltage probe with $9-\mathrm{pF}$ capacitance. The figure shows that the pumpcircuit current is lagging the switching-node voltage, and accordingly full ZVS is obtained.

Fig. 13 shows scope captures for the implemented prototype waveforms at half-load operation. Fig. 13(a) shows a reduced input current amplitude, while the current is still proportional to and in phase with the input voltage, resulting in high power factor. Fig. 13(b) shows the high-frequency waveforms with an extended time scale to show the switching-frequency pulse skipping respective to the burst-signal duty-cycle of $50 \%$.

(a)

(b)

Fig. 13. Scope images for the implemented prototype waveforms at half-load operation. (a) Line-frequency waveforms ( $100 \mathrm{~V} / \mathrm{div}, 200 \mathrm{~mA} / \mathrm{div}$, with 5 $\mathrm{ms} /$ div). (b) Switching-frequency waveforms ( $100 \mathrm{~V} / \mathrm{div}, 1 \mathrm{~A} / \mathrm{div}$, with $50 \mu \mathrm{~s} / \mathrm{div}$ ).

Fig. 14 shows the input current harmonics distribution at full- and half-load operations against the IEC 61000-3-2 standard classC device limits, where THD figures of $6 \%$ and $9 \%$ are measured, respectively. It is shown that the measured harmonics magnitudes are well within the limits set by the standard across the load range.

Table IV shows a comparison of the proposed work with the prior art reported in [9][10]. It is seen that the power factor and THD figures for both converters are within close proximity at full-load operation. However, the prior art converter offers less power factor and higher THD at half-load than the proposed 1.5-stage structure. Another key performance indicator is the efficiency, where a peak efficiency of $90 \%$ is achieved at full-load by the proposed converter, which is the main outcome of splitting the current paths and reducing the stress on the resonant tank. Furthermore, although the prior art converter has lower component count, it offers a much higher output voltage, which is dictated by the criteria to achieve high power factor, and a high-frequency transformer


Fig. 14. Input current harmonics distribution at half- and full-load operation.
and possibly a bridge rectifier needs to be incorporated to achieve a lower output voltage. The proposed converter offers more flexibility for the dc-dc stage as well as easier ZVS maintenance.

## V. CONCLUSION

A 1.5-stage LED driver is presented. The system incorporates an improved charge-pump PFC converter with inherent PFC capability, and a class-DE converter. Both converters share the same switch network and gate-driving circuit. Compared to prior art, the proposed architecture offers lower circuit stresses and high efficiency, in addition to higher flexibility with low components count. Furthermore, the operation is based on soft switching, allowing for increased switching frequencies and higher power densities. A 1-MHz prototype is built and tested. The prototype achieves up to 42 W of power, with a power density of $2 \mathrm{~W} / \mathrm{cm}^{3}$, power factor of 0.99 , a THD of $6 \%$, and an efficiency of up to $90 \%$, with harmonic magnitudes well-within the limits of the IEC 61000-3-2 standard. The proposed converter has the potential for operation at higher frequencies, as all of the circuit components scale with the switching frequency (other than the dc capacitor size, which is dictated by the $50-/ 60-\mathrm{Hz}$ standard line frequency).

Table IV. Comparison with Prior Art

| Reference |  | $[10]$ | This work |
| :---: | :---: | :---: | :---: |
| Input Voltage [ $\mathrm{V}_{\mathrm{ms}}$ ] |  | 230 | 230 |
| Output Power [W] |  | 50 | 42 |
| Output voltage [V] |  | 300 | 45 |
| Power Factor | FL | 0.99 | 0.99 |
|  | HL | 0.95 | 0.98 |
| THD [\%] | FL | 8.6 | 6 |
|  | HL | 18 | 9 |
| Efficiency [\%] | FL | 84 | 90 |
|  | HL | 88 | 88 |
| Switching freq. [kHz] |  | 1000 | 1000 |
| PFC Control |  | Inherent | Inherent |
| Oumber of Components |  | 17 | 23 |
| Output Power Control |  | Switching- <br> Frequency <br> Modulation | On/Off operation |

## References

[1] Y. Wang, J. M. Alonso and X. Ruan, "A Review of LED Drivers and Related Technologies," in IEEE Transactions on Industrial Electronics, vol. 64, no. 7, pp. 5754-5765, July 2017.
[2] S. Li, S. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui and C. K. Tse, "A Survey, Classification, and Critical Review of Light-Emitting Diode Drivers," in IEEE Transactions on Power Electronics, vol. 31, no. 2, pp. 1503-1516, Feb. 2016.
[3] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[4] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[5] W. Chen, F. C. Lee and T. Yamauchi, "An improved "charge pump" electronic ballast with low THD and low crest factor," in IEEE Transactions on Power Electronics, vol. 12, no. 5, pp. 867-875, Sept. 1997.
[6] Jinrong Qian, F. C. Lee and T. Yamauchi, "Charge pump power-factor-correction dimming electronic ballast," in IEEE Transactions on Power Electronics, vol. 14, no. 3, pp. 461-468, May 1999.
[7] J. Qian, F. C. Lee and T. Yamauchi, "Analysis, design and experiments of a high power factor electronic ballast," Proceedings of APEC 97 - Applied Power Electronics Conference, Atlanta, GA, USA, 1997, pp. 1023-1029 vol.2.
[8] Jinrong Qian, F. C. Lee and T. Yamauchi, "Analysis, design, and experiments of a high-power-factor electronic ballast," in IEEE Transactions on Industry Applications, vol. 34, no. 3, pp. 616-624, May-June 1998.
[9] A. M. Ammar, F. M. Spliid, Y. Nour and A. Knott, "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-5.
[10] A. M. Ammar, F. M. Spliid, Y. Nour and A. Knott, "Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
[11] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, ${ }^{\text {nd }}$ edition. Kluwer Academic Publishers, 2001.
[12] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd edition. Wiley-IEEE Press, 2011.

## Appendix [J7]

C. K. Lumby, A. M. Ammar, Y. Nour, and A. Knott, "Switched-Capacitor Current Multiplier Front-End Converter for Power Factor Correction Applications," letter draft for IEEE Journal of Emerging and Selected Topics in Power Electronics.

# Switched-Capacitor Current Multiplier Front-End Converter for Power Factor Correction Applications 

Christian Kaalø Lumby, Member, IEEE, Ahmed Morsi Ammar, Student Member, IEEE, Yasser Nour, Senior Member, IEEE, Arnold Knott


#### Abstract

Universal power factor correction circuits must operate with a wide range of input voltages, which limits their optimization abilities. A switched-capacitor current multiplier frontend is proposed to greatly reduce the power factor correction circuit's input voltage range and allow for better optimization. The proposed front-end operates in open-loop and has negligible effect on the power factor correction circuit control scheme, which enables easy integration with pre-existing circuit designs. The front-end's effect on system power factor is determined through circuit analysis. A 50 W prototype intended for LED lighting applications is implemented to experimentally validate the proposed system architecture. The switched-capacitor converter by itself obtained a power factor of 0.99 . A power factor of 0.94 is achieved with cascading the front-end switched-capacitor by a boost PFC converter designed designed for US main and producing a stable 200 V output DC Bus voltage. Excellent correlation between calculated and measured performance is observed.


Index Terms-Switched-Capacitor, Current Multiplier, Power Factor Correction

## I. INTRODUCTION

POWER factor correction (PFC) in AC-DC power converters is required in many applications. In the case of lighting equipment, the EN 61000-3-2 standard specifies power factor ( PF ) and input current harmonics requirements for $>25 \mathrm{~W}$ rated solutions. At such low-power levels, the PFC circuit is often a limiting factor for power density of the overall system.
Two stage AC-DC architectures are dominating the LED systems whenever precise dimming is required. This is mainly due to the usage of a dedicated PFC rectifier which generates a regulated DC bus voltage which simplifies the DC-DC downstream converters function of controlling the output power.

Pulse width modulated converters are widely used as a PFC stage in offline converters. Several topologies encountered a lot of advancement during the last decade. Boost converters are the most commonly employed topology in many applications [1], [2]. Moreover, several research efforts have been reported based on buck [3]-[6], buck-boost [7], [8], flyback [9], and SEPIC [10], [11] converters. Resonant PFC converters have been given a considerable attention mainly due to their abilities to operate a significantly higher switching frequencies and achieving high power densities [12]. The common power

This project has received funding from the European Unions Horizon 2020 research and innovation programme under grant agreement No 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark
Corresponding Author: Yasser Nour (ynour@elektro.dtu.dk)
density limiting factor of the aforementioned topologies whenever it is applied in universal mains- is the complicated design optimization of the main energy storing elements.
Recent research [13]-[15] show the potential of utilizing SC based converters for high power density PFC circuits. However, these design concepts require many switching elements and impose challenges in combining traditional PFC control schemes with charge balancing of capacitors. Therefore, these approaches are not suitable for low power designs, where component count by itself quickly becomes the limit for power density. In contrast, the SC converter in the proposed topology uses only four switches and operates without control feedback.
Furthermore, universal offline power converters suffer from variation of input RMS voltages ranging from 100 V to 240 V . As a result, universal PFC circuits must handle approximately double current or double voltage for the same power transfer at either of the input condition extremes compared to the opposite extreme. This variation makes it impossible to optimize key power processing components, which lead to bulky circuit implementations. In this work, we present a system architecture to reduce the voltage/current stress variation for a PFC circuit through the use of a switched-capacitor (SC) converter as a front-end stage for the PFC circuit.

## II. Proposed Concept

The proposed architecture uses a SC front-end to lower the input voltage of a PFC circuit in the case of high AC line voltage. In the case of low AC line voltage, the SC converter is instead bypassed using its internal switches. The system is illustrated in Fig. 1. Using a 2:1 voltage step-down SC converter, this topology limits the maximum PFC circuit input RMS voltage to be $240 \mathrm{~V} / 2=120 \mathrm{~V}$. The range of PFC circuit input voltages is therefore greatly reduced compared to the conventional universal single PFC stage solution. Furthermore, the PFC circuit output voltage, which is usually around 400 V for a boost converter PFC, can be halved to 200 V and thereby reduce the voltage stress of the following DC-DC converter. Finally, control of the PFC circuit is simplified due to the reduced input voltage range, and a properly designed frontend SC can in principle be added to any pre-existing PFC circuit without modification.

To analyze the effect of the front-end SC converter on the circuit PF, the simplified schematic in Fig. 2 is utilized. It is well-known that a SC converter can be modelled as a DC-DC transformer with an output resistance that is dependent on the converter design and operation [16], [17]. For this analysis,
an ideal converter with $100 \%$ efficiency is assumed, i.e. the output resistance is set to zero. The total effective capacitance $C$ seen at the output of the SC converter is included in the circuit, and the resistor $R_{p f c}$ models the load of the following PFC stage. The forward drop of the bridge diodes is assumed insignificant, but a series resistance is included, since it is useful for the subsequent mathematical analyses.
For large values of $C$, the circuit operates with narrow current pulses at the line voltage peak similar to the operation of a simple peak-detection rectifier using a diode bridge and bulk capacitor, as the current only flows when the input voltage is higher than the voltage across the capacitor. For small values of $C$, the current waveform approaches that of a purely resistive load, as $v_{a c}$ is higher than $v_{c}$ across the entire line cycle. An intermediate effective capacitance cause the circuit to operate with the input and output current and voltage waveforms shown in Fig. 3. During the interval $\phi_{1} \rightarrow \phi_{2}$, the diode bridge is conducting and the output voltage is scaled to half the input voltage by the SC converter. During the interval $\phi_{2} \rightarrow \pi+\phi_{1}$, the diodes are reverse biased and the output voltage is an exponential decay with the time constant $\tau=R_{p f c} C$, and a dead angle is introduced to the input current waveform. The following analysis considers the boundaries between these two operating modes to determine the angles $\phi_{1}$ and $\phi_{2}$, which will accordingly determine the harmonic content in the input current.

## A. Conduction Boundaries

First, the rectifier diodes are assumed to be conducting. The differential equation (1) is constructed to describe the current delivered to the PFC stage. A cosine is used for the ac source, as this simplifies the following derivation.

$$
\begin{align*}
\frac{v_{c}(t)}{R_{p f c}} & =2 i_{\text {rect }}(t)-C \frac{d v_{c}(t)}{d t}  \tag{1}\\
& =2 \frac{v_{a c} \cos (\omega t)-2 v_{c}(t)}{R_{\text {rect }}}-C \frac{d v_{c}(t)}{d t}
\end{align*}
$$



Fig. 1. Proposed system topology. The SC front-end is used with high input voltages and bypassed through internal switches for low input voltages.


Fig. 2. Simplified circuit schematic for power factor analysis.

This equation is solved using the initial condition $v_{c}(0)=v_{a c}$, yielding the result in (2).

$$
\begin{gather*}
v_{c}(t)=\left(v_{a c}-a b\right) e^{-a t}+a b \cos (\omega t)+b \omega \sin (\omega t) \\
a=\left(R_{\text {rect }}+4 R_{p f c}\right) /\left(R_{\text {rect }} R_{p f c} C\right)  \tag{2}\\
b=2 v_{a c} /\left(R_{\text {rect }}\left(\omega^{2}+a^{2}\right) C\right)
\end{gather*}
$$

Utilizing the reasonable assumptions $R_{r e c t} \ll R_{p f c}$ and $R_{\text {rect }} C \ll 1$, it follows directly that $a \gg 1$. Equation (2) can therefore be simplified to (3).

$$
\begin{equation*}
v_{c}(t) \approx a b \cos (\omega t)+b \omega \sin (\omega t) \tag{3}
\end{equation*}
$$

When the capacitor voltage of (3) is equal to half the ac line voltage, as expressed in (4), the boundary between sinusoidal and exponentially decaying capacitor voltage is found.

$$
\begin{equation*}
a b \cos (\phi)+b \omega \sin (\phi)=\frac{v_{a c}}{2} \cos (\phi) \tag{4}
\end{equation*}
$$

From this equation an expression for the angle $\phi_{2}$ can be obtained, which is given in (5). Note that $\phi_{2}$ is the solution to (4) plus an additional $\pi / 2$, since a cosine was used in (1), while the angle $\phi_{2}$ is defined referenced to a sine, see Fig. 3.

$$
\begin{align*}
\phi_{2} & =\arctan \left[\left(v_{a c}-2 a b\right) /(2 b \omega)\right]+\pi / 2 \\
& \approx \arctan \left[\left(\omega R_{p f c} C\right)^{-1}\right]+\pi / 2 \tag{5}
\end{align*}
$$

The approximation in (5) is valid for an ideal diode rectifier with zero series resistance, i.e. $R_{\text {rect }}=0$.
Following the transition from sinusoidal to decaying voltage waveform after time $\phi_{2}$, the output voltage is given by (6), in which the time $t$ is referred to the transition point $\phi_{2}$.

$$
\begin{equation*}
v_{c}(t)=\frac{v_{a c}}{2} \sin \left(\phi_{2}\right) e^{-t /\left(R_{p f c} C\right)} \tag{6}
\end{equation*}
$$

The boundary $\phi_{1}$ where the rectifier diodes begin to conduct can be found by solving (7).

$$
\begin{gather*}
\frac{v_{a c}}{2} \sin \left(\phi_{2}\right) e^{-t_{1} /\left(R_{p f c} C\right)}=-\frac{v_{a c}}{2} \sin \left(\omega t_{1}+\phi_{2}\right)  \tag{7}\\
t_{1}=\left(\phi_{1}-\phi_{2}+\pi\right) / \omega
\end{gather*}
$$

Using the small angle approximation $\sin \left(\phi_{1}\right)=\phi_{1}$, it can be shown that $\phi_{1}$ is approximated by (8), where $W_{0}$ is the principal branch of the Lambert W function.

$$
\begin{equation*}
\phi_{1} \approx W_{0}\left(\frac{\sin \left(\phi_{2}\right) e^{\left(\phi_{2}-\pi\right) /\left(\omega R_{p f c} C\right)}}{\omega R_{p f c} C}\right) \omega R_{p f c} C \tag{8}
\end{equation*}
$$

Note that the expressions (5) and (8) describing $\phi_{2}$ and $\phi_{1}$ respectively, are only functions of the effective capacitance seen at the output of the SC converter, the equivalent load resistance of the PFC circuit and the line frequency.

## B. Power Factor

The total system PF is of course the ratio of active to apparent power as seen from the AC supply, which is given by (9).

$$
\begin{equation*}
P F=P_{i n, a v g} /\left(v_{a c, r m s} i_{a c, r m s}\right) \tag{9}
\end{equation*}
$$

From the schematic in Fig. 2 and the current waveform in Fig. 3 , it is identified that the AC current is described by (10), in


Fig. 3. Voltage and current waveforms for power factor analysis.


Fig. 4. Implemented two-phase $2: 1$ switched-capacitor converter schematic. The switch pairs $Q_{1}-Q_{3}$ and $Q_{2}-Q_{4}$ conduct in anti-phase.
which the capacitor voltage $v_{c}(t)=\left|v_{a c} / 2 \sin (\omega t)\right|$ for the time interval of non-zero AC current.

$$
\begin{align*}
\left|i_{a c}(t)\right| & =\frac{1}{2}\left(C \frac{d v_{c}(t)}{d t}+\frac{v_{c}(t)}{R_{p f c}}\right) & , \phi_{1}+n \pi<\omega t<\phi_{2}+n \pi \\
i_{a c} & =0 & , \text { otherwise } \tag{10}
\end{align*}
$$

From the symmetry of the positive and negative halves of the periodic current waveform, the instantaneous and RMS value of the AC current can be determined. Assuming the AC voltage to be sinusoidal, it is therefore straight forward to calculate the PF in (9) for a given AC voltage, output load and effective capacitance.

## C. Effective Capacitance

The SC converter's effective output capacitance is a weighted sum of its input, output and flying capacitance. The output capacitance add directly to the effective capacitance, while the input capacitance is scaled by the squared 'turns ratio' of the DC transformer i.e. the ideal SC conversion ratio. The effect of the flying capacitance can in general be dependent on the topology and operation of the SC converter. In this work, a two-phase $2: 1$ conversion ratio SC as shown in 4 have been implemented. For this topology the flying capacitance adds directly to the effective capacitance, and (11) is therefore the expression for calculation of effective capacitance.

$$
\begin{equation*}
C=C_{o u t}+\alpha_{s c} C_{f l y}+C_{\text {in }} / N^{2}=C_{o u t}+C_{f l y}+C_{\text {in }} / 4 \tag{11}
\end{equation*}
$$

## III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A high PF SC converter is designed for nominal EU mains input ( $50 \mathrm{~Hz}, 230 \mathrm{~V}_{\mathrm{rms}}$ ) and 50 W output power. The calculated relation between capacitance, power factor and current displacement for this specification ${ }^{1}$ is shown in Fig. 5. The current displacement is calculated from the first harmonic of the Fourier series decomposition of (10). As expected, higher values of effective capacitance cause an increase in current displacement and decrease in PF.
In order to show that the SC converter can be designed to have negligible affect on power factor, the goal of this work was to obtain a power factor greater than 0.99 . From Fig. 5 it is seen that such performance is expected with effective capacitance lower than $1.6 \mu \mathrm{~F}$. The circuit in Fig. 4 was implemented using the components in Table I. The PCB is shown in Fig. 6, and the converter is switched at 270 kHz . An input filter constructed from a $100 \mu \mathrm{H}$ inductor in series with the ac line and 30 nF of capacitance in parallel to the diode bridge ac input was also added to reduce high frequency switching noise.
The measured line voltage and current as well as the output voltage of the SC converter loaded with a resistive load is shown in Fig. 7. The current waveform is sinusoidal with a small dead angle around the voltage zero crossing as expected. The performance was quantified using a Newtons4th PPA5530 power analyzer at half and full power with the results in Table II. The 50 W metrics are marked with circles in Fig. 5, and good agreement between calculated and measured performance is observed.

To further validate the developed model, $C_{f l y}$ was increased using $1 \mu \mathrm{~F}$ class II capacitors, since class I capacitors became impractically large, and PF was again measured. These results are also marked in Fig. 5 with their effective capacitance corrected for capacitance decrease due to voltage bias at the transition time $\phi_{2}$. Even though the calculations assume ideal capacitors, the model and measurements are well correlated.
${ }^{1}$ Output power varies from 49.9 W 50.4 W in the plotted range, since the RMS output voltage of the SC converter increases when $\phi_{2}$ decreases.


Fig. 5. Power factor and displacement angle (leading) for the fundamental component of the input current with $v_{a c}=230 \mathrm{~V}_{\mathrm{rms}}, f_{a c}=50 \mathrm{~Hz}$ and $R_{p f c}=265 \Omega$ (i.e. $P_{\text {out }} \approx 50 \mathrm{~W}$ ). The solid lines show calculated values from the derived equations. The markers are measured values. The encircled markers are the 50 W results from Table II.


Fig. 6. Implementation of the switched-capacitor converter using class I capacitors for $C_{f l y}$. The utilized circuit area inside the rectangle is $32 \mathrm{~mm} \times 18 \mathrm{~mm}$ and is significantly reduced by using class II capacitors.


Fig. 7. Measured voltage and current from the AC supply and output voltage of the switched-capacitor converter. Output power is 50 W .

Finally, the SC converter is cascaded with a conventional PFC boost converter to verify the complete system functionality. The boost converter is based on a reference design [18] for the Texas Instruments UCC28056 controller and slightly modified to give an output voltage of 210 V . Measured current and voltage waveforms for the complete system are shown in Fig. 8. The 50 W system performance is summarized in Table III.

The current displacement is only slightly affected by the addition of the boost converter as seen from the high fundamental PF. However, the boost converter contributes a significant amount of distortion, which lowers the overall PF. Likewise,

TABLE I
KEY COMPONENTS USED FOR IMPLEMENTATION OF SWITCHED-CAPACITOR CONVERTER

|  | Manufacturer \& Part no. | Description | Amount |
| :---: | :--- | :---: | :---: |
| $Q_{1-4}$ | GaN Systems GS-065-004-1-L | GaN, $0.5 \Omega$ | 4 |
| $C_{\text {in }}$ | TDK C3216C0G2W153J160AA | $15 \mathrm{nF}, \mathrm{C} 0 \mathrm{G}$ | 2 |
| $C_{\text {fly }}$ | TDK CKG45NC0G2W943J500JJ | $94 \mathrm{nF}, \mathrm{C} 0 \mathrm{G}$ | 6 |
| $C_{\text {out }}$ | TDK CGA8P3X7T2E105K250KA | $1 \mu \mathrm{~F}, \mathrm{X} 7 \mathrm{~T}$ | 1 |

TABLE II
MEASURED PERFORMANCE OF THE SWITCHED-CAPACITOR CONVERTER at half and full output power.

|  | 25 W | 50 W |
| :--- | :---: | :---: |
| PF [\%] | 97.3 | 99.1 |
| PF (fundamental) [\%] | 97.8 | 99.3 |
| Current displacement [deg] | 12.1 | 6.7 |
| Current THD [\%] | 6.9 | 2.8 |
| Efficiency [\%] | 96.6 | 97.1 |

TABLE III
MEASURED PERFORMANCE OF THE SWITCHED-CAPACITOR CONVERTER, BOOST CONVERTER AND COMPLETE SYSTEM AT 50 W OUTPUT POWER.

|  | SC | Boost | Total |
| :--- | :---: | :---: | :---: |
| PF [\%] | 99.1 | 98.7 | 94.3 |
| PF (fundamental) [\%] | 99.3 | 99.5 | 97.4 |
| Current displacement [deg] | 6.7 | 6.0 | 13.2 |
| Current THD [\%] | 2.8 | 12 | 10.5 |
| Efficiency [\%] | 97.1 | 95.0 | 92.5 |

the boost converter is the bottleneck for system power efficiency. Hence, to improve the overall system performance, the boost converter operation should be optimized for the lower input and output voltage, but it is not an absolute necessity as is apparent from these results.

## IV. Conclusion

A switched-capacitor front-end for universal PFC circuits has been presented and analyzed. This front-end stage reduces the voltage stress of the PFC circuit and significantly limits the input voltage range, which allows for better optimization of the PFC circuit. Through circuit analysis, the front-end's effect on system power factor is modelled. Experimental results for the SC front-end show good correlation between calculated and measured performance. The implemented switched-capacitor front-end standalone achieves a power factor of 0.991 at 50 W output power and a power factor of 0.973 at 25 W output power. Finally, the switched-capacitor front-end is cascaded with a low voltage boost converter PFC circuit, which results in a power factor of 0.943 and $92.5 \%$ efficiency at full load with 230 V RMS input. The implemented prototype shows that the proposed topology is capable of providing high power factor without any additional control efforts. The full potential of the topology can be quantified through optimization of the PFC circuit for reduced input voltage range.

## References

[1] R. Fernandes and O. Trescases, "A multimode 1-mhz pfc front end with digital peak current modulation," IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5694-5708, 2016.
[2] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of singlephase pfc topologies based on the boost converter," in 2010 9th IEEE/IAS International Conference on Industry Applications - INDUSCON 2010, 2010, pp. 1-6.
[3] L. Huber, L. Gang, and M. M. Jovanovic, "Design-oriented analysis and performance evaluation of buck pfc front end," IEEE Transactions on Power Electronics, vol. 25, no. 1, pp. 85-94, 2010.
[4] X. Wu, J. Yang, J. Zhang, and M. Xu, "Design considerations of softswitched buck pfc converter with constant on-time (cot) control," IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3144-3152, 2011.


Fig. 8. Measured voltage and current from the AC supply and output voltage of the switched-capacitor in the complete system with cascaded boost converter. Output power is 50 W .
[5] X. Xie, C. Zhao, L. Zheng, and S. Liu, "An improved buck pfc converter with high power factor," IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2277-2284, 2013.
[6] Y. Ohnuma and J. Itoh, "A novel single-phase buck pfc acdc converter with power decoupling capability using an active buffer," IEEE Transactions on Industry Applications, vol. 50, no. 3, pp. 1905-1914, 2014.
[7] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated buckboostquadratic buck pfc rectifier for universal input applications," IEEE Transactions on Power Electronics, vol. 24, no. 12, pp. 2886-2896, 2009.
[8] Y. Li and C. Chen, "A novel primary-side regulation scheme for singlestage high-power-factor acdc led driving circuit," IEEE Transactions on Industrial Electronics, vol. 60, no. 11, pp. 4978-4986, 2013.
[9] C. Zhao, J. Zhang, and X. Wu, "An improved variable on-time control strategy for a crm flyback pfc converter," IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 915-919, 2017.
[10] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New bridgeless dcm sepic and cuk pfc rectifiers with low conduction and switching losses," IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 873-881, 2011.
[11] B. Poorali and E. Adib, "Analysis of the integrated sepic-flyback converter as a single-stage single-switch power-factor-correction led driver," IEEE Transactions on Industrial Electronics, vol. 63, no. 6, pp. 3562-3570, 2016.
[12] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Analysis and design of a charge-pump-based resonant ac-dc converter with inherent pfc capability," IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1-1, 2020.
[13] Z. Liao, N. C. Brooks, Z. Ye, and R. C. N. Pilawa-Podgurski, "A high power density power factor correction converter with a multilevel boost front-end and a series-stacked energy decoupling buffer," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 9 2018, pp. 72297235.
[14] S. Qin, Y. Lei, Z. Ye, D. Chou, and R. C. N. Pilawa-Podgurski, "A high-power-density power factor correction front end based on sevenlevel flying capacitor multilevel converter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1883-1898, 92019.
[15] E. Candan, A. Stillwell, N. C. Brooks, R. A. Abramson, J. Strydom, and R. C. N. Pilawa-Podgurski, "A 6-level flying capacitor multi-level converter for single phase buck-type power factor correction," in 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 3 2019, pp. 1180-1187.
[16] M. S. Makowski and D. Maksimovic, "Performance limits of switchedcapacitor dc-dc converters," in Proceedings of PESC '95 - Power Electronics Specialist Conference, vol. 2, 6 1995, pp. 1215-1221 vol.2.
[17] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 841-851, 32008.
[18] "UCC28056 data sheet," Texas Instruments Incorporated, Texas, United States.

## Appendix [J8]

N. J. Dahl, A. M. Ammar, and M. A. E. Andersen, "Identification of ZVS Points and Bounded Low-Loss Operating Regions in a Class-DE Resonant Converter," under revision in IEEE Transactions on Power Electronics.

# Identification of ZVS Points and Bounded Low-Loss Operating Regions in a Class-DE Resonant Converter 

Nicolai J. Dahl, Student Member, IEEE, Ahmed M. Ammar, Student Member, IEEE, Michael A.E. Andersen, Member, IEEE


#### Abstract

This paper presents an analysis of the different loss modes of the switching devices in a class-DE series resonant converter operating with either a fixed dead time or fixed duty cycle. A feasible operating region where the FETs in the inverter stage only exhibit reverse conduction losses, with no hard switching, is identified, and an upper bound for the diode losses is determined. Furthermore, the impact of using a fixed dead time compared to a fixed duty cycle is investigated. We find that using a fixed dead time is superior to using a fixed duty cycle, as a broader operating range can be achieved for the same losses, or the same operating range can be achieved with lower losses. A reduction in the reverse conduction losses of up to $\mathbf{5 9 . 6 \%}$ or an expansion of the operating range by $\mathbf{3 3 . 2 \%}$ when using a fixed dead time is found. Lastly, the modeling approach is validated on a 1 MHz prototype employing GaN switching devices. The obtained results are especially useful when optimizing the selection of the FETs and for the case of using frequency control with a fixed dead time to regulate converter output.


Index Terms-Resonant converters, Modeling, First Harmonic Approximation, DC-DC power converters.

## I. Introduction

TODAY, most electronic devices are powered with a Switch Mode Power Supply (SMPS) thanks to their small form factor and high efficiency. The majority of the SMPS are different types of hard switching PWM topologies. These supplies have high switching losses, which limit the switching frequency that the supplies can handle. Nonetheless, higher switching frequencies allow for smaller passive components, and hence an overall smaller power supply, as well as higher bandwidth to better react to various load and line disturbances. To improve the switching frequencies, soft switching topologies have been receiving much attention in recent years [1-8]. One family of soft switching converters is the resonant converters [9]. Resonant converters work by having a resonant tank responsible for providing AC gain, in addition to charging and discharging the switching node during the dead time before the switching event and thus obtain Zero Voltage Switching (ZVS). This vastly reduces the switching losses allowing for a higher operating frequency.

In many cases it is of interest to control the output voltage of the resonant converter. This could be to compensate for

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby (e-mail: nicoje@elektro.dtu.dk; ammma@elektro.dtu.dk; ma@elektro.dtu.dk)
changes or disturbances in the load or in the supply voltage, but it could also be to obtain a variable power supply. Multiple different control strategies have been proposed in the literature. Some of the most common control techniques are: Tunable resonant tank capacitor control [10-13], bang-bang control [14-17], and frequency control [18-21]. The tunable resonant tank capacitor control adjust the resonance frequency by biasing the resonant tank capacitor, thereby regulating the output voltage. The method can be used with other control strategies, but requires access to a tunable capacitor in the circuit. Bang-Bang control works by turning the converter either completly on or off. This allows for a simpler converter design since the converter only need to operate at full power. Lastly, frequency control works by changing the switching frequency of the converter and thereby changing the gain by moving closer or further away from the resonance frequency. Frequency control works for a wide range of resonant converters. However, changing the switching frequency changes both the magnitude and the phase of the resonant current. Therefore, the exact dead time needed to have ZVS becomes increasingly difficult to obtain and maintain over a broad range of switching frequencies. As a simple control strategy is often preferred, frequency control is often applied. Hence it is relevant to investigate how the losses in the switching devices can be minimized when out of the ZVS point.

This paper presents an analysis of the different switching loss modes in the FETs for a class-DE Series Resonant Converter (SRC) when the dead time is assumed fixed, and frequency control is utilized. Multiple ZVS points for the same dead time and limitations of the operating range is identified. Further, we define a feasible soft-switching operation region where we determine an upper loss bound for the FETs. The analysis both looks at the case where a fixed dead time is used and where a fixed duty cycle is used and determines the best of the two options. The findings in this paper can be used for optimizing the selection of the FETs while also providing valuable information for both the design of the converter and controller. Finally, the analysis is validated on a 1 MHz class-DE SRC, where the feasible region and worst-case losses within the region are measured.

Although the presented analysis and results are carried out for a class-DE SRC, the analysis and findings are applicable for any resonant converter that uses a sinusoidal current to
charge and discharge the switching node. Such converters are, among others, class-D based converters using either parallel ans/or series resonance tanks like the LLC and LCC converters.

## II. Losses in Inverter Switching Devices

Fig. 1 shows a Class-DE SRC with the parasitic capacitances for the FETs $C_{o s s_{H}}$ and $C_{o s s_{L}}$. It is assumed that the converter operates above the resonance frequency in the inductive mode where the resonant current lags the switching node voltage, and that the parasitic capacitances are static. When driving the converter outside the point of ZVS, losses occur in the FETs either due to insufficient charging/discharging of the combined output capacitance $C_{o s s_{(t)}}$, reverse conduction losses of the FETs, or both. This section presents the loss mechanisms with the magnitude and conditions for each type of switching loss.


Fig. 1: The class-DE series resonant converter with the parasitic capacitance for the FETs.

For resonant converters, ZVS is achieved by having the resonant tank current $I_{r}$ charge/discharge the switching node $V_{s w}$ to $V_{s} /$ ground before turning on the corresponding FET. Doing this results in zero volts across the FET at the switching moment, thus achieving ZVS, and no power is dissipated. Due to the symmetry of the resonant current and the power stage, achieving ZVS in the charge direction implies that ZVS is likewise achieved in the discharge direction. Hence the presented math in this and the following sections will focus on the charge case only when determining ZVS and losses. Also, the time dependency is omitted from the equations unless mentioned otherwise.

The time that $I_{r}$ has to charge $C_{o s s_{(t)}}$ to $V_{s}$ is given by the dead time $t_{d}$, which is related to the duty cycle by:

$$
\begin{equation*}
t_{d}=\frac{0.5-D}{f_{s w}} \tag{1}
\end{equation*}
$$

where $D$ is the duty cycle for each FET and $f_{s w}$ is the switching frequency of the converter. In some cases, the dead time is implemented as a constant time and will be independent of the switching frequency. If the dead time is too short or the resonant current too small, $C_{o s s_{(t)}}$ is insufficiently charged, leading to a voltage across the FET at the switching moment that will results in switching loss. Equation (2) shows the loss. $V_{D S}$ is the voltage across the FET at the switching moment.

$$
\begin{equation*}
P_{s w}=\frac{1}{2} C_{o s s_{(t)}} V_{D S}^{2} f_{s w} \tag{2}
\end{equation*}
$$

If the dead time is too long, the FET will enter reverse conduction which prevent overcharging of $C_{o s s}$ but leads to reverse conduction losses. For this analysis, GaN switches are considered for the FETs. Accordingly, with the zero reverserecovery charge of GaN devices, the reverse conduction losses are limited to the product of the effective reverse voltage and current. Equation (3) shows the reverse conduction loss. Here $V_{f}$ is the voltage drop across the FET in reverse conduction and $t_{\text {cond }}$ is the reverse conduction time.

$$
\begin{equation*}
P_{\text {rev }}=V_{f} t_{c o n d} I_{r} f_{s w} \tag{3}
\end{equation*}
$$

Lastly, there is the case where the dead time is so long that the resonant tank changes direction at time $t_{r}<t_{d}$ causing an undesired discharge of the switching node $V_{s w}$. In this case both reverse conduction losses and switching losses occur. Fig. 2 shows the four types of switching.

Through a rewriting of (2) and (3), the losses of the three lossy switching modes in Fig. 2 can be determined. In the case of partial hard switching losses, $V_{D S}$ can be determined as the voltage over $C_{o s s_{(t)}}$ due to the accumulated charge from $I_{r}$ during the dead time subtracted from the supply voltage. Hence (2) can be rewritten to (4).

$$
\begin{equation*}
P_{s w}=\frac{1}{2} C_{o s s_{(t)}} f_{s w}\left(\frac{1}{C_{o s s_{(t)}}} \int_{t_{d}} I_{r} d t-V_{s}\right)^{2} \tag{4}
\end{equation*}
$$

In the case of reverse conduction losses, the term $t_{\text {cond }} I_{r}$ provides the number of charges passing through the FET during the conduction time. This can be written as the total number of charges accumulated during the dead time subtracted with the


Fig. 2: Typical switching waveforms for $V_{s w}(t)$. From the top: ZVS; where $V_{s w}(t)$ is fully charge/discharged during the dead time. Reverse conduction; where reverse conduction occurs due to long dead time. Current reversal; where $V_{s w}(t)$ starts to discharge again before the end of the dead time. Partial hard switching; where the dead time is too short resulting in a jump in the voltage at turn on/off.
number of charges needed to charge $C_{o s s_{(t)}}$ to $V_{s}$. Equation (5) shows the rewritten version of (3).

$$
\begin{equation*}
P_{r e v}=V_{f} f_{s w}\left(\int_{t_{d}} I_{r} d t-V_{s} C_{o s s_{(t)}}\right) \tag{5}
\end{equation*}
$$

Finally, in the cases where both reverse conduction losses and switching losses occur due to a long dead time causing the reversal of the current flow, the losses can be written as in (6). Here the charges for $P_{\text {rev }}$ are only accumulated up to the point where the current flow changes direction $\left(t_{r}\right)$ and the switching loss is evaluated from $t_{r}$ to the end of the dead time $t_{d}$.

$$
\begin{array}{r}
P_{r e v}=V_{f} f_{s w}\left(\int_{t_{r}} I_{r} d t-V_{s} C_{o s s_{(t)}}\right) \\
P_{s w}=\frac{1}{2} C_{o s s_{(t)}} f_{s w}\left(\frac{1}{C_{o s s_{(t)}}} \int_{t_{d}-t_{r}} I_{r} d t\right)^{2} \tag{6b}
\end{array}
$$

## III. Switching Loss Analysis

In this section, we determine a feasible operation region in regards to power losses. The region is encircled by the ZVS points and the boundary where the direction of the resonant current changes. Thus both of these behaviors will be described analytically. Furthermore, the losses induced in the FET's related to switching are determined for the feasible region. The analysis is carried out using the First Harmonic Approximation (FHA) approach [9] combined with the methods presented by Hamill in [22] to include the effects of the parasitic capacitance in the rectifier diodes. Normalized units will be used to generalize the findings.

Using the FHA, we assume that the resonance current, $I_{r}$, can be adequately described as a pure sine waveform. Equation (7) shows the approximated resonance current $\hat{I}_{r}$.

$$
\begin{equation*}
I_{r} \approx \hat{I}_{r}=I_{m} \sin \left(\omega_{n} t+\phi\right) \tag{7}
\end{equation*}
$$

where $I_{m}$ is the magnitude of the current given by (8a), and $\phi$ is the phase shift between the resonant current and $V_{s w}$ given by ( 8 b ).

$$
\begin{align*}
I_{m} & =\frac{\left|\mathcal{F}_{1}\left\langle V_{s w}\right\rangle\right|}{R_{e q} \sqrt{1+Q^{2}\left(\omega_{n}-\omega_{n}^{-1}\right)^{2}}}  \tag{8a}\\
\phi & =-\arctan \left(Q\left(\omega_{n}-\omega_{n}^{-1}\right)\right) \tag{8b}
\end{align*}
$$

$\mathcal{F}_{n}\langle\cdot\rangle$ denotes the function for the $n$ 'th harmonic Fourier series, and $\omega_{n}$ is the normalized angular switching frequency given by:

$$
\begin{equation*}
\omega_{n}=\omega / \omega_{c} \tag{9}
\end{equation*}
$$

where $\omega$ is the switching frequency and $\omega_{c}$ is the resonance frequency of the converter in rad $/ \mathrm{sec}$. Lastly, $Q$ is the resonant tank quality factor, and $R_{e q}$ is the ideal equivalent resistive
load of the rectifier as seen from the output of the inverter and is given by (10).

$$
\begin{equation*}
R_{e q}=\frac{2 R_{L}}{\left(\pi+C_{d} \omega R_{L}\right)^{2}}+R_{e s r} \tag{10}
\end{equation*}
$$

where $R_{L}$ is the load resistance and $R_{e s r}$ is the combined parasitic series resistance in the resonant tank. In Hamill's work, the parasitic capacitance of the rectifier diodes is modeled as a capacitor, $C_{h}$ in series with $R_{e q}$. The capacitor $C_{h}$ being in series with the resonant capacitor $C_{r}$ effectively reduces the total resonant tank capacitance and makes it dependent on the switching frequency. This impacts the resonance frequency, $\omega_{c}$ and the quality factor $Q$ such that both increase slightly with the switching frequency. Modeling the small increase in both the resonance frequency and quality factor results in a better prediction of the resonant current when the switching frequency is far away from the resonance frequency of the converter, hence improving the fidelity of the model.

## A. Zero Voltage Switching Points

Zero Voltage Switching can be achieved whenever the accumulated charge from the resonant current is equal to that needed to charge the parasitic capacitance, $C_{o s s_{(t)}}$ to the supply voltage, $V_{s}$. The resonance current is only able to deliver charge during the dead time which is assumed fixed. Hence to obtain ZVS, the equality in (11) needs to be true.

$$
\begin{equation*}
\int_{\bar{t}_{z v s}}-\hat{I}_{r} d t-V_{s} C_{o s s_{(t)}} \omega_{c}=0 \tag{11}
\end{equation*}
$$

Where $\bar{t}_{z v s}$ is the normalized dead time needed for ZVS. Inserting (7) in the integral of (11) and evaluating the integral we get:

$$
\begin{equation*}
\frac{I_{m}\left(\cos \left(\omega_{n} \bar{t}_{z v s}+\phi+\theta\right)-\cos (\phi+\theta)\right)}{\omega_{n}}-V_{s} C_{o s s_{(t)}} \omega_{c}=0 \tag{12}
\end{equation*}
$$

where $\theta=\left\langle\mathcal{F}_{1}\left\langle V_{s w}\right\rangle\right.$. The switching node $V_{s w}$ is described by a piecewise function such that the charge and discharge of the output capacitance is included []. A result of this is that the phase of the Fourier approximation becomes non-zero. Thus $\theta$ accounts for any phase shift present in $V_{s w}$ such that it aligns properly with $I_{r}$. By solving for $\bar{t}_{z v s}$ in (12) an expression for the dead time needed to obtain ZVS is found.

$$
\begin{equation*}
\bar{t}_{z v s}=-\frac{\phi+\theta+\arccos \left(\cos (\phi+\theta)+\frac{V_{s} \omega C_{o s s_{(t)}}}{I_{m}}\right)}{\omega_{n}} \tag{13}
\end{equation*}
$$

To obtain a condition for ZVS similar to (13) but for a fixed duty cycle, the relation in (1) is used in its normalized form (14).

$$
\begin{equation*}
\bar{t}_{z v s}=2 \pi \omega_{n}^{-1}\left(0.5-D_{z v s}\right) \tag{14}
\end{equation*}
$$

Substituting $\bar{t}_{z v s}$ with (13) and solving for the duty cycle results in (15).

$$
\begin{equation*}
D_{z v s}=\frac{1}{2}+\frac{\phi+\theta+\arccos \left(\cos (\phi+\theta)+\frac{V_{s} \omega C_{o s s}(t)}{I_{m}}\right)}{2 \pi} \tag{15}
\end{equation*}
$$

By sweeping $\omega$ in (13) and (15) it is possible to trace out the ZVS curve. Fig. 3 shows the obtained ZVS curve for a fixed duty cycle (Fig. 3a), and a fixed dead time (Fig. 3b) when the resonant tank has a $Q=4$. As seen, the computed solution indicates that two simultaneous ZVS points exist for a fixed dead time in the normalized range from 0.44 to 0.68 , and for a fixed duty cycle from $42.2 \%$ to $38.5 \%$. For the low frequency part of the ZVS curve i.e. the ZVS curve below the "Max Loss" curve, the resonant current is almost in phase with the switching node. Thus the voltage of the switching node will reach $V_{s} /$ ground with a decreasing slope, leading to Zero Voltage derivative Switching (ZVdS) and thereby also Zero Current Switching (ZCS). The ZVdS will result in a decreased sensitivity to changes in the dead time, which is seen in Fig. 3 by the small slope of the low frequency ZVS. At large dead times, or small duty cycles, the low frequency section of the ZVS curve disappears due to the reversal of the current flow marked by the dashed line.

## B. Current Flow Reversal Limit

During the desired operation of a resonant converter, the resonance current will monotonically charge the switching node during the dead time period. However, if the dead time becomes too extensive, the direction of the resonant current will change during the dead time resulting in an unwanted discharge of the switching node near the end. This behavior inhibits ZVS. Thus it is of interest to work out when this phenomena occurs.

Whenever the current flow changes direction, a zero-crossing occurs. This means that the time needed to reach the zerocrossing is equivalent to finding the point of the current flow reversal. Hence we have:

$$
\begin{equation*}
-I_{m}\left(\omega_{s}\right) \sin \left(\omega_{n} \bar{t}_{r}+\phi+\theta\right)=0 \tag{16}
\end{equation*}
$$

Where $\bar{t}_{r}$ is the normalized time needed to reach the zerocrossing given by: $\bar{t}_{r}=t_{r} \omega_{c}$. The only practical solution to (16) is when the trigonometric term is zero. Due to the nature of the sine function it follows:

$$
\begin{align*}
& \Rightarrow-\omega_{n} \bar{t}_{r}-\phi-\theta=0  \tag{17}\\
& \Leftrightarrow \bar{t}_{r}=(\phi+\theta) / \omega_{n} \tag{18}
\end{align*}
$$

From where the zero-crossing time is found. Using the relationship between the normalized time and duty cycle from (14), the corresponding duty cycle limit, $D_{r}$, can be determined:

$$
\begin{align*}
& 2 \pi \omega_{n}^{-1}\left(0.5-D_{r}\right)=(\phi+\theta) / \omega_{n}  \tag{19}\\
& \Leftrightarrow D_{r}=\frac{1}{2}-\frac{\phi+\theta}{2 \pi} \tag{20}
\end{align*}
$$

The dashed lines in Fig. 3 shows the boundaries for where the current flow reversal occur. Fig. 3a shows it when operating with a fixed duty cycle (20), and Fig. 3b for when operating with a fixed dead time (18). Due to the nature of the current flow reversal limit, ZCS will always happen when operating on the limit.


Fig. 3: The feasible operation region of the resonant converter encircled by the ZVS curve and the current reversal boundary. (a) shows the region for a fixed duty cycle, and (b) shows the region for a fixed normalized dead time. The max loss indicates the curve where the worst case losses in the region will be.

## C. Maximum Reverse Conduction Loss

The area encircled by the ZVS curve and the reverse current boundary in Fig. 3 is the region of reverse conduction losses. It is usually preferable to stay in this region compared to staying in the region with quadratic switching losses since lower losses are achievable. This is especially the case with GaN devices which has zero reverse recovery charge. Thus the encircled region with its encirclement constitutes the feasible operating region for the resonant converter. As only reverse conduction losses occur in the feasible region, an upper bound of the losses in the FETs can be determined to assess the worst-case operation mode and location.

To find the worst-case reverse conduction losses in the feasible operating region we first evaluate the losses in every point in the region using the normalized reverse conduction loss (22). Finally, the maximum loss for each dead time/duty cycle is logged.

$$
\begin{align*}
\bar{P}_{\text {rev }} & =V_{f} \frac{\omega_{n}}{2 \pi}\left(\int_{\bar{t}_{d}}-I_{r} d t-C_{o s s_{(t)}} V_{s} \omega_{c}\right)  \tag{21}\\
& =V_{f} \frac{\omega_{n}}{2 \pi} \int_{\bar{t}_{z v s}}^{\bar{t}_{d}}-I_{r} d t \tag{22}
\end{align*}
$$

In Fig. 3 the contour lines indicates the magnitude of the reverse conduction losses in the feasible region. The curve "Max Loss" represents the points of the worst case losses in the feasible region. The max loss curve follows the contour lines by intersecting the peaks of the contours which indicate the highest loss point for the given dead time / duty cycle. Once the max loss curve reaches the current flow reversal limit, the worst-case loss will follow the limit until it reaches the upper bound of the feasible region. Lastly, the curve for the current flow reversal boundary indicates the end points of where ZVS is achievable. However, increasing the dead time slightly beyond this boundary does not have a significant impact on the losses. This is because the reverse current flow can be used to reduce the voltage difference due to the forward voltage drop that would otherwise create an additional small switching loss.

## IV. Comparison of Dead Time and Duty Cycle

For a selected dead time / duty cycle the feasible operating region will have a certain range of switching frequencies where the converter will operate within the region. For a normalized dead time of 0.5 , the range of feasible operating frequencies is approximately 0.15 . However, as the dead-time increases, the range expands until the effect of the current reversal becomes severe and begins limiting the range once again. Fig. 4 shows this effect for both the fixed dead time and the fixed duty cycle cases.
As the dead time is increased, the feasible operating frequency range expands until it reaches 0.31 from where it rapidly subtracts due to the current reversal limiting the


Fig. 4: The operational frequency range against the normalized worst case diode conduction loss in the feasible region for the given range. The arrows are indicating the direction of increased dead time and decreased duty cycle, equivalent of moving to the right on Fig. 3. The dead time and duty cycle each moves up to the point of the highest diode loss.

TABLE I: Specifications of the converter. The capacitances, $V_{f}$, and $R_{d}$ are based on device characterization using a Keysight B1505A power device analyzer.

|  | Value | Unit | Acquired |
| :---: | :---: | :--- | :--- |
| $V_{s}$ | 350 | V | Measured |
| $R_{L}$ | 1000 | $\Omega$ | Measured |
| $R_{e s r}$ | 2 | $\Omega$ | Measured |
| $C_{o s s}(t r)$ | 40 | pF | Measured |
| $C_{d}$ | 12.6 | pF | Measured |
| $V_{f}$ | 1.3 | V | Measured |
| $R_{d}$ | 0.6 | $\Omega$ | Measured |
| $f_{c}$ | 836 | kHz | Calculated |

switching frequency from below. The same effect is observed when the duty cycle is decreased. However, the duty cycle is only able to reach a maximum frequency range of 0.23 . Moreover, the maximum losses in the feasible region when using a fixed duty cycle is higher than using a fixed dead time. More specifically, the analysis shows that a fixed dead time provides an expansion of up to $33.2 \%$ in the operating range for the same losses compared to using a fixed duty cycle, or up to a $59.4 \%$ decrease in reverse conduction losses for the same operating range compared to using a fixed duty cycle.

## V. Experimental Validation

To validate the findings in the analysis, a 1 MHz class-DE resonant converter prototype using GaNFETs [23] for the inverter switches is constructed. A complete characterization was performed on both the GaNFETs and the rectifier diodes using a Keysight B1505A power device analyzer to obtain accurate data from the model. To characterize the output capacitance, the capacitance is measured for multiple bias voltages across the device going from 0 V to $V_{s}$. Then the average of the acquired capacitance values is calculated to get the time related output capacitance. The same approach is used to obtain the rectifier diode capacitance with the only difference being that the bias voltage only going to 250 V . The reverse conduction characteristic of the GaNFET is modeled as a diode using a forward voltage $V_{f}$ and a resistor $R_{d}$. Figure 5 shows the prototype and Table I shows the specifications and test conditions.

Points across both the ZVS curve and the current reversal curve are measured for encircling the feasible region and for comparison with the analysis. The measurements are performed by changing the switching frequency and duty cycle


Fig. 5: Prototype class-DE SRC.


Fig. 6: Measured (points) and analytic (lines) results for the prototype converter. (a) shows the result for the fixed duty cycle, and (b) shows the results for the fixed dead time.
of the converter until ZVS is observed. The same procedure is used for the current reversal. To determine the curve and size of the worst case reverse conduction losses in the feasible region, an experiment is designed to map the response surface in the feasible region. Thus the reverse conduction losses are measured at multiple points inside the feasible region. From the measurements, a $4^{\text {th }}$ order model is fitted and the maximum loss is derived from the estimated model.

Fig. 6a shows the measurement results (points) with the expected results from the analysis (lines) for a fixed duty cycle, and Fig. 6b shows the measurement results for the fixed dead time.

Looking at Fig. 6 we find that the ZVS measurements and the location of the worst case losses correspond to the theory. The ZVS measurements follow the theoretical curve exactly until 1.2 MHz where the measurements starts to fall slightly below the curve while the max loss points are measured to be at a slightly higher frequency than predicted. The reverse current limit follows the expected curve up to approximately 1

MHz from where the points are found at a greater dead time than expected. The discrepancy between the measurement and theory with the increasing switching frequency is partly due to the breakdown of the FHA method since the resonant current $I_{r}$ no longer acts like a pure sinusoidal current. Furthermore, at higher switching frequencies, the model becomes more sensitive to the values of the parasitic capacitance in the FETs and rectifier diodes.

The measured feasible region, both when using a fixed dead time and a fixed duty cycle, assimilates the shape of the corresponding theoretical region with the main difference being the lower reverse current limit that expands the region slightly more. This suggests that the difference in performance identified in section IV is valid and a fixed dead time in general is preferred.

To verify the claim made in section III-A, that the ZVS points below the max diode loss curve provide ZCS besides ZVS, the resonant tank current waveform $I_{r}$ and the switch node waveform $V_{s w}$ are logged for ZVS at 926 kHz . Figure 7 shows the waveforms.


Fig. 7: Switch node voltage and resonant tank current at 926 kHz and 130 ns dead time where ZVS and ZCS are achieved. The dashed line indicates the zero-crossing of the current


Fig. 8: Switch Node and resonant tank current at 1.05 MHz and 200 ns dead time where ZVS and ZCS are achieved. The dashed line indicates the zero-crossing of the current

From Fig. 7 it is clear to see that $V_{s w}$ charges up with a decreasing slope and reaches the final voltage with almost zero slope, indicating that the resonant current is zero i.e. ZCS is achieved, which is likewise observed from the resonant tank current waveform. Finally, Fig. 8 shows a case where the converter is operating at the current flow reversal limit. The resonant current charges the switching node within the first 87 ns resulting in a reverse conduction time of 113 ns . When the resonant current reaches zero the dead time expires and the inverter switches. Hence only reverse conduction losses is present during operation and both ZVS and ZCS are achieved.

## VI. Conclusion

This paper presents an analysis of the different switching loss modes in a class-DE SRC using either a fixed dead time or fixed duty cycle. A feasible operating region where the FETs in the inverter stage only exhibit reverse conduction losses is defined and fully enclosed by the ZVS curve and the reverse current limit. This results in the possibility of calculating the worstcase loss in the FETs prior to prototyping, thereby optimizing the FET selection and dead time adjustment. Furthermore, the impact of using a fixed dead time compared to a fixed duty cycle was investigated. We found that using a fixed dead time is superior to using a fixed duty cycle since a broader operating range can be achieved for the same reverse conduction losses, or the same operating range can be achieved with lower losses. A reduction in the reverse conduction losses of up to $59.6 \%$ or an expansion of the operating range by $33.2 \%$ when using a fixed dead time rather than a fixed duty cycle was found. The modeling approach is validated on a 1 MHz class-DE SRC prototype employing GaN switching devices, where the measurements followed the patterns predicted by the model.

## References

[1] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1-14, Feb 2009.
[2] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. Andersen, "Evolution of very high frequency power supplies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, 2014.
[3] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," in Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE, pp. 1-11, IEEE, 2006.
[4] N. Bertoni, G. Frattini, R. G. Massolini, F. Pareschi, R. Rovatti, and G. Setti, "An Analytical Approach for the Design of Class-E Resonant DC-DC Converters," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7701-7713, 2016.
[5] P. C. Luk, S. Aldhaher, W. Fei, and J. F. Whidborne, "State-Space Modeling of a Class $E^{2}$ Converter for In-
ductive Links," IEEE Transactions on Power Electronics, vol. 30, pp. 3242-3251, June 2015.
[6] X. Gao, H. Wu, and Y. Xing, "A Multioutput LLC Resonant Converter With Semi-Active Rectifiers," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1819-1827, 2017.
[7] M. Noah, S. Endo, H. Ishibashi, K. Nanamori, J. Imaoka, K. Umetani, and M. Yamamoto, "A Current Sharing Method Utilizing Single Balancing Transformer for a Multiphase LLC Resonant Converter With Integrated Magnetics," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 977-992, 2018.
[8] H. Ma, Y. Li, Q. Chen, L. Zhang, and J. Xu, "A Single-Stage Integrated Boost-LLC AC-DC Converter With Quasi-Constant Bus Voltage for Multichannel LED Street-Lighting Applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1143-1153, 2018.
[9] M. K. Kazimierczuk and D. Czarkowski, Resonant power converters. John Wiley \& Sons, 2012.
[10] B. Guo, S. Dwari, and S. Priya, "Voltage-controlled tunable capacitor based resonant power converter," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2164-2169, IEEE, 2019.
[11] Y. Hu, A. Amara, and A. Ioinovici, "Llc resonant converter operated at constant switching frequency and controlled by means of a switched-capacitor circuit," in 2013 1st International Future Energy Electronics Conference (IFEEC), pp. 691-696, IEEE, 2013.
[12] K. Harada, A. Katsuki, M. Fujiwara, H. Nakajima, and H. Matsushita, "Resonant converter controlled by variable capacitance devices," IEEE Transactions on Power Electronics, vol. 8, no. 4, pp. 404-410, 1993.
[13] I. Kolberg, D. Shmilovitz, and S. S. Ben-Yaakov, "Ceramic capacitor controlled resonant llc converters," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2162-2167, IEEE, 2018.
[14] K.-H. Lee and J.-I. Ha, "Resonant switching cell model for high-frequency single-ended resonant converters," IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 11897-11911, 2019.
[15] W. Zhong and S. Hui, "Maximum energy efficiency operation of series-series resonant wireless power transfer systems using on-off keying modulation," IEEE Transactions on Power Electronics, vol. 33, no. 4, pp. 3595-3603, 2017.
[16] K.-H. Lee, E. Chung, Y. Han, and J.-I. Ha, "A family of high-frequency single-switch dc-dc converters with low switch voltage stress based on impedance networks," IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2913-2924, 2016.
[17] J. M. Rivas, O. Leitermann, Y. Han, and D. J. Perreault, "A very high frequency dc-dc converter based on a class $\phi 2$ resonant inverter," IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 2980-2992, 2011.
[18] N. J. Dahl, A. M. Ammar, A. Knott, and M. A. Andersen, "An improved linear model for high frequency class-
de resonant converter using the generalized averaging modeling technique," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.
[19] M. Salem, V. K. Ramachandaramurthy, A. Jusoh, S. Padmanaban, M. Kamarol, J. Teh, and D. Ishak, "Threephase series resonant dc-dc boost converter with double llc resonant tanks and variable frequency control," IEEE Access, vol. 8, pp. 22386-22399, 2020.
[20] M. Salem, A. Jusoh, N. R. N. Idris, C. W. Tan, and I. Alhamrouni, "Phase-shifted series resonant dc-dc converter for wide load variations using variable frequency control," in 2017 IEEE Conference on Energy Conversion (CENCON), pp. 329-333, IEEE, 2017.
[21] S. Zou, A. Mallik, J. Lu, and A. Khaligh, "Sliding mode control scheme for a cllc resonant converter," IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 12274-12284, 2019.
[22] D. C. Hamill, "Class de inverters and rectifiers for dc-dc conversion," in PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, vol. 1, pp. 854-860, IEEE, 1996.
[23] GaNSystems, "GaN transistor GS66502B," 2017.

## Appendix [C1]

A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Miniaturization of LED Drivers," 6th International Workshop on Power Supply-On-Chip (PwrSoC), Hsinchu, 2018.

## 5

Hsinchu, Taiwan Oct. 17-19, 2018

## Miniaturization of LED Drivers

Ahmed Ammar, Frederik Spliid, Yasser Nour \& Arnold Knott
Technical University of Denmark, DTU Electrical Engineering, Electronics group
Elektrovej 325, $2^{\text {nd }}$ floor, 2800 Kgs. Lyngby, Denmark


Fig. 1 Miniaturization Strategy.

- Topologies: Soft-switching resonant converters
- Control: Combination of control schemes (e.g. frequency control + burst mode control)
- Devices: Wide band-gap (WBG) devices and Integrated Passive Devices (IPDs) technologies
- Energy Storage: Active ripple port circuits allowing for employment of smaller and more robust capacitor technologies
- Frequency: HF and VHF operation.


## Experimental Results

Measurement results of a class-DE series-resonant converter that can be incorporated for the AC-DC and the DC-DC stages in an LED driver:

- Up to 400 V input with soft-switching
- 1 MHz operation
- High voltage GaN switches and SiC diodes
- Potential for operation in HF and VHF ranges
- Frequency modulation can be used for line/load regulation.


Fig. 2 Class-DE Series-Resonant Converter.


Fig. 3 Scope image showing the switching node voltage (blue), sinusoidal resonant inductor current (green), and gate signals for 350 V input voltage.


Fig. 4 Efficiency and output power for different output voltages.

## Conclusion

- Operation at high frequencies is key for miniaturization
- Good candidate: soft-switching resonant converters
- WBG devices show great potential for high efficiencies
- Combined control can allow for enhanced line/load regulation.


## References

[1] A. Knott et al., "Evolution of Very High Frequency Power Supplies," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sept. 2014.
[2] Y. Nour and A. Knott, "Module integrated GaN power stage for high switching frequency operation," 2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS), Honolulu, HI, 2017, pp. 848-852.

## Acknowledgement

$\square$ This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466

## Appendix [C2]

F. M. Spliid, A. M. Ammar, and A. Knott, "Stacked class E resonant Very High Frequency converter for European mains power factor correction," 6th International Workshop on Power Supply-On-Chip (PwrSoC), Hsinchu, 2018.

# Stacked class E resonant Very High Frequency converter for European mains power factor correction 

Frederik Spliid, Ahmed Ammar \& Arnold Knott<br>Technical University of Denmark, DTU Electrical Engineering, Electronics group

Elektrovej 325, 2nd floor, DK-2800 Kgs. Lyngby, Denmark

## Introduction

- Great demand for compact PFCs in LED products.
- Driver size can be reduced by increasing switching frequency.
- This poster: design of 50 W resonant VHF AC/CD converter


## Design

- Stacked configuration reduce voltage stresses and improve efficiency. [1]
- Class E inverter and class DE rectifier enables zero-voltage switching.


Fig. 1 Stacking configuration.

- GaN devices with low parasitic capacitance enable high switching frequency.
- Air-core inductors gives high $Q$ magnetics at high frequencies.
- Self-resonant gate driver enables VHF switching [2].


Fig. 2 Class E inverter stage with self-oscillating resonant gate drive

| Input voltage | $230 \mathrm{~V}_{\mathrm{AC}} @ 50 \mathrm{~Hz}$ |
| :---: | :---: |
| Output voltage | $110 \mathrm{~V}_{\mathrm{DC}}$ |
| Switching frequency | $30-37 \mathrm{MHz}$ |

Tab. 1 Converter specifications


Fig. 3 Left: $\mathrm{V}_{\mathrm{ds}}$ (red) and $10 x$ scaled $\mathrm{V}_{\mathrm{gs}}$ (blue) of inverter switch Right: Rectifier input voltage (red) and current (blue)


Fig. 4 Input voltage (red) and current (blue)

| Output power | 52.2 W |
| :---: | :---: |
| Efficiency | $90.3 \%$ |
| Power Factor | $93 \%$ |
| Input current THD | $38 \%$ |

Tab. 2 Simulated converter performance


#### Abstract

Conclusion - Stacked topology reduce voltage stresses. - GaN transistors and air-core inductors enable VHF operation - Self-oscillating gate drive enables open-loop operation


## References

[1] M. Madsen et al., "Input-Output Rearrangement of Isolated Converters", in Proceedings of 2015 IEEE Power and Energy Conference at Illinois, 2015.
[2] M. Madsen et al., "Self-oscillating resonant gate drive for resonant inverters and rectifiers composed solely of passive components", in Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2014.
[3] J. Pedersen et al., "US Mains Stacked Very High Frequency Self-oscillating Resonant Power Converter with Unified Rectifier", in Thirty-first Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2016

## Acknowledgement

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466

## Appendix [C3]

A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," 2019 IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, 2019.

# A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability 

Ahmed M. Ammar, Frederik M. Spliid, Yasser Nour and Arnold Knott<br>Department of Electrical Engineering<br>Technical University of Denmark<br>Kongens Lyngby, Denmark<br>\{ammma, frmsp, ynour, akn\}@elektro.dtu.dk


#### Abstract

This paper presents a power factor correction (PFC) rectifier for single-phase offline converters. With the addition of a charge pump circuit comprised of a capacitor and a diode to a class-DE series-resonant converter, PFC is achieved inherently. The converter operation is based on soft-switching, and a 1 MHz 50 W prototype employing wide bandgap devices is implemented, achieving a power factor of 0.99 and a total harmonic distortion (THD) of $8.6 \%$, at an efficiency of $84 \%$, with substantially low input current harmonic magnitudes compared to the limits set by the IEC 61000-3-2 standard.


Keywords-AC-DC power conversion, rectifiers, power factor correction, resonant power conversion, wide bandgap semiconductors.

## I. Introduction

With the recent advancements in industrial electronics that aim for added performance, reliability, and portability, there exists a great demand for new technologies in power converters that can cope with such trend. Pulse-width-modulated (PWM) converters have been the primary candidate for offline converters for years, thanks to their high efficiency and power quality. However, they typically operate at low frequencies in order to limit the switching losses, as their operation is based on hard-switching. On the other hand, resonant converters allow for the utilization of soft-switching techniques through the intrinsic alternating behavior of the currents and voltages through the switches, thus expensing substantially lower switching losses, making them a good candidate for operation at higher frequencies, which has many benefits including the smaller sizes for the passive components, higher power densities, higher loopgain bandwidths, and faster transient responses. This has led to the investigation of their adoption into different applications typically dominated by PWM converters [1]-[5].

The typical solution for offline converters is a two-stage architecture, as shown in fig. 1, where the first stage is an ACDC power factor correction (PFC) rectifier, followed by an energy storage capacitor to filter the double-the-line (100/120 Hz ) frequency component, while the second stage is a DC-DC converter providing the voltage and current levels that apply to the load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current and harmonic limits to reduce the mains voltage distortion [6][7].

This paper presents a resonant PFC rectifier for the first stage in single-phase offline converters. The proposed rectifier, shown in fig. 2, incorporates an input filter and bridge, a charge pump

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466.


Fig. 1. Offline converter structure. The red box outlines the focus of this work.


Fig. 2. Proposed PFC rectifier.
circuit, a DC energy storage capacitor, and a class-DE seriesresonant converter.

The paper is organized as follows. Section II overviews the principle of operation. The implementation process is illustrated in section III. Experimental results and waveforms are presented in section IV. Eventually, conclusion is provided in section V.

## II. Principle of Operation

## A. Class-DE Resonant Stage Operation

A resonant converter is comprised of two stages [8], as shown in fig. 3. First, an inverter that employs a switch network which converts the DC (or low frequency AC) input to a high frequency AC output, followed by a resonant tank that provides $\mathrm{AC}-\mathrm{AC}$ gain. The second stage is a high frequency AC-DC rectifier, where energy is tapped off the resonant tank and delivered to the load. In this work, a class-DE stage is used in the converter, which combines the low-voltage stress of class-D converters and the zero voltage switching (ZVS) capabilities of class-E converters [9]. Accordingly, the half-bridge switches are rated for the converter peak input voltage, and with a proper switching frequency and dead-time adjustment, the resonant tank current charges/discharges the output capacitances of the switches, such that their voltages reach the appropriate rail voltage before switching the gate, thus ensuring ZVS. That, in turn, allows for design at higher switching frequencies while achieving high efficiencies.


Fig. 3. Class-DE series-resonant converter.

## B. Charge Pump Circuit Operation

A charge pump electronic ballast circuit was reported in [10]. Through the addition of a capacitor and a diode to a conventional high-frequency inverter circuit, the input current can be regulated to follow the input voltage. In this design, a series-resonant inverter circuit is used and a high-frequency rectifier is added for enabling use in AC-DC converters, where the energy storage capacitor is moved to the converter input to allow for soft-switching operation with the varying AC line voltage.

An equivalent circuit for the charge pump is shown in fig. 4, with $C_{P}$ and $D_{P}$ referring to the pump capacitor and diode, $D_{B}$ to the input bridge, $\mathrm{C}_{\mathrm{DC}}$ to the energy storage capacitor, while the rectifier input, to which the pump capacitor is coupled, is modelled by an independent high frequency voltage source $\mathrm{V}_{\mathrm{REC}}$. The DC capacitor $\mathrm{C}_{\mathrm{DC}}$ is designed in accordance with the pump capacitor $C_{P}$, such that the voltage $V_{D C}$ is always higher than $\mathrm{V}_{\mathrm{IN}}$, and thus the diode bridge $\mathrm{D}_{\mathrm{B}}$ and the pump diode $\mathrm{D}_{\mathrm{P}}$ do not cross-conduct. Consequently, the input current is equal to the positive charging current of the pump capacitor $\mathrm{C}_{\mathrm{P}}$.

Fig. 5 shows the low-frequency operation of the pump circuit, where the pump capacitor is charged and discharged within the fall and rise times of $\mathrm{V}_{\mathrm{REC}}$ respectively, and the charge $\Delta \mathrm{Q}_{\mathrm{p}}$ is proportional to the voltage difference across the capacitor $\mathrm{V}_{\mathrm{P}}$, which varies between a low-frequency high-value $\mathrm{V}_{\mathrm{P} \text { _high }}$ and a constant low-value $\mathrm{V}_{\mathrm{P} \text { _low. }}$. The circuit design ensures that the charge variation of $C_{P}$, which is proportional to the voltage variation across it ( $\mathrm{V}_{\mathrm{P} \_ \text {high }}-\mathrm{V}_{\mathrm{P} \_ \text {low }}$ ), follows the input voltage $\mathrm{V}_{\text {IN }}$ across the line cycle ( $50 / 60 \mathrm{~Hz}$ ). Accordingly, the average input current follows the input voltage and a unity power factor can ideally be obtained.


Fig. 4. Charge pump equivalent circuit.


Fig. 5. Low-frequency operation across half a line cycle ( 50 Hz ).
Fig. 6 shows the high-frequency operation across two switching cycles, and includes waveforms illustrating the converter operation at the maximum power point $\left(\omega_{\mathrm{t}} \mathrm{t}=\pi / 2\right.$, with $\omega_{l}$ being the line frequency) to illustrate the charge pump circuit operation. Across every switching cycle, at steady-state, the operation spans four intervals as follows.
In the first interval, the voltage $\mathrm{V}_{\mathrm{B}}$ is lower than the DC capacitor voltage $\mathrm{V}_{\mathrm{DC}}$ and higher than the input voltage $\mathrm{V}_{\mathrm{IN}}$, so both the diode bridge and the pump diode are off and no current flows through the pump capacitor $C_{P}$ and the voltage $V_{P}$ is constant $\left(\mathrm{V}_{\mathrm{P}_{-} \text {low }}\right)$. The $\mathrm{V}_{\text {IN }}$ waveform in figure refers to the voltage on the node interfacing the LC-filter and the diode bridge.
The second interval takes place across the fall time of $\mathrm{V}_{\text {REC }}$. Once $V_{\text {REC }}$ starts to decrease, $V_{B}$ has to decrease along, until $D_{B}$ gets forward biased and $\mathrm{V}_{\mathrm{B}}$ gets pulled to $\mathrm{V}_{\mathrm{IN}}$. While $\mathrm{V}_{\text {Rec }}$ continues decreasing, with $V_{B}$ constant (as the grid frequency is significantly lower than the frequency of $\mathrm{V}_{\mathrm{REC}}$ ), $\mathrm{V}_{\mathrm{P}}$ increases and $C_{P}$ is charged by the line current $\mathrm{I}_{\mathrm{IN}}$, until $\mathrm{V}_{\text {REC }}$ reaches its low-value and $V_{P}$ reaches its high-value, where

$$
\begin{equation*}
V_{P_{\_} \text {high }}=V_{I N}-V_{\text {REC_low }} \tag{1}
\end{equation*}
$$

The third interval begins once $\mathrm{V}_{\text {Rec }}$ settles at the low-value, where $C_{P}$ stops charging while $D_{P}$ still blocks. Similar to the first interval, no current flows through the pump capacitor and $\mathrm{V}_{\mathrm{P}}$ is constant.


Fig. 6. Operation across two switching cycles.

Eventually, the fourth interval takes place across the rise time of $\mathrm{V}_{\mathrm{REC}}$. Once $\mathrm{V}_{\mathrm{REC}}$ starts to increase, $\mathrm{V}_{\mathrm{B}}$ has to increase along until $D_{P}$ gets forward biased and $V_{B}$ gets pulled to $V_{D C}$. While $V_{\text {rec }}$ continues increasing, with $V_{D C}$ constant, $V_{P}$ decreases and $C_{P}$ discharges into the resonant tank, until $\mathrm{V}_{\text {Rec }}$ reaches its highvalue, $\mathrm{V}_{\text {REC_high }}$, and $\mathrm{V}_{\mathrm{P}}$ reaches its low-value, where

$$
\begin{equation*}
V_{P_{-} \text {low }}=V_{D C}-V_{R E C_{\_} \text {high }} \tag{2}
\end{equation*}
$$

By the end of the fourth interval, operation enters interval 1 again and the cycle repeats. The analysis shows that the input current is discontinuous and only flows into the circuit during the second interval.

For a series-resonant converter, the voltage $\mathrm{V}_{\text {REC }}$ varies between $V_{\text {Out }}$ and 0 V , where (1) and (2) can be evaluated as follows

$$
\begin{align*}
V_{P \_h i g h} & =V_{I N}-V_{R E C \_l o w}=V_{I N}-0=V_{I N}  \tag{3}\\
V_{P \_l o w} & =V_{D C}-V_{R E C \_h i g h}=V_{D C}-V_{O U T} \tag{4}
\end{align*}
$$

The equations show that the high-values for the voltage across the pump capacitor take the envelope of the input voltage, while the low-values take the envelope of the difference between the resonant converter input and output voltages, which can be considered constant in high frequency. Across one switching cycle, the variation of charge in the capacitor is

$$
\begin{align*}
\Delta Q_{P}= & C_{P} \cdot \Delta V_{P}=C_{P}\left(V_{P_{-} \text {high }}-V_{P_{-} \text {low }}\right) \\
& =C_{P}\left(V_{I N}-V_{D C}+V_{\text {OUT }}\right) \tag{5}
\end{align*}
$$

The pump capacitor charging current, which is equal to the input current, averaged across one switching cycle is equal to

$$
\begin{equation*}
I_{I N}=\frac{\Delta Q_{P}}{T_{s}}=f_{s} \cdot \Delta Q_{P}=f_{s} \cdot C_{P}\left(V_{I N}-V_{D C}+V_{O U T}\right) \tag{6}
\end{equation*}
$$

where $f_{s}$ is the converter switching frequency. Considering that the class-DE stage operates near resonance with a high gain close to 1 , the difference between $V_{D C}$ and $V_{\text {Out }}$ will be very small. Therefore, at steady state, for a constant switching frequency, the pump capacitor charging current, and accordingly the input current, become proportional to the input voltage, resulting in a high power factor and low total harmonic distortion (THD).

## III. Implementation

A prototype is designed and implemented, targeting low to mid power range applications supplied from European mains. A switching frequency of 1 MHz is specified for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. The converter is implemented and assembled on a two-layer printed circuit board (PCB). Fig. 7 shows a photograph of the implemented prototype power stage.

Considering the charge pump circuit operation, high frequency AC current runs through the input bridge, which is implemented using four fast-recovery diodes. In addition, as the resonant tank carries both the charge pump circuit current as well as the current to the output load, high current stress takes place at the peak of the input power, which requires custom design of the resonant inductor. For such application with high


Fig. 7. Prototype power stage.
frequency AC current, the choice of the magnetic material is of key importance. Fig. 8 shows a comparison of several highfrequency magnetic materials in terms of core losses at 1 MHz [11][12]. The 3F46 material is chosen as it shows the lowest core losses at the operational switching frequency. The inductor is designed with 52 turns of two parallel layers of $20 * 0.05 \mathrm{~mm}$ Litz wire wound on an EFD 25/13/9 core. An airgap of 1.2 mm , distributed across the three legs of the core, adjusted the desired inductance.

With respect to the selection of switches, fig. 9 shows a comparison based on datasheet parameters between the best-inclass switches figures of merit [13]-[15], where gallium nitride FETs show superior performance in that voltage range compared to the silicon super-junction and silicon carbide counterparts. Device 6 (GS66502B) is used for the inverter halfbridge design. For the rectifier side, silicon carbide schottky diodes (GB01SLT06-214) are employed, as they result in higher efficiency compared to the silicon high-voltage counterparts.

Table I lists the proposed converter power-stage bill of materials (BOM). The switches gate driving circuit is comprised of a digital isolator (Si8610BC by Silicon Labs) and a gate driver (UCC27611 by Texas Instruments) for each of the high side and low side switches. For the high side driver supply, a bootstrap network of a diode (GB01SLT06-214, SiC Schottky) and a capacitor $(1 \mu \mathrm{~F}$, ceramic X 7 R$)$ is used, in addition to a peripheral


Fig. 8. Core power loss density (Pv) vs. magnetic flux density (B) for different magnetic materials at 1 MHz .


Fig. 9. Summary of the best-in-class switching devices figures of merit.
solution comprised of isolated power supplies (MTE1S0506MC by Murata), and both circuits are equally operational.

## IV. Experimental Results

## A. Lab Setup

A thermal camera (Flir T650SC) continuously monitors the converter operation and a 1 GHz scope (LeCroy Wavesurfer 104MXS-B) displays the high frequency signals including switching node voltage, inductor current, and gate-signals, where the dead-time is adjusted and fixed at a point where softswitching is achieved and the average devices temperature is minimal. Another 200 MHz scope (LeCroy Wavesurfer 24XsA) is used to display the low frequency signals, which include the input and output voltages and input current. A low voltage DC power supply (Rohde \& Schwarz HMP2020) supplies the driving circuit, while a high voltage AC power supply (Keysight AC6802A) emulates the AC mains. A 120 MHz dual-channel waveform generator (Keysight 33622A) generates the driving circuit signals. A DC electronic load (Itech IT8812B) acts as an active load for the circuit under test. Finally, a precision power analyzer (N4L PPA5530) measures efficiency, power factor, displacement factor, THD, and the magnitudes of input current harmonics.

TABLE I. Proposed CONVERTER BOM

| Component | Value | Type |
| :---: | :---: | :---: |
| $\mathrm{L}_{\mathrm{IN}}$ | $100 \mu \mathrm{H} / 0.5 \mathrm{~A}$ | Inductor |
| $\mathrm{C}_{\mathrm{IN}}$ | $2 * 15 \mathrm{nF} / 450 \mathrm{~V}$ | Ceramic (C0G) |
| Diode Bridge | $4 *$ ESH1GM RSG | Si Fast Recovery |
| $\mathrm{C}_{\mathrm{DC}}$ | $1 * 10 \mu \mathrm{~F} / 450 \mathrm{~V}$ | Electrolytic |
|  | $3 * 0.1 \mu \mathrm{~F} / 450 \mathrm{~V}$ | Ceramic (C0G) |
| $\mathrm{D}_{\mathrm{P}}$ | RF 201 LAM 4 S | Si Fast Recovery |
| $\mathrm{C}_{\mathrm{P}}$ | $2 * 680 \mathrm{pF} / 500 \mathrm{~V}$ | Ceramic (C0G) |
| $\mathrm{Q}_{\mathrm{HS}}, \mathrm{Q}_{\mathrm{LS}}$ | GS 66502 B | GaN Switches |
| $\mathrm{L}_{\mathrm{RES}}$ | $152 \mu \mathrm{H} / 1.7 \mathrm{~A}$ | Custom design |
| $\mathrm{C}_{\mathrm{RES}}$ | $220 \mathrm{pF} / 3 \mathrm{kV}$ | Ceramic (C0G) |
| $\mathrm{D}_{\mathrm{R} 1}, \mathrm{D}_{\mathrm{R} 2}$ | $\mathrm{~GB} 01 \mathrm{SLT06-214}$ | SiC Schottky |
| $\mathrm{C}_{\mathrm{OUT}}$ | $2 * 15 \mathrm{nF} / 450 \mathrm{~V}$ | Ceramic (C0G) |

## B. Results

The converter is tested for operation from $230 \mathrm{~V}_{\mathrm{RMS}}$, achieving 50 W of output power, with an efficiency of $84 \%$, a power factor of 0.99 and a THD of $8.6 \%$ at 0.96 MHz . Fig. 10 shows a scope capture for the switching node voltage, the resonant tank current, and the signals to the gate drivers at fullload operation. The capture is taken with infinite persistence to visualize the variations across the input voltage range, which is the low-frequency ripple on the DC capacitor voltage. The switching node voltage $\mathrm{V}_{\text {SW }}$ is measured using a 500 MHz 10 x voltage probe with 9 pF capacitance, while the resonant circuit current $\mathrm{I}_{\text {Res }}$ is measured using a 50 MHz current probe (LeCroy AP015). The figure illustrates inductive mode of operation, with the resonant current lagging the switching node voltage. The driving signals are synchronized with the same duty-cycle and extended dead-time to avoid cross conduction between the two switches and achieve ZVS. It is noted that the converter is partially soft-switching for the low voltages across the DC capacitor, which can be alleviated by employing a larger energy storage capacitor ( $\mathrm{C}_{\mathrm{DC}}$ ).

Fig. 11 shows the input voltage and current and the output voltage at full-load. The input voltage is displayed using a high voltage differential probe (Testec SI 9001), while the input current is measured using a 50 MHz current probe (Hioki CT6700), and the output voltage is measured using a 500 MHz voltage probe with 9 pF capacitance. The figure shows an almost sinusoidal input current with a phase difference of $5.7^{\circ}$ with the input voltage, and an average output voltage of 300 V .


Fig. 10. Scope image for the resonant tank waveforms ( $\mathrm{V}_{\text {SW }} 100 \mathrm{~V} /$ div, $\mathrm{I}_{\text {RES }} 1$ A/div, HSG/LSG 5 V/div with $200 \mathrm{~ns} /$ div).


Fig. 11. Scope image for the input voltage, current, and output voltage. ( $\mathrm{V}_{\text {IN }}$ $100 \mathrm{~V} / \mathrm{div}, \mathrm{I}_{\text {IN }} 100 \mathrm{~mA} /$ div, V Vut $100 \mathrm{~V} /$ div with $5 \mathrm{~ms} / \mathrm{div}$ ).

An AC 100 Hz ripple of 40 V is measured on the output voltage, which is about $13.3 \%$ of the average output voltage and can be reduced through the incorporation of a larger DC energy storage capacitor, depending on the specification of the following DCDC converter stage.

Fig. 12 shows the input current harmonics distribution at full-load operation, where a THD of $8.6 \%$ is measured. Since one of the potential applications for the proposed converter is the rectifier stage in LED drivers, the figure compares the harmonic magnitudes against the IEC 61000-3-2 standard classC device limits [6][7], where it is shown that the measured harmonics magnitudes are substantially lower than the limits set by the standard.

Fig. 13 shows a thermal photograph for the prototype under full-load operation, where the inductor windings are the hottest element in the circuit, with a maximum temperature of $84.5^{\circ} \mathrm{C}$ (with airflow). That is due to the charge pump circuit operation, which requires the resonant tank to store both the energy from the input line as well as the energy to the load every switching cycle, resulting in additional current stress on the resonant inductor.


Fig. 12. Input current harmonics distribution against the IEC 61000-3-2 standard.


Fig. 13. Thermal image for converter at full-load.

## V. Conclusion

A PFC rectifier for the AC-DC stage in single-phase offline converters is presented. With the addition of a charge-pump circuit comprised of a capacitor and a diode to the class-DE series-resonant converter, PFC functionality is achieved inherently, while operation is based on soft-switching, allowing for high frequency design. A 1 MHz 50 W prototype employing WBG devices is designed and implemented, achieving a power factor of 0.99 and THD of $8.6 \%$ at an efficiency of $84 \%$, with input current harmonic magnitudes substantially lower than the IEC 61000-3-2 standard limit.

## References

[1] J. M. Rivas, R. S. Wahby, J. S. Shafran and D. J. Perreault, "New Architectures for Radio-Frequency DC-DC Power Conversion," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 380-393, March 2006.
[2] D. J. Perreault et al., "Opportunities and Challenges in Very High Frequency Power Conversion," 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, 2009, pp. 1-14.
[3] A. Knott et al., "Evolution of Very High Frequency Power Supplies," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, Sept. 2014.
[4] A. Knott, T. M. Andersen, P. Kamby, M. P. Madsen, M. Kovacevic and M. A. E. Andersen, "On the ongoing evolution of very high frequency power supplies," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2013, pp. 2514-2519.
[5] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," 2006 37th IEEE Power Electronics Specialists Conference, Jeju, 2006, pp. 1-11.
[6] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[7] EN 61000-3-2, European Committee for Electrotechnical Standardization, 2014.
[8] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd edition. Wiley-IEEE Press, 2011.
[9] D. C. Hamill, "Class DE inverters and rectifiers for DC-DC conversion," PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, Baveno, Italy, 1996, pp. 854-860 vol.1.
[10] W. Chen, F. C. Lee and T. Yamauchi, "An improved "charge pump" electronic ballast with low THD and low crest factor," in IEEE Transactions on Power Electronics, vol. 12, no. 5, pp. 867-875, Sept. 1997
[11] Ferroxcube material datasheet https://www.ferroxcube.com/upload/media/design/FXCStainmetzCoeffi cients.xls.
[12] Micrometals material datasheet https://micrometalsarnoldpowdercores.com/pdf/mix/Mix-6DataSheet.pdf.
[13] E. Hoene, G. Deboy, C. R. Sullivan and G. Hurley, "Outlook on Developments in Power Devices and Integration: Recent Investigations and Future Requirements," in IEEE Power Electronics Magazine, vol. 5, no. 1, pp. 28-36, March 2018.
[14] G. Deboy, O. Haeberlen and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 89-100, 2017.
[15] A. Hopkins, N. McNeill, P. Anthony and P. Mellor, "Figure of merit for selecting super-junction MOSFETs in high efficiency voltage source converters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 3788-379.

## Appendix [C4]

A. M. Ammar, Y. Nour, and A. Knott, "A High-Efficiency 1 MHz 65 W GaN-Based LLC Resonant DC-DC Converter," 2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE), Aswan, 2019.

# A High-Efficiency 1 MHz 65 W GaN-Based LLC Resonant DC-DC Converter 

Ahmed M. Ammar, Yasser Nour and Arnold Knott<br>Department of Electrical Engineering<br>Technical University of Denmark Kongens Lyngby, Denmark<br>\{ammma, ynour, akn\}@elektro.dtu.dk


#### Abstract

This paper presents an LLC resonant DC-DC converter for single-phase offline converters. A 1 MHz 400 V to 48 V prototype employing gallium nitride ( GaN ) switching devices is designed and implemented. A high-frequency magnetic material is used for the magnetic devices, with the resonant inductor integrated in the transformer. The converter operation is based on soft switching and achieves up to 65 W of output power with a peak efficiency of 96 \% at full-load. Inherent load regulation capability is demonstrated from 5 to 65 W of power with fixed switching frequency, while line regulation for 360 to 440 V input is verified with a frequency modulation range of 816 to 1256 kHz respectively.


Keywords—resonant power conversion, dc-dc converters, offline converters, wide bandgap semiconductors, zero voltage switching (ZVS)

## I. INTRODUCTION

PWM converters have been the primary candidate for switch-mode power supplies (SMPS) for years. They offer high efficiency and power quality with simple control. Nevertheless, their operation is mostly based on hard switching, which limits their switching frequencies to few hundred kHz for high-voltage converters, in order to reduce their switching losses. This in-turn results in the need for larger passive devices to process and deliver the power to the load. On the other hand, resonant converters allow for the utilization of soft-switching techniques through the intrinsic alternating behavior of the currents and voltages through the switches, which results in substantially lower switching losses, and enables the design for higher switching frequencies, and thus achieving higher power densities. This has led to the investigation of their adoption into different applications typically dominated by PWM converters [1], one of which is offline converters [2][3].

The conventional solution for single-phase offline converters is a two-stage structure, as shown in fig. 1. The first stage is an AC-DC power factor correction (PFC) rectifier followed by an energy storage capacitor to filter the $100 / 120 \mathrm{~Hz}$ frequency component. The second stage is a DC-DC converter which steps-down the DC-bus voltage to the voltage level that applies to the load characteristics. With the boost converter being the primary candidate for the PFC front-end converter, the typical bus voltage interfacing the two stages is around 380-400 V , with the $100 / 120 \mathrm{~Hz}$ ripple on top, typically being $10 \%$ of the nominal bus voltage, which sets the specification for the lineregulation capability of the DC-DC stage.

[^6]

Fig. 1. Single-phase offline converters structure. The red box outlines the focus of this work.
This paper presents an LLC resonant converter solution for the DC-DC stage in offline converters. The LLC topology offers high-efficiency and inherent load regulation capability. It also offers soft-switching operation, thus allowing the design for high switching frequencies, which allows for achieving higher power densities. A 65 W prototype is designed and implemented for 48 V output voltage, which is a common voltage for several applications including computing power supply unit (PSU), telecom, power-over-Ethernet ( PoE ) and lighting.

This paper is organized as follows. Section II overviews the converter structure. The design procedure is illustrated in section III. Section IV covers the implementation process. Experimental results and waveforms are presented in section V. Eventually, conclusion is provided in section VI.

## II. Converter Structure

A resonant converter is comprised of two stages [4]-[6]. First, an inverter which incorporates a switch network that converts the DC input to a high frequency AC , followed by a resonant tank that provides AC-AC gain. The second stage is a high-frequency AC-DC rectifier, which taps-off the energy in the resonant tank and delivers it to the load. Fig. 2 shows the LLC converter block diagram. The switch network can be configured as a half-bridge or a full-bridge arrangement. The resonant tank is comprised of the series connection of a resonant capacitor $C_{R E S}$, a resonant inductor $L_{R E S}$, and the magnetizing inductance of the rectifier transformer $L_{M}$. The


Fig. 2. LLC Converter block diagram.

TABLE I. COMPARISON BETWEEN SWITCH AND RECTIFIER NETWORKS CONFIGURATIONS

| Parameter | Switch Network |  | Rectifier Network |  |
| :---: | :---: | :---: | :---: | :---: |
|  | HB | FB | FW | FB |
| Number of devices | 2 | 4 | 2 | 4 |
| Voltage Gain | 0.5 | 1 | 1 | 1 |
| Current Rating | $\times 2$ | x 1 | x 1 | x 1 |
| Voltage Rating | x 1 | x 1 | x 2 | x 1 |
| Conduction Loss | x 2 | x 1 | x 0.5 | x 1 |
| Winding Copper Loss | x 2 | x 1 | $\times 2$ | x 1 |

rectifier can be implemented by a full-wave or a full-bridge configuration. Table I shows a comparison between the switch network and rectifier network configurations [7]. A half-bridge switch network would need to sustain double the current stress for the full-bridge network switches, but with half of the fullbridge number of devices. That results in reduced devices count at the expense of twice the total FETs conduction losses of the full-bridge, assuming the same power devices. In addition, a half-bridge voltage gain of one half requires half the transformer primary-winding number of turns for the same voltage gain and magnetic flux density, giving half the primarywinding resistance. However, the primary copper losses are still twice that of the full-bridge because of the four times squaredrms current. On the other hand, the full-wave rectifier has half the number of diodes compared to the full-bridge, with the same average current in the diode, resulting in half the diode conduction losses, but at the expense of twice the voltage rating. Additionally, a full-wave rectifier has two secondary windings, giving double the resistance for the same winding area, which results in twice the secondary-winding copper losses.

## III. Design Procedure

## A. Specifications and Design Considerations

Table II lists the design specifications for the presented converter, which target the low-mid power range applications. A switching frequency $(f s)$ of 1 MHz is specified for the design, as it constitutes a good trade-off between the converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. With the specified power range, for which the primary current isn't high, a design choice of a half-bridge switch network is made, as the switches conduction losses and transformer primary winding copper loss are limited. On the other hand, a full-bridge rectifier configuration is chosen, since this simplifies the transformer design, and to ease the choice of the diodes with the availability of high-performance low-voltage Schottky diodes.

## B. Design Procedure

The main design goal is to maintain zero-voltage switching (ZVS) within a frequency range that enables high efficiency across all line and load conditions. The design procedure illustrated in [7] is followed here. In order to maintain ZVS, the entire operation has to be within the inductive region of

TABLE II. DEsign Specifications

| Parameter | Specification |
| :---: | :---: |
| Input Voltage | $400 \mathrm{~V}+10 \% 100 / 120 \mathrm{~Hz}$ ripple |
| Output Voltage | 48 V |
| Output Power | 65 W |
| Efficiency | $\geq 95 \%$ at full-load |

operation, where the resonant current lags the switching node voltage. From the specifications, the converter gain is calculated as follows.

$$
\begin{equation*}
M=\frac{V_{\text {OUT }}}{V_{I N}} \tag{1}
\end{equation*}
$$

The converter gain is the product of the switch-network gain, the resonant-tank gain, and the transformer turns ratio. Considering a half-bridge for the switching network and a 4:1 turns ratio ( $n$ $=N_{S} / N_{P}$ ) in the transformer, the required resonant tank gain is evaluated from

$$
\begin{equation*}
M_{R E S}=\frac{M}{M_{H B} \cdot n} \tag{2}
\end{equation*}
$$

For a nominal input voltage of 400 V and $10 \%$ double the line frequency ripple, resulting in a line regulation range of 360-440 V , the required range of resonant tank gain is calculated to 0.87 - 1.07 across the input-voltage range. The resonant-tank gain is the magnitude of the LLC resonant-circuit transfer function, which is a function of the loaded quality factor $\left(Q_{L}\right)$, the normalized switching frequency $\left(f_{n}\right)$, and the ratio of the total primary inductance to the resonant inductance $(k)$, and is evaluated by

$$
\begin{equation*}
M_{R E S}=\frac{f_{n}^{2}(k-1)}{\sqrt{\left(k \cdot f_{n}^{2}-1\right)^{2}+f_{n}^{2} \cdot\left(f_{n}^{2}-1\right)^{2} \cdot(k-1)^{2} \cdot{Q_{L}}^{2}}} \tag{3}
\end{equation*}
$$

where

$$
\begin{gather*}
k=\frac{L_{R E S}+L_{M}}{L_{R E S}}  \tag{4}\\
f_{n}=\frac{f_{s}}{f_{o}}  \tag{5}\\
Q_{L}=\frac{\sqrt{L_{R E S} / C_{R E S}}}{R_{R E C}} \tag{6}
\end{gather*}
$$

with $f_{o}$ being the resonant frequency and $R_{R E C}$ being the reflected load resistance at the rectifier input, and are evaluated by

$$
\begin{gather*}
f_{o}=\frac{1}{2 \pi \sqrt{L_{R E S} \cdot C_{R E S}}}  \tag{7}\\
R_{R E C}=\frac{8 R_{L}}{\pi^{2} n^{2}} \tag{8}
\end{gather*}
$$

The value for the parameter $k$ constitutes a trade-off between line-regulation capability through frequency modulation and efficiency. A low- $k$ value results in higher peaking of the resonant-tank gain curve for the same quality factor and resonant frequency, allowing for a higher gain variation within a narrow range of frequency modulation, and thus a better line-regulation capability. At the same time, a low- $k$ value is achieved with a smaller transformer magnetizing inductance $L_{M}$, which in-turn results in higher peak magnetizing current, causing increased conduction losses. For this design, a preliminary value of ten was chosen for the $k$ value in order to enable the integration of the resonant inductance $L_{R E S}$ into the transformer as the primary leakage inductance. This value also goes in hand with the choice of a half-bridge for the switch network, where the reduced
circulating current limits the conduction losses. Circuit simulations are then used to verify the line-regulation capability for the specified line-input range within a reasonable frequency range, and accordingly high efficiency can be maintained.

Fig. 3 shows the resonant tank again across the normalized switching frequency for different values of the loaded quality factor and the chosen $k$ value. It can be observed that all load curves cross at $f_{n}=1$ and have a gain of unity. The curves peaks define the boundary between the capacitive and inductive regions of the resonant tank impedance across different loads. A maximum value for $Q_{L}$ needs to be specified and associated with the maximum load, while satisfying the gain requirements. The figure shows that a $Q_{L}$ value of 0.1 can reach the high gain value of 1.07 , however it is less sensitive to frequency modulation in the above resonance ( $f_{n}>l$ ) region, thus reaching the low-gain value of 0.87 at a normalized frequency of $\sim 3.5$, causing extra switching losses in the switch network, in addition to increased AC conduction losses in the transformer. On the other hand, a higher $Q_{L}$ value of 0.75 reaches the minimum required gain at a lower normalized frequency $\sim 1.4$, but however fails to reach the maximum gain. A trade-off design choice of a maximum $Q_{L}$ of 0.22 is made. Using (6-8), the values for resonant tank components can be obtained.

## C. Simulation Results

Fig. 4 shows simulation results of the presented converter switching-node voltage and resonant-tank current waveforms across different loads at a fixed switching frequency and constant DC output voltage of 1 MHz and 48 V respectively. The figure shows that soft switching is achieved on the switching node across a wide load range of 5 W to 65 W , while the resonant tank current scales with the output power. For the light-load range, the resonant current is observed to be mainly dominated by the transformer magnetizing current, which peaks at $\sim 350 \mathrm{~mA}$, resulting in a lower efficiency at light load, as the circulating energy is large relative to the energy delivered to the load. Light-load efficiency can be enhanced with a higher $k$ value (a higher magnetizing inductance $L_{M}$ ).

Fig. 5 shows simulation results for the switching-node voltage and resonant-tank current across different input voltages


Fig. 3. Resonant tank gain as a function of the normalized switching frequency for different loads and $\mathrm{k}=10$ (Dashed lines represent required high and low gain limits).


Fig. 4. Switching-node voltage and resonant-tank current across different loads (simulation results).


Fig. 5. Switching-node voltage and resonant-tank current across different input voltages (simulation results).
and switching frequencies, at a constant output voltage and power of 48 V and 65 W respectively. With a fixed duty cycle, full ZVS is achieved at the nominal input voltage with 1 MHz switching frequency. Whereas partial soft-switching is observed at the 440 V input with 1.27 MHz switching frequency, as a longer dead-time is needed. On the other hand, a short interval with diode-conduction is noticed at the 360 V input with 0.8 MHz switching frequency, where a reduced dead-time can achieve full ZVS. Accordingly, adaptive dead-time adjustment can result in the best efficiency across line and load ranges. With respect to the resonant tank current, the 360 V condition results in the highest peak current, where it is observed that transformer magnetizing current freewheels for longer time with no power delivered to the load, as operation is far from resonance. On the other hand, for the 440 V input with a switching frequency much closer to resonance, the current is almost sinusoidal and power is delivered to the output across almost the entire cycle.

## IV. Implementation

## A. Power Stage Design

The ideal switch for the LLC converter is a one which allows for minimum conduction loss (low on-resistance) and maximum power transfer (short dead-time, low gate charge and output capacitance). Fig. 6 shows a comparison based on datasheet parameters between the best in-class switches figures of merit [8][9], where the gallium nitride ( GaN ) devices outperform the silicon superjunction ( Si ) and silicon carbide ( SiC ) ones for this voltage and power range. Device 6 (GaN Systems GS66502B)


Fig. 6. Comparison between the best in-class devices figures of merit.
is used for the half-bridge switches realization. The switches gate driving circuit is comprised of a digital isolator (Si8610BC) and a gate driver (UCC27611) for each of the high-side and lowside switches. For the high-side driver supply, a bootstrap network of a diode (RFN1LAM6S) and a capacitor ( $1 \mu \mathrm{~F}$, ceramic X7R) is used. For the rectifier diodes, a low reverserecovery charge is key for achieving high efficiencies, as zerocurrent switching (ZCS) is not necessarily met across all line and load conditions. Schottky diodes offer near-zero reverserecovery charge, so the diode junction capacitance determines the switching loss. Accordingly, Schottky diodes with low capacitance for the rated voltage and current are chosen. The resonant capacitor is implemented using three parallel capacitors to reduce the effective series resistance (ESR). Table III shows a breakdown of the presented prototype bill of materials (BoM), including simulated and realized values.

## B. Magnetic Devices

For this application with a high-frequency AC current, the choice of the magnetic material is of key importance. Fig. 7 shows a comparison of several high-frequency magnetic materials in terms of core losses at 1 MHz [10][11]. The 3F46 material is chosen for the transformer core, as it shows the lowest core losses at the specified switching frequency. Regarding the core and winding structures, an EFD 25/13/9 core is used, and the primary and secondary windings are divided between the core halves and separated, in order to achieve a coupling coefficient aiding with the integration of the resonant inductor in the transformer through the primary leakage inductance, thus saving the space and cost for an additional component. The primary winding is realized using 26 turns of $60 \times 0.04 \mathrm{~mm}$ single-layer insulated Litz wire, while 6 turns of $255 \times 0.05 \mathrm{~mm}$ same-type wire is used for the secondary

TABLE III. PROTOTYPE BOM

| Component | Simulated | Prototype | Type |
| :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\text {IN }}$ | $10 \mu \mathrm{~F}$ | $1^{*} 10 \mu \mathrm{~F} / 450 \mathrm{~V}$ | Electrolytic |
|  |  | $3 * 0.1 \mu \mathrm{~F} / 450 \mathrm{~V}$ | Ceramic $(\mathrm{C} 0 \mathrm{G})$ |
| $\mathrm{Q}_{\mathrm{HS}}, \mathrm{Q}_{\mathrm{LS}}$ |  | GS 66502 B | GaN Switches |
| $\mathrm{C}_{\text {RES }}$ | 1 nF | $3 * 330 \mathrm{pF}$ | Ceramic $(\mathrm{C} 0 \mathrm{G})$ |
| $\mathrm{L}_{\text {RES }}$ | $15 \mu \mathrm{H}$ | $12.9 \mu \mathrm{H}$ | Custom Design |
| $\mathrm{L}_{\mathrm{M}}$ | $135 \mu \mathrm{H}$ | $134.5 \mu \mathrm{H}$ | Custom Design |
| $\mathrm{L}_{\mathrm{S}}$ | $7 \mu \mathrm{H}$ | $7.15 \mu \mathrm{H}$ | Custom Design |
| $\mathrm{D}_{\mathrm{R} 1}-\mathrm{D}_{\mathrm{R} 4}$ |  | PMEG6020ETP | Si Schottky |
| $\mathrm{C}_{\text {OUT }}$ | $0.1 \mu \mathrm{~F}$ | $0.13 \mu \mathrm{~F}$ | Ceramic $(\mathrm{C} 0 \mathrm{G})$ |



Fig. 7. Core power loss per volume $(P v)$ vs. magnetic flux density $(B)$ for different magnetic materials at 1 MHz .
winding. An air-gap of 0.21 mm achieved the desired magnetizing inductance. The air-gap is distributed equally between the inner and outer core legs, with clearance of windings turns in order to minimize the effect of the fringing flux and the losses associated with it. The transformer smallsignal characterization is conducted using a $40 \mathrm{~Hz}-110 \mathrm{MHz}$ precision impedance analyzer (Agilent Technologies 4294A). At 1 MHz , a total primary side inductance of $147.5 \mu \mathrm{H}$ and an ESR of $2.5 \Omega$ are obtained, with $12.9 \mu \mathrm{H}$ measured leakage inductance used towards the resonant tank inductance $L_{\text {RES }}$, and leaving $134.6 \mu \mathrm{H}$ for the magnetizing inductance $L_{M}$. A secondary side inductance of $7.15 \mu \mathrm{H}$ is measured. That results in an effective transformer turns ratio of 4.34.

## V. Experimental Results

## A. Lab Setup

A thermal camera (Flir T650SC) continuously monitors the converter operation and a 2 GHz scope (LeCroy WaveRunner 620 Zi ) displays the high-frequency signals, including the switching-node voltage, the resonant-tank current, and the gatesignals, where a 50 MHz current probe (Hioki CT6700) captures the resonant-tank current waveform. A low-voltage DC power supply (Keysight B2962A) supplies the driving circuit, while a high-voltage power supply (Keysight AC6802A) is used for input-voltage supply, where another supply (Delta Elektronika SM400-AR-4) is stacked on top to source the 440 V input for the high-end of the line regulation test. A 120 MHz dual-channel waveform generator (Keysight 33622A) generates the driving circuit signals, where the dead-time is adjusted and fixed at a point where soft switching is achieved and the average devices temperature is minimal. A DC electronic load (Itech IT8812B) acts as an active load for the circuit under test. Finally, a precision power analyzer (N4L PPA5530) is used for remote sensing and efficiency measurements.

## B. Measurements

Accounting for the printed circuit board (PCB) layout parasitics, tolerances in the resonant-tank components values and temperature variations, the exact resonance frequency becomes subject to variations. Accordingly, an operating frequency of 1 MHz guarantees below resonance operation at all conditions, yet maintaining the inductive mode of operation, which sustains soft switching and high efficiency across line and


Fig. 8. Converter waveforms at 400 V input, 60 W and 1 MHz . ( $V_{S W} 100 \mathrm{~V} / \mathrm{div}, I_{R E S} 500 \mathrm{~mA} /$ div, $V_{\text {OUT }} 20 \mathrm{~V} /$ div at $200 \mathrm{~ns} /$ div).
load variations. Fig. 8 shows a scope capture for the switchingnode voltage, resonant-tank current and the output voltage, with the nominal 400 V input voltage and 48 V output voltage, at 60 W of output power and 1 MHz switching frequency. The figure illustrates the inductive mode of operation, with the resonant current lagging the switching node voltage, achieving full ZVS operation with an efficiency of $96 \%$.

Fig. 9 illustrates the inherent load-regulation capability of the LLC converter, showing the measured efficiency and output voltage across an output power range of 5 W to 65 W , with a constant switching frequency of 1 MHz . The figure shows that high efficiency is achieved across the load range, with a peak efficiency of $96 \%$ at full load, while the maximum error on the nominal 48 V output voltage is $1.12 \%$ at the 5 W load. The reason for the low light-load efficiency is the dominance of the circulating energy of the freewheeling magnetizing current over the energy delivered to the load, as illustrated in fig. 4.

Fig. 10 illustrates the line regulation capability of the presented converter, where a fixed 48 V output voltage at a fixed load of 50 W is achieved through a frequency modulation range of 816 to 1256 kHz for an input voltage range of 360 V to 440 V respectively, where the entire frequency range falls within the inductive region of operation and partial/full ZVS is maintained as illustrated in fig. 5.

## VI. Conclusion

An LLC DC-DC converter for single-phase offline converters is presented. A 1 MHz prototype employing gallium nitride ( GaN ) switching devices is illustrated, where a high-


Fig. 9. Efficiency and output voltage vs. output power for 400 V input voltage at 1 MHz operation.


Fig. 10. Line regulation with frequency modulation at 50 W output power.
frequency magnetic material is used for the transformer design, with the resonant inductor integrated in the transformer through the primary leakage inductance. The experimental results show up to 65 W of output power with $96 \%$ efficiency at full-load. Inherent load regulation capability is demonstrated from 5 to 65 W of power, while line regulation for 360 to 440 V input is verified with frequency modulation.

## References

[1] J. M. Rivas, R. S. Wahby, J. S. Shafran and D. J. Perreault, "New Architectures for Radio-Frequency DC-DC Power Conversion," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 380-393, March 2006.
[2] A. M. Ammar, F. M. Spliid, Y. Nour and A. Knott, "A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-5.
[3] Bo Yang, F. C. Lee, A. J. Zhang and Guisong Huang, "LLC resonant converter for front end DC/DC conversion," APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), Dallas, TX, USA, 2002, pp. 1108-1112 vol.2.
[4] D. C. Marian, K. Kazimierczuk, Resonant Power Converters, 2nd edition. Wiley-IEEE Press, 2011.
[5] R. Mammano, Resonant Mode Converter Topologies-Additional Topics; Unitrode Design Seminars, 1990.
[6] Y. Nour, A. Knott, L. P. Petersen, "High frequency soft switching half bridge series-resonant DC-DC converter utilizing gallium nitride FETs", 2017 19th European Conference on Power Electronics and Applications EPE 2017 ECCE Europe, pp. 1-7, 2017.
[7] S. Abdel-Rahman, Resonant LLC Converter: Operation and Design, Infineon Technologies AN2012-09 V1.0, September 2012.
[8] E. Hoene, G. Deboy, C. R. Sullivan and G. Hurley, "Outlook on Developments in Power Devices and Integration: Recent Investigations and Future Requirements," in IEEE Power Electronics Magazine, vol. 5, no. 1, pp. 28-36, March 2018.
[9] Y. Nour, Z. Ouyang, A. Knott and I. H. H. Jørgensen, "Design and implementation of high frequency buck converter using multi-layer PCB inductor," IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1313-1317.
[10] Ferroxcube material datasheet https://www.ferroxcube.com/upload/media/design/FXCStainmetzCoeffi cients.xls.
[11] Micrometals material datasheet https://micrometalsarnoldpowdercores.com/pdf/mix/Mix-6DataSheet.pdf

## Appendix [C5]

C. H. K. Jensen, R. B. Lind, J. C. Hertel, A. M. Ammar, A. Knott, M. A. E. Andersen, "A TimeBased Control Scheme for Power Factor Correction Boost Converter", 2019 IEEE Nordic Circuits and Systems Conference (NORCAS), Helsinki, 2019.

# A Time-Based Control Scheme for Power Factor Correction Boost Converter 

Christopher H. K. Jensen, Rasmus B. Lind,<br>Jens C. Hertel, Ahmed M. Ammar, Arnold Knott, Michael A. E. Andersen<br>Department of Electrical Engineering<br>Technical University of Denmark<br>Kongens Lyngby, Denmark<br>Email: \{s144042, s144053\}@student.dtu.dk, \{chrhert, ammma, akn, ma\} @elektro.dtu.dk


#### Abstract

A time-based control scheme for the power factor correction (PFC) boost rectifier is presented. Average-currentmode control in time is achieved using time-based compensators performing a proportional-integral control action. The controller is fully CMOS compatible, which allows for monolithic integration with the power switching elements. The time-based controller also eliminates the need for the pulse-width-modulation (PWM) generator required in the conventional analog and digital controllers. The proposed controller draws a sinusoidal input current in phase with the input mains voltage and delivers a dc output voltage. The control scheme model is verified on a 600 W PFC boost converter, achieiving a power factor of 0.99 and a 400 V dc output from a $230 \mathrm{~V}_{r m s} 50 \mathrm{~Hz}$ input voltage.


Index Terms-AC-DC converter, time-based control, power factor correction, voltage-controlled oscillator, boost converter

## I. Introduction

With the recent advancements in industrial electronics that aim for added performance, reliability and portability, a great demand for new technologies in power supplies becomes persistent. Research is taking steps towards highly integrated systems in the form of the Power-System-in-Package (PSiP) and the more compact Power-Supply-onChip (PwrSoC), where application-specific integrated circuits (ASICs) are combined with power devices to produce highly integrated power supplies with high power densities and reduced physical dimensions [1]. While different technologies advanced the power stage miniaturization with the design of power converters switching in the very-high frequency (VHF) range [2][3], new technologies in controller designs are needed to cope with the miniaturization trend. One application with such potential is the power factor correction (PFC) controllers.
A high power factor is generally required in a power supply system connected to the grid. In case the power grid is loaded by a nonlinear load, e.g. switching converter, the current drawn by the load is interrupted by the switching action, which introduces harmonics in the current waveform with frequencies that are multiples of the input line frequency (in

[^7]addition to the switching frequency harmonics). That harmonic distortion reduces the average power transferred to the load, as the average power is the product of the fundamental components of the input current and voltage. In addition, the current harmonics contaminate the grid, affecting the power quality for other grid-connected loads. Accordingly, international standards such as the IEEE/ANSI 519 [4] and the IEC 61000-3-2 [5] set limits on the power factor and input current harmonic magnitudes to reduce the mains voltage distortion. PFC converters bring the power factor of a power circuit closer to unity by making the load appearing more resistive to the grid, thus achieving a close-to-sinusoidal input current that is proportional to and in phase with the sinusoidal input voltage. As a result, PFC rectifiers and their controllers are incorporated in most offline (grid-interfacing) power converters.
Over the past few years, signal processing in the time domain was introduced for several applications [6] [7]. Timebased signal processing utilizes the voltage-to-time properties of ring oscillators and delay lines to synthesize gain blocks, integrators, and differentiators. It is finding new applications to improve performance and reduce die area and power consumption, as it copes better with the technology scaling that comes with increased speeds and reduced power supplies. One application reported in prior art is time-based controllers for DC-DC buck converters [8]-[10], where a time-based control loop compares the output voltage with a reference, and provides regulation across line and load disturbances.
This work investigates the incorporation of time-based control in an AC-DC PFC boost converter, where an additional control loop is included to regulate the input current to follow the input voltage. A time-based control scheme is proposed where two time-based control loops are combined, with a similar function to the conventional average-current-mode controller (ACMC). The presented scheme model is verified on a 600 W PFC boost converter and achieves a power factor of 0.99 with a constant output voltage of 400 V .
This paper is organized as follows. Section II describes the ACMC controller using traditional analog signal processing techniques. The proposed time-based controller is introduced in section III. Section IV covers the design process of the presented controller. Model results are then illustrated in
section V. Eventually, conclusion is provided in section VI.

## II. Average-Current-Mode Controller

To ensure that a power supply appears resistive to the grid, a controlled rectifier is implemented to ensure both a stable dc output voltage and a sinusoidal input current in phase with the grid voltage. There are several ways of controlling a power circuit to ensure a resistive grid-load. PFC controllers operating at a fixed frequency and varying duty-cycle are the most commonly employed controllers, thanks to their simple design and high power factor. One such control method is the Average Current Mode Control (ACMC) [11]. Fig. 1 shows a block diagram of the ACMC controller incorporated in a boost converter, one of the most common topologies for PFC applications.


Fig. 1: Average-current-mode control of a boost PFC converter [11].

The grid voltage, $v_{g}(t)$, is rectified using a full wave bridge rectifier, then fed to a switch-mode power supply (SMPS), in this case a boost converter. The boost converter has a conversion ratio, $M(t)$, ranging from one to infinity, ideally, which is essential to perform PFC. For the input current to follow the input voltage, the conversion ratio of the converter moves from a minimum level, $M_{\text {min }}$, to infinity, as illustrated in fig. 2.
The controller seen in fig. 1 is comprised of two control loops. A current controller, $G_{C}(s)$, which controls the shape of the input current, and a voltage controller, $G_{C V}(s)$, controlling the output voltage. The current controller takes a scaled version of the input voltage as a reference and compares it with the sensed input current. The voltage controller compares the output voltage with a reference voltage and generates a control signal, $v_{\text {control }}(t)$. This control signal is fed into a multiplier which multiplies the control signal by the input voltage and divides the quantity by the peak voltage squared of the input voltage, $V_{g, p e a k}^{2}$, to ensure correct power delivery. This is shown in (1), where $K_{v}$ is a factor which is dimensioned to the operating ranges of the input and output voltages to ensure


Fig. 2: Voltage and current waveforms of the boost PFC as well as conversion ratio $M(t)$ [11].
proper operation in the case of the minimum input ac voltage at the max output power.

$$
\begin{equation*}
v_{r e f 1}(t)=\frac{K_{v} \cdot v_{g, \text { rect }}(t) \cdot v_{\text {control }}(t)}{V_{g, p e a k}^{2}} \tag{1}
\end{equation*}
$$

The two controllers together set a control voltage to a pulse width modulation (PWM) generator that then controls the switch $Q_{1}$, such that the load seen by the grid is ideally resistive. These controllers are traditionally implemented using analog compensators. An analog proportional-integrating (PI) controller is shown in fig. 3. While well-known and easy to implement, analog controllers constitute a challenge for integration on an integrated circuit, due to the need for large passives, which increases the total area and price of the circuit. In many cases, they are employed as discrete passives, thus increasing the cost and bill of materials, as well as consuming area on the board. Furthermore, the generation of a PWM signal consumes a large die area if implemented monolithically. Additionally, analog compensators use voltage as the reference, whereas the trend of scaling transistor feature sizes continues, and so decreases the voltage supplies. This in turns results in less resolution on the controller, as the available reference range is reduced.


Fig. 3: Traditional analog PI controller.
On the other hand, digital controllers are incorporated in some cases. Fig. 4 shows the block diagram of a digital PI
controller. The error voltage is converted from analog to digital using an analog-to-digital converter (ADC). This digitized voltage is processed through digital compensation, where the proportional and integral control portions of the analog compensator are implemented using a gain scaler and a digital accumulator. A digital PWM (DPWM) then conducts the digital-to-time conversion and generates a duty-cycle signal proportional to the error voltage. While digital controllers can operate at a high switching frequency and eliminate the need for large passives, they produce additional ripples on the output voltage, which result from the quantization error introduced by the ADC and DPWM blocks. Reducing the ripple requires high precision ADC and DPWM blocks, thus adding complexity and increasing power consumption.


Fig. 4: Block diagram of a digital PI controller.

## III. Time-Based Controller

Time-based control is based on signal processing in the time domain [6] [7], where the error voltage is converted to a time signal using a voltage-to-time converter and the output is processed by a time-based compensator. The output of the compensator is a pulse-width modulated signal. Compared to the digital controller, time-based control eliminates the quantization error introduced by the ADC and DPWM blocks, thus behaving like a linear system in steady state, and achieving a small voltage ripple similar to the analog controller. Compared to both analog and digital controllers, the time-based controller eliminates the need for a PWM generator, as the PWM signal is inherently generated in time-based signal processing. Furthermore, the needs for large passives, high gain-bandwidth (GBW) error amplifiers, high-speed comparators, and ADC are obviated. Time-based control also enables converters operation at the VHF range ( $30-300 \mathrm{MHz}$ ), which is a main trend in switch-mode power converters design, in addition to being fully CMOS compatible, where it takes advantage of technology scaling and low feature-size devices, which allows for monolithic integration with the power switching devices. That makes it a main candidate for controller design towards the highly integrated PSiP and PwrSoC converters.
A time-based PI controller is shown in fig. 5. A voltagecontrolled oscillator (VCO) converts the error voltage into frequency, and as phase is the integral of frequency, the VCO acts as a voltage-to-phase integrator, thus providing both voltage-to-time conversion and integration functions. The proportional portion is implemented using a voltage-controlled delay line (VCDL) that incorporates a chain of tunable delay cells, providing voltage-to-time conversion with proportional function, as a time delay corresponds to a voltage gain in the voltage domain. A phase detector (PD) compares the phase of
the VCDL output signal with that of a reference clock that is generated from a replica VCO with an input bias voltage that sets the free-running frequency of the PWM signal. That frequency is designed to be equal to the switching frequency of the converter. The output of the PD is a PWM signal equivalent to the control signal in time domain.


Fig. 5: Block diagram of a time based PI controller.
While prior art reported time-based controllers for DC-DC buck converters with a single control loop to regulate the output voltage [8]-[10], this work investigates the employment of time-based controllers for an AC-DC boost PFC converter, where an additional control loop is added to control the input current, and the two time-based loops are combined to achieve a sinusoidal input current in phase with the input voltage, as well as a dc output voltage.

## A. Proposed Time-Based Control Scheme

Fig. 6 shows a block diagram of the proposed time-based ACMC PFC rectifier, with the two control loops synthesized in the time-domain, and combined using the multiplier circuit shown. By comparing this control scheme with the conventional controller shown in fig. 1, it is seen that each control loop is replaced by a time-based equivalent comprised of two VCOs, a VCDL, and a PD. It is also observed that the timebased controller eliminates the need for the PWM generator block, thanks to the inherent PWM generation capability.

## B. Voltage-Frequency and Gain-Delay Conversions

Fig. 7 shows a schematic for the VCO and VCDL circuits, which is functionally identical to the blocks shown in fig. 6. It is possible to design the transfer functions using conventional methods and then find the corresponding parameters for a time-based controller. Within the linear operation range of the VCO, the relationship between voltage and frequency is

$$
\begin{equation*}
\omega_{o u t}(t)=\omega_{f r}+K_{v c o} \cdot V_{v c o}(t) \tag{2}
\end{equation*}
$$

where $K_{v c o}$ is the voltage-to-frequency gain, $V_{v c o}(t)$ is the control voltage of the oscillator, $\omega_{f r}$ is the free running frequency of the reference VCO , and $\omega_{\text {out }}(t)$ is the output frequency of the VCO. The integral gain $K_{i}$ of a conventional PID controller is identical with $K_{v c o}(\mathrm{~Hz} / \mathrm{V})$ [9].

$$
\begin{equation*}
K_{i}=K_{v c o} \tag{3}
\end{equation*}
$$

The switching frequency of the power converter is set by $\omega_{f r}$.

$$
\begin{equation*}
f_{s w}=\frac{\omega_{f r}}{2 \pi} \tag{4}
\end{equation*}
$$



Fig. 6: Time-based average-current-mode control for a PFC boost converter.

The proportional gain $K_{p}$ is realized as the control gain of the VCDL, $K_{v c d l}(\mathrm{~s} / \mathrm{V})$.

$$
\begin{equation*}
K_{p}=K_{v c d l} \cdot 2 \pi \cdot f_{s w} \tag{5}
\end{equation*}
$$



Fig. 7: Schematic for the VCO and VCDL blocks.
In order to ensure linearity, the gains of the VCOs and VCDLs must be operating in their linear region. In previous work [12], a low gain, linear oscillator and delay line is implemented by varying the bias on a varactor at the output of the inverter cells.

## C. Phase Detector

Several varieties of phase detectors can be used for time-based controllers. The most common ones include the exclusive-OR phase detector (XOR PD), the two-state PD, and the tri-state PD. The XOR PD has a linear range which is equal to only $\pi$ and an output frequency of twice the input frequency. This would complicate the controller design dramatically and increase the impact of a parasitic pole [6] [7]. The two-state PD has a linear range of $2 \pi$. Thus, the two phases can not be more than $\pi$ apart, thereby limiting
the duty cycle to $50 \%$. This constitutes an issue for boost-converter-based PFC applications, as the controller utilizes the fact that the converter's voltage transfer ratio tends towards infinity when the duty cycle approaches $100 \%$. By using the tri-state PD , which has a linear range of $4 \pi$, it is possible to produce duty cycles up to $100 \%$ [12]. Fig. 8 shows a plot of the input-output relationship of the tri-state PD [7].


Fig. 8: Relationship between a phase difference at the input and the average output of a tri-state PD.

One persisting issue with the tri-state PD is the fact that when the duty cycle goes beyond $100 \%$, the signal flips over to $0 \%$, rather than decreasing linearly. The flipping of the signal beyond $2 \pi$ corresponds to a major non-linearity seen at the controller output. A solution to this problem was proposed and implemented in a buck converter in [9] [13] but for the two-state PD. The tri-state PD is recommended for time-based controllers in a PFC boost converter. However, it requires cautiousness during the design stage to ensure stability. Fig. 9 shows a conventional tri-state PD, which is functionally identical to the PD block shown in fig. 6.


Fig. 9: Tri-state phase detector.

## D. Combining the Two Loops

The proposed circuit for combining the two control loops necessary for PFC is shown in fig. 6. The circuit is able to multiply the rectified input voltage $v_{g, \text { rect }}(t)$ and the output of the time-based voltage controller $v_{\text {control }}(t)$. The circuit works by having the control signal operate two switches which connect the output to either $v_{g, \text { rect }}(t)$ or ground, depending on whether the control signal is high or low. The control signal is a PWM signal and the output voltage becomes a chopped version of $v_{g, \text { rect }}(t)$. The passives $R$ and $C$ filter this signal and provide the mean value of the chopped version of $v_{g, \text { rect }}(t)$. The value $K_{v} / V_{M}^{2}$ ensures that the multiplier provides the correct gain which yields the desired output
power. This gain is achieved with accurate scaling of the sensed current and voltages. The output voltage of the circuit can be expressed as

$$
\begin{equation*}
V_{\text {ref } 1}(t)=\frac{\operatorname{mean}\left(v_{\text {control }}(t) \cdot v_{g, \text { rect }}(t)\right) \cdot K_{v}}{V_{M}^{2}} \tag{6}
\end{equation*}
$$

It is seen that (6) provides the same expression as the conventional multiplier in (1), where $V_{M}=V_{g, p e a k}$. The bandwidth of the RC filter needs to be higher than the input rectified-voltage frequency of 100 Hz while still below the oscillation frequencies of the VCOs, i.e. the converter switching frequency.

## IV. Design

The proposed time-based control scheme is simulated for a boost PFC with the specifications listed in table I. The system functionality is verified using the system simulator CppSim [14], which is a behavioral simulation tool used for the design of phase-locked loops (PLLs) and other systems.

TABLE I: Design specifications for the boost PFC converter

| Input voltage $V_{\text {in }}$ | $230 \mathrm{~V}_{\text {rms }} 50 \mathrm{~Hz}$ |
| :--- | :--- |
| Output voltage $V_{\text {out }}$ | 400 V |
| Output Power $P$ | 600 W |
| Operating frequency $f_{s w}$ | 50 kHz |

## A. Controller Gains

Controller gains are evaluated for each of the control loops. First, the current controller gains are obtained using the boost converter's duty-cycle-to-input-current transfer function. The boost PFC duty-cycle-to-input-current response, controller response and the corresponding loop gain for the current controller are shown in fig. 10. The current controller is shown to have a crossover frequency of 18 kHz and a phase margin of $100^{\circ}$. Second, the voltage controller gains are evaluated using the transfer function from the input of the multiplier, with the current controller, to the output voltage of the boost PFC. The boost PFC $V_{\text {control }}$-to- $V_{\text {out }}$ response, controller response and the corresponding loop gain for the voltage controller are shown in fig. 11. The voltage controller is shown to have a crossover frequency of 1.3 Hz and a phase margin of $90^{\circ}$. The time-based circuit parameters are then obtained using the conversion of the $K_{i}$ and $K_{p}$ to $K_{v c o}$ and $K_{v c d l}$ presented in the previous section. The values are shown in table II.

TABLE II: Time-based control circuit parameters

|  | Current Controller | Voltage Controller |
| :--- | :--- | :--- |
| $K_{v c o}$ | $377 \mathrm{~Hz} / \mathrm{V}$ | $62.84 \mathrm{~Hz} / \mathrm{V}$ |
| $K_{v c d l}$ | $3.18 \mu \mathrm{~s} / \mathrm{V}$ | $15.92 \mu \mathrm{~s} / \mathrm{V}$ |

## B. Multiplier Circuit Parameters

As mentioned in section III, the multiplier circuit proposed in this work has to have a bandwidth which is above the 100 Hz of the rectified input voltage and below the converter switching frequency, i.e. 50 kHz . Since the phase detector is by nature a sample system, the bandwidth of the multiplier must be kept


Fig. 10: Bode plot of the current controller $G_{c}(s)$.


Fig. 11: Bode plot of the voltage controller $G_{c v}(s)$.
a decade lower than the switching frequency, to ensure the validity of the linear models for the transfer functions. The bandwidth is set to

$$
\begin{equation*}
f_{3 d B, \text { mult }}=\frac{1}{2 \pi R C} \approx 4.5 \mathrm{kHz} \tag{7}
\end{equation*}
$$

where the values of the passives $R$ and $C$ are chosen accordingly. It is noted that these passives sizes are indirectly proportional to the switching frequency of the converter, where the higher the switching frequency is, the smaller the sizes for $R$ and $C$ will be, which aids with the passives integration on the same die for high switching frequency designs, and that can result in full monolithic integration of the converter. Table III lists the values for the passive components bill-of-materials (BoM) shown in fig. 6 .

TABLE III: Passive components BoM

| Component | Value |
| :--- | :--- |
| $L_{1}$ | 4.34 mH |
| $C_{\text {out }}$ | $600 \mu \mathrm{~F}$ |
| $R_{\text {load }}$ | $266.7 \Omega$ |
| $C$ | 3.5 pF |
| $R$ | $10 \mathrm{M} \Omega$ |

## V. Model Results

This section shows the results of the boost PFC time-based control scheme model simulated in CppSim. Fig. 12 shows the moving average (low-frequency envelope of 50 kHz signal) of the control signals from the voltage and current controllers respectively. It can be seen that in steady-state operation, the voltage control signal is almost constant, with minimal variation around the dc value for achieving a low 100 Hz ripple on the output voltage. On the other hand, the current control signal is varying with the input voltage, regulating the input current, and going in accordance with the conversion ratio waveform shown in fig. 2.


Fig. 12: Moving average of voltage and current controllers outputs from the model results.


Fig. 13: Input voltage, input current and output voltage from the model results.

Fig. 13 shows the converter input voltage, input current and output voltage. It can be seen that the PFC boost converter is able to maintain a low ripple dc output voltage whilst having an in-phase sinusoidal input current and voltage. The power factor is evaluated to 0.99 at 600 W of output power.

## VI. Conclusion

A time-based control scheme for a boost PFC converter is presented. The controller is based on the average current mode control, with the PI control loops implemented in timedomain using VCOs, VCDLs and tri-state phase detectors. A multiplier circuit is proposed for combining the two timebased control loops. The system functionality is verified on the system simulator CppSim for a 600 W PFC boost converter with a 400 V dc output and $230 \mathrm{~V}_{\text {rms }} 50 \mathrm{~Hz}$ input voltages. Results show a stable output voltage with a small ripple, and a low-harmonic-content input current in phase with the input voltage, achieving a power factor of 0.99 .

## References

[1] F. Waldron, R. Foley, J. Slowey, A. N. Alderman, B. C. Narveson, and S. C. OMathuna, "Technology Roadmapping for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC)," IEEE Transactions on Power Electronics, vol. 28, no. 9, pp. 4137-4145, September 2013.
[2] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 1-14, 2009.
[3] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. E. Andersen, "Evolution of Very High Frequency Power Supplies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 28, no. 9, September 2014.
[4] IEEE 519. IEEE Recommended Practice And Requirements For Harmonic Control In Electric Power Systems, 2014.
[5] IEC 61000-3-2, Fifth Edition, International Electrotechnical Commission, 2018.
[6] B. G. Drost, "Time-Based Analog Signal Processing," Master's thesis, Oregon State University, June 2011.
[7] B. Dorst, M. Talegaonkar, and P. K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," IEEE Journal of Solid-State Circuits, vol. 47, no. 12, December 2012.
[8] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-Phase $30-70 \mathrm{MHz}$ Switching Frequency Buck Converter Using a Time-Based Compensator," IEEE Journal of SolidState Circuits, vol. 50, no. 12, December 2015.
[9] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High Frequency Buck Converter Design Using Time-Based Control Techniques," IEEE Journal of Solid State Circuits, vol. 50, no. 4, pp. 990-1001, April 2015.
[10] S. J. Kim, W. Choi, R. Pilawa-Podgurski, and P. K. Hanumolu, "A $10 \mathrm{MHz} 2-800-\mathrm{mA} 0.5-1.5-\mathrm{V} 90 \%$ Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes," IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 814-824, March 2018.
[11] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed., 2007.
[12] M. Perrott, "Integer-N Frequency Synthesizers," Phase-Locked Loops and their Applications, August 2008.
[13] J. Zhang and S. Sanders, "An Analog CMOS Double-Edge Multi-Phase Low-Latency Pulse Width Modulator," IEEE Applied Power Electronics Conference (APEC), 2007.
[14] M. H. Perrott, CppSim/VppSim Primer, version 5.3 ed., 2014.

## Appendix [C6]

A. M. Ammar, K. Ali, and D. Rogers, "A Bidirectional GaN-Based CLLC Converter for Plug-In Electric Vehicles On-Board Charger," submitted to IECON 2020-46th Annual Conference of the IEEE Industrial Electronics Society.

# A Bidirectional GaN-Based CLLC Converter for Plug-In Electric Vehicles On-Board Chargers 

Ahmed M. Ammar<br>Department of Electrical Engineering<br>Technical University of Denmark<br>Kongens Lyngby, Denmark<br>ammma@elektro.dtu.dk

Kawsar Ali and Dan Rogers<br>Department of Engineering Science<br>University of Oxford<br>Oxford, United Kingdom<br>\{kawsar.ali, dan.rogers\}@eng.ox.ac.uk


#### Abstract

This paper presents a bidirectional CLLC converter solution for the dc-dc stage in plug-in electric vehicle (PEV) onboard battery chargers. The proposed architecture allows the converter to operate at resonance for the bidirectional constantpower (CP) load range with a variable bus voltage, while frequency modulation is employed for the constant-current (CC) load range in the grid-to-vehicle (G2V) mode with a fixed bus voltage, resulting in a limited bus voltage range. This enables the use of $650-\mathrm{V}$ Gallium nitride ( GaN ) devices for the primary and secondary sides' switches. The design flow is presented and a 1kW high-frequency prototype is implemented. GaN reverse conduction characteristics are investigated and employed for the high-frequency current rectification. The prototype operates with soft switching across the operational range, achieving an efficiency of up to $\mathbf{9 5 . 7 \%}$, with the resonant inductances integrated in the transformer.


Keywords-Electric vehicles, dc-dc converters, resonant power conversion, wide bandgap semiconductors, bidirectional converters

## I. Introduction

As the world is moving towards green energy as a replacement for the traditional fossil-fuel-based systems, electric vehicle (EV) technology is advancing, with a rapidly growing market. Plug-in electric vehicles (PEVs), which include plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs), are gaining wider adoption, thanks to their efficient energy utilization and reduced combustion emission. In addition, with the recent advancements in the smart-grid technology, bidirectional power flow in PEV battery chargers is necessary to provide the vehicle-to-grid (V2G) support. V2G helps support the grid during voltage sags and frequency dips, especially given the higher dependence of the grid on renewable energy sources. In addition, bidirectional chargers enable consumers to use their EV stored energy for local consumption during power outages, as in the vehicle-to-home (V2H) and vehicle-to-load (V2L) technologies (together with V2G, these are referred to as V2x [1]). Accordingly, new technologies in PEV charger systems are needed to cope with the demand for lightweight, small size, and efficient PEV on-board chargers.

Wide bandgap (WBG) semiconductors technology has greatly evolved and can currently offer many advantages over silicon devices, including much better figures of merit and reduced reverse recovery charge [2]. That has allowed designers to push operational frequencies higher, resulting in higher power densities. For applications with requirements for high efficiency, and at a high switching frequency, soft-switching topologies can
help make the most of WBG devices through the elimination of turn-on losses.

The conventional architecture of a PEV battery charging system is a two-stage solution, as shown in Fig. 1. A front-end ac-dc converter rectifies the grid voltage and provides power factor correction (PFC), and a following dc-dc stage regulates the intermediate bus voltage into the respective load voltage/current based on the battery state-of-charge (SoC). While the bridgeless totem-pole boost is commonly used for the first stage, two common topologies for dc-dc stage are the phaseshifted full-bridge converter, and the dual active bridge (DAB) converter [3]. However, with the wide output voltage range of state-of-the-art battery technologies, both topologies are limited with respect to the load range for which zero-voltage switching (ZVS) is achieved. On the other hand, the $L L C$ converter can achieve ZVS under any load conditions, making it a good candidate for servers and telecom applications [4]. Nevertheless, it is incapable of the reverse power flow necessary in bidirectional applications with its asymmetric resonant tank [5].

This paper presents a bidirectional $C L L C$ resonant converter for the dc-dc stage in modular level-2 on-board chargers. The operation is similar to the conventional $L L C$ converter, with an added $L C$ tank on the secondary side of the transformer [6], [7]. A variable dc-bus voltage allows the converter to operate at resonance for the entirety of the bidirectional mode, whereas switching frequency modulation is employed for the low battery voltage range in the grid-to-vehicle (G2V) mode, resulting in a reduced dc-bus voltage range. That, in turn, allows for the use of $650-\mathrm{V} \mathrm{GaN}$ devices for both the primary and secondary sides' switches. A $1-\mathrm{kW}$ high-frequency prototype is designed and implemented. The prototype operates the rectifying devices in reverse conduction and the associated loss is quantified. The high-frequency transformer integrates the resonant tank series inductances, reducing the component count and allowing for high power density.

This paper is organized as follows. Section II shows the system architecture of the proposed converter. Converter design and implementation procedure is presented in Section III. Section IV shows the experimental results of the implemented prototype. Conclusion is then provided in section V.


Fig. 1. Conventional PEV charger system architecture.

## II. System Architecture

## A. Variable bus voltage

A typical 400-V EV propulsion battery pack has a terminal voltage of around 250 V at the lowest SoC, which increases to 450 V at the highest SoC along the battery charging profile. The fast charging profile consists of two modes [8]. A constantcurrent (CC) mode for the battery voltage range of 250 V to 320 V , and a constant-power (CP) mode for the range between 320 V and 450 V . The battery discharge operation in V2G mode is only applicable for the CP range as the battery stops delivering power when its voltage reaches 320 V . While a fixed bus voltage is typical in two-stage systems, it would require the dcdc stage to transform a fixed $V_{\text {bus }}$ to the widely varying battery voltage. In the case of resonant converters, which operate most efficiently at the resonant frequency, the overall system efficiency would be compromised with operation below and above resonance to provide the needed voltage gain. Accordingly, prior art reported a varying $V_{\text {bus }}$ voltage to enable the resonant dc-dc stage to work largely or entirely at resonance [9], with a unity voltage gain, which achieves the optimal efficiency for the dc-dc stage. The tradeoff in that case is the requirement for high-voltage (1000-1200 V) silicon (Si) or silicon carbide ( SiC ) switches for the primary side devices in the dc-dc stage, in addition to the PFC stage switches.

In this work, a limited bus voltage range is used as the input for the dc-dc stage. Fig. 2 illustrates the bus and battery voltage ranges with the converter modes of operation, where $f_{s}$ and $f_{r}$ are the switching and resonant frequencies, respectively. The converter is designed to operate at resonance, with unity voltage gain, for the entirety of the CP load mode. This eliminates the contribution of the resonant tank voltage gain to the overall converter voltage gain, which is provided through the transformer turns-ratio $n$, thus ensuring symmetry for bidirectional operation. With a minimum $V_{\text {bus }}$ voltage of 380 V , which is the minimum output voltage of a conventional boost/totem-pole converter operating from universal mains input, the required turns-ratio is calculated by

$$
\begin{equation*}
n=\frac{V_{\text {bus_min }}}{V_{C P_{-} \min }}=1.19, \tag{1}
\end{equation*}
$$

where $V_{C P \text { min }}$ is the minimum battery voltage for the CP load mode ( 320 V in the defined charging profile). Designing for a turns-ratio of 1.2, the minimum and maximum voltages for $V_{b u s}$ are calculated to 384 and 540 V, as shown in Fig. 2. For the CC load range, switching frequency modulation is applied on the minimum input voltage of 380 V , where the resonant tank provides additional step-down voltage gain on top of the transformer turns-ratio in order to deliver the battery terminal voltage of 320 V down to 250 V .

Although the converter operation is not entirely at resonance as in [9], high efficiency can still be achieved as the converter operates at resonance for the entire CP load range, with a reduced frequency modulation operation for the CC load range. At the same time, the need for boost gain in the resonant tank is eliminated, which simplifies the tank design, especially with respect to the magnetic devices. Critically, the reduced $V_{b u s}$


Fig. 2. Converter modes of operation with the presented architecture.
TABLE I. COMPARISON of Primary Side Devices with the Same Current Rating (30 A)

| Application | $[8]$ | $[9]^{*}$ | This work |
| :---: | :---: | :---: | :---: |
| Max. $V_{\text {bus }}[\mathrm{V}]$ | 680 | 840 | 540 |
| Device | C 3 M 0065100 K | C 3 M 0075120 J | GS 66508 T |
| Technology | SiC | SiC | GaN |
| Breakdown Voltage $[\mathrm{V}]$ | 1000 | 1200 | 650 |
| $R_{\text {os(on) }}$ @ $25^{\circ} \mathrm{C}[\mathrm{m} \Omega]$ | 65 | 75 | 50 |
| $Q_{g}[\mathrm{nC}]$ | 35 | 51 | 5.8 |
| $E_{\text {oss }} @ \max . V_{\text {bus }}[\mu \mathrm{J}]$ | 18 | 25 | 10 |
| $Q_{r r}[\mathrm{nC}]$ | 310 | 220 | 0 |
| FoM1 $=R_{D S(o n)} \cdot Q_{g}$ | $2.28 \mathrm{E}-09$ | $3.83 \mathrm{E}-09$ | $2.90 \mathrm{E}-10$ |
| $\mathrm{E}-\mathrm{FoM}=R_{\text {os }(o n)} \cdot E_{\text {oss }}$ | $1.17 \mathrm{E}-06$ | $1.88 \mathrm{E}-06$ | $0.50 \mathrm{E}-06$ |

* The 100-A device used in this reference is replaced with a 30-A device for the same rated voltage for a better comparison.
range allows for the incorporation of $650-\mathrm{V}$ GaN devices for both the primary and secondary switches, whereas prior art reports higher maximum bus voltages, and accordingly SiC devices are incorporated for the ac-dc stage and the primary switches in the dc-dc stage. Table I shows a comparison between the device employed in this work with the state-of-theart devices incorporated in prior art. The comparison shows that a GaN device rated for the same current and a lower breakdown voltage has significantly better figures of merit compared to the SiC counterparts. That can lead to the improvement of the overall system efficiency with the incorporation GaN devices in both stages. Furthermore, the GaN device has zero reverserecovery charge. As a result, the presented work investigates and employs the reverse conduction characteristics for the resonant tank high-frequency current rectification. This simplifies the design and eliminates the need for synchronous driving circuitry or matching circuits in the resonant tank.


## B. Converter Topology

The CLLC converter schematic is shown in Fig. 3. Halfbridge switch networks are employed for the primary and secondary sides. The switch voltages are confined by the dcbus and battery voltages. Depending on the power flow direction, the inverting half bridge is switched at the switching frequency with $50 \%$ duty cycle and fixed dead time, while the rectifying half-bridge operates in reverse conduction throughout the entirety of the switching period. ZVS is achieved at turn-on for the inverting devices at all loads. The resonant tank is designed to offer symmetric operation across both power directions, where the transformer leakage inductance is part of the resonant tank, allowing for the

$$
\begin{equation*}
M_{r}=\frac{k \cdot f_{n}{ }^{3}}{\sqrt{\left[Q_{l} \cdot\left(f_{n}{ }^{4} \cdot(1+2 k)-f_{n}{ }^{2} \cdot(2+2 k)+1\right)\right]^{2}+\left[f_{n} \cdot\left(1-f_{n}{ }^{2} \cdot(1+k)\right)\right]^{2}}} \tag{2}
\end{equation*}
$$

integration of the resonant inductors in the transformer. Equation (2) shows an expression for the resonant tank gain (excluding transformer turns ratio) derived based on the first harmonic approximation (FHA) approach for analyzing resonant converters. The quantities $f_{n}, Q_{l}$, and $k$ are the normalized switching frequency, the loaded quality factor, and the ratio between the transformer magnetizing inductance and the primary resonant inductance, respectively. They are defined as follows:

$$
\begin{gather*}
f_{n}=\frac{f_{s}}{f_{r}}  \tag{3}\\
Q_{l}=\frac{\sqrt{L_{r p} / C_{r p}}}{R_{r}}  \tag{4}\\
k=\frac{L_{m}}{L_{r p}}, \tag{5}
\end{gather*}
$$

where $R_{r}$ is the load resistance $R_{l}$ reflected at the rectifier input and referred to the primary side.

$$
\begin{gather*}
f_{r}=\frac{1}{2 \pi \sqrt{L_{r p} \cdot C_{r p}}}  \tag{6}\\
R_{r}=\frac{2 n^{2} \cdot R_{l}}{\pi^{2}} \tag{7}
\end{gather*}
$$

## III. Design \& Implementation

## A. Design Specifications

Table II lists the specifications for the dc-dc stage design based on the architecture discussed in Section II, where different operational points are identified for the different load modes and power directions. Point A corresponds to the operation at the terminal voltage of the battery low SoC, with the minimum battery voltage of 250 V . Point B corresponds to the border between the CC and CP modes, with a battery voltage of 320 V . Points C and D then lie along the CP charging mode, with point D corresponding to the terminal voltage at the battery high SoC. On the other hand, points BR-DR represent the reverse power flow in the V2G mode. The $1-\mathrm{kW}$ power specification targets modular level-2 on-board chargers, where the same design can be scaled for higher power. A maximum switching frequency of 500 kHz is chosen for this design, which
makes a good tradeoff between the power density and efficiency, considering the range of high frequencies that the state-of-the-art magnetic materials allow for.

## B. Resonant Tank Design

The main design goal is to maintain soft switching operation across the entire charging cycle. The design process starts with the calculation of the minimum needed resonant tank gain.

$$
\begin{equation*}
M_{r_{\_} \min }=\frac{V_{\text {batt_min }} \cdot n}{V_{\text {bus_min }}}=0.78 \tag{8}
\end{equation*}
$$

With a specified maximum switching frequency, and choosing a maximum normalized switching frequency of 1.25 , which is not too far from the resonant frequency, ensuring the validity of the FHA approach, the resonant frequency is calculated to

$$
\begin{equation*}
f_{r}=\frac{f_{s_{\_} \max }}{f_{n_{\_} \max }}=400 \mathrm{kHz} \tag{9}
\end{equation*}
$$

Following, a preliminary value for $k$ is chosen. The value for the parameter $k$ constitutes a tradeoff between the maximum gain and efficiency. A low $k$ value results in peaking of the resonant tank gain curve below resonance for the same quality factor, providing boost function and extending the inductive mode of operation below the resonant frequency. At the same time, the low $k$ value is achieved with a smaller transformer magnetizing inductance $L_{m}$, which, in turn, results in higher magnetizing current that results in increased conduction losses. On the other hand, if the $k$ value is made too high, the magnetizing current can be too small to deplete the inverter devices' output capacitances before turn on (for the same dead time), resulting in partial or full loss of ZVS. For the presented architecture, where no boost gain is needed in the resonant tank, the choice of the $k$ value solely depends on the ZVS operation of the converter. The optimal design is the one with the highest $k$ value that helps reduce the magnetizing current to the limit that guarantees ZVS at all conditions with minimized circulating energy. Starting with a value of $k=10$, which allows for easy integration of the resonant tank series inductances into the transformer leakage inductance, (2) is plotted in Matlab against $f_{n}$ for different values of $Q_{l}$, shown in Fig. 4. The maximum loaded quality factor, respective to point $A$, is defined by selecting the curve that achieves the required minimum gain $M_{r_{-} \text {min }}$ at the maximum normalized frequency


Fig. 3. CLLC converter schematic.

TABLE II. DESIGN Specifications

| Power Flow | Forward (G2V) |  |  |  | Reverse (V2G) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Load Mode | CC | CP |  | CP |  |  |  |
| Point $(i)$ | A | B | C | D | BR | CR | DR |
| $V_{\text {in }}[\mathrm{V}]$ | 380 | 384 | 504 | 540 | 320 | 420 | 450 |
| $V_{\text {out }}[\mathrm{V}]$ | 250 | 320 | 420 | 450 | 384 | 504 | 540 |
| $I_{\text {out }}[\mathrm{A}]$ | 3.13 | 3.13 | 2.38 | 2.22 | 2.6 | 1.98 | 1.85 |
| $P_{\text {out }}[\mathrm{W}]$ | 781.25 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 |



Fig. 4. Resonant tank gain across the normalized switching frequency for different loads for $k=10$.


Fig. 5. Resonant tank gain across the normalized switching frequency for different loads for $k=5$.
TABLE IV. LOADED QUALITY FACTORS FOR THE MAIN OPERATIONAL POINTS FOR DIFFERENT K VALUES

| $k$ | 10 | 5 |
| :--- | :--- | :--- |
| $Q_{L A}$ | 0.82 | 0.75 |
| $Q_{L B}$ | 0.64 | 0.59 |
| $Q_{L C}$ | 0.37 | 0.34 |
| $Q_{L D}$ | 0.33 | 0.3 |

$f_{n_{-} \max }$. Having defined the maximum $Q_{l}$, the corresponding values for the other operational points are calculated as follows.

$$
\begin{equation*}
Q_{l_{-} i}=\frac{Q_{l_{-} \max } \cdot R_{l_{-} \max }}{R_{l_{-} i}} \tag{10}
\end{equation*}
$$

The values are listed in Table III. As the operational points B, C, and D operate at resonance, ZVS is ensured (by design) by maintaining a lag between the resonant current and switching node voltage at resonance. By checking the respective load curves at $f_{n}=1$, it is observed that achieving ZVS at resonance with $k=10$ is challenging. Accordingly, a design iteration with respect to a lower $k$ value is conducted. Fig. 5 shows the gain function for $k=5$ at the same loads, where higher boost gains
are achieved below resonance. A maximum $Q_{l}$ value of 0.75 is defined and the respective values for the other loads are calculated and listed in Table III. Circuit simulations are then conducted for the different operational points for forward and reverse power directions to validate gains and ZVS operation for the different $k$ values. It is found that $k=5$ ensures a wider range of operation with ZVS, leading to a higher efficiency. Following, the resonant tank values are calculated as follows:

$$
\begin{gather*}
L_{r p}=\frac{Q_{l_{-} \max } \cdot R_{r_{-} \max }}{2 \pi f_{r}}=6.96 \mu \mathrm{H}  \tag{11}\\
C_{r p}=\frac{1}{2 \pi f_{r} \cdot Q_{l_{-} \max } \cdot R_{r_{-} \max }}=22.7 \mathrm{nF}  \tag{12}\\
L_{r s}=\frac{L_{r p}}{n^{2}}=4.84 \mu \mathrm{H}  \tag{13}\\
C_{r s}=C_{r p} \cdot n^{2}=32.7 \mathrm{nF}  \tag{14}\\
L_{m}=k \cdot L_{r p}=34.8 \mu \mathrm{H} \tag{15}
\end{gather*}
$$

## C. Implementation

Table IV lists the bill of material of the presented converter, including the designed and implemented values. For the switching devices, the GaN systems GS66508T devices are incorporated, as they offer the best-in-class figures of merit compared to other commercial devices for the same voltage and power. The 3 F46 magnetic material is selected for the transformer core, as it has low losses at the design switching frequency. A P-36/22 core is used and the primary and secondary windings are divided between the core halves and separated, in order to achieve a low coupling coefficient aiding with the integration of the resonant tank series inductances in the transformer leakage inductance, thus saving the space and cost for two additional magnetic devices. The primary winding is realized using 14.5 turns of $140 \times 90 \mu \mathrm{~m}$ Litz wire over three layers, while 3 layers of 4 turns each from the same-type wire are used for the secondary winding realization. An air gap of 2.6 mm is implemented and distributed equally between the inner and outer core legs. A 3D-printed custom bobbin is used to provide 2 mm separation between the windings to achieve the desired coupling coefficient. The separation also provides clearance of the windings turns around the airgap, which reduces the effect of the fringing flux and the losses associated with it. The transformer small-signal characterization is conducted using an N4L PSM1735 phase sensitive meter with an impedance analyzer interface. The obtained magnetizing inductance is less than that designed for, as shown in Table IV, resulting in an effective $k$ value of about 3.2.

TABLE III. PROTOTYPE BOM

| Component | Design | Prototype | Type |
| :--- | :--- | :--- | :--- |
| $C_{\text {bus }}$ |  | $5.64 \mu \mathrm{~F}$ | Ceramic |
| $Q_{h p}, Q_{l p}$ |  | $2 * \mathrm{GS} 66508 \mathrm{~T}$ | GaN Switches |
| $C_{r p}$ | 22.7 nF | 22.4 nF | Film |
| $C_{r s}$ | 32.7 nF | 32.4 nF | Film |
| $L_{r}$ | $13.92 \mu \mathrm{H}$ | $13.4 \mu \mathrm{H}$ | Custom Design |
| $L_{m}$ | $34.8 \mu \mathrm{H}$ | $21.54 \mu \mathrm{H}$ | Custom Design |
| $C_{\text {batt }}$ |  | $5.64 \mu \mathrm{~F}$ | Ceramic |



Fig. 6. Scope captures for different operational points. $\mathrm{CH} 1: V_{S W_{-} P} 250 \mathrm{~V} / \mathrm{div}, \mathrm{CH} 2: I_{R_{-} P}$ at $5 \mathrm{~A} / \mathrm{div}, \mathrm{CH} 3: V_{S W_{-} S}$ at $250 \mathrm{~V} / \mathrm{div}$, and CH4: $I_{R_{-} S}$ at $5 \mathrm{~A} / \mathrm{div}$. (a) Point A, (b) point B, (c) point C, (d) point BR, (e) point CR, and (f) point DR.

With the implemented resonant capacitances, the resonant frequency is measured as 391 kHz .


Fig. 9. Obtained power and efficiency across the different operational points.

## IV. RESULTS

## A. Lab setup

A thermal camera (Testo 875) continuously monitors the converter operation, and a $350 \mathrm{MHz} 2.5 \mathrm{GS} / \mathrm{s}$ oscilloscope (Yokogawa DLM4038) displays the high-frequency signals. The primary and secondary half bridges switching nodes are displayed using $150-\mathrm{MHz}$ differential probes (Yokogawa PBDH0150); whereas the currents are displayed using $100-\mathrm{MHz}$ current probes (Agilent N2783A). A low-voltage DC power supply (EA-PS 2342-10 B) supplies the driving circuit, and a $750-\mathrm{V}$ 1500-W power supply (EA-PSI 9750-06 DT) acts as power source. On the other hand, a $750-\mathrm{V} 15-\mathrm{kW}$ bidirectional DC power supply (EA-PSB 9750-60) acts as the load. The source and load connections are interchanged across the converter terminals to test forward and reverse power flows.

## B. Measurements

Fig. 6 shows scope captures for the different operational points discussed in the previous section. It can be observed that active switching takes place on the primary half-bridge switches in subfigures (a-c), where the secondary half-bridges are in reverse conduction for the entirety of the switching period. On the other hand, the roles are changed for the operational points in subfigures (d-f) for which reverse power flow takes place by actively switching the secondary half-bridge, while the primary half-bridge switches reverse conduct. The primary and secondary switching nodes voltages are seen to overlap across all figures with operation at resonance, while a phase shift between the two voltages exists in subfigure (a) where the switching frequency is higher than the resonant frequency and a lower output voltage is achieved. Soft switching is achieved across the different operational points in both power directions.


Fig. 7. Measured GS66508T device reverse conduction characteristics across different temperatures.


Fig. 8. Converter loss distribution for point B in Watts.
Fig. 9 shows the obtained output power and efficiency across the different operational points for both power directions. The figure illustrates that an efficiency of up to $95.7 \%$ is obtained, with an average efficiency of $95.2 \%$ across the load range. The gain and power mismatches at several points are due to the differences between designed and implemented values of the resonant tank and can be eliminated with the accurate setting of the switching frequency.

## C. GaN Reverse Conduction Characteristics

Considering that the GaN device has zero reverse recovery charge $\left(Q_{R R}\right)$, the loss due to reverse conduction can be estimated as follows. From Fig. 6, it can be seen that the maximum resonant current amplitude takes place on the secondary side at point B , where a sinusoidal current with an amplitude of 10.1 A is measured. Fig. 7 shows measurement results for the reverse conduction characteristics of the employed GaN device across different temperatures with zero gate-source voltage (obtained using a Keysight B1505A curve tracer). By inspecting the characteristics, the corresponding device voltages for the resonant current values along the sine wave are extracted. The average power loss due to reverse conduction $P_{r c}$ is then calculated as follows.

$$
\begin{equation*}
P_{r C}=\frac{1}{T_{s}} \int_{0}^{T_{S}} I_{D S}(t) \cdot V_{D S}\left(I_{D S}(t)\right) d t=17.3 \mathrm{~W} \tag{16}
\end{equation*}
$$

Fig. 8 illustrates the converter power loss breakdown at the same operational point. The figure shows that about one third of the total power loss is taking place in the rectifying switches reverse conduction. Accordingly, this design offers simplicity and lower
cost by eliminating the need for a complex synchronous driving circuitry or a matching network in the resonant tank at the expense of additional power loss with the reverse conduction of the rectifying devices.

## V. Conclusion

A bidirectional CLLC resonant dc-dc converter for on-board EV charger systems is presented. The proposed architecture allows the converter to operate at resonance for the bidirectional constant-power load range, while frequency modulation is employed for the constant-current load range along the battery charging profile. This enables a limited bus voltage range, allowing for the use of $650-\mathrm{V} \mathrm{GaN}$ devices for both the primary and secondary switches, and simplifying the requirements on the preceding ac-dc stage. A high-frequency $1-\mathrm{kW}$ prototype with integrated magnetics is implemented. The prototype operates in ZVS across load range, achieving up to $95.7 \%$ efficiency, with the resonant tank series inductances integrated in the transformer. GaN reverse-recovery characteristics are exploited for the rectifying switches to eliminate the need for synchronous driving scheme or a matching network in the resonant tank. One third of the total power loss is dissipated in rectification, thus constituting a tradeoff between efficiency and simplicity/cost.

## References

[1] A. Khaligh and M. D'Antonio, "Global Trends in High-Power On-Board Chargers for Electric Vehicles," in IEEE Transactions on Vehicular Technology, vol. 68, no. 4, pp. 3306-3324, April 2019.
[2] E. Hoene, G. Deboy, C. R. Sullivan and G. Hurley, "Outlook on Developments in Power Devices and Integration: Recent Investigations and Future Requirements," in IEEE Power Electronics Magazine, vol. 5, no. 1, pp. 28-36, March 2018.
[3] P. He and A. Khaligh, "Comprehensive Analyses and Comparison of 1 kW Isolated DC-DC Converters for Bidirectional EV Charging Systems," in IEEE Transactions on Transportation Electrification, vol. 3, no. 1, pp. 147-156, March 2017.
[4] A. M. Ammar, Y. Nour, and A. Knott, "A High-Efficiency 1 MHz 65 W GaN-Based LLC Resonant DC-DC Converter," 2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE), Aswan, 2019.
[5] J. Deng, S. Li, S. Hu, C. C. Mi and R. Ma, "Design Methodology of LLC Resonant Converters for Electric Vehicle Battery Chargers," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1581-1592, May 2014.
[6] J. Jung, H. Kim, M. Ryu and J. Baek, "Design Methodology of Bidirectional CLLC Resonant Converter for High-Frequency Isolation of DC Distribution Systems," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1741-1755, April 2013.
[7] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen and J. Lai, "Design of Bidirectional DC-DC Resonant Converter for Vehicle-to-Grid (V2G) Applications," in IEEE Transactions on Transportation Electrification, vol. 1, no. 3, pp. 232-244, Oct. 2015.
[8] 6.6 kW Bi-Directional EV On-Board Charger, Cree Power Applications, Application Note CPWR-AN25, Rev B, July 2018.
[9] B. Li, Q. Li, F. C. Lee, Z. Liu and Y. Yang, "A High-Efficiency HighDensity Wide-Bandgap Device-Based Bidirectional On-Board Charger," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1627-1636, Sept. 2018.

Technical
University of
Denmark
Department of Electrical Engineering
Ørsteds Plads
Building 348
DK-2800 Kongens Lyngby, Denmark
Phone: +45 45253800
E-mail: elektro@elektro.dtu.dk
www.elektro.dtu.dk


[^0]:    General rights
    Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

    - Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
    - You may not further distribute the material or use it for any profit-making activity or commercial gain
    - You may freely distribute the URL identifying the publication in the public portal

    If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

[^1]:    ${ }^{1}$ Resonant inductor is mounted on the bottom side of the circuit board.

[^2]:    This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark (e-mail:

[^3]:    ammma@elektro.dtu.dk; frmsp@elektro.dtu.dk; ynour@elektro.dtu.dk; akn@elektro.dtu.dk).

    Part of this work has been presented at the 2019 IEEE 20th Workshop on Control and Modeling for Power Electronics in Toronto, Canada.

[^4]:    This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark (e-mail: frmsp@elektro.dtu.dk; ammma@elektro.dtu.dk; ynour@elektro.dtu.dk; akn@elektro.dtu.dk).

[^5]:    This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark (e-mail: ammma@elektro.dtu.dk; frmsp@elektro.dtu.dk; ynour@elektro.dtu.dk; akn@elektro.dtu.dk).

[^6]:    This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466.

[^7]:    This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466 and from the Danish Energy Development and Demonstration Platform (EUDP) under journal number 64014-0558.

