Fast Estimation of Phase Angle for Three-Phase Voltage Systems under Distorted Conditions

Reza, Md Shamim; Hossain, Md Maruf; Nasif, Ahmed O.; Agelidis, Vassilios G.

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

Link to article, DOI:
10.1109/JESTPE.2020.3044058

Publication date:
2022

Document Version
Peer reviewed version

Link back to DTU Orbit

Citation (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
Abstract—This paper proposes a fast and robust technique for instantaneous phase angle estimation of three-phase voltage systems under unbalanced and distorted conditions. It mainly relies on the Clarke transformation, Teager energy operator and delayed signal cancellation (DSC) approach. Unlike an adaptive DSC-based synchronous-reference frame phase-locked loop (PLL), the proposed technique avoids interdependent loops, thus increasing the overall stability and easing the tuning process. Moreover, it removes the phase loop of the PLL, hence eliminates the requirement of in-loop filter (low-pass filter) and/or loop filter (proportional plus integral controller). As a result, the tuning of these filters is not required and a quicker response is produced. The proposed technique also avoids inverse trigonometric function operation. In addition, it shows harmonics immunity at steady-state and can generate fast dynamic response with a settling time less than one nominal fundamental cycle. Both simulation and experimental results are presented to reveal the benefits of the technique.

Index Terms: Clarke transformation, delayed signal cancellation, phase angle estimation, and three-phase system.

I. Introduction

A fast and accurate estimation technique for instantaneous phase angle of three-phase voltage systems plays an important role for efficient operation of grid-connected power converters [1-3]. A phase-locked loop (PLL) is the commonly applied technique for phase estimation [4]. Three-phase PLL-based on synchronous-reference frame (SRF) is the simplest one and can provide accurate estimation at high speed under balanced and undistorted conditions. However, it requires in-loop filter or pre-filter as it suffers by harmonics and imbalances [5-9]. The inclusion of additional filter may require optimum tuning and may also introduce interdependent loops.

A moving average (MA) based in-loop filter may slow down dynamic response of the PLL significantly [5]. In this case, a proportional–integral–derivative (PID) controller is suggested as a loop filter to improve the dynamic performance while maintaining a good filtering capability [5, 6]. The MA filter can be replaced by one or more notch filters [7]. On the other hand, a variable sampling frequency based approach may not be suitable for real-time application due to the requirement of changing parameters of other algorithms implemented in the same digital signal processing board [6]. Multiple SRF filtering based PLL structure can reject adverse effects caused by harmonics and negative-sequence (NS) components, but it increases computational effort considerably [10]. Complex coefficient filters (CCFs) can also be used in the pre-filtering stage [8]. In this structure, the CCFs are cross-connected where each of them is responsible for tracking a particular frequency component. An enhanced PLL generates slower response under grid disturbances [9]. Additional second-order generalized integrator (SOGI) based quadrature signal generator (QSG) tuned at harmonic frequencies may be combined with the QSG-SOGI based PLL (SOGI-PLL) to improve the lower-order harmonic filtering capability [11, 12]. Moreover, mixed second-and third-order generalized integrator based PLL (MSTOGI-PLL) can be used to enhance the estimation accuracy under DC offset condition [13].

A delayed signal cancellation (DSC) approach can be used as an in-loop or pre-filter of the SRF-PLL for extracting the phase angle of the fundamental frequency positive-sequence (FFPS) component [14-18]. The in-loop filter based on a cascaded DSC (CDSC) operator increases delay in the control loop of the PLL and slows down the dynamic response [16]. On the other hand, the frequency estimated by the SRF-PLL is fed back to adjust the pre-filter based on CDSC operator to the frequency variations [15]. In this case, the system becomes highly nonlinear due to the presence of interdependent loops [17].

The technical literature shows that the presence of interdependent loops between the phase and frequency estimation reduces the stability margin of the PLL due to the influence of one loop by other one at the same time. In this case, the tuning of proportional plus integral (PI) controller (loop filter) is also more sensitive. In addition, a time delay is generated by the loop filter and hence a slower response is produced. A better stability and an easier tuning process can be achieved by using a separate frequency estimator for the adaptive pre-filter where the interdependent loops between the phase and frequency estimation are avoided. The time delay associated with the PI controller and/or in-loop filter can also be avoided if, instead of the PLL, a separate phase estimation algorithm is used.

The objective of this paper is to propose a relatively fast and robust technique for instantaneous phase angle estimation of three-phase voltage systems. It relies on a Teager energy operator (TEO) based frequency detection algorithm and a CDSC operator based phase estimation approach. Unlike the CDSC based SRF-PLLs, the proposed TEO-CDSC technique avoids interdependent loops between the frequency and phase estimation, thus increasing the overall stability and easing the tuning process. Moreover, it does not need the phase loop of the PLL, thus eliminates the requirement of in-loop low-pass filter (LPF) and/or loop filter (PI/PID controller). As a result,
the tuning of these filters is not required and a faster response is produced. It also avoids inverse trigonometric function operations. In addition, it shows harmonics immunity at steady-state and can generate fast dynamic response with a settling time less than one nominal fundamental cycle.

The remaining parts of the paper are organized as follows. Section II contains an overview of the SRF-PLLs based on the CDSC operator. The proposed TEO-CDSC technique is documented in section III. Simulated performance comparison of the proposed technique with the CDSC-PLL [15] and dqCDSC-PLL [16] are presented in section IV. Section V contains the real-time experimental results. Section VI includes the conclusions of the proposed work.

II. Overview of CDSC Based PLLs

The voltage signals of three-phase systems can be unbalanced due to the grid faults or sudden connection/disconnection of heavy loads to/from the grid. The unbalanced voltage signals can be expressed by

\[
\begin{align*}
\bar{v}_a(n) &= A_\alpha \sin(\phi(n)) \\
\bar{v}_b(n) &= A_\beta \sin(\phi(n) - 2\pi/3) \\
\bar{v}_c(n) &= A_c \sin(\phi(n) + 2\pi/3)
\end{align*}
\]  

Symbols used in (1) are defined as follows: \( n \): sampling index, \( A_\alpha, A_\beta \) and \( A_c \): fundamental amplitudes of phases \( \alpha \), \( \beta \) and \( c \) respectively, \( \phi(n) = \omega T n + \theta \): instantaneous phase angle of phase \( \alpha \), \( \theta \): initial phase angle of phase \( \alpha \), \( T \): sampling time interval, \( \omega = 2\pi f \): fundamental angular frequency, and \( f \): fundamental frequency. The unbalanced voltage signals can also be distorted by harmonics due to the non-sinusoidal current drawn by the nonlinear loads connected to the grid. The SRF-PLL is the commonly applied technique for the extraction of phase angle of the FFPS component. However, to obtain an accurate estimation, a pre-filter or in-loop filter is combined with the SRF-PLL under distorted and unbalanced conditions. The following subsections present an overview of the SRF-PLLs based on the pre-filter or in-loop filter relying on the CDSC operator.

A. Three-Phase SRF-PLL Based on CDSC Pre-Filter

Fig. 1 shows the block diagram representation of the three-phase SRF-PLL based on the CDSC pre-filter. In this method, the Clarke transformation generates \( v_a, v_b \) and \( v_c \) signals in \( \alpha-\beta \) stationary reference frame from the three-phase grid voltages \( v_a, v_b, \) and \( v_c \). The generated voltages contain FFPS \((\bar{v}_a, \bar{v}_b)\), fundamental frequency NS (FFNS), harmonic frequencies PS and NS components under unbalanced and harmonic conditions. A frequency adaptive band-pass filter (BPF) is then used as the pre-filter to extract only the FFPS component. The DSC operator has excellent filtering characteristics and is recently used as the pre-filter for improving the disturbance rejection ability of the SRF-PLL [15, 16, 19, 20]. Several configurations of the CDSC operator can be used under several conditions of the input voltages. The use of a number of DSC operators in the CDSC chain depends on the expected harmonic components [15, 16, 19, 20]. The SRF-PLL relying on the Park transformation, PI controller (loop filter) and integrator is then employed to track the instantaneous phase angle \( \phi^* \) of the FFPS component. The CDSC pre-filter based SRF-PLL has two shortcomings. The first one is that the frequency adaptive nature of the CDSC has introduced interdependent loops between the phase and frequency estimation. The frequency estimated by the SRF-PLL is fed back to adjust the CDSC operator to the frequency variations [15, 19, 20]. In this case, the system becomes highly nonlinear due to the presence of interdependent loops [17]. The interdependent loops reduce the stability margin of the PLL due to the influence of one loop by other one at the same time. In this case, the tuning of the PI controller (loop filter) is also more sensitive. The second one is that a time delay is generated by the loop filter and hence a slower response may be produced.

B. Three-Phase SRF-PLL Based on CDSC In-Loop Filter

The in-loop filter based SRF-PLL is employed to avoid the interdependent loops so that a better stability margin and improved tuning process are obtained. Fig. 2 shows a block diagram representation of the in-loop filter based SRF-PLL. In this method, a fixed tuned in-loop filter is placed just before the loop filter of the PLL. The in-loop filter behaves like a LPF for rejecting all the unwanted high frequency oscillations from the generated \( \omega \) component of the Park transformation. The CDSC structure is also reported as the in-loop filter of the SRF-PLL [16]. However, the CDSC based in-loop filter is tuned at a constant frequency and hence the disturbance rejection capability may degrade under variable frequency environment. Moreover, the in-loop CDSC operator increases delay in the control loop of the PLL and causes sluggish dynamic response [16]. In addition, the PLL structure includes loop filter (PI/PID controller) which creates more dynamic delay.

III. Proposed CDSC Based Phase Estimation Technique

Fig. 3 shows the block diagram representation of the proposed technique for tracking the instantaneous phase angle of the FFPS component. As it can be seen, the proposed technique avoids the interdependent loops between phase and frequency estimation and hence a better stability and relatively easier tuning process can be achieved. The proposed technique also removes the in-loop and loop filters, which help generating faster dynamic response when compared to the SRF-PLL structures shown in Figs. 1 and 2. In the proposed technique, the orthogonal voltage signals of the FFPS component are extracted by using the frequency adaptive CDSC based BPF which is similar to the pre-filter of the SRF-PLL shown in Fig. 1. However, the fundamental frequency for adjusting the window size of the CDSC is tracked by using an auxiliary algorithm. The voltage signals generated by the Clarke transformation are also used as the inputs of the auxiliary algorithm for frequency estimation.
When compared to the techniques shown in Figs. 1 and 2, the proposed one replaces PLL by an arctangent approximation function, hence it does not require in-loop and loop filter for calculating the phase angle of the FFPS component. The extracted orthogonal voltages, without passing through any other filters, are directly used to calculate the phase angle and hence faster phase estimation can be achieved. The detail functions of each block shown in the proposed technique (Fig. 3) are documented in the following subsections.

A. Clarke Transformation

The voltage signals \(v_a\) and \(v_b\) in \(\alpha\)–\(\beta\) stationary reference frame can be generated from the three-phase grid voltages by using the Clarke transformation shown bellow [21].

\[
\begin{align*}
\begin{bmatrix} v_a(n) \\ v_b(n) \\ v_0(n) \end{bmatrix} &= \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & -1/\sqrt{3} & 1/\sqrt{3} \end{bmatrix} \begin{bmatrix} v_a(n) + v_b(n) \\ v_a(n) - v_b(n) \\ 0 \end{bmatrix}
\end{align*}
\]

(2)

where

\[
\begin{align*}
\begin{bmatrix} v_a(n) \\ v_b(n) \\ v_0(n) \end{bmatrix} &= \begin{bmatrix} A' \sin(\omega T_n + \theta') \\ A' \cos(\omega T_n + \theta') \\ A' \sin(-\omega T_n - \theta') \\ A' \cos(-\omega T_n - \theta') \end{bmatrix}
\end{align*}
\]

where \((A', -A')\) and \((\theta', -\theta')\) are the amplitude and initial phase angle of the FFPS and FFNS components, respectively. All elements of the second row in the Clarke transformation matrix are multiplied by -1 to produce a positive cosine signal for \(v_c\). The voltage signals \(v_a\) and \(v_b\), as shown in (2), may contain PS and NS components at harmonic frequencies if the unbalanced three-phase voltages include harmonic distortions. Hence, a BPF is required to extract the FFPS components.

B. BPF Based on CDSC

The characteristics of the CDSC operator as a filter are well studied in the technical literature [15]-[18]. The orthogonal voltages of the FFPS component can be extracted by using the CDSC\(_{4,8,16,32}\) operator when the three-phase voltages are unbalanced and distorted by odd harmonics. The frequency response of the CDSC\(_{4,8,16,32}\) operator is shown in Fig. 4 [15]. As it can be seen, the CDSC\(_{4,8,16,32}\) operator can extract the FFPS component without any phase shift and amplitude attenuation. It can reject both the PS and NS components of all odd harmonics including the FFNS one. On the other hand, all the odd and even harmonics including the FFNS one and dc offset can also be eliminated by using the CDSC\(_{2,4,8,16,32}\) operator.

The block diagram implementation of the CDSC\(_{4,8,16,32}\) operator is shown in Fig. 5, where \(C_{\pi}\) is \(\cos(2\pi/8)\), \(S_{\pi}\) is \(\sin(2\pi/8)\) and \(N\) is the number of voltage samples in one fundamental time period. As it can be seen, the CDSC\(_{4,8,16,32}\) operator is formed by combining DSC\(_4\), DSC\(_8\), DSC\(_{16}\) and DSC\(_{32}\) in chain. The CDSC\(_{4,8,16,32}\) operator has two inputs and two outputs. The \(v_a\) and \(v_b\) voltages are used as the inputs and the orthogonal voltages (\(v_a'\) and \(v_b'\)) of the FFPS component are obtained from the outputs. The number of delays shown in the DSC operator can be integer or non-integer. For the non-integer value of the delays, a relatively simple linear interpolation operation can be executed to enhance the estimation accuracy. The dynamic time delay caused by the frequency adaptive CDSC\(_{4,8,16,32}\) operator is 47% (=1/4+1/8+1/16+1/32) of the fundamental period. It can be seen from Fig. 5 that the DSC\(_4\) operator is relatively simple to implement and hence the CDSC\(_{4,8,16,32}\) operator can be easily executed for the real-time application. The DSC\(_2\) can also combined with the CDSC\(_{4,8,16,32}\) to form the operator CDSC\(_{2,4,8,16,32}\). In this case, an additional half fundamental time period is required by the operator CDSC\(_{2,4,8,16,32}\) when compared to the CDSC\(_{4,8,16,32}\) one under dynamic condition. In our proposed technique, the value of \(N\) (\(=n/f_s\), where \(f_s\) is a fixed sampling frequency) is updated by using the estimated fundamental frequency, as can be noticed in Fig. 3. The outputs of the frequency adaptive CDSC operator can be expressed by

\[
\begin{align*}
\begin{bmatrix} v_a'(n) \\ v_b'(n) \end{bmatrix} &= \begin{bmatrix} A' \sin(\omega T_n + \theta') \\ A' \cos(\omega T_n + \theta') \end{bmatrix}
\end{align*}
\]

(3)

C. Arctangent Approximation

An arctangent function can be employed to calculate the phase angle of the FFPS component, as expressed by

\[
\phi(n) = \arctan\left(\frac{v_a'(n)}{v_b'(n)}\right)
\]

(4)

However, the arctangent operation is computationally demanding for real-time application [22]. Moreover, the division of \(v_a'/v_b'\) is ill-conditioned when the value of the voltage sample \(v_b'\) is zero. To avoid the inverse tangent operation and ill-condition, the following approximation function can be used to estimate the FFPS instantaneous phase angle from the extracted orthogonal voltages [22].

\[
\phi^*(n) = \begin{cases} 
\pi + \phi(n) & \text{for } v_a'(n) < 0 \text{ and } v_b'(n) < 0 \\
2\pi - \phi(n) & \text{for } v_a'(n) > 0 \text{ and } v_b'(n) > 0 \\
\phi(n) & \text{for } v_a'(n) > 0 \text{ and } v_b'(n) < 0 \\
\phi(n) & \text{for } v_a'(n) < 0 \text{ and } v_b'(n) > 0
\end{cases}
\]

(5)
where $\varphi^\circ(n) = \frac{\pi}{2} - \arctan \left( \frac{0.6404|\sin(\omega T_n)|^2 + |\sin(\omega T_n)|^2 + |\cos(\omega T_n)|^2 + |\cos(\omega T_n)|^2}{|\sin(\omega T_n)|^2 + 1.6404|\sin(\omega T_n)|^2 + 1.6404|\cos(\omega T_n)|^2 + |\cos(\omega T_n)|^2} \right)$

and $| \cdot |$ symbol indicates absolute value. In this case, the peak value of approximation error is 0.00811° which is very small [22]. The absolute values of $v_a$ and $v_b$ are used in (5) for calculating $\varphi^\circ$. The value of $v_a$ is maximum when $v_b$ is zero and vice versa. Therefore, the denominator of (5) is always positive and non-zero. As a result, the ill-condition for calculating the instantaneous phase angle from the orthogonal voltage signals $v_a$ and $v_b$ is avoided.

### D. Fundamental Frequency Estimation

An auxiliary algorithm is used in the proposed method for tracking the fundamental frequency. It combines the second harmonic generation process and TEO.

#### D-1. Second Harmonic Generation

The Clarke transformed voltage signal $v_{\alpha\beta}$ as shown in (2), under unbalanced condition can be written as

$$v_{\alpha\beta}(n) = A_{\alpha\beta} \{\sin(\omega n T_a) \cos(\theta_a) + \cos(\omega n T_a) \sin(\theta_a)\} - A_{\alpha\beta} \{\sin(\omega n T_b) \cos(\theta_b) + \cos(\omega n T_b) \sin(\theta_b)\} = \sin(\omega n T_a) \{A_{\alpha} \cos(\theta_a) - A_{\beta} \cos(\theta_b)\} + \cos(\omega n T_b) \{A_{\alpha} \sin(\theta_a) - A_{\beta} \sin(\theta_b)\} = \sin(\omega n T_a) A_{\alpha} \cos(\theta_a) + \cos(\omega n T_b) A_{\beta} \sin(\theta_b)$$

where

$$A_{\alpha} = A_{\alpha\beta} \cos(\theta_a) - A_{\beta} \cos(\theta_b)$$

$$A_{\beta} = A_{\alpha\beta} \sin(\theta_a) - A_{\alpha} \sin(\theta_b)$$

$$\theta_a = \tan^{-1} \left( \frac{A_{\alpha} \sin(\theta_a)}{A_{\alpha} \cos(\theta_a) - A_{\beta} \cos(\theta_a)} \right)$$

Similarly, the Clarke transformed voltage signal $v_{\beta\alpha}$ as shown in (2), under unbalanced condition can be expressed as

$$v_{\beta\alpha}(n) = A_{\beta\alpha} \sin(\omega n T_b) + \theta_b$$

where

$$A_{\beta\alpha} = \sqrt{A_{\alpha}^2 + A_{\beta}^2 + 2A_{\alpha} A_{\beta} \cos(\theta_a - \theta_b)}$$

$$\theta_b = \tan^{-1} \left( \frac{A_{\alpha} \sin(\theta_b)}{A_{\alpha} \cos(\theta_b) + A_{\beta} \cos(\theta_b)} \right)$$

In the proposed technique, the voltage signals $v_{\alpha\beta}$ and $v_{\beta\alpha}$, as expressed in (6) and (7), are multiplied to generate the second harmonic. Their multiplication can be expressed by

$$v_{\alpha\beta}(n) = v_{\alpha\beta}(n) v_{\beta\alpha}(n) = A_{\alpha\beta} A_{\beta\alpha} \sin(2\omega n T_a + \theta_a) \cos(2\omega n T_b + \theta_b) = 0.5A_{\alpha\beta} A_{\beta\alpha} [\cos(2\omega n T_a + \theta_a + \theta_b) + \cos(2\omega n T_a + \theta_a - \theta_b) + \sin(2\omega n T_a - \theta_b) + \sin(2\omega n T_a + \theta_b)]$$

$$A_{\alpha\beta} A_{\beta\alpha} \theta_a \theta_b = [\cos(\theta_a + \theta_b) + \cos(\theta_a - \theta_b)]$$

Expression (8) contains second harmonic and a dc value when the undistorted three-phase voltages are unbalanced. However, the generated dc value can be zero under balanced condition due to $\theta_a, \theta_b = 0$ for $A = 0$ and $\theta_a = \theta_b = \pi$. On the other hand, high-order even harmonics including the second one can be present in (8) when the fundamental component of the unbalanced three-phase voltages is distorted by odd harmonics. Moreover, odd harmonics can be generated in (8) when even harmonics are present in the three-phase voltages. So, $v_{\alpha\beta}$ always includes the second harmonic whether the balanced/unbalanced three-phase voltages contain harmonics or not. The generated second harmonic component can be extracted for the fundamental frequency detection.

#### D-2. BPF for Second Harmonic Extraction

The recursive DFT (RDFT) of the voltage signal $v_{\alpha\beta}$ can be expressed as follows [23]:

$$v_{\alpha\beta}(n) = v_{\alpha\beta}(n-1) + \{v_{\alpha\beta}(n) - v_{\alpha\beta}(n-P)\}e^{-2\pi i \frac{2kn}{P}}$$

where $P$ indicates the window size, $k$ is the frequency index and $j$ is the complex operator. The value of $P$ is the number of voltage samples in the window. The real and imaginary parts of the RDFT can also be tracked by (10) and (11), respectively [23]:

$$\text{Re}[V_{\alpha\beta}(n)] = \text{Re}[V_{\alpha\beta}(n-1)] + \{v_{\alpha\beta}(n) - v_{\alpha\beta}(n-P)\} \cos(\frac{2\pi kn}{P})$$

$$\text{Im}[V_{\alpha\beta}(n)] = \text{Im}[V_{\alpha\beta}(n-1)] + \{v_{\alpha\beta}(n) - v_{\alpha\beta}(n-P)\} \sin(\frac{2\pi kn}{P})$$

For a window size of one fundamental cycle ($P=\pi$) and $k=2$, this approach can extract the second harmonic component by rejecting all the odd and other even harmonics including the fundamental one at a cost of one fundamental cycle dynamic delay. This configuration is useful when the three-phase grid voltages contain DC offset, odd and even harmonics. On the other hand, expression (12) can extract the generated second harmonic component by eliminating all other high-order even harmonics for a window size of half fundamental cycle and $k=1$ at a cost of half fundamental cycle dynamic delay. This configuration is useful when the three-phase grid voltages contain only odd harmonics. So, the above approach with a half fundamental cycle window can be used in the proposed technique for tracking the generated second harmonic when the grid voltages contain odd harmonics. The output of the BPF based on (12) can be expressed by

$$v_{\alpha\beta}(n) = A_{\alpha\beta} \sin(2\omega n T_a + \theta_a)$$

An additional advantage of using this approach is that it can provide the amplitude estimation of the extracted second harmonic component as it relies on the RDFT operation. The amplitude of the extracted second harmonic component can be obtained as follows [23]:

$$A_{\alpha\beta}(n) = \sqrt{\text{Re}[V_{\alpha\beta}(n)]^2 + \text{Im}[V_{\alpha\beta}(n)]^2} / P$$

where $k=1$ or 2 depending on the size of the window $P=\pi/2$ or $P=\pi$, respectively.

### D-3. TEO for Frequency Estimation

The expression of the TEO for $v_2$ can be expressed as follows [25-28]:

- **2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.**
- **Authorized licensed use limited to: Danmarks Tekniske Informationscenter. Downloaded on January 05, 2021 at 13:38:30 UTC from IEEE Xplore. Restrictions apply.**
As it can be
seen, the TEO can be employed to track the fundamental frequency from three consecutive voltage samples when the amplitude of $v_2$ is known. However, expression (15) requires computationally demanding square root and inverse sine operations. These computationally demanding operations can be avoided by using a polynomial function as follows.

$$f = \sigma_1 \gamma^2 - \sigma_2 \gamma + \sigma_3$$

(16)

where $\sigma_1 = 50454854.888$, $\sigma_2 = 1014758.195$, $\sigma_3 = 12000.361$ and $\sigma_4 = 15.37262$. The values of the above coefficients are obtained using a curve-fitting command ‘polyval’ in MATLAB by considering 10 kHz sampling frequency and ±10 Hz variation of the fundamental frequency. The frequency difference between the actual relation and approximated function (16) at different fundamental frequencies is shown in Fig. 6. As it can be noticed, the maximum frequency error created by the approximated function is around 0.01 Hz.

The TEO is sensitive to the presence of unwanted frequency components, as it depends on only three consecutive voltage samples. So, it requires robust pre-filtering for extracting the second harmonic and its amplitude. The RDFT method used for the BPF may experience an accumulation error [23]. However, the amplitude accumulation error is eliminated by normalising the second harmonic component using the estimated amplitude. On the other hand, the accumulated phase error is assumed to be constant within the three consecutive voltage samples of the second harmonic component. The TEO algorithm, as shown in (15), is not affected by the constant accumulated phase error for calculating the fundamental frequency.

E. Tuning

The proposed technique shows that the Clarke transformation, CDSC operator and arc tangent approximation operation do not contain any feedback path, thus they are unconditionally stable. On the other hand, the frequency estimation approach is also an open-loop structure and stable if the RDFT based BPF is fixed tuned at the nominal frequency of the second harmonic. In this case, the performance of the TEO may degrade when the fundamental frequency deviates from the nominal value because the fixed tuned BPF may not be able to reject unwanted frequency components. However, to obtain improved results, the window size of the BPF may be adaptively adjusted by the estimated fundamental frequency. The adaptive window approach introduces a feedback path in the frequency estimation algorithm. In this case, to obtain stable frequency estimation, the response time of the TEO should be equal or slower than the window size of the BPF [15, 24, 26]. However, the response time of the TEO (relies on only 3 consecutive samples) is actually faster than the window size of the BPF due to $PT > 3T$. For this reason, a first-order infinite-impulse-response LPF can be cascaded with the TEO to provide the required additional time delay to make the frequency estimation stable [15, 24, 26]. In this case, the bandwidth of the LPF should be equal or smaller than the one used for the BPF. The overall dynamics of the proposed method due to the use of the frequency adaptation and LPF will be slower when the TEO introduces a time delay. The dynamic delay will depend on the time constant of the LPF.

IV. Simulation Results

Simulated performance of the proposed TEO-CDSC technique is investigated and compared with the pre-filter based CDSC-PLL [15] and in-loop filter based dqCDSC-PLL [16] methods. All methods are implemented in MATLAB/Simulink for a sampling frequency of 10 kHz. For a fair comparison, the same number of DSC operators (DSCb, DSCs, DSCf & DSCg) are used in all three techniques. The respective references are followed to tune other parameters of the CDSC-PLL and dqCDSC-PLL methods. Throughout the simulation studies for comparison, the fundamental component of the three-phase grid voltages is contaminated by harmonics. The percentage of the contaminated harmonics with a total harmonic distortion (THD) of 10.464% is shown in Table I and their amplitudes are chosen according to the European standard EN 50160 [29]. The following case studies are carried out for performance analysis.

Case-1. Steady-State with Harmonics

The steady-state phase error generated by the proposed TEO-CDSC, CDSC-PLL and dqCDSC-PLL methods under harmonics is presented in Fig. 7. In this case, the fundamental frequency is varied from 45 Hz to 55 Hz. It can be seen from Fig. 7 that the phase error produced by the dqCDSC-PLL method is increasing when the fundamental frequency deviates from the nominal value. The maximum phase errors created by the proposed, CDSC-PLL and dqCDSC-PLL methods are around 0.03°, 0.015° and 0.6°, respectively, for the fundamental frequency variation range of ±5 Hz from the nominal value.

Case-2. Unbalanced Amplitude Step with Harmonics

The distorted three-phase voltage waveforms with unbalanced amplitude steps are shown in Fig. 8(a). The fundamental voltage amplitude steps are +0.2 pu, -0.2 pu and -0.4 pu, from their nominal value for the phases ‘a’, ‘b’ and ‘c’, respectively. The harmonic contents are changed accordingly to keep the THD constant. The responses of the proposed, CDSC-PLL, and dqCDSC-PLL techniques are depicted in Figs. 8(b) and (c). As it can be seen, the proposed technique spends around 10 ms and 15 ms as response time for estimating the actual frequency and phase angle, respectively, under dynamic condition. When compared to
The harmonic contents are shown in Table I and the estimation by 33.83% and 49.14% technique improves the settling time for the phase step. CDSC, CDSC-PLL and techniques are 17.8 ms, 26.9 ms and 35 ms, respectively for a proposed TEO-CDSC, CDSC-PLL, and techniques under harmonics and -20° phase step at time 0.5 s. (a) Three-phase voltage waveforms. (b) Estimated fundamental frequency error. (c) Estimated FFFS phase error.

The settling time comparison among the proposed TEOCDSC, CDSC-PLL, and $dq$CDSC-PLL techniques under different phase steps including harmonics is shown in Fig. 10. The settling time is estimated based on ±2% error criteria. Fig. 10 shows that the maximum settling time required by the proposed TEO-CDSC, CDSC-PLL, and $dq$CDSC-PLL techniques take 17.3 ms, 24.3 ms and 34.3 ms, respectively, as settling time for tracking the -20° phase step, as can be noticed in Fig. 9(b).

The settling time comparison among the proposed TEOCDSC, CDSC-PLL, and $dq$CDSC-PLL techniques under a phase step including harmonics. The phase step created at time 0.5 s is -20°. In this case, when compared to the CDSC-PLL and $dq$CDSC-PLL techniques, the proposed one shows quicker response for tracking both the fundamental frequency and phase angle. The proposed TEO-CDSC, CDSC-PLL, and $dq$CDSC-PLL techniques take 17.3 ms, 24.3 ms and 34.3 ms, respectively, as settling time for tracking the -20° phase step, as can be noticed in Fig. 9(b).

The settling time comparison among the proposed TEOCDSC, CDSC-PLL, and $dq$CDSC-PLL techniques under a harmonic sweep and fundamental frequency. On the other hand, it can be noticed from the phase estimation shown in Fig. 11(b) that the proposed technique takes less than 15 ms to converge to the actual value of the phase angle and also shows a faster response when compared to other two techniques.

The performance comparison among the proposed TEOCDSC, CDSC-PLL and $dq$CDSC-PLL techniques under a frequency step and harmonics condition is shown in Fig. 11. The harmonic contents are shown in Table I and the fundamental frequency step created at time 0.5 s is -2 Hz. The settling time taken by the proposed and CDSC-PLL methods are 11 ms and 20.8 ms, respectively, for estimating the frequency step, as can be seen in Fig. 11(a). However, the fixed tuned CDSC based $dq$CDSC-PLL technique produces higher ripples in the estimated off-nominal fundamental frequency. On the other hand, it can be noticed from the phase estimation shown in Fig. 11(b) that the proposed technique takes less than 15 ms to converge to the actual value of the phase angle and also shows a faster response when compared to other two techniques.

Fig. 12 demonstrates the dynamic responses of the proposed TEO-CDSC, CDSC-PLL, and $dq$CDSC-PLL techniques under fundamental frequency sweep of -10 Hz/s sweep of the fundamental frequency. (a) Estimated fundamental frequency error. (b) Estimated FFFS phase error.
techniques under harmonics and frequency sweep condition. In this case, the fundamental frequency sweep is -10 Hz/s and it starts from 50 Hz and stops at 49.5 Hz. The frequency sweep of the harmonics is also changed accordingly. The time range of the frequency sweep is 0.5 s to 0.55 s. It can be noticed from Fig. 12 that the proposed TEO-CDSC technique generates smaller transient error in both the estimated fundamental frequency and instantaneous phase angle under the frequency sweep condition as compared to other two PLL based techniques.

**Case-6. Steps in Frequency, Phase and Amplitude with Harmonics**

The performances of the proposed, CDSC-PLL, and $dq$CDSC-PLL techniques for a combination of frequency step, phase step and unbalanced amplitude step including harmonics are demonstrated in Fig. 13. In this case, the fundamental frequency and phase steps are -2 Hz and -20°, respectively. The fundamental voltage amplitude steps are +0.2 pu, -0.2 pu and -0.4 pu, from their nominal value for the phases 'a', 'b' and 'c', respectively. The harmonic contents are changed accordingly to keep the THD constant. Similar to the individual case studies presented above, the proposed technique generates quicker transient response to follow the frequency and phase angle steps under this adverse condition. The proposed technique also requires less than one nominal fundamental cycle (20 ms) as the response time.

**Case-7. Steady-State with DC Offset and Harmonics**

Fig. 14 demonstrates the steady-state performance of the proposed, CDSC-PLL, and $dq$CDSC-PLL techniques under DC offset and harmonics condition. In this case study, the CDSC-PLL technique is used in all the three compared techniques. For performance analysis, different DC offsets are injected in different phase voltages. The voltage waveforms of phases 'a', 'b' and 'c' in Fig. 14(a) contain -0.05 pu, 0.10 pu and 0.15 pu DC offsets, respectively. It can be noticed from Figs. 14(b) and (c) that the proposed and CDSC-PLL methods are able to reject the negative effects caused by the DC offset and also generate improved phase and frequency estimation when compared to the $dq$CDSC-PLL one.

### V. Experimental Results

The real-time performance comparison between the proposed and MSTOPGI-PLL [13] techniques is carried out by several experimental case studies in a laboratory setup. The dSPACE DS1104 control board platform is used to conduct the experiments. The proposed and MSTOPGI-PLL methods in MATLAB/Simulink environment are uploaded to the DS1104 control board using automatic code generation process. The real-time three-phase voltages with various grid events are produced by the DS1104 with the help of the digital-to-analog converters. The generated real-time three-phase voltages are sent to the inputs of the techniques through the analog-to-digital converters of the DS1104. Throughout the experimental studies, the fundamental component of the three-phase grid voltages is polluted by harmonics, as presented in Table I. The real-time experimental results are taken from the display of a digital oscilloscope.

The fundamental voltage amplitudes steps of +0.2 pu, -0.2 pu and -0.4 pu for the phases 'a', 'b' and 'c', respectively, are used to observe the real-time performances of the proposed and MSTOPGI-PLL techniques. The voltage waveforms and responses of the proposed and MSTOPGI-PLL techniques are shown in Fig. 15. As it can be observed, the proposed and MSTOPGI-PLL methods generate maximum around 2.3 Hz and 1.3 Hz swing, respectively, in the estimated fundamental frequency under the considered amplitude step condition. However, the proposed technique can track the frequency and phase angle with a dynamic time of less than one nominal fundamental cycle. On the other hand, the MSTOPGI-PLL method requires around two nominal fundamental cycles as the dynamic time. Moreover, the MSTOPGI-PLL method produces more ripples at steady-state in the estimated fundamental frequency.

A phase step of -20° including harmonics is used for evaluating the real-time performance comparison between the
Fig. 16. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under -20° phase step and harmonics.

Fig. 17. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under -2 Hz fundamental frequency step and harmonics.

Fig. 18. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under a combination of harmonics, fundamental frequency step (-2 Hz), phase step (-20°), and unbalanced amplitude step (1 to 1.2 pu, 1 to 0.8 pu and 1 to 0.6 pu for the phases ‘a’, ‘b’ and ‘c’, respectively).

proposed and MSTOGI-PLL techniques. The voltage waveforms and responses of both techniques are depicted in Fig. 16. As it can be seen, the proposed technique shows larger swing in the estimated frequency but needs less dynamic time when compared to the MSTOGI-PLL. In this case, the proposed method requires less than one nominal fundamental cycle whereas the MSTOGI-PLL one spends around three nominal fundamental cycles as the dynamic time.

The performances of the proposed and MSTOGI techniques for the fundamental frequency step of -2 Hz including harmonics is shown in Fig. 17. In this case, around 12 ms and 60 ms are taken by the proposed and MSTOGI-PLL techniques, respectively, as the response time for following the fundamental frequency step.

The performance comparison for a combination of step phase, step phase, and amplitude step is shown in Fig. 18. In this case, the steps of the fundamental frequency, phase angle and amplitudes are -2 Hz, -20°, and +0.2 pu, -0.2 pu and -0.4 pu, respectively, from the nominal value. It can be seen from Fig. 18 that the proposed and MSTOGI-PLL methods produce around 4.8 Hz and 4.0 Hz swing, respectively, in the estimated fundamental frequency. However, the proposed technique shows quicker response and generates accurate frequency and phase angle with a response time less than 20 ms whereas 60 ms is required by the MSTOGI-PLL method.

VI. Conclusions

A fast and robust technique based on the Teager energy and delayed signal cancellation operators has been reported in this paper for instantaneous phase angle estimation of three-phase voltage systems. When compared to the delayed signal cancellation based phase-locked loops, the proposed technique removes interdependent loops between the frequency and phase estimation, thus increasing the overall stability and easing the tuning process. Moreover, it avoids the phase loop of the phase-locked loop, thus eliminates the requirement of in-loop and loop filters. As a result, the tuning of these filters is not required and a faster response is produced. It also avoids the online operation of the inverse trigonometric functions. In addition, it shows harmonics immunity at steady-state and generates fast dynamic response with a settling time less than one nominal fundamental cycle. The presented simulated and experimental results have confirmed the practical application of the technique.

References


