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A 1-MHz Resonant LED Driver with Charge-Pump-Based Power Factor Correction

Ahmed M. Ammar, *Member, IEEE*, Frederik M. Spliid, Yasser Nour, *Senior Member, IEEE*, and Arnold Knott

Abstract— This paper presents the design and implementation of a resonant LED driver. The driver structure comprises a charge-pump-based power factor correction (PFC) converter and a class-DE dc-dc converter. The PFC converter employs a charge-pump circuit that achieves PFC inherently. The class-DE converter comprises a series-resonant tank and a high-frequency transformer. Both converters share the same half-bridge and gate-driving circuit, resulting in an integrated-stage architecture. The inherent PFC operation limits the controller responsibility to the regulation of the output current. The overall converter operates with zero-voltage switching (ZVS) across the entire load range, allowing for increased switching frequencies with reduced switching losses. A 1-MHz prototype employing wide bandgap (WBG) switching devices is built and tested. The prototype delivers up to 42 W of output power, with a power density of 1.8 W/cm³. A power factor of 0.99 and a total harmonic distortion (THD) of 6 % are achieved, with an efficiency of 90 % at full load. The input current harmonic magnitudes are well-within the IEC 61000-3-2 standard limits for class-C devices. Burst-mode (on/off) modulation is used for output current regulation between 20 and 900 mA for dimming functionality.

Index Terms— LED drivers, power factor correction, resonant power conversion, charge pump, zero-voltage switching.

I. INTRODUCTION

The majority of current light systems are using high-brightness light-emitting diodes (LEDs) as the light source. That is owing to many reasons that include their longer lifetime, higher energy savings, smaller form factors, as well as higher quality and durability compared to other technologies [1]. The complete system comprises the electrical part (light engine), the mechanical part (luminaire), and the optical part (reflector and lens). The bottleneck for the size, weight, and cost reduction, as well as higher reliability and efficiency, is the light engine. It consists of an LED module (the LED array and the substrate material it is mounted on) and a driver (electrical engine). While the LED module is responsible for the limit in energy efficacy

Fig. 1. Conventional LED driver structure.

(lm/W), the driver is the limiting factor for size, weight, cost and reliability [2][3].

Fig. 1 shows the conventional solution for LED driver systems, which is comprised of a two-stage converter structure. The ac mains are first interfaced with a power factor correction (PFC) converter that rectifies the mains voltage and regulates the input current to satisfy the regulations on input current displacement and harmonics set by international standards [4][5]. A following dc-dc stage converts the intermediate dc-bus voltage to the voltage and current levels that apply to the LED load electrical characteristics. An energy-storage capacitor is inserted to filter the double-the-line 100/120 Hz frequency component on the output side.

Hard-switched pulse-width-modulated (PWM) converters have been the primary candidate for both LED driver stages. They can provide high power factor and efficiency with simple control methods. Prior art report solutions based on different topologies, including buck [6]–[8], boost-flyback [9], buck-boost-flyback [10][11], SEPIC-flyback [12], and flyback [13]–[16] topologies. However, in addition to the high conducted electromagnetic interference (EMI) from the rectangular waveforms, they are typically designed to operate at low frequencies in the range of few hundred kHz. That helps limit the switching losses, yet results in larger sizes for the passive converter components. On the other hand, high-frequency designs (1 MHz and above) have less efficiency and may incorporate a heatsink for thermal management, which counteracts the gain in power density.

Accordingly, soft-switching resonant converters have received increased attention in the recent years. They incur substantially lower switching losses compared to their PWM counterparts. That makes them a primary candidate for achieving high efficiencies at high frequencies, resulting in reduced sizes for the passive components and, therefore, higher power densities. In addition, high-frequency operation offers

Fig. 2. Proposed LED driver structure.

higher loop-gain bandwidths and faster transient responses. This has led to the investigation of their adoption into the converter stages in different applications [17], including the ac-dc [18]-[21] and the dc-dc [22]-[24] stages. One of such applications is the LED driver, where there is a high demand for small-size and compact solution for several applications, such as in-track LED drivers [25]. Prior art introduced different resonant LED driver structures, including resonant-SEPIC [26], class-E [21], class-E-LLC [27], class-DE [18]-[20], and LLC [28] topologies. In addition, combined PWM-resonant solutions were reported, such as the flyback-class-E [29], boost-LLC [30]-[32], and buck-boost-resonant [33][34] converters. Nevertheless, the reported solutions operate with relatively low switching frequencies and have limited power densities. Accordingly, the potential of high-frequency resonant converters for high-power-density LED driver applications can be further investigated.

This paper presents a 1-MHz resonant-converter-based LED driver. The structure, shown in Fig. 2, comprises a charge-pump-based PFC stage and a class-DE dc-dc stage in an integrated architecture, where the semiconductor switches and their driving circuit are shared between both stages. The PFC stage employs an improved charge-pump circuit that achieves PFC inherently, which eliminates the need for a current control-loop and limits the controller's task to regulation of the output current. That is key for resonant converters with challenging control, and provides freedom from the limited bandwidths of commercially available PFC controllers. The class-DE dc-dc stage provides the voltage and current scaling for the LED load.

This paper is organized as follows. Section II outlines the principle of operation of the proposed converter. The circuit analysis and design flow is illustrated in Section III. Section IV describes the design, implementation, and experimental results of a 1-MHz prototype. Finally, Section V concludes the achieved results.

II. PRINCIPLE OF OPERATION

A. Charge-Pump PFC Circuit

The use of the charge-pump-based techniques for PFC applications was reported in the 90's for the use in electronic ballast circuits [35]-[38]. Fig. 3 shows an equivalent circuit for the charge-pump PFC converter, where a single diode D_B represents the input bridge that rectifies the ac mains, and the dc-dc converter stage is modelled with a resistor R_{DC} . The variable voltage source V_{HF} is equivalent to a high-frequency

Fig. 3. Basic charge-pump circuit.

Fig. 4. Charge-pump circuit operation across half a line cycle.

voltage node in the converter circuit. The proper circuit operation is dependent on the design of the energy-storage capacitor C_{DC} and the pump capacitor C_P . A proper design ensures that the voltage V_{DC} is higher than the input voltage V_{IN} across the entire line cycle, and accordingly the diode bridge D_B and the pump diode D_P do not cross-conduct. Consequently, the input current is equal to the positive charging current of the pump capacitor.

Fig. 4 shows representative waveforms for circuit operation across one half of a line cycle. The pump capacitor is charged and discharged within the rise and fall times of V_{HF} , respectively. The capacitor charge ΔQ_P is proportional to the voltage difference across the capacitor V_P , which varies between a low-frequency high value V_{P_high} and a constant low value V_{P_low} . The circuit design ensures that the charge variation of C_P , which is proportional to the voltage variation across it ($V_{P_high} - V_{P_low}$), follows the input voltage V_{IN} across the line cycle (50/60 Hz). Accordingly, the average input current follows the input voltage and a unity power factor can be obtained. From circuit analysis, the voltage variation across C_P in one switching cycle is evaluated as follows [18]

$$\begin{aligned} \Delta V_P &= V_{P_high} - V_{P_low} \\ &= V_{IN} - V_{DC} + (V_{HF_high} - V_{HF_low}) \end{aligned} \quad (1)$$

From (1), in a converter circuit where the voltage V_{HF} has a peak-to-peak amplitude equal to V_{DC} , the voltage variation across the C_P becomes equal to the input voltage, and the variation of the pump capacitor charge is calculated as

$$\Delta Q_P = C_P \cdot \Delta V_P = C_P \cdot V_{IN} \quad (2)$$

The pump capacitor charging current, which is equal to the input current, averaged across one switching cycle, then equals

Fig. 5. Charge-pump-based converter reported in [19].

$$I_{IN} = \frac{\Delta Q_P}{T_s} = f_s \cdot C_P \cdot V_{IN} \quad (3)$$

Where T_s is the switching period and f_s is the converter switching frequency. Therefore, in steady state operation with a constant switching frequency, the input current becomes proportional to the input voltage, and a unity power factor can be obtained.

B. Charge-Pump-Based Class-DE Series-Resonant Converter

In [19], the charge-pump circuit is added to a class-DE series-resonant converter, where the pump capacitor is coupled to the high-frequency node interfacing the inverter and the rectifier, V_{REC} , as shown in Fig. 5. That results in the sharing of the converter switches and resonant tank between the pump circuit and the dc-dc stage, which reduces the component count and cost. However, that comes with two drawbacks. First, the power factor of the converter becomes dependent on the resonant tank gain, as coupling to the V_{REC} node results in the following expression for the input current after re-evaluating (1)

$$I_{IN} = \frac{\Delta Q_P}{T_s} = f_s \cdot \Delta Q_P = f_s \cdot C_P \cdot (V_{IN} - V_{DC} + V_{OUT}) \quad (4)$$

From (4), it is seen that operation close to resonance with a high resonant tank gain (close to unity) is a condition for eliminating the $V_{OUT} - V_{DC}$ term and achieving a high power factor. Accordingly, with the use of frequency modulation for load regulation, low power factor is obtained at low-load operation owing to the reduced resonant-tank gain. Second, a high current stress is imposed on the resonant tank components, as the charge-pump circuit operation entitles the resonant tank to store the energy from the input line as well as the energy to load every switching cycle. That complicates the resonant inductor design and results in limited efficiency.

C. Modified Charge-Pump PFC Circuit

By moving the charge-pump coupling from the V_{REC} node to the switching node V_{SW} , the resonant tank only processes the power to the load and the current stress is reduced. However, the circuit becomes impractical for high-frequency operation, as the charge pump circuit capacitively loads the half-bridge, resulting in loss of ZVS. In addition, the pump capacitor charges and discharges with a low time constant, owing to the relatively low switch on-resistance $R_{ds(on)}$. That results in high current spikes that can reach tens of amperes through the bridge

Fig. 6. Modified charge-pump circuit.

Fig. 7. Circuit operation across two switching cycles. Patterned areas illustrate the charge flow in the charge-pump capacitor (checked) and clamping diodes (solid).

and pump diodes and switches. Therefore, to allow for operation at high frequencies, an inductor needs to be placed in the input current path to smooth the pump capacitor high-frequency current.

Fig. 6 shows the modified charge-pump circuit, where an inductor L_P is added in series with the charge pump capacitor C_P to smooth the capacitor current. That, however, results in reduction of the power factor, as the voltage change across the capacitor is no longer equal to the input voltage with the voltage drop across the inductor. To bind the voltage across the capacitor to the input voltage, two clamping diodes D_{C1} and D_{C2} are added to clamp V_C to a maximum voltage of V_{DC} and minimum voltage of zero [35].

The circuit operation spans six intervals every switching cycle. Fig. 7 shows waveforms for several circuit currents and voltages across two switching cycles, where the circuit and devices parasitics are ignored for simplicity. Fig. 8 shows the equivalent circuits and current paths across the different intervals of operation.

Fig. 8. Equivalent circuits with charge-pump circuit current paths (red) and load current paths (blue) across different intervals of operation. (a) Interval 1, (b) interval 2, (c) interval 3, (d) interval 4, (e) interval 5, and (f) interval 6 equivalent circuits.

Interval 1 starts once the half-bridge toggles, with the high-side switching off and low-side on. The energy stored in the pump capacitor is discharged in C_{DC} . I_{LP} decreases linearly, with the voltage across the pump capacitor decreasing until it reaches zero, while V_C keep increasing until it reaches V_{DC} . At that point, interval 2 starts, where D_{C1} turns on and V_C is clamped to V_{DC} , while I_{LP} continues decreasing until it reaches zero. Meanwhile, no current flows in C_P . Interval 3 starts once the energy in the charge-pump tank gets depleted. D_{C1} stops conducting and D_B turns on to charge C_P by the line input current. This interval terminates when the half-bridge toggles again and interval 4 begins. In that interval, the high-side switch is on and the low-side is off. D_B continues to conduct until C_P is charged to V_{IN} , while V_C decreases to zero.

At that point, interval 5 starts and D_{C2} turns on, clamping V_C to zero. I_{LP} linearly increases as a positive voltage of V_{DC} is applied across it and the interval ends once it reaches zero. Interval 6 then starts, where part of the energy stored in C_P is released into L_P while the charge-pump tank current freewheels through D_P and Q_{HS} . By the end of that interval, Q_{HS} turns off, and the next switching cycle begins.

The operation shows that the ac line input current is discontinuous and equal to the pump capacitor charging current, which is equal to I_{LP} in intervals 3 and 4. In addition, the voltage across the pump capacitor is changing between V_{IN} and zero every switching cycle, as seen in Fig. 7, and accordingly (2) and (3) hold for this circuit and unity power factor is achievable.

D. Proposed Converter

Fig. 9 shows the proposed converter schematic, where the R_{DC} load in Fig. 6 is replaced with a class-DE series-resonant converter for the dc-dc stage. The half-bridge switch network and its driving circuit are shared between the two converters, resulting in an integrated-stage architecture, where the current paths to the PFC and class-DE stages are split from the switching node. Compared to the two-stage conventional architecture, the proposed converter offers lower components

count, and thus higher power density and lower cost. Compared to the prior art in [19], by sharing only the switches between the two paths and splitting the single resonant tank into two, the current stress in each tank is reduced and the design of magnetic devices becomes simpler. Additionally, higher design flexibility is achieved for the dc-dc stage that is decoupled from the charge-pump circuit operation, with no dependence of the power factor on the dc-dc stage gain.

III. CIRCUIT ANALYSIS AND DESIGN

A. Charge-Pump Capacitor Design

The charge pump capacitor needs to be designed for handling the maximum line input current at the peak input voltage. From (3), the input power averaged over a switching cycle is given by

$$P_{IN} = V_{IN} \cdot I_{IN} = f_s \cdot C_P \cdot V_{IN}^2 \quad (5)$$

Where the input voltage is a sinusoid of the angular line frequency ω_l

$$V_{IN} = V_{IN,pk} \sin(\omega_l t) \quad (6)$$

The input power averaged over a line cycle is obtained as follows

$$P_{IN,avg} = \frac{1}{T_l} \int_0^{T_l} P_{IN} dt = \frac{2}{T_l} \int_0^{\frac{T_l}{2}} P_{IN} dt \quad (7)$$

Where T_l is the line period. With the substitution of (5) and (6) in (7), the integral is evaluated to

$$P_{IN,avg} = \frac{1}{2} f_s \cdot C_P \cdot V_{IN,pk}^2 \quad (8)$$

Equating to P_{OUT} / η and rearranging for C_P

$$C_P = \frac{2P_{OUT}}{\eta \cdot f_s \cdot V_{IN,pk}^2} \quad (9)$$

Fig. 9. Proposed integrated-stage structure, with shared switch network and driving circuit.

Where η is the converter efficiency.

B. Charge-Pump Inductor Design

The size of the charge pump inductor determines the length of intervals 2 and 5 in Fig. 7, during which the clamping diodes conduct to clamp the voltage V_C and achieve high power factor. A low value for L_P results in higher conduction times of the clamping diodes and less efficiency. While a high value for L_P results in loss of power factor and high THD. The optimal value of L_P is the one that is sized to store the exact energy stored in the pump capacitor, as follows.

$$\frac{1}{2} C_P \cdot V_P^2 = \frac{1}{2} L_P \cdot I_{LP}^2 \quad (10)$$

Assuming a triangular current in the pump circuit, I_{LP} can be calculated from the total charge Q_P (area of triangle shown in Fig. 7, assuming $Q_C = 0$) as follows

$$Q_P = C_P \cdot V_P = \frac{T_s}{4} \cdot I_{LP} \quad (11)$$

$$I_{LP} = 4 \frac{C_P \cdot V_P}{T_s} = 4 f_s \cdot C_P \cdot V_P \quad (12)$$

Substituting (12) in (10) and arranging for L_P

$$L_P = \frac{1}{16 C_P \cdot f_s^2} \quad (13)$$

C. Energy-Storage Capacitor Design

The energy-storage capacitor needs to store the difference between the instantaneous input power and the constant output power, as follows.

$$P_{DC} = P_{IN} - P_{OUT} \quad (14)$$

Rewriting (5) as the product of two sinusoids

$$\begin{aligned} P_{IN} &= V_{IN_{pk}} \cdot I_{IN_{pk}} \sin^2(\omega_l t) \\ &= \frac{V_{IN_{pk}} \cdot I_{IN_{pk}}}{2} [1 - \cos(2\omega_l t)] \end{aligned} \quad (15)$$

For simplicity, assuming 100 % efficiency, the output power is evaluated to

$$P_{OUT} = P_{IN_{avg}} = \frac{V_{IN_{pk}} \cdot I_{IN_{pk}}}{2} \quad (16)$$

Substituting (15) and (16) in (14) gives

$$P_{DC} = -P_{OUT} \cos(2\omega_l t) \quad (17)$$

Finding the energy

$$\begin{aligned} E_{DC} &= \int_0^{T_l} P_{DC} dt \\ &= E_{DC}(0) - \frac{P_{OUT} \sin(2\omega_l t)}{2\omega_l} = \frac{1}{2} C_{DC} \cdot V_{DC}^2 \end{aligned} \quad (18)$$

Rearranging for V_{DC} and knowing that $V_{DC}(0)$ is equal to the rms voltage [39]

$$V_{DC} = V_{DC_{rms}} \sqrt{1 - \frac{P_{OUT}}{\omega_l \cdot C_{DC} \cdot V_{DC_{rms}}^2} \sin(2\omega_l t)} \quad (19)$$

With the ac ripple being sufficiently smaller than the rms voltage, the ripple amplitude can be evaluated by

$$V_{DC_{ripple}} \approx \frac{P_{OUT}}{2\omega_l \cdot C_{DC} \cdot V_{DC_{rms}}} \quad (20)$$

The energy-storage capacitor C_{DC} needs to be sized such that the voltage across it is higher than the peak input voltage across the line cycle. That guarantees that no cross-conduction occurs through the diode bridge and the pump diode, and accordingly the input current is forced into the pump capacitor that achieves PFC. Therefore, for a high power factor, the following condition needs to be satisfied.

$$V_{DC_{ripple}} < V_{DC} - V_{IN_{pk}} \quad (21)$$

By substitution of (21) in (20), rearranging for C_{DC} , and considering a conservative substitution of the average voltage for the rms, the sizing of the energy-storage capacitor for a given average bus voltage is found from

$$C_{DC} \geq \frac{P_{OUT}}{2\omega_L \cdot V_{DC} \cdot (V_{DC} - V_{IN_pk})} \quad (22)$$

Regarding the double-the-line-frequency ripple, in the conventional two-stage converter structure shown in Fig. 1, where each stage has a separate switch network and control loop, the dc-dc stage controller can be used towards the rejection of the 100/120 Hz ripple on the output current, resulting in low-flicker [40][41]. In the proposed work, however, the two converter stages share the same switch network and controller. Accordingly, controlling the switches towards the 100/120 Hz ripple reduction can result in the distortion of the input current and reduction of power factor, since the same switches are used by the pump circuit to achieve PFC. As a result, the means for the reduction of the double-the-line-frequency ripple (e.g. given by specifications set for the flicker content) in the proposed topology is by increasing the size of the capacitors C_{DC} and/or C_{OUT} , where C_{OUT} provides easier means for that with the availability of high-density low voltage capacitors, compared to the higher voltage across C_{DC} .

D. Class-DE Stage Design

While the class-DE series-resonant converter and the *LLC* converter are very similar topologically, the main difference between them lies in the resonant tank circuit and transformer design. In the class-DE series-resonant converter, the resonant tank is comprised of the series-connection of the tank's resonant inductance L_{RES} and capacitance C_{RES} , where the transformer is designed with a very high (ideally infinite) magnetizing inductance. On the other hand, in the *LLC* converter, the transformer magnetizing inductance is designed to be relatively small (few multiples of L_{RES}) that it becomes incorporated in the resonant tank. That introduces an additional resonant frequency that is lower than the series tank ($L_{RES} - C_{RES}$) resonant frequency and is function of the converter load. Accordingly, the main difference between the two converters lies in the gain function with respect to frequency modulation. That is, however, irrelevant for the proposed converter that uses burst-mode control for modulating the output power of the converter. The transformer magnetizing inductance is accordingly not part of the following analysis.

The design procedure given in [42], which is based on the first-harmonic approximation (FHA) approach for the analysis and design of resonant converters, is used for the class-DE converter design. The procedure starts by the calculation of the load resistance R_L referred to the rectifier input, as follows.

$$R_{REC} = \frac{8R_L}{\pi^2 \cdot n^2} = \frac{8V_{OUT}^2}{\pi^2 \cdot n^2 \cdot P_{OUT}} \quad (23)$$

Where n is the transformer turns ratio (N_S / N_P). The converter voltage gain is the product of the half-bridge gain M_{HB} , the resonant tank gain M_{RES} , and n .

$$M = \frac{V_{OUT}}{V_{DC}} = M_{HB} \cdot M_{RES} \cdot n \quad (24)$$

Knowing that the half-bridge gain is equal to one half and rearranging to evaluate the required resonant tank gain

$$M_{RES} = \frac{2V_{OUT}}{n \cdot V_{DC}} \quad (25)$$

The resonant tank gain is the magnitude of the resonant tank transfer function and can be expressed as a function of the loaded quality factor Q_L and the normalized switching frequency f_n as follows.

$$M_{RES} = \frac{f_n}{\sqrt{[Q_L \cdot (f_n^2 - 1)]^2 + f_n^2}} \quad (26)$$

From the value obtained in (25), and with a proper choice of Q_L , the normalized switching frequency is obtained from (26). Following, for a specified switching frequency, the resonant frequency and tank components are calculated as follows.

$$f_o = \frac{f_s}{f_n} \quad (27)$$

$$L_{RES} = \frac{Q_L \cdot R_{REC}}{\omega_o} \quad (28)$$

$$C_{RES} = \frac{1}{\omega_o \cdot Q_L \cdot R_{REC}} \quad (29)$$

E. Circuit Stresses

Starting with the energy-storage capacitor, the maximum voltage across the capacitor is equal to the maximum allowed voltage ripple on top of the average value.

$$V_{DC_max} = V_{DC} + (V_{DC} - V_{IN_pk}) = 2V_{DC} - V_{IN_pk} \quad (30)$$

With respect to the charge-pump circuit, the voltage stress across the pump capacitor is clamped to the input voltage, and accordingly the voltage stress across the capacitor is

$$V_{P_max} = V_{IN_pk} \quad (31)$$

Substituting (31) in (12), the current stress in the pump circuit inductor is

$$I_{P_max} = 4f_s \cdot C_P \cdot V_{IN_pk} \quad (32)$$

The pump diodes stresses are equal to

$$V_{DP_max} = V_{DC_max} \quad (33)$$

$$I_{DP_max} = I_{P_max} \quad (34)$$

Where the clamping diodes are rated for the same voltage as the pump diode, yet for a lower current stress, which depends on the accuracy of the design of the pump inductor. The class-DE resonant tank components stresses are calculated from the following formula (with a conservative assumption of operation at resonance).

$$V_{RES_max} = \frac{2V_{DC_max} \cdot Q_L}{\pi} \quad (35)$$

$$I_{RES_max} = \frac{2V_{DC_max}}{\pi \cdot R_{REC}} \quad (36)$$

The class-DE stage rectifier diodes stresses are calculated as follows

$$V_{DR_max} = V_{OUT} \quad (37)$$

$$I_{DR_max} = \frac{\pi \cdot I_{OUT}}{2} = \frac{\pi \cdot P_{OUT}}{2V_{OUT}} \quad (38)$$

The voltage stress across the half-bridge switches and the energy storage capacitor is calculated as

$$V_{S_max} = V_{DC_max} \quad (39)$$

While the current in the switches is equal to the sum of the pump-circuit inductor and the class-DE resonant tank currents. With a conservative assumption of zero phase difference between the two currents, the current stress in the switches is equal to

$$I_{S_max} = I_{P_max} + I_{RES_max} \quad (40)$$

F. Achieving ZVS Operation

Assuming operation at the class-DE dc-dc stage tank resonant frequency, the resonant tank voltage gain is unity. Substituting that in (25) gives the following expression for the turns ratio

$$n = \frac{2V_{OUT}}{V_{DC}} \quad (41)$$

Substituting (23) and (41) in (36) gives

$$I_{RES_max} = \frac{\pi \cdot P_{OUT}}{V_{DC}} \quad (42)$$

By dividing (32) by (42) and substitution of (9)

$$I_{P_max} = \frac{8V_{DC_max}}{\eta \cdot \pi \cdot V_{IN_pk}} \cdot I_{RES_max} \quad (43)$$

With a conservative assumption of V_{DC_max} being equal to V_{IN_pk} and 100 % efficiency, the pump-circuit branch current amplitude is at least 2.5 times the class-DE stage branch current amplitude. Accordingly, the pump-circuit branch current is the one defining the criteria for achieving ZVS operation for most of the line cycle. From (9) and (13), the resonant frequency of the pump-circuit tank can be obtained as follows.

$$f_P = \frac{1}{2\pi \cdot \sqrt{L_P \cdot C_P}} = \frac{2f_s}{\pi} \quad (44)$$

Accordingly, the switching frequency is sufficiently higher than the pump tank resonant frequency. That goes in accordance with the assumption of the triangular pump inductor current

Table I. LED Driver Design Specifications

Input Voltage	230 V _{rms}
Line Frequency	50 Hz
Output Power	50 W
Output Voltage	45 V
Power Factor	> 0.9
THD	< 10 %
Efficiency	> 90 %

Fig. 10. Converter design flow chart.

shown in Fig. 7, and results in inductive-mode of operation for the pump circuit branch and ZVS operation is achieved.

IV. 1-MHZ PROTOTYPE

A. Design Specifications

Table I lists the specifications for the designed prototype, which is proposed for LED drivers supplied from European mains for low-mid power applications. An output voltage of 45 V is common for LED modules in the specified power range.

B. Prototype Design Procedure

Fig. 10 shows the design flow chart for the proposed converter. From the design specifications for the input voltage, line frequency, output power, the design process starts by the design of the energy-storage capacitor using (22) and (30). With respect to the choice of the switching frequency, except for the energy-storage capacitor C_{DC} , all of the converter passive components scale inversely with the switching frequency. That is shown by (9), (13), (28) and (29) for the resonant tanks components, as well as the input filter size when designed for a higher cross-over frequency. On the other hand, the size of C_{DC} is dictated by the 50/60 Hz standard line frequency, as shown by (22). Therefore, the higher the switching frequency is, the higher the overall converter's power density. Yet, despite the soft-switching nature of the proposed topology, high-frequency AC loss is still incurred in the magnetic devices. A preliminary choice of the switching frequency that constitutes a good balance between size and loss is made. The charge-pump circuit is then designed using (9) and (31) for the pump capacitor, (13)

and (32) for the pump inductor, and (33) and (34) for the pump diodes. Following, a design choice is made with respect to the transformer turns ratio and the class-DE stage resonant tank loaded quality factor. The choice of the loaded quality factor Q_L constitutes a trade-off between accuracy and implementation complexity. A higher Q_L guarantees a more sinusoidal resonant tank current with lower harmonic content, and thus additional validity for the design equations based on the FHA approach. However, it complicates the magnetic devices design with the need for a higher value for the resonant inductor. The resonant tank components design takes place using (28) - (29) and (35) - (36). The rectifier diodes are then designed using (37) and (38). Eventually, the shared half-bridge switches stresses are calculated from (39) and (40). A design decision is then made for the output voltage, where a design iteration with respect to a higher quality factor or different turns ratio may be needed to obtain the desired V_{OUT} . Another decision is made with respect to the obtained double-the-line frequency ripple, where a larger energy-storage capacitor may be required. Finally, a design decision is made with respect to the converter power density, and a design iteration with respect to the switching frequency can take place to meet the desired converter size.

In this work, a switching frequency of 1 MHz is chosen for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. A lower switching frequency will not be suitable for the adopted dimming control scheme based on burst-mode operation. In order to guarantee a high control resolution, the burst signal frequency needs to be low enough compared to the switching frequency, without falling into the audio band (up to 20 kHz). Accordingly, a few-hundred kHz design would be challenging to control with a high resolution using burst-mode operation. On the other hand, prior art has shown that the optimal switching frequency range with respect to the ac losses in the magnetic components is 500 kHz – 2 MHz [43], with the peak performance at 1 MHz using the 3F64 magnetic material adopted in this work. A low Q_L value is chosen in order to enable the integration of the resonant inductor into the transformer through the transformer leakage inductance. That

Fig. 11. Prototype picture. (a) Top side, (b) bottom side.

results in the reduction of component count and increased power density. Table II lists the obtained design values according to the specifications given in Table I, with a loaded quality factor of 0.3, a transformer turns-ratio of 4:1 for the class-DE stage, and assuming 360 V for V_{DC} and 95 % efficiency.

C. Implementation

Fig. 11 shows a photograph of the implemented prototype. The converter is assembled on a four-layer printed circuit board (PCB), which is mounted on a test-bench board with terminals for testing. Because of the charge-pump circuit operation, a high-frequency ac current runs through the input bridge, which is implemented using four fast-recovery diodes. Gallium nitride (GaN) FET switches are employed for the half-bridge, as they show superior performance over the silicon and silicon carbide (SiC) counterparts for that voltage range. SiC Schottky diodes are employed for the pump circuit diodes, namely D_P , D_{C1} , and D_{C2} . They show higher efficiency compared with the silicon high-voltage alternatives. On the other hand, silicon Schottky diodes are employed in the high-frequency rectifier full bridge. Electrolytic capacitors are chosen for C_{DC} and C_{OUT} as they offer high capacitive densities, where they can be replaced with ceramic capacitors with higher lifetime at the expense of larger size/cost for the same capacitance budget. That constitutes a trade-off between reliability and power density/cost. Table III shows a breakdown of the incorporated power stage bill-of-materials (BoM).

A half-bridge gate driver (Si8274 by Silicon Labs, Austin, TX, USA) drives the half-bridge switches. The dead time is set to 88 ns using a fixed resistor and adjusted to achieve ZVS with minimal reverse-conduction through the switches [44]. The gate driver package is placed adjacent to the devices' gate terminals in order to control noise coupling from the power loop

Table II. Design Values Calculated from Circuit Analysis Equations

Parameter	Calculated
$C_{DC\ min}$	6.32 μ F
$V_{DC\ max}$	395 V
C_P	0.99 nF
V_P	325.3 V
L_P	63.13 μ H
I_{LP}	1.29 A
$V_{DP\ max}$	395 V
$I_{DP\ max}$	1.29 A
L_{RES}	25.08 μ H
C_{RES}	1.01 nF
$V_{RES\ max}$	75.44 V
$I_{RES\ max}$	0.48 A
$V_{DR\ max}$	45 V
$I_{DR\ max}$	1.75 A
$V_S\ max$	395 V
$I_S\ max$	1.77 A

to the gate-drive loop. Another layout consideration taken is the separation of the source terminal to the gate-driving and power loops in a star-connected fashion, which is allowed with the source-sense pad of the GS-065-004-1-L device package. That helps alleviate the gate ringing resulting from the common-source inductance. The driving signal is generated from a voltage controlled oscillator (LTC6990 by Analog Devices) and the 1-MHz frequency is set by fixed resistors.

It should be noted that the effect of switching frequency modulation on both stages is not monotonic. An increase in f_s leads to higher input power, as per (3). On the other hand, the higher f_s is, the lower the resonant tank gain for the dc-dc stage, and accordingly lower output power. The difference in the input and output powers can lead to a stress on the energy-storage capacitor if not modeled. Accordingly, switching frequency modulation is not preferable for this architecture, and burst-mode operation prevails. To enable dimming functionality, a 20-kHz PWM signal is applied to the gate driver enable input for on/off modulation of the converter, where the output power is modulated using the PWM signal duty-cycle. To suppress the PWM signal noise on the input current, an LC filter of 10-mH choke and 100-nF shunt capacitor is incorporated on the test-bench board, resulting in a cross-over frequency of 5 kHz.

Custom magnetic components are implemented for the charge-pump circuit inductor L_P and the class-DE converter transformer. The 3F46 material from Ferroxcube is selected for both devices, as it has low losses at the design switching frequency. EFD 15/8/5 cores are used for both devices. The class-DE converter transformer primary and secondary windings are divided between the core halves and separated in order to achieve a low coupling coefficient. That enables the integration of the resonant tank series inductance L_{RES} in the transformer leakage inductance, thus saving the space and cost for an additional magnetic device. The magnetic components small-signal characterization is conducted using a 40 Hz – 110 MHz precision impedance analyzer (Agilent Technologies 4294A). At 1 MHz, an inductance of 68 μH and an ESR of 0.7 Ω are measured for the pump circuit inductor L_P , whereas a total primary side inductance of 139 μH and an ESR of 1.5 Ω are obtained for the class-DE transformer, with 26 μH measured leakage inductance used towards the resonant tank inductance

Table III. Prototype power-stage BoM

Component	Prototype	Type
L_{IN}	100 μH	Inductor
C_{IN}	2 * 15 nF	Ceramic
Diode Bridge	4 * ESH1GM RSG	Si Fast Recovery
C_{DC}	1 x 10 μF 2 x 0.1 μF	Electrolytic Ceramic
D_P, D_{C1}, D_{C2}	GB01SLT06-214	SiC Schottky
C_P	1 x 470 pF 1 x 560 pF	Ceramic (C0G) Ceramic (C0G)
L_P	68 μH	Custom design
Q_{HS}, Q_{LS}	GS-065-004-1-L	GaN Switches
C_{RES}	3 x 330 pF	Ceramic (C0G)
L_{RES}	26 μH	Custom design
$D_{R1}-D_{R4}$	PMEG60T20ELP	Si Schottky
C_{OUT}	1 x 100 μF 2 x 1 μF	Electrolytic Ceramic

Fig. 12. Obtained prototype measurements across operational range. (a) Output power and efficiency. (b) Output voltage and current. (c) Power factor and input current THD.

L_{RES} . A secondary side inductance of 7.2 μH is measured, which results in an effective transformer turns ratio of 3.96:1.

D. Experimental Results

The converter is tested for operation from 230 V_{rms} across the burst signal duty-cycle modulation between 1-100 %. The prototype is loaded with an industrial LED lamp (36-W 3430-lm 40-48-V RRC03645-01 by ROBUS,) with 105 LEDs connected in a 7 × 15 array. Fig. 12 shows the obtained results across operational range. The prototype delivers up to 42 W of output power. The reduced output power at 1 MHz is the result

(a)

(b)

Fig. 13. Scope images for the implemented prototype waveforms at full-load operation. (a) Line-frequency waveforms (100 V/div, 200 mA/div, with 5 ms/div). (b) Switching-frequency waveforms (100 V/div, 1 A/div, with 200 ns/div).

of an offset in the pump inductor implemented value compared to the calculated one, and can be fixed by reducing the pump inductor size, increasing the pump capacitor size, or operating at a higher switching frequency. The efficiency across the output power range is shown in Fig. 12(a), where a peak efficiency of 90.4 % is achieved at full-load, with an efficiency of 88 % at half-load. The figure also shows the correspondent burst signal duty cycle across the load range. Fig. 12(b) shows the output voltage and current across the operational range, where an output current range of 20 – 900 mA is achieved with an almost linear dependence on the burst signal duty-cycle. That simplifies the dimming control and enables the fine-tuning of the current with a PWM burst signal of high resolution. The power quality results are shown in Fig. 12(c), where a power factor higher than 0.98 and a THD lower than 10 % are obtained across the power range where power factor correction is demanded by the IEC 61000-3-2 standard for class-C devices (> 25 W).

Fig. 13 shows scope captures for the implemented prototype waveforms at full-load operation. Fig. 13(a) shows the line-frequency waveforms, including the input voltage and current, output voltage and the voltage across the energy-storage capacitor C_{DC} . The input and output voltages are measured using high-voltage differential probes (Testec SI 9001), the input current using a 50-MHz current probe (LeCroy AP015), while the dc capacitor voltage is measured using a 500-MHz 10x voltage probe with 9-pF capacitance. The figure shows an

(a)

(b)

Fig. 14. Scope images for the implemented prototype waveforms at half-load operation. (a) Line-frequency waveforms (100 V/div, 200 mA/div, with 5 ms/div). (b) Bursts of V_{SW} (blue) and I_{RES_sec} (green) waveforms (100 V/div, 1 A/div, with 50 μs/div).

almost-sinusoidal input current in phase with the input voltage, and an average output voltage of 47 V. V_{DC} is seen to be higher than V_{IN} across the line cycle, which goes in accordance with the analysis in Section III-C to achieve high power factor. The reason for the flat peaks in the input current is due to the implemented pump inductance L_p value being slightly higher than the designed value, which is the same reason for the reduced output power than the specification. That, however, has negligible effect on the power factor and can be resolved by using planar magnetic devices to reduce the tolerances associated with Litz-wire-based magnetics. Fig. 13(b) shows the switching-frequency waveforms at full-load operation. The pump-circuit inductor and transformer-secondary currents are measured using 50-MHz current probes (LeCroy CP030 and AP015, respectively). The transformer-secondary current is seen to be sinusoidal owing to the operation at resonance, thus ensuring the validity of the design process of the class-DE stage which is based on the FHA approach. On the other hand, the pump-circuit inductor current is seen to be triangular, as the switching frequency is considerably higher than the charge-pump tank resonant frequency. The pump inductor current has an amplitude that is larger than the class-DE resonant tank current primary, which is $1/n$ times the transformer secondary current. The switching-node voltage waveform V_{SW} is measured using a 500-MHz 10x voltage probe with 9-pF capacitance. The figure shows that the pump-circuit current is lagging the switching-node voltage, resulting in inductive mode of

Fig. 15. Input current harmonics distribution at half- and full-load operation.

Fig. 16. LED current and voltage at full-load (top) and half-load (bottom) operations.

operation and a trapezoidal V_{SW} waveform, and ZVS is obtained, which is in agreement with the analysis in Section III-F. A short interval of reverse conduction is observed on the V_{SW} waveform, and can be eliminated with a finer tuning of the dead time.

Fig. 14 shows scope captures for the implemented prototype waveforms at half-load operation. Fig. 14(a) shows a reduced input current amplitude, while the current is still proportional to and in phase with the input voltage, resulting in high power factor. Fig. 14(b) shows the switching-frequency waveforms with an extended time scale to show the switching-frequency pulse skipping respective to the burst-signal duty-cycle of 50 %.

Fig. 15 shows the input current harmonics distribution at full- and half-load operations against the IEC 61000-3-2 standard class-C device limits, where THD figures of 6 % and 9 % are measured, respectively. It is shown that the measured harmonics magnitudes are well within the limits set by the standard across the load range.

Fig. 16 shows the measured LED load voltage and current at half- and full-load operation. It is seen that a considerable 100-Hz ripple component exists on the load current. By doubling the

Fig. 17. Thermal picture of prototype under full-load operation.

size of the energy-storage capacitor C_{DC} , the ripple is reduced about 25 % of the average current.

Fig. 17 shows a thermal picture of the converter under full-load operation after the temperature reached steady state. It is seen that the converter is thermally stable, with the bridge diodes (rated for 150 °C) at a maximum temperature of 72 °C. In the actual application, the driver is usually potted, which reduces the temperature of the converter components.

Table IV shows a comparison of the proposed work with several recently reported LED drivers. Starting with the prior art charge-pump-based converter reported in [19], the prior art converter was proposed as a solution for the ac-dc stage only. As a result, despite the lower component count, prior art converter offers a much higher output voltage, which is dictated by the criteria to achieve high power factor; where a high-frequency transformer and possibly a bridge rectifier need to be incorporated to achieve a lower output voltage. Otherwise, a subsequent dc-dc stage is needed, which will incur additional components and reduced overall efficiency. On the other hand, the proposed solution offers end-to-end (mains to LED load) conversion capability, with few components and accordingly low cost. In addition, splitting the current paths from the switching node results in reduced stress on the resonant tank, which is a main limitation of the prior art topology. That results in a higher efficiency across load range, and substantially higher efficiency at full load, in addition to simplifying the magnetic devices design. More specifically, in the prior art converter, a resonant inductor of 158 μH is needed to carry a 1.6-A_{pk} 1-MHz sinusoidal current, resulting in a core size of EFD 25/13/9. In the proposed converter, two inductors of 68 μH and 25 μH are needed to carry 1-MHz currents of 1.3 A_{pk} and 0.48 A_{pk}, respectively. The first inductor has a core size of EFD 15/8/5, and the second is integrated into a transformer of the same core size. That results in resonant magnetic devices size and mass of 5.7 cm³ and 16.6 g of the prior art converter vs. 2.1 cm³ and 5.6 g, respectively, for the proposed converter (excluding windings mass). That is reflected in the total converter volume and mass figures shown in Table IV, resulting in power densities of 1.2 W/cm³ for the prior art converter (excluding dc-dc converter) vs. 1.8 W/cm³ for the proposed

Table IV. Comparison with Prior Art

Reference		[29]	[27]	[8]	[31]	[34]	[19]	This work
Year		2019	2018	2018	2016	2017	2020	2020
Type		PWM-resonant	Resonant	PWM	PWM-resonant	PWM-resonant	Resonant	Resonant
Application		LED driver	LED driver	LED driver	PFC stage	LED driver	PFC stage	LED driver
Input Voltage [V_{ms}]		110	180-250	Universal	90-135	220	230	230
Output Power [W]		100	150	60	100	21	50	42
Output voltage [V]		50	32	74	45, 50	30	300	45
Power Factor	FL	0.99	0.99	0.91	0.99	0.99	0.99	0.99
	HL	0.96	0.98	-	-	-	0.95	0.98
THD [%]	FL	2	8	-	6	2.6	8.6	6
	HL	8	17	-	-	-	18	9
Efficiency [%]	FL	90	91	93	94	92	84	90
	HL	88	93	-	92	90	88	88
Switching freq. [kHz]		100	55	100	130	50	1000	1000
PFC Control		PWM+PFM	-	PWM	PWM+PFM	PWM	Inherent	Inherent
Output Power Control		PWM+PFM	-	PWM	PWM+PFM	PWM	PFM	Burst-mode
Number of Components		18	19	15	19	18	17	23
Volume [cm^3]		102*	465*	94*	315*	145*	41	24
Mass [g]		-	-	-	-	-	40	21
Power Density [W/cm^3]		0.98*	0.32*	0.64*	0.32*	0.18*	1.2	1.8

* Estimated converter heights from prototype picture and bill of material.

converter. Another advantage of splitting the resonant tanks is the easier ZVS maintenance in the proposed topology, since the charge-pump circuit current peak is sufficiently higher than the class-DE stage current with more phase lag, dominating ZVS criteria fulfillment (as covered in Section III-F). It is seen that the power factor and THD figures for both converters are within close proximity at full-load operation. However, the prior art converter offers less power factor and higher THD at half-load than the proposed structure, owing to the dependence of the power factor on the output voltage. On the other hand, the proposed converter offers a high power factor and low THD across the load range, as well as added flexibility for the dc-dc stage design for any output voltage.

With respect to other reported driver solutions that include different flavors of PWM, PWM-resonant, and resonant converters, it can be seen that the proposed solution is designed with a significantly higher switching frequency than the prior art. That results in a considerably higher power density, and at the same time, a high efficiency of up to 90 % at full-load. While the reported solutions are controlled to achieve PFC, the proposed converter achieves PFC inherently, with power factor and THD figures on par with those achieved by the reported solutions.

V. CONCLUSION

A resonant LED driver is presented. The system incorporates a charge-pump PFC converter with inherent PFC capability, and a class-DE dc-dc converter. Both converters share the same switch network and gate-driving circuit in an integrated-stage architecture. Compared to prior art, the proposed architecture offers lower circuit stresses and high efficiency, in addition to higher flexibility with low components count. Furthermore, the operation is based on soft switching, allowing for increased switching frequencies and higher power densities. A 1-MHz prototype is built and tested. The prototype achieves up to 42 W of power, with a power density of $1.8 W/cm^3$, a power factor

of 0.99, a THD of 6 %, and an efficiency of up to 90 %. The input current harmonic magnitudes are well-within the limits of the IEC 61000-3-2 standard. The proposed converter has the potential for operation at higher frequencies, as all of the circuit components scale with the switching frequency (other than the dc capacitor size, which is dictated by the 50-/60-Hz standard line frequency).

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