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Published in:

Additional Conferences (device Packaging, Hitec, Hiten, and Cicmt)

Link to article, DOI:

[10.4071/2380-4491.2021.HiTEC.000048](https://doi.org/10.4071/2380-4491.2021.HiTEC.000048)

Publication date:

2021

Document Version

Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):

Duraij, M. S., Xiao, Y., Zsurzsan, G., & Zhang, Z. (2021). Enhancement Mode GaN-FETs in Extreme Temperature Conditions, Part I: Static Parasitic Parameters. *Additional Conferences (device Packaging, Hitec, Hiten, and Cicmt), 2021*(HiTEC), 000048-000052. <https://doi.org/10.4071/2380-4491.2021.HiTEC.000048>

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Enhancement Mode GaN-FETs in Extreme Temperature Conditions, Part I: Static Parasitic Parameters

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Abstract

Smaller packaging and sizing of power electronics and higher operating temperatures of switching devices call for an analysis and verification on the impact of the parasitic components in these devices. Found drift mechanisms in an eGaN-FET are studied by literature and related to measurements performed in extreme temperature conditions far beyond the manufacturer recommended operating range. A thermal chamber was build to precisely measure the effect of temperature in these devices using a curve tracer. It is found that the increment in R_{DSon} , I_{DSS} , I_{GSS} and V_{SD} can be justified by the theory and backed up by measurements. It is also found that the particular eGaN-FET can be suited for extreme temperature operating conditions.

Key words

Conduction losses; Device characterization; eGaN-FET; High temperature; Parasitic components

I. Introduction

High temperature applications gain more focus in all industries where power converter designs must fit in smaller and smaller form factors. In high temperature industries like oil and gas, military, aeronautical and geothermal, power devices must be verified at extreme operating conditions. Temperature rating in these industries may vary by the application, where, for example, the oil and gas industry are reaching to deeper well environments. Therefore, encountered temperatures of electronic components in these operating conditions can reach up to 200 degrees Celsius. The need for high temperature rated devices has been outlined decades ago by [1] and more recently by the introduction of high temperature rated electronics by [2,3]

GaN material has been found to be well suited as a semiconductor material capable to withstand high temperature stress. GaN transistors have been used in RF circuitry in data transmission channels for the oil and gas industry. Cunningham et.al. [4] have implemented a wideband amplifier using GaN RF transistors in the 260 MHz range. Also, in power conversion within the same industry applications can be found such as Perrin et.al. [5]. Here in the use of eGaN-FETs in a fly-back converter, capable of delivering an output power of 2W under 200 degrees Celsius operation.

When using these types of eGaN-FETs in extreme temperature conditions, as 200 degrees Celsius ambient temperature, the device operating parameters must be verified. Domestic appli-

cations see dimensioning of absolute maximum temperatures of 150 degrees Celsius where eGaN devices show great reliability [6]. With the operating temperatures extending far above the rated values a drastic change in performance can be expected which lead to significantly larger design efforts for engineers.

In this paper the influence of temperature towards static parasitic components is addressed. Static parasitic components are considered where the device is either in a fully on or off state and therefore do not include the switching or dynamic characteristics. The dynamic characteristics of eGaN-FETs in extreme temperatures is addressed in [7].

The most widely used parasitic in the use of switching devices is the residual resistance in the conductive channel (R_{DSon}) of the device when the FET is completely turned on. When the device is driven with a lower gate-source voltage (V_{GS}), the R_{DSon} increases due to operation in its linear region. The R_{DSon} is used to calculate the losses seen in the device when it operates as a switch when it is fully conductive.

When the device is in its on state a leakage current in the gate (I_{GSS}) will be present. This current must be supplied by a gate driver to keep the device in its operating condition to allow a current flow from drain to source. The leakage current is expected to be highly dependent on the temperature of the switching device [8,9]. For high temperature applications that incorporate a high side driver circuit with a boot-strap capacitor, this leakage current becomes of importance when dimensioning

this capacitance.

When the device is in its off state a voltage will be present from drain to source across the device. As with the gate, a leakage current is present in this terminal and expected to be dependent on the voltage across the device as well as the temperature of operation [10]. The drain to source leakage current is referred to as (I_{DSS}).

One more static operation of the FET can be found when the device is in its off state and a current is flowing in the reverse direction from source to drain. During this reverse conduction interval, a voltage drop across a body diode can be observed. For eGaN-FETs it is known that this voltage drop is higher than for its MOSFET counterparts. The reverse voltage drop becomes of interest when estimating the losses during this time interval. However, due to the absence of a reverse recovery charge, the estimated losses and impact on Electromagnetic Compatibility (EMC) due to reverse conduction can be small. When building an inverter using eGaN-FETs this voltage drop during reverse conduction can lead to distortion artifacts in a sinusoidal output waveform compared to the use of MOSFETs.

After this introduction the paper will address a short theory overview behind the drift of these parameters in section II. Section III will discuss the measurement setup and method where section IV will be presenting and discussing the results. Conclusion and future work are outlined in section V.

II. Theory of parasitic drift

Potentially the most lossy characteristic of a switching device is the R_{DSon} . The residual resistance in the channel is build up by several mechanisms in series. Identifying these elements in the construction of an eGaN-FET given an overview of these elements.

Figure 1: Construction of an eGaN-FET and its elements contributing towards the total R_{DSon} . Reprinted from [10]

The channel resistance when the eGaN-FET fully on is proportional to the mobility and the quantity of the electrons in the channels two dimensional electron gas (2DEG). The length and width shape the channel to its performance where a wider and shorter channel is preferred. However, a shorter channel limits the applied static voltage present across the channel when a device is turned off. Since the gate is the terminal controlling the current in channel a $R_{2DEG(gate)}$ is defined for the area underneath the gate.

The drain metal and source metal connections see an

impedance, which is depended on the used allow for making these connections. Temperature coefficients in these connections can be found in the range of $3.8 \times 10^{-3} \text{ K}^{-1}$ where the coefficients of the 2DEG layer are significantly higher around $1.3 \times 10^{-2} \text{ K}^{-1}$ [10]. This means that the expected increase of resistance in high temperature finds its largest contributor from the 2DEG.

In a reverse conduction state the eGaN device can conduct current from source to drain. Different than in silicon devices, this is path is not formed by a p-n junction, but by turning on the 2DEG. A similar thermal dependency can be expected due to the thermal characteristics of this 2DEG, where the voltage drop across the channel is increased with temperature. GaN transistors do not store any charge in this configuration and therefore a reverse recovery charge is absent ($Q_{RR} = 0$).

Leakage current in the drain can flow from drain to source, from drain to gate or from the drain into the substrate of the device. The total leakage current I_{DSS} is the sum of these.

III. Measurement methods

The devices that were selected for the parasitic measurements are available from commercial vendors. The selection of the chosen eGaN-FETs was a straightforward decision due to the build-up of their devices. The selected eGaN-FET are made available as a bare die with exposed solder bumps, like a flip-chip. Other manufacturers may use a packaging strategy where the die is encapsulated in a FR4 PCB material. Selected eGaN-FETs were preferred to minimize secondary effects in this test due to bonding and sintering.

Table 1: Typical EPC8010 device parameters in 25°C [11]

R_{DSon}	160 m Ω
I_{DSS}	20 μA
I_{GSS}	100 μA
V_{SD}	2.5 V

The eGaN-FET device was mounted in dedicated break-out board for testing at high temperature. The footprints of the very small FETs have been routed out to allow wire connections for a four-point measurement. A final residual of copper trace in the path has to be compensated for which is highlighted in Fig. 2. The length of the trace from the connection terminals to the footprint is evaluated to be $R_{PCB} = 37.9 \text{ m}\Omega$ at 25°C . Adding the temperature coefficient to the calculation of this resistance allows for an error correcting R_{PCB} to get to the correct R_{DSon} in the device.

Figure 2: Layout and implementation of PCB break-out fixture where the addition of R_{PCB} is highlighted in red.

A thermal chamber was built to create a stable measurement environment. Available thermal chambers were limited to a maximum of 180 °C where a total chamber temperature of 225 °C was desired. The 25 °C excess of the 200 °C ambient temperature from the industry is to incorporate self-heating effects in these measurements. When operating in the field it can be expected that the device itself heats up in these conditions and therefore the effects in doing so can be evaluated.

The thermal chamber was built using aerated concrete blocks as can be seen in Fig. 3. The heating elements were stripped out from a countertop kitchen oven and placed in carved slots in the blocks. The heating elements were hooked up with a Solid-State Relay (SSR) which was on its turn controlled with an Arduino Uno equipped with a temperature sensor. A PI controller in the Arduino Uno took care of controlling the chambers temperature tightly to its set values. The control was configured as a pulse with modulation of 0.5 Hz with a resolution of 0.5 % duty cycle step size.

A Keysight B1505A Power Device Analyzer / Curve Tracer device was used to measure the performance parameters of the eGaN-FETs. An interconnect was prepared to connect the Curve Tracer to the components in the oven by the means of high temperature rated wire connections.

Figure 3: Overview of the test setup and thermal chamber in close-up.

IV. Results

The first test shows the variance in the on-resistance in the eGaN-FET for different temperatures in Fig. 4. The measurement was carried out using a drain source current of 0.5 A. The resulting

measured voltage from drain to source looks noisy which is due to the long measurement harness between the curve tracer and the thermal chamber. However, it can be observed that the device matches the expected R_{DSon} at $V_{GS} = 5$ V from the datasheet [11] in 25 °C, as well as the curve does at 125 °C.

Figure 4: Measurement results of R_{DS} versus V_{GS} in various temperatures.

Using SPICE software, a sanity check of these measurements was performed comparing the data to a simulation at 25 °C in Fig. 5. Here the eGaN-FET would see an increased resistance for applied gate-source voltage of 2.5 V. When the gate-source voltage was increased to 5 V the measured R_{DSon} of the device would match the measurements at 139 mΩ. In high temperature at 200 °C the R_{DSon} was around 296 mΩ in the measurements where the simulations show a correlating 299 mΩ.

Figure 5: Simulated results of R_{DS} versus V_{GS} in various temperatures.

The increase of R_{DSon} in temperature can be seen all the way up to 225 °C. At 150 °C the R_{DSon} is about 1.9 times the normal

value and at 225 °C this is increased to 2.5 times. The normalized On-State Resistance graph in the datasheet can therefore be extrapolated towards 225 °C.

Figure 6: Measurement results of I_{DSS} versus V_{DS} in various temperatures.

The measured leakage current in the drain is highly dependent on the junction temperature of the device as the plot shows in Fig. 6. An quadratic increase is seen when temperature is creased from 150 °C up to 225 °C in 25 °C steps. This matches the projected increase that was shown by [10] and proves that one can extrapolate the increment of I_{DSS} to 225 °C

Figure 7: Measurement results of I_D versus V_{DS} in various temperatures.

When the 2DEG in the eGaN-FET is used during reverse conduction, plotted in Fig. 7, the losses of the eGaN-FET are increased due to the higher reverse voltage drop. For comparison, when a 1 A current is flowing in the reverse direction at 25 °C a higher voltage drop in the channel is present in high temperature environments. This higher voltage drop leads to higher

losses in the device and more self-heating in its turn. There is a knee point visible in. For a small current the voltage drop from source to drain can be reduced in temperature when utilizing the reverse conduction. One could use an over dimensioned eGaN-FET and run low reverse direction currents to optimize losses in a power stage. This would come at the likely penalty of a slower switching stage due to increased capacitances in such a device.

Figure 8: Measurement results of I_{GSS} versus temperature.

The gate leakage current depicted in Fig. 8 follows the expected trend described earlier in this paper. Exponentially increasing gate leakage currents I_{GSS} in temperature follow the same trend as for the drain leakage currents I_{DSS} . An exponential increase can be observed when temperature is increased and therefore come of high importance when dimensioning a possible bootstrap capacitor application.

V. Conclusion and future work

The parasitic components in the eGaN-FET in its static operation modes fit the expected increase in R_{DSon} , I_{DSS} , I_{GSS} and V_{SD} when increasing the temperatures. Listed curves from the datasheet can be extrapolated for up to 225 °C to evaluate the performance of the parts in these extreme conditions. With these measuementes it is also shown that devices are capable of operation in these temperatures. More research is needed to evaluate the impact on lifetime in these conditions. Lifetime tests as well as a model adaption towards high temperature environments can be addressed in future work packages.

Acknowledgment

The authors would like to thank the Danish Innovation Fund for their financial contribution towards this project under reference number 9065- 00005B

References

- [1] J. J. Den Boer, "The use of high temperature electronics in downhole applications," *HITEN 1999 - 3rd European Conference on High Temperature Electronics*, pp. 149–152, 1999.
- [2] M. Taylor, "Introduction of Texas instruments high temperature semiconductors," *Proceedings - 2009 Imaps International Conference on High Temperature Electronics Network, Hiten 2009*, pp. 57–63, 2009.
- [3] B. Kerrigan, F. L. Pour, and D. Sam Ha, "System Design of a High-Temperature Downhole Transceiver: Part II - Transmitter," *Midwest Symposium on Circuits and Systems*, vol. 2019-Augus, pp. 822–825, 2019.
- [4] M. L. Cunningham, D. S. Ha, and K. J. Koh, "A high temperature wideband low noise amplifier for downhole applications," in *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2016-July, pp. 938–941, IEEE, 2016.
- [5] R. Perrin, N. Quentin, B. Allard, C. Martin, and M. Ali, "High-Temperature GaN Active-Clamp Flyback Converter with Resonant Operation Mode," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1077–1085, 2016.
- [6] A. Lidow, R. Strittmatter, C. Zhou, and Y. Ma, "Enhancement mode gallium nitride transistor reliability," *IEEE International Reliability Physics Symposium Proceedings*, vol. 2015-May, pp. 2E11–2E15, 2015.
- [7] M. S. Duraij, Y. Xiao, G. Zsurzsan, and Z. Zhang, "Enhancement Mode GaN-FETs in Extreme Temperature Conditions, Part II: Dynamic Parasitic Parameters," *HiTEC 2021, Submitted for publication*, no. HiTEC, 2021.
- [8] W. S. Tan, P. A. Houston, P. J. Parbrook, D. A. Wood, G. Hill, and C. R. Whitehouse, "Gate leakage effects and breakdown voltage in metalorganic vapor phase epitaxy Al-GaN/GaN heterostructure field-effect transistors," *Applied Physics Letters*, vol. 80, no. 17, pp. 3207–3209, 2002.
- [9] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Temperature dependence of gate-leakage current in AlGaIn/GaN high-electron-mobility transistors," *Applied Physics Letters*, vol. 82, no. 18, pp. 3110–3112, 2003.
- [10] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion: Second Edition*, vol. 9781118844762. 2014.
- [11] EPC, "EPC8010 – Enhancement Mode Power Transistor, Datasheet," pp. 1–6, 2013.