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Design of a Single Chip, Single Core, ZVS Buck Converter in MHz Domain

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Abstract—Venturing into MHz switching frequency promotes the integration of inductive DC-DC converter into mobile devices. Combining GaN power switch with low-loss ferrite core materials opens up new possibilities for high-frequency operations. In this work, we investigate the design of a single core inductor and single chip half-bridge switch for ZVS buck converter. Design guidelines are accompanied by preliminary performance assessment via simulations. To demonstrate the performance of our device, we fabricated and tested a 20 W prototype converting 6 – 12 V to 4 V at 2 MHz switching frequency. The prototype achieves $\eta > 90\%$ at $P_{\text{out}} > 15\text{ W}$ and power density of 9.26 W/m^2 with $< 5\text{ mm}$ thickness.

Index Terms—high frequency, high power density, ZVS, single chip half-bridge

I. INTRODUCTION

As the capacity of batteries in mobile devices keeps growing, faster and faster charging is needed. The USB Power Delivery architecture [1] provides multiple input voltages (5, 9, 15, and 20 V) and input currents up to 5 A. A promising avenue to accelerate charging is the switched capacitor DC-DC converter. However, this device is limited by voltage regulation since the division factor is architecture dependent. Inductive DC-DC converters, such as the buck converter, is advantageous in this regard. Nevertheless, combining miniaturization with high performance is still a challenge.

Typically, the switching frequency of the converter is pushed too higher values to reduce its overall size [2]–[4]. For smartphone charging applications, the switching frequency is expected to be in the MHz range. In this regime, the switching power loss is often the primary factor limiting the converter performance. The main mitigation measure in this respect is to operate in ZVS mode. Furthermore, new GaN HEMT device also offers improved FOM over Silicon technology. As for the inductive components, new materials such as PC200 [5] and ML91S [6] open new possibilities. In this work, a combination of this two main enablers of HF power converter will be tested, while keeping the final footprint minimal, i.e. using only one chip and one core.

II. ZVS-QSW BUCK CONVERTER

Despite its simplicity, the buck converter is still used extensively in low power conversion (up to 100 W) applications; its main advantage is the low number of active and passive

components. However, when venturing into high frequency operations, it has one major drawback: hard switching, which will make the switching loss in power switches high. One way to mitigate the high switching loss is the Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) technique. This scheme entails using the inductor current to charge and discharge the output capacitance of the semiconductor switches, resulting in a significantly lower output-capacitance-related switching losses, at the price of a higher conduction loss. To achieve this benefit, the circuit has to be dimensioned properly. Once the circuit parameters have been selected, the losses can be estimated.

A. Circuit Dimensioning

The first critical design parameter is the boundary inductance value, as given by eq. (1). When the inductance L of the circuit is larger than L_{BCM} , the converter enters the continuous conduction mode, transitioning to hard switching. On the other hand, when $L < L_{\text{BCM}}$ the inductor will feature a negative current valley and achieve the ZVS operation mode. However, L cannot be too much smaller than L_{BCM} , otherwise the current ripple generates excessive conduction losses. As a rule of thumb, 70% - 80% L_{BCM} is a good compromise to ensure ZVS at the nominal output current.

With inductance determined, other parameters such as peak and RMS current, and peak flux density follow. The peak-to-peak current is given by eq. (2), while its RMS value is shown in eq. (3). Please note that eq. (3) is only valid within the ZVS-QSW regime, i.e., when the inductor current has a negative valley value. Peak flux density can be estimated from eq. (4) when using a standard core geometry with known effective core cross section A_c . Note that the peak flux density B_{PK} in this formula includes a DC bias. Altogether, these parameters can be used to select the proper core and coil design.

Another important aspect is the dead time selection. Having too small dead time will make an incomplete ZVS transition, while having it too large will create additional losses through the reverse diode conduction. In a buck converter, dead time is inserted at the inductor current peak ($I_{\text{L,OFF}}$) transition and at the inductor current valley ($I_{\text{L,ON}}$) transition. At the current peak, coinciding with the control switch turn-off, the analysis is analogue to that of the hard-switching explained in [7]. At

the current valley, the dead time must be large enough to allow charging and discharging of the switches' output capacitance.

$$L_{\text{BCM}} = \frac{D \cdot T_{\text{SW}}}{2 \cdot I_{\text{OUT}}} \cdot (V_{\text{IN}} - V_{\text{OUT}}) \quad (1)$$

$$\Delta I_{\text{L,pp}} = \frac{D \cdot (V_{\text{IN}} - V_{\text{OUT}})}{L \cdot f_{\text{SW}}} \quad (2)$$

$$I_{\text{L,rms}} = \sqrt{I_{\text{OUT}}^2 + \left(\frac{\Delta I_{\text{L,pp}}}{2\sqrt{3}} \right)^2} \quad (3)$$

$$B_{\text{PK}} = \frac{L \cdot \left(I_{\text{OUT}} + \frac{\Delta I_{\text{L,pp}}}{2} \right)}{N_{\text{turns}} \cdot A_c} \quad (4)$$

In the equations above, D is the duty cycle of buck converter, T_{SW} is the switching period, V_{IN} is the converter input voltage, V_{OUT} is the output voltage, I_{OUT} is the nominal output current, $\Delta I_{\text{L,pp}}$ is the peak-to-peak inductor current, $I_{\text{L,rms}}$ is the RMS inductor current, N_{turns} is the number of winding turns in inductor, and L is the selected inductor value.

B. Semiconductor Losses

The first big chunk of converter losses comes from the power semiconductor or switches. This loss can be separated into conduction and switching loss. Conduction loss can be calculated using RMS current formula in (5), (6) and the power switches' $R_{\text{DS,ON}}$ value. Switching loss for hard-switching topology has been well described in [7]. The remaining switching loss components for ZVS-QSW buck converter are therefore: gate driving loss (E_{GD}) in (7), turn-off overlap loss ($E_{\text{OFF,overlap}}$) in (8), and reverse diode conduction loss during excess dead time period. Among these, turn-off overlap loss is the hardest to calculate due to the nonlinear output capacitance of the switches. In (8), T_{cf} corresponds to the channel current fall time which can be approximated by $Q_{\text{GS}}/I_{\text{G,cf}}$ (average gate current during the switching transition). The turn-off overlap discussed here is the transition from high-side switch to low-side switch and $I_{\text{L,OFF}}$ is the inductor current value at this transition.

$$I_{\text{HS,rms}} = I_{\text{L,rms}} \cdot \sqrt{D} \quad (5)$$

$$I_{\text{LS,rms}} = I_{\text{L,rms}} \cdot \sqrt{1-D} \quad (6)$$

$$E_{\text{GD}} = (V_{\text{drv,ON}} - V_{\text{drv,OFF}}) \cdot Q_{\text{G}} \quad (7)$$

$$E_{\text{OFF,overlap}} = \frac{1}{12} \cdot \frac{(T_{\text{cf}} \cdot I_{\text{L,OFF}})^2}{C_{\text{OSS,HS}}(0) + C_{\text{OSS,LS}}(V_{\text{BUS}})} \quad (8)$$

C. Inductor Losses

The losses in inductor can be divided into core loss and winding loss. Core loss can be calculated using improved Generalized Steinmetz Equation ($i\text{GSE}$) [8], given the available Steinmetz parameter of the core material. When higher accuracy is necessary, $i^2\text{GSE}$ [9] can also be used. However, the second method requires dedicated core loss measurements. Thus, only $i\text{GSE}$ will be used in this work.

The winding loss is generally due to skin and proximity effects, which will escalate the AC resistance significantly. In high-frequency application, i.e. $f_{\text{sw}} \geq 1$ Mhz, the skin depth of copper is less than 70 μm . Therefore, foil winding or flat wire geometry is preferred such that performance does not suffer from skin effect. Proximity effect is known to have big impact in multi-turn foil winding structure [10]. Estimating the proximity effect impact requires a careful external magnetic field calculation on each wire. Since for ZVS-QSW buck converter operating in HF region, usually low inductance value is needed, it is possible to realize the inductor with only one turn. Hence, inter-winding proximity effect can be avoided. Proximity effect in the parallel conductor of the same winding will still occur and this is easier addressed using FEM simulation analysis to get a sense of the current distribution. When accounting only for skin effect, the total AC resistance can be calculated using (10) with h_{cu} and b_{cu} correspond to foil thickness and breadth, while δ is the foil material skin depth.

$$\nu = \frac{h_{\text{Cu}}}{\delta} \quad (9)$$

$$R_{\text{AC}} = 2 \cdot \frac{\nu}{4} \cdot \frac{\sinh \nu + \sin \nu}{\cosh \nu - \cos \nu} \cdot R_{\text{DC}} \quad (10)$$

III. DESIGN SELECTION

Loss analysis is performed on a buck converter with specifications listed in Table I. Switching frequency range is set to 1 - 3 MHz and the inductance value 70 - 90 % of the boundary value (to ensure enough negative current for ZVS). The inductance value at 80 % of the boundary value is presented in Fig. 1. Using the loss estimation considerations above, the trade-off between switching vs conduction and also between winding vs core losses will be investigated. Finally a design point will be selected and the prototype will be built to confirm the developed model.

TABLE I
CONVERTER SPECIFICATION

V_{in}	6, 9, 12 V
$V_{\text{out,nom}}$	4 V
I_{out}	5 A
f_{sw}	1 - 3 MHz

Fig. 1. Inductance limit to achieve ZVS at 80% L_{BCM}

A. Power Switch Selection

Power switch losses are estimated using the formulas presented in section II-B. Alternatively, one can use automatic loss calculation tool from [11], which should not deviate from section II-B since both are based on [7]. One important note here is that the diode conduction loss during dead time is eliminated. This assumption will be valid when the dead time is accurately adjusted such that the reverse diode conduction time is minimized.

From the specification defined in I, namely input voltage and output current, 3 switch candidates are selected: EPC2014, EPC2015, and EPC2100. The first two are a scaled version of each other. EPC2015 has 4 times the active area of EPC2014. EPC2100 is a half-bridge package with 2 different active areas for high-side and low-side. In this case, the low-side has about 4 times the area of the high-side. This model is attractive especially for applications with higher current through the low-side switch, i.e. when $D < 0.5$ in a buck converter. The loss analysis of the 3 switches is presented in Fig. 2 to 4 for 12 V input, 4 V 5 A output.

When comparing EPC2014 and EPC2015, we can see how this application favors power switch with bigger active area although it means lower utilization of the semiconductor. In theory EPC2014 would be sufficient, but high conduction losses make it's usage unfavorable. Looking at the EPC2100 performance, it can be seen that the conduction loss challenge in the low-side switch is answered. Though with higher gate driving losses this option offers a good combination of high-side and low-side switch. This results not only in lower loss, but also in smaller final assembly area. EPC2100 sizes $13.9mm^2$ while EPC2015 $13.1mm^2$, but when considering the connection for 2 x EPC2015 chips, the former clearly has an advantage. Therefore, considering all reasons above, EPC2100 will be a good choice for this application.

B. Inductor Design

The custom inductor design and dimensions are shown in Fig. 5. The core material is PC200 from TDK [5], which is supposed to offer good performance in 1 – 3 MHz range. The winding return path will be formed in the second PCB

Fig. 2. EPC2014 switch performance as a half-bridge

Fig. 3. EPC2015 switch performance as a half-bridge

which is put under the magnetic core. This will be clear in the next section where the final prototype is shown. This single-turn structure provides enough inductance for the specified application. Calculations by FEM software show that a single turn structure without air gap provides inductance of 715 nH. The inductance was then adjusted to the required 70-90 % of the boundary inductance by introducing air gap. This design is selected due to the availability of the magnetic core during prototype fabrication and the possibility to extend to 2 phase

Fig. 4. EPC2100 switch performance as a single chip half-bridge

Fig. 5. Magnetic core design and dimension

buck converter with self-balancing coupled inductor, similar to [12].

The inductor loss is estimated using methods explained in section II-C. The winding loss can be calculated based on the copper track parameters in Fig. 5 with copper thickness of 35 μm . The detailed proximity effect AC resistance calculation is omitted. Accurate core loss calculation is challenging, especially with the core geometry at hand. In this work the Steinmetz parameter in Tab. II will be used. The Steinmetz parameters are obtained from [13] where two additional parameters, f_{cr} and α_{cr} , are proposed to account for the increase in loss density at higher frequency. These parameters can also be found by curve fitting from manufacturer's data sheet. The use of these parameters in SE expression is presented in (11). From here, it is possible to extract α_{eff} for a given frequency resulting in the same loss density as in the traditional SE. Then, α_{eff} is used in $iGSE$ to calculate core loss. The results from this loss calculation are presented in Fig. 6 - 8.

$$P_V = K_c \cdot f^\alpha \cdot \hat{B}^\beta \cdot \left[1 + \left(\frac{f}{f_{cr}}\right)^{\alpha_{cr}}\right] \quad (11)$$

It can be seen that the winding loss does not depend much on switching frequency, but more on the current ripple value, which translates to higher current RMS value. This is sensible since the copper track thickness is lower than the skin depth. At 3 MHz, the skin depth is 37 μm .

The core loss dominates at higher input voltage, which can be explained by Fig. 9 where the AC peak flux density is plotted for different frequency and input voltage. Although $B_{AC,pk}$ reduces with higher switching frequency, the loss component due to α parameter increases. Therefore in the core loss graph we see points where it is minimized, that is when loss due to α and β reach optimal value. P_{fe} does not depend on the current ripple amplitude since we lock the core design (N and A_c), meaning that the flux density in the core only changes with frequency and input voltage. In the above, DC Bias effects, which might increase core loss significantly, were ignored.

IV. EXPERIMENTAL VALIDATION

A ZVS-QSW buck converter prototype was built to verify the model and method presented here. The prototype features

TABLE II
CORE MATERIAL STEINMETZ PARAMETER

K_c	0.021
α	1.83
β	2.98
α_{cr}	5.8
f_{cr}	2.5 MHz

*These parameters give P_V in W/m^3

Fig. 6. Inductor Loss at 6 V input and 3 A output

Fig. 7. Inductor Loss at 9 V input and 5 A output

Fig. 8. Inductor Loss at 12 V input and 5 A output

Fig. 9. AC Peak Flux Density at different input voltage and switching frequency

Fig. 10. Top view of the prototype and solution area size

the selected power switch and inductor design described in previous sections. Pictures of the prototype are shown in Fig. 10 and 11. With maximum output power of 20 W, this prototype achieves power density of 9.26 W/m^2 with thickness less than 5 mm. Switching frequency of 2 MHz was selected due to minimum predicted core losses at this frequency. The trade off is that ZVS operation will be lost at higher load. The inductor air-gap is adjusted such that inductance value of 70 - 80 % L_{BCM} is achieved. This is demonstrated in Fig. 12 where the current slope reflects inductance value of around 80 nH, which is enough to achieve ZVS at 5A output with 12V and 9V input, but not for 6V input, as will be shown in the following section.

Fig. 11. Side view of the prototype and solution thickness

Fig. 12. Waveform of inductor current (red), switch node voltage (yellow), and output voltage (green) at 6 V input and 0A load

Fig. 13. Full ZVS operation at 12 V input 5.2 A output and 33% duty cycle

A. ZVS Operation

The next verification step is to see if the ZVS operation of high side switch is achieved. The low side can usually achieve ZVS due to the nature of buck topology. The high side ZVS operation can be observed from Fig. 13 - 15. At 9V and 12V input, inductor current ripple is big enough such that at high output current the negative inductor current is still enough to discharge $C_{oss,HS}$ before it's turned on by the gate source voltage. This can be observed in Fig. 13 and 14 where v_{sw} rises to the input voltage, making $v_{ds,HS}$ zero, before $v_{gs,HS}$ reaches the threshold voltage. The situation for 6 V input, as shown in Fig. 15 is different. The negative inductor current is not sufficient to fully discharge $C_{oss,HS}$ before $v_{gs,HS}$ reaches the threshold voltage, resulting in an incomplete ZVS and increased switching loss [14].

B. Performance Evaluation

As final step, converter performance is recorded for 2 MHz switching frequency with inductance value of around 80 nH after adding air gap to the inductor. Due to unavailability of

Fig. 14. Full ZVS operation at 9 V input 4.7 A output and 44% duty cycle

Fig. 15. Incomplete ZVS operation at 6 V input 3.5 A output and 67% duty cycle

EPC2100 device during the work of this testing, EPC2101 device is used instead, which has higher $R_{ds,on}$ and double the rated maximum voltage. This replacement leads to increased semiconductor loss, but should not be significant to the total system efficiency.

The measurement results are presented in Fig. 16 as efficiency plot, and in Fig. 17 as total loss plot. The converter can maintain efficiency higher than 90% at output power higher than 10 W and 6 - 9 V input voltage. From the converter loss measurement, it can be seen that at 6 V input, P_{loss} increases almost in quadratic fashion as P_{out} increases. This may be caused by dominating conduction loss, either from AC winding resistance or switch $R_{ds,on}$. From 6 V to 9 V input, there is a big jump in P_{loss} . This can be caused by dramatically increased P_{fe} , due to B_{peak} exceeding the 50 mT limit recommended in the datasheet [5]. In this case, the significance of conduction loss is still visible, though not as strong as before. In 12 V input case, core loss still dominates and P_{loss} increases almost linearly with output power until

Fig. 16. Converter efficiency at 2 Mhz switching frequency

ZVS is lost.

An interesting phenomena is seen when P_{loss} at 12 V input slightly decreases around 5 W output range. This can be explained by the decreasing body diode loss. As P_{out} increases, the body diode conduction time during dead time between 2 switches decreases, thus leading to decreased loss. This effect is counter acting the increasing conduction loss and if it has bigger share, P_{loss} will decrease slightly at a certain power range.

The converter was also tested at 2.25 MHz, a little higher frequency. The measured converter loss is given in Fig. 18. It can be seen that the base line loss (loss at very low load) is reduced at higher frequency. This can be caused by the smaller flux density amplitude in the core. There is around 10% loss reduction at 12 V input. However, this gain is opposed by the loss of ZVS at higher load, as can be seen by the change in the loss line gradient. Therefore, a trade off situation is faced.

Another highlight to mention here is how the calculated loss is in the same range as the measured one. Taking 12 V input and 5 A output at 2 MHz as an example, the measured loss is around 2 W with the approximate loss distribution presented in Fig. 19. From calculation result in section III-A, there is about 0.5 W loss from semiconductor, and from III-B, there is about 0.75 W core loss and 0.25 W copper loss. Higher measured loss is expected since the power switch used in testing is slightly different. Moreover, higher winding loss can occur due to the proximity effect in parallel conductor in PCB, which is not accounted for in this paper. This effect may increase winding AC resistance significantly. ESR loss from the installed capacitor also contributes to the total loss.

V. CONCLUSION

From above discussion, model and design considerations presented can be regarded valid to the extent that the calculated loss lies in the same range (20 % error) as the measured one. The deviation of predicted and measured losses can be explained by: ignored proximity effect in winding, inaccurate core loss parameter, esp. when $B_{AC,pk}$ is higher than 50 mT,

Fig. 17. Converter total loss at 2 Mhz switching frequency

Fig. 18. Converter total loss at 2.25 Mhz switching frequency

Fig. 19. Converter loss distribution at 12 V input and 4 V 5 A output with 2 MHz switching frequency

and a different power device. It can be concluded that the new asymmetrical single chip GaN device together with HF MnZn core material have extended the path to a more integrated, high power density step down converter, although high efficiency is still a challenge.

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