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Switching Performance in a GaN Power Stage at Extreme Temperature Conditions

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Abstract—Exposure to an extreme ambient temperature leads to increased losses in a Gallium Nitride Field Effect Transistor (GaN-FET) when operating in a switch-mode power stage. The output capacitance of Gallium Nitride (GaN) devices is decreased at higher voltages but increased at higher temperatures. This paper highlights the effect of output capacitance in a half-bridge switching stage and offers analysis towards the switching losses. A power stage was built and tested with two timing optimizations: for room temperature and high temperature, respectively. Trading off dead time and the loss mechanisms involved, a loss reduction of 16.1% was achieved. This loss reduction was further improved to 26.1% after thorough investigation of the switch node transient responses.

Index Terms—GaN-FET; High Temperature; Switching losses

High frequency switch mode applications have become the industry standard for power conversion circuits. Higher switching speeds in converters allow a designer to drastically decrease the size of their converters, mostly by downsizing required filter components. Downsizing allows packing components in a confined space [1], [2]. The increase of switching frequencies is aided by the introduction of wide-bandgap materials in transistor switching devices [3].

In relation to higher switching frequencies and smaller power supplies, operating temperatures see an elevation. Generated heat is harder to dissipate into smaller heatsinks, if heatsinks are used at all. It becomes challenging to operate switching devices within temperature boundaries in a small dimensioned power stage. Smaller packed converters do not allow large heatsinks, which leads to a higher temperature difference (ΔT) between junction temperature and ambient temperature. When ambient temperature is increased, the acceptable temperature difference in the converter becomes very small to allow for operational self-heating.

Employing GaN-FETs in high to extreme temperature conditions requires a thorough understanding of loss mechanisms. As ambient temperatures rise, the temperature headroom is decreased. In conventional electronics design, a maximum junction temperature of 150 °C is considered a rule of thumb.

When ambient temperatures rise above this level, a high degree of understanding of the parasitic loss mechanisms is required.

Gallium Nitride Field Effect Transistors (GaN-FETs) parasitic parameters in extreme temperatures have previously been investigated [4], [5]. It was shown that parasitic loss mechanisms have an increased exposure towards potential losses in temperatures up to 225 °C. GaN-FETs have been used under these extreme conditions in a low power application capable of operating in 200 °C [6]. Hu et al. [7] have shown a 10 W fly-back converter operating at 110 °C equipped with GaN-FETs.

This paper aims to create an understanding of the switching stage behaviour and different loss mechanisms in a GaN-FET equipped power stage under extreme ambient temperatures up to 200 °C. Switching losses and characteristics are highly dependent on the timing of the gate driving signals, which can be altered to tune the performance for elevated temperatures. An application specific timing can aid a converters performance, reliability and life time [8]. When gate signals are properly timed, the switching transition losses can be minimized. Exact timing in a power stage with output filter results in zero voltage switching (ZVS), where the switching losses approach to 0 W.

After this section, the theory of importance towards switching timing in high temperatures is presented in Section I. In Section II, a trade-off in application specific timing strategies is made. Section III presents the methods used to verify of the presented theory after which the results are presented in Section IV. The paper is finalized by summarizing the conclusions in Section V.

I. SWITCHING TIMING

Output capacitances (C_{OSS}) of the used switches in a half bridge (Fig. 1) form the most important parameter to investigate and optimize switching losses. Switching losses are a combination of output capacitance P_{COSS} losses and switching transient losses P_{TR} , where P_{COSS} is dependent on

Fig. 1. Schematic of the half bridge power stage under test

the drain to source voltage V_{DS} at the moment of switching (2).

$$P_{TR} = \frac{1}{2} I_D \cdot V_{DS} \quad (1)$$

$$P_{COSS} = \frac{1}{2} \cdot C_{OSS}(V_{DS}) \cdot V_{DS}^2 \quad (2)$$

$$P_{SW} = P_{TR} + P_{COSS} \quad (3)$$

Since there are two devices in the switch node, the actual switch node capacitance is the sum of the parasitics ($C_{OSS-HS} + C_{OSS-LS}$). Both capacitances depend on the voltage present in the switch node. As one switch sees an increasing voltage across drain to source and the other a decreasing, the sum of the two capacitances as function of the voltage is plotted in Fig. 2 [5], [9]. As C_{OSS} becomes larger at low voltages for higher temperatures, the total capacitance in the node increases. A dip can be observed in ambient or room temperatures (RT) of 25 °C as C_{OSS} decreases with V_{DS} on one GaN-FET as it increases on the other. At 175 °C the total capacitance is rather flat for the full switch node voltage swing, whereas at high temperature (HT) of 200 °C a peak is observed at the mid point of the voltage swing.

With the changing capacitance in the switching node versus temperature and voltage, timing of the two switches in the half bridge is crucial to minimize losses. The dead time (t_d) allows for charging and discharging of C_{SW} and ZVS can be reached when the remaining voltage is 0 V. The charging and discharging current is set by the ripple current in the output filter inductor L_F . At the switching transients, the ripple current peaks at $\hat{I}_L$.

In room temperature the capacitance is much lower than in high temperature. Therefore, at high temperature, it can

Fig. 2. Total switch node capacitance versus switch node voltage V_{DS}

be expected that a switch node will have a remaining charge in the switching devices at the moment of switching. This results in hard switching transients where losses are increased. The exact losses are depended on the switching frequency but are exponentially increasing with leftover V_{SW} . Combined with the decreasing ΔT headroom as ambient temperature is increased, precise timing in the circuit design is paramount.

II. APPLICATION SPECIFIC DESIGN

The switch node behaviour at various temperatures can be analyzed using Fig. 2. The dip in C_{OSS} at ambient temperatures, seen around the mid point of the switching node voltage swing, means that the derivative of the voltage during the transients is increased at that point. On the contrary, for high temperatures, the peak at the midpoint of the voltage swing will cause the switch node to act slower and decrease the derivative (4).

$$\frac{\delta V}{\delta t} = \frac{C_{OSS}}{I_d} \quad (4)$$

The decrease in derivative means that the complete voltage swing takes longer and therefore a longer dead time may be required. On the other side, when using a longer dead time, reverse conduction occurs at room temperatures because the switching transients voltage swing takes a shorter amount of time. This leads to a trade off where additional losses due to reverse conduction may be allowed at low temperatures because the headroom (ΔT) is larger. The reverse conduction current is equal to the peak of the ripple current ($\hat{I}_L$) as set by the used inductor used in the output filter circuit.

It must be noted that GaN-FETs do not have a reverse recovery charge, hence this loss mechanism can be neglected. Although reverse recovery charge is neglected, $\hat{I}_L$ charges C_{OSS} dependent on the reverse conduction voltage drop V_{SD} . When the GaN-FET is then turned on, this capacitance is shorted by the GaN-FET channel and dissipated in the device. Normally V_{SD} is small, which means this loss mechanism can be neglected.

By extending the dead time in a half bridge power stage and using the reverse conduction path of the GaN-FET, switching losses can be calculated. It is assumed that the switching transients are fast in respect to the switching cycle, meaning that the inductor current I_L can be assumed constant during this period. From Fig. 2 the average capacitance in the switch node can be integrated for $C_{SW}(T = 25^\circ\text{C}) = 122\text{ pF}$ and $C_{SW}(T = 200^\circ\text{C}) = 133\text{ pF}$. This is an increase of 9.1%. Trough detailed design of the PCB any additional capacitance in the switch node is kept to a minimum.

III. METHODS

The circuit from Fig. 1 is build and tested in a temperature chamber. A digital multi meter is placed in series with the power supply input at 50 V and an oscilloscope is used to analyze the waveforms in the switch node. Due to the small dimensions of the used circuit, it can be assumed the thermal constant is low. The temperature chamber is heated to temperatures of 25, 100, 150, 175 and 200 °C after which a 15 minute settling time is maintained. The temperature dependent loss mechanisms impact the input current of the circuit, therefore data is retrieved when the current measurement shows a stable outcome.

The data of interest is foremost the switch node behaviour. By measuring the switch node one can analyze the derivative of the voltage swing and relate this to the node capacitance using (4). It is expected that the shape of this response is inverse proportional to the shape of the capacitance versus node voltage.

The circuit will be driven by a gate driver which is controlled by a waveform generator. Two outputs of the waveform generator are used to create independent pulse signals of 2.5 MHz for both the high side GaN-FET and the low side GaN-FET. Doing so, the dead time can be precisely timed between a room temperature performance setting and a high temperature optimized setting. For room temperature a dead time of 18 ns was used as for high temperature optimization the dead time was approximately doubled to 35 ns.

Temperature dependent additional losses can be investigated by analyzing the input current. It is expected that the input current will increase when temperatures are increased. The power stage is running at a fixed frequency with the inductor placed outside of the thermal chamber, omitting temperature effects in the core material. This way the ripple current in the inductor remains constant, therefore performance analysis of the switch nodes can be easily be compared. The additional effect of output capacitance losses becomes clear as a difference between the two settings.

IV. MEASUREMENTS

The aforementioned methods are implemented on a half bridge circuit prototype. Due to the nature of the analysis, an AC coupling was preferred on the oscilloscope settings. For the clarity of the plots of measured responses, only the waveforms at 25, 175 and 200 °C are plotted. It was found

that results measured at 100 °C and 200 °C fell between the boundaries set by the presented data as in this paper.

Fig. 3 shows the full switching cycle measured for a traditional room temperature optimized circuit. The waveforms show that a small deviation in the switch node can be observed. Also, from the current measurement if I_L in the bottom plot, it can be seen that the current in the switching transient stays approximate equal.

Fig. 3. Switching period at room temperature optimized dead time.

From Fig. 3 it became clear that both the falling and rising edges of the switching cycle need further investigation as are respectively plotted in Fig. 4 and Fig. 5.

Fig. 4. Falling edge at room temperature optimized dead time.

During the falling edge, a clear deviation in the switching slope becomes present when temperatures are increased. The higher capacitance in the switch node causes the voltage swing to take longer, hence with the short dead time setting the power stage enters a hard switching transient at these temperatures.

In the rising edge transient depicted in Fig. 5 a similar effect can be observed. However, in this case the hard switching

Fig. 5. Rising edge at room temperature optimized dead time.

effect does not necessarily originates from the output capacitance. The turn on of the GaN-FET seem to appear earlier than expected. This could be due to a faster propagation time in the gate driver at high temperatures or the lower gate threshold voltage in the GaN-FET at high temperatures [5]. Both the rising and falling hard switching transients at high temperatures increase the the losses, which is unwanted under such conditions.

High temperature optimized dead time shows a similar waveform when investigating a full switching cycle depicted in Fig. 6. It does not seem there are any disturbances in the waveform timing, but when looking closely a reverse conduction period can be observed. This will become more appear ant in the following falling and rising edge plots.

Fig. 6. Switching period at high temperature optimized dead time.

Fig. 7 shows the switching waveform of the falling edge in the half bridge power stage, where Fig. 8 shows the rising slope. For the blue 25 °C traces in the plots, a clear

reverse conduction time interval can be observed from approx. 18 – 35 ns. This emphasizes the absence of a hard switching transient, therefore aiding a lower loss. Following (2), the voltage squared dominated losses are much lower as $V_{SD} \ll V_{SW}$ at the moment of switching.

Fig. 7. Falling edge at high temperature optimized dead time.

Fig. 8. Rising edge at high temperature optimized dead time.

In Fig. 9 one can observe incremental losses versus increasing temperature for both dead time settings. The blue trace shows the idle losses for the room temperature optimized dead time of 18 ns, where the red trace plots the idle losses for the high temperature optimized dead time of 35 ns. A clear advantage at 25 °C for the shorter dead time. The lower total switch node capacitance allows for ZVS and therefore idle losses are 6.7% lower than for the longer high temperature optimized dead time.

Towards higher temperatures a cross over point can be observed around 120 °C. For temperatures higher than this cross over point, idle losses are lower using an high temperature

Fig. 9. Idle losses versus temperature.

optimized dead time of 35 ns. At 200 °C a reduction of losses of 16.1% was achieved compared to the a deadtime of 18 ns. Upon investigation of the switching transients from Fig. 7 and 8, the estimation was made that a dead time of approx. 25 ns would result in the lowest losses at 200 °C. After fine tuning by increasing dead time in 1 ns steps the optimal timing was found at 27 ns. This setting resulted in a total loss reduction of 26.7% compared to a room temperature dead time setting in idle operation.

V. CONCLUSION

Investigation in a half bridge switching stage at various temperatures is conducted and presented in this paper. The theory of a higher capacitance in the switch node at high temperatures is verified. Where the node capacitance peaks at the midpoint of the complete voltage swing, the switching transient is slowed down. This causes the switch node to act slower that has an impact on the losses. Two different timing regimes show that a high temperature optimization can decrease idle losses by 16.1%, and when precisely matches a reduction of 26.1% was achieved. High temperature optimized timing utilizes the reverse conduction path in GaN-FETs, which show a rather preferred use compared to hard switching transients.

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