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Directional Nanoscale Silicon Etching using SF_6 and O_2 Plasma

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To my beloved family

Preface

During the past three years, I have had great opportunities to meet and work with many wonderful people who directly or indirectly influenced me to become what I am today. This is a special moment for me to look back and express my gratitude to all of them.

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Kongens Lyngby, November 30th 2020
Vy Thi Hoang Nguyen

Abstract

Plasma etching is important to realize fine geometry for the fabrication of silicon nanostructures. The Bosch process is probably the most popular technique in the nanofabrication industries today. However, the high roughness with finite sidewall scallop size and hard to remove fluorocarbon residue on the sidewalls of etched structures make the process less favorable for nanoscale engineering. This PhD project focuses on the development of a reliable and stable technology for nanoscale silicon plasma etching which addresses both issues. The specific contributions of this thesis are summarized below.

First, a fluorocarbon-free directional silicon etching procedure called CORE (stands for Clear, Oxidize, Remove, and Etch) has been developed in which a switching sequence of SF_6 and O_2 is operated at room temperature. Compared to other etch processes, the CORE sequence has the advantage of precise profile control, high selectivity, small sidewall roughness and flexible process programming. It also shows an excellent performance in nanoscale structures with an accurate and controllable etch rate between 1 and 50nm/min (and SiO_2-selectivity of ca. 35) using the etch-tool in the RIE-mode. By adding the ICP source (DRIE-mode), a directional etch rate up to 1µm/min and selectivity >200 for SiO_2 is possible.

Second, the formation of black silicon (BSi) in SF_6/O_2 plasma has been investigated based on the CORE sequence. By manipulating its parameters and utilizing the self-limiting property of the oxidation step, the CORE sequence can easily be modified to create either BSi-full or BSi-free surfaces independent of the aspect ratio of the etch features. The latter distinguishes the BSi formation clearly from other directional processes, thus provides a versatile tool for creating BSi anywhere at anytime, as it is called ‘BSi on Demand’.

Third, the performance of the CORE sequence has been demonstrated to fabricate ultra-high aspect ratio (HAR) nanofeatures. The effect of different CORE parameters on the etch rate and profile are investigated and optimized with respect to low mask undercut and high directionality (vertical) etch. The nanopillar arrays (200nm diameter, 400nm pitch and 60nm diameter, 500nm pitch) have smooth straight sidewalls with aspect ratios beyond 55 for gaps and up to 200 for pillars. Due to the very mild plasma condition (less than 40W RIE power), the mask selectivity can be tuned above 500.

Finally, a procedure for Cr etching using SF_6 and O_2 plasma has been demonstrated for the first time. The etch mechanism is explained by considering the formation of volatile chromyl fluoride in which the Cr is first reacting with oxygen radicals and the formed CrO_x subsequently reacts with fluorine radicals into CrO_2F_2. For the mixed mode, the proposed etch procedure performs at 300W plasma power with etch rates of Cr up to

150nm/min for a SF_6/O_2 gas ratio below 1%. For the switched mode, the etch rate is around 7nm/min with high selectivity with respect to silicon (> 20) and better profile control.

Resumé

Plasmaætsning er en vigtig metode til realisering af højt opløste geometriske emner ved fremstilling af nanostrukturer i silicium. Den såkaldte Bosch proces er formentlig den mest fremherskende teknik indenfor nanofabrikations-industrien i dag. I denne forbindelse er den høje ruhed som følge af korrugerede sidevægge, såkaldte "scallops", og rester af fluorcarbon-baserede forbindelser, problemer, som gør Bosch-processen mindre favorabel indenfor nanoskala fremstillingsmetoder. Det foreliggende PhD projekt omhandler udviklingen af en pålidelig og stabil nanoskala plasmaætsnings-teknologi i silicium, som adresserer begge problemstillinger. De specifikke bidrag fra denne afhandling er opsummeret i det følgende.

For det første er en fluorcarbon-fri retningsbestemt siliciumæts-procedure kaldet CORE (forkortelse af de engelske udtryk Clear, Oxidize, Remove og Etch) blevet udviklet, i hvilken alternerende sekvenser af SF_6 and O_2 benyttes ved stuetemperatur. Sammenlignet med andre ætseprocesser har CORE processen fordele ved præcis profilkontrol, høj selektivitet, lav sidevægsruhed og fleksibel procesprogrammering. Den demonstrerer ligeledes fremragende resultater for nanoskala strukturer med nøjagtige og kontrollerbare ætserater mellem 1 og 50 nm/min (og en SiO_2-selektivitet på ca. 35) ved brug af ætseudstyret i RIE-tilstand. Når ICP-kilden tilføjes (DRIE-tilstand) er det muligt at opnå en retningsbestemt æts med ætserate op til 1µm/min og selektivitet >200 for SiO_2.

For det andet er dannelse af "sort silicium" (engelsk: black silicon (BSi)) ved ætsning i et SF_6/O_2 plasma, baseret på CORE-sekvensen, blevet undersøgt. Ved justering af dens parametre og udnyttelse af den selvbegrænsende egenskab af oxidationssteppet kan CORE-sekvensen let modificeres til enten at frembringe hele BSi overflader eller BSi-fri overflader uafhængigt af aspektforholdet for de ætsede strukturer. Denne egenskab adskiller dannelsen af BSi klart fra andre retningsbestemte ætseprocesser og giver dermed et alsidigt værktøj til fremstilling af BSi "hvor som helst" til "ethvert tidspunkt" og derfor betegnelsen "BSi efter behov".

For det tredie er det med CORE-sekvensen blevet demonstreret muligt at frembringe nanostrukturer med ultra-højt aspektforhold. Effekten af forskellige CORE-parametre på ætserate og ætseprofil er blevet undersøgt og optimeret med henblik på minimering af maske-undersæts og forbedring af retningsbestemt (vertikal) æts. Rækker af ætsede nanosøjler (200nm diameter, 400nm repetitionsafstand og 60nm diameter, 500nm repetitionsafstand) fremviser glatte, rette sidevægge med aspektforhold mellem 55 for huller og op til 200 for søjler. På grund af de meget milde plasma betingelser (mindre end 40 W RIE effekt) kan maskeselektiviteten justeres til over 500.

Endelig er der for første gang demonstreret en procedure for Cr-ætsning baseret på et SF_6 og O_2 plasma. Ætsemekanismen forklares ud fra dannelsen af chromylfluorid, hvor Cr indledningsvis reagerer med O-radikaler, hvorefter den dannede CrO_x reagerer med F-radikaler, hvilket resulterer i CrO_2F_2. Ved "mixed mode" kørsel med 300 W plasmaeffekt resulterer den foreslåede ætseprocedure i Cr ætserater op til 150nm/min for et SF_6/O_2 gasforhold mindre end 1%. Ved "switched mode" kørsel er ætseraten omkring 7nm/min med høj selektivitet i forhold til silicium (> 20) og med bedre profilkontrol.

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Chapter 1. Introduction

1.1. Background and motivation

Advances in the semiconductor industry in recent years has been attributed to the development of very large scale integration (VLSI) technology in which various functional devices are built into a small chip size with improved performance. Many VLSI devices such as microprocessors, central process unit (CPU), dynamic random access memory (DRAM), etc. are growing quickly with the device density continue to double approximately every 2 years following the exponential growth of Moore's law[1]. In addition to density increases, the device scaling also plays an important role in the development of VLSI technology. It is estimated that the minimum feature size of the VLSI devices has been shrunk down approximately by 30% every 2-3 years, and a process that enables 3nm feature size has been established in 2020 by IMEC (Leuven, Belgium) and ASML (Veldhoven, Netherlands)[2-4].

To realize a high VLSI device density, it requires a large number of devices integrated into a single chip and an effective approach is to make each device as small as possible. The key for achieving this is based on fine geometry processing which is comprised of three basic pillars – deposition, lithography and etching – placed in an arbitrary adaptable sequence of process steps to create the requested devices. Until recently, focus has been directed to upgrade the lithographic tools to decrease the lateral resolution. Following the development of photolithography, etching technologies have also participated in the race towards smaller dimensions and high density. With the lithographic tools pushing the critical dimension further down and the improvement of etch tools/recipes, the dimensions of micro electromechanical systems (MEMS) devices are rapidly decreasing and commercial nano electromechanical systems (NEMS) are underway.

The scaling down scenario in the semiconductor industry, however, is about to reach its limitations because of the technical challenge in improving device performance and power assumption at the shrinking size. To overcome this barrier, the VLSI technology is forced to further evolve and a lot of research study is focusing on the replacement of conventional planar devices by nonplanar structures to enable the increasing of device

density or functionality per cubic centimeter. In 2007, Tanaka et al. proposed a three-dimensional (3D) gate stack NAND flash memory consists of stacked layers of poly-Si and the insulating film one after the other to increase the device density[5]. This 3D structure is called bit-cost scalable (BiCS) flash memory and is promising for ultrahigh density memory. A similar transition from planar to 3D devices can also be observed in logic transistors such as fin field-effect transistor (FinFET) that results in the development of a vertical transistor with a gate-all-around (GAA) structure[6,7]. These complex structures create stringent technical challenge on the fabrication technologies. For example, fabrication of 3D gate stacks requires an etching technology capable of opening high aspect ratio holes in a single step through all the stacked layers. Etching technology is also important in the fabrication of through-silicon vias (TSVs) for chip-to-chip connections in the 3D integrated circuits[8,9]. Large cavities are etched for subsequent chips or wafer scale packaging and sensor structures may comprise multi-wafer stacks with one or more having through wafer etches. Therefore, the etching technology needs to be developed for high speed etching with excellent profile control but still able to offer low rate for etching thin gate film.

In the early days of integrated circuits processing, the etching technology was mainly based on wet chemicals to transfer the lithographic patterns into the target film. In 1970s, plasma etching was introduced and quickly replaced wet etching to become the mainstream etching technology in semiconductor industry[10,11]. During the plasma process, gas species (e.g. SF_6, CHF_3, O_2, etc.) are injected into a vacuum chamber and ionized (by radio frequency, microwave, etc.) to generate the etching chemistry consisting of reactive radicals, electrons and ions with high energy. The use of plasma to clean or transfer patterns was motivated primarily by the need to reduce the chemical waste associated with the use of wet etchants. However, other advantages of plasma etching later became more apparent such as the possibility to create highly anisotropic profiles without depending on the crystal orientation and the ability to achieve high aspect ratio structures.

The development of plasma etching for patterning semiconductor devices has evolved along two main paths: physical (sputtering) and chemical etching. Each path has different fabrication mechanisms and goals. The sputtering method is needed when there is no chemical etchants available to etch a specific substrate materials or when the patterning could not be easily accomplished by wet etching. For example, in the fabrication process of beam-leads devices, it is hardly possible to use chemical etchants to etch the platinum and titanium below the gold layer because the chemicals used to etch platinum (e.g. aqua regia) can etch the gold much faster[12]. Therefore in this case, the devices patterning is carried out only by utilizing an energetic ion flux to physically sputtering the platinum layer[13,14]. The typical sputtering equipment uses a blocking capacitor to couple a radio frequency (RF) generator to the electrode on which the substrate has been placed[15]. With this configuration, a negative bias is produced on the wafer electrode and the energetic ions will be accelerate toward this bias electrode to bombard the substrate. The sputtering

method has a disadvantage of redeposition of materials that results in the positively tapered etch profiles with low selectivity and low etch rates[16,17]. The second path, the chemical plasma etching, is intended to use as an alternative of wet etching in the fabrication of integrated circuits. It is characterized by the minimal ion bombardment and purely chemical etching. The chemical plasma etching started when Stephen Irving demonstrated the ability of using oxygen plasma to strip photoresist and later on recognized the possibility of using either fluorine or chlorine-based compounds for etching other materials (e.g. SiO_2 or aluminum)[18,19]. A classical reactor type for chemical plasma etching is the barrel in which wafers were placed in a quartz chamber with external electrodes[20]. A RF generator is applied across the electrodes to create the plasma when the appropriate gas is introduced into the chamber. This configuration is adequate for resist stripping but suffers from poor etch uniformity which is important for the device processing. In a further development, a parallel plate reactor is introduced in which the wafers are placed on the ground electrodes while RF is applied to the opposite one[21]. This approach gives high etch rates and selectivity but with an isotropic etch profiles.

These two paths in plasma etching converged when Hosokawa et al. introduced fluorine and chlorine-based gases (e.g. CF_4, CCl_2F_2, CCl_3F, etc.) into a RF sputtering apparatus in order to enhance the etching rate of various materials[22]. This innovated technique, now called reactive ion etching (RIE) or ion enhanced plasma etching, has become the method of choice for pattering devices in the semiconductor industry[23]. Due to the combination of the physical sputtering and chemical activity of reactive radicals, it enables the achievement of profiles control with high etch rate and selectivity[24]. Depending on the gas chemistry, a wide range of materials such as silicon, silicon oxide, aluminum, chromium, etc… can be etched with a high level of fidelity making the fabrication of complex devices more practicable. In this thesis we will focus on the technical development in plasma etching of silicon as it is a favorable material in semiconductor industry with an appropriate bandgap (around 1.12eV), high refractive index (~ 3.88 at wavelength of 632nm) and other superior properties[25]. Silicon can be etched in the halogen based (e.g. fluorine, chlorine and bromine) plasma with the gas of choice depends on specific applications. In general, Cl- and Br-based plasma are primarily used to achieve anisotropic etch profiles while F-based plasmas are used for isotropic etching because of the spontaneous reaction of the F radicals with silicon[26]. The F-based plasmas also etch silicon faster than the Cl- or Br-based plasma. Therefore, for applications such as micromachining for MEMS devices or TSVs when larger depths or heights must be created in silicon, F-based plasmas are the better choice.

Although requirements for the etching performance may be different depends on specific devices and applications, there is still a standard criteria for a plasma etching process in which the etch profiles are expected to be anisotropic with minimize undercut and high etch rate. Since silicon is etched spontaneously in F-based plasmas causing in large undercut of the mask, different techniques has been developed to prevent this isotropic nature. Zhang et al. proposed a mixed process in which the etching gas SF_6 and the O_2

inhibitor gas are introduced into the chamber at the same time resulting in a reasonable directional etch profile with less undercutting[27]. However, this technique comes with a weak sidewall protection and the etch profiles are pattern dependent (e.g. smaller trenches generally show a more positive tapered profile than the wider ones[28]). In 1988, Tachi et al. demonstrated that the horizontal silicon etch rate can be reduced drastically by cooling the substrate to below -100ºC and highly anisotropic etch profiles can be obtained[29]. This is because at low temperature, the created silicon oxy fluoride (SiO_xF_y) products start to freeze at the surface, thus improves the sidewall protection. This method is commonly known as cryogenic etching and has been studied intensively in the past years[30-32]. However, the pattern dependency cannot be removed in this way and mixed mode etch recipes are typically highly design specific that requires cumbersome optimizations.

With the introduction of the patented 2-steps Bosch process in 1994, the switched etching of complicated structures gained popularity and becomes probably the most popular technique in MEMS production facilities today[33,34]. It uses a repeating sequence of plasma enhanced deposition to passivate silicon features, a physical etch for directional removal of this layer at the base of the features, and an isotropic etch for silicon removal at the cleared surfaces. The Bosch process creates prominent scallops, but it also forms nice directionality and the pattern dependency almost vanishes, which makes process optimization relatively easy. Moreover, it enables a better selectivity than mixed mode because bias is only applied during the etch step and not continuously. The Bosch process can be further improved by decoupling the bias from the etch step and forming the 3-steps process called DREM (Deposit, Remove, and Etch Many times)[35]. Compare with the traditional Bosch process, the DREM process has the advantage of higher etch selectivity, uniform sidewall roughness and better control of the etch process.

Although it is widely used, the switched process is not well suited to the nanoscale due to finite sidewall scallop size and undercut unless rate and selectivity are severely compromised. Typically it is not applied below 500nm trench feature sizes – although 200nm features have been demonstrated[35]. Transport effects 'down the etched cavity' limit rate and selectivity while aspect ratios, profile and passivation control are more challenging. For example, aspect ratios beyond 30 are rarely utilized and fluctuations in the results are common. Another RIE technique called atomic layer etching (ALE) has been proposed to etch silicon at nanoscale[36]. It uses chlorine-based plasma and exploit the self-limiting property of reaction between chlorine and silicon surface to create a monolayer of nonvolatile silicon chlorides ($SiCl_4$). This nonvolatile $SiCl_4$ monolayer then can be removed by a mild argon ion bombardment. The ALE technique claims to be able to control the etch depth in atomic resolution and transfer patterns with atomic-scale fidelity while maintaining both the material properties and feature dimensions[37]. However, the limited etch rate and low mask selectivity limit the flexibility of this technique for various application purposes.

Understanding the increasing demands and technical challenges in silicon etching at nanoscale, this PhD project aimed to develop a technology for nanoscale silicon plasma etching towards a reliable and sustainable solution which addresses these issues. The project objectives are presented in the next section.

1.2. Thesis objectives

In this project, the usability of SF_6 and O_2 plasma will be studied as a replacement for Bosch process to avoid fluorocarbon (FC) residue and facilitate the nanoscale silicon etching with profile control and sufficient mask selectivity preferably at room temperature. The aim is to get a fundamental understanding of the special challenges involved in etching silicon at nanoscale including the physics and chemistry involved. Based on this understanding, a reliable and sustainable technology for nanoscale silicon etching will be established for future application. Specific goals include:

- Develop a generic procedure for directional etching of silicon based on SF_6/O_2 plasma which is able to operate at room temperature to prevent thermal runaway. The etch profiles are required to be controllable (e.g. straight, positive or negative tapered) with minimized sidewall roughness and pattern independent. The developing etching procedure should perform excellent at nanoscale accuracy with a low etch rates but still be able to perform for microstructures without the need for further process optimization in between. In addition, it must be flexible in programming, tool friendly and clean to avoid the process drift causing severe effects on the overall throughput and reproducibility as in the Bosch process.
- Based on the established process for directional silicon etching, develop a procedure for the fabrication of ultra-high aspect ratio (HAR) nanostructures (> 100) with low mask undercut and high directionality. A further task is to find a mask material that have high selectivity towards silicon and then investigating the highest achievable aspect ratio using that material as a mask.
- Demonstrate the ability of the developed technology in fabrication of various structures for different applications such as black silicon on demand, tuning fork, spiral structures, 3D nanostructures, etc.

1.3. Thesis outline

This thesis consists of seven chapters with the main focuses of each chapter are described as below:

- Chapter 1 will introduce about the motivation and objection of the project.
- Chapter 2 will give a general introduction about plasma etching. In the first part, the plasma is presented with a general overview about its basic properties. There is also a discussion about the radio frequency (RF) discharge, ion sheath and the motion of ion in the sheath. The second part introduces plasma etching with the focus on plasma-

surface interaction and the difference in etching mechanism between isotropic and anisotropic etching. Parameters for characterization of the etch results such as the etch rate, loading effect, aspect ratio dependent etching (ARDE), selectivity, and etch profiles will also be described.

- Chapter 3 will present a study on the development of a fluorocarbon-free directional silicon etching procedure called CORE (standing for Clear, Oxidize, Remove, and Etch) in which a switching sequence of SF_6 and O_2 is operated at room temperature. The CORE process resembles the well-known SF_6-based Bosch process, but the usual C_4F_8 inhibitor is replaced by O_2 oxidation with a self-limiting characteristic. In this chapter, the effect of varying the time in each step on the etch profiles is carefully investigated. Based on the obtained results, the design rules of the CORE sequence are formulated for further optimization. Then other etching characters includes profile tuning, mask selectivity, 3D fabrication and microscale etching process will be presented sequentially. The last part of the chapter will discuss about the self-limiting property of the CORE sequence.
- Chapter 4 will present a study on the formation of black silicon (BSi) in SF_6/O_2 plasma. In this chapter, different sources that contribute to the formation of BSi are documented and explained. Then a method to prevent and control the onset of BSi is proposed based on the CORE sequence. Due to the self-limiting property of the oxidation step, the formation and controllability of BSi in the CORE sequence is different from how BSi presents itself in the FC-based sequences. The effect of different process parameters of the CORE sequence on the creation of masks and formation of BSi are carefully investigated. By manipulating these parameters, the ability to create either BSi-full or BSi-free surfaces independent of the aspect ratio of the etching features is feasible.
- Chapter 5 will present a procedure to fabricate ultra-HAR silicon pillars using chromium mask and the CORE sequence. In this chapter, the effect of different CORE parameters (e.g. O-time, R-power, and E-pressure) on the etch rate and profile are carefully investigated and optimized with respect to low mask undercut, smooth sidewall and high directionality. In addition to the CORE parameters, we also examine the effect of total etch time on the evolution of ultra-HAR silicon pillars. Then based on the gained knowhow, the CORE recipe is fine-tuned to get ultra-HAR features with straight and smooth sidewalls. Finally, the retraction of chromium mask in SF_6/O_2 plasma and the effect of carrier wafer on the etch rate will be discussed.
- Chapter 6 will present a procedure to etch Cr and CrO_x using SF_6 and O_2 plasma as an alternative of the conventional Cl_2+O_2 plasma. The etch mechanism is explained by considering the formation of volatile chromyl fluoride (CrO_2F_2) which sublimes readily at room temperature. First, the effect of different plasma parameters (SF_6/O_2 ratio, plasma power, gas flux, loading) on the Cr and CrO_x etch rate will be studied using non-patterned samples. These non-patterned samples are simply used to find

some quick indication on the overall etch rate performance without considering the selectivity or etch profile. Then based on this obtained information, the patterned samples will be etched with the optimized plasma settings using both mixed mode and switched mode of SF_6 and O_2 plasma. Finally, the Cr etch procedure will be combined with other established etch process to demonstrate a complete fabrication scheme of silicon nanostructures using Cr as a mask.

- Chapter 7 will summarize the thesis and present an outlook for future development.

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Chapter 2. Introduction of plasma etching

Plasma etching is an important technology in semiconductor industry to transfer patterns defined by lithography into a target material. In the first part of this chapter, the plasma is presented with a general overview on its basic properties. There is also a discussion about the radio frequency (RF) discharge, ion sheath and the motion of ions in the sheath. The second part introduces plasma etching with the focus on the plasma-surface interaction and the difference in etching mechanisms between isotropic and anisotropic etching. Parameters for characterization of the etch results such as etch rate, loading effect, aspect ratio dependent etching (ARDE), selectivity, and etch profiles will also be described.

2.1. Basics of plasmas

2.1.1. Plasma and collision process in a plasma

Plasma is the forth fundamental state of matter that contains freely moving charged particles (ions and electrons) in a gas volume and is therefore highly conductive. Consider a chamber filled with a gas. A gas is highly insulating but will always have a few freely moving electrons inside. When a power source is applied on the chamber electrodes, the generated electric field will accelerate these electrons towards the positively charged anode. Under the correct conditions, these electrons gain energy high enough to ionize gas and liberate additional electrons. These collisions create an ever-increasing number of free electrons (avalanche) while passing towards the anode and will generate a gas discharge or plasma. This mechanism is illustrated in Figure 2.1a. Important plasma characteristics are the electron density (n_e) and ion density (n_i) which are substantially equal to each other thus making a plasma electrically neutral from the macroscopic viewpoint.

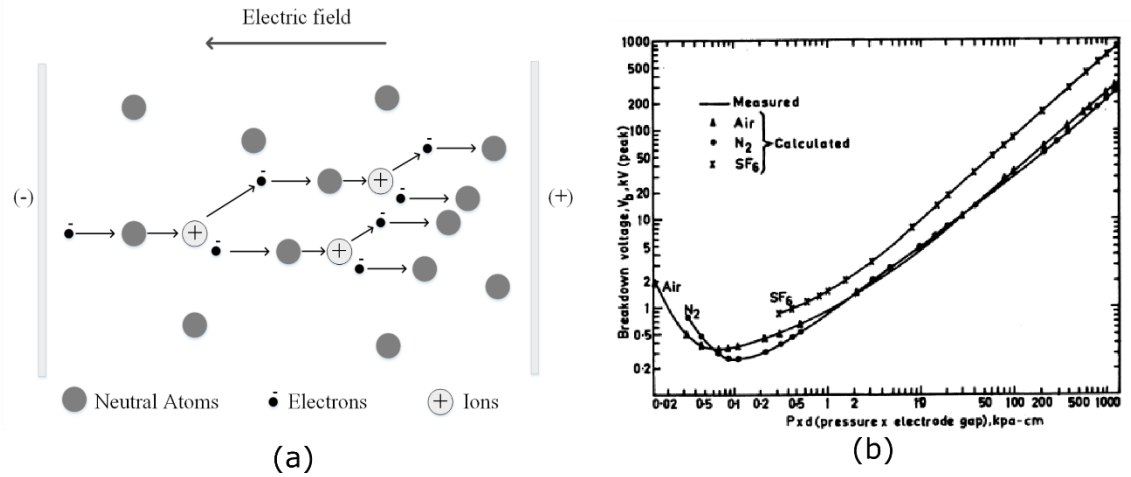

Figure 2.1. (a) Principle of a gas discharge. (b) The Paschen curve[1]

An important discharge property is the Paschen curve[1]. It shows the relationship between the minimum breakdown voltage needed to create plasma and the chamber pressure (calculated as the pressure ***p*** times the separated distance ***d*** between two electrodes). In Figure.2.1b, the breakdown voltage needed to create plasma has a minimum around 0.1kpa.cm ~ 0.7 Torr.cm. When the chamber pressure is too low, there are not enough collisions to cause avalanche while at the high chamber pressure, there is not enough RF energy gained by the accelerating electrons to cause ionization. This is why the plasma process needs to take place in a vacuum chamber with the pressure range between a few milliTorrs and a few hundreds of milliTorrs.

Plasma can be categorized into two main types: fully ionized plasma (referred to as arc discharge or high temperature plasma) and weakly ionized plasma (referred to as glow discharge or low temperature plasma). In this study, we only consider cold plasma as it is widely used in the semiconductor industry for etching materials. The degree of plasma ionization is defined as $\frac{n_i}{n_i+n_n}$, with n_i is the density of ions and n_n is the density of neutral species. Typically, a plasma used for etching has an ionized degree between 10^{-6} and 10^{-4}. This means that the majority of the particles remain neutral and only one ion/electron pair are generated out of every 10,000 neutral particles. In the standard plasma system such as a glow discharge or capacitively coupled plasma (CCP), the ion density is within a range of 10^9-10^{11} cm^{-3} whereas in an inductively coupled plasma (ICP) system, a higher ion density of 10^{12} cm^{-3} can be achieved[2].

In plasma, the collisions between moving electrons and atoms/molecules are categorized as elastic collision and inelastic collisions. With an elastic collision, only the kinetic energy changes while the internal energy remains unchanged. This type of collision tends to take place when the electron energy is low in between gas molecules. Assume a moving mass m_1 collides with a stationary mass m_2 at an angle α to the line joining the centers of

m_1 and m_2. The fractional energy E transferred from mass m_1 to mass m_2 can be derived by the conversation of linear momentum and energy[3]:

$$\frac{E_2}{E_1} = cos^2(\alpha)\frac{4m_1m_2}{(m_1+m_2)^2} \tag{2.1}$$

When $m_1 = m_2$ and the collision is frontal ($\alpha = 0$), this fraction has the maximum of 1. It means that mass m_2 gains an energy equal to that of mass m_1 and mass m_1 will lost all of its kinetic energy. This situation resembles the collision of billiard balls. In contrast, when an electron strikes a molecule, because the electron's mass is so much smaller than the molecule, the transfer function can be simplified as $4m_1/m_2$ ($\sim 10^{-5}$ for SF_6 molecules). Therefore, very little energy can be transferred from an electron to a molecule through an elastic collision. In plasma the more interesting collisions are inelastic, where the internal energy a struck molecule gains can be calculated as:

$$\frac{\Delta U}{E_1} = cos^2(\alpha)\frac{m_2}{m_1+m_2} \tag{2.2}$$

So, whereas the elastic energy transfer from an electron to a SF_6 molecule is close to 0%, this may rise to near 100% by inelastic collision. Consequently, electrons driven by the RF generator will lose their kinetic energy mostly by the inelastic collisions and will only slightly raise the gas temperature. This is why they are frequently referred to as cold plasma. Some of the typical collisions processes in plasma are described as below:

- Excitation and relaxation: In the excitation process, a moving electron that collides with an atom will transfer its kinetic energy to the bound electron in the atom and enables this electron to jump to a higher energy level. The excited electron stays at high level for a short time and then falls back to the ground state. This relaxation will emit a photon and create the plasma glow. A general excitation process can be described as $A + e \rightarrow A^* + e \rightarrow A + e + h\nu$, in which A denotes a neutral atom, A^* denotes A at the excited state, h is the Planck's constant and ν is the frequency of the emitted light.
- Dissociation: If the kinetic energy of the colliding electron is higher than the binding energy of the molecule, the dissociation process may occur. This reaction process can be described as $AB + e \rightarrow A + B + e$. The dissociation process will create highly active species called radicals that will contribute to the enhancement of chemical activities. For example, in SF_6 plasma, the fluorine radical produced after dissociation will etch silicon spontaneously.
- Ionization: The process in which a primary electron removes an electron from an atom, producing a positive ion and an extra electron is called electron impact ionization. The reaction process can be described as $A + e \rightarrow A^+ + 2e$. The prime feature of discharges is its conductance due to ionization, with perhaps as many as 10^{18} electron-ion pairs being produced per second.

- Attachment: There is a possibility that a low energetic electron colliding with an atom may join the atom and turn it into a negative ion. This process is known as electron attachment. The reaction process can be described as $A + e \rightarrow A^-$. The noble gases already have the outer shell filled with electrons, thus have little or no probability to form negative ions. However, halogen atoms (e.g. F, Cl, and Br) have an unfilled state in their outer shells, thus have high electron affinity to form negative ions.

2.1.2. Plasma parameters

The energy of a particle is related to its temperature. For gases the colliding particles will have the same temperature and thus thermal energy, irrespective their size. In contrast, in plasma there exists a lack of thermal equilibrium between the various particles. This is due to the difference in the kinetic energy gained by these particles under the applied electric field. Because electrons have a much smaller mass compared to ions or molecules, they will move faster and thus gain larger kinetic energy. The relationship between the kinetic energy and temperature of an electron is expressed as:

$$E_{rms} = \frac{1}{2} m_e v_{rms}^2 = \frac{3}{2} k T_e \tag{2.3}$$

in which m_e is the electron mass, v is the velocity, k is the Boltzmann's constant and T_e is the electron temperature. Since the average electron energy in a weakly ionized plasma is typically around 2eV, according to equation (2.3) the calculated electron temperature T_e ~15000K. The ion temperature T_i and gas temperature T_g are much lower: typically 500K and 400K, respectively. Although the electron temperature T_e is very high, the wafers and etch chamber remain at a low temperature because the electron mass is too small to heat them up.

For a collection of moving molecules or electrons colliding with each other, the collision frequency is calculated as:

$$f_{gg}(gas - gas) = \sigma n_g v_{avg} 4\sqrt{2} \tag{2.4a}$$

$$f_{eg}(electron - gas) = \sigma n_g v_{ave} \tag{2.4b}$$

where σ is the collision cross section, n is the density and v_{av} is the average speed. The mean free path is defined as the average distance a molecule or electron travels between collisions. Based on the collision frequency, the mean free path can be derived as:

$$\lambda_g = \frac{v_{avg}}{f_{gg}} = \frac{1}{\sigma n_g 4\sqrt{2}} \tag{2.5a}$$

$$\lambda_e = \frac{v_{ave}}{f_{eg}} = \frac{1}{\sigma n_g} = \frac{kT}{\sigma p_g} \tag{2.5b}$$

So, according to equation 2.5, the mean free path of an electron is much larger (approximate 6 times larger) than the gas molecule due to its very small size. It is also noticed that the mean free path is inversely proportional to the pressure. The lower the

pressure, the longer the mean free path. This is because less particles exist at a low pressure so that they will be able to travel without collisions for a longer distance.

Since a plasma is conducting, it will respond to local changes in potential. If a charged particle is inserted into a plasma, a cloud of opposite charges will quickly surround the particle. This prevents an electric field to develop outside the cloud. This phenomenon is called Debye shielding and the cloud is called the sheath. The Debye length is referred to the thickness of the sheath and can be formulated by the equation below:

$$\lambda_D = \sqrt{\frac{\varepsilon_o k T_e}{n q^2}} \tag{2.6}$$

For an etch system with the plasma density of ~10^9-10^{12}, the Debye length is typically in the range of 0.01 to 0.1mm. This value is significantly smaller than the dimension of the reactor chamber. Therefore, a plasma is considered as macroscopically neutral. Given the Debye length, we can describe the oscillation of electrons inside a plasma. When a group of electrons are displaced with respect to the ions, a restoring force is developed and pulls the charges back toward each other. They accelerate to their equilibrium positions and then separate in the opposite sense. The frequency of this motion is estimated as:

$$\omega_{pe} = \frac{v_e}{\lambda_D} = \sqrt{\frac{n q^2}{m \varepsilon_o}} \tag{2.7}$$

Plasma oscillations are classified into plasma-electron oscillations and plasma-ion oscillations. The frequency of plasma-electron oscillation is usually very high since the mass of an electron is small. For a SF_6 plasma of density n=10^{10}cm^{-3}, the frequency of electron and ion are approximate 1GHz and 2MHz, respectively. A typical RF frequency of plasma sources is 13.56MHz. This frequency is low enough to enable electrons to respond and extract electrical energy while the ions cannot follow the fluctuation and will stay relatively motionless.

2.1.3. DC bias, ion sheath and ion motion in the sheath

DC bias is an important plasma parameters that controls the etch rate, selectivity and profile. Thus in the first part we will give a brief introduction about the generation of DC bias. Figure 2.2a is an illustration of a parallel plate etch tool in which the upper electrode is grounded and the lower electrode is connected to an RF power generator through a blocking capacitor. With the RF alternating potential, the polarity on the lower electrode is changed accordingly. When the polarization is positive the plasma electrons will be attracted to the lower electrode and when the electrode is negative polarized, the electrons will be repelled and positive ions will be attracted. However, because the frequency of the RF alternating potential is very high (commonly 13.56 MHz), the ions are too heavy to follow the alternating RF field and thus unable to travel across the plasma sheath. On

the other hand, electrons with much smaller mass can respond and will therefore gradually charge both electrodes and leaving the plasma positively charged. If both electrodes would have the same area facing the plasma, nothing special would happen. However, in RIE plasma systems, the lower electrode (cathode) has a much smaller area than the opposing chamber wall (anode). This difference in area is causing that the cathode will acquire a much more negative voltage with respect to the plasma than the anode. As a result, a measurable DC bias (or self-bias) is generated between two electrodes (the cathode being more negative than the anode) and denoted as V_{dc}. Typically, the chamber (i.e. anode) is grounded and the positive plasma potential V_p is taken with respect to the grounded anode. The V_{dc} value depends on the RF power and is in the range of ten to several hundred of volts. Because of the average negative potential of the lower electrode, the ions are attracted towards the bottom electrode and will bombard a sample placed on that electrode. The larger the V_{dc} in combination with V_p, the stronger the bombardment will be. This ion bombardment is involved in the etching process.

The magnitude of voltage induced at an electrode is dependent on its surface area. The relationship of the induced voltages and surface areas between two electrodes can be approximated as[4]:

$$\frac{V_1}{V_2} = \left(\frac{S_2}{S_1}\right)^4 \tag{2.8}$$

in which V_1, V_2 are the voltages induced at each electrode and S_1, S_2 are the surface areas, respectively. This means that for the smaller electrode (cathode), a higher voltage is induced. In an etching system, the anode electrode (the chamber wall) is designed much larger than the cathode electrode (the platen where the wafer is placed) so that an adequate V_{dc} is induced at the wafer while induced voltage at the chamber wall is minimized to prevent sputtering of the wall material.

Figure 2.2b shows the potential waveform at the cathode when it reaches the equilibrium state. At this state, the cathode is negatively charged most of the time and turns positive for a small period during each cycle. Therefore, high electron currents flow onto the cathode only for a short time while the much lower ion currents flow almost continuously. When the cathode is negatively charged, electrons will be pushed away and therefore almost no electrons exist in the nearest region of the cathode. This region is called the ion sheath in which almost no electron collision will happen and excitation and relaxation events are rare. For this reason, no light is coming out from this region and, therefore it is called the dark space. The ion sheath thickness can be represented by the following equation:

$$d = \frac{2}{3}\left(\frac{\varepsilon_o}{j_i}\right)^{\frac{1}{2}}\left(\frac{2e}{m_i}\right)^{\frac{1}{4}}\left(V_p - V_{dc}\right)^{\frac{3}{4}} \tag{2.8}$$

Where j_o is the ion current density, ε_o is the permittivity of vacuum, e is the electric charge, m_i is the ion mass and V_p is the plasma potential. For a high density plasma such as the inductively coupled plasma, the ion sheath thickness is on the order of 0.01 to 1cm.

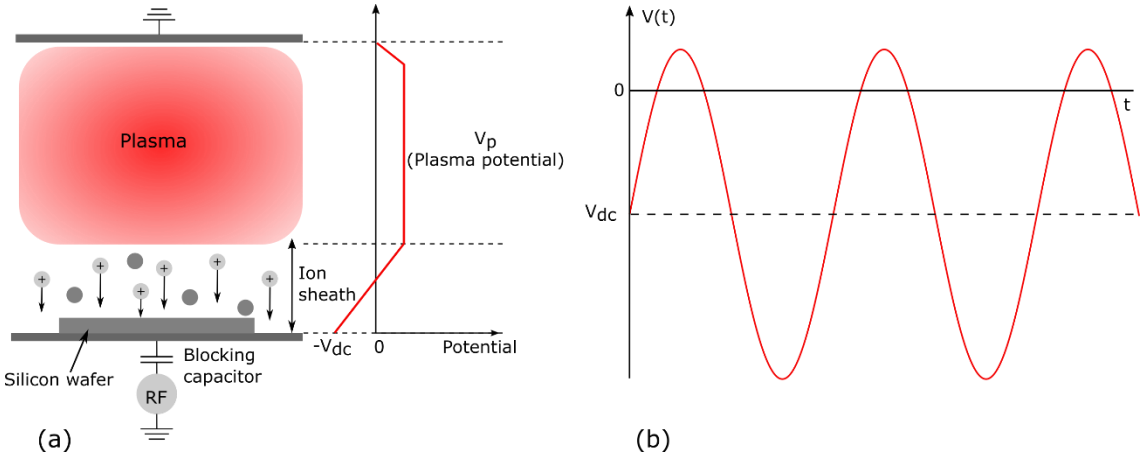

Figure 2.2. (a) Illustration of the DC bias and ion sheath in a RF plasma. (b) Voltage waveform at the cathode in a RF plasma.

As mentioned earlier, the plasma is electrical conductive in which electrons and ions travel in random directions. The ions that reach the wafer surface will have an energy equal to what they have in the plasma plus what they have gained in passing through the ions sheath. Therefore the total obtained energy of ions when reaching the wafer equals $V_p + V_{dc}$, which will drive the etching mechanism. The directionality of the impinging ions depends on the pressure as collisions inside the plasma sheath will divert the ions from their trajectory. This scattering of ions in the ion sheath is determined by comparing the ion sheath thickness and ion mean free path. If the mean free path of ion is much larger than the ion sheath thickness, ion can travel to the sample surface with almost no scattering. This directionality of ions is an important factor for anisotropic etching and will be discussed in the next section.

2.2. Introduction of plasma etching

2.2.1. Etching mechanism

Plasma etching is an important technology in semiconductor industry to transfer the lithographic defined patterns into the target materials. The basic concepts of plasma etching are making use of a glow discharge to crack relatively stable molecules into chemically reactive and ionic species that will react with the material to be etched and form volatile products. More specifically, a suitable feed gas (e.g. SF_6 for silicon etching) is introduced to an etch system (RIE, ICP) and the gas phase etching environment, consisting of neutrals, electrons, ions, radicals, etc., is generated through the process of

electron-impact dissociation/ionization. The reactive species will diffuse from the plasma bulk to the sample surface (silicon wafer), that is placed on an RF driven capacitively coupled electrode. The positive ions from the bulk of the plasma are attracted to the sample by the DC self-bias and plasma potential that assist the etching. A series of reaction processes will happen when the radicals and ions arrive on the sample surface, which are shown in Figure 2.3 for the case of etching silicon with SF_6 plasma.

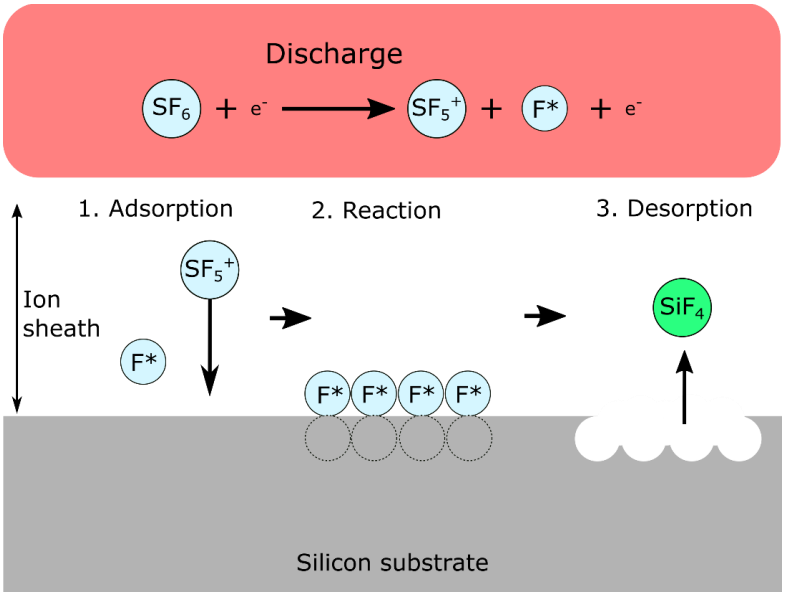

Figure 2.3. A schematic illustration of plasma etching in the case of silicon etching with SF_6 plasma.

- Adsorption: when plasma species reach the silicon substrate or the chamber wall, they will adsorb. This adsorption depends on the chemical affinity and surface temperature. The lower the temperature at the surface, the thicker the adsorbed layer becomes. Therefore, the chamber walls are normally set at higher temperature than the silicon surface to avoid chamber contamination and other interactions.
- Reaction: a chemical reaction between the adsorbed radicals and the sample atoms will take place and create etch products. In case of etching silicon with SF6 plasma, the chemical reactions between the F radicals and the silicon atoms occur spontaneously forming the volatile silicon tetrafluoride (SiF4). However, for other halogens such as chlorine or bromine, the chemical reaction between Cl/Br radicals and silicon atoms does not happen spontaneous. In this case, ion bombardment is needed to provide energy for the absorbed radicals to attack the backbones of silicon atoms efficiently, thus enhance the reaction.
- Desorption: when the chemical reaction between the reactive radical and the silicon atoms finish, the reaction by-products should desorb from the surface so that the etch

can continue. This requires that the products of the reaction must have a high vapor pressure at the substrate temperature so that they are volatile at the process conditions.

- Exhaust: after the etch products desorb from the sample surface, they will diffuse into the plasma chamber and should be pumped out. Otherwise, plasma-induced dissociation of product molecules will occur and re-deposition can take place.

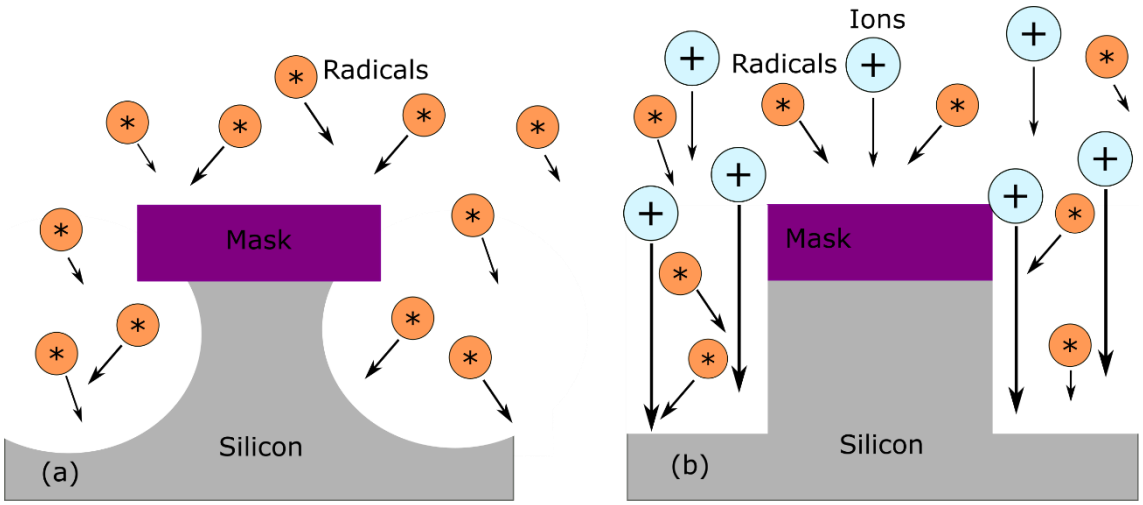

Figure 2.4. (a) Isotropic etching. (b) Anisotropic etching.

Figure 2.4 illustrates the difference between isotropic and anisotropic etching. For an etching process in which only the radicals of the plasma are attributed to the removal of the target materials, the etching will proceed not only in the vertical direction, but also in the horizontal direction. This is because the radicals diffuse from the bulk of plasma to the sample randomly by Brownian motion and get access to the sample at all directions. This phenomenon is called isotropic etching and results in an undercut under the mask. In some applications such as surface micromachining, the buried layer can be removed completely by using isotropic etching. However, undercut caused by isotropic etching will make fine patterning more difficult. In order to transfer the lithographic patterns with a high level of fidelity, it is desired that the etching should proceed only in a vertical direction. This type of etching is referred to as anisotropic etching which will be explained more in the next section.

2.2.2. Mechanism of anisotropic etching

As mention earlier, anisotropic etching is realized when the reaction between radicals and sample surface proceed only in the vertical direction. One approach to achieve this goal is using incoming ions to strike the etch target surface at normal incidence in order to induce the surface reactions. Figure.2.5a shows an anisotropic etch in which the reaction between the radicals and sample material is facilitated by impinging kinetic ions. This is

called ion-induced etching in which the ion bombardment will increase the etch rate significantly[5]. Otherwise, the etch rate will be very low when it is etched only by the radicals or by physical sputtering. The main cause of this phenomenon is believed to be due to the effect of temperature at the bombarded areas[6]. When the ions attack this area, its temperature becomes so high that enhance the radicals reactions. As a result, the etch rate by ion-assisted reactions goes up in orders of magnitude larger than that by only neutral radicals. Because the ions imping the wafer in a vertical direction, it is possible to achieve anisotropic etching in which the etch rate in the vertical direction (by ion-assisted reactions) is much faster than in the horizontal direction (by radicals). This is the mechanism of realizing anisotropic etching by ion-induced reactions.

Another approach to obtain anisotropic etching is to protect the sidewall from lateral etching by putting a passivation gas together with the etch gas into the etching chamber. The passivation gas will form a thin layer all over the sample surface, thus prevent the sidewall from the invasion of radicals during the etching process. Figure.2.5b shows a model illustrating the sidewall passivation process. Because the ions come to the sample surface in the vertical direction, only the horizontal part of the passivation layer is sputtered away and the etching proceeds through the reactions between the exposed sample surface and the radicals. On the other hand, the passivation layer on the sidewalls remains since there are almost no ions coming at this angle. As a result, the sidewalls are protected from the attack of radicals while the etching occurs in the vertical direction makes it possible to achieve anisotropic etching. This approach is used for many materials and especially helpful when etching with a gas chemistry that is in essence isotropic. For example, silicon etching with fluorine chemistry will occurs isotropically so that a passivation method is needed to prevent the lateral etching. In this case, either oxygen or fluorocarbon can be added to the etch gas to create the passivation layer[7-9]. The passivation step can either happen simultaneously with the etching process or it can be done in a so-called Bosch process where the etch step and passivation steps are sequentially altered[10].

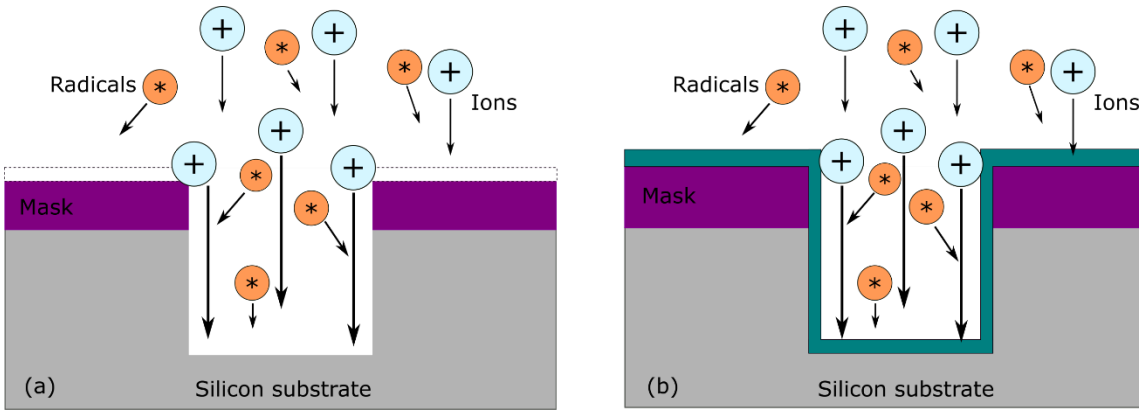

Figure 2.5. (a) Ions-induced etching. (b) Ions-inhibitor passivation.

2.2.3. Characterization of the etch performance

In an etching process, there are different requirements that depend on the specific application. Some parameters are widely used in order to characterize the etch performance, which are illustrated in Figure.2.6a.

Etch rate

The usual first parameter to evaluate is the etch rate, which is defined as the thickness of the film that has been etched divided by the etch time. The process condition can be modified such that the etch rate will get as high as possible for high throughput microscale etching or it can be made very low for nanoscale etching. For an etch process with only chemical reactions the etch rate is typically high but also isotropic. In contrast, for purely physical sputtering the etch rate is very low but directional. However, by combining both methods, the synergetic effect leads to a strong increase in the etch rate while preserving directionality. The gas chemistry also has a strong impact on the etch rate. With a specific sample material, the etching gas should be selected so that it results in a higher surface reactions and desorption of etch byproducts. For examples, it is known that the fluorides of silicon are more volatile than the chlorides[11]. Therefore when the fluorides chemistry is used, the etch products desorb more easily and the etch rate becomes higher.

Selectivity

The next parameter is the selectivity which is calculated as the ratio between the etch rate of the mask and the target film. This parameter indicate how well the mask can protect the underlying structures while etching proceeds. A high selectivity means that less mask material is etched away while the target film is removed. In photolithography, normally thinner resist film is used to enhance the resolution on the devices. Therefore a high selectivity is necessary to ensure that the resist will be able to sustain the etch process. The etch selectivity is dependent on the parameter setting in the etch process in which the ion energy and the bonding strength of atoms should be considered[12]. Since the reaction occurs in a direction that creates a larger bond strength, the gas chemistry can be selected corresponding to the etch target so that the selectivity can be improved. For example, the bond strength between silicon and halogen gases (Cl, Br, and F) is smaller than that of Si-O, therefore these gases can be used for the etching of silicon with SiO_2 as a mask[13]. In this case, the etch rate of SiO_2 will be very low with respect to silicon and a high selectivity will be achieved. Another effective approach to increase the selectivity is to decrease the ion energy in a gas system in which the etch rate of the mask material is much dependent on the ion energy than that of the etched target. Therefore, when the ion energy is lower, the mask material will be etched away slower resulting in a high selectivity.

Etch profile

In anisotropic etching, the etch profiles should have straight sidewalls with minimized dimensional shifts from the mask patterns. However, in some cases, the sidewalls of the etch profiles may be not perfectly straight with a deviation of an angle θ from the vertical. We call it positive tapered if the angle $\theta < 90^{o}$ and negative tapered if the angle $\theta > 90^{o}$. A positive tapered profile is normally created by reposition of materials on the sidewall. This can be either passivation layer created by the plasma chemistry or non-volatile materials which is sputtered off by the ion bombardment[14]. A positive tapered sidewall is preferred in applications such as nanoimprinting to fabricate master molds with tilted sidewalls so that an imprinted polymer can be released easier[15]. A negative tapered profile can happen when a trench/hole with an isotropic chemistry is etched in combination with a passivating chemistry. When the trench/hole gets deeper, the passivation gets thinner and the etching will start having a lateral component. This will lead to a negative tapered etch shape. The negative tapered profiles should be avoided since it can create shadow effects for the post etch processing.

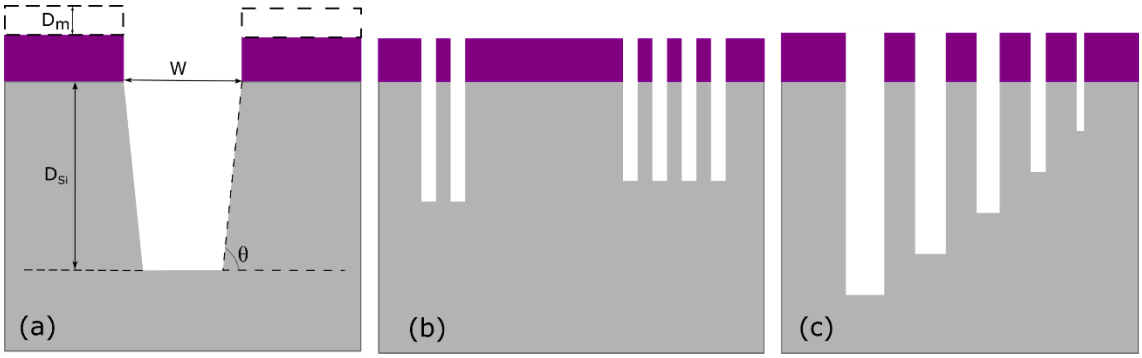

Figure 2.6. (a) Parameters for characterization of the etch performance. (b) Microloading effect. (c) Aspect ratio dependent etching (ARDE).

Loading effect

The loading effect is the phenomenon in which the etch rate during plasma etching depends on the total exposed area[16]. It is observed when the etch rate in a batch etcher decreases according to the increased number of wafers in the processing chamber. This effect is called macroloading to differentiate it from the microloading effect in which the local variation in patterns densities can lead to the local variation of the etch rate[17-19]. The microloading is not pronounced for an etching process in which the etch rate is limited by ion bombardment[20]. However, for an etching process limited by reactive species, the areas with high pattern density will have lower etch rate than the areas with low pattern density as shown in Figure.2.6b[21]. This is because for the regions of higher pattern density, there will a higher local depletion of reactive species resulting is the decrease of

etch rate. In order to reduce the nonuniformity caused by the microloading effect, the process parameters can be modified by increasing the gas flow rate or decreasing the plasma pressure[22].

Aspect ratio dependent etching (ARDE)

Aspect ratio dependent etch rate (ARDE) or RIE lag is a well-known phenomenon in plasma etching that describes how the etch rate depends on the aspect ratio of the patterns[23, 24]. The aspect ratio (AR) is defined as the depth of the feature divided by its width. Figure.2.6c shows the schematic demonstration of ARDE lag phenomenon. The silicon trenches with various dimensions are etched simultaneously resulting in a lower etch rate in the smaller trenches than in the bigger ones. This implies that the etch rate decreases when the etched depth increases and the ARDE phenomenon is affected by the aspect ratio rather than by the width or the depth of the trench. There are several main factors causing the ARDE phenomenon with the dominant one depending on the plasma process and the material being etched. Some studies show that ARDE occurs because of the depletion or reflection of reactive radicals along the trench[25, 26]. Other studies demonstrate chemistries where the decrease of ion flux at the bottom of the trench slows down the etch process[27, 28].

2.3.4. Etch profiles obtained after the plasma etching

In plasma etching, the etch profile is expected to be straight with the same width both at the top and bottom of the patterns. However, the obtained etch profiles may be different and depends on the etch conditions and target material. Let us have a look at various etch profiles obtained after etching.

Undercut

The undercut profile is a result of lateral etching of material under the mask where the passivation layer has been eroded. This removal of passivation layer may be caused by the bombardment of ions being reflected from the mask or deflected by due to differential charges to the sidewall. The passivation layer can also be removed by chemical etching of the reactive radicals. Once it is removed, the reactive radicals can laterally etch the target materials and create undercut (Figure.2.7a). Normally, the undercut occurs under the mask where the radicals flux is largest and the passivation layer is more vulnerable. In order to prevent the undercut, a stronger passivation step should be implemented to provide a better sidewall protection that is able to resist the whole etching process.

Faceting

Faceting of the mask during etching is mainly caused by the ion sputtering. Since the sputtering yield depends on the angle of incoming ions, the sharp corners of the mask will be eroded faster than other parts due to a higher momentum transfer and faceting occurs[29].

As a result, sidewalls of the mask will slowly become positive tapered and attain at an angle correlated to the maximum sputtering rate. When the etching proceeds, the ions bombardment will continue to erode the mask and the positive tapered will be transferred into the silicon features as shown in Figure 2.7b.

Bottling

Bottling is a phenomenon in which the etch profiles have the arched sidewalls with the largest width of the trenches/holes is not localized at their entrance (Figure 2.7c). It is mainly caused by the collisions of ions during their travel through the ion sheath. The more collisions, the broader the ion distribution function will be. This divergence of ion flux to the sidewall will weaken the passivation layer causing bottling. The consequence of bottling is that it will make the process of filling trenches/holes more difficult because the top part may close before the other part is filled. Bottling can be minimized by lowering the pressure or increasing the DC bias. Both solutions sharpen the ion angular distribution of the incoming ion flux.

Trenching

Trenching is the effect in which the corner has a higher etch rate than other parts at the bottom of the etched pattern. This happens due to ions being reflected from the sidewall when either the sidewall is a little off from vertical or the impinging ions can be a little off normal to the surface[30, 31]. As a result, the ion flux will be locally focused into the corner at the bottom of the patterns leading to the enhancement of the etch rate near the edge as shown in Figure.2.7d. Trenching can be avoided by decreasing the energy of ions or switching the etching process into the regime that is limited by reactive radicals rather than by ions so that the influence of ions will be reduced.

Notching

Notching is an effect that evolves a local lateral etching at the interface between an etch layer and etch stop layer (Figure 2.7e). It is a typical etch profile obtain when etching silicon down to a buried SiO_2 layer. When reaching the SiO_2 layer, the SiO_2 layer will charge positively and thus deflect the following positive ions towards the sidewall. This ions deflection will remove the passivation layer on the sidewall close to the bottom of the patterns and the local lateral etching will take place under the attack of reactive radicals[32]. In order to reduce notching, the process parameter can be optimized to strengthen the passivation layers during the over etch time. Another method is to use a low-frequency pulsed plasma that attracks both positive and negative ions so that the effect of differential charges built up can be minimized[33].

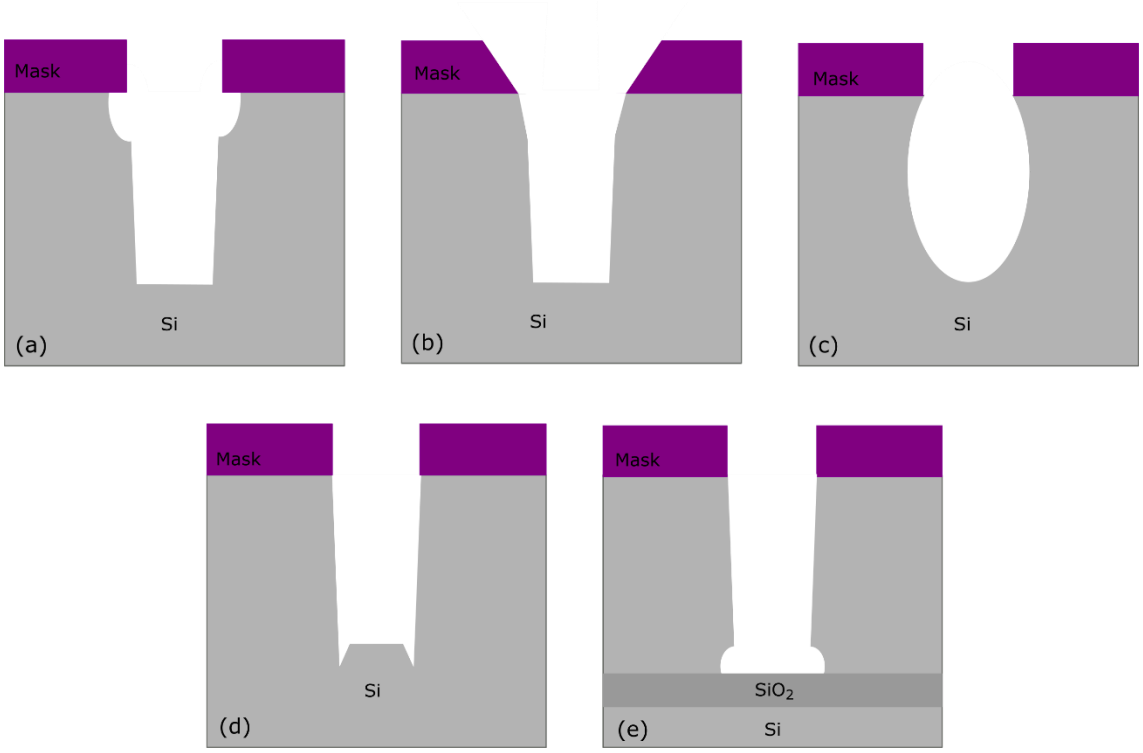

Figure 2.7. Schematic illustration of patterns profiles obtained after plasma etching. (a) Undercut. (b) Faceting. (c) Bottling. (d) Trenching. (e). Notching.

2.3. Silicon etching using fluorine-based plasma

The development of silicon etching using fluorine-based plasma is summarized in table 2.1. Based on the introduction of the etch gases into the etch tool, the plasma etching of silicon can be categorized into two main techniques. One technique called mixed mode in which the etch gases are added to the chamber at the same time. Another one is the switched mode in which the etch gases are sequentially fed into the chamber during the etching process. Depending on what the type of gas is used to protect the sidewall, silicon etching can also be divided into oxygen-inhibitor or fluorocarbon-inhibitor etching. In the next sections, a brief overview of the mixed mode and switched mode will be presented.

2.3.1. Mixed mode

Plasma etching of silicon started around the late 1970s when various etch gases were introduced to transfer lithographic patterns from resist mask into silicon. Within these years, gases like HBr and Cl_2 gained popularity and became the widely used gases in semiconductor processing. After SF_6 was introduced and showed its high silicon etch rate potential, it became the standard choice in the MEMS community, especially when mixing SF_6 with oxygen showed good directionality at room temperature[34]. However, the

SF_6+O_2 mixture comes with a weak sidewall protection that can hardly withstand the higher fluorine pressure needed for the requested high etch rates in MEMS fabrication.

In 1988, the cryogenic etching was proposed in order to improve the sidewall protection[35]. With this technique, the silicon substrate was cooled by liquid nitrogen to below -80^{o}C so that the desorption of silicon oxy-fluoride was suppressed and thus could protect the sidewall from corrosion. The cryogenic etch has shown promising results with high silicon etch rates and smooth sidewalls. However, this technique requires a constant cooling at cryogenic temperatures and the etch result will depend on the substrate temperature. In addition, the profiles are pattern dependent that needs cumbersome optimization when complex MEMS patterns are requested. These drawbacks limit a large scale industrial applications.

Table 2.1. The development of silicon etching using fluorine-based plasma.

Si etch	**O-inhibitor**	**FC-inhibitor**
Mixed mode	1983: Conventional process Gas: SF_6+O_2 at RT 1988: Cryogenic process Gas: SF_6+O_2 at -100^{o}C	1970s: Early plasma etching Gas: SF_6+C-Cl-Br-F at RT
Switched mode	2010: Black Silicon Method XI Gas: SF_6/O_2 at cryogenic 2019: CORE process Gas: SF_6/O_2 at RT	1994: Bosch process Gas: SF_6/C_4F_8 at RT 2009: DEM process Gas: SF_6/CHF_3 at -40C 2018: DREM process Gas: SF_6/C_4F_8/Ar at RT 2018: DREAM process Gas: SF_6/O_2/C_4F_8/Ar at RT

2.3.2. Switched mode

The limitation associated with the continuous mixed mode has been overcome with the introduction of the Bosch process in 1994[36]. This is a 2-step process using a sequence of SF_6/C_4F_8 gas in which the task of silicon etching and sidewall passivation are separated into individual step so that the etchant and inhibitor species will not interfere with each other, thus enabling a better sidewall protection. Figure 2.8a illustrates a standard Bosch process. It uses a repeating sequence of plasma enhanced deposition to passivate silicon features, a physical etch for directional removal of this layer at the base of the features, and an isotropic etch for silicon removal at the cleared surfaces. The switched mode enables high rates and makes the etching of complicated structures relatively straightforward. However, due to the isotropic etching of silicon in fluorine radicals, the Bosch process creates scallops that cause a prominent sidewall roughness.

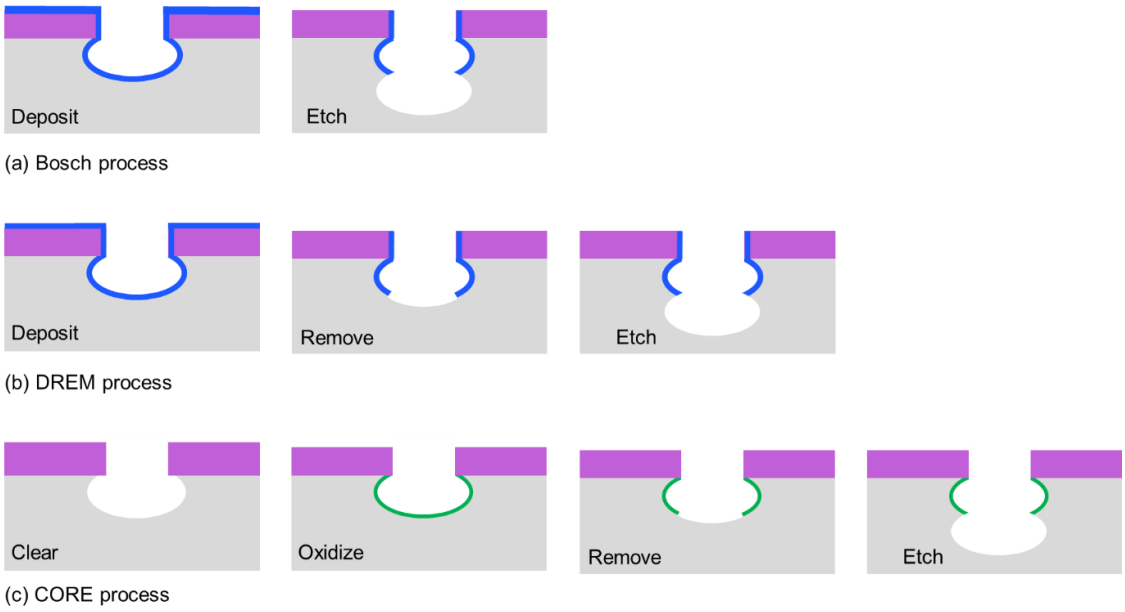

Figure 2.8. Schematic illustration of Bosch process (a), DREM process (b) and CORE process (c).

The Bosch process can be improved further by separating its basic functions into perfectly synchronized individual steps. In 2018, Chang et al. developed a 3-step etching process called DREM (stands for Deposit, Remove, and Etch Many times) that separates the etch step from the Bosch process into an ion-assisted removal of the fluorocarbon layer and almost bias-free reactive radicals etching of silicon[37]. The DREM process is illustrated in Figure 2.8b. Compare with the traditional Bosch process, the DREM process has the advantage of higher etch selectivity, uniform sidewall roughness and better control of the etch process. The DREM process has also empowered groundbreaking three dimensional

(3D) engineering with silicon sausages, fences or stacked perforated membranes are now considered to be standard manufacturing[38, 39].

Based on a similar concept, this thesis has adapted the DREM process in order to make it more reliable and sustainable by replacing the C_4F_8 gas (a major gas in mainstream directional silicon etching, but also an extremely strong greenhouse gas) into O_2 gas. This proposed process is called CORE (stands for Clear, Oxidize, Remove, and Etch) and illustrated in Figure 2.8c. Using the CORE process, it is now relatively straightforward to shape silicon material (using Cr as a hard mask) with aspect ratios beyond 50. Moreover, it shows an excellent performance in nanoscale structures with an accurate and controllable etch rate. It is the first switched sequence of its kind and challenges the monopoly of the established Bosch sequence due to its better stability, reliability, robustness, sustainability and tool-friendliness. More details about the CORE process will be introduced in the next chapters.

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Chapter 3. The CORE sequence

A nanoscale fluorocarbon-free silicon plasma etch process based on SF_6/O_2 cycles with excellent 3D profile control at room temperature

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This chapter will present a study on the development of a fluorocarbon-free directional silicon etching procedure called CORE (standing for Clear, Oxidize, Remove, and Etch) in which a switching sequence of SF_6 and O_2 is operated at room temperature. The CORE process resembles the well-known SF_6-based Bosch process, but the usual C_4F_8 inhibitor is replaced by O_2 oxidation with a self-limiting characteristic. In this chapter, the effect of varying the time in each step on the etch profiles is carefully investigated. Based on the obtained results, the design rules of the CORE sequence are formulated for further optimization. Then other etching characters includes profile tuning, mask selectivity, 3D fabrication and microscale etching process will be presented sequentially. The last part of the chapter will discuss about the plasma oxidation in the CORE sequence and its self-limiting property.

This chapter is based on the publication: Nguyen, V.T.H., Silvestre, C., Shi, P., Cork, R., Jensen, F., Hubner, J., Ma, K., Leussink, P., de Boer, M. and Jansen, H., 2020. The CORE Sequence: A Nanoscale Fluorocarbon-Free Silicon Plasma Etch Process Based on SF_6/O_2 Cycles with Excellent 3D Profile Control at Room Temperature. ECS Journal of Solid State Science and Technology, 9(2), p.024002

3.1. Introduction

Ever since the invention of the transistor in the Bell laboratories (in 1947) and the introduction of lithographic reproduction tools for integrated circuits (in 1958), the sizes of patterns have been downscaled to create more functionality or computing power on a smaller chip size. Till recently, focus has been directed to upgrade the lithographic tools to decrease the lateral resolution or improving etch tools/recipes to transfer lithographic defined patterns deeper into the bulk forming 2½D etched material (More Moore). However as this approach is predicted to reach the ultimate limit within a few years, only novel materials (Beyond Moore) and system diversity like sensor integration or truly 3D techniques (More Than Moore) can further increase chip density or functionality per cubic centimeter. To have a better understanding of current technology drivers and near future trends or needs, the reader is invited to read a few of the latest review papers on these subjects and the final International Roadmap for Semiconductors ITRS 2015 or the more recent IRDS roadmaps[1-7].

In the early years of plasma etching, various etch gases were introduced to transfer patterns from resist-mask into silicon[8-10]. In general good directionality could be achieved, but at the expense of a poor mask selectivity. Within these years, gases like HBr and Cl_2 became the standard choice in semiconductor plasma processing and kept their position ever since. However after SF_6 was introduced and showing its high silicon etch rate potential, it became the number one choice in the MEMS community, especially when mixing the SF_6 with oxygen showed good directionality (less undercutting)[11]. Even though the SF_6+O_2 plasma mixture shows a reasonable selectivity and profile control at room temperature, it comes with a weak sidewall protection that barely can cope with the higher fluorine pressure needed for the requested high etch rates in MEMS fabrication. Furthermore, the profiles are pattern dependent (i.e. smaller trenches generally show a more positive tapered profile than the wider ones[12-14]), which is probably the most bothersome fact and partly explains why the semiconductor industry has not yet embraced this technique.

Mixed mode - cryogenic etch*:* Lowering the substrate temperature below -80°C improves the sidewall oxygen protection as the silicon oxy-fluoride reaction products start to freeze at the surface[15]. This method enables high silicon etch rates with a good directionality and is commonly known as cryo etching[16-20]. However, the pattern dependency cannot be removed in this way (Figure 3.1a) and mixed mode etch recipes are typically highly design specific and the recipes often need cumbersome optimizations. So, in general the cryogenic etch gives an acceptable performance, yet it needs proper and time-consuming fine-tuning when complex MEMS patterns are requested.

Switched mode – Bosch sequence*:* With the introduction of the patented 2-steps Bosch process in 1994 (we call it DEM, which stands for Deposit and Etch Many times), the switched etching of complicated MEMS structures gained popularity and totally overruled the cryogenic etching within a few years[21,22]. It uses the sequential inlet of

inhibitor and etch-gas. Truly enough, the cycle creates prominent scallops, but it also forms nice directionality and the pattern dependency almost vanishes, which makes process optimization relatively easy (Figure 3.1b). Moreover, a higher selectivity than mixed mode is possible because bias is only applied during the etch step (Figure 3.2a) and not continuously.

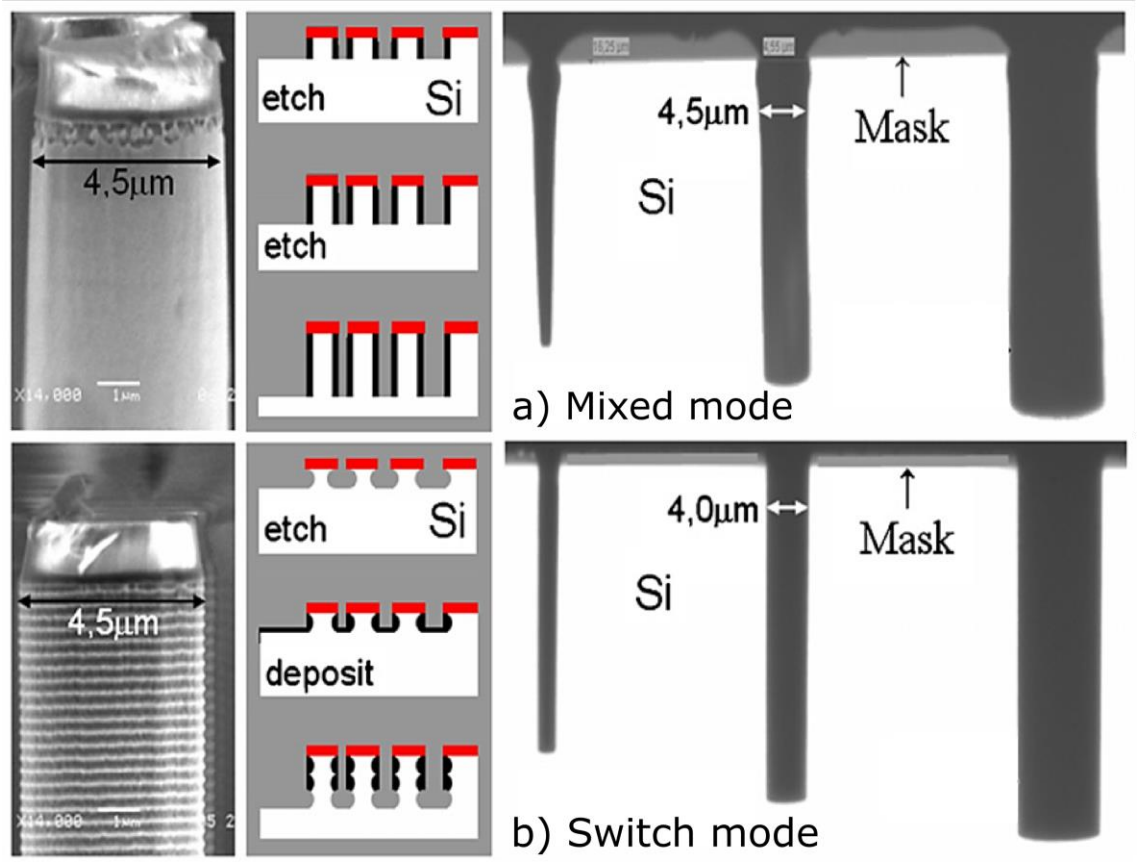

Figure 3.1. The SEM cross-sectional views of trenches after DRIE[20]. (a) The trenches were etched in mixed-mode. (b) The trenches were etched in switched-mode.

***Switched mode – DREM sequence**:* The DEM sequence can be further improved by decoupling the bias from the etch step and forming the 3-steps DREM process (Deposit, Remove, and Etch Many times). Consequently, the bias time can be set just long enough to remove the bottom of the etching feature (Figure 3.2b). In this way, the mask selectivity can potentially reach infinity[23]. This DREM procedure is in fact an improved version of the 1986 patent by Okudaira, but using C_4F_8 instead of CCl_4 and a better separation between the bottom remove and etch steps[24].

A familiar characteristic of directional plasma etching is that the etch rate decreases with increasing etch depth and it is specifically pronounced for high aspect ratio features (holes and trenches). For the switched sequence this so-called RIE lag will result in scallops that are getting smaller and smaller for every next etch cycle further down the trench. To

counteract this lag effect, the DREM sequence is able to increase the etch time of the individual cycle (called time ramping in Figure 3.2b). In this way, scallop sizes are programmed to become uniform throughout the etch process and high aspect ratio structures above AR=50 with a minimum of profile distortion are relatively easily achieved[23]. Furthermore, 3D silicon sculpturing has become straightforward; a procedure called DREM within a DREM, because it is basically the original DREM loop chopped into a bigger DREM loop. Using this concept, silicon sausages, fences, or stacked perforated membranes are now considered to be standard manufacturing[25-28].

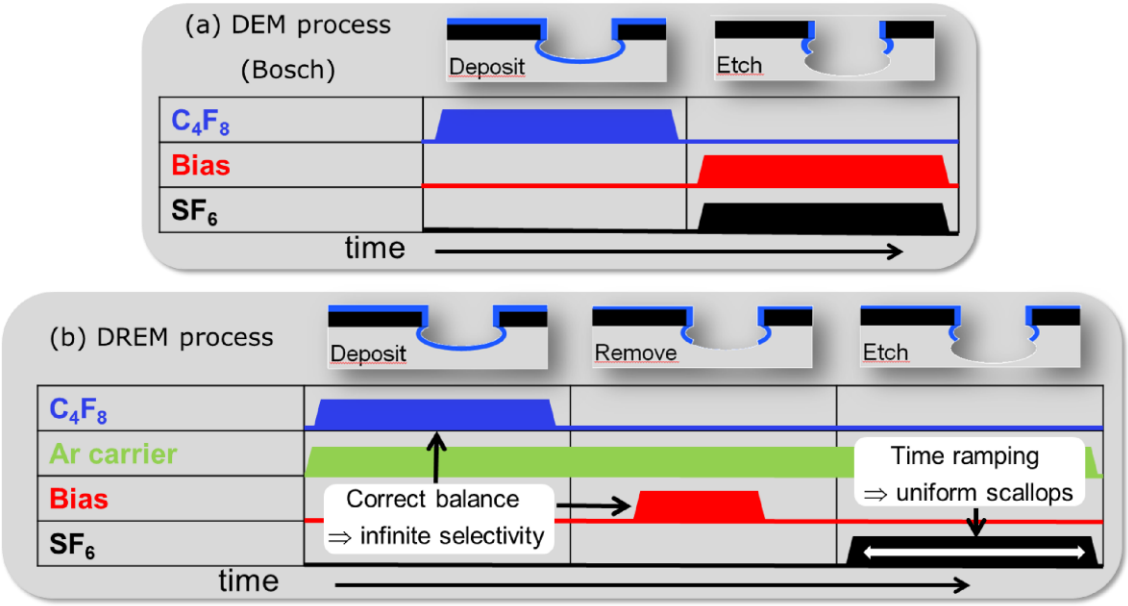

Figure 3.2. Process representation of the switched modes. (a) 2-steps DEM sequences. (b) 3-steps DREM sequences.

***Switched mode – DREAM sequence**:* Like all processes derived from the 2-steps Bosch process, the 3-steps DREM process comes with a flaw: trenches tend to close at the entrance due to the pile-up of fluorocarbon (clogging) as illustrated in Figure 3.3a, which limits the fabrication of nanoscale structures and deep trenches or holes. The consequence of a closing entrance is that the smaller dimension will be copied downwards the trench and consequently the profile becomes more positive tapered with proceeding etch time and eventually halts (Figure 3.3 encircled area). This pile-up can be prevented by proper tuning, but this is time-consuming.

A more appropriate approach is to introduce an additional ash step to remove the remaining fluorocarbon deposit directly after the etch step (Figure 3.3b). This results in the 4-steps DREAM (Deposit, Remove, Etch, Ash, Many times) procedure[29]. In this way the next deposition step starts with a clean sidewall and trench closing is prevented (Figure 3.3c). Again, the DREAM sequence can be part of a bigger loop to enable the manufacturing of high-quality 3D structures: the DREAM within a DREAM strategy. An

additional benefit arrived from the DREAM sequence is that the tool is more protected against process drift from polymer pile-up. This is because the ashing step not only cleans the trench entrance but also the reactor walls. Of course, due to the ashing plasma we rather prefer e.g. SiO_2 than resist as the pattern transfer mask. The DREAM sequence slightly resembles the dual sidewall protection approach as proposed in 2000 by Ohara, yet following a different philosophy[30,31].

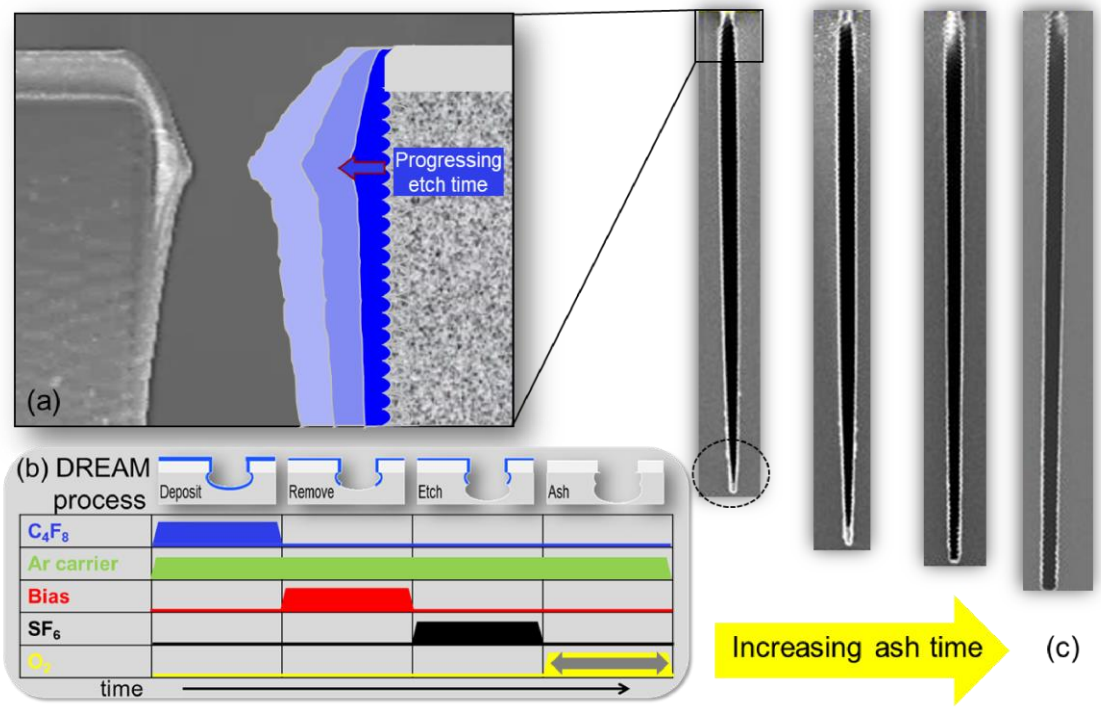

Figure 3.3. DREAM (Deposit, Remove, Etch, Ash Many times) sequence to prevent neck clogging (blue) and to improve directionality.

Let us capture the previous DRIE techniques in a single picture (Figure 3.4): *Mixed mode* generally shows low mask selectivity with some undercut, smooth but size dependent profiles and asks for time-consuming process development. When solely using *O inhibitor*, however, mixed mode is clean with low process drift and is tool-friendly. *FC inhibitor* causes process drift and reactor contamination, which needs frequent and time-consuming cleaning and conditioning procedures. Most FC gases are also more expensive and environment unfriendly. However, the *switched mode* is operator/process friendly and creates design freedom (due to the pattern-independent slopes of etching features) and 3D options.

To move a step closer to an ideal process there is a need to combine the maintainability and sustainability from the mixed oxygen process with the robustness and design freedom from the switched fluorocarbon process. A proper method is found by replacing the C_4F_8 inhibitor gas from the DREAM sequence into O_2. This also has the advantage of addressing at least part of the quest to find environmental sustainability by exchanging

the environmental non-green C_4F_8 for perfectly green O_2. The rest of this paper will concentrate on this novel process called CORE (meaning Clear, Oxidize, Remove, and Etch).

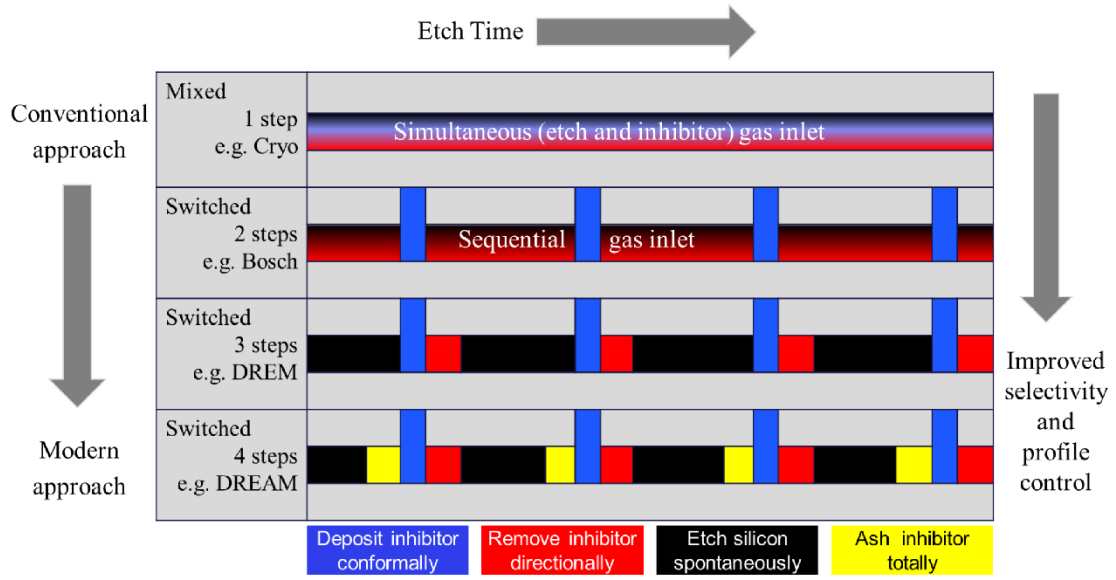

Figure 4: Resume of all the established (D)RIE modes

3.2. Equipment and experimental

The silicon etching system used in this study is the SPTS/Pegasus DRIE, which facilitates switched mode and RIE mode. The system has been dedicated for SF_6/O_2 based plasma etching solely and has no prior fluorocarbon history. This fluorocarbon-free chamber is needed to ensure the absence of any contamination or influence on the fragile oxygen plasma oxidation that is required for the CORE sequence. The system is much like the Alcatel/Adixen AMS 100 SE DRIE system that has been described extensively in a previous review paper, but lacks the cryogenic option[20].

Silicon <100> wafers (150mm diameter, 675µm thick, 5-10Ωcm, phosphorous-doped n-type) have been prepared with 1.5µm thick resist patterns (AZ MIR 701 DUV resist from MicroChemicals) and exposed using a maskless aligner (MLA150, Heidelberg) to create patterns above 400nm. For nano-sized patterns between 30 and 100nm, a 100kV electron beam writing system (JEOL JBX-9500FSZ) scanning with 10nm steps is used. Positive tone e-beam resist ZEP520A (ZEON) having a thickness of 145nm is spin-coated for 60s at 4000rpm followed by a bake for 3min at 180°C. During the electron exposure current is set at 12nA with 10nm spot size and dose between 293µC/cm^2 (30nm lines) and 263µC/cm^2 (100nm lines). Exposed samples are developed for 180s with ZED-N50 (n-amyl acetate) and rinsed with Iso-Propanol Alcohol.

The patterned wafers are cleaved into 1cm × 1cm chips and individually mounted on a silicon carrier wafer using Galden® PFPE fluid (Solvay Solexis SpA) for sufficient

thermal contact or to fix it[32]. As the current study is aiming at nanoscale accuracy useful for the semiconductor industry, the etch tool is put in the RIE-mode and set for low etch rate (between 1 and 50nm per minute for sufficiently tight dimensional control). This is done by adjusting the SF_6 flow (ca. 15sccm) and the platen power (ca. 10W) accordingly. The oxidation step is set for 50sccm O_2 flow. The SF_6 MFC has a maximum of 50sccm and, thus, providing an accuracy of better than 1sccm. After the etching, the Galden heat transfer fluid is wiped gently from the backside of the sample with alcohol sprayed on a tissue and the sample is cleaved manually using a diamond pen for SEM analysis.

To determine the optical thickness of growing films less than 5nm, the film is scanned by 690 wavelengths between 210 and 1690nm to get the corresponding Psi-Delta values (Variable Angle Spectroscopic Ellipsometer M2000XI-210, J.A. Woollam Co.) at standard cleanroom conditions (22.5^{o}C and 45% humidity). Five different impinging incident angles (59, 60, 61, 62, 63 degrees) and 5s acquisition time are used to improve accuracy further. This data is analyzed and fitted with inbuilt models as provided by Woollam. The most convenient model to fit the growing oxide films in this study has been found to be an interfacial layer resembling silicon monoxide film (Intr_JAW) on top of silicon (Si_JAW). Therefore, we assumed the film to be having a known refractive index spectrum and only fitting the optical film thickness for the best root mean square error (RMSE) value. Even though this SiO-equivalent might present faulty values as the growing film most likely changes its composition in the initial stages resulting in a graded index[33-35] and it will for sure incorporate a water layer, it has the advantage of making the analysis far simpler while still keeping good statistical parameters (high confidence level of the presented variance and low RMSE). So, the ellipsometric measurement is accurate, but the interpretation (or analysis) can be wrong. Nevertheless, independent of the model used, the observed trends are correctly presented and can be trusted.

The CORE recipe always starts with a non-selective 60s so-called ‘DeDamage’ etch in front (15sccm SF_6 at 100% Throttle → 0.5mT and 10W Platen) to remove any wafer process history (e.g. resist scum and native or subsurface plasma oxide) without etching the silicon or harming its subsurface too much. The CORE sequence is specifically aiming at the nanoscale and operates without coil power (i.e. ICP source) or plasma focusing funnel and outer electromagnet at 10A. For higher etch rates and improved selectivity, the ICP source can be added (DRIE-mode), but care should be taken to prevent reactor wall sputtering (e.g. by using a Faraday cage). That is, the normally strong Al_2O_3 ceramic of the reactor wall can be transformed into the much weaker AlF_3 that subsequently sputters onto the wafer causing roughening (e.g. for 100sccm and 2mT Ar and 2kW we observed 0.3nm/min sputter-deposition).

The silicon carrier is electrostatically clamped with 10Torr Helium backside pressure at 20^{o}C with platen down even though the nanoscale CORE performs excellent without backside cooling or clamping as well. The main reason is that the oxidation step improves with increasing temperature and therefore thermal runaway is prevented when the wafer-

temperature rises. This is another disadvantage of the Bosch and cryogenic techniques where a slight increase in temperature will slightly reduce the passivation that will slightly increase the etch rate and increasing the temperature even further, i.e. thermal runaway.

Finally, to stress the issue, it is advised not to use any fluorocarbon-based chemistries in the etch tool and limit the excessive use of Galden oil. These processes have shown to affect adversely the CORE etch performance. Fluorocarbon residues are very persistent and tough to remove even after prolonged cleaning plasma (O_2 or NF_3) and might cause process drift. For example, trying to perform the CORE sequence on an identical DRIE tool – but mainly used for Bosch processing – gave unsatisfactory results (lot of sidewall erosion) even after several hours of O_2 plasma cleaning.

3.3. Results

Even though switched etch processing that uses oxygen for the sidewall passivation is already known for a decade, these existing techniques rely on cryogenic temperatures in order to freeze the silicon etch products (SiO_xF_y) and to enable sufficient profile control[36-37]. The current innovation discusses the use of O_2 pulses to oxidize surfaces (or rather terminates the silicon surface atoms with atomic oxygen) conveniently at room temperature in a fluorine-based chemistry to create high-raised silicon structures. The proposed room temperature oxidation technique has its roots in the early years of continuous (or mixed) mode plasma etching[11].

The procedure to find the correct profile is following the Black Silicon Method as described extensively in literature before, and basically boils down to 3 steps[12, 20]. The first step is to determine the spontaneous silicon etch rate for the whole SF_6 plasma spectrum (e.g. gas flow, pressure, plasma power) and select an appropriate etch rate (e.g. for nanoscale etching around 20nm/min). The second step switches on the oxygen inhibitor to suppress the etch to almost zero. The last step will add or adjust the bias to increase the ion bombardment and create the requested directionality. For the first step, a convenient continuous etch rate of 15nm/min is found for 15sccm SF_6 flow at 2% throttle position (resulting in 50mTorr process pressure) and 10W platen power. In the second step, we needed 3s at 50sccm O_2 flow, also at 50mTorr and 10W platen power, to block the silicon etching. At the last step, it shows that 20s at 5sccm SF_6 with APC throttle valve fully opened (giving a pressure below 0.2mT) is sufficient to clear the bottom.

The initial test was simply transforming the DREAM sequence into CORE (Figure 3.5a) and coarse-tuned the observed profile for directionality and to form big scallops that are easily detectable by SEM tool. Figure 3.5b shows the result after performing a sequence of 5 cycles. The scallops of around 60nm in size are correctly shaped and without severe erosion such as etch pits. The following sections will investigate the impact of the individual steps of the CORE sequence on the final etch result.

CORE	Time	Pressure	SF_6	O_2	Power
Step	s	mTorr	sccm	sccm	W
C	0-10	~0	0	50	0
O	3-6	50	0	50	10
R	5-30	0.2	5	0	10
E	120-480	50	15	0	10

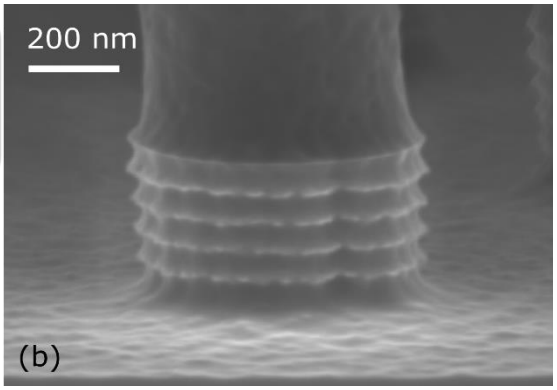

Figure 3.5. (a) Coarse-tuned CORE cycle used as the center point run in the designed experiments. (b) 5 well-controlled regular 60nm scallops along silicon pillars with resist still on top.

3.3.1. Development of the CORE process

C-step

The Clear-step might be the surprising step in the CORE cycle, but it is found to be crucial to include this reactor clearance step in order to get a reliable etch result. Basically, the step is performed with an oxygen sweeping flow (to prepare the mass flow controller for the upcoming O-step), but without plasma. The turbo throttle valve is fully opened to ensure the fastest removal rate of silicon etch gas residue left inside the reactor. The step prevents the SF_6 plasma – that has created SiF_x products during the previous E-step – to come into contact with the O_2 plasma of the next O-step. This contact would annihilate part of the incoming oxygen radicals by the leaving fluorine radicals and, therefore, the passivation would be compromised. A second possibility of arriving oxygen radicals that briefly meet the departing silicon fluoride is that they may combine into silicon-oxide species. The latter are nonvolatile and will contaminate the etching, for instance causing surface roughness and create the well-known black silicon[37].

Samples with a 1µm diameter pillar array were etched and observed with SEM having a fixed setting (e.g. 3kV high voltage and 400KX magnification). As observed in Figure 3.6, when the C-time is zero seconds (this means that there is no clear-step at all), the profile is strongly undercut as oxygen radicals are lost. Only after at least 4s C-time, both plasmas (SF_6 and O_2) are separated correctly and the SEM images look alike.

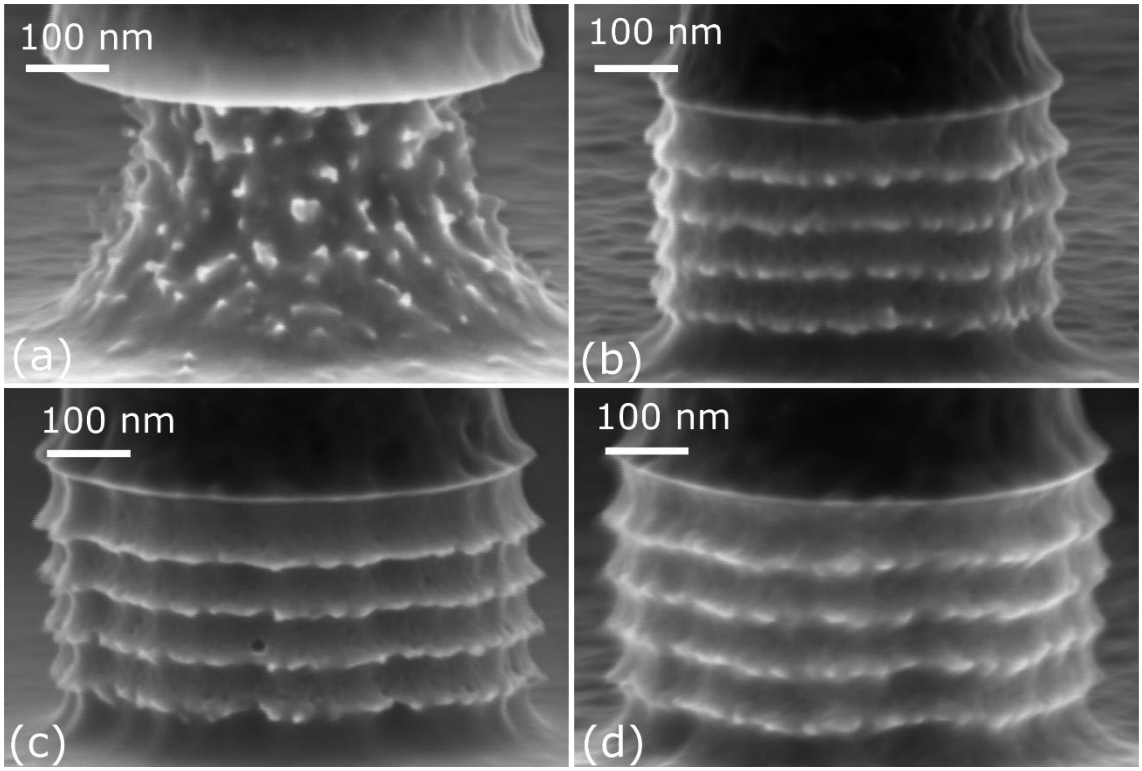

Figure 3.6. Effect of varying the C-time with O-time = 3s, R-time = 20s, and E-time = 4min always. (a) C-time = 0s. (b) C-time = 2s. (c) C-time = 4s. (d) C-time = 10s.

O-step

Obviously, the Oxidation-step is essential to enable a directional switching plasma sequence. It is assumed that the silicon surface is highly fluorinated after the Etching-step (E-step) and the fluorine-terminated silicon will be preserved during the C-step even while sweeping oxygen molecules are already present. It is only after the plasma is started that (atomic) oxygen radicals are formed. They will start to replace fluorine radicals and create an oxygen-terminated silicon surface.

Figure 3.7 shows the effect of additional oxidation time (O-time = 3, 4, 5, and 6s) on the etch profiles at a fixed E-time of 8 minutes. It is observed that the scallops only become smooth and correct when at least 5 seconds O-time is taken. Further experiments (see Appendix A) showed correct scallops for the combination O-time versus E-time: 2sO→2minE, 3sO→4minE, 4sO→6minE, 5sO→8minE, 6sO→10minE, 7sO→12minE and 8s→14min**.** This gives us the first CORE design rule: every extra second O-time will enable 2min extra E-time. However, above 8s O-time, this linear rule doesn't apply anymore. For instance, to enable 20min E-time it is found that instead of 11s, more than 25s O-time is needed. More about this abnormality, which is basically caused by the self-terminating feature of the oxidation process, will be presented later.

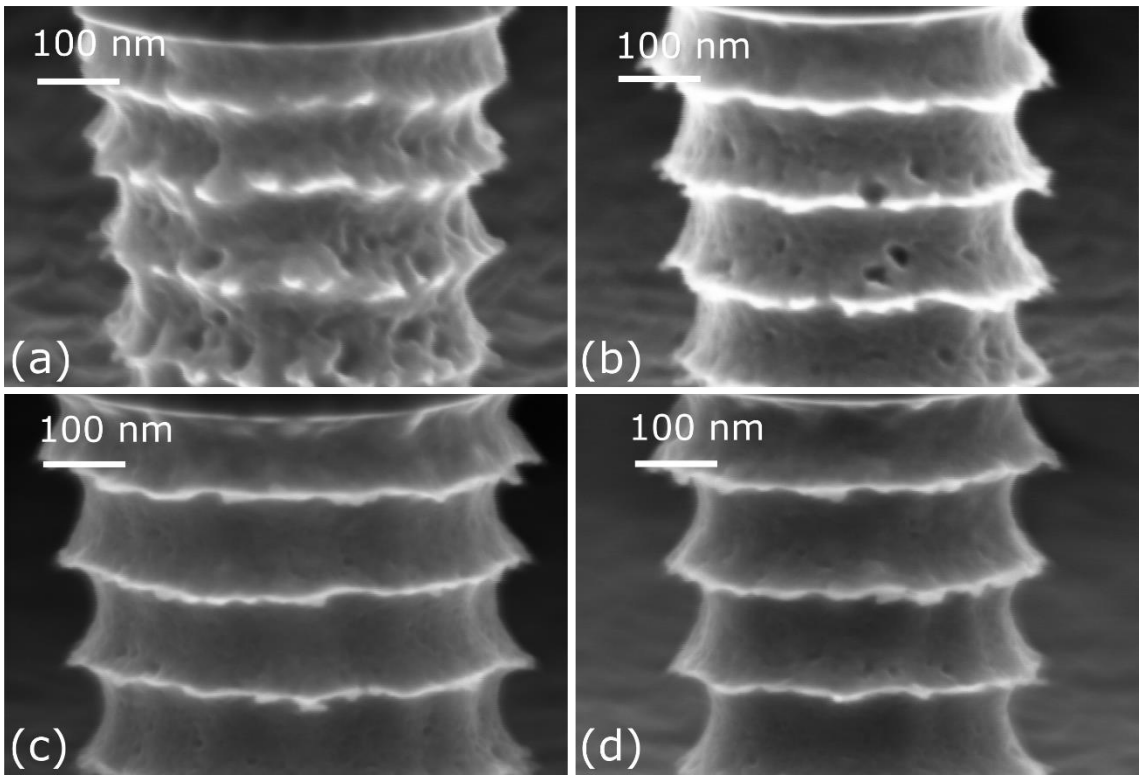

Figure 3.7. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 3s. (b) O-time = 4s. (c) O-time = 5s. (d) O-time = 6s. With C-time = 4s, R-time = 20s and E-time = 8min always.

R-step

This Removal-step to clear the bottom of etching features is the most crucial step for creating the requested directionality. The question is how we can raise the bias and ion energy only during this step and with only a single power source (since the ICP source is not used to increase accuracy and to prevent wall sputtering). The answer lies in the effect of the reactor pressure on the plasma potential. As can be found in many in-depth textbooks, the plasma potential is a function of the pressure. The lower the pressure, the higher the potential[38]. With this in mind, we can manipulate the plasma potential simply by adjusting the reactor pressure. This is accomplished by opening the throttle valve completely in this step. An additional benefit of this approach to get adaptable ion energy is that the ion angular distribution function becomes much sharper as ion collisions in the dark space vanish and accurate process synchronization is guaranteed[23]. On top of this plasma potential, the usual mentioned DC self-bias is still present and the total kinetic energy gained by the ions accelerated in the dark space facing the wafer will be the summation of both potentials: V_p+V_{DC}. We should note that all the other surfaces (e.g. grounded and floating) will have to deal with V_p only. This means that V_p can still cause reactor wall sputtering.

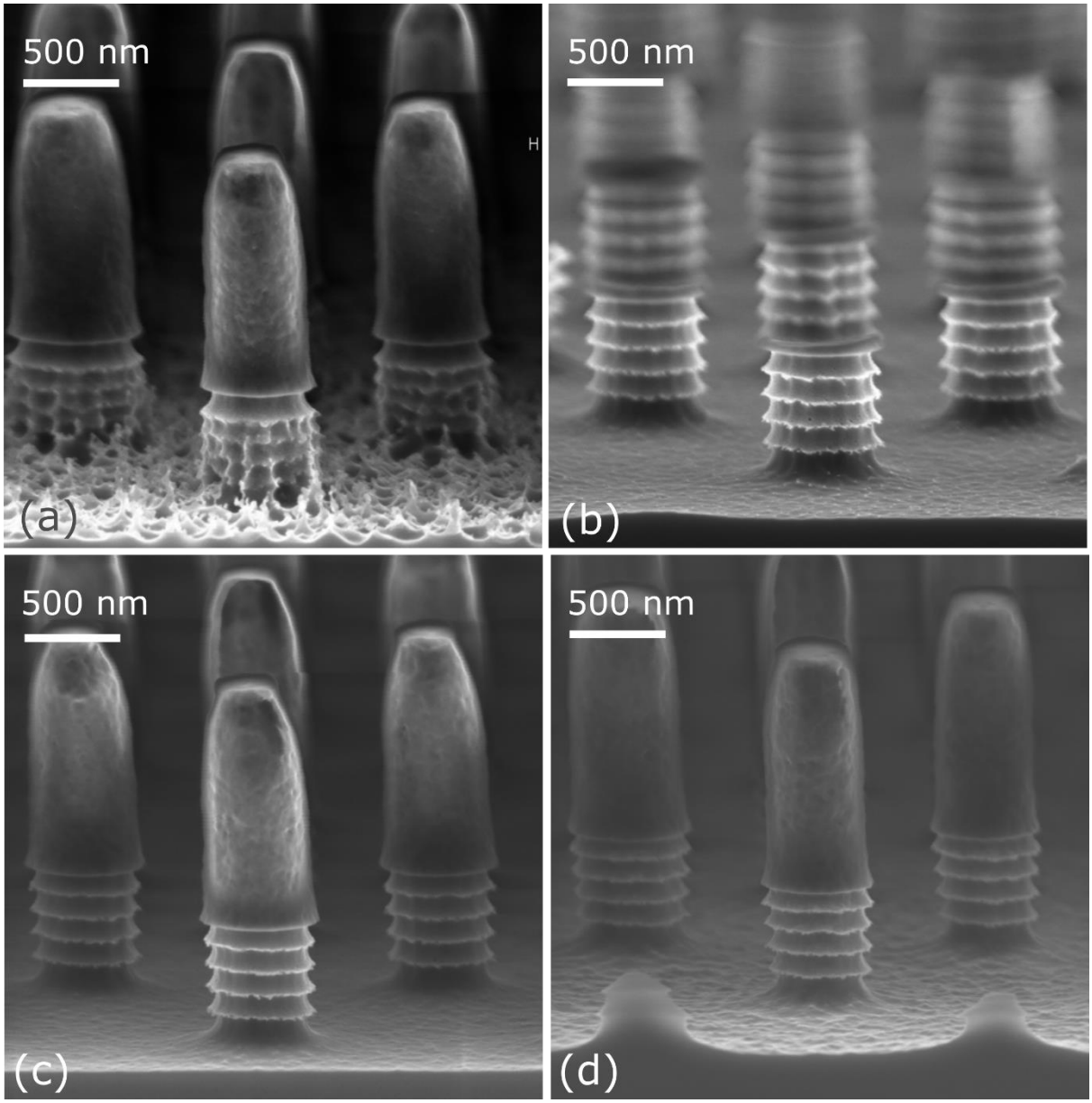

Figure 3.8. Prolonged R-time clears the bottom protection. (a) R-time = 5s. (b) R-time = 15s. (c) R-time = 25s. (d) R-time = 30s. With C-time = 4s, O-time = 8s, and E-time = 8min always.

While performing the R-step, it makes sense to assume that the removal rate of the passivation layer will increase linearly with the R-time and that this step can be halted when all the passivation has gone. Figure 3.8 shows the result of increasing R-time at a fixed CORE settings with C-time = 4s, O-time = 8s, and E-time = 8min always. The result for the 5s R-time is still rather rough (i.e. black silicon or micro grass appears) at the features bottom because not all the passivation has been removed, but after 25s R-time it is correct as expected. Indeed, checking also other O-time settings, we found a correct

smooth bottom when the R-time was set to roughly 3 times the O-time for 8min E-time . This provides us the second CORE design rule: every second of O-time needs 3 seconds R-time. Beyond 25s R-time, the bottom becomes a bit rougher again. The latter is probably because the additional R-time starts to damage the silicon below the passivation.

E-step

So far we have focused on the normal etch rate and assumed that the lateral etch will follow in the same way as many papers claim: pure SF_6 plasma etches isotropically. However, only in a perfect diffusion-controlled (viscous) isotropic etch (e.g. liquids), the horizontal etch (undercut) will match the vertical etch (etch depth) as depicted in Figure 3.9a. In case of free molecular transport, which is close to expectation in DRIE, there cannot be etching directly underneath the mask and ideally a semicircle will form (Figure 3.9b). In reality, the result is bit of both: the lateral etch is between two and three times slower than the normal etch (Figure 3.9b). Surface transport might be responsible for the result. For the plasma settings used in the CORE sequence, we found that the undercut is around 5nm when the etch depth gain per cycle is 10nm. This brings us to the third CORE design rule: the undercut is the normal etch per cycle divided by 2.

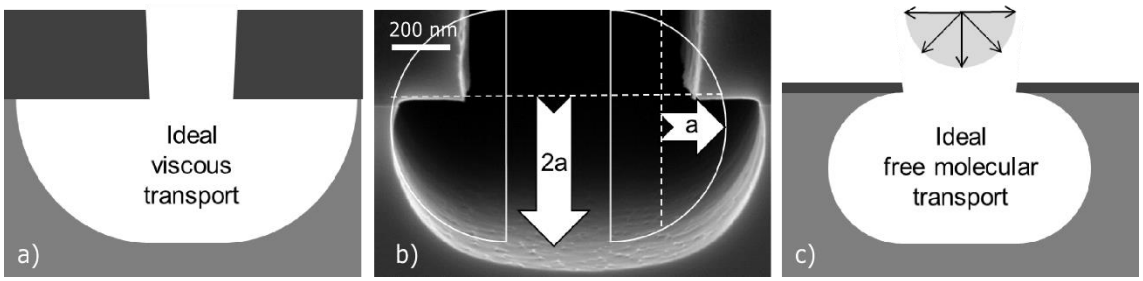

Figure 3.9. 'Isotropic behavior' in SF_6 plasma etching of silicon. The normal etch rate is typically twice the lateral etch rate (undercut).

As already stated in the first CORE design rule, the maximum allowed E-time is fixed by the O-time. However, we did not yet show implicitly what happens if the E-time exceeds its optimum value. Figure 3.10 shows the result of the CORE sequence for increasing SF_6 etch time at 3s O-time.

Here, we highlight the moment where the fluorine pressure starts to degrade the scallop's oxide protection and causing so-called sidewall pitting. Only by keeping the etch time at or below 4 minutes, the scallops are showing up virtually without pitting. Furthermore, it is observed that open field structures (the pillars at top of Figure 3.10) suffer much more from sidewall erosion than enclosed structures (the trenches at bottom of Figure 3.10). This is probably related to the difference in fluorine supply, e.g. due to Knudsen restriction in high aspect ratio features[17].

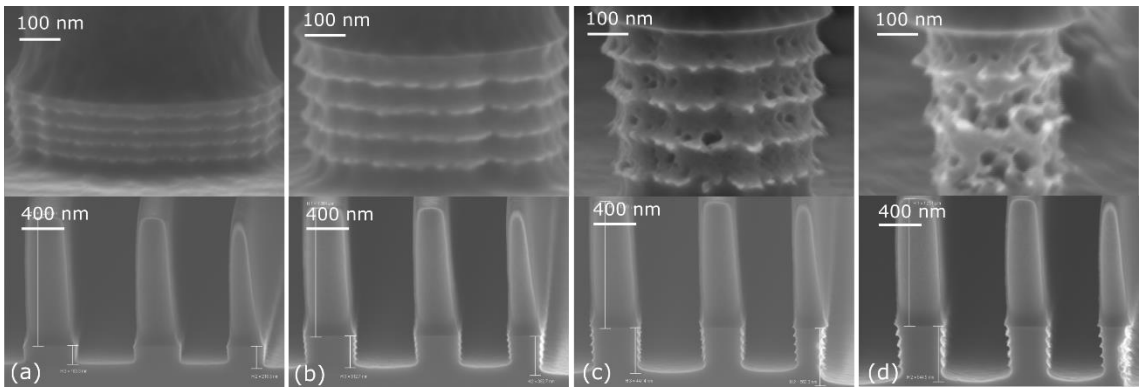

Figure 3.10. Prolonged SF_6 E-time degrades the sidewall protection. (a) E-time = 2s. (b) E-time = 4s. (c) E-time = 6s. (d) E-time = 8min. With C-time = 4s, O-time = 3s and R-time = 20s always.

The CORE cycle design rules and optimized recipe

We are now ready to put together the design rules that control the CORE sequence for the etch rate per cycle fixed at 15nm per minute:

Rule 1: 2min E-time needs 2s O-time. Every 2min extra E-time will need 1s extra O-time until a maximum of 14min E-time.

Rule 2: Every second of O-time needs at least 3 seconds R-time (for 8min E-time).

Rule 3: The undercut is roughly half of the gained etch depth per CORE cycle.

It is noticed that when the CORE sequence is performed at an elongated E-time (> 2min), surface particles below a certain threshold of lateral size (< 30nm) will be undercut totally rendering the surface relatively smooth. The shorter the E-time, the smaller this threshold will be and this results in an increased number of particles that are able to survive the lateral undercutting. Consequently, surface roughening becomes more pronounced so that a longer R-time is required to prevent it. For E-time shorter than one minute, we found that the bottom surface is smooth and clean only after at least 20s O-time as presented in Table 3.1. With this fine-tuned CORE cycle, the scallop-size reduces and proper profiles emerge with smooth, straight sidewalls and a minimum of resist mask undercutting (Figure 3.11a-c).

This virtual scallop-free ability is very attractive for applications where surface roughness compromises the application (e.g. for imprinting or high-density trench capacitors). In addition, the lack of inhibitor deposits makes the CORE procedure outstanding with respect to Bosch and related techniques. CORE also outperforms the cryogenic etching, because complicated cryogenic chucks are unnecessary (infrastructure adaptations to support the supply of liquid nitrogen can be a major roadblock for many small laboratories). Furthermore, the same recipes that perform well for microstructures are now also showing excellent performance for nanostructures down to 30nm resolution

(Figure 3.11d). Note that unlike all the other samples of this study, the 1x1cm^2 sample with the nanostructures is taken from a silicon-on-insulator (SOI) wafer. Noticeably, as found in the same image, due to the extreme mild plasma condition in which the etching is performed, plasma-induced silicon (sub-) surface damage is low and notching is virtually non-existing[39-40]. Consequently, over-etching – to take care of the notorious RIE lag – is not at all degrading the etched features.

Table 3.1. Typical fine-tuned CORE cycle.

CORE	*C*	*O*	*R*	*E*
Time (s)	4	3	20	73
Pressure (mT)	~0	50	0.2	50
SF_6 (sccm)	0	0	5	15
O_2 (sccm)	50	50	0	0
Platen power (W)	0	10	10	10

3.3.2. Demonstration of the CORE process

CORE and profile tuning

Even though a perfectly straight profile is probably the most requested demand in directional etching, sloped profiles are sometimes beneficial for specific applications. For example, in nanoimprint lithography, a slightly scallop-free and positive taper of the (silicon) mold will ease demolding[41-44]. The CORE sequence is able to support this request by ramping the E-time while etching proceeds. As established in the previous sections, the amount of undercutting is directly related to E-time and therefore it controls the profile. Figure 3.12 demonstrates the difference between a fixed E-time (a, b) and ramping E-time (c). It is observed that the CORE sequence for a fixed E-time delivers a slightly positive taper whereas the ramping E-time is slightly negative.

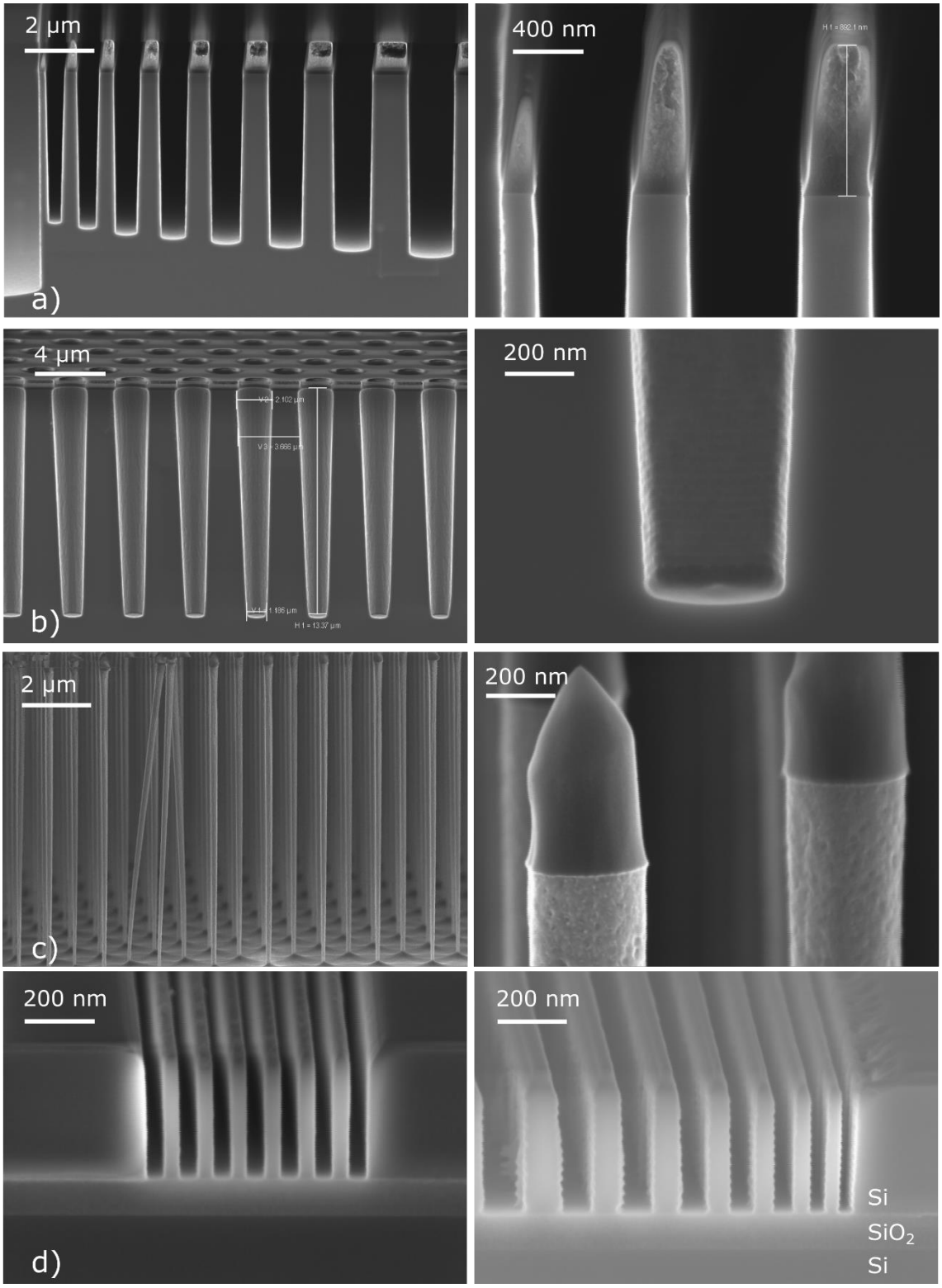

Figure 3.11. (a) Submicron silicon trenches and lines derived from the fine-tuned CORE sequence. (b) Submicron silicon holes derived from the fine-tuned CORE sequence. The sidewall angle is ca. 2º. (c) Submicron silicon pillars derived from the fine-tuned CORE sequence. (d) Notch-free nanostructures in SOI material derived from the fine-tuned

CORE sequence. (Left) Grating with 80nm periodicity. (Right) RIE lag test structure between 30 and 100nm.

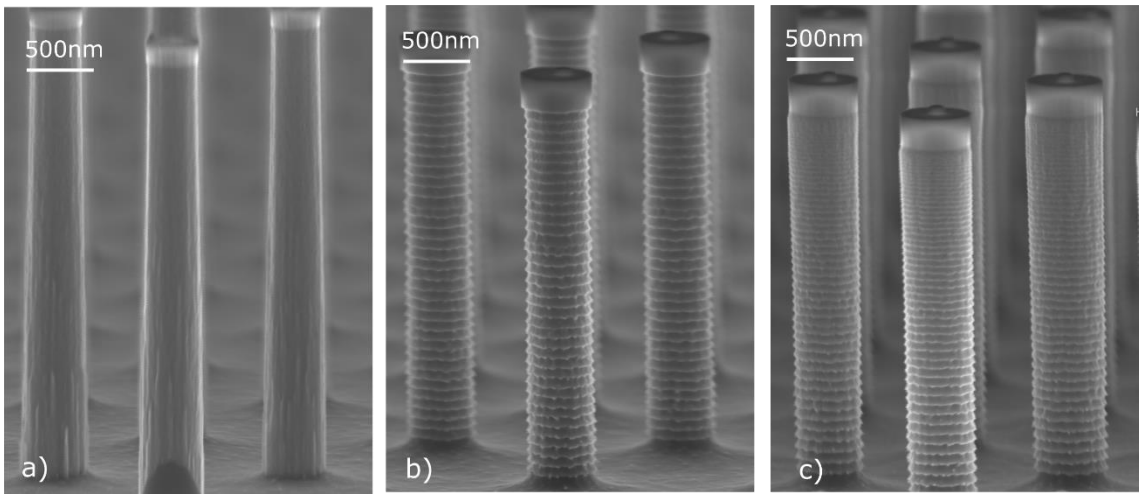

Figure 3.12: Profile tuning by fixing or ramping the E-time in the CORE sequence from Table 3.1. (a) A fixed E-time of 73s results in a positive taper. (b) A fixed E-time of 300s shows a straight profile. (c) E-time that is ramped from 70s to 330s with steps of 5s during the sequence will provide a negative taper.

CORE and mask selectivity

Till here, only photoresist has been used as a mask to create the silicon structures. Of course, resist is etched by the plasma as well and having a selectivity of ca. 10. Moreover, the use of oxygen to passivate the silicon sidewalls will inevitable consume hydrocarbons and therefore the resist will slowly retract not only at its top surface but also from aside[45]. To demonstrate this effect, Figure 3.13 shows dot patterns are etched using solely photoresist (a) and SiO_2 with resist still on top (b). Evidently, the pillars having only resist as mask are heavily eroded at their top while the SiO_2 pattern is nicely preserved even though the resist on top of it has clearly retracted. The reason for this behavior is the lateral etch of the resist pattern in time. While etching proceeds, the diameter of the resist dots will slowly decrease and therefore leaving the top part of the silicon pillars exposed. Consequently, the incoming ions in the final stages of the CORE etch will also attack the unprotected top part of the pillars and degrade the sidewall. A hard mask like SiO_2 is not suffering from this mask retraction effect and therefore will enable better control and shows an improved selectivity of ca. 35. Al_2O_3 is even better with selectivity around 700.

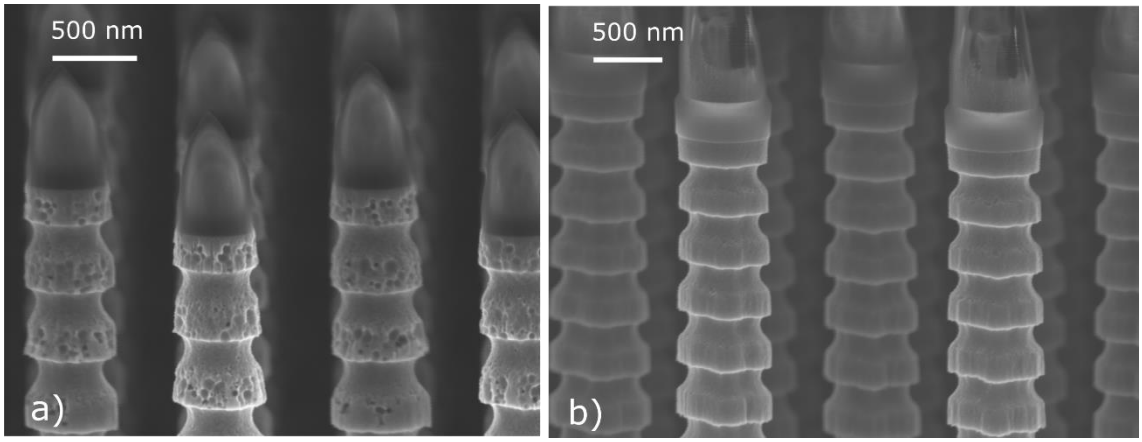

Figure 3.13. Submicron silicon pillars derived from resist dots only (a) and SiO_2 with resist on top (b).

3D CORE

Just like the DREAM sequence, CORE can handle 3D features too[46-50]. In Figure 3.14a, a total of 100 cycles of the 'standard fine-tuned' CORE sequence of Figure 3.12 is alternated every ten cycles by much longer isotropic etches or undercuts (10min at 15sccm SF_6 and 10 W platen power). This creates a vertically modulated etch profile having a 400nm periodicity and that consists of ten straight cylinders separated by nine bottlenecks. It is noticed that there is still sufficient oxide mask left. This allows for even higher aspect ratio structures. Furthermore, the number of cycles of the standard CORE sequence and the etching time of isotropic etch can be varied at will in different ways to create various 3D patterns. Figure 3.14b, c are an example of such a modified structure having shorter and longer cylinders separated by different size of bottlenecks. This demonstrates the ability of CORE process to fabricate various 3D structures, thus enable novel functionalities and better device performance in many fields.

Micro CORE

Besides the CORE sequence aiming at the nanoscale, it is obvious to find out how far we can push the limit to higher etch rates that are favorable in MEMS technology. Surely, the self-limitation is now a true burden as this will limit the amount of allowed etching during the E-step. To speed up the process, the ICP source is used to promote stronger oxidation, which allows a higher fluorine pressure during the E-step (Table 3.2). When the ICP source is used, the platen source can be discarded, thus removing the DC bias which improves selectivity.

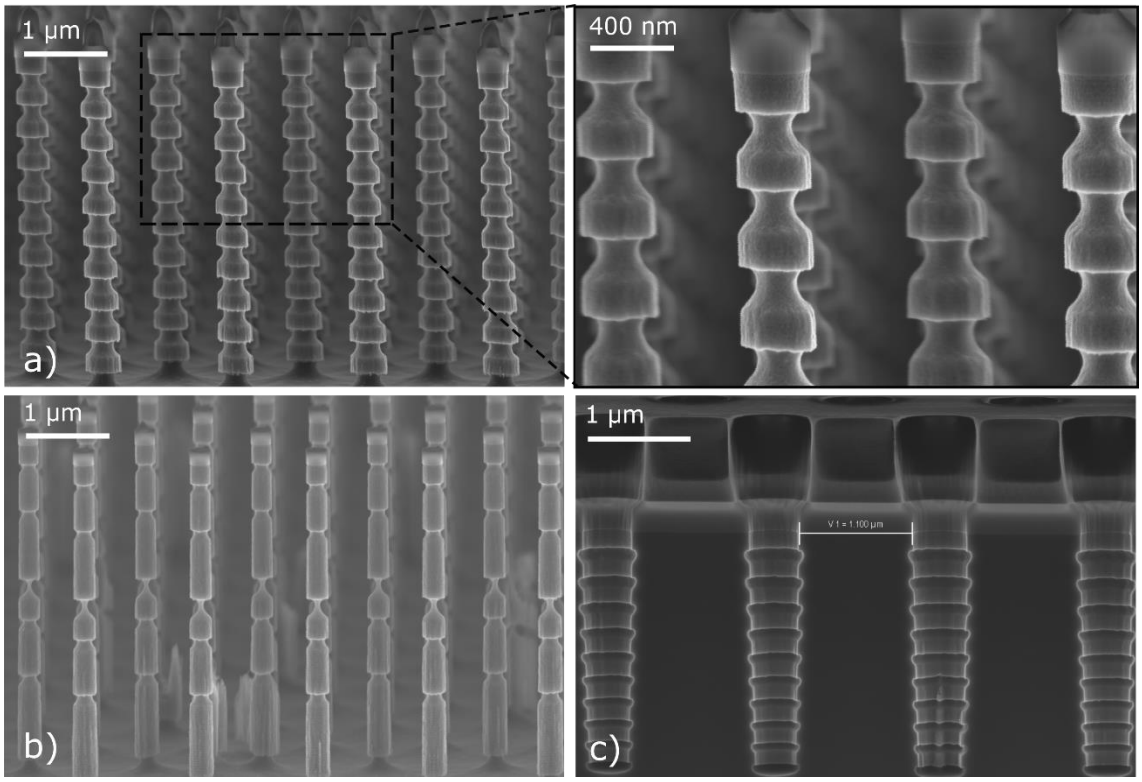

Figure 3.14. Various 3D structures shaped by interrupting a train of e.g. 10 normal CORE cycles by a single much bigger 'isotropic' undercut.

Figure 3.15 shows silicon pillars etched with the micro CORE sequence at the etch rate of 330nm/min resulting in 113µm depth and a selectivity of 200 towards SiO_2. Of course the higher etch rate will sacrifice the nanoscale accuracy due to the larger undercut and higher fluorine pressure at the sidewalls. Another disadvantage might be the increasing risk of reactor wall sputtering that will contaminate the etching process. A Faraday cage, with the ability of blocking the electric fields produced by the ICP source, could be used to avoid this reactor wall erosion.

Table 3.2. Micro CORE cycle etching using the ICP source.

CORE	*C*	*O*	*R*	*E*
Time (s)	4	3	20	33
Pressure (mT)	~0	50	0.2	50
SF_6 (sccm)	0	0	5	15
O_2 (sccm)	50	50	0	0
Platen power (W)	0	0	20	0
ICP (W)	0	2000	0	2000

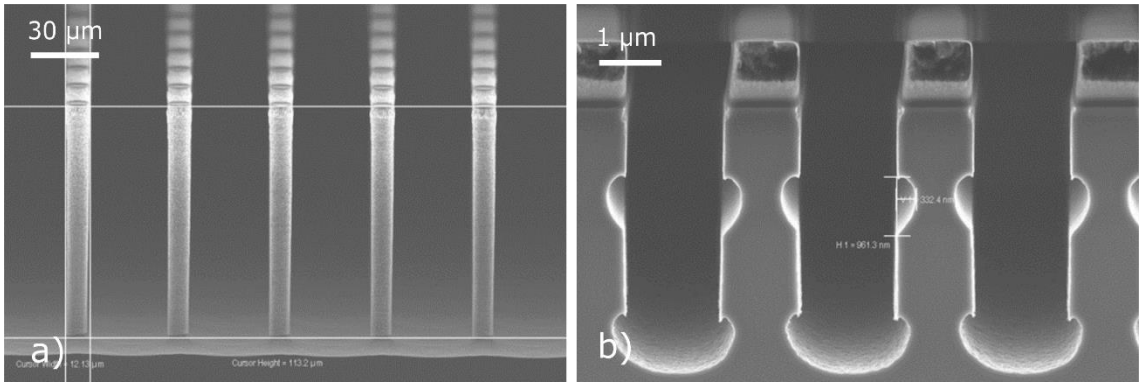

Figure 3.15. (a) 113µm high silicon features arrived from the micro CORE sequence and etching at 330nm/min. (b) 3D micro CORE.

3.3.3. Plasma oxidation and the self-limiting property

In the previous section we found that the plasma oxidation process of a freshly created F-terminated silicon surface initially seems to depend linearly on the oxidation time for 50sccm O_2 at 50mTorr and 10Watt. However, the oxidation process becomes nonlinear after ca. 8 seconds. Why is that? This section will answer the question.

It is well known that a silicon surface will start to oxidize when exposed to open air. After a few nanometers of oxide layer has grown, the process will then slow down quickly and virtually halt within a few weeks. This is the so-called native oxide growth. It is scientifically accepted that this retardation happens because the growing oxide layer acts as effective barrier and delays oxygen reaching the Si-SiO_x interface[51-64]. We assume that the plasma oxidation is much like native oxidation, only proceeding is much faster because radicals and negative O-atoms are plenty available. We further assume that, in the initial plasma oxidation process directly following an etch step, the whole silicon surface is transformed from fully F-terminated into fully O-terminated. After this rather fast surface exchange reaction, the usual plasma oxidation process of the subsurface starts, but at a much slower rate and finally virtually stops as oxygen cannot penetrate the dense oxide.

To test this hypothesis, unprocessed full wafers are loaded in the reactor and a 60s 'DeDam-step' (15sccm SF_6 at 0.5mTorr and 10Watt platen) is performed that removes the native oxide and leaves the silicon surface F-terminated. Subsequently, the wafer is in-situ oxidized using the O-step parameters from Figure 3.5 (i.e. 50sccm O_2 at 50mTorr and 10W) for a selected amount of time *t*. Then the wafer was unloaded and analyzed using ellipsometry. To minimize the influence of a varying cleanroom condition within the experimental time frame, the measurements were taken always within the first minute after releasing the wafer from the reactor loadlock[65-67]. The initial growth rate under standard cleanroom condition was confirmed to be sufficiently low to guarantee the correctness of this experimental procedure.

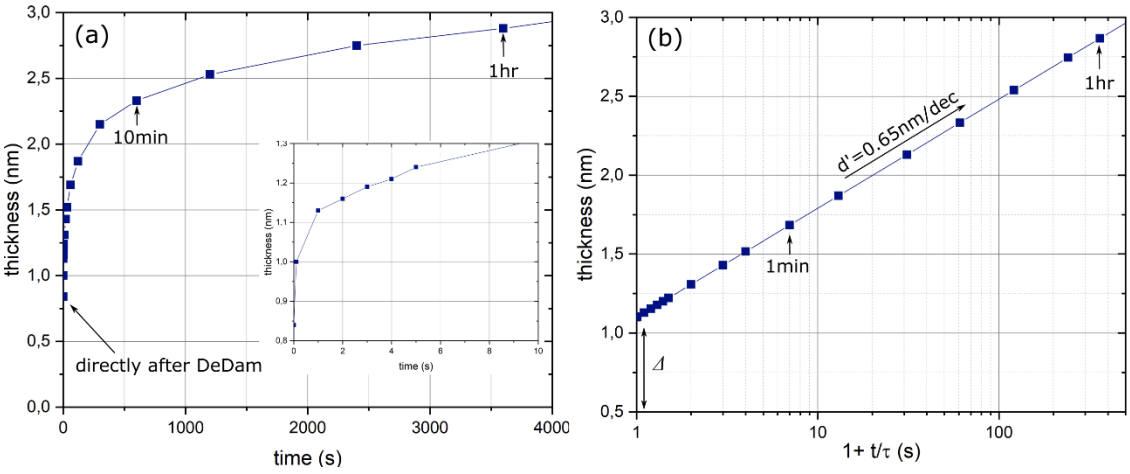

Figure 3.16. Prolonged plasma oxidation time after a 60s mild SF_6 pre-etch ('DeDam'). (a) linear scale. Inset for the magnified view of the first 10 seconds. Immediately after the DeDam Δ=0,84nm. (b) Logarithmic scale. Long term growth d'=0.65nm/decade

Figure 3.16a presents the linear plot of the plasma oxidation time t versus the oxide layer thickness d. The blue '×' crosses are ellipsometric points (typically with a 0.03nm variance at 90% confidence interval + 0.02nm error due to temperature and humidity fluctuations of the cleanroom air) and the green line represents a logarithmic model fit as proposed by Fehlner and Mott as a follow up for the famous Cabrera-Mott model to explain anodic oxidation[68-69]:

$$d(t) = d_0 + d_0' \cdot \tau \cdot \ln\left(1 + \frac{t}{\tau}\right) \tag{3.1}$$

The model has three parameters to be fitted with the ellipsometric data: d_0, d_0', and τ in which d_0=1.1nm denotes the initial thickness modeled at t=0s, d_0'=0.03nm/s stands for the initial growth rate at t=0, and τ=10s is a time constant. The experimental curve starts with a Δ=0.84nm offset and shows a rapid increase of surface oxide within the first minutes, but then continues to slow down until after ca. 1 hour the growth is virtually halted. The model predicts the plasma oxidation correctly except for the first second. The growth rate within the first second is extremely fast – possibly 1nm/s or more – but could not be determined accurately. This initiation period is thought to be caused by the rapid replacement of the fluorine termination of the silicon surface by oxygen (≡Si-F → ≡Si-O). The slope between 1 and 5 seconds is more or less linear (d_o'~0.03nm/s) and represents the beginning of the usual oxidation process which follows a purely logarithmic law. After ca. 1hour the layer has grown to a few nm and due to diffusion limitations this barrier will effectively compromise further growth, i.e., the growth proceeds at a rate of 0.65nm/decade (=d_o'·τ·ln10) for t>>τ. Thus, no indication is found that supports the Deal-Grove model[51] in which the growth should have been following a

linear-parabolic law. In fact, the results confirm a perfect logarithmic growth behavior in plasma oxidation, which is made clearer with the help of the plot in Figure 3.16b. In addition, we have seen no sign of layer-by-layer growth as observed by Taft and confirmed by many others[54-59]. A reasonable explanation why some researchers find time-logarithmic law and others layer-by-layer growth is studied by Cerofolini[70]. He provides evidence that the difference is likely to be caused by difference in the initial surface roughness: only atomically smooth wafers will cause layer-by-layer growth.

However why does the film directly after a DeDam etch start off with Δ=0.84nm? This peculiar offset is repeatedly found in literature and never explained satisfactory[52,54,71,72]. In case of the plasma oxidized surfaces presented in Figure 3.16, we believe the followings could happen. These surfaces are highly hydrophilic and consequently between three and four monolayers of water ought to be present (at 22.5ºC and 45%RH), corresponding to roughly 1nm of (ice-like) water having a refractive index of 1.31[73-76]. In the model we assumed a growing silicon monoxide (SiO, n=2.0) to be present, so we should have found a Δ-value of 0.54nm[77]. This is still not the 0.84nm offset we found, therefore we further propose the presence of an additional Si-OH interfacial layer bridging the Si-O and adsorbed water. So, when we measure plasma oxidation, we measure as well a layer of Si-OH with a few monolayers of water. This is believed to be the initial Δ-value measured by ellipsometry immediately (within a minute) after the plasma oxidation.

Besides the previous abnormalities, the observed behavior most certainly corresponds with the CORE behavior found before in the O-step section. In the first 8s the passivation improves fast, almost linearly with performed plasma oxidation time due to the rapid replacement of Si-F by Si-O. For O-times longer than 8s, the passivation does not improve as quickly as before and practically halts at a few nm, because the slow bulk oxidation regime is entered. Then, when the E-time becomes very large the profile degradation cannot be fixed at all by extra O-time anymore because of this inherent self-limiting feature. Nevertheless, even though the plasma oxidation is self-limiting, in some cases increasing the O-time will be beneficial to give high aspect ratio trenches and holes sufficient time to reinforce their sidewall to counteract transport limitations (Knudsen diffusion) of the oxygen species. A final note to make here is that the ellipsometric experiments can only partly represent the real O-step behavior of the CORE sequence. For example, Takahashi recently showed aspect ratio dependency of silicon trench oxidation using oxygen plasma[78].

3.5. Conclusions

In this chapter, a fluorocarbon-free directional silicon etch procedure using a conventional RIE settings at room temperature is demonstrated. It is based on a sequence of SF_6 and O_2 plasma cycles called CORE - meaning Clear, Oxidize, Remove, and Etch. It performs excellent in traditional high aspect ratio processing of nanoscale structures and is

particularly specialized in 3D shaping and nanoscale accuracy (i.e. ultralow etch rates). The latter is required for the More than Moore heterogeneous integration architectures for which the CORE sequence allows convenient programming and parameter ramping of the individual cycle steps in a single plasma run. A typical silicon etch rate of a fine-tuned CORE sequence is 15nm/min with a selectivity of ca. 10 towards resist (both DUV and e-beam), ca. 35 for HSQ and SiO_2, and ca. 700 for ALD Al_2O_3. Besides shaping at the nanoscale, by switching on the ICP source the technique also performs for microstructures without the need for further process optimization in between. Therefore, the procedure creates a lot of design freedom and is operator and tool friendly. When the ICP source is used and the platen source is discarded to remove the DC bias, the etch rate can be above 1µm/min and the selectivity can be as high as 200 for SiO_2 masking and low silicon loading.

The silicon oxidation from the CORE sequence works excellent at room temperature. This means that the more troublesome cryogenic alternative, which freezes the reaction products to protect the silicon sidewalls while etching, is not needed. In addition, the use of oxygen as the inhibitor has the advantage of being self-terminating: the plasma oxidation effectively halts after around 2nm of growth irrespective of the feature's dimension. This is because the silicon-oxide acts as a diffusion barrier just like in thermal oxidation. Consequently, additional oxidation time to ensure sufficient sidewall passivation of high aspect ratio trenches or holes will not negatively affect the low aspect ratio open field structures (as is the case for e.g. C_4F_8, Cl_2, or HBr based plasma chemistries due to passivation buildup resulting in clogging). After the silicon surface has become fully O-terminated, the plasma oxidation of the bulk silicon will continue but at the hampered speed due to the growing silicon oxide barrier. The oxidation will eventually come to a halt when reaching 2nm or so. Important to remember here is that the first monolayers form quickly and these layers that are used in the CORE sequence as it provides sufficient passivation during the E-time.

The result of the CORE sequence is similar to the conventional Bosch process, but has the advantage of not struggling for the pile-up of fluorocarbon deposits at the topside of the deep-etched or nano-sized features. At the same time, process drift is prevented as the reactor walls are staying perfectly clean. There is no need for excessive reactor cleaning or process conditioning procedures that generally kill the overall throughput and reproducibility. Therefore, the replacement of C_4F_8 by O_2 has at least removed part of the sustainability problem coming with the Bosch related techniques.

In this chapter, a fluorocarbon-free directional silicon etch procedure with the conventional RIE settings, called CORE, is demonstrated. The CORE process uses a switching sequence of SF_6 and O_2 plasma and is operated at room temperature. This distinguishes it from the old-fashioned room temperature and cryogenic mixed RIE processes as CORE enables a higher selectivity and creates pattern independency of etching profiles. The CORE process resembles the well-known SF_6-based Bosch process,

but the usual C_4F_8 inhibitor is replaced by O_2 oxidation with self-limiting characteristics. The etch result of the CORE process is similar to the Bosch process, however has the advantage of preventing the pile-up of fluorocarbon deposits at the topside of deep-etched or nano-sized features. At the same time, process drift is minimized as the reactor wall is staying perfectly clean.

A typical silicon etch rate of a fine-tuned CORE sequence is 15nm/min with a selectivity of ca. 10 towards resist (both DUV and e-beam), ca. 35 for HSQ and SiO_2, and ca. 700 for ALD Al_2O_3. Besides shaping at the nanoscale, by switching on the ICP source the technique also performs for microstructures without the need for further process optimization in between. Therefore, the procedure creates a lot of design freedom and is operator and tool friendly. When the ICP source is used and the platen source is discarded to remove the DC bias, the etch rate can be above 1µm/min and the selectivity can be as high as 200 for SiO_2 masking and low silicon loading.

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Chapter 4. On the formation of Black Silicon in SF_6-O_2 plasma: The CORE sequence and BSi on Demand

This chapter will present a study on the formation of black silicon (BSi) in SF_6-O_2 plasma. In this chapter, different sources that contribute to the formation of BSi are documented and explained. Then a method to prevent and control the onset of BSi is proposed based on the CORE sequence. Due to the self-limiting property of the oxidation step, the formation and controllabilty of BSi in the CORE sequence is different from how BSi presents itself in the FC-based sequences. The effect of different process parameters of the CORE sequence on the creation of masks and formation of BSi are carefully investigated. By manipulating these parameters, it enables the ability to create either BSi-full or BSi-free surfaces independent of the aspect ratio of the etching features.

This chapter is based on the publication: Nguyen, V.T.H., Jensen, F., Hübner, J., Leussink, P. and Jansen, H., 2020. On the formation of black silicon in SF_6-O_2 plasma: The clear, oxidize, remove, and etch (CORE) sequence and black silicon on demand. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 38(4), p.043004.

4.1. Introduction

The topography of silicon surfaces controls many of its physical, chemical and biological properties. Especially texturing at the nanoscale has shown to effectively reduce the reflection of the visible light due to enhanced absorption and scattering. Because of the almost perfect light absorption, this type of silicon has been given the appropriate name of black silicon (BSi) and has found a prominent place in photovoltaic applications[1-4]. The strongly increased surface area has also shown attractive opportunities in chemical and optical devices[5-7]. In addition, another already established characteristic of BSi is its ability to prevent cell growth and as such creates anti-bacterial, anti-fogging and self-cleaning surfaces[8-10].

Even though the appearance of BSi possesses many beneficial features, the formation is considered to be a downside in most MEMS-related applications[11-20]. It is consequently of importance to control the onset and subsequent evolution of BSi to either enhance or reduce its appearance. Therefore, it is helpful to find the root cause of BSi formation and many studies have been devoted to find this. However, the BSi onset is still highly debated and many studies have documented and explained the problem differently. They can be grouped into three main categories:

Fluorocarbon-related sources: (#1) FC deposits from the reactor walls that loose contact and drop particles on the silicon surface[21, 22] and (#2) plasma deposition of the requested FC inhibitor on the etching features, but insufficient removal from the horizontal surfaces by ion impact (puncture convolution) leaving residues[32].

Oxygen-related sources: (#3) oxide participants/clusters/defects/impurities inside e.g. Czochralski Si, (#4) non-volatile SiO_xF_y particles arriving from the plasma as a result of oxidizing SiF_4 reaction products (plasma dust)[20,23-26], (#5) redeposit from sputtered SiO_x that has formed at horizontal Si surfaces, (#6) inhomogeneous removal of the initial native oxide[20,23,27], and (#7) plasma oxidation of the Si surface and insufficient removal by ion impact leaving residues[23,28].

Other sources: (#8) 'Dirty' wafers due to previous process steps (e.g. resist residues or scum)[23], (#9) mask sputtering and subsequent redepositing[23], (#10) non-volatile sulphur compounds (SO_xF_y) formed in the plasma bulk, (#11) AlF_3 particles sputtered from the reactor walls or from the wafer clamp[21,29], (#12) natural roughness of the silicon surface causing self-shadowing[30], and (#13) temperature-dependent amplification of particle diffusion along the surface[31].

It is commonly believed that the formation of BSi is mainly caused by particles unintentionally deposited on a silicon surface or by remaining residues due to an incomplete removal of a passivation layer. Once present on the surface these particles or residues act like tiny masks and locally prevent the silicon from further etching. The evolution of these micromasks into long pointy nanostructures is more pronounced when operating with an anisotropic etch recipe. Most of the self-inflicted masks listed above

can be easily prevented by proper pre-treatments and careful controlling the etch conditions, except for those related to the insufficient bottom removal of the plasma passivation using fluorocarbon (#2) or oxygen (#7) that leaves residues. More specifically, the formation of grass in the FC related processes (#2) is often more pronounced in large open areas than in high aspect ratio structures and is highly time-dependent[32]. The main reason is the larger influx of passivating species in the open areas as will be explained further on.

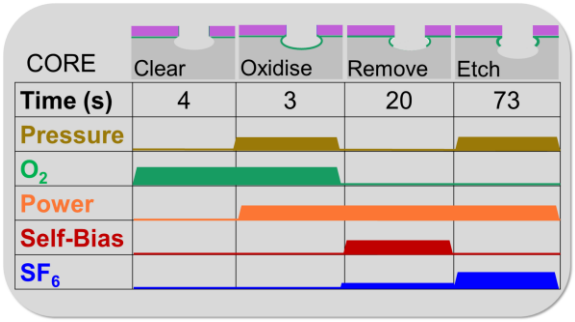
In this study, we replace the conventional Bosch process by a recently developed CORE sequence in which the C_4F_8 passivation cycle is replaced by an O_2 cycle. The oxide thickness at the trench bottom is less dependent on the aspect ratio because the plasma oxidation is experimentally found to be self-limiting[33]. In short, during plasma oxidation the growing oxide film will slow down the oxidation process logarithmically and effectively limit its thickness to about 3nm or less. Consequently, all the horizontal surfaces will be cleared from the passivation in approximately the same R-time. Using CORE, we demonstrate the possibility to control the resilient BSi initiator while keeping the ability to faithfully etch the intended pattern anisotropically. This finding has provided the authors a tool to manipulate and control BSi formation at will and independent of the aspect ratio of the etching features or time, hence it is called 'Black Silicon on Demand'.

4.2. Materials and Methods

Silicon wafers (150 mm Czochralski, n-doped, <100> orientation) are coated with 1.5 µm thick positive photoresist (AZ MiR 701, Merck) using a spin coating system (Gamma 2M, Süss MicroTech). Subsequently, patterns are defined by maskless UV-lithography (MLA150, Heidelberg Instruments), which is a direct writing system with high power laser light source. The exposure dose of 180 $mJ \cdot cm^{-2}$ will result in a resolution of around 600 nm. Then, the wafers are developed in AZ726 MIF (AZ Electronic Materials), rinsed in DI water and dried by spin coating with a gentle nitrogen stream.

To verify the critical dimension of the exposed patterns, the samples are inspected using an optical microscope (Nikon eclipse L200) that allows a measurement resolution of 200 nm. Then, most wafers receive a short descum to remove any surface resist residue (preventing #8). For this, a barrel etcher including a Faraday cage (Tepla 300 Semi-Auto) is used for 10 min at room temperature with 500 sccm O_2 at 1 mbar and 150 W. Subsequently, the samples are cleaved manually into pieces of around 1×1 cm^2 and attached on a 150 mm silicon carrier wafer by a small drop of Galden PFPE fluid (Solvay Solexis SpA). The PFPE fluid is a chemically inert perfluoropolyether vacuum oil with good thermal conductivity. Finally, the etch process is performed in a commercial available plasma etch system (Pegasus, SPTS). After etching, the samples are characterized using a scanning electron microscopy (SEM, Supra V60, Zeiss) that allows for a 10 nm resolution.

The procedure to create directional profiles with BSi on demand is a recently developed 4 steps CORE sequence as schematically shown in Figure 4.1. CORE uses a sequence of sulphur-hexafluoride (SF_6) plasma to etch silicon (the E-step), repeatedly alternated with oxygen (O_2) plasma to passivate the sidewall of the etching features (the O-step). Both steps have a very low bias in order to minimize the mask erosion. The R-step is included after the O-step to remove the passivation layer from the horizontal surfaces completely, but leaving the vertical wall passivation intact. This step operates at a very low pressure to create a high plasma potential that will combine with the DC self-bias to enhance the ion energy for the directional removal. The C-step is less evident, but it is added as a purge step to remove the SF_6 species from the reactor before the O-radicals from the next O-step arrive. Finally, the plasma is solely generated by the platen source (i.e. CCP) as the coil source (i.e. ICP) without a protecting Faraday cage has a substantial risk of generating AlFx particles (thus preventing #11) especially at low pressure.



CORE	C	O	R	E
Time (s)	4	3	20	73
Pressure (mT)	0.8	50	0.2	50
O_2 (sccm)	50	50	0	0
Platen Power (W)	0	10	10	10
DC Self-Bias (V)	0	0	4	0
SF_6 (sccm)	0	0	5	15

Figure 4.1. Typical fine-tuned CORE cycle for nanoscale etching.

4.3. Results and Discussions

4.3.1. Characteristic of BSi in the Bosch and the CORE sequence

The CORE sequence has been shown to enable the etching of nanostructures having straight, smooth sidewalls with low (resist) mask erosion and undercutting[33]. Unlike the Bosch process[34-37], the CORE sequence has no pile-up of inhibitor deposits at the top of etching features. This is because the passivation layer originates from the silicon oxidation has a limited thickness as the growing silicon dioxide acts as a diffusion barrier. This feature makes the procedure outstanding for high aspect ratio or nanoscale directional etching. In addition, the bottom appears either everywhere clean (i.e. smooth inside high aspect ratio features as well as in the large open field area) or everywhere roughened. To study this atypical BSi formation behaviour, this section focusses on the onset of BSi formation in high aspect features and open field areas. The main difference between the FC- and O-related sequences on how the deposition mechanism affects the overall BSi formation will be explained next.

As illustrated in Figure 4.2, the directional sequence can be separated into three basic steps: passivation with FC or O species (left), removal of this layer using an ionic flux

(middle) and silicon etching using F-radicals (right). All three steps have their own aspect ratio dependent characteristics. For example, during the Bosch deposition step (Figure 4.2a1), the arrival cone of the FC species is smaller in high aspect ratio features than in the open field area due to neutral shadowing[38]. This leads to 'deposition lag' as the incoming species hit and stick, which means that the open field area will accumulate more deposits than the high aspect ratio features. The next step, the R-step, is controlled by the directional ion flux and therefore the removal rate will slightly depend on the ion angular distribution (IAD)[38-40]. In this step, the pressure is so low that it will limit collisions inside the dark space, thus prevent broadening of the IAD. In addition, a low pressure will raise the electron temperature and consequently raises the plasma potential[41]. This in turn will increase the ratio of the directed ion energy gained in the sheath to the random ion energy in the plasma, resulting in a sharper IAD[42]. Therefore, the R-step is considered to be less dependent of the aspect ratio. As a result, exactly after the FC layer at the bottom of high aspect ratio features is totally removed, there are still some residues remaining in the open field area (Figure 4.2a2). This FC residue will initiate BSi when the time to undercut these residues in the next E-step is too short (Figure 4.2a3). The E-step is, like the deposition step, highly aspect ratio dependent due to Knudsen transport limitations causing depletion. It means that in the free molecular regime, random reflections of the passivated sidewalls will increasingly restrict the number of etching species to reach the bottom. This is the mechanism behind the well-known RIE lag.

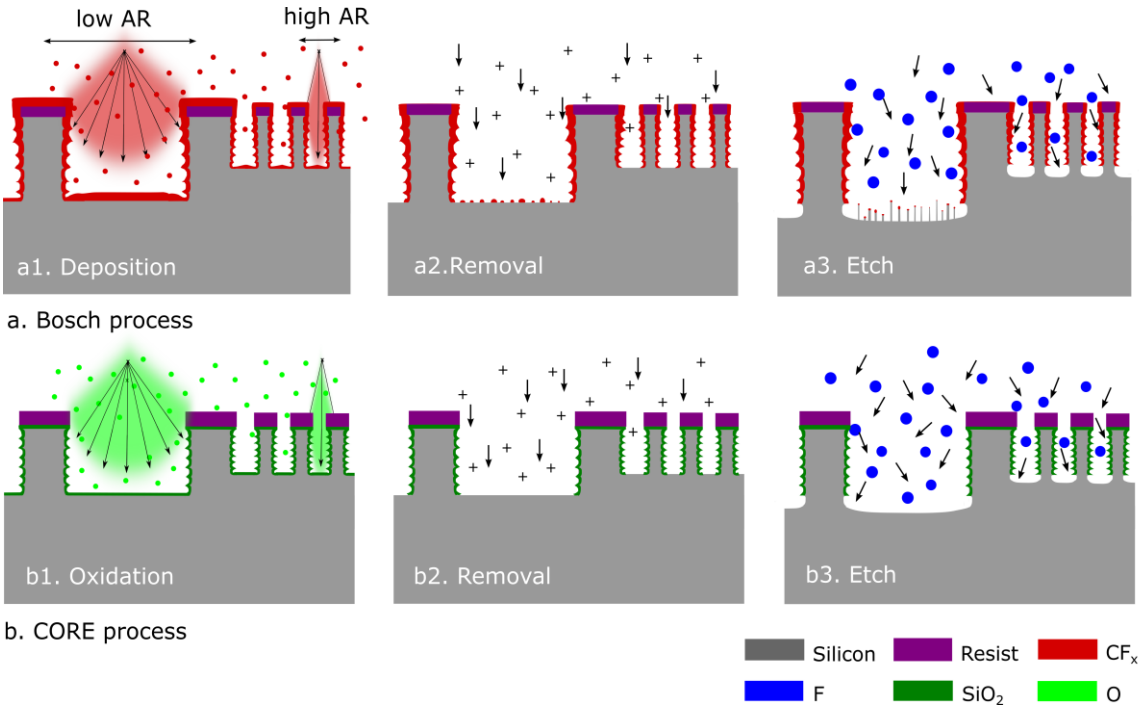


Figure 4.2. Schematic illustration of BSi formation in the Bosch process (a) and BSi-free CORE process (b).

In contrast, the plasma oxidation process of the CORE sequence is self-limiting (Figure 4.2b1). This characteristic allows the oxide layer to grow with almost the same thickness everywhere either in the high aspect ratio areas or in the large open field areas. The oxide layer in the open field areas is always a little bit thicker than inside high aspect ratio features. However, the difference in absolute thickness will be less when the oxidation time increases due to the logarithmic film growth. Therefore, the deposition lag associated with the Bosch process is virtually not present in the CORE process. As a result, in the upcoming R-step (Figure 4.2b2) being also almost independent of the aspect ratio, all passivation at the horizontal surfaces will be cleared almost at the same time independent of the aspect ratio. Figure 4.3 is an illustrative demonstration of Figure 4.2 to highlight the difference between the Bosch and CORE process on the formation of BSi. Two samples with increasing line widths were etched to almost the same depth (4 µm) using the Bosch and CORE process respectively. It can be seen that with the Bosch process, there is BSi formation in the large open field area due to surface residues while the bottom surface is clean in the high aspect ratio features. This aspect ratio dependent phenomenon usually does not show up as strong in case of the CORE process in which the etch sample has a clean and smooth bottom surface everywhere (Figure 4.3b).

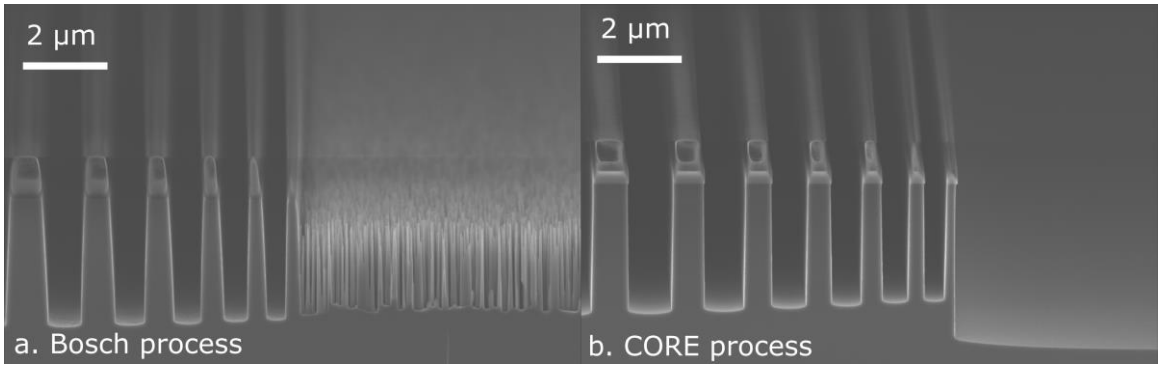


Figure 4.3. Samples etched using (a) the Bosch process result in clean bottom in high aspect ratio features and BSi in the large open field areas, while (b) the CORE process result in a clean and smooth bottom everywhere.

Although the CORE sequence has been developed for BSi-free applications, it is also possible to modify the recipe to create BSi for other applications such as solar cells. This request can be addressed due to the flexibility of the CORE parameters. It is noticed in Figure 4.1 that there are four distinct steps in the CORE sequence and parameters in each step can be changed independently to investigate the formation of BSi. The advantage of using the CORE sequence is that we can combine different parameters to control when surface roughening occurs, and then manipulate the parameters to either enhance or suppress the BSi appearance. In this study, the BSi formation will be investigated by first taking the most straightforward technique by limiting the R-time to ensure that not all the passivation at the horizontal surfaces is removed after the ion bombardment. After that, other options will follow.

4.3.2. The effect of R-step on the formation of BSi

To create the requested directionality with smooth surface and reasonable mask selectivity, the removal time is adjusted typically to be just enough to clear away the oxide layer on the horizontal surfaces. But, if the removal time is too short, residues will still remain at random spots on the bottom surface and act as micromasks. In the subsequent E-step, and assuming the etch time to be too short to fully undercut the self-inflicted micromasks, local roughness in the silicon will initiate and strengthen further in the upcoming cycles, until sharp needle-like structures (BSi) appear. This formation mechanism is explained in more detail in Figure 4.4.

In the first row (Figure 4.4a-d), where the E-step time is taken quite long (73s), it is observed that the R-time of 15s is sufficient to prevent BSi (Figure 4.4a and b). In case of shorter R-times (Figure 4.4c and d), the removal and undercut is insufficient and larger oxide residues will remain. It is also noticed that when BSi appears (Figure 4.4c and d), the resist mask is considerably more undercut than when BSi is absent (Figure 4.4a and b). The reason is that when BSi is formed, the etch rate will drastically slow down and less fluorine will be consumed. Consequently, the fluorine pressure is getting higher and thus will erode more the sidewall of the etching feature. The same happens when the E-time is shortened to 35s, as shown in the second row (Figure 4.4e-h). However, in this case the R-time of 15s (Figure 4.4f) is not enough to prevent BSi as the undercut is shorter and smaller oxide residues will able to remain at the surface area. It is noted in this case, just like the Bosch process (Figure 4.3a), that the open field structures are more likely to form BSi. This is because in this experiment we only use 3s for the O-step which is not yet operational in the self-limiting regime as shown in our previous study[33]. Therefore, the open field areas will have a little more passivation and are more likely to develop grass when the R-time is restricted. Again, the formation of BSi in the open field will raise the fluorine pressure and therefore we observe a faster etch rate in the high aspect ratio features as these are virtually free of oxide residues. Finally, in the last row (Figure 4.4i-l), where the E-time is shortest (15s), BSi is present even for the longest R-time of 20s. Remarkably, in this case (Figure 4.4i) BSi only appears in the higher aspect ratio features while the open field is free of BSi. This time the reason is believed to be caused by Knudsen restrictions of the fluorine species inside the high aspect ratio features that limits the etch rate and undercutting locally, thus preventing very small oxide residues from undercutting. Therefore, in order to get the best BSi-free etch performance with a minimum of undercut, it is important to make sure that the passivation is removed from all the horizontal surfaces.

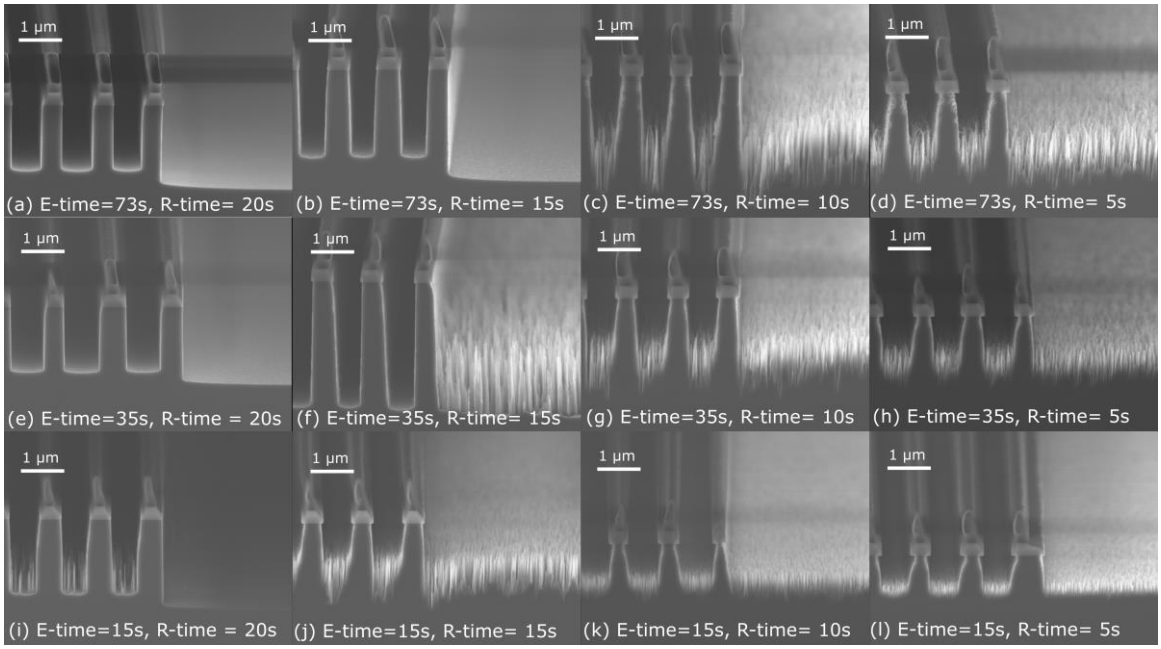


Figure 4. 4. The effect of decreasing R-time on the formation of BSi. C-time is 4s and O-time is 3s.

From the previous experiment and discussion we can conclude that the R-time of 20s is not enough to clear all the oxide residues since Figure 4.4i proves that some very small oxide residues have survived. Therefore the R-time is increased further as shown in Figure 4.5. When the E-time stays at 15s, like Figure 4.4i, but the R-time is increased to 25s (Figure 4.5a), the grass indeed disappears. However, decreasing the E-time further to 5s and keeping the R-time at 25s (Figure 4.5b) is again developing grass as the tiniest oxide residues survive the ultrashort undercut. Finally, increasing the R-time to 30s at 5s E-time (Figure 4.5c) is also removing these tiny leftovers and all the surfaces become smooth.

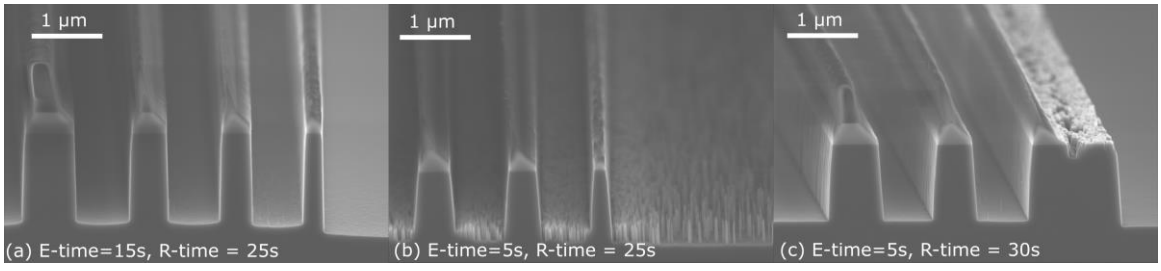


Figure 4.5. The relation between R-time and E-time on the formation of BSi. C-time is 4s and O-time is 3s.

4.3.3. The effect of E-step on the formation of BSi

The E-step seems to have no direct contribution to the formation of surface residues as it basically only etches silicon isotropically. However, when oxygen is added in the E-step

(as usual in mixed mode RIE) and causing an intimate contact between the etching and passivating species, BSi is formed. The main reason is believed to be due to a competition between oxygen and fluorine radicals to react with silicon surface atoms. Some areas will be oxidised and stop etching while other areas are fluorinated and continue to etch. This will cause initial surface roughening. In subsequent steps, this roughness will further enhance to BSi because of the directionality provided by the R-step. Another possibility to form BSi by mixing SF_6 with O_2 during silicon etching is that the SiO_2 plasma dust is created[26]. These dust particles might settle on the silicon surface and form micromasks. However, the presence of plasma dust has not been verified and therefore we will ignore this mechanism in this section. Anyways, BSi is clearly enhanced by mixing SF_6 with O_2.

Figure 4.6 shows the result after adding 5, 10 and 15sccm of O_2 into the E-step. In the first row, when E-time is at 73s, there is no BSi appearing regardless of the amount of O_2 added into the E-step. Seemingly, the long etch time is sufficient to undercut all the micromasks and therefore prevent the evolution of BSi. Nevertheless, with the presence of O_2 content, the bottom is getting rougher as the oxygen radicals compete with the fluorine radicals to oxidize the silicon randomly. Furthermore, it is noted that when the amount of O_2 in the E-step increases, these species will inhibit the etching process increasingly and making it more difficult for the fluoride radicals to penetrate the oxide layer and to react with the silicon. Therefore, the etch rate lowers and the etch profiles become more positive (Figure 4.6a-d). Since the etch rate gets lower, the fluorine pressure will raise and as a result, the lateral etching (undercut) is more pronounced. The same principle applies for 35s and 15s E-time (Figure 4.6e-l), but in these cases BSi appears as the micromasks are big enough to survive the lower undercut. The shorter the E-time, the lower the undercut and the easier it is to get BSi. It is also observed that BSi is more pronounced in the open field areas. The reason is because the micromasks responsible for BSi is probably caused by the local oxidation from the arriving oxygen radicals and thus, have a tendency to form more in the open field areas than in the high aspect ratio structures. This is just like the deposition lag mechanism that has been found to be responsible for the BSi formation in the Bosch process (Figure 4.2a). Therefore, even though the method of adding O_2 into the E-step can create BSi, it is not what we aim for. BSi formation is not uniform as more BSi appears in the large open field area than in the high aspect ratio structures.

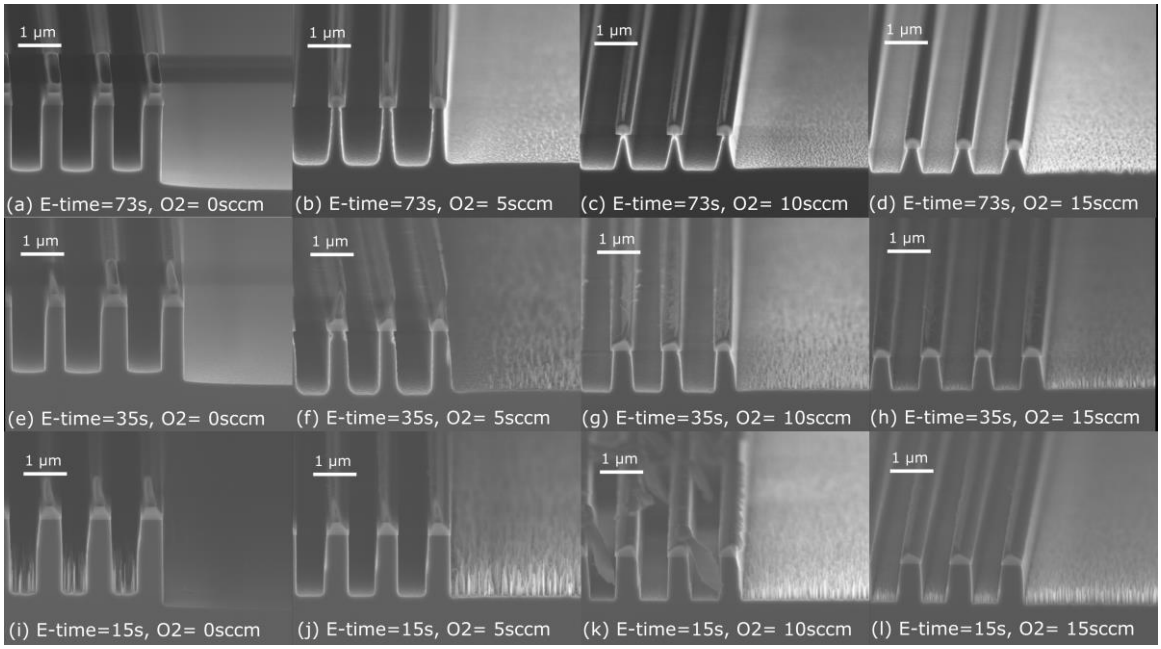


Figure 4. 6. The effect of adding O2 into the E-step. C-time is 4s, O-time is 3s and R-time is 20s.

4.3.4. The effect of O-step on the formation of BSi

Another option to manipulate BSi formation is changing the O-step. During the O-step, the F-terminated silicon surface created during the earlier E-step will be replaced by the O-terminated silicon surface. This plasma oxidation process is essential to enable the anisotropic etching. More to the point, oxide growth slows down logarithmically once it is formed and becomes self-limiting when roughly 3nm SiOx passivation has grown[33]. The latter means that at the longer oxidation times, all surfaces tend to have exactly the same protective layer thickness independent of the aspect ratio. For the shorter O-step times, though, the limitation is not yet completed and the open areas will have more passivation than the high aspect ratio features and can result in BSi when the R-step is insufficient (as previously observed in Figure 4.4f). Therefore, in order to have BSi formation on all locations, the O-step time should be enough to form an almost identical layer on any topography. The higher the differences in aspect ratio, the longer O-time is needed to ensure that the self-limiting regime is reached.

4.3.5. The effect of C-step on the formation of BSi

The last option to manipulate BSi formation we studied is the change in C-step. As already introduced in the method section, the C-step is included to prevent the SF_6 plasma from the preceding E-step to come into contact with the O_2 plasma in the next O-step. Although the SF_6 flow has stopped in this step, the SF_6 gas still has a certain residence time in the reactor. For example, for a plasma volume V= 3l with a flow Q= 15sccm (~ 25Pa·l/s) and a pressure p= 50mT (~7Pa) the residence time is about t_{res}= V×p/Q = 1s[18].

If there is no such C-step, the O-step will contain SF_6 that allows for etching and passivation happen at the same time. Consequently, the passivation layer becomes weaker and therefore the etch profile is strongly eroded and undercut (Figure 4.7a and b). This undercutting will prevent BSi formation even though micromasking might be present. Decreasing the etch time to 35s and 15s (Figure 4.7c and d) will help to reduce the erosion of the structures sidewall as expected. The profile looks great without undercut and does not form BSi. The observation that no BSi is formed when the E-time is very short and the C-time is omitted (Figure 4.7d) makes us to believe that the CORE cycle does not generate plasma dust that could have initiated BSi. In conclusion, this method has failed to create aspect ratio independent BSi and is consequently not suited for BSi on demand.

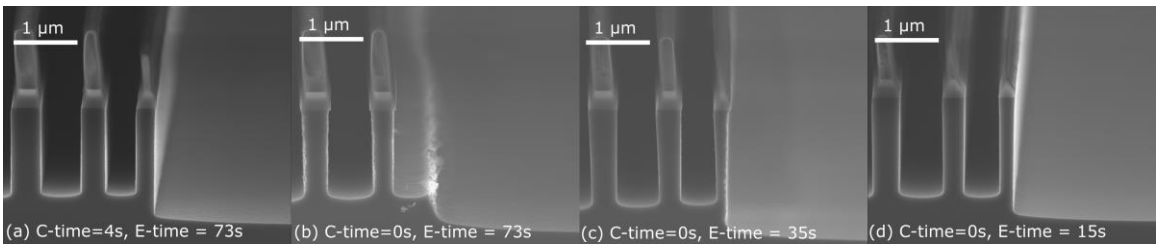


Figure 4.7. The effect of decreasing C-time on the formation of BSi. O-time is 3s and R-time is 20s.

4.3.6. Black silicon on demand

We have demonstrated in the previous sections the freedom to tune parameters of the CORE sequence to uniformly create BSi-free or BSi-full surfaces. For the BSi-free recipe, the etch process should follow the fine-tuned parameters listed in Figure 4.1 (or an adapted version arrived from the results shown in Figure 4.4 and 4.5). This ensures the etch profiles always have clear and smooth bottom surfaces, both in the high aspect ratio structures and open field area. With respect to the BSi-full recipe, it is shown that there are several ways to modify the CORE parameters for the generation of BSi. However, the most easy and straightforward way is to decrease the removal time in the R-step. This approach facilitates the existence of micromasks everywhere independent of the aspect ratio, which then further evolve into BSi.

Figure 4.8a shows silicon pillars having 1 µm diameter that are etched with a BSi-free recipe. The structures are smooth and directional. By combining BSi-free and BSi-full recipes sequentially interesting features can be created. Figure 4.8b is an example of silicon pillars etched first with a BSi-free recipe and then continued with a BSi-full recipe. This combination results in high aspect ratio pillars with BSi coverage at the bottom. By removing the mask on top of the pillars, the BSi can be formed on top of the these pillars as well (Figure 4.8c-h). This proves that the CORE sequence has the ability to form BSi everywhere, either at the bottom of high aspect ratio features or on top of it (the latter resembles an open field feature). It can be observed that, regardless the dimension of the design, the bottom of the etched features always have the same property, which is either

clean and smooth (Figure 4.8a), or with BSi everywhere (Figure 4.8c-h). This advantage outperforms the CORE process over other RIE techniques like the DREM or Bosch process. The latter having the tendency to grow more grass in the open field areas than inside the high aspect ratio features.

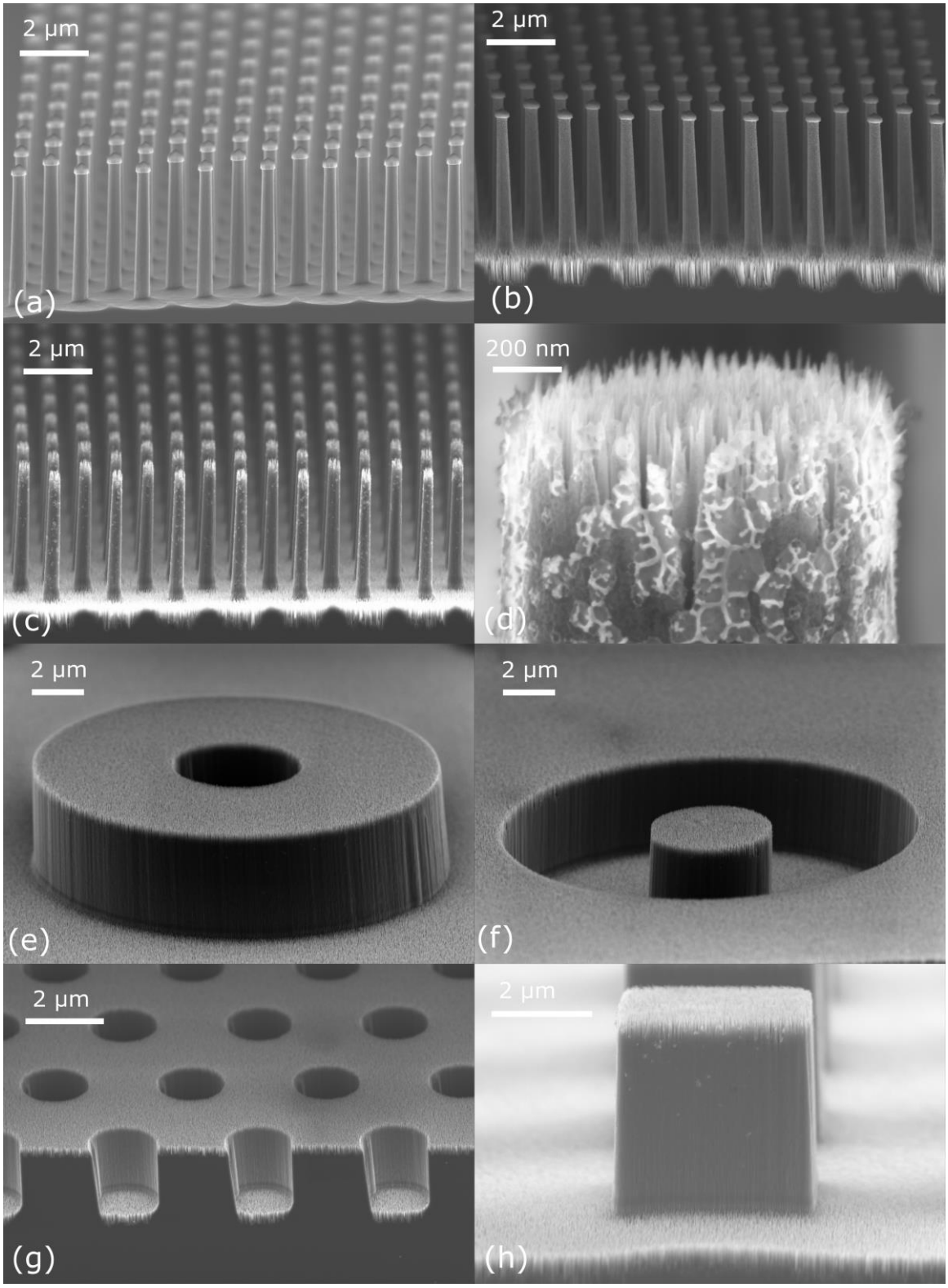


Figure 4.8. Silicon pillars etched with (a) BSi-free recipe, (b) BSi-free recipe followed by a BSi-full recipe. And (c-h) the same double etch process, but the mask is stripped in between.

4.4. Conclusions

This study is built on the CORE sequence which has been introduced in chapter 3. Due to the self-limiting property of the oxidation step, the formation and controllabilty of BSi in the CORE sequence is different from how BSi presents itself in FC-based sequences. The effect of different process parameters on the creation of masks and formation of BSi have been carefully investigated. It is concluded that the CORE sequence is able to create BSi or micrograss at will and there is a strong relationship between the R-time and E-time on its formation. The usual function of the R-time is to remove any surface passivation while the E-time should undercut possible leftovers. This will result in smooth surfaces. However, if we restrict the R-time to leave oxide residue and use an E-time short enough to prevent undercut of this residue, BSi will develop. The advantage of this method and using the CORE sequence is that BSi is created with the same properties everywhere: it covers horizontal surface either in and on top of high aspect ratio structures or in large open field areas. The latter distinguishes the BSi formation clearly from other directional processes such as the Boch process. The proposed CORE process thus provides the authors a versatile tool for creating BSi anywhere at anytime or - as we call it - ‘BSi on Demand’.

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Chapter 5. Ultrahigh aspect ratio etching of silicon in SF_6-O_2 plasma: The CORE sequence and chromium mask

This chapter will present a procedure to fabricate ultra-high aspect ratio (HAR) silicon pillars using chromium mask and the CORE sequence. First, the effect of different CORE parameters (e.g. O-time, R-power, and E-pressure) on the etch rate and profile are carefully investigated and optimized with respect to low mask undercut, smooth sidewall and high directionality. In addition to the CORE parameters, we also examine the effect of total etch time on the evolution of ultra-HAR silicon pillars. Then based on the gained knowhow, the CORE recipe is fine-tuned to get ultra-HAR features with straight and smooth sidewalls. Finally, the retraction of chromium mask in SF_6/O_2 plasma and the effect of carrier wafer on the etch rate will be discussed.

This chapter is based on the publication: Nguyen, V.T.H., Shkondin, E., Jensen, F., Hübner, J., Leussink, P. and Jansen, H., 2020. Ultrahigh aspect ratio etching of silicon in SF_6-O_2 plasma: The clear-oxidize-remove-etch (CORE) sequence and chromium mask. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 38(5), p.053002.

5.1. Introduction

The importance of anisotropic etching dates back to the introduction of semiconductor fabrication in the early 1970s to increase device density. In particular, the need for high aspect ratio (HAR) etching (say AR>10) has been of interest for the semiconductor industry to enable trench DRAM capacitors, trench MOSFET isolation, or FinFETs. The aspect ratio is defined as the depth of a trench/hole or height of a plate/pillar divided by its width/diameter. In addition to large scale integrated circuit manufacturing, HAR structures are increasingly requested in applications such as biological or chemical sensors[1-4], electronic devices[5-7], energy conversion and solar cells[8-9], photon-absorbent surfaces[10], confined phonon or photonic devices[11-12] and quantum-based devices[13]. The success of HAR etching depends on controlling the lateral etch rate while keeping or enhancing the vertical etch rate. In general, wet chemical etching is not suitable for HAR fabrication due to sloped walls and/or severe mask undercutting (with the notable exceptions of metal assisted chemical etching or <110> single crystalline silicon etching)[14-18]. Instead, dry plasma etching has proven to faithfully transfer the requested mask pattern into the underlying silicon[19-28]. The maximum ratio between the vertical and horizontal etch is mostly depending on the directionality of the incoming ions, so the ion angular distribution function (IADF) is an important plasma parameter to consider in HAR etching. Modern HAR processes tend to minimize the reactor pressure and increase the self-bias during the etch process as this sharpens the IADF even though this compromises mask selectivity.

In this chapter, a simple, reliable and reproducible procedure is developed to fabricate ultra-HAR nanofeatures using the CORE sequence[29-31]. It is related to the conventional mixed mode plasma etching in which SF_6 and O_2 are inserted simultaneously[32-34], but this time the gases enter the reactor sequentially. The effect of different CORE parameters (e.g. O-time, R-power, and E-pressure) on the etch rate and profile are carefully investigated and optimized with respect to low mask undercut, smooth sidewall, high directionality, and ultra-HAR ability. Since CORE uses a switching sequence of SF_6 and O_2 plasma, it has limited selectivity towards the usual photoresist mask. Therefore, in order to have sufficient selectivity that enables ultra-HAR etching, chromium is utilized as a mask. However, it is known that chromium is damaged (or etched) when exposed to plasma ash systems and O_2 is a basic ingredient of the CORE sequence[35-38]. Therefore, a further task of this study is to find the limits of ultra-HAR etching using chromium as a hard mask.

5.2. Materials and Methods

The procedure to sculpture ultra-HAR structures uses the following cleanroom processes. First, resist patterns are created using DUV stepper lithography (200nm dots, 400nm periodicity) or electron-beam (e-beam) lithography (60nm dots, 500nm periodicity).

Subsequently, the stepper BARC layer or e-beam residue is removed with plasma oxygen. Then, chromium is deposited and lift-off is performed. The chromium is easily integrated in standard semiconductor process flows because it can be stripped conveniently using plasma ashing tools. Finally, the silicon is etched using the CORE sequence and the samples are characterized using a scanning electron microscopy (SEM, Supra V60, Zeiss) that allows for a 10nm resolution. The details of the process flow are described below.

Stepper: Silicon wafers (150mm diameter Czochralski, 675µm thick, 5-10Ωcm phosphorous-doped n-type, <100> orientation) are coated with 65nm BARC (DUV42S-6) and 360nm DUV resist (KRF 230Y) using a spin coating system (Gamma 2M spin-coater, Süss MicroTech). Then, pillar patterns are defined by a DUV stepper (FPA-3000EX4, Canon) equipped with a 248 nm KrF excimer laser. The exposure dose is 86mJ/cm^2. Then, the wafers are developed in 2.38% Tetra-Methyl-Ammonium-Hydroxide in water (AZ726 MIF, AZ Electronic Materials), rinsed in DI water and spin dried with a gentle nitrogen stream. Finally, the BARC layer is etched using a RIE system providing oxygen plasma.

E-beam: For nanosized patterns between 30 and 100nm, a 100kV e-beam writing system (JEOL JBX-9500FSZ) scanning with 10nm steps is used. Positive tone e-beam resist ZEP520A (ZEON) having a thickness of 145nm is spin-coated for 60s at 4000rpm followed by a bake for 3min at 180°C. During exposure the electron current is set at 12nA with 10nm spot size and dose between 293µC/cm^2 (30nm lines) and 263µC/cm^2 (100nm lines). Exposed samples are developed for 180s with ZED-N50 (n-amyl acetate) and rinsed with isopropanol alcohol (IPA). Then, the wafers receive a short descum to remove any surface resist residue. For this, a barrel etcher including a Faraday cage (Tepla 300 Semi-Auto) is used for 10min at room temperature with 500sccm O_2 at 1mbar and 150W.

Chromium deposition and lift-off: After photoresist patterning and BARC removal, the deposition of 30nm or 60nm chromium is performed using a conventional e-beam evaporator (Temescal FC-2000, Ferrotec). The deposition rate is kept at 5Å/s and the base pressure at 10^{-6}Torr. The lift-off is done by placing the wafers into an ultrasonic bath containing N-Methyl-2-N-Pyrrolidone (NMP, Remover 1165) for a few minutes, following 5min rinse in IPA. The lift-off from DUV stepper patterned wafers becomes a more complicated procedure, since Remover 1165 can not dissolve photoresist properly, probably due to chromium deposition on the sidewall of the positive tone DUV polymer. The problem is solved by placing the wafer into a beaker containing 250ml deionized (DI) water and adding 500ml sulphuric acid (H_2SO_4). The solution develops heat and the lift-off eventually succeeds leaving only a hard mask pattern attached to the silicon substrate. After 10min the wafer is taken out and properly rinsed in DI water. Finally, to verify the critical dimension of the retrieved patterns, the samples are inspected using an optical microscope (Nikon eclipse L200) that allows a measurement resolution of 200nm.
Silicon etching: After lift-off, the samples are cleaved manually into pieces of around 1×1cm^2 and attached on a 150mm silicon carrier wafer by a small drop of Galden PFPE

fluid (Solvay Solexis SpA). The PFPE fluid is a chemically inert perfluoropolyether vacuum oil with good thermal conductivity. Finally, the etch process is performed in a dual source plasma system (DRIE Pegasus, SPTS) operating in the RIE mode (i.e. no ICP power). The schematic illustration of the SPTS Pegasus system is shown in Figure 5.1. The system has been dedicated for SF_6/O_2 based plasma etching solely and has no prior FC history. This FC-free chamber is needed to ensure the absence of any contamination or influence on the fragile oxygen plasma oxidation that is required for the CORE sequence.

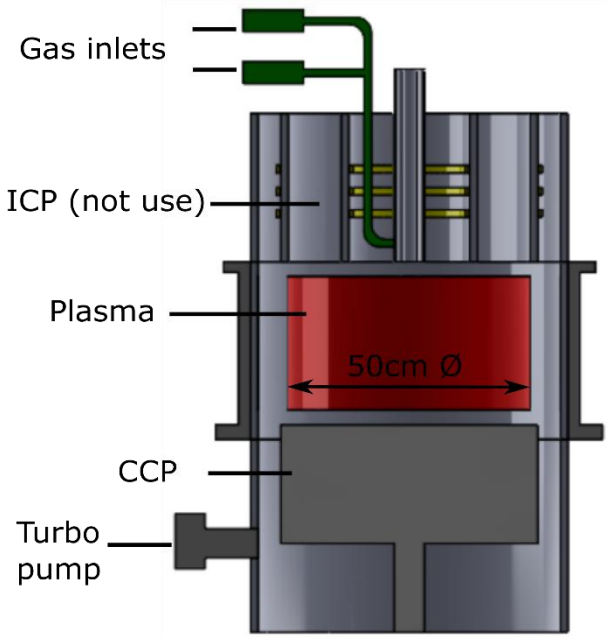

Figure 5.1. The schematic illustration of the SPTS Pegasus etch system

5.3. Results and Discussions

The procedure to create ultra-HAR nanostructures is based on the recently developed four steps CORE sequence as schematically shown in Figure 5.2. It uses a sequence of sulphur-hexafluoride (SF_6) plasma to etch silicon (the E-step), repeatedly alternated with oxygen (O_2) plasma to passivate the etched features (the O-step). Both steps operate at a relatively high pressure above 20mTorr to ensure low mask erosion. The extra R-step uses ion energy at a very low pressure (0.2mTorr) to ensure a high directionality. It is included after the O-step to remove the passivation layer on horizontal surfaces, but leaving the vertical wall passivation intact. The C-step is added to flush the reactor from remaining SF_6 gas and SiF_4 reaction products. Finally, the plasma is solely generated by the RIE (i.e. platen) source as the ICP source without a protective Faraday cage has a substantial risk of generating AlF_x particles.

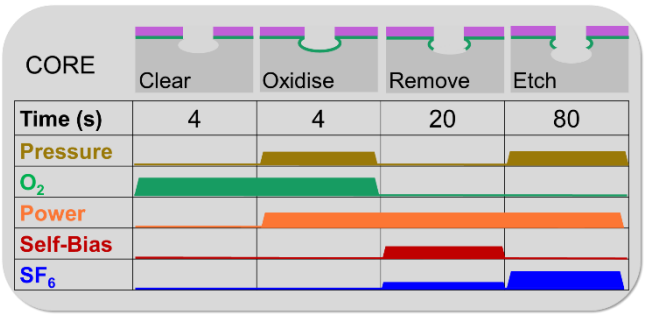

Figure 5.2. The schematic illustration of the CORE sequence.

In the following sections, the effect of different CORE parameters on the etch rate and profile is investigated using the initial CORE recipe shown in Table 5.1, including a guideline to tune nanoscale pillar arrays for ultra-HAR.

Table 5.1. The initial CORE recipe to study ultra-HAR silicon nanoscale etching.

CORE	C	O	R	E
Time (s)	4	4	20	80
Pressure (mT)	0.8	50	0.2	24
O_2 (sccm)	50	50	0	0
Platen power (W)	0	10	18	15
DC Self-bias (V)	0	0	32	0
SF_6 (sccm)	0	0	5	10

5.3.1. The effect of O-parameters

In the CORE sequence, oxygen is used instead of FC to protect the silicon sidewall during etching. Therefore, the effect of oxidation (O-) power P_O and time t_O on the etch profile is investigated. First, the O-power is increased from 10 to 20W while keeping other parameters in Table I fixed. When the O-power is at 10W (Figure 5.3a) the etch profile is deeper with stronger undercut at the top part compared to 15W (Figure 5.3b) and 20W (Figure 5.3c). Meanwhile, the chromium mask is eroded independent of the O-power at a rate of ca. 2nm/hr. This is because the produced bias and plasma potential during the O-step is too low to have a noticeable effect on the mask erosion rate. There is a strong undercut at 10W as the oxygen plasma is believed to be too weak to completely protect the sidewall from the attack of fluorine radicals during a comparatively long E-time in the CORE cycle. Above 15W, the profile and undercut have no noticeable improvement. This might be because at 15W the oxygen plasma is already fully dissociated. Therefore, in order to further increase the sidewall protection and reduce the mask undercut, the oxidation time t_O is increased from 4s to 8s (Figure 5.3d). However, the consequence of

longer oxidation time is that the profile becomes positive, which restricts the fabrication of ultra-HAR structures.

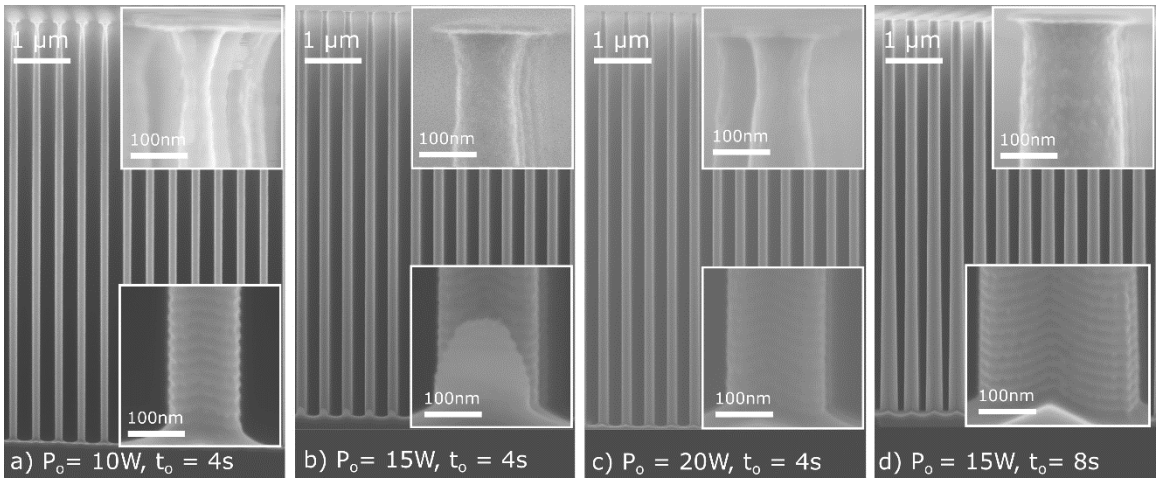

Figure 5.3. Effect of changing the O-power (a, b, and c) and time (d) on the etch profile.

5.3.2. The effect of R-parameters

In order to make the etch profile in Figure 5.3d straight, the removal power (P_R) and time (t_R) are varied. As shown in Figure 5.4, when P_R is increased from 18W (Figure 5.4a) to 22W (Figure 5.4b) the profile straightens. The produced DC bias at 18W and 22W are 32V and 48V, respectively. When the DC bias increases, it will sharpen the ion angular distribution (IAD). Thus, most ions will bombard the bottom of the features resulting in a straight profile. Furthermore, the erosion rate is 2nm/hr at 18W and 2½nm/hr at 22W, so it scales almost linearly with R-power. Consequently, the selectivity towards silicon decreases from 450 (P_R=18W) to 370 (P_R=22W). To improve the selectivity, one might opt for a shorter R-time as shown in Figure 5.4c, where t_R is decreased from 20 to 16s. Indeed the selectivity improves to 400, but the profile becomes positive again. So both higher power or longer removal time will straighten the profile, but will also erode the chromium mask faster. Therefore, it is important to limit P_R and t_R to be just enough to straighten the profile in order to preserve the mask as much as possible.

5.3.3. The effect of E-parameters

A basic part of the CORE sequence is the etching (E-) step. In this step SF_6 gas is inserted into the reactor and transformed into plasma with the aid of a 13.56MHz radio frequency (RF) platen source. Before the effect of the E-parameters is going to be discussed, a few plasma concepts will be highlighted in order to understand the observed behavior.

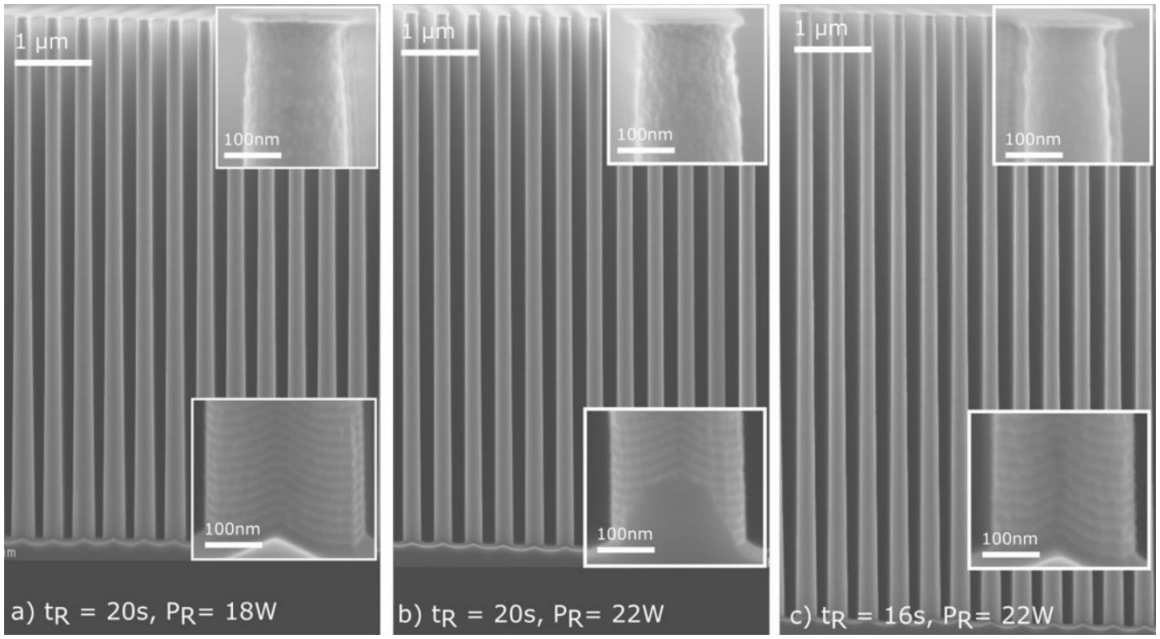

Figure 5.4. Effect of changing the R-power (a, b) and time (c) on the etch profile.

Prominent constituents of the plasma are the electrons, ions, radicals and photons. The electrons are accelerated by the platen power and consequently gain large amounts of kinetic energy (expressed by the electron temperature T_e), but sooner or later will inelastically collide with SF_6 molecules and producing many species by dissociation, ionisation, attachment and excitation[39, 40]. When an electron collides 'soon' with an SF_6 molecule, it can only excite the molecule which gives the plasma its characteristic glow. If the electron is able to escape an early collision, its kinetic energy might be high enough to dissociate an SF_6 molecule and create F radicals. The latter F radical is responsible for the etching following the reaction $Si+4F \rightarrow SiF_4$. If the electron collides 'later' and gains energy beyond several electron volts, the collision will cause ionisation such as $e^-+SF_6 \rightarrow 2e^-+SF_5^+$+F. The extra electron is needed to sustain the plasma as it will trigger a cascade reaction of additional electrons. Even though the electron temperature T_e (eV) is the main drive underneath the etch process, the common parameters to vary are the (platen) power P_E (W), SF_6 flow Q_E (sccm) and the process pressure p_E (mTorr). Therefore, it is important to predict how these parameters affect T_e. In a previous study it has been found for a fairly identical plasma system that the etch rate has a maximum when the following relation between P, Q and p is met: i) the flow is set for 0.2sccm per W and ii) the pressure is set for 0.15mTorr per sccm[41]. So, if a power of 15W is selected, then the highest etch rate is found at 3sccm and 0.45mT. When the flow is lower, for example 2sccm, there is not enough SF_6 available to produce the highest possible active fluorine concentration out of the supplied power. This is called the flow-limited regime where additional power has minor effect on the etch rate. In contrast, when the flow is increased to 6sccm, not sufficient energy is available to break all the bonds and a lot of incoming

SF_6 gas is unused. This is the power-limited regime where additional flow has almost no influence on the etch rate.

E-power

First, the SF_6 flow rate is fixed at 15sccm and the valve position is fixed at 2%. This corresponds to a process pressure of 36mTorr. Then, the plasma power P_E is increased from 10 to 20W as shown in Figure 5.5. The power increase is in the range of the power-limited regime. Therefore, as expected, the pillar height increases almost linearly with increasing plasma power, i.e., 5.0µm at 10W, 6.6µm at 15W, and 8.8µm at 20W. Since the R-step is fixed, the mask erosion rate is not affected. Therefore, the Cr/Si selectivity will increase linearly with increasing power. However, there is a difference in the etch profile when the plasma power increases. At 10W the etch profile is positive (Figure 5.5a) while at 15W it becomes straighter (Figure 5.5b) and even more so at 20W (Figure 5.5c). Furthermore, the higher the plasma power the stronger the lateral etch and mask undercut. This is a direct consequence of the increased fluorine pressure that erodes the fragile oxide sidewall and making the pillars thinner. As a result, the ultra-thin pillars (AR≈200) tend to collapse and stick together while performing SEM imaging as observed in Figure 5.5c. This collapse during SEM imaging can be prevented by scanning the electron beam along the pillar direction instead of perpendicular. It is an interesting topic and deserves more attention, but 'electronic pillar actuation' is besides the focus of this study.

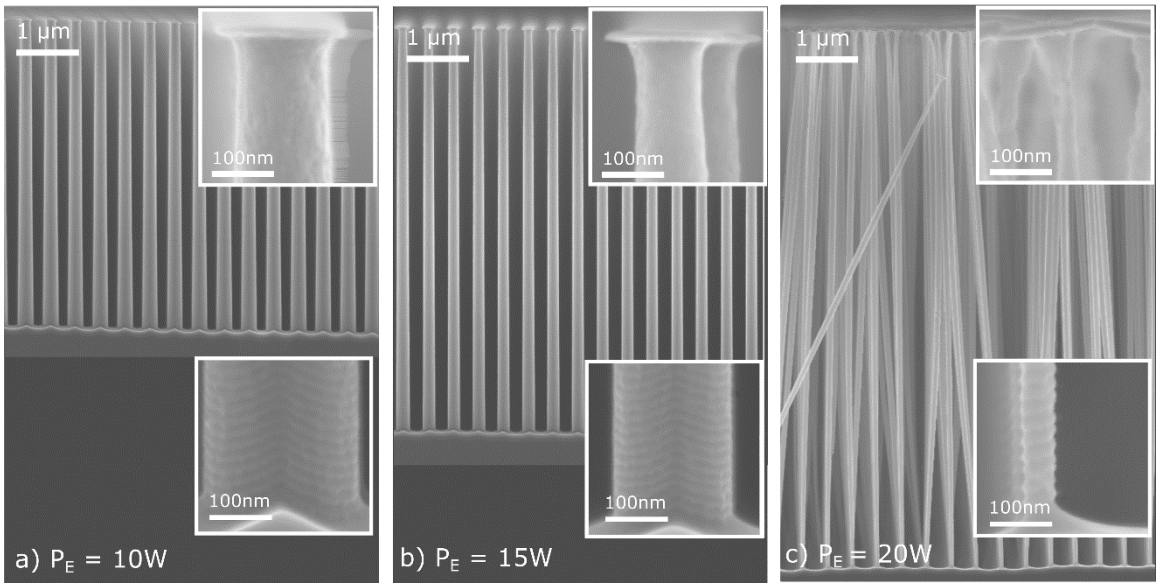

Figure 5.5. Effect of changing the E-power on the etch profile at 15sccm SF_6 flow and 2% valve (and 36mTorr).

E-pressure

Next, both the SF_6 flow (10sccm) and the plasma power (15W) are fixed and the pressure p_E is increased by closing the valve between 2% (24mT) and 1% (54mT). It is observed in Figure 5.6 that the etch rate decreases with increasing pressure and the etch profile becomes more positive. The etch rate decreases because at a fixed plasma power, the increased pressure will increase the number of collisions between electrons and SF_6 molecules (the so-called collision frequency). Because the plasma is operating in the power-limited regime, the higher collision rate will lower the electron temperature T_e. This will result in less dissociation of SF_6 molecules and consequently, the etch rate will decrease. Again, the mask erosion is not affected as the R-step is unchanged. Thus, the selectivity will be lower when the pressure is increased.

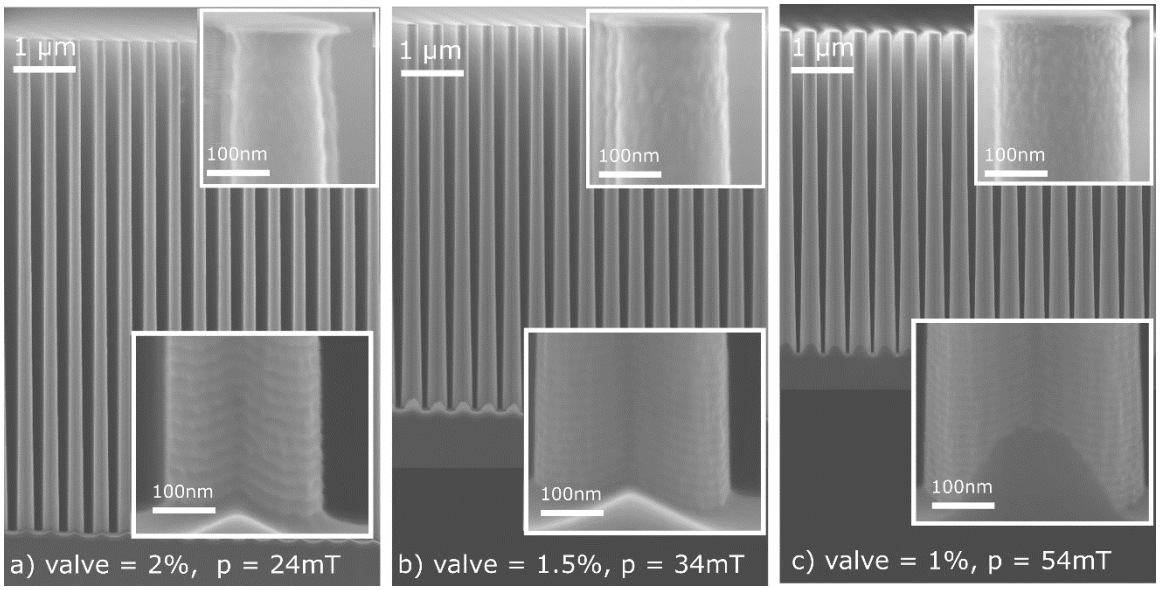

Figure 5.6. Effect of changing the E-pressure on the etch profile at 10sccm SF_6 flow and 15W power.

E-flow

Finally, the power P_E is fixed at 10W and the valve position is fixed at 2%. Then, the SF_6 flow is increased from 5 to 15sccm. Due to the fixed valve position, the pressure increases from 12 to 37mTorr. As shown in Figure 5.7, the etch profiles at 5sccm (Figure 5.7a) and 10sccm (Figure 5.7b) are deeper and straighter compared to that of 15sccm (Figure 5.7c). We already found that the plasma operates in the power-limited regime in which a higher SF_6 flow will marginally contribute to a higher etch rate. Instead, a higher SF_6 flow at a fixed valve position will increase the pressure in the reaction chamber. Therefore, just like explained in the previous section, the electron temperature T_e will be lower, and both the etch rate and mask selectivity will drop when the flow is increased.

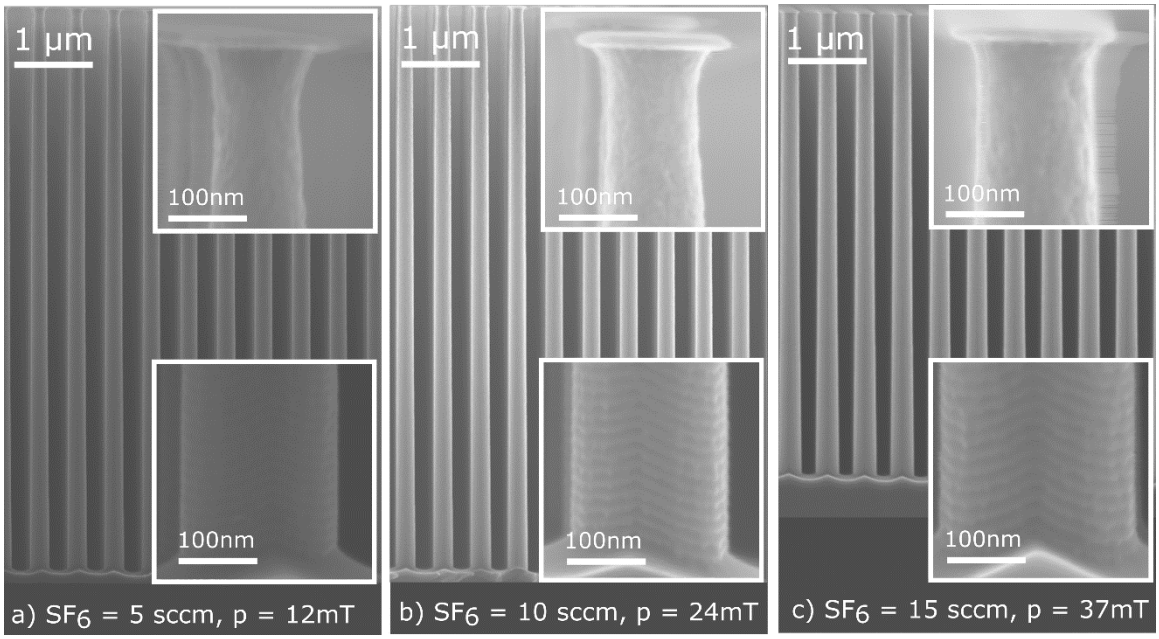

Figure 5. 7. Effect of changing the SF_6 flow on the etch profile at 10W power and 2% valve position.

5.3.4. The effect of total etch time

In the previous sections, the effect of some CORE parameters on the etch rate and profile of pillars have been investigated. In the following sections, the main goal is to create pillars as high as possible with low undercut using the knowhow already gained. In the chosen CORE recipe, the O-step is improved for a strong protection of the silicon sidewall, especially at the top part of the etching pillar. Subsequently, the R-step is carefully tuned to straighten the profile with minimum mask erosion. The E-parameters are chosen such that a reasonable etch rate and small scallop size is formed. Then, samples are etched for increasing time. After 1hr (Figure 5.8a), the etch pillars are 1.1µm high and slightly negative tapered. After 2hrs (Figure 5.8b), the pillars are 2.1µm high and almost perfectly straight. 4hrs of etching (Figure 5.8c) results in 3.9µm etch depth with a slightly positive slope. 8hrs (Figure 5.8d) gives 7.1µm etch depth and a more positive slope. 12hrs (Figure 5.8e) results in a height of 9.5µm and even more positive slope. Finally, 16hrs (Figure 5.8f) results in a height of 12.0µm and the most positive slope. It is observed that the topside of the pillars becomes thinner with increasing etch time. This is because they are continuously being exposed to fluorine radicals. These radicals slowly and steadily etch the oxide passivation away. In addition, the pillar diameter at the bottom increases with time probably due to a decrease in etch rate caused by RIE lag[42-45]. These observations are causing the pillar profile to become more positive. So, the total etch time has a pronounced impact on the slope of the pillars and should be considered in order to get the highest possible aspect ratio. Furthermore, the erosion of the mask is remarkable.

The first 8hrs, the erosion rate is closely following the expected 2nm/hr. But after that the erosion rate drops strongly: between 8 and 12hrs it slows down to 1.25nm/hr and between 12 and 16hrs it becomes only 0.25nm/hr. The authors have no explanation. Moreover, the chromium mask is not only getting thinner with etch time, but also the diameter of the deposited dots decreases while etching. This phenomenon is similar to photoresist in which the mask is retracting during the CORE etching process[46-49]. This retraction will have consequences for ultra-HAR processing and, therefore, this subject is studied in the next section.

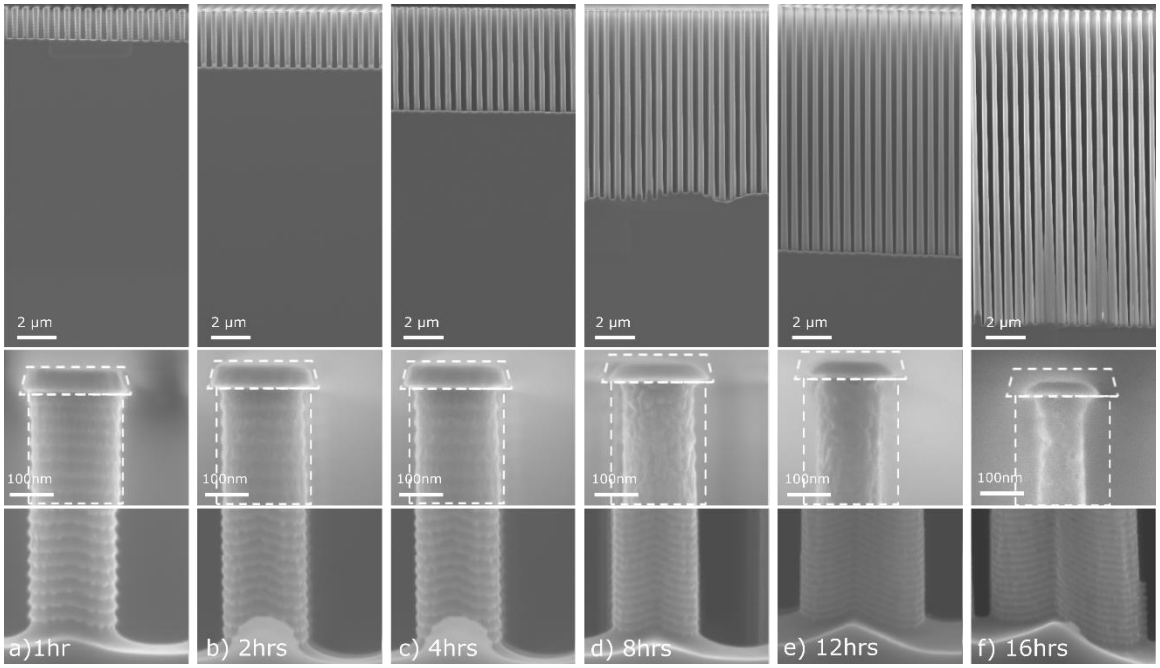

Figure 5.8. The evolution of ultra-HAR silicon pillars while increasing the total etch time.

5.3.5. Ultra-HAR silicon etching

Since the CORE sequence has proper design rules, it makes the fine-tuning for ultra-HAR silicon structures easier and less time consuming than e.g. the FC-based DREM procedure[50-54]. For instance, given the results presented in Figure 5.8 and knowing the effect of the CORE parameters, the recipe was fine-tuned to get ultra-HAR features with straight and smooth sidewalls. More precisely, the recipe of Figure 5.8 has been further improved by increasing the O-time to 8s. This reduces the lateral etch while improving the self-limitation property. In addition, the R-power is increased from 25 to 35W to ensure a straight profile. The ultra-HAR parameters are found in Table 5.2. As shown in Figure 5.9a, an array of 200nm pillars with 400nm periodicity are etched to a height of 11.4µm. This corresponds to an aspect ratio of 57. The blurry parts of the zoom-in at the topside of the pillars (Figure 5.9b) are believed to be due to local charging of the ultra-HAR pillars making them to vibrate during scanning.

To demonstrate the ability of the CORE sequence to fabricate sub-100nm HAR features, samples with 60nm dots created by e-beam and lift-off are used. The pillars in Figure 5.9c are correctly shaped except for the top part as shown in Figure 5.9d, which is positive tapered. The positive taper is believed to be induced by the chromium retraction as described in the previous section that has become severe at the end of the pillar etch process. Consequently, the retraction will be transferred into the silicon and causing profile distortion. This restricts the maximum achievable aspect ratio. The distortion can be reduced by improving the mask topography (e.g. by optimizing the lift-off procedure).

Table 5.2. The ultra-HAR CORE recipe for nanoscale silicon etching.

CORE	C	O	R	E
Time (s)	4	8	20	80
Pressure (mT)	0.8	50	0.2	24
O_2 (sccm)	50	50	0	0
Platen power (W)	0	10	35	15
DC Self-bias (V)	0	0	100	0
SF_6 (sccm)	0	0	5	10

5.3.6. Chromium mask etching and retraction

In the previous sections we have found that chromium is retracting substantially while performing CORE etching. To find out the cause, a specific sample is created. The sample consists of a silicon wafer with a layer of chromium and on top of that is a layer of polysilicon. Subsequently, stepper lithography is used to form 200nm holes with 400nm periodicity. This resist pattern is transferred into the polysilicon layer using the CORE sequence and will stop on the chromium layer. Finally, the sample is placed in a plasma oxygen system and ashed for 20min with 400sccm O_2 flow at 1Torr and 1000W power. During the ashing, the temperature quickly raises from room temperature up to almost 200^{o}C.

The result is shown in Figure 5.10a. Evidently, the resist is stripped totally, but it is also observed that the sandwiched chromium layer is undercutting the polysilicon top-layer isotropically by approximately 250nm and leaving a free-hanging polysilicon membrane. Additional experiments revealed that the chromium isotropic erosion rate is highly depending on the temperature and applied power during the plasma ashing[35-38]. Below 100^{o}C almost no erosion is observed and the erosion is only substantial at the maximum power. Nitrogen or CF_4 plasmas do not attack chromium, only O_2 supports the ashing. Therefore, it is assumed that the erosion is due to volatile CrO_x species. The above experiment shows that chromium can be an appropriate sacrificial layer for surface micromachining, because sticking of movable parts of nano- or micro-devices during wet etching is avoided[54-56]. The isotropic etch behaviour of the chromium layer is exploited

to remove it from the 60nm diameter pillars as presented in Figure 5.10b (before ashing) and Figure 5.10c (after ashing).

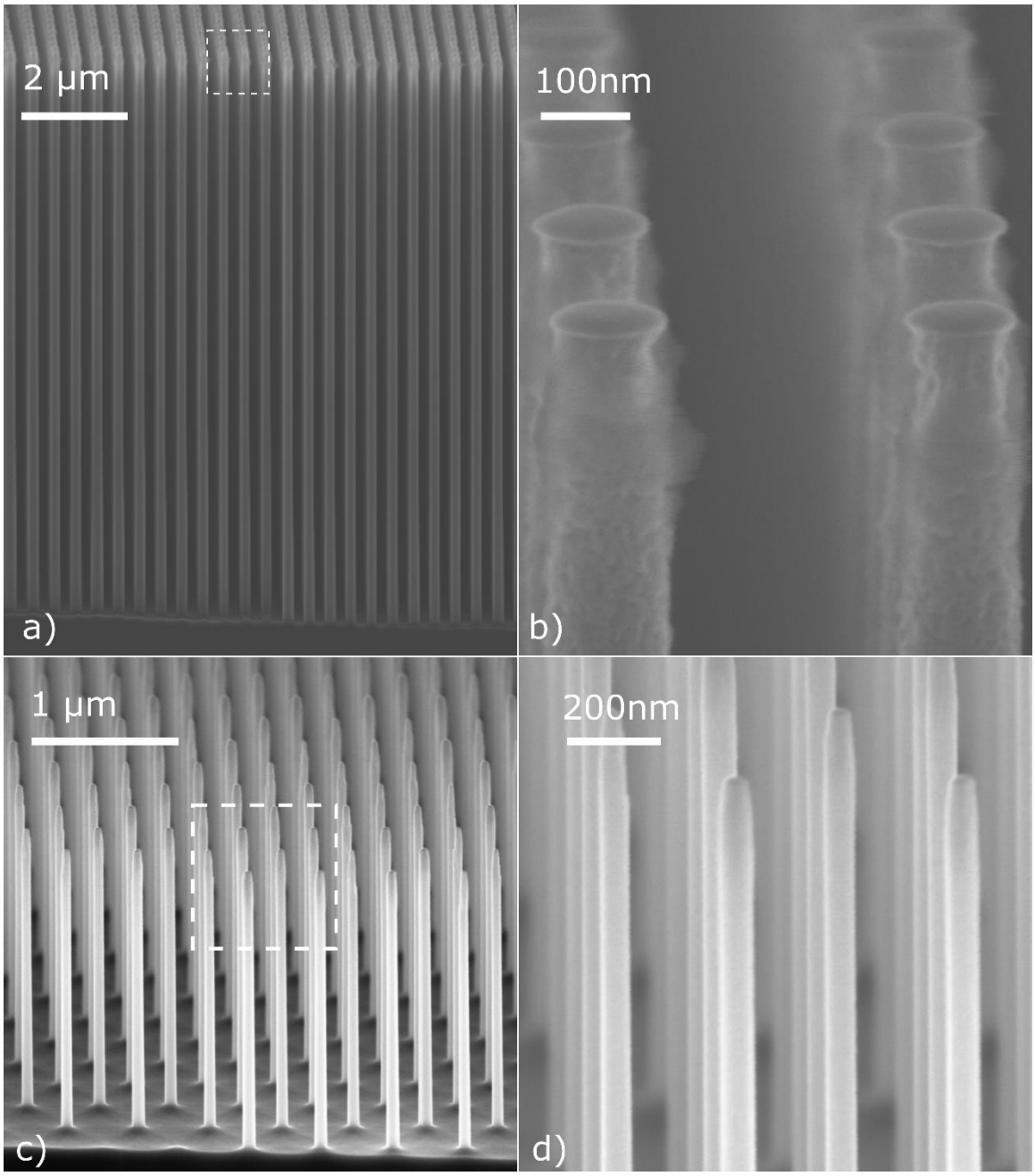

Figure 5.9. a) Ultra-HAR 200nm diameter silicon pillars etched by the CORE recipe. b) The blurry imaging at the topside might be due to 'pillar vibration' by the locally charging scanning electron beam. c) 60nm diameter pillars derived from e-beam lithography. d) The positive taper at the topside is believed to be due to chromium retraction during CORE etching.

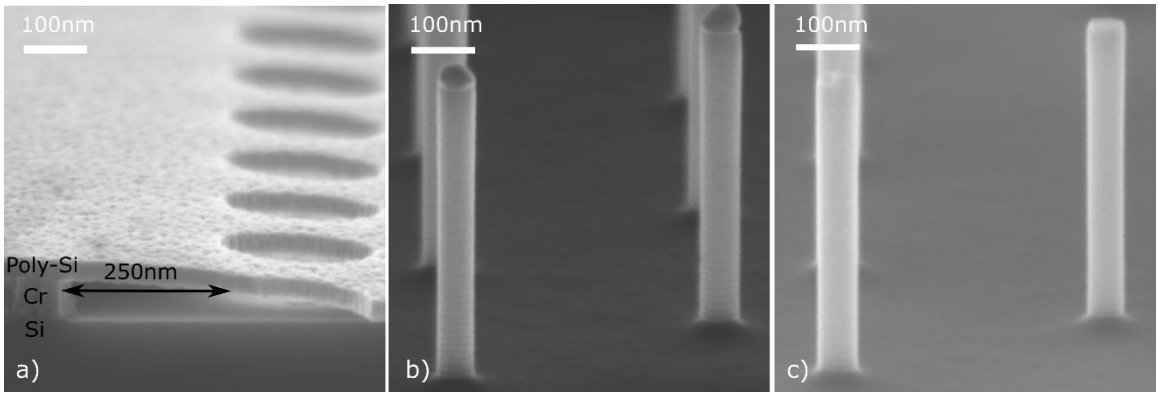

Figure 5.10. Chromium etching in a plasma ash system. a) Isotropic undercutting of a polysilicon membrane. b) 60nm e-beam defined pillars before chromium removal. c) The same pillars after chromium removal.

5.3.7. The effect of the carrier wafer

Additional experiments have been carried out to examine the impact of the surface condition of the silicon carrier wafer on the etch result. The first sample is attached to a new polished wafer (Figure 5.11a) and another sample is attached to a used wafer (Figure 5.11b). The latter has been used several times and started to become rough and blackened. The consequence of a roughened carrier wafer with respect to a polished wafer is that the etch rate of this carrier wafer is lower and therefore the fluorine concentration inside the reactor will be higher. As a result, the etch rate of a sample attached to a roughened wafer increases and the etch profile becomes less positive tapered with respect to a sample attached to a new wafer.

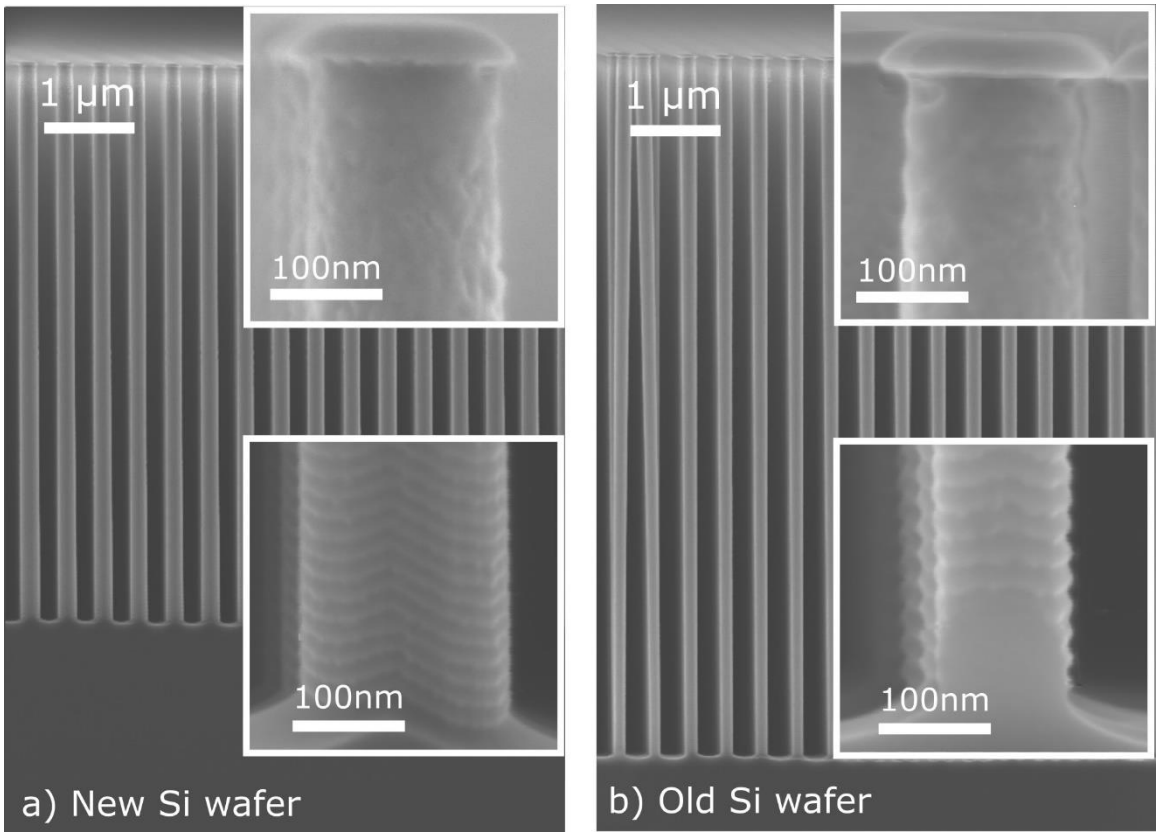

Figure 5.11. Effect of the carrier wafer on the etch profile. a) a new wafer and b) a roughened wafer.

5.4. Conclusions

This study demonstrated a process to fabricate ultra-HAR silicon pillars using chromium mask and the CORE sequence. The influence of various CORE parameters has been carefully investigated and optimized with respect to low mask undercut, high directionality and highest achievable aspect ratio. Using the optimal parameter setting in which all the CORE steps are well balanced, the fabricated pillars have smooth and straight sidewalls with low undercut. In general, a stronger oxidation will improve the silicon surface passivation and step coverage. The latter because the plasma oxidation is diffusion controlled and therefore the growing oxide film will limit the oxide growth at about 3nm. Therefore, after sufficient oxidation all surfaces including ultra-HAR features tend to have the same protection. The subsequent R-step controls the directionality and should be just enough to fully remove the horizontal surfaces from the grown oxide, but it should be limited to prevent too much mask erosion. The following E-step is able to control the scallop size and slope profile, the longer the E-step the less positive the slope will become. However, the E-step should be taken not too long in order not to penetrate the sidewall protection and causing sidewall roughness. In addition, the strength of the E-step (i.e. the amount of silicon etched per cycle) is affected by the E-pressure and flow,

but the effect depends on the specific parameter choice (i.e. if it is operating in the power-limited or flow-limited regime). Furthermore, RIE lag in HAR features will weaken the E-step and, thus, make the scallops smaller and the profile more positive.

It shows that a stronger oxidation step, whether due to more O-time or O-power, will result in less mask undercut and in a more positive taper. A stronger removal step, whether due to more R-time or R-power, will result in stronger mask erosion and in a less positive taper. A stronger E-step, whether due to more E-time or E-power, will result in bigger scallop size and a less positive taper. Finally, the chromium mask has proven to be an appropriate candidate to etch silicon with a selectivity up to 500. Using 60nm of chromium, the aspect ratio of the pillar gaps has been tuned beyond 55 and the pillars itself could reach 200. This is believed to be further improvable when a thicker mask is used.

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Chapter 6. Cr and CrO_x Etching using SF_6 and O_2 Plasma

This chapter will present a procedure to etch Cr and CrO_x using SF_6 and O_2 plasma as an alternative of the conventional Cl_2+O_2 plasma. The etch mechanism is explained by considering the formation of volatile chromyl fluoride (CrO_2F_2) which sublimes readily at room temperature. First, the effect of different plasma parameters (SF_6/O_2 ratio, plasma power, gas flux, loading) on the Cr and CrO_x etch rate will be studied using non-patterned samples. The non-patterned samples are simply used to find some quick indication on the overall etch rate performance without considering the selectivity or etch profile. Then with this obtained information, the patterned samples will be etched at the optimized plasma settings using both mixed mode and switched mode of SF_6 and O_2 plasma. Finally, the Cr etch procedure will be combined with other established etch process to demonstrate a complete fabrication scheme of silicon nanostructures using Cr as a mask.

6.1. Introduction

Chromium (Cr) is a widely used material in modern nanofabrication due to its advantageous properties. Cr is opaque (useful in optical lithography[1-3]), conductive (enabling many sensors and actuators[4-8]) and wear-resistant in harsh environments (useful as hard mask in plasma etching[9-15]). It is also used as an important adhesion layer for noble metals (such as gold) to prevent dewetting[16,17]. Cr can form a self-limiting dense and thin oxide layer that protects itself from further corrosion, which is crucial in all-Cr single electron transistors devices based on $Cr/CrO_x/Cr$ junctions[18,19]. Other potential applications lay in photonic crystals having a relatively thick Cr layer[20], RF MEMS electrodes[21,22], or corrosion resistant purification membranes[23,24]. In addition, the ferromagnetic CrO_2 (known from the old-fashioned cassette tape) is currently having a revival in spin-based devices for nanomagnet arrays and bit-patterned media[25].

In ***Chapter 3***, we have already introduced the CORE process that is able to structure high aspect ratio features into silicon[26-28]. Cr is of particular interest in the CORE sequence as

it serves as a durable hard mask in the quest to go beyond an aspect ratio of 100 in Si etching. In ***Chapter 6***, we used the lift-off procedure to pattern Cr[28]. However, with the continuous downscaling of nanoscale devices, the size control of the patterned Cr features becomes increasingly more important and lift-off is not sufficiently accurate nor reliable at the nanoscale. This is why plasma etching has become the standard technique for many decades in mainstream nanofabrication.

Currently, the plasma etching of Cr is mostly dependent on chlorine and oxygen plasma to create volatile chromyl chloride (CrO_2Cl_2) as the final etch product[29-41]. The consensus is that the presence of both chlorine (e.g. Cl_2 plasma) and oxygen radicals (e.g. O_2 plasma) are necessary to create the chromyl chloride product. The etch mechanism was first demonstrated by Abe[29] and a few years later explained by Nakata[30] using the reaction below:

$$Cr + 2O + 2Cl = CrO_2Cl_2 \quad (T_{melt} = -96.5^oC, T_{boil} = 117^oC \text{ @1 bar})$$

Since it requires both chlorine and oxygen radicals to remove a Cr atom (with the possibility of allowing any intermediate CrO_xCl_y reaction path), the etch rate shows an optimum for a specific ratio between the supplied Cl_2 and O_2 gas. This ratio is typically around 30% O_2 in the mixture of Cl_2 and O_2 plasma, but depends on the temperature and other plasma parameters[33,40]. Indeed, at low O_2 content, the formed $CrCl_x$ species have a very high melting temperature ($CrCl_2$ and $CrCl_3$) or simply decompose ($CrCl_4$). At high O_2 concentrations, the CrO_x species are difficult to evaporate. Only at sufficient O_2 concentration, it will create a volatile etch product CrO_2Cl_2 having boiling temperature of 117°C at 1 bar. This means that in a low pressure environment (i.e. the plasma reactor), CrO_2Cl_2 will easily evaporate even at room temperature (Figure 6.1)[40].

Even though Cr is typically patterned using Cl_2+O_2 plasma, there are some challenges of this etching at nanoscale. Firstly, CrO_2Cl_2 is an unstable compound that starts to decompose at temperature above 150°C [35,42]. As a result, CrO_x species released by this decomposition will deposit on close-by surfaces including the emerging sidewalls. Therefore, the process is getting more difficult to pattern the smallest and/or high aspect ratio features. Secondly, the Cl-based process contaminates the reactor as Al corrodes heavily with Cl_2 species and adequate cleaning or conditioning protocols are needed especially when the reactor has to be opened[31,32]. Thirdly, high O_2 concentration will erode the photoresist both vertically and laterally. This results in low selectivity (typically less than two[1,20,35,36]) and resist retraction[1,12,34,37] that restricts the critical dimension performance and hampers the minimum achievable feature size[1-3]. Fourthly, there is a trade-off between the requested straightness of the etch profile (decided by the O_2/Cl_2 ratio) and the mask selectivity. The reason is that during etching it need a mask on top of the Cr film and there is always a substrate below the Cr film. Typically, the mask is photoresist and the substrate is silicon. If one decides to increase the O_2/Cl_2 ratio to improve directionality, the selectivity towards the resist will drop. Similarly, if the O_2/Cl_2 ratio is decreased, the selectivity towards the silicon will drop. Therefore, there is always

a compromise between the mask selectivity and substrate attack. Finally, reactor history (or memory effect) is an important issue as it is found that Cr films are damaged (i.e. etched) even for seemingly pure oxygen plasma conditions[43-44]. The etching is likely caused by Cl contributions stuck on the reactor walls from a preceding etch process. Therefore, reproducibility is often a difficult task.

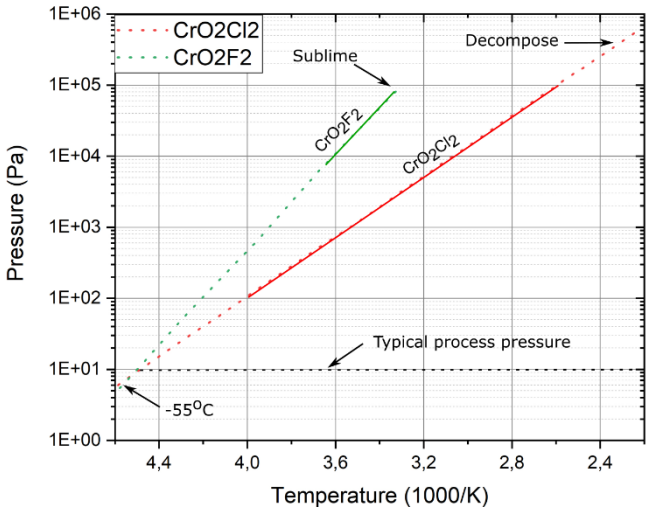

Figure 6.1. Vapor pressure of CrO_2Cl_2 and CrO_2F_2[40,45]. The estimated extrapolated sublimation temperature at 76mT is -55°C.

To overcome the above mentioned challenges, different approaches have been addressed such as adding reducing agents (such as CO_2, C_2H_5OH, H_2[1,34-36]) or performing cryogenic etching[39,40]. In this study, we propose a new approach for directional etching of Cr thin film by exchanging the chorine by the fluorine plasma. The reaction process in the SF_6+O_2 plasma resembles that in the Cl_2+O_2 plasma and is demonstrated as below:

$$Cr + 2O + 2F = CrO_2F_2 \quad (T_{melt} = 31.6^oC, T_{sublime} = 29.6^oC \text{ @1 bar})$$

Although the existence of CrO_2F_2 species has been known long time ago, it is rarely mentioned in literature. As shown in Figure 6.1, it is found to sublime readily at 29.6°C and melt at 31.6°C when the pressure is one bar[45]. Therefore, at a sufficiently low process pressure and the substrate holder is kept at room temperature, Cr can be easily etched away in the SF_6+O_2 plasma.

The test the etch performance of Cr and CrO_x thin film in SF_6+O_2 plasma, an experimental procedure has been designed using both patterned and non-patterned coated wafers. The non-patterned wafers are simply used to find some quick indication on overall etch rate performance without considering the selectivity or profile. With this information, patterned samples will be etched using optimized plasma settings and analyzed with SEM to extract the profile and selectivity towards Si.

6.2. Materials and Methods

Non-patterned samples: <100> Si wafers (150mm diameter) are coated with 70nm Cr (Lesker CMS18 sputter system). The CrO_x coated wafers are prepared by depositing 200nm CrOx on top of 30nm Cr. This deposited CrO_x layer has a refractive index of 2.39, which is close to the expected 2.55 value for Cr_2O_3. Then the Cr- and CrO_x- coated wafers are cleaved into 2 × 1cm^2 chips and individually mounted in the center of a 150mm diameter Si carrier wafer using a tiny drop of Galden® PFPE fluid (Solvay Solexis SpA) for sufficient thermal contact or to fix it.

Patterned samples: First, Si wafers are coated (Wordentec QCL800 Metal evaporator) with two different thicknesses. One with 30nm polySi on top of 70nm Cr and another with 150nm polySi on top of 1µm Cr. Then these coated wafers are covered by a layer of 65nm BARC (DUV42S-6) and 360nm DUV resist (KRF 230Y) using a spin coating system (Gamma 2M spin-coater, Süss MicroTech). Subsequently, line patterns (200nm width, 400nm pitch) are defined by a DUV stepper (FPA-3000EX4, Canon) equipped with a 248nm KrF excimer laser. The exposure dose is 86mJ/cm^2. The wafers are developed in 2.38% tetra-methyl-ammonium-hydroxide in water (AZ726 MIF, AZ Electronic Materials), rinsed in de-ionized (DI) water, and spin dried with a gentle nitrogen stream. Similar to the non-patterned wafers, the patterned ones are cleaved into 1× 1cm^2 chips and mounted on a Si carrier wafer.

Etching: The prepared samples are loaded into a commercial dual source etch system (SPTS/Pegasus DRIE). The dual source plasma can provide ICP assisted etching, but in this study the RIE mode is used (i.e. solely platen power)[28]. The system has been dedicated for SF_6/O_2 based plasma etching solely and has no prior fluorocarbon or chlorine history. The FC- and Cl-free chamber is required to ensure the absence of any contamination or influence that might affect the Cr etch performance. In case of the non-patterned samples, the etching process is continue until the Cr (or CrO_x) is gone. Then the etch rate is simply deduced by dividing the thickness of Cr (70nm) or CrO_x (200nm) by the recorded time. In case of patterned samples, first 65nm BARC layer is etched using O_2 plasma followed by a polySi etch using SF_6/O_2 plasma to open the Cr surface to be etched. The initial Cr etch setting is fixed at 200sccm total flow at 2% throttle valve (pressure ca. 60mT) and 100W platen power (V_{dc} bias between 270 and 140V). The SF_6 flow is varied to extract the influence of the SF_6/O_2 ratio (i.e. % SF_6) on the etch rate at four different temperatures: -20ºC, 0ºC, 20ºC, and 40ºC.

Analysis: After the etching, the Galden heat transfer fluid is wiped gently from the backside of the patterned samples with alcohol sprayed on a tissue. The sample is cleaved manually using a diamond pen and then characterized using a SEM (Supra V60, Zeiss).

6.3. Results and Discussion

6.3.1. The effect of SF_6/O_2 ratio on the Cr etch rate

In this section, the effect of plasma parameters on the Cr etch rate will be studied first using non-patterned samples. All the experiments are performed at 100W plasma power with the O_2 flow rates fixed at 200sccm. The valve is set at 2% that will result in the etching pressure of 60-70mT. The initial etch results are presented in Figure 6.2 where the Cr etch rate is determined as a function of SF_6/O_2 ratio at four different temperatures: -20 ºC, 0 ºC, 20 ºC, and 40ºC.

Similar to Cl_2+O_2 plasma, the Cr etch rate in SF_6+O_2 plasma shows an optimum value at a specific ratio between the supplied SF_6 and O_2 gas. This indicates that both fluorine and oxygen species are necessary to chemically etch the Cr layer. If only pure O_2 or SF_6 plasma is used, Cr will be barely etched as the products are not volatile. However, unlike the Cl_2+O_2 plasma where the maximum etch rate is typically found around 70-80% Cl_2 of the total flow[36], the Cr etch rate in SF_6+O_2 plasma seems to increase linear and peaks sharply at a very small SF_6/O_2 ratio below 1%. Beyond that ratio, the Cr etch rate gradually decreases and finally stops when the SF_6/O_2 ratio increases more than 6%.

As shown in Figure 6.2, the Cr etch rate in SF_6+O_2 plasma depends on the temperature of the samples. The higher temperature, the faster of the Cr etch rate. However, when the SF_6/O_2 ratio is decreased to below 0.5%, the Cr etch rate seems to be independent on the temperature. This result suggests that the etching process at very low SF_6/O_2 ratios is plasma-supply limited and the surface reactions are fast enough to have no effect on the etch rate. When the SF_6/O_2 ratio is increased more than 1%, the plasma-supply limited regime will change into the surface-reaction limited regime and facilitate a faster etching process at high temperature. Therefore, with high SF_6/O_2 ratio the Cr etch rate is strongly dependent on the temperature. It is also noticed that the self bias V_{dc} at the SF_6/O_2 ratio of 0% (corresponds to pure O_2 plasma) is around 270V, but the Cr etch rate is still close to zero. Therefore, the influence of physical etching (i.e. sputtering) on Cr can be ignored.

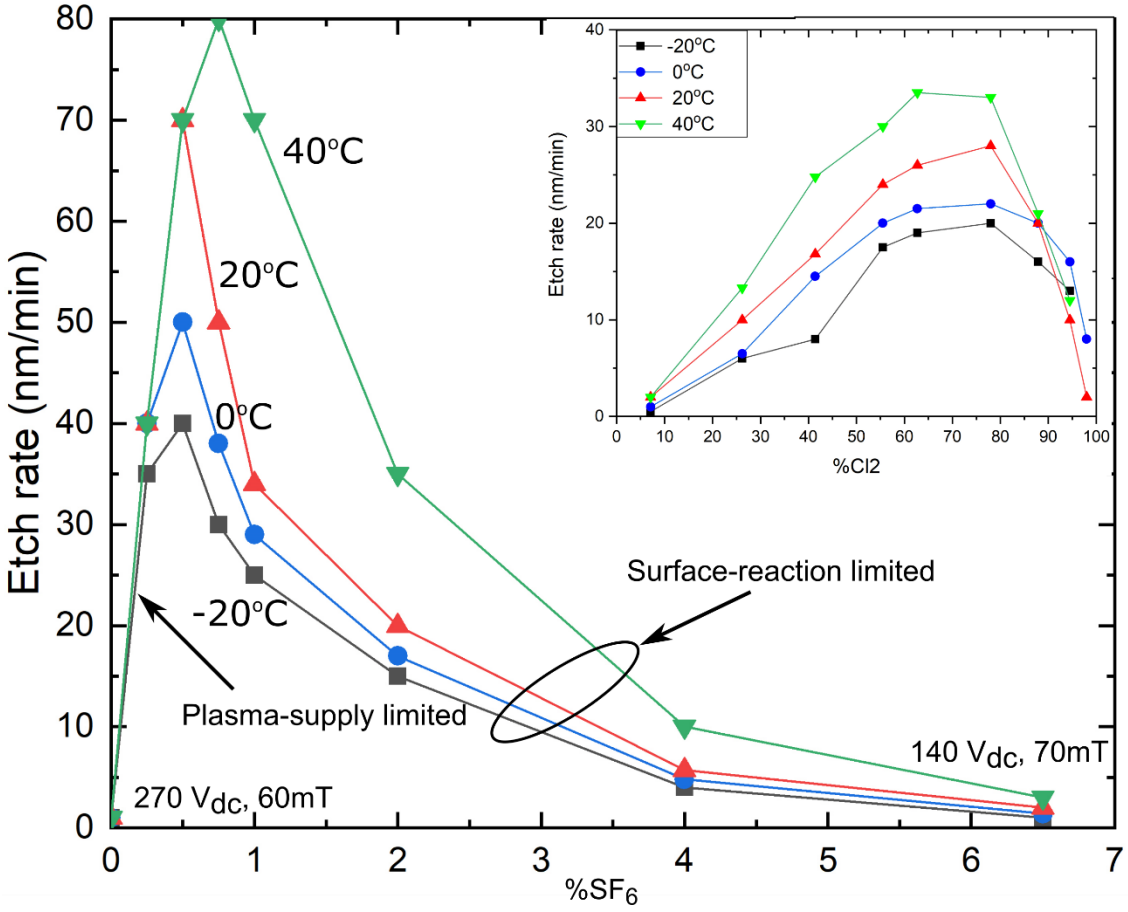

Figure 6.2. The Cr etch rate is presented as a function of the SF_6/O_2 ratio at different temperatures: -20 °C, 0 °C, 20 °C, and 40°C. Other process conditions are kept at a fixed plasma power (100W), O_2 flow rate (200sccm) and valve position (2%). The inset is reproduced from Staaks showing the Cr etch rate in Cl_2+O_2 plasma[36].

6.3.2. The effect of plasma power and gas flux on the Cr etch rate

It has been shown in the previous section that the Cr etch rate with the SF_6/O_2 ratio below 0.5% is limited by the supply of active species from the plasma bulk and not by the reaction speed at the Cr surface. Then the next study is to find out what controls this supply. There are two main influences: the plasma power and the gas flux (i.e. pressure and/or gas flow rate). Their effect on the Cr etch rate is tested by varying both the plasma power and the gas flux in a reasonable broad process window at a fixed temperature (40°C), SF_6/O_2 ratio (0.5%) and throttle valve (2%).

As shown in Figure 6.3, the Cr is etched faster when either the gas flux or the plasma power is increased. However it is noticed in Figure 6.3a that for 50W plasma power, the Cr etch rate seems to saturate when the gas flow rate increases between 200sccm and 800sccm. This is probably because all the available plasma power is already used and there will be not sufficient power to convert the additional gas into active species.

Therefore increasing the gas flow rate more than 200sccm when the plasma power is at 50W will not enhance the Cr etch rate. Similarly, for the gas flow rate of 100sccm in Figure 6.3b, the Cr etch rate increases slowly and seems to saturate at higher power. In this case, the amount of gas is controlling the Cr etch rate and extra power will only have a slightly influence on it. One interesting phenomenon can be observed is that the Cr etch rate doubles when both the plasma power and the gas flow rate are doubled. This is illustrated by the dashed lines in Figure 6.3a giving an example that the Cr etch rate for 800sccm at 200W is twice the etch rate for 400sccm at100W and quadruple the etch rate for 200sccm at 50W.

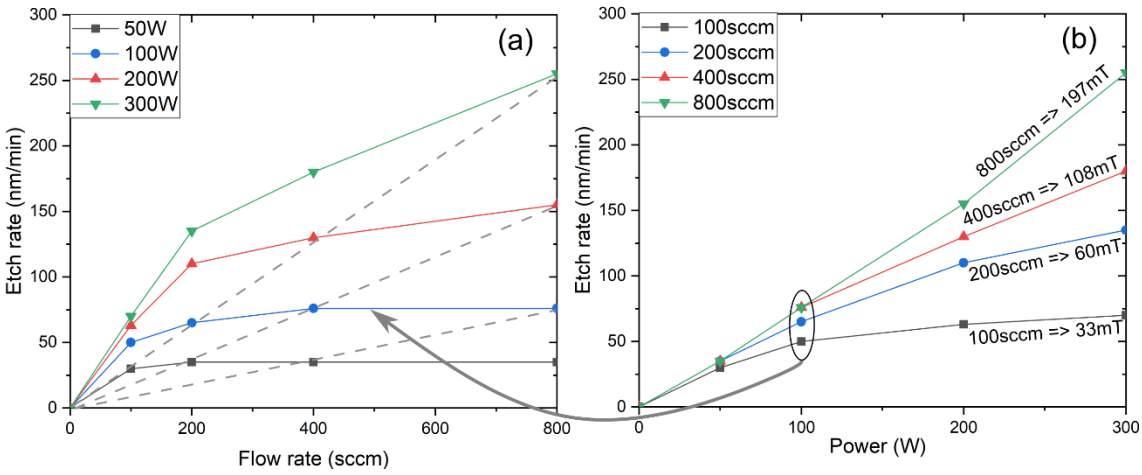

Figure 6.3. The Cr etch rate when increasing the gas flux (a) and the plasma power (a). Other process conditions are kept at a fixed temperature (40^{o}C), SF_6/O_2 ratio (0.5%), valve position (2%) and exposed Cr surface area (2cm^2).

In the above experiments, the throttle valve has been fixed at 2% which means that the process pressure increased together with the gas flow rate. Since the gas flux depends on both the process pressure and gas flow rate, an additional experiment is needed to separate these two variables and find out which one has more effects on the Cr etch rate. In this experiment, instead of fixing the turbo throttle valve, it is allowed to adapt for different gas flow rates applied at a specific pressure value.

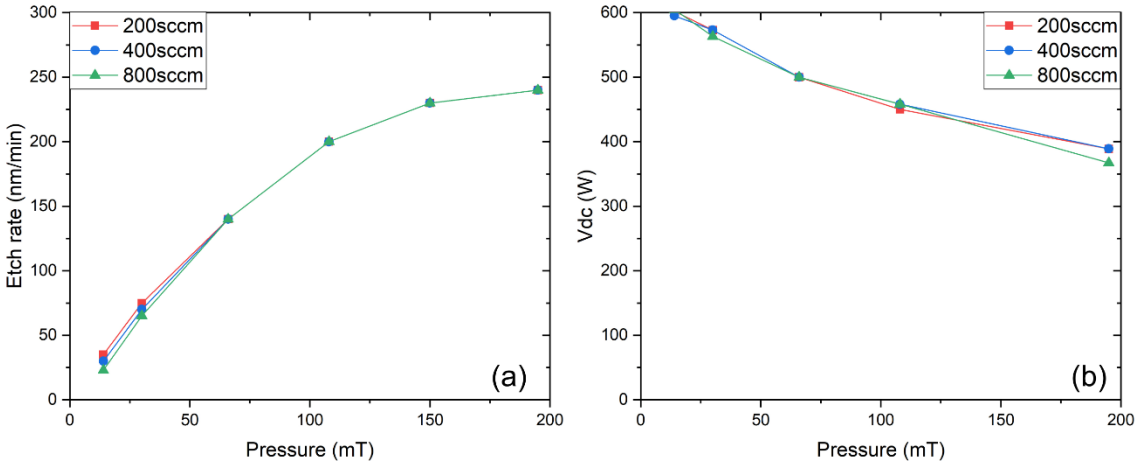

Figure 6.4. The Cr etch rate (a) and the self-bias (b) as diffrent process pressure and flow rates.

Figure 6.4a shows that the Cr etch rate increases when the pressure is increased. As the curves for 200sccm, 400sccm, and 800sccm flow rates almost coincide with each other, we can conclude that the pressure and not the flow rate controls the Cr etch rates in the process window investigated above. Therefore, a more appropriate conclusion of the previous finding is that the etch rate doubles when both the power and the process pressure are doubled. Furthermore, the induced self-bias also depends mainly on the process pressure and the flow has minor effect on it (Figure 6.4b).

6.3.3. The effect of SF_6/O_2 ratio on the CrOx etch rate

With the obtained information for the optimum parameter settings, the graph in Figure 6.2 is partly repeated to get a more detailed curve at low SF_6/O_2 ratios, but this time at the highest allowed power (300W), pressure (200mT), flow rate (800sccm) and temperature (40°C). The Cr and CrO_x etch rates are plotted in Figure 6.5a as a function of the SF_6/O_2 ratio. As expected, the Cr etch rate increases linearly at very low SF_6/O_2 ratios. When the SF_6/O_2 ratio is at 0.75%, the Cr etch rate reaches its maximum and then gradually slows down. In contrast, the CrO_x etch rate increases linearly with the increased SF_6/O_2 ratio. Figure 6.5b demonstrated a further study on the CrO_x etch rate at different plasma settings and higher SF_6/O_2 ratios. It shows that the highest CrO_x etch rate increased with the increased pressure and barely depends on the flow rate. For 200sccm flow rate (or 170mT), the CrO_x etch rate keeps raising until it saturates at below 2500nm/min. This saturation is likely caused by the limited pressure and power supply when there is not enough gas or enery to support a higher etch rate.

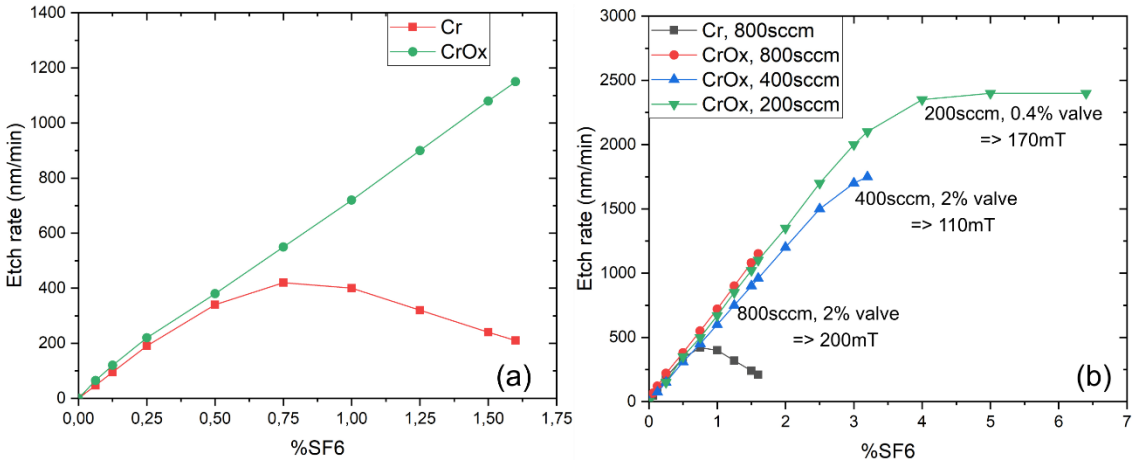

Figure 6.5. (a) The Cr and CrO_x etch rate as function of SF_6/O_2 ratios at a fixed plasma power (300W), pressure (200mT), flow rate (800sccm) and temperature (40°C). (b) The CrO_x etch rate is further study at different plasma settings and higher SF_6/O_2 ratios.

The complex etch rate behavior of Cr or CrO_x is not unfamiliar in plasma etching in general. For instance, in Si etching using SF_6 and O_2 plasma, it is found that when the plasma power is relatively high and the gas flux is low, the flux will control the radical production. This is called the flux-controlled or power-saturated region. In contrast, if the gas flux is sufficiently high and the power is low, the power will control the etch rate. This is called the power-controlled or flux-saturated region. Also for Si etching, the etch rate doubles when both the power and gas flux are doubled. However, in contrast to the Cr etching, the gas flow and not the pressure affect the silicon etch rate. This may be due to the lifetime of active species that play a crucial role.

A specific observation in Figure 6.5 is that the Cr etch rate is higher than that in Figure 6.3 at the same plasma condition. This is because the samples selected for this experiment are smaller in area (1.5cm^2) compared to previous experiments (2cm^2). This brings us to the subject of how the loading affects the etch rate. Mogab was the first to derive an equation, which correctly predicts the loading effect[46]. The loading effect is defined as the decrease of the etch rate for an increasing area of etching material inside the plasma. In a simplistic manner, it can be argued that the amount of etched material will not change for an identical plasma setting and thus, the etch rate will drop 2 times when the exposed area is doubled. A more detailed and more correct analysis though can be found in literature where a pragmatic loading equation is formulated[47]:

$$ER = ER_{sat}/(1+\alpha L)$$

The saturation etch rate ER_{sat} occurs for a very low Cr loading area L and $\alpha=\alpha(T)$ is a constant depending on the lifetime of the etching species and temperature[32,46]. Both ER_{sat} and α are varying with the specific plasma setting and can be deduced by measuring a few ER values at different L values. For example, at the plasma settings of 300W, 200mT and 40°C, we find that the etch rate of 1.5cm^2, 3cm^2 and 6cm^2 sample are 380nm/min,

300nm/min and 210nm/min, respectively. Therefore, ER_{sat} =525nm/min and α =0.25cm^2 (Figure 6.6) and only when $\alpha L >> 1$ (i.e. A>20cm^2) the above simplistic '1/L' argument holds. Furthermore, the samples have been placed on a Si carrier. It seems that this carrier does not affect the fluorine concentration, even though SiF_4 is very volatile. This indicates that there is a passivating SiO_2 layer presents that prevents the consumption of fluorine radicals.

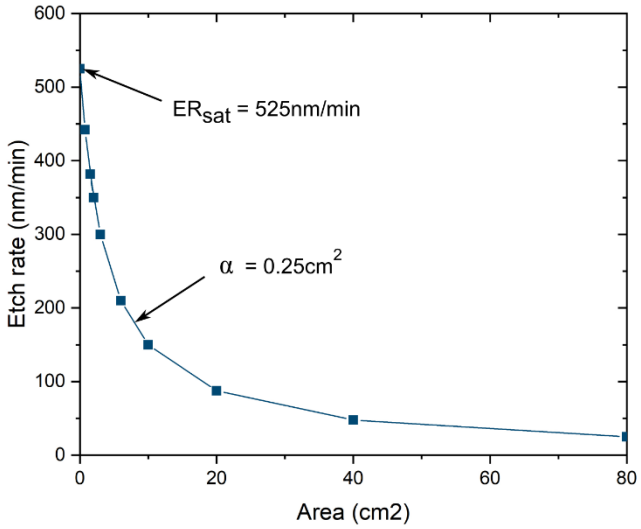

Figure 6.6. The Cr etch rate as function of sample area. The plasma settings are fixed at 300W, 800sccm, and 40°C.

6.3.4. The etching mechanism of Cr and CrO_x in SF_6+O_2 plasma

With all the results obtained from the above study, it allows us to explain the etch mechanism of Cr in $SF_6 + O_2$ plasma based on these reactions on the Cr surface:

Initial reaction: $Cr + 2O = CrO_2$
Followed by: $CrO_2 + 2F = CrO_2F_2$

Starting from pure O_2 plasma that creates oxygen radicals, the Cr surface is rapidly oxidized until a protective skin is formed that prevents further oxidation. Then, by introducing small amounts of SF_6, the generated fluorine radicals will react with the adsorbed CrO_x species and produce volatile chromyl fluoride (CrO_2F_2) products. The desorption of CrO_2F_2 will expose fresh Cr surface that will immediately be oxidized by the available oxygen radicals and the volatile reaction awaits the next fluorine radical to arrive. When more SF_6 is added, the latter process will go faster and thus the Cr etch rate increases. The Cr etch rate will improve further with the additional supply of SF_6 until the fluorine radicals start to attach to the exposed Cr layer before oxygen radicals arrive. If this happens, part of the exposed Cr will be fluorinated producing a nonvolatile CrF_x layer. As the result, further reactions will be blocked and the Cr etch rate will go down.

The CrF_x shielding will continue until the SF_6/O_2 ratio is more than 6%, the Cr etch rate becomes almost zero.

For the CrO_x material, the situation is different as the Cr is already fully oxidized. Therefore the CrO_x etch rate continues to increase with the increased SF_6/O_2 ratio without showing a maximum etch rate since the protective CrF_x skin cannot be created. However, it will saturate when the process power or the gas flux is insufficient to create additional radicals. As the CrO_x continuous to increase with the increased SF_6/O_2 ratio while the Cr etch rate drops to almost zero, the selectivity between Cr and CrO_x at high SF_6/O_2 ratios will go to extremely high values (>>10.000). This observation implies that it is possible to accurately remove a CrO_x surface layer on a Cr thin film by exposing the surface to a pure SF_6 plasma. The fluorine radicals will first etch the CrO_x layer by creating volatile CrO_2F_2 and then block the Cr surface with the forming CrF_x.

6.3.5. Cr patterning using SF_6 and O_2 plasma

In the previous sections, we have established the plasma settings with a much faster Cr etch rate than that in the Cl_2+O_2 plasma, so the next study is to investigate the selectivity and the etch profile of Cr patterns. It should be noticed that the low SF_6/O_2 ratio used for achieving high Cr etch rate means that the plasma contains almost pure O_2. Consequently, the photoresist will be etched very fast in O_2 plasma resulting in a low selectivity. In order to improve the selectivity, an intermediate hard mask is required to reliably transfer the resist patterns. We have opted for polySi as this material is standard available and perfectly compatible with mainstream fabrication processes. Another reason is that Si will unlikely be etched in pure O_2 due to the strong oxidation that forms nonvolatile SiO_2 products. This indicates that both the polySi mask and bulk Si underneath the Cr layer will be preserved during the Cr etching. Furthermore, polySi can be etched with an extreme high selectivity towards resist or Cr layer using the established F-based plasma[47-49].

Patterned samples (200nm width, 400nm pitch) having 150nm polySi on top of 1µm Cr are first etched in a mixture of SF_6 and O_2 plasma. Using the results obtained from Figure 6.5, the plasma settings are optimized at a fixed SF_6/O_2 ratio (0.5%), flow rate (200sccm) and pressure (150mT). The samples are etched at different combinations of temperature (-20 ^oC, 0 ^oC, 20 ^oC, and 40^oC) and plasma power (50W, 100W and 300W). The etch time at 50W, 100W and 300W are 40min, 20min and 4min, respectively. Figure 6.7 presents the preliminary etch results of Cr using the mixture of SF_6 and O_2 plasma. The odd pronounced sideways cut approximately halfway into the Cr the layer is believed to be caused by rapid CrO_x removal. This CrO_x layer seems to have developed during the Cr deposition, which has been performed in two runs even though the vacuum has not been broken in between.

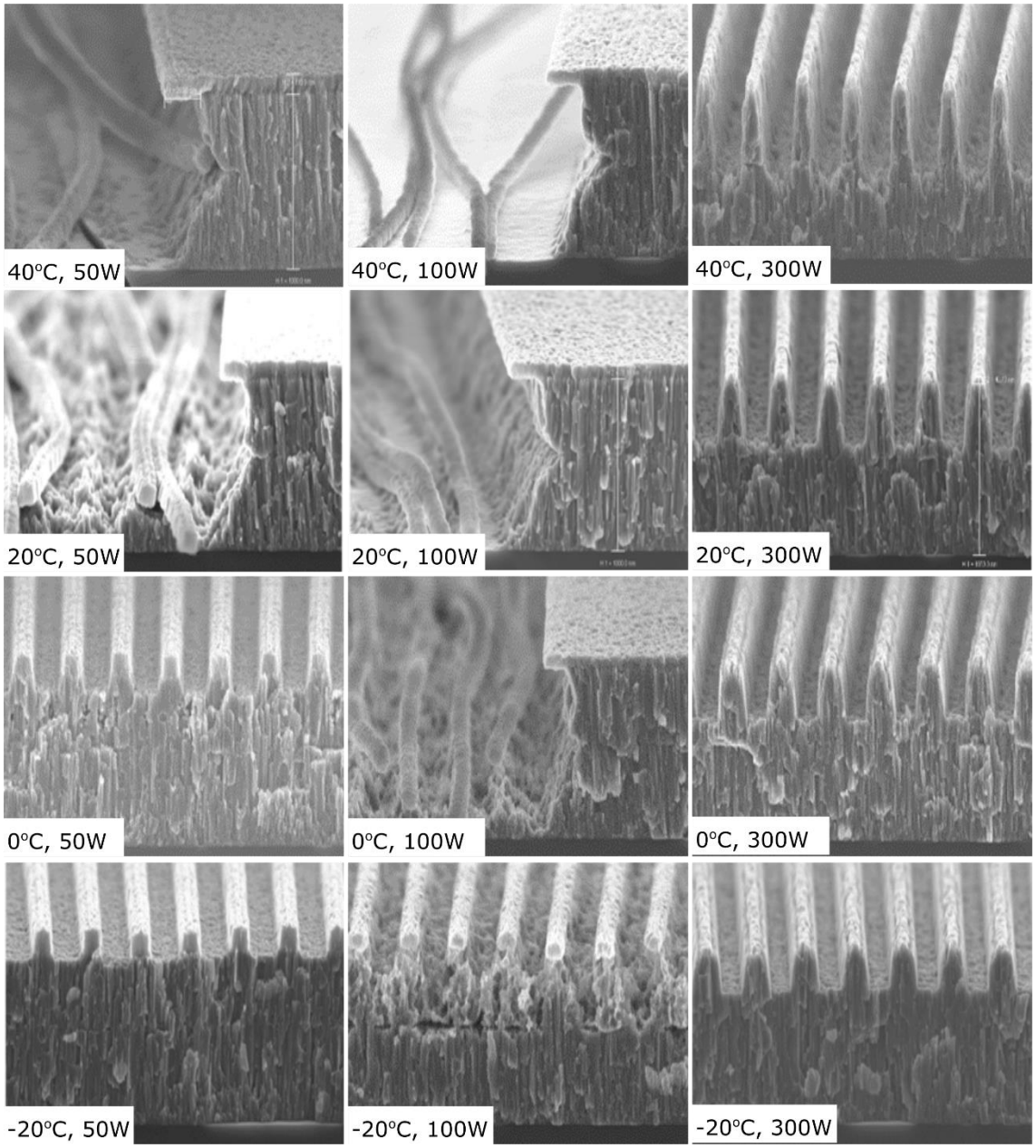

Figure 6.7. Cr etch using mixed 0.5% SF_6 in O_2 plasma for various temperature and plasma power. The mask is 150nm polySi on top of 1000nm Cr. Top to bottom: 40, 20, 0, -20°C. Left to right: 40min at 50W (45Vdc), 20min at 100W (140Vdc), and 4min at 300W (420Vdc).

The Cr and polySi etch rates are extracted from Figure 6.7 and shown in Figure 6.8 as a function of plasma power at different temperatures. Similar to non-patterned samples, the Cr etch rate of patterned samples increases for higher power and higher temperature settings. The Cr etch rate is up to 150nm/min for the plasma power at 300W. In contrast, the polySi etch rate in Figure 6.8b scales quadratic with the plasma power and does not

depend on the temperature. Since both the ion density and energy increase with power, the polySi mask is physically eroded resulting in low selectivity.

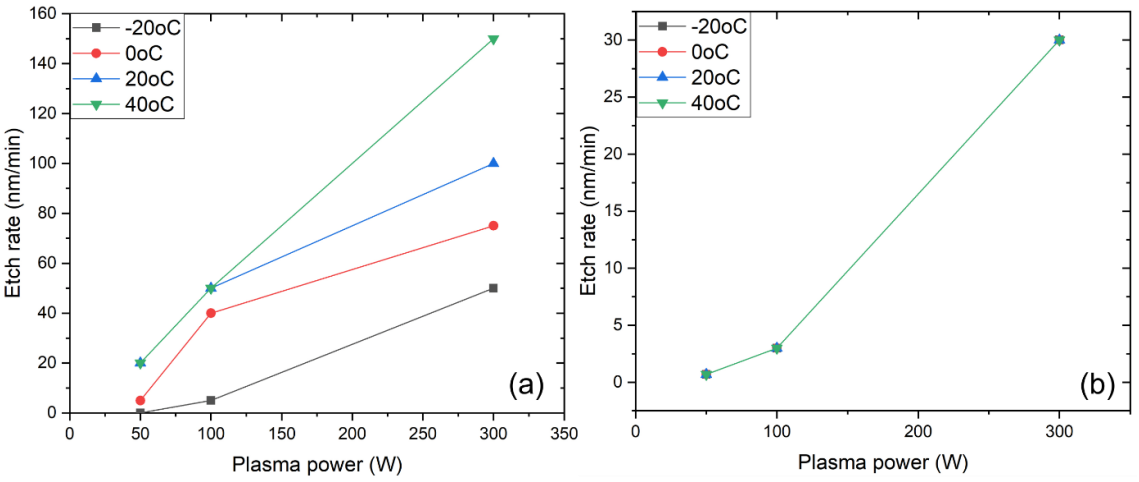

Figure 6.8. The Cr etch rate (a) and polySi etch rate (b) as the function of plasma power at diffrent temperatures. The numbers are extract from Figure 6.7.

The most important observation should be noticed is that it seems to be difficult to achieve both reasonable selectivity and directional profile of Cr using a mixture of SF_6 and O_2 plasma. This difficulty is similar to silicon etching in the mixed mode. However, since the switched CORE process has shown an excellent directional and selective performance in silicon etching, the same switched procedure is tested for etching Cr. The initial switched recipe to study the etching performance of Cr patterns are shown in Table 6.1.

Table 6.1. The initial switched recipe to study the etching of Cr

	O-Step	F-Step
Time (s)	9	1
O_2 (sccm)	50	50
SF_6 (sccm)	0	3
Pressure (mT)	50	50
Power (W)	30	30
Temperature(^{o}C)	20	20

In the adapting switched mode, the etching process of Cr is accomplished by alternating the chemistry back-and-forth between an oxygen-rich (O-step) and fluorine-rich (F-step) plasma. In the F-step, it is opted to keep the O_2 flowing to prevent major plasma changes that might trigger the matching unit to change and causing etch fluctuations. As shown in Figure 6.9, the etch depth of Cr and polySi after 45min is around 330nm and 15nm corresponds to the Cr and polySi etch rates of 7nm/min and 0.3nm/min respectively. This results in a much better selectivity (>20) than in the mixed mode. The chaotically arranged vertical lines are caused by the polycrystalline film growth during Cr deposition. It can

be seen that the etch sidewall is slightly positive tapered with no undercut. The latter is probably due an AlF_x layer forming on the sidewall during the E-step. Since there is almost no ion bombardment to the sidewall, this AlF_x layer is preserved and protect the sidewall. In contrast, the bottom surface receives a constant supply of ions that removes the F-species. Then the coming oxygen radicals in the O-step will react with the open Cr surface forming CrO_x. Subsequently, this CrO_x layer will be removed by the fluorine radicals in the next F-step and the etching proceeds.

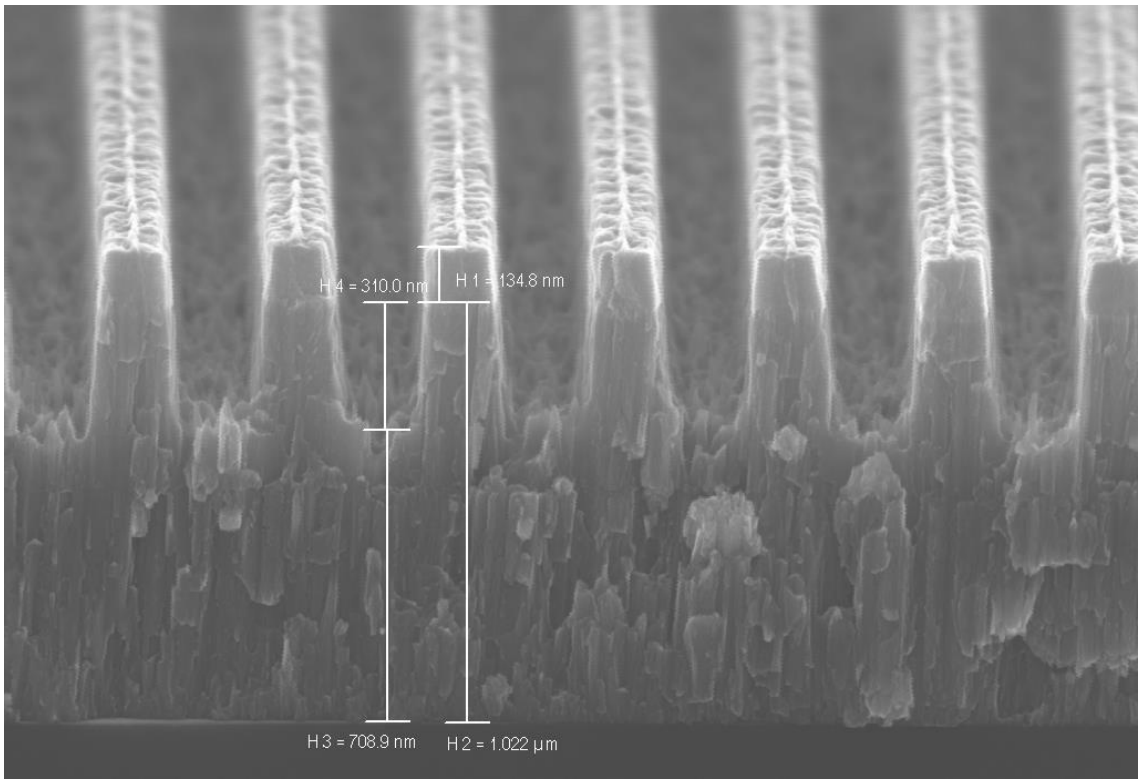

Figure 6.9. 1µm Cr patterns are etched using a switched SF_6 and O_2 plasma sequence having etch rate of 7nm/min with good selectivity (>20) towards the initial 150nm polySi mask. The chaotically arranged vertical lines are a result of the polycrystalline film growth during Cr deposition.

Since a convenient procedure for Cr etching has been defined, the next step is to see how it operates in a complete fabrication scheme of Si nanostructures. Figure 6.10a shows a sample having 400nm pitch DUV grating patterns on top of a stack layers to be etched. The stack is composed of 65nm Barc layer on top of 30nm polySi and 70nm Cr. The sample is etched in a single run without breaking vacuum in the same system. First, the Barc polymer is etched using 50sccm oxygen plasma for 10min (Figure 6.10b). The throttle valve is fully opened (100%) to ensure a low process pressure (ca.1mT) that will promote ions to control the pattern transfer (radicals will cause retraction). The plasma power is kept low at 10W (showing 18Vdc) to minimize the physical impact of ionic species that would degrade the pattern shape. Subsequently, the polySi is etched using 10

cycles of the CORE sequence (Figure 6.10c)[28]. This etch is followed by 10min oxygen plasma resist strip which is performed at sufficiently high pressure (50mT) to promote radical etching and prevent any surface damage cause by ions (Figure 6.10d). Subsequently, the Cr is etched using the switching SF_6 and O_2 plasma (Figure 6.10e). Finally, the patterned Cr is served as a mask to etch the bulk Si using the CORE sequence (Figure 6.10f).

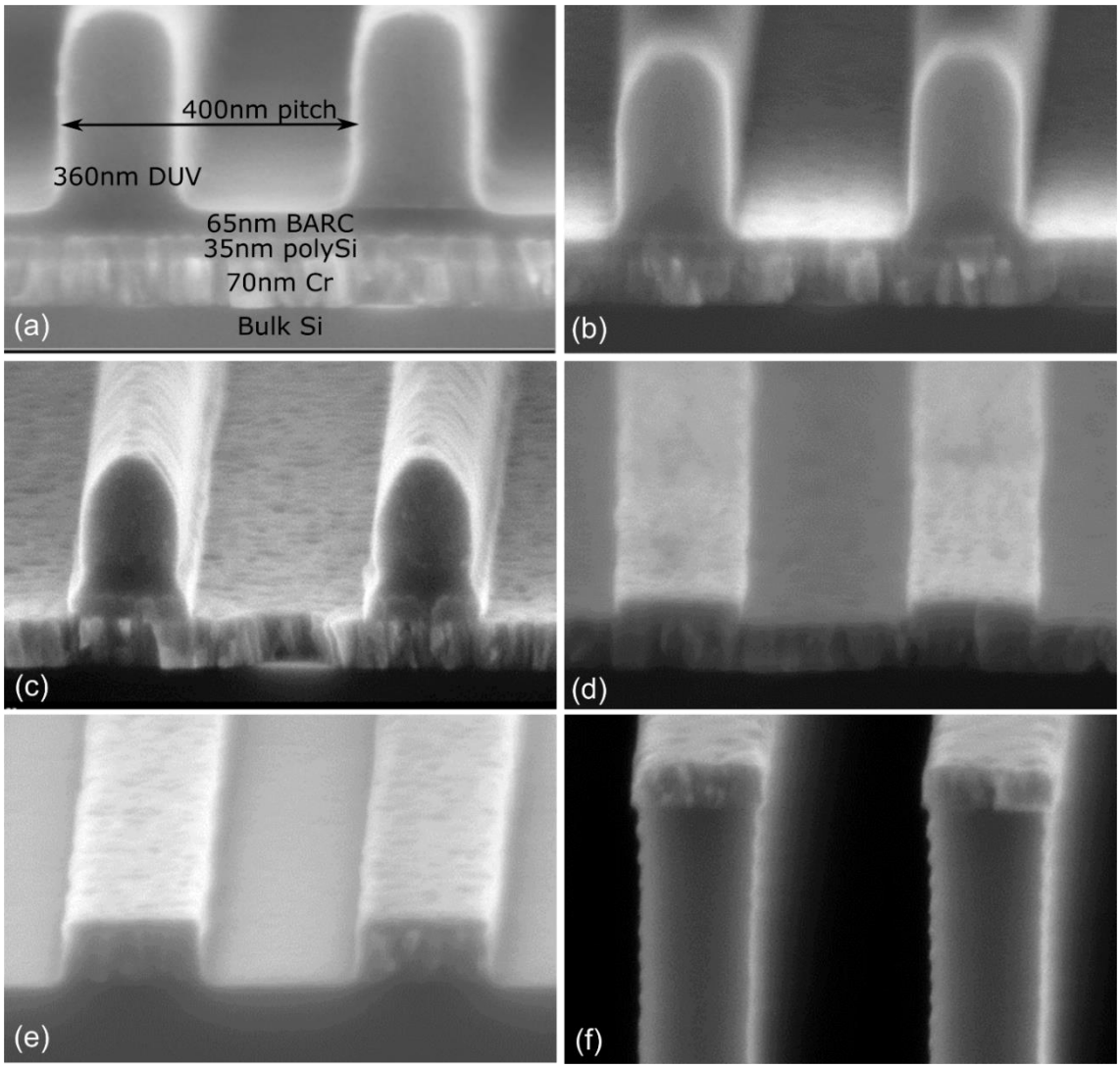

Figure 6.10. The procedure for etching 400nm pitch grating patterns composed of 360nm thick DUV resist on top of the sample stack: bulk Si + 70nm Cr + 30nm polySi + 65nm Barc. (a) the initial measures before the etch. (b) after O-based directional barc etch. (c) directional polySi etch using the switched SF_6/O_2 CORE sequence. (d) isotropic polymer strip. (e) directional Cr etch. (f) the final transfer into the bulk silicon.

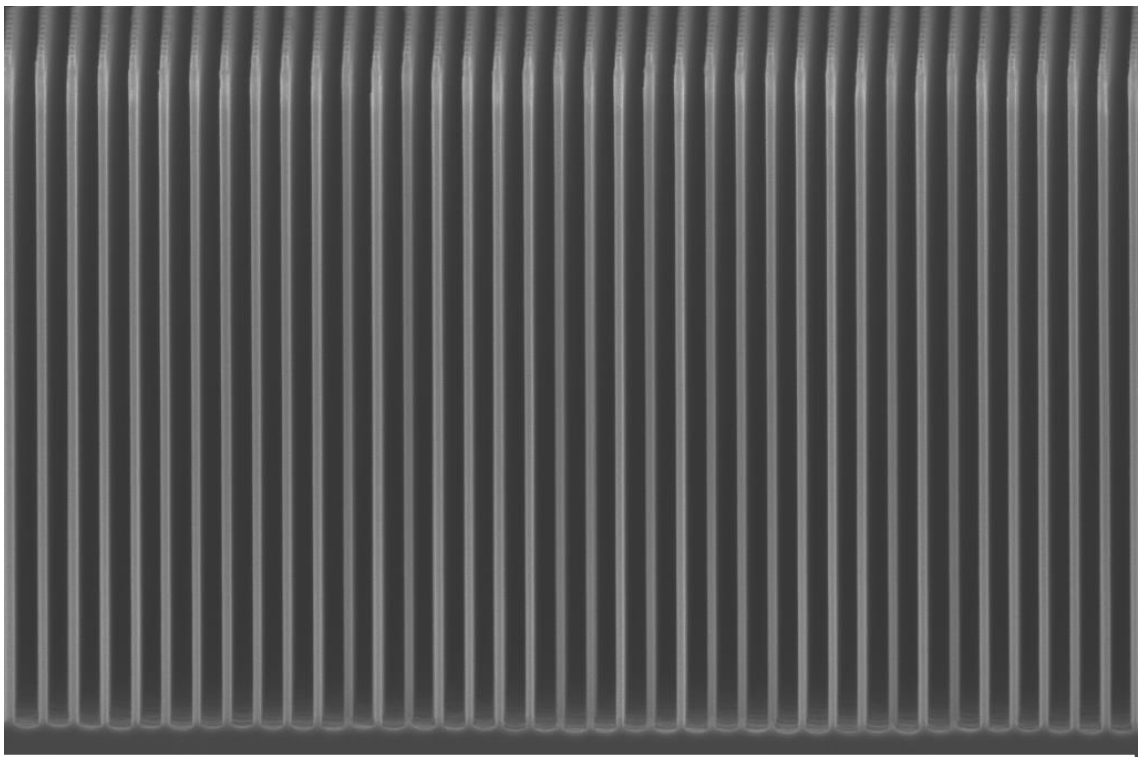

Figure 6.11. Zoom-out of Figure 6.10f after prolonging the etch time (9µm deep). The Cr mask is just gone.

The etch time in Figure 6.10f is prolonged in order to achieve a high aspect ratio silicon structures. The etch result is zoom-out in Figure 6.11 showing 9µm deep silicon gratings. Clearly, the pattern transfer proceeds with high fidelity and the 70nm Cr layer allows an aspect ratio beyond 50. However, while etch time proceeds the Cr mask shows pronounced retraction that prevents further silicon etching. Figure 6.12 shows how the Cr mask slowly erodes not only normally, but also laterally. The latter is problematic as it will degrade the topside of the nanoscale features causing erosion on the sidewall. The Cr retraction is the consequence of using O- and F-generating plasmas for the Si etching. This is true even when both plasmas are not present at the same time as in the CORE sequence. The reason is because during the O-step in the CORE sequence, the Cr surface is oxidized by the oxygen radicals and the forming CrO_x layer will be removed by the fluorine radicals in the subsequent E-step. Therefore while the silicon is patterning in the SF_6 and O_2 plasma, the Cr mask is also etched. This will restrict the maximum achievable aspect ratio of silicon with Cr as a mask.

Even though the initial results of Cr etching using a switching of SF_6 and O_2 plasma has shown a promising result, some questions remain and should be addressed in future work. The plasma does not allow the gases to be replaced instantaneously. This means that there will be a transition period where that plasma passes through the '0.75%' peak and both fluorine and oxygen radicals will etch together. This will promote undercut. To prevent

this from happening, one could introduce additional steps in between both steps. This is like the CORE sequence where the C-step has been introduced to prevent fluorine from the E-step to compete with the oxygen radicals in the O-step. In addition, the presence of O_2 in the F-step can be replaced by other gas (e.g. Ar) in order to push the Cr etch system as far as possible into the pure F-based chemistry.

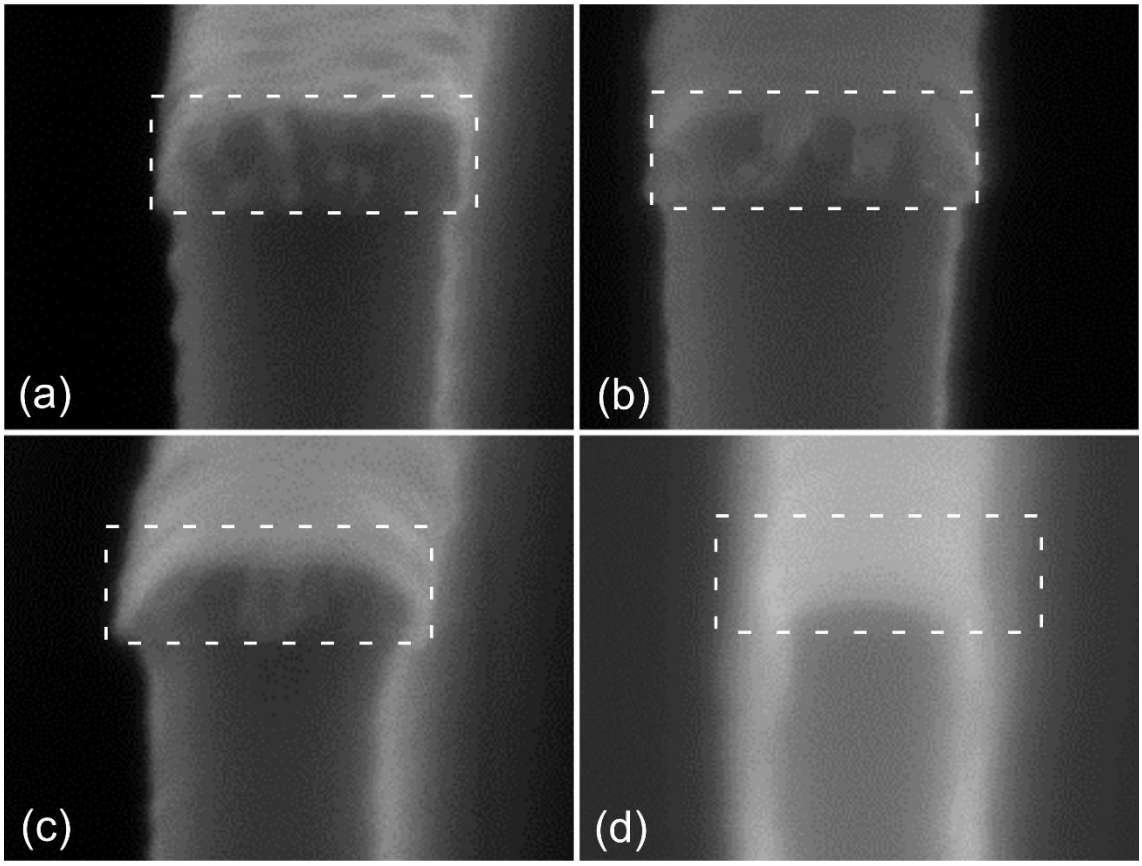

Figure 6.11. Mask retraction during SF_6/O_2 plasma etching of bulk silicon. (a) after 1hr. (b) after 2hrs. (c) after 4hrs. (d) 8hrs.

6.4. Conclusion

Chromium is a widely used material in modern nanofabrication either directly as a functional material (e.g. photomask generation) or indirectly as a hard mask (e.g. to etch quartz). In this chapter, a procedure for directional etching of Cr and CrOx is demonstrated for the first time using SF_6+O_2 plasma as an alternative of the conventional Cl-O-based plasma. The etch mechanism is explained by considering the formation of volatile chromyl fluoride in which the Cr is first reacting with O-radicals and the forming CrO_x subsequently reacts with F-radicals into CrO_2F_2. Due to the identical gas chemistries, this Cr etch procedure can be combined with the CORE sequence into a single run, thus prevents cross contamination, increases throughput and relaxes the infrastructure.

For etching non-patterned samples using the mixture of SF_6 and O_2 plasma, the Cr etch rate at 300W plasma power is up to 400nm/min at a SF_6/O_2 gas ratio below of 1%. The etch rate of CrO_x can reach much higher values (beyond 2000nm/min at 300W) without the need of O_2. For etching the patterned samples, the mixed mode procedure performs at 300W plasma power resulting in the Cr etch rates up to 150nm/min for a SF_6/O_2 gas ratio below 1%. The etch procedure is also adapted into the switched mode having the Cr etch rate around 7nm/min with high selectivity with respect to silicon (> 20) and better profile control.

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Chapter 7. Conclusions and Outlook

This chapter will summarize the results that have been achieved during the PhD project. After that, recommendations for future developments will be discussed.

7.1. Conclusion

This thesis treats a novel plasma etch process for directional nanoscale silicon etching and aiming at a more reliable and sustainable process than conventional approaches can fulfill. It is called CORE (meaning Clear, Oxidize, Remove, and Etch) and uses a switching sequence of SF_6 and O_2 plasma. As demonstrated in ***Chapter 3***, CORE is a fluorocarbon-free directional etch process operating at room temperature and using a conventional RIE tool. The switching distinguishes CORE from the old-fashioned room temperature and cryogenic mixed RIE processes. It enables the process to have a higher selectivity and creates pattern independency of etching profiles. The CORE process resembles the well-known SF_6-based Bosch process, but the usual C_4F_8 inhibitor deposition is replaced by O_2 oxidation with self-limiting characteristics. The etch result of the CORE process is in many aspects similar to the Bosch process, however has the advantage of preventing the pile-up of fluorocarbon deposits at the topside of deep-etched or nano-sized features. At the same time, process drift is minimal, as the reactor wall is staying perfectly clean. The CORE process has shown an excellent performance in high aspect ratio nanoscale structures with an accurate and controllable etch rate between 1 and 50nm/min (and SiO_2-selectivity of ca. 35) using the etch-tool in the RIE-mode. By adding the ICP source (DRIE-mode), a directional etch rate up to 1µm/min (at 50sccm SF_6 flow) and selectivity >200 for SiO_2 is possible. Due to its better stability, reliability, robustness, sustainability and tool-friendliness, the CORE process is believed to be the first switched sequence of its kind that challenges the monopoly of the established Bosch sequence. It is expected to find its position in the semiconductor and micro-system fabrication market soon.

Based on the developed CORE sequence, ***Chapter 4*** studies the formation of Black Silicon (BSi) in SF_6 and O_2 plasma. BSi is a frequently encountered phenomenon in highly directional etching of silicon using mainstream plasma etch tools. It is highly appreciated in application such as highly light adsorbing solar cell surfaces or superwetting surfaces, but can be very notorious in micro/nanofabricated devices that depend on smooth surfaces. Due to the self-limiting property of the oxidation step, the formation and controllability of BSi in the CORE sequence is different from how BSi presents itself in the FC-based sequences and it is therefore much more manageable. We show that the time in the removal (R) step of the passivating oxide layer, in tight combination with the undercut time in the isotropic etch (E) step, are the most important parameters to consider. By manipulating these two parameters and utilizing the self-limiting property of the oxidation (O) step, the CORE process can easily be modified to create either BSi-full or BSi-free surfaces independent of the aspect ratio of the etching features. The latter distinguishes the BSi formation clearly from other directional processes. The proposed CORE process thus provides us a versatile tool for creating BSi anywhere at anytime or - as we call it - 'BSi on Demand'.

The research study in ***Chapter 5*** is also built on the CORE sequence and develops a procedure for fabricating ultra-high aspect ratio (HAR) silicon nanopillars with chromium as a mask. Using the optimal parameter settings in which all the CORE steps are well balanced, it is demonstrated that 60nm of chromium masking is well suited for ultra-HAR etching without complicating the plasma process or compromising the overall fabrication procedure. Nanopillar arrays (200nm diameter, 400nm pitch and 60nm diameter, 500nm pitch) are demonstrated having smooth straight sidewalls with aspect ratios beyond 55 for gaps and up to 200 for pillars. Due to the very mild plasma condition (less than 40W RIE power), the Cr mask selectivity with respect to silicon can be tuned above 500. In addition, the clean operation of the CORE sequence (no FC pile up as is typical in the Bosch-process) prevents time-consuming profile tuning and enables process freedom and reproducibility.

Chapter 6 is an extended study of ***Chapter 5***. It proposes for the first time a novel procedure for directional etching Cr and CrO_x layers using a mixture of SF_6 and O_2. The proposed etch procedure performs excellent at 300W plasma power with etch rates of Cr up to 400nm/min for a SF_6/O_2 gas ratio below of 1%. The etch rate of CrO_x can reach much higher values (beyond 2000nm/min at 300W) without the need of O_2. The polysilicon is used as a mask resulting in a high selectivity towards chromium (> 15). Due to the identical gas chemistries, this chromium etch procedure can be combined with the CORE sequence into a single run, thus prevents cross contamination, increases throughput and relaxes the infrastructure.

7.2. Outlook

Although the achievements of this thesis have made an innovative and substantial contribution to the technical development of nanoscale silicon etching, there are still many aspects that can be improved to enable more freedom and possibilities for the fabrication of novel NEMS devices.

- The CORE process developed in ***Chapter 3*** can be further optimized to create a more generic platform for silicon etching.
  - The CORE process consists of four steps in which the C-step is included to prevent the SF_6 plasma and the created SiFx products from the preceding E-step to come into contact with the O_2 plasma in the next O-step. However, the results in Chapter 4 shows that this contact only weakens the etch sidewalls but does not trigger the formation of BSi. Therefore, we can exclude the C-step and meanwhile increase the O-step to strengthen the sidewall protection. Without the C-step, the CORE process becomes the ORE process and this will give the etch software more flexibilities in programming the recipe.
  - The plasma oxidation process in the O-step can be studied in more details to find the optimal settings that provide the strongest oxidation value as well as best uniformity. In addition to the oxidation time, other parameters such as power, pressure and their combination can be investigated further.
  - Based on the result from the O-step, parameters in the R-step also need to be tuned to create a perfect balance between the passivation and removal of this passivation layer in one etch cycle. The relationship between the R-power and R-time can be examined to answer the question about which combination is better: high power in a short time or low power for a longer time. Besides that, SF_6 is currently used in the R-step as the removal gas, but we can also investigate possibility to replace SF_6 by Ar or another gas.
  - It is known that the E-time has a prominent effect on the profile. The shorter the E-time, the more positive the profile will be. This phenomenon can be further investigated by observing the etch profile when the E-time varies e.g., from 0 to 100s with other parameters are fixed. In addition to the etch profiles, the etch rate also needs to be considered. Currently, the typical etch rate of the CORE process using the RIE settings is about 1µm/hr. This etch rate can be higher by increasing the E-power or E-flow, but it is expected that the self-limiting feature of the CORE sequence will limit the maximum etch rate.
- As mentioned in ***Chapter 5***, the silicon nanopillars are able to have a higher aspect ratio if a thicker Cr mask is used. Therefore, by optimizing the lift-off method or adapting the Cr etch procedure proposed in ***Chapter 6***, the thickness of the Cr mask could be 100nm or more. As a result, the aspect ratio of features reaching beyond 100 is believed to be feasible, but mask retraction of the Cr mask will create a limit. An

approach to get a higher aspect ratio than achievable with Cr is to use a hard mask material that does not retract during the silicon etching. Nickel or Yttrium oxide seems to be good candidates.

- The CORE process can be used to facilitate the fabrication of complex 3D silicon micro- and nanostructures with well-defined geometries that exhibit an intriguing attraction in optical and photonics applications. Some interesting devices worth for explore in a future study include Casimir-based devices, double tuning forks, AFM tips, etc.
- Besides the technological developments, another aspect rarely mentioned, but that will certainly determine future technology development and direction, is process sustainability and environmental greenishness. The conventional Bosch process relies totally on two process gases: C_4F_8 and SF_6. A substantial drawback is that both gases have very high greenhouse warming potentials and survive for thousands of years in the earth atmosphere. CORE has replaced one of these gases (C_4F_8) into the environmental-friendly O_2, but still uses SF_6 as a silicon etch gases. Therefore, the need for an alternative (green) gas that can produce high aspect ratio features in silicon is highly requested. F_2 - or H_2 - based silicon etching are good candidates to consider and implement in future research.

Appendix A. The CORE sequence

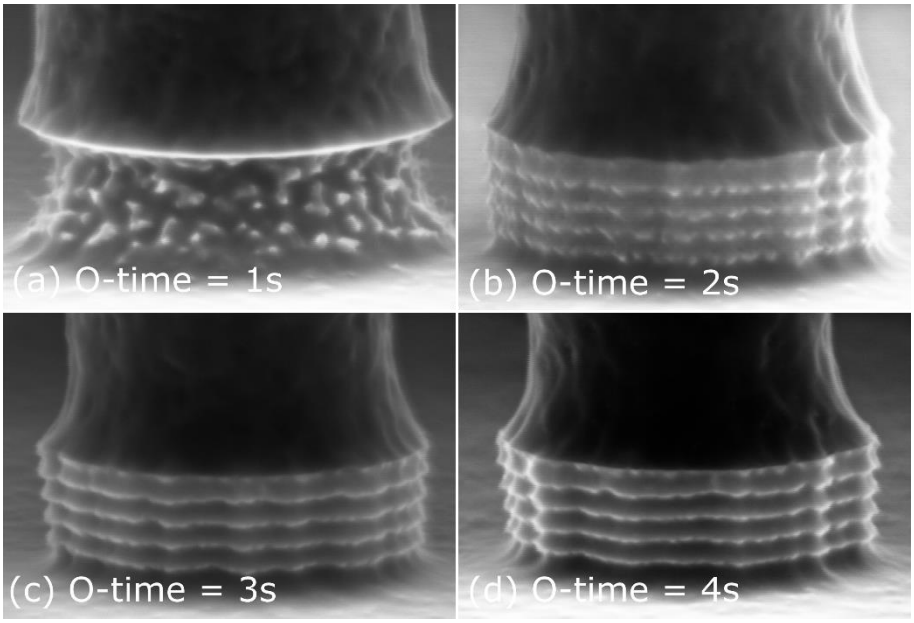

Figure A.1. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 1s. (b) O-time = 2s. (c) O-time = 3s. (d) O-time = 4s. With C-time = 4s, R-time = 20s and E-time = 2min always.

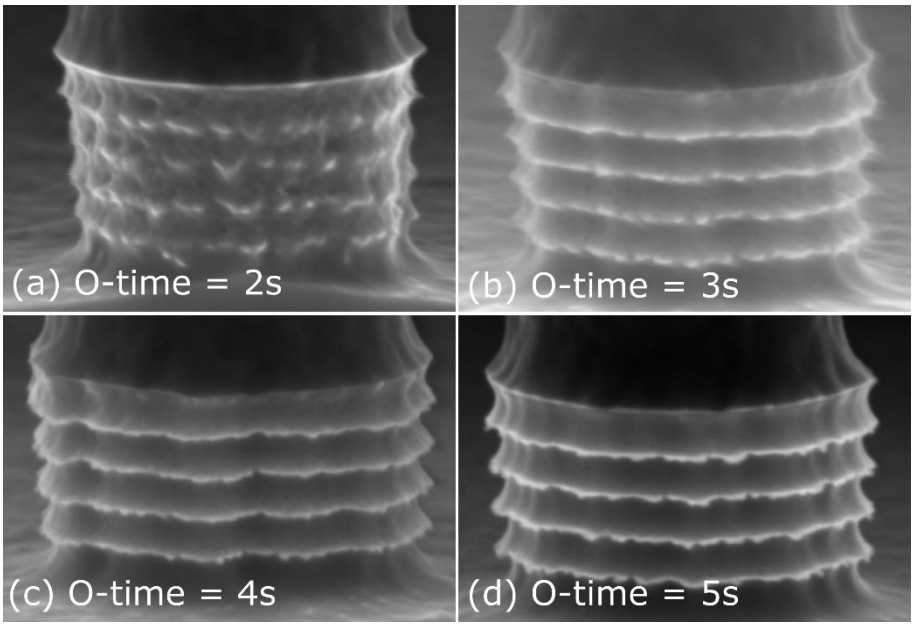

Figure A.2. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 2s. (b) O-time = 3s. (c) O-time = 4s. (d) O-time = 5s. With C-time = 4s, R-time = 20s and E-time = 4min always.

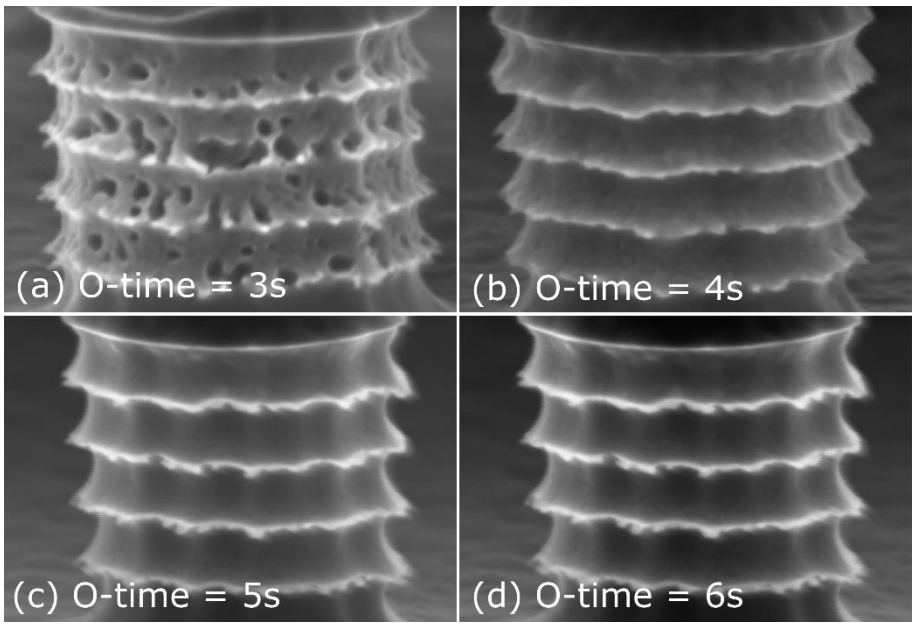

Figure A.3. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 3s. (b) O-time = 4s. (c) O-time = 5s. (d) O-time = 6s. With C-time = 4s, R-time = 20s and E-time = 6min always.

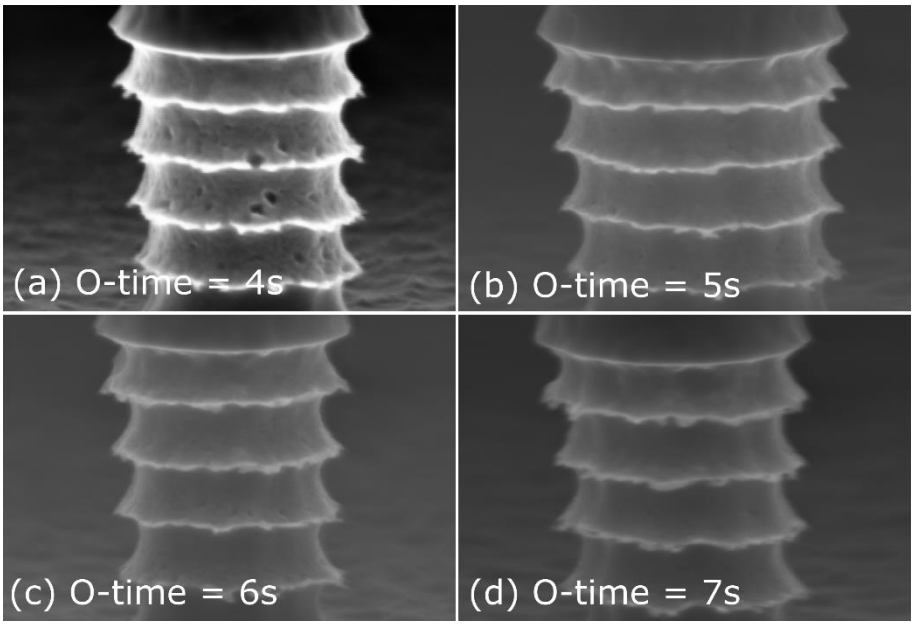

Figure A.4. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 4s. (b) O-time = 5s. (c) O-time = 6s. (d) O-time = 7s. With C-time = 4s, R-time = 20s and E-time = 8min always.

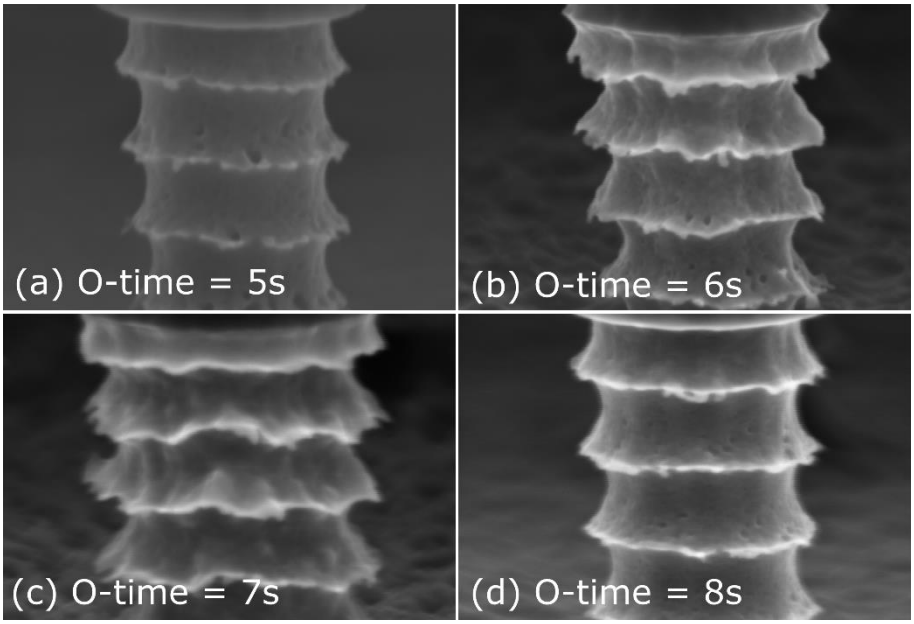

Figure A.5. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 5s. (b) O-time = 6s. (c) O-time = 7s. (d) O-time = 8s. With C-time = 4s, R-time = 20s and E-time = 10min always.

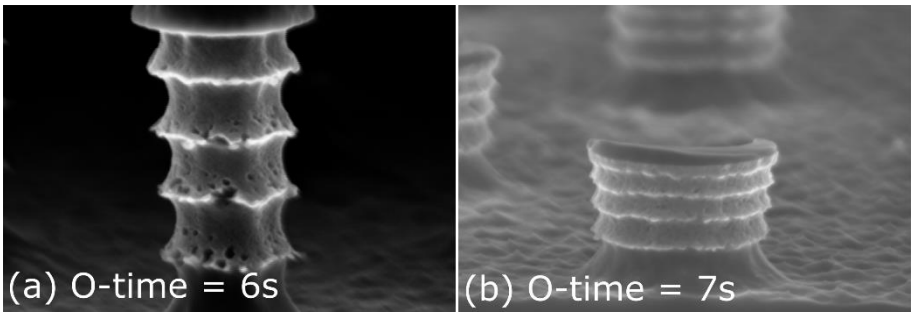

Figure A.5. Prolonged O_2 oxidation time saturates the sidewall protection. (a) O-time = 6s. (b) O-time = 7s. With C-time = 4s, R-time = 20s and E-time = 12min always.

Appendix B. Abbreviation

ALE	Atomic Layer Etching
ARDE	Aspect Ratio Dependent Etching
BiCS	Bit-Cost Scalable
Bsi	Black Silicon
CCP	Capacitively Coupled Plasma
CORE	Clear, Oxidize, Remove, And Etch
CPU	Central Process Unit
DRAM	Dynamic Random Access Memory
DREM	Deposit, Remove, And Etch Many times
FC	Fluorocarbon
FinFET	Fin Field-Effect Transistor
GAA	Gate-All-Around
HAR	High Aspect Ratio
ICP	Inductively Coupled Plasma
MEMS	Micro Electromechanical Systems
NEMS	Nano Electromechanical Systems
RF	Radio Frequency
RIE	Reactive Ion Etching
$SiCl_4$	Silicon Chlorides
SiO_xF_y	Silicon Oxy Fluoride
TSVs	Through-Silicon Vias
VLSI	Large Scale Integration

Appendix C. List of publication

Journal papers

[1]. **Nguyen, V.T.H.**, Silvestre, C., Shi, P., Cork, R., Jensen, F., Hubner, J., Ma, K., Leussink, P., de Boer, M. and Jansen, H., 2020. The CORE Sequence: A Nanoscale Fluorocarbon-Free Silicon Plasma Etch Process Based on SF_6/O_2 Cycles with Excellent 3D Profile Control at Room Temperature. ECS Journal of Solid State Science and Technology, 9(2), p.024002

[2]. **Nguyen, V.T.H.**, Jensen, F., Hübner, J., Leussink, P. and Jansen, H., 2020. On the formation of black silicon in SF_6-O_2 plasma: The clear, oxidize, remove, and etch (CORE) sequence and black silicon on demand. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 38(4), p.043004.

[3]. **Nguyen, V.T.H**., Shkondin, E., Jensen, F., Hübner, J., Leussink, P. and Jansen, H., 2020. Ultrahigh aspect ratio etching of silicon in SF_6-O_2 plasma: The clear-oxidize-remove-etch (CORE) sequence and chromium mask. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 38(5), p.053002.

[4] Silvestre, C.M., **Nguyen, V**., Jansen, H. and Hansen, O., 2020. Deep reactive ion etching of 'grass-free'widely-spaced periodic 2D arrays, using sacrificial structures. Microelectronic Engineering, 223, p.111228.

[5] Nguyen, V.T.H., Shkondin, E., Jensen, F., Hübner, J., Leussink, P. and Jansen, H. High rate and selective Cr and CrOx Etching using SF_6 and O_2 Plasma. *Manuscript is in preparation.*

Conference contribution

Nguyen, V.T.H., Jensen, F., Hübner, J., Leussink, P. and Jansen, H (2019). On the formation of Black Silicon in SF_6-O_2 plasma: The CORE sequence and BSi on Demand. 45th International conference on Micro and Nano Engineering - Rhodes, Greece. (oral presentation).