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High-Speed SiGe BiCMOS Detector Enabling a 28 Gbps Quasi-Coherent Optical Receiver

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***Abstract*—This brief presents a high-speed detector targeting quasi-coherent optical receivers operating up to 28 Gbps data rates. The circuit consists of a balanced rectifier based on diode-connected heterojunction bipolar transistors (HBTs) together with tailored input and output filtering networks. The rectifier is buffered by a linear DC-coupled single-ended to differential amplifier providing a $50\,\Omega$ output interface. The design was fabricated in a commercial 130 nm SiGe BiCMOS technology with f_t/f_{max} of 250/340 GHz, and was tested on a quasi-coherent receiver setup. Optical receiver sensitivity better than -28 dBm and -26 dBm (FEC-limited BER of 1E-3) is demonstrated, respectively, at 25 and 28 Gbps data rates. To the best of the author's knowledge, the reported circuit represents the fastest envelope detector published to date.**

***Index Terms*—Analog processing circuits, Application specific integrated circuits, Demodulation, Envelope detectors, High-speed integrated circuits, Nonlinear circuits, Optical receivers, Rectifiers, SiGe BiCMOS.**

I. Introduction

Global data trafic has experienced an ever-increasing growth, a trend that is expected to continue in the foreseeable future [1]. Access network technologies have responded to the challenge with increased fiber deployment [2], while new solutions emerge aiming to fully exploit these networks in terms of data rates, reach, and overall efficiency [3]. Commonly employed direct-detection receivers based on high-speed avalanche photodetectors (APDs) provide a simple and cost-effective solution, both desirable merits within access networks. However, this type of receiver faces major limitations to achieve longer reach, where fiber chromatic dispersion at typical C-Band optical wavelengths impairs performance in uncompensated links. Moreover, dedicated filtering for channel selection is required in systems employing wavelength division multiplexing (WDM).

Recently, quasi-coherent receiver solutions targeting intensity-modulated schemes have received attention [4]. This type of receiver offers an attractive compromise between cost, complexity and performance, enabling dispersion compensation techniques at the receiver end, advanced amplitude modulation formats towards higher data rates, and filterless WDM channel selectivity [5], [6].

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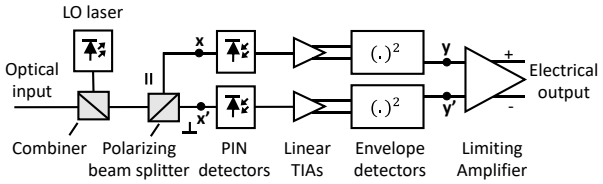


Fig. 1. Block diagram of a quasi-coherent receiver implementation with polarization diversity. The LO laser boosts sensitivity and preserves phase information. Both polarizations are treated independently by a PD-TIA-ED chain and combined at the last stage (limiting amplifier/CDR).

A simplified block diagram of a quasi-coherent receiver implementation is shown in Fig. 1. A local oscillator (LO) laser is combined with the received optical signal using an optical coupler. A polarizing beam splitter (PBS) separates the optical signals into orthogonal polarization components, which are processed by independent receiver branches. This ensures that the receiver in Fig. 1 can operate for any incoming signal polarization without the need for polarization control. The square-law power-to-current nature of photodetectors (PDs) produces heterodyning of the combined optical signals, which translates the received information to an intermediate frequency (IF) band. Linear transimpedance amplifiers (TIAs) are used to raise the IF signal level, after which the baseband information is recovered by means of envelope detection. The detected signals for each polarization are finally combined in a limiting amplifier or clock and data recovery (CDR) block for further processing. Since phase information is preserved at the IF, dispersion compensation techniques can be applied before detection. Moreover, a shot-noise limited receiver can be approached due to the use of the LO, achieving the highest possible receiver sensitivity. The use of envelope detection in the quasi-coherent receiver avoids expensive, complex and power-hungry digital or analog signal processing blocks commonly found in alternative coherent-based receivers (e.g. [7], [8]). In this way, a high performance receiver is obtained at contained cost and transceiver power budget suitable for access networks.

Key to the performance of this receiver is an envelope detector circuit capable of high data-rate demodulation. This brief describes the design and testing of a high-speed envelope detector towards silicon-based quasi-coherent receivers up to 28 Gbps data rates. A commercial SiGe BiCMOS technology with f_t/f_{max} of 250/340 GHz was chosen for fabrication. The

following sections review, respectively, the operation principle of this detector within a quasi-coherent receiver, the circuit design aspects, and a series of system tests to validate the performance of the fabricated detector.

II. Envelope Detection in Quasi-coherent Receivers

In general terms and for each polarization, the incident field at a given photodetector in the receiver of Fig. 1 can be expressed (equivalently for nodes x and x') as $E_{in}(t) = E_{LO}(t) + E_s(t)$, where the individual fields can be written as

$$\begin{aligned} E_s(t) &= A_s(t)e^{-j(\omega_s t+\phi_s(t))}, \\ E_{LO}(t) &= A_{LO}e^{-j(\omega_{LO}t+\phi_{LO})} \end{aligned} \tag{1}$$

$A_s(t)$ and A_{LO} represent normalized field amplitudes of signal and LO fields, respectively. Under incident light, a photodetector generates a photocurrent given by

$$I_p = R \cdot P_{in} \propto R \cdot |E_{in}|^2 \tag{2}$$

where R is the responsivity of the photodetector and P_{in} the incident optical power. The squaring term on the electric field leads to a mixing effect, where only the mixing terms within the photodetector electrical bandwidth will appear at the output. The resulting photocurrent becomes

$$\begin{aligned} I_p(t) \propto R \cdot |E_s(t) + E_{LO}(t)|^2 = \\ = RP_s(t) + RP_{LO} + 2R\sqrt{P_{LO}P_s(t)}cos(\omega_{IF}t + \phi_{IF}) \end{aligned} \tag{3}$$

where $P_s(t) = A_s^2(t)$ and $P_{LO} = A_{LO}^2$. The different terms in (3) correspond to a direct-detection term $RP_s(t)$, a DC component RP_{LO}, and the desired IF component, where $\omega_{IF} = \omega_s - \omega_{LO}$ and $\phi_{IF} = \phi_s(t) - \phi_{LO}$. Amplitude and phase information of the received signal are thus preserved in the IF term, while the remaining terms can be filtered out. The LO laser is tuned to produce an IF signal centered within the PD-TIA bandwidth for a selected channel. For intensity-modulated transmitters where phase modulation is not employed ($\phi_s(t) = const$), the received information is contained in the term $P_s(t)$, while being boosted by P_{LO}. In this case, the IF becomes an amplitude modulated (AM) signal with carrier frequency ω_{IF}, which can be demodulated by envelope detection based on classical diode topologies. From (3), it can also be noted that linear-in-power intensity modulations will show compression of the level spacing compared to the original information caused by the square-root factor affecting $P_s(t)$. For NRZ formats, this has no repercussion as long as the output level reaches the desired amplitude and bit error rate (BER) value. For multi-level modulation formats (e.g. PAM-4), the square-law characteristic of diode-based envelope detectors can recover the original level spacing, for which the detector input level must remain within the square-law regime of the diodes [9].

III. Circuit Design

Fig. 2 shows a schematic of the proposed detector circuit. Its main functional blocks, corresponding to the rectifier circuit and following baseband amplifier, are discussed next.

A. Detector circuit

The detector circuit, shown in Fig. 2, consists of a balanced rectifier formed by a pair of diode-connected heterojunction bipolar transistors (HBTs), as high quality Schottky diodes are not available in the technology. Rectification of the input voltage produces current terms including the recovered baseband signal together with undesired higher-order mixing terms [9]. Assuming a balanced input signal and well matched diodes, odd-order mixing terms are cancelled in a balanced rectifier [10], while even-order terms can be removed by filtering.

The differential inputs to the rectifying diodes include high-pass filters (HPFs) having a dual purpose. First, significant filtering of the direct-detection term $RP_s(t)$ in (3) is achieved, which can extend the receiver dynamic range. At the same time, the HPF provides a short-circuit termination for the baseband current terms at the detector input. This prevents any voltage from being developed at this node, thus maximizing available baseband power that can be delivered to the load and reducing distortion due to generation of further mixing products [9]. A cut-off frequency of 10 GHz was found to be a good compromise to achieve these benefits while consuming a contained portion of PD-TIA bandwidth. The HPF also provides biasing to the diodes so that they operate on their conduction threshold for maximum responsivity. A separate supply (labeled V_{BED} in Fig. 2) is used for this purpose, which allows to fine tune the operating point and reduce it under large drive levels to stay within the square-law regime. This supply operates nominally at 3.3 V coinciding with the VCC supply. A low-pass filter (LPF) follows the rectifier, providing a short-circuit termination for even-order terms, the second harmonic being the dominant one. The order and frequency response of the LPF were optimized taking into account the response of the baseband amplifier following the detector to yield a combined 3 dB cutoff around 19 GHz.

B. Baseband amplifier

A linear DC-coupled baseband amplifier buffers the detector circuit. A common base (CB) stage acts as a current buffer, where transistor sizing was selected to provide optimal loading to the LPF. A degenerated common-emitter (CE) differential stage serves both as single-ended to differential converter and $50\,\Omega$ output buffer. The purpose of the single-ended to differential conversion is to provide selectable inverting and non-inverting outputs (V_{D+}, V_{D-}), so that signals at nodes y and y' in the receiver of Fig. 1 can be readily combined in a differential limiter circuit. In each case, the complementary output is intended for monitoring, but can also be terminated externally, or internally via wirebonds to the on-chip terminations V_{T+} and V_{T-} accessed through on-chip pads. The emitter degeneration resistor R_E increases the linearity of the differential pair to maintain compatibility with PAM-4 formats. A value of $40\,\Omega$ was chosen, which did not compromise single-ended to differential conversion significantly. A dummy detector is used to match the DC levels at the inputs of the differential pair. An additional shunt resistor before the CB stage cushions self-biasing effects and sinks additional current under higher drive levels, which prevents

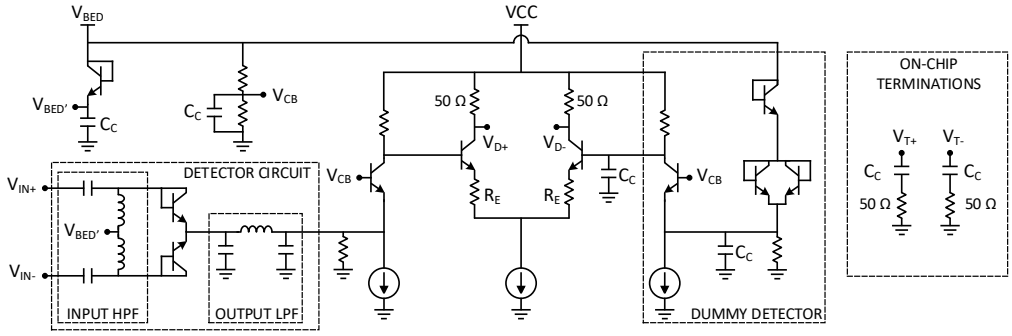


Fig. 2. Schematic of the proposed high-speed detector.

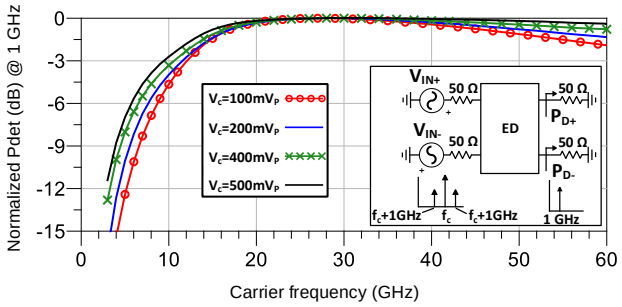


Fig. 3. Post-layout simulation of the complete detector with an AM signal.

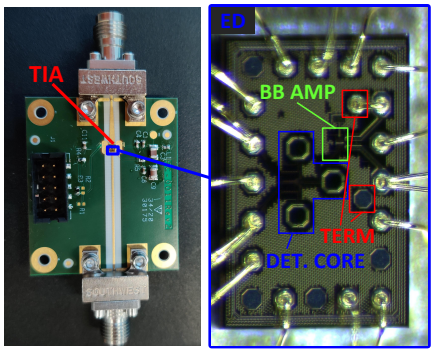


Fig. 4. Evaluation board hosting a commercial linear TIA and the fabricated envelope detector, shown magnified on the right. Marked areas on the chip show the placement of the detector core, baseband linear amplifier, and internal pads for on-chip termination of unused outputs.

build-up of excessive DC offset that can affect the balance of the outputs. Additionally, this resistor improves matching of the LPF to the CB without affecting the transconductance of this stage. Finally, all current sources are implemented as cascoded current mirrors. Post-layout simulation of the standalone amplifier (without detector and and filter) on a 50 Ω environment shows a differential voltage gain of 10 dB (6 dB for power gain) at 1 GHz, with 1 dB compression point at -8 dBm input power (-5 dBm single-ended output power).

Fig. 3 shows a post-layout simulation of the complete detector circuit. The circuit is driven differentially from $50\,\Omega$ sources, feeding an AM signal with carrier frequency f_c and sidebands at $f_c \pm 1$ GHz. The plot shows normalized detected output power (at 1 GHz) as a function of f_c (swept from 3 to 60 GHz). Different carrier amplitude levels (V_c) are reported, where sideband amplitudes are set ten times lower than the carrier for each case. The detector response is dominated by the HPF in the lower end, while showing only mild performance degradation towards higher carrier frequencies. At 30 GHz, a simulated conversion loss of 6.1 dB and 4.2 dB was obtained, respectively, for 100 mV_p and 500 mV_p carrier levels, defined as the differential input power to the detector at $f_c \pm 1$ GHz relative to the single-ended output power (e.g. P_{D+}) at 1 GHz. A chip photograph is reported in Fig. 4. The chip has dimensions of 0.7 mm × 1.1 mm and has a nominal power consumption of 78 mW from a single 3.3 V supply.

IV. Measurement Results

Fig. 5 shows the system setup used to verify the performance of the fabricated circuit. It represents a single-polarization version of the quasi-coherent receiver in Fig. 1. An externally modulated laser (EML) is employed as a transmitter, having a center wavelength of 1561.41 nm, 2.9 dBm output power and 9 dB extinction ratio (ER). The transmitter is followed by a variable optical attenuator (VOA) to adjust the received signal power coming into the receiver, after which LO and received optical signals are combined in an optical coupler. Polarization of both LO and incoming signal is adjusted by means of polarization controllers to maximize one of the outputs of the polarizing beam splitter, which is then connected to an electrical front-end for detection and recovery of the baseband information.

The electrical front-end consists of a commercial packaged waveguide photodetector (50 GHz bandwidth) and a tailored evaluation board hosting both a commercial linear TIA and the fabricated detector. The TIA has 34 GHz bandwidth, 5 kΩ differential gain and 2.6 uA_{RMS} input referred noise (on 30 GHz bandwidth). The photodetector connects through coaxial interface to the evaluation board, and features an internal $50\,\Omega$ load resistor. The internal loading adds excess thermal noise before the TIA and sinks part of the generated photocurrent, which can compromise sensitivity. However, this

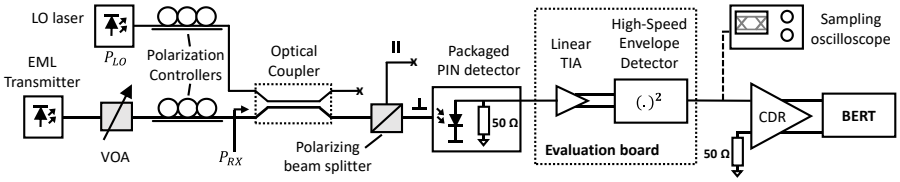


Fig. 5. Simplified single-polarization quasi-coherent receiver for testing of the fabricated high-speed detector.

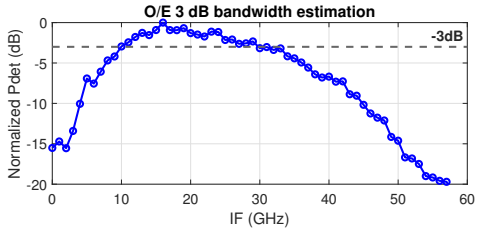


Fig. 6. Estimation of the O/E bandwidth of the electrical front-end (PD-TIA-ED) by means of a 3 Gbps NRZ transmission with swept IF center frequency.

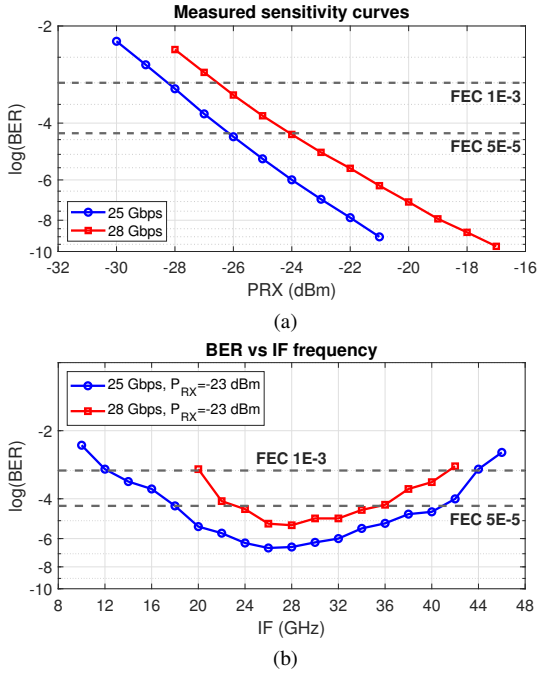


Fig. 7. NRZ data reception: (a) Measured sensitivity curves for 25 and 28 Gbps NRZ transmission with 12 dBm LO power (P_{LO}). Marker lines indicate typical FEC limits of 1E-3 (e.g. PON) and 5E-5 (e.g. Ethernet); (b) BER as a function of IF carrier frequency for 25/28 Gbps showing low dependence on wavelength drift. FEC limits indicated as per (a).

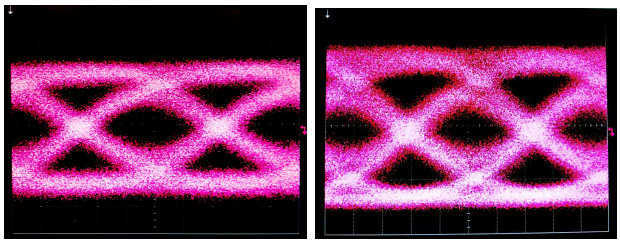
solution was preferred over a more complex setup with bare die photodetectors in order to simplify testing. The evaluation board is shown in Fig. 4 together with a detailed view of the bonded detector chip. TIA and envelope detector are connected directly by chip-to-chip wirebonds. For the single polarization setup, only one of the detector outputs is used, while the other one is bonded to the nearby internal pad providing on-chip termination as shown in Fig. 4. A commercial CDR block and a bit-error-rate testset (BERT) complete the setup.

In order to estimate the opto-electrical (O/E) bandwidth of the electrical front-end, a narrowband 3 Gbps NRZ signal was transmitted, and the signal power after envelope detection was measured in an oscilloscope. The IF, controlled by tuning the LO wavelength, was swept in 2 GHz steps while keeping all power levels constant. The resulting curve shown in Fig 6 represents normalized output power (on $50\,\Omega$) as a function of IF center frequency, and provides an estimation of O/E bandwidth of the electrical front-end. The estimated 3 dB response covers a 20 GHz band, defined on the lower end by the high-pass filter in the envelope detector, and limited on the higher end by TIA bandwidth.

Next, sensitivity curves were measured for an optimal IF placement. 25 and 28 Gbps NRZ modulations were applied to the transmitter laser and the received optical power (P_{RX}) was swept while keeping the LO power (P_{LO}) constant at 12 dBm. This is shown in Fig. 7a where BER is plotted against P_{RX}. Marked on the plot are the 1E-3 and 5E-5 forward error correction (FEC) limits typical in passive optical networks (PON) and Ethernet standards, respectively. The sensitivity at the 1E-3 FEC limit is better than -28 dBm and -26 dBm received optical power for 25 and 28 Gbps respectively, respresenting a 6 dB improvement over results previously reported in [6]. For the 5E-5 FEC limit, the sensitivity in both cases is 2 dB lower that the aforementioned values.

An IF sweep was also performed in order to assess the tolerance to IF placement, which can be affected by wavelength drift and detuning of both LO and transmitter lasers. Low BER dependency to IF placement is desirable to relax the requirement to tightly control laser wavelength, especially on the transmitter side. Fig. 7b shows BER as a function of IF center frequency for 12 dBm LO power and -23 dBm received optical power, at 25 and 28 Gbps. The best BER values are obtained for an IF center frequency around 26 GHz, corresponding to the midband of the electrical front-end response as estimated by Fig. 6. BER decreases towards higher and lower carrier frequencies, which is mainly attributed to the partial filtering of the IF sidebands. At 25 Gbps and -23 dBm received optical power, the BER stays below the 1E-3 FEC limit for an IF center frequency in the range of 12 to 44 GHz, showing low dependence to IF placement and achieving a bitrate to carrier frequency ratio above 200% with a 12 GHz carrier, enabled by the filtering of the lower sideband. Both VCC and the detector bias voltage V_{BED} were fixed at the nominal 3.3 V throughout this test.

Eye diagram measurements taken from a sampling oscillo-



(a) (b)

Fig. 8. Eye diagrams taken from a sampling oscilloscope (without CDR module) at: (a) 25 Gbps; (b) 28 Gbps. In both cases, 12 dBm LO power (P_{LO}) and -25 dBm received optical power (P_{RX}) are used, obtaining similar eye amplitudes of 51 mV_{pp} (a) and 52 mV_{pp} (b) through TIA gain adjustment.

TABLE I
STATE-OF-THE-ART FOR HIGH-SPEED ENVELOPE DETECTORS

Ref	f_c (GHz)	R_b (Gbps)	BER	P_{DC} (mW)	FoM (pJ/bit)	Technology
[11]	300	24	<1E-4[1]	165	6.88[1a]	250 nm InP HBT
[12]	101	26	N/A	0	0[2]	35 nm InGaAs mHEMT
[13]*	60	17	<1E-12	6.1	0.36	45 nm CMOS
[14]	60	11.5	1E-12[3]	27.5	2.4	250 nm SiGe BiCMOS
This work	12-42**	28	<1E-9[4]	78	2.79	130 nm SiGe BiCMOS

* Provides simulation data only.
** For -23 dBm pre-FEC sensitivity (BER<1E-3) at 25 Gbps, cf. Fig. 7b.
[1] Estimated from measured Q. Wireless transmission including transmitter and a receiver formed by Lens+Antenna+RF Amplifier+Detector. [1a] Calculated from reported data accounting for detector power consumption only.
[2] Calculated from reported data.
[3] Measured with Modulator+Demodulator(detector) chips directly connected.
[4] Real-time measurement down to 1E-9 using full optical receiver including Optics+PD+TIA+ED (Fig. 5). No errors observed below this value.

scope are also reported in Fig. 8, with CDR block and BERT bypassed as indicated in Fig. 5. Fig. 8a shows the eye at 25 Gbps data rate, while Fig. 8b corresponds to 28 Gbps, both taken with an LO power of 12 dBm and -25 dBm received optical power. Open eyes are achieved in both cases, and no overshoot or excessive jitter appear to be present.

Finally, the proposed circuit is benchmarked in Table I against the state-of-the-art in high-speed detectors. The table reports carrier frequency f_c, maximum achieved bitrate R_b and associated BER, power consumption, energy efficiency in pJ/bit and technology used for chip fabrication. The reported circuit achieves record demodulating speed among reported detectors in different technologies.

V. CONCLUSION

The design and testing of a high-speed envelope detector has been presented enabling high-performance quasi-coherent receivers up to 28 Gbps. The detector is based on a 130 nm SiGe BiCMOS technology, where diode-connected HBTs are used in a balanced rectifier configuration and followed by a linear buffer amplifier. Testings on a receiver setup demonstrate an optical receiver sensitivity better than -28 dBm at 25 Gbps NRZ, and better than -26 dBm at 28 Gbs NRZ. The reported detector achieves record demodulation speed among state-of-the-art detectors in different technologies.

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