

# Universal mains high power-density ac-dc converter

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*Publication date:*
2021

*Document Version*
Publisher's PDF, also known as Version of record

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 October 2021 (07.10.2021)

WIPO | PCT

(10) International Publication Number
WO 2021/198075 A1

(51) International Patent Classification:
*H02M 1/42* (2007.01) *H02M 7/06* (2006.01)
*H02M 3/07* (2006.01) *H02M 1/00* (2006.01)

(21) International Application Number:
PCT/EP2021/057952

(22) International Filing Date:
26 March 2021 (26.03.2021)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20167496.7 01 April 2020 (01.04.2020) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) Title: UNIVERSAL MAINS HIGH POWER-DENSITY AC-DC CONVERTER

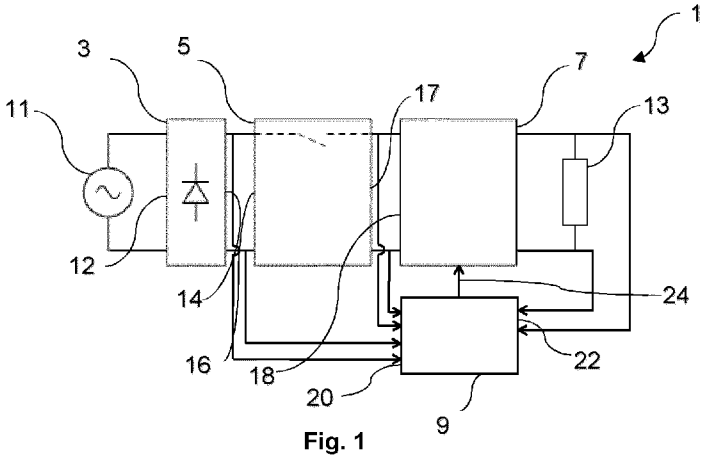


Fig. 1

(57) Abstract: The invention regards an AC-DC converter comprising a rectifier comprising a first input configured to receive an AC signal, and a first output, wherein the rectifier is configured to rectify the AC signal to a first rectified AC signal having a first VRMS, a voltage scaling circuit comprising a second input connected to the first output, wherein the second input is configured to receive the first rectified AC signal, and a second output, wherein the voltage scaling circuit is configured, if the first VRMS is within a first voltage range, to scale the first rectified AC signal by a first scaling factor generating a second rectified AC signal, a power factor correction (PFC) circuit for keeping the current in phase with and proportional to the voltage of the second rectified AC signal. the PFC circuit comprising a third input connected to the second output, and a third output configured to supply a DC signal on an AC-DC converter-output.

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TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

— *of inventorship (Rule 4.17(iv))*

**Published:**

— *with international search report (Art. 21(3))*

# Universal Mains High Power-Density AC-DC Converter

## Field of Invention

The invention relates to a high power-density universal-mains AC-DC Converter.

## Background of the Invention

Power factor correction (PFC) in AC-DC power converters is required in many applications. In the case of lighting equipment, the European Standard specifies power factor requirements for > 25W rated solutions. At such low power levels, the PFC circuit is often a limiting factor for power density. Furthermore, universal offline power converters are required to adopt different variations of input RMS voltages ranging from 100V to 240V. As a result, universal PFC circuits must handle approximately double current or double voltage for the same power transfer at either of the input condition extremes compared to the opposite extreme. This variation results in difficulties in the optimization of key power processing components, which often lead to bulky circuit implementations.

US 2010/289423 discloses a PFC in a DC-DC power converter with a controller with feedback from the output and feedforward from the input. US 2010/289423 further discloses a single inductor-based buck-boost converter, where control of the PFC is by the buck-boost converter and where voltage scaling is also based on the buck-boost converter.

US 2010/109571 discloses a DC-DC converter that is electrically isolating the input and the output by being transformer-based.

## Summary of the Invention

Considering the prior art described above, it is an object of the present invention to present a PFC circuit, where the key power processing components can be optimized irrespective of the input voltage.

The object can be achieved by means of an AC-DC converter according to claim 1.

The second rectified AC signal has a voltage and a current, which have a phase shift. A purpose of the power factor correction (PFC) circuit is to minimize the phase shift of the current in relation to the phase of the voltage of the second rectified AC signal. When the phase shift of the voltage and the current is minimised and the voltage and the current are substantially in phase, the real power is almost equal to the apparent power and the reactive power is almost zero, reducing the amount of non-productive power, so that nearly all of the power provided can be utilised by the load.

Alternatively, the phase shift of the voltage of the second rectified AC signal can be minimized in relation to the phase of the current of the second rectified AC signal. The voltage scaling circuit can be a voltage divider or a current multiplier when the first $V_{RMS}$ is within a certain upper range, or the voltage scaling circuit can be a voltage multiplier or a current divider when the first $V_{RMS}$ is within a certain lower range. The purpose of the voltage scaling circuit is to expose the PFC circuit to similar conditions irrespective of whether the received AC signal on the first input is AC mains with a voltage of around 120 $V_{RMS}$ or around 230 $V_{RMS}$. Either a first scaling factor above one is applied to the rectified lower voltage, like e.g. 120 $V_{RMS}$, and the rectified upper voltage, like e.g. 230 $V_{RMS}$, is uninfluenced or at least substantially uninfluenced by the voltage scaling circuit, or the first scaling factor is below one and the first scaling factor is applied to the rectified upper voltage and the rectified lower voltage is uninfluenced or at least substantially uninfluenced by the voltage scaling circuit.

That the PFC circuit is exposed to similar conditions irrespective of the received AC signal on the first input means that the PFC circuit can be designed so that there will be lower voltage stresses (in case of scaling voltage down) or lower current stresses (in case of scaling voltage up) on the whole circuit and particularly on the PFC circuit, and so that the PFC circuit can allow much higher switching frequency, and hence smaller magnetic components. The whole circuit comprises the rectifier, the voltage scaling circuit, and the PFC circuit, and maybe a control circuit.

The rectifier – if used without a PFC circuit – can distort the current waveform to a non-sinusoidal waveform so that unwanted harmonic currents and/or voltages are created in addition to the fundamental frequency of the signal. The harmonic currents are unwanted, since the high frequencies of the harmonic currents can be fatal to some

electrical components in the circuit and, since the high frequencies can cause e.g. increased heating.

Another purpose of the power factor correction (PFC) circuit can be to change the shape of the current and/or voltage waveform to a sinusoidal waveform to remove the unwanted harmonic currents, e.g. by filters.

If the voltage scaling circuit can be a voltage divider or a current multiplier, a further advantage is that the whole circuit can be used to produce a lower output voltage depending on the voltage scaling circuit.

The AC-DC converter can be configured or suitable for receiving a high power AC signal and convert the high power AC signal to a DC signal, where high power AC signal can be at least 100 $V_{RMS}$ or between 100-500 $V_{RMS}$ like e.g. AC mains. For an alternating electric voltage, $V_{RMS}$, the root-mean-square voltage of the signal, can be equal to the value of the direct current that would produce the same average power dissipation in a resistive load.

The AC-DC converter according to the present disclosure reduces the PFC converter size by 30% compared to the state-of-the-art converters with a comparable efficiency and results in a simplification of the down-stream DC-DC converter.

The PFC circuit operation can be controlled, configured or designed to supply a constant DC voltage at its output. It is capable of supplying a constant output voltage while minimising voltage-current phase shift and reducing unwanted harmonic content as described above by utilising internal energy storage component(s). The PFC circuit can use sensing of the second signal voltage and current (after rectifier) or sensing of the third signal voltage and current (after voltage scaling) or sensing of the fourth signal (after PFC) voltage or any combination of these signals to control its operation.

The voltage scaling circuit can be a voltage scaling AC-AC circuit configured for providing a scaled AC from the input AC, i.e. AC-AC conversion, so that the voltage scaling circuit does not require a controller changing the switches duty-cycle along the input line voltage.

The AC-DC Converter can be suitable for universal AC mains, which means 120 $V_{RMS}$ and 230 $V_{RMS}$.

In an embodiment, the voltage scaling circuit can be a switched-capacitor circuit.

Using switched-capacitor circuits – with no need for magnetic devices such as inductors or transformers, and in addition at low costs and easy integration in an integrated circuit – is beneficial in terms of low energy consumption, and high power density.

In an embodiment, the first voltage range can be a certain lower range, which can be below a first limit, or a certain upper range, which can be above the first limit, wherein the first limit can be between 140 and 200 $V_{RMS}$, more preferably between 150 and 180 $V_{RMS}$.

AC mains are generally either 120 $V_{RMS}$ or 230 $V_{RMS}$, so that the first limit somewhere between 140 and 200 $V_{RMS}$ will always distinguish between AC mains of 120 $V_{RMS}$ or 230 $V_{RMS}$. AC mains voltage has a tolerance. It is normal to have an input mains voltage lower or higher than the nominal values according to the specified range. To be on the safe side the first limit can be somewhere between 150 and 180 $V_{RMS}$.

In an embodiment, the voltage scaling circuit can be configured to scale the first rectified AC signal by a second scaling factor different from the first scaling factor, if the first $V_{RMS}$ is within a second voltage range different from the first voltage range generating a third rectified AC signal.

By a second scaling factor different from the first scaling factor acting, wherein the first scaling factor and the second scaling factor are applied within two different ranges, two voltage ranges of the first rectified AC signal can be brought close to a third range, or two voltage ranges of the first rectified AC signal can be brought closer to each other, wherein for both voltage ranges of the first rectified AC signal the first rectified AC signal is lowered or increased.

In an embodiment, the second voltage range can be the certain upper range if the first voltage range is the certain lower range, and the second voltage range can be the certain lower range if the first voltage range is the certain upper range.

This way the whole range is covered and the certain lower range as well as the certain upper range will be scaled with either the first scaling factor or the second scaling factor. Irrespective of the voltage of the first rectified AC signal, the voltage of the first rectified AC signal can be lowered and/or increased.

In an embodiment, the first scaling factor and the second scaling factor can both be above one, or can both be below one, or the first scaling factor can be above one and the second scaling factor can be below one, or vice versa.

Such a voltage scaling circuit can e.g. be designed to lower the first rectified AC signal irrespective of whether the first $V_{RMS}$ is in the certain lower range or in the certain upper range, wherein if the first $V_{RMS}$ is in the certain upper range the first rectified AC signal can e.g. be lowered more than if the first $V_{RMS}$ is in the certain lower range. In that way, the voltage supplied to the third input, i.e. to the input of the PFC circuit can be made much lower than the received AC signal reducing stress on the PFC circuit. Since AC mains is normally either around 120 $V_{RMS}$ or around 230 $V_{RMS}$ (for a single phase, but the ratio is one or two also for three phase systems) a ratio between the first scaling factor and the second scaling factor of around two will yield a voltage supplied to the third input that is more or less the same irrespective of the AC mains being around 120 $V_{RMS}$ or around 230 $V_{RMS}$.

In an embodiment, the AC-DC converter can comprise a control circuit for controlling the PFC circuit based on the first rectified AC signal of the second input and/or the DC signal of the third output.

The PFC circuit can have one control loop, even two control loops, or even three control loops. One loop can control the shape of the current of the first rectified AC signal, and for that, the voltage of the first rectified AC signal and/or the second rectified AC signal can be the controller input. The other loop can control the voltage of the output DC signal, and for that, the voltage of the output DC signal is a control input. The controller output can be a duty-cycle modulated signal to the power stage.

What is important is that the AC mains voltage and the current drawn by the whole circuit are in phase and have equal profiles, preferably sinus shapes, so that the active power equals or at least is close to the apparent power, the input power of the whole circuit. In other words, the power factor should preferably be as close to 1 as possible.

In an embodiment, the control circuit can control the power factor of the PFC circuit by minimising the phase shift between the voltage and the current of the second rectified AC signal.

Phase shift control and waveform shape control are both obtained by sensing the first rectified AC signal and/or the second rectified AC signal. In a simple PFC circuit, the current waveform is controlled to be an amplitude scaled version of the voltage, and hence both phase and shape can be corrected.

The exact method by which the control is implemented can vary and the skilled person will know how to design and implement the control. The present invention can utilise any PFC control method that would also work if connected directly to the AC mains.

In an embodiment, the first scaling factor of the scaling circuit can be two if the first $V_{RMS}$ is within the certain lower range, or the first scaling factor can be one half if the first $V_{RMS}$ is within the certain upper range.

Since the two dominating AC mains voltages are around 120 $V_{RMS}$ and 230 $V_{RMS}$ it is preferable either that the PFC circuit is dimensioned for a rectified 230 $V_{RMS}$ signal, in which case a voltage around 120 $V_{RMS}$ is multiplied by a factor 2, while a voltage around 230 $V_{RMS}$ is left uninfluenced, or that the PFC circuit is dimensioned for a rectified 120 $V_{RMS}$ signal, in which case a voltage around 230 $V_{RMS}$ is multiplied by a factor ½, while a voltage around 120 $V_{RMS}$ is left uninfluenced.

In an embodiment, the first scaling factor can be two if the first $V_{RMS}$ is within the certain lower range, and the first scaling factor can be 1 otherwise, or the first scaling factor can be one half if the first $V_{RMS}$ is within the certain upper range, and the first scaling factor can be 1 otherwise.

In an embodiment, the AC-DC converter can comprise at least one switch for bypassing the voltage scaling circuit for more than one second or continuously, where the voltage scaling circuit can be configured for being bypassed when the first $V_{RMS}$ is outside the certain lower range or the certain upper range.

If the voltage of the first rectified AC signal is below the certain upper range, the at least one switch bypasses the voltage scaling circuit so that the first rectified AC signal is uninfluenced by the voltage scaling circuit, while if the voltage of the first rectified AC signal is within the certain upper range, the at least one switch does not bypass the voltage scaling circuit so that the first rectified AC signal is influenced by the voltage scaling circuit, by a factor lower than one being applied on the first rectified AC signal.

Alternatively, if the voltage of the first rectified AC signal is above the certain lower range, the at least one switch bypasses the voltage scaling circuit so that the first rectified AC signal is uninfluenced by the voltage scaling circuit, while if the voltage of the first rectified AC signal is within the certain lower range, the at least one switch does not bypass the voltage scaling circuit so that the first rectified AC signal is influenced by the voltage scaling circuit, by a factor above one being applied on the first rectified AC signal.

The AC mains supply can have a constant voltage of e.g. 120 $V_{RMS}$ within a first country. When the AC-DC converter is connected to an electrical socket in the first country, the at least one switch for bypassing the voltage scaling circuit should either continuously bypass the voltage scaling circuit if the first scaling factor of the voltage scaling circuit is ½, or continuously not bypass the voltage scaling circuit if the first scaling factor of the voltage scaling circuit is two.

When the same AC-DC converter is connected to an electrical socket in a second country, where the AC mains supply has a constant voltage of 230 $V_{RMS}$, the at least one switch for bypassing the voltage scaling circuit should either continuously not bypass the voltage scaling circuit if the first scaling factor of the voltage scaling circuit is ½, or continuously bypass the voltage scaling circuit if the first scaling factor of the voltage scaling circuit is two.

This will be a small, simple and cost-effective way of exposing the PFC circuit to a similar signal irrespective of whether the received AC signal on the first input is 120 $V_{RMS}$ or 230 $V_{RMS}$.

In an embodiment, the switched-capacitor circuit can comprise an out-capacitor, Cout, parallel over a second output and connecting a node 1 and a node 2, a first switch, Q1, and a second switch, Q2, in series, parallel with the out-capacitor, wherein the first switch and the second switch are connected in a node 3, wherein the node 3 is connected to the node 1 by the first switch and to the node 2 by the second switch, a fly-capacitor, Cfly, connecting the node 3 to a node 4, a third switch, Q3, connecting the node 2 to the node 4, a fourth switch, Q4, connecting the node 4 to a node 5, an in-capacitor, Cin, parallel over the second input and connecting the node 5 and the node 1, wherein either Q1 and Q3 are conducting simultaneously or Q2 and Q4 are conducting simultaneously.

Design concepts of the art require many switching elements and impose challenges if traditional PFC control schemes would be combined with charge balancing of capacitors. These approaches are not suitable for low power designs, where component count by itself quickly becomes the limiting factor for power density. In contrast, the voltage scaling circuit in the proposed topology uses as few as four switches and three capacitors and operates in open-loop. With as few as four switches and three capacitors the power density can be kept high.

In an embodiment, the switched-capacitor circuit can comprise ten or less switches, preferably eight or less switches, more preferably six or less switches, and most preferably five or less switches.

The aforementioned switches can be integrated in one chip or module. Hence, the size and complexity of the scaling circuit can be reduced. Integration of the switches can also provide a way to optimize the efficiency.

As mentioned above, at low power designs component count by itself quickly becomes the limiting factor for power density. The fewer the number of components the better. Five or less switches will be advantageous.

In an embodiment, the voltage scaling circuit can be a step-down converter following the input voltage.

If the voltage scaling circuit is a step-down converter the first scaling factor of the voltage scaling circuit will be below 1 so that the second rectified AC signal will have a lower voltage than the first rectified AC signal. With a lower voltage supplied to the PFC circuit, the components can be chosen so that they only be exposed to lower voltages. The PFC circuit can be made more cost-effective.

In an embodiment, the voltage scaling circuit can be a step-up converter following the input voltage.

The PFC circuit must store energy during each period of the AC mains frequency to be capable of delivering power to the load, when the rectified input voltage is low. This storage is usually implemented with a bulk storage capacitor. The energy in a capacitor is proportional to the square of its charged voltage. Hence, more energy can be stored at a high capacitor voltage than a low capacitor voltage with the same capacitance.

Due to component limitations, the higher voltage rated capacitors provide less capacitance per volume, so there exists an optimal balance between capacitor voltage rating and capacitance value, which is determined by the component technology.

In general, whether to choose a step-up or step-down scaling is determined by development of component manufacturing technologies. Some components provide lower volume at high voltages and others at low voltages. In designing the AC-DC converter the voltage-volume relation must be considered/weighted for all components to decide between step-up and step-down. In either case, the nearly constant PFC input voltage due to adaptive voltage scaling results in reduction of overall volume with the reduced operating condition variation.

In some applications, the needed output voltage can be higher than the AC mains voltage (for example 600V or 1200V). In these cases, it is beneficial to design the scaling circuit to “help” achieving the system requirements by scaling in the right direction – by stepping up the voltage.

That the voltage scaling circuit can be a step-down converter or a step-up converter means that only one converter is needed that can easily be designed to be a step-down converter or a step-up converter. If the voltage scaling circuit is a switched-capacitor circuit, the voltage scaling circuit can be changed between the step-down converter and the step-up converter by controlling the opening and closing times of the switched-capacitors. The voltage scaling circuit only being one converter makes the whole AC-DC converter a simple, small and cost-effective construction.

In an embodiment, the voltage scaling circuit can be step up/down converter (for example buck-boost converter) which can step down or up the voltage, respectively, depending on the voltage of the AC signal or of the first rectified AC signal.
Since the two dominating AC mains voltages are around 120 $V_{RMS}$ and around 230 $V_{RMS}$ it is preferable that the step-down converter or the step-up converter steps down 230 $V_{RMS}$ by a factor of 2 and leaves 120 $V_{RMS}$ uninfluenced or steps up 120 $V_{RMS}$ by a factor of 2 and leaves 230 $V_{RMS}$ uninfluenced, respectively. The amplitude of the voltage of the first rectified AC signal entering the step-down converter or the step-up converter can control the step-down converter or the step-up converter to step down the voltage or leave the voltage uninfluenced, or step up the voltage or leave the voltage uninfluenced, respectively. A control unit, like e.g. the control circuit for controlling the PFC circuit, can measure the voltage of the AC signal or the first rectified AC signal and control the step-down converter or the step-up converter.

With such a step-down converter or step-up converter, the same AC-DC converter can be used almost anywhere in the world. Since the electrical outlet varies between countries, AC-DC converter only needs to be adapted to have the plugs that fit the electrical outlets of the country, where the AC-DC converter is sold.

In an embodiment, the voltage scaling circuit can be operating in open-loop, i.e. without a feedback, so that the input of the voltage scaling circuit is independent of the output of the voltage scaling circuit.

The proposed AC-DC converter can use the voltage scaling circuit as a simple voltage/current divider/multiplier. The voltage scaling circuit multiplies/divides the second input voltage by e.g. 2 to scale the second input voltage up or down. The voltage scaling circuit does not regulate the output based on a feedback signal that

senses the second output and/or the third output. Since the PFC circuit takes care of the power factor correction, the voltage scaling circuit can be treated as a simple voltage multiplier/divider that enables translation of universal input voltage to the rated input voltage of the following PFC stage. This will make the AC-DC converter a simple, cost-effective and space-effective unit.

In an embodiment, the voltage scaling circuit can be a stand alone voltage scaling circuit and/or the PFC circuit can be a stand alone PFC circuit.

That the voltage scaling circuit can be a stand alone voltage scaling circuit means that the voltage scaling circuit can function independently of the PFC circuit, and that the PFC circuit can be a stand alone PFC circuit means that the PFC can function independently of the voltage scaling circuit. The advantage is that the voltage scaling circuit and the PFC circuit can be controlled independently of each other, which means that the voltage scaling circuit and the PFC circuit are easier to control.

**Description of the Drawings**

The invention will in the following be described in greater detail with reference to the accompanying drawings:

Fig. 1 a schematic view of a AC-DC converter

Fig. 2 a schematic view of an embodiment of a switched-capacitor circuit

Fig. 3 a simplified schematic to analyse the effect of the voltage scaling circuit/SC converter on the overall AC-DC converter power factor, where the SC converter is modelled as a DC transformer

Fig. 4 input and output current and voltage waveforms when the effective capacitance has an intermediate value

Fig. 5 shows the power factor and the current phase as a function of the effective capacitance of the switched-capacitor circuit shown in Fig. 2

Fig. 6 measured input and output current and voltage waveforms without a PFC circuit

Fig. 7 measured input and output current and voltage waveforms for the complete system with a PFC circuit

**Detailed Description of the Invention**

Fig. 1 shows an AC-DC converter 1 comprising a rectifier 3, a voltage scaling circuit 5, a power factor correction (PFC) circuit 7, and a control circuit 9 for controlling the PFC circuit. An AC source 11 provides an AC signal applied over a first input 12 of the AC-DC converter 1. For illustrative reasons a load 13 is connected over the exit of the AC-DC converter 1. The load 13 is provided with the generated DC signal from the AC-DC converter 1.

The AC signal from the AC source 11 is rectified by the rectifier 3 into a first rectified AC signal from a first output 14 of the rectifier 3. The first rectified AC signal is applied over a second input 16 of the voltage scaling circuit 5. The voltage scaling circuit 5 will apply a scaling factor above one to the first rectified AC signal only if the first rectified AC signal has a peak voltage within a certain lower range, or the voltage scaling circuit 5 will apply a scaling factor below one to the first rectified AC signal only if the first rectified AC signal has a peak voltage within a certain upper range.

The first rectified AC signal maybe boosted, reduced or left uninfluenced by the voltage scaling circuit 5 and applied as a second rectified AC signal over a second output 17 connected to a third input 18 of the PFC circuit 7.

However there is a gain to a lower range or an upper range is reduced, the result is that the PFC circuit 7 is exposed to a signal with more or less the same voltage irrespective of the voltage of the AC signal from the AC source 11, since the AC signal is in most cases either around 120 $V_{RMS}$ or around 230 $V_{RMS}$. That the PFC circuit 7 is exposed to a signal with more or less the same voltage means that the PFC circuit 7 can be made much more specific and does not need to be able to handle both 120 $V_{RMS}$ and 230 $V_{RMS}$. The more specific PFC circuit can be made smaller, more efficient, and with a with a better power factor at a lower production cost.

The PFC circuit 7 will apply a DC voltage over the load 13.

The control circuit 9 has a first control circuit input 20 for reading the first rectified AC signal from the first output of the rectifier 3 and/or the second rectified AC signal from the second output of the voltage scaling circuit 5 as well as a second control circuit input 22 for reading the generated constant DC signal from the AC-DC converter 1.

The control circuit 9 also has a control circuit output 24 for controlling the PFC circuit 7 so that the power factor is close to 1 before the conversion to the DC voltage.

**Example**

Fig. 2a shows an example of the voltage scaling circuit as a switched-capacitor circuit 32 with the second input 16 and the second output 17.

The switched-capacitor circuit 32 comprises

an out-capacitor ($C_{out}$) 34 parallel over the second output 17 and connecting a node N1 and a node N2,

a first switch 36,a second switch 38 and the out-capacitor, wherein the first switch and the second switch are connected in a node N3, wherein the node N3 is connected to the node N1 by the first switch 36 and to the node N2 by the second switch 38,

a fly-capacitor ($C_{fly}$) 40 connecting the node N3 to a node N4,

a third switch 42 connecting the node N2 to the node N4,

a fourth switch 44 connecting the node N4 to a node N5, and

an in-capacitor ($C_{in}$) 46 parallel over the second input 16 and connecting the node N5 and the node N1.

In the switched-capacitor circuit 32, either the first switch 36 and the third switch 42 are conducting simultaneously or the second switch 38 and the fourth switch 44 are conducting simultaneously.

Fig. 2b shows an example of the voltage scaling circuit as a buck converter 47 with features, which can be similar or the same as in features of Fig. 2a having the same reference numbers. The buck converter 47 has the second input 16, and the second output 17, wherein the voltage over the second output 17 is lower than the voltage over the second input 16. The buck converter can have a scaling factor with any number below one.

The buck converter 47 comprises

an out-capacitor ($C_{out}$) 34 parallel over the second output 17 and connecting a node N1 and a node N2,

a first inductor 48 connecting the node N2 to a node N6,

a fifth switch 49 connecting the node N6 to the node N1,

a sixth switch 50 connecting the node N6 to a node N5, and
an in-capacitor ($C_{in}$) 46 parallel over the second input 16 and connecting the node N5 and the node N1.

The fifth switch 49 and the sixth switch 50 are closed interchangeably. When the sixth switch 50 is closed (conducting) and the fifth switch 49 is open (non-conducting), the voltage over the second input 16 will drive an increasing current through the first inductor 48 and the out-capacitor ($C_{out}$) 34, increasing the voltage over the second output 17. When the sixth switch 50 is open and the fifth switch 49 is closed, voltage over the second input 16 is removed from the circuit, and the current will decrease, decreasing the voltage over the second output 17.

The skilled person will understand that the buck converter can have different designs.

Fig. 2c shows an example of the voltage scaling circuit as a buck/boost converter 51 with features which can be similar or the same as in features of Figs. 2a and 2b having the same reference numbers. The buck/boost converter 51 has the second input 16 and the second output 17. The buck/boost converter can have a scaling factor with any number below one or above one.

The buck/boost converter 51 comprises
an out-capacitor ($C_{out}$) 34 parallel over the second output 17 and connecting a node N1 and a node N2,
a seventh switch 52 connecting the node N2 to a node N6,
a second inductor 53 connecting the node N6 to the node N1,
a sixth switch 50 connecting the node N6 to a node N5, and
an in-capacitor ($C_{in}$) 46 parallel over the second input 16 and connecting the node N5 and the node N1.

The sixth switch 50 and the seventh switch 52 are closed interchangeably. The skilled person will understand that the buck/boost converter can have different designs.

Fig. 2d shows an example of the voltage scaling circuit as a forward converter 54 with features which can be similar or the same as in features of Figs. 2a, 2b and/or 2c having the same reference numbers. The forward converter 54has the second input 16

and the second output 17. The forward converter 54 can have a scaling factor with any number below one or above one.

The forward converter 54 comprises

an out-capacitor ($C_{out}$) 34 parallel over the second output 17 and connecting a node N1' and a node N2,

a third inductor 55 connecting the node N2 to a node N7,

a first diode 56 connecting the node N7 to the node N1' and allowing current to pass from the node N1' to the node N7,

a second diode 57 connecting the node N7 to a node N8 and allowing current to pass from the node N8 to the node N7,

an in-capacitor ($C_{in}$) 46 parallel over the second input 16 and connecting the node N5 and the node N1'',

a third diode 58 connecting the node N1'' to a node N9 and allowing current to pass from the node N1'' to the node N9,

a demagnetization winding 59 of a transformer 60 connecting the node N9 to the node N5,

a seventh switch 61 connecting the node N1'' to a node N10,

a main primary winding 62 of the transformer 60 connecting the node N10 to the node N5, wherein the demagnetization winding 59 and the main primary winding 62 together make up a primary winding, and

a secondary winding 63 of the transformer 60 connecting the node N8 to the node N1'.

The skilled person will understand that the forward converter can have different designs and how the forward converter works.

**Theoretical Approach**

The proposed topology can use a switched-capacitor (SC) front-end to lower the input voltage of a PFC circuit in the case of high AC line voltage. In the case of low AC line voltage, the SC circuit or SC converter can instead be bypassed using internal switches ($Q_3$ and $Q_4$ in Fig. 2) of the SC converter. The system is illustrated in Fig. 1. Using a 2:1 voltage step-down SC converter, this topology limits the maximum PFC circuit input RMS voltage to be 240V / 2 = 120V. The range of PFC circuit input voltages is therefore greatly reduced compared to the conventional universal single-

stage solution. Furthermore, the PFC circuit output voltage, which is usually 400V for a boost converter PFC, can be halved to 200V and thereby reduce the voltage stress of any following DC-DC converter. Finally, control of the PFC circuit can be simplified due to the reduced input voltage range, and a properly designed frontend SC can in principle be added to any pre-existing PFC circuit without modification.

To analyse the effect of the front-end SC converter on the PFC circuit 7 in Fig. 1, the simplified schematic in Fig. 3 is utilized. The SC converter can be modelled as a DC-DC transformer 70. For this analysis, an ideal converter with 100% efficiency is assumed, i.e. the output resistance is set to zero, and the PFC circuit is assumed to ensure ideal unity power factor. In addition, the PFC circuit is assumed to use the voltage at the second output from the SC converter as the sensing input for PFC control. A total effective capacitance $C$ 71 seen at the output of the SC converter is included in the circuit, and a resistor $R_{pfc}$ 72 models the load of the following PFC circuit. The forward drop of the rectifier diodes is assumed insignificant, but the series rectifier resistance 73 is included, since it is useful for the subsequent mathematical analyses.

In this model, the AC line voltage, $v_{ac}$, drives an AC current, $i_{ac}$. The AC current is rectified by the rectifier 3 so that a rectified current, $i_{rect}$, flows on the other side of the rectifier. Likewise, the AC line voltage, $v_{ac}$, is rectified to $v_{rect}$, which drops over a series rectifier resistance, $R_{rect}$, 73 down to a SC-input voltage, $v_{sc,in}$, applied over the input of the DC-DC transformer 70. Since the DC-DC transformer 70 has been chosen in this case to have the ratio 2:1, a double rectified current, $2i_{rect}$, is driven by a capacitor voltage, $v_c$, which will be half of $v_{sc,in}$ in this case.

For large values of $C$, the circuit operates with narrow current pulses at the line voltage peak similar to the operation of a traditional AC-DC converter using a diode bridge and bulk capacitor. For small values of $C$, the current waveform approaches that of a purely resistive load. An intermediate effective capacitance can cause the circuit to operate with the input and output current and voltage waveforms shown in Fig. 4. During the interval $\phi_1 \rightarrow \phi_2$, the diode bridge can be conducting and the output voltage can be scaled to half the input voltage by the SC converter. During the interval $\phi_2 \rightarrow \pi + \phi_1$, the diodes can be reverse biased and the output voltage can be an exponential decay with

the time constant $\tau = R_{pfc}\, C$. The following analysis considers the boundaries between these two operating modes to determine the angles $\phi_1$ and $\phi_2$.

*A. Conduction Boundaries*

First, the rectifier diodes are assumed to be conducting. The differential equation (1) is constructed to describe the current delivered to the PFC stage. A cosine is used for the AC source, as this simplifies the following derivation.

$$\begin{aligned} \frac{v_c(t)}{R_{pfc}} &= 2\, i_{rect}(t) - C\, \frac{dv_c(t)}{dt} \\ &= 2\, \frac{v_{ac}\, cos(\omega t) - 2\, v_c(t)}{R_{rect}} - C\, \frac{dv_c(t)}{dt} \end{aligned} \qquad (1)$$

This equation is solved using the initial condition $v_c(0) = v_{ac}$, yielding the result in (2).

$$\begin{aligned} v_c(t) &= (v_{ac} - a\, b)\; e^{-a\, t} + a\, b\, cos(\omega t) + b\, \omega\, sin(\omega t) \\ a &= (R_{rect} + 4R_{pfc}) \,/\, (R_{rect}\, R_{pfc}\, C) \\ b &= 2 v_{ac} /\, \left(R_{rect}\, (\omega^2 + a^2)\, C\right) \end{aligned} \qquad (2)$$

Utilizing the reasonable assumptions $R_{rect} << R_{pfc}$ and $R_{rect}\, C << 1$, it follows directly that $\alpha >> 1$. Equation (2) can therefore be simplified to (3).

$$v_c(t) \approx a\, b\, cos(\omega t) + b\, \omega\, sin(\omega t) \qquad (3)$$

When the capacitor voltage of (3) is equal to half the AC voltage, as expressed in (4), the boundary between sinusoidal and exponentially decaying capacitor voltage is found.

$$a\, b\, cos(\phi) + b\, \omega\, sin(\phi) = \frac{v_{ac}}{2} cos(\phi) \qquad (4)$$

From this equation an expression for the angle $\phi_2$ can be obtained, which is given in (5). Note that $\phi_2$ is the solution to (4) plus an additional $\pi/2$, since a cosine was used in (1), while the angle $\phi_2$ is defined referenced to a sine, see Fig. 4.

$$\begin{aligned} \phi_2 &= arctan\left[(v_{ac} - 2\, a\, b)/(2\, b\, \omega)\right] + \pi/2 \\ &\approx arctan\left[(\omega\, R_{pfc}\, C)^{-1}\right] + \pi/2 \end{aligned} \qquad (5)$$

The approximation in (5) is valid for an ideal diode rectifier with zero series resistance 73, i.e. $R_{rect} = 0$.

Following the transition from sinusoidal to decaying voltage waveform after time $\phi_2$, the output voltage is given by (6), in which the time $t$ is referred to the transition point $\phi_2$.

$$v_c(t) = \frac{v_{ac}}{2} sin(\phi_2)\, e^{-t/(R_{pfc}\, C)} \qquad (6)$$

The boundary $\phi_1$ where the rectifier diodes begin to conduct can be found by solving (7).

$$\frac{v_{ac}}{2} sin(\phi_2)\, e^{-t_1/(R_{pfc}\, C)} = -\frac{v_{ac}}{2} sin(\omega t_1 + \phi_2) \qquad (7)$$
$$t_1 = (\phi_1 - \phi_2 + \pi)/\omega$$

Using the small angle approximation $\sin(\phi_1) = \phi_1$, it can be shown that $\phi_1$ is approximated by (8), where $W_0$ is the principal branch of the Lambert $W$ function.

$$\phi_1 \approx W_0\left(\frac{sin(\phi_2)\, e^{(\phi_2 - \pi)/(\omega\, R_{pfc}\, C)}}{\omega\, R_{pfc}\, C}\right) \omega\, R_{pfc}\, C \qquad (8)$$

Note that the expressions (5) and (8) describing $\phi_2$ and $\phi_1$ respectively, are only functions of the effective capacitance seen at the output of the switched-capacitor (SC) converter, the equivalent load resistance of the PFC circuit and the AC mains frequency or line frequency.

*B. Power Factor*

The total system Power Factor (PF) is of course the ratio of active to apparent power as seen from the AC supply, which is given by (9).

$$PF = P_{in,avg}/(v_{ac,rms}\, i_{ac,rms}) \qquad (9)$$

From the schematic in Fig. 3 and the current waveform in Fig. 4, it can be identified that the AC current is described by (10), in which the capacitor voltage

$$v_c(t) = |v_{ac}/2\, sin(\omega t)|$$

for the time interval of non-zero AC current.

$$|i_{ac}(t)| = \frac{1}{2}\left(C\frac{d\, v_c(t)}{dt} + \frac{v_c(t)}{R_{pfc}}\right), \quad \phi_1 + n\pi < \omega t < \phi_2 + n\pi$$
$$i_{ac} = 0 \qquad , \text{ otherwise} \qquad (10)$$

From the symmetry of the positive and negative halves of the periodic current waveform, the instantaneous and RMS value of the AC current can be determined. Assuming the AC voltage to be sinusoidal, it is therefore trivial to calculate the PF in (9) for a given AC voltage, output load and effective capacitance.

*C. Effective Capacitance*

The SC converter's effective output capacitance is a weighted sum of its input, output and flying capacitance. The output capacitance add directly to the effective capacitance, while the input capacitance is scaled by the squared 'turns ratio' of the DC transformer i.e. the ideal SC conversion ratio. The effect of the flying capacitance can in general be dependent on the topology and operation of the SC converter. In this work, a two-phase 2:1 conversion ratio SC as shown in Fig. 2 have been implemented. For this topology, the flying capacitance adds directly to the effective capacitance, and (11) is therefore the expression for calculating the effective capacitance.

$$C = C_{out} + \alpha_{sc} C_{fly} + C_{in}/N^2 = C_{out} + C_{fly} + C_{in}/4 \quad (11)$$

where N is the voltage scaling factor of the SC converter, when the conversion ratio is described in the form N:1. For scaling factor of ½, the ratio is 2:1, and hence N=2

$\alpha_{sc}$ is a topology dependent weight factor used to model how much the flying capacitance adds to the effective capacitance 'seen' at the SC converter output.

**Implementation and Experimental Results**

A high PF SC converter has been designed for nominal EU mains input (50 Hz, 230$V_{rms}$) and 50W output power. The calculated relation between effective capacitance, power factor 78 and current displacement 79 for this specification is shown in Fig. 5. The current displacement is calculated from the first harmonic of the Fourier series decomposition of (10). As expected higher values of effective capacitance causes an increase in current displacement and decrease in PF.

By obtaining greater than 99% PF it is shown that the SC converter can be designed to have negligible effect on PF. From Fig. 5 it is seen that such performance is expected with effective capacitance lower than 1,6 µF. The schematic in Fig. 2 was implemented using the components in Table I. The converter was operated at 270 kHz. An input filter constructed from a 100 µH inductor and 30 nF capacitor was also added, where the input filter was placed before the rectifier with the capacitor in parallel to the rectifier input and the inductor in series with one of the AC input wires.

TABLE I
CRITICAL COMPONENTS USED FOR IMPLEMENTATION OF SWITCHED-CAPACITOR CONVERTER.

| | Manufacturer & Part no. | Description | Amount |
|---|---|---|---|
| $Q_{1\text{-}4}$ | GaN Systems GS-065-004-1-L | GaN, 0.5 Ω | 4 |
| $C_{in}$ | TDK C3216C0G2W153J160AA | 15 nF, C0G | 2 |
| $C_{fly}$ | TDK CKG45NC0G2W943J500JJ | 94 nF, C0G | 6 |
| $C_{out}$ | TDK CGA8P3X7T2E105K250KA | 1 µF, X7T | 1 |

The measured line voltage, $v_{ac}$, 80 and current, $i_{ac}$, 82 as well as the output voltage 84 of the SC converter are shown in Fig. 6. In Fig. 6 measurements are without PFC circuit, i.e. only rectifier, SC converter and load are cascaded. This is directly comparable to the theoretical waveforms in Fig. 4. The current waveform is sinusoidal with small non-conducting intervals around the voltage zero crossing as expected. The performance was quantified using a Newtons4th PPA5530 power analyser at half and full power with the results in Table II. The 50W metrics are marked with circles in Fig. 5, where a circle around an "x" means the measured PF and a circle around "+" means the measured current phase for the 50W metrics. The measured PF and measured current phase show good agreement between calculated and measured performance.

TABLE II
MEASURED PERFORMANCE OF THE SWITCHED-CAPACITOR CONVERTER AT HALF AND FULL OUTPUT POWER.

| | 25 W | 50 W |
|---|---|---|
| PF [%] | 97.3 | 99.1 |
| PF (fundamental) [%] | 97.8 | 99.3 |
| Current displacement [deg] | 12.1 | 6.7 |
| Current THD [%] | 6.9 | 2.8 |
| Efficiency [%] | 96.6 | 97.1 |

To further validate the developed model, $C_{fly}$ was increased using 1 µF X7T capacitors, since C0G capacitors became impractically large, and PF was again measured. The measured PF values and the measured current phase values are shown in Fig. 5 by the "x" and "+" signs, respectively. The results are marked in Fig. 5 with their effective capacitance corrected for capacitance decrease with voltage bias at the transition time $\phi_2$. Even though the calculations assume ideal capacitors, the model and measurements are well correlated.

Finally, the SC converter was combined with a conventional PFC boost converter to verify the complete system functionality. The boost converter was based on a reference design for the Texas Instruments UCC28056 controller and slightly modified to output 210V. Measured current 90, line voltage, $v_{ac}$, 92, and output voltage, $v_{out,sc}$, 94 for the complete system are shown in Fig. 7. In Fig. 7 measurements are with all blocks including PFC circuit, i.e. rectifier, SC converter, PFC (boost converter in this proof-of-concept implementation) and load are cascaded. The system performance at 50W output is quantified in Table III.

TABLE III
MEASURED PERFORMANCE OF THE SWITCHED-CAPACITOR CONVERTER, BOOST CONVERTER AND COMPLETE SYSTEM AT 50 W OUTPUT POWER.

| | SC | Boost | Total |
|---|---|---|---|
| PF [%] | 99.1 | 98.7 | 94.3 |
| PF (fundamental) [%] | 99.3 | 99.5 | 97.4 |
| Current displacement [deg] | 6.7 | 6.0 | 13.2 |
| Current THD [%] | 2.8 | 12 | 10.5 |
| Efficiency [%] | 97.1 | 95.0 | 92.5 |

The current displacement is only slightly affected by the addition of the boost converter as seen from the high fundamental PF. However, the boost contributes with a significant amount of distortion, which lowers the overall PF. Likewise, the boost converter is the bottleneck for system power efficiency. Hence, to improve the overall system performance, the boost converter should be optimized for the lower input and output voltage, but it is not an absolute necessity as is apparent from these results.

**Conclusion**

A switched-capacitor front-end for universal PFC circuits has been presented and analysed. This front-end reduces the voltage stress of the PFC circuit and significantly limits the input voltage range, which allows for better optimization of the PFC circuit. Through circuit analysis, the front-end's effect on system power factor has been modelled. Experimental results for such front-end showed good correlation between calculated and measured performance. The implemented switched capacitor front-end by itself obtained 99,1% power factor at 50W output power and 97,3% power factor at 25W output power. Finally, the switched-capacitor front-end was combined with a low voltage boost converter PFC circuit, which resulted in 94,3% power factor and 92,5% efficiency at full load with 230V RMS input. The implemented prototype shows that the

proposed topology is capable of providing good power factor without any additional control efforts. The full potential of the topology is still to be shown through optimization of the PFC circuit for reduced input voltage range.

## Claims

1. An AC-DC converter comprising
   - a rectifier comprising
     - a first input configured to receive an AC signal, and
     - a first output,

     wherein the rectifier is configured to rectify the AC signal to a first rectified AC signal having a first $V_{RMS}$,
   - a voltage scaling circuit comprising
     - a second input connected to the first output, wherein the second input is configured to receive the first rectified AC signal, and
     - a second output,

     wherein the voltage scaling circuit is configured, if the first $V_{RMS}$ is within a first voltage range, to scale the first rectified AC signal by a first scaling factor generating a second rectified AC signal,
   - a power factor correction (PFC) circuit for keeping the current in phase with and proportional to the voltage of the second rectified AC signal, the PFC circuit comprising
     - a third input connected to the second output, and
     - a third output configured to supply a DC signal on an AC-DC converter-output.

2. The AC-DC converter according to claim 1, wherein the voltage scaling circuit is a switched-capacitor circuit.

3. The AC-DC converter according to any of the preceding claims, wherein the first voltage range is
   - a certain lower range, which preferably is below a first limit, or
   - a certain upper range, which preferably is above the first limit ,

   wherein the first limit is between 140 and 200 $V_{RMS}$, more preferably between 150 and 180 $V_{RMS}$.

4. The AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is configured to scale the first rectified AC signal by a second scaling factor different from the first scaling factor, if the first $V_{RMS}$ is

within a second voltage range different from the first voltage range generating a third rectified AC signal.

5. The AC-DC converter according to claim 4, wherein the second voltage range is the certain upper range if the first voltage range is the certain lower range, and the second voltage range is the certain lower range if the first voltage range is the certain upper range.

6. The AC-DC converter according to claim 4 or 5, wherein the first scaling factor and the second scaling factor
   - are both above one, or
   - are both below one, or

   the first scaling factor is above one and the second scaling factor is below one, or vice versa.

7. The AC-DC converter according to any of the preceding claims, wherein the AC-DC converter comprises a control circuit for controlling the PFC circuit based on the first rectified AC signal of the second input and/or the second rectified AC signal of the second output and/or the DC signal of the third output.

8. The AC-DC converter according to claim 4, wherein the control circuit controls the power factor of the PFC circuit by minimising the phase shift between the voltage and the current of the second rectified AC signal.

9. The AC-DC converter according to any of the preceding claims,
   wherein the first scaling factor is 2 if the first $V_{RMS}$ is within the certain lower range, or
   wherein the first scaling factor is ½ if the first $V_{RMS}$ is within the certain upper range.

10. The AC-DC converter according to any of the preceding claims,
    wherein the first scaling factor is 2 if the first $V_{RMS}$ is within the certain lower range, and the scaling factor is 1 otherwise, or
    wherein the first scaling factor is ½ if the first $V_{RMS}$ is within the certain upper range, and the first scaling factor is 1 otherwise

11. The AC-DC converter according to any of the preceding claims, wherein the AC-DC converter comprises at least one switch for bypassing the voltage scaling circuit for more than one second, wherein the voltage scaling circuit is configured for being bypassed when the first $V_{RMS}$ is outside the certain lower range or the certain upper range.

12. The AC-DC converter according to any of the preceding claims 2-11, wherein the switched-capacitor circuit comprises
    - an out-capacitor, $C_{out}$, parallel over the second output and connecting a node N1 and a node N2,
    - a first switch, $Q_1$, a second switch, $Q_2$, and the out-capacitor, wherein the first switch and the second switch are connected in a node N3, wherein the node N3 is connected to the node N1 by the first switch and to the node N2 by the second switch,
    - a fly-capacitor, $C_{fly}$, connecting the node N3 to a node N4,
    - a third switch, $Q_3$, connecting the node N2 to the node N4,
    - a fourth switch, $Q_4$, connecting the node N4 to a node N5,
    - an in-capacitor, $C_{in}$, parallel over the second input and connecting the node N5 and the node N1,

    wherein either $Q_1$ and $Q_3$ are conducting simultaneously or $Q_2$ and $Q_4$ are conducting simultaneously.

13. The AC-DC converter according to any of the preceding claims 2-12, wherein the switched-capacitor circuit comprises ten or less switches, preferably 8 or less switches, more preferably 6 or less switches, and most preferably 5 or less switches.

14. The high power density AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is
    - a step-down converter, or
    - step-up converter.

15. The high power density AC-DC converter according to any of the preceding claims, wherein the step-up/down converter steps down or up the voltage depending on the voltage of the AC signal or of the first rectified AC signal.

16. The AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is operating in open-loop.

17. The AC-DC converter according to any of the preceding claims, wherein the voltage scaling circuit is a stand-alone voltage scaling circuit and/or the PFC circuit is a stand-alone PFC circuit.

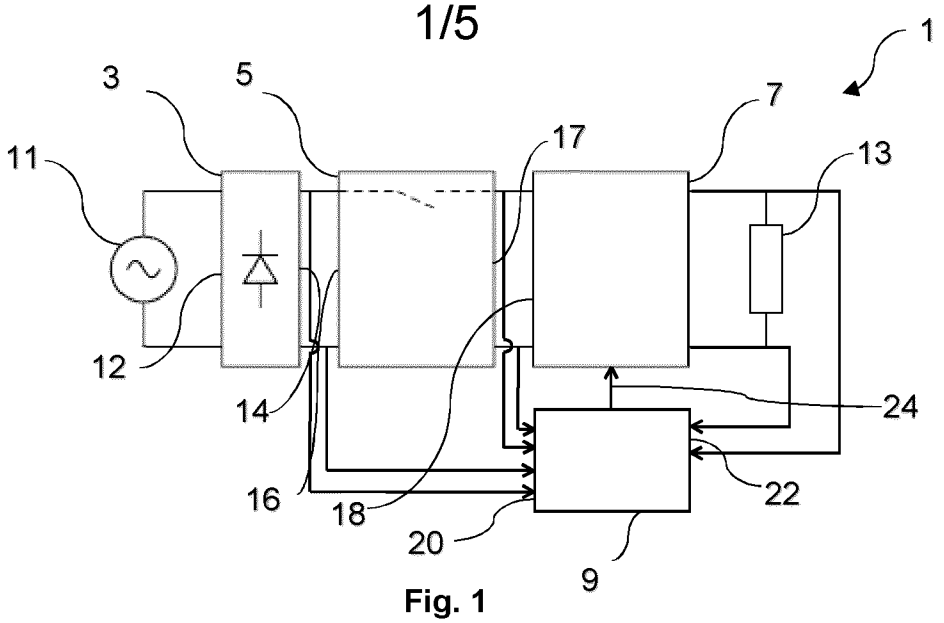

1
3
5
7
11
17
13
12
14
24
16
18
22
20
9

Fig. 1

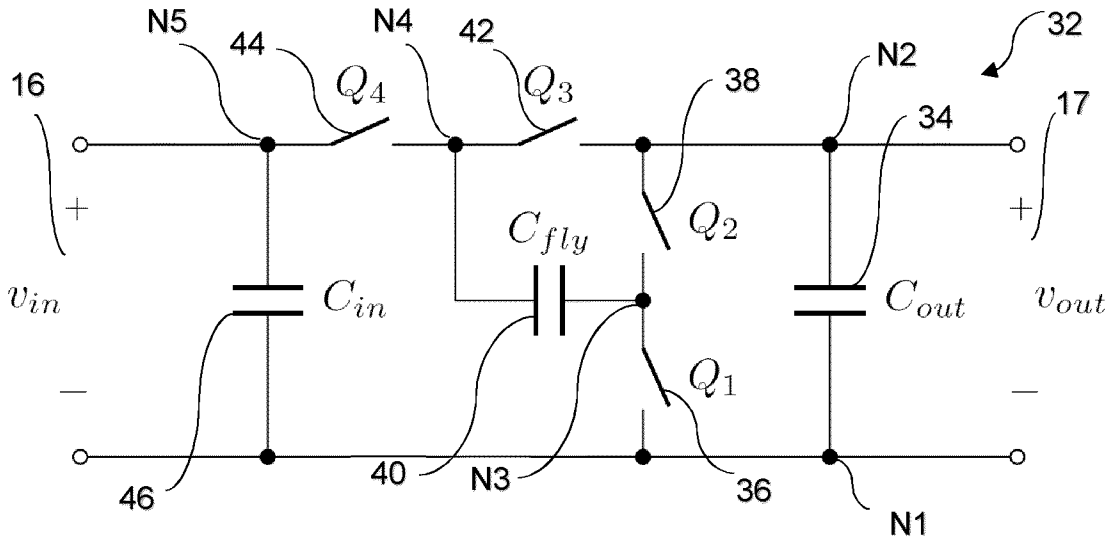

N5
44
N4
42
32
16
$Q_4$
$Q_3$
38
N2
34
17
+
$C_{fly}$
$Q_2$
+
$v_{in}$
$C_{in}$
$C_{out}$
$v_{out}$
$Q_1$
–
–
46
40
N3
36
N1

Fig. 2a

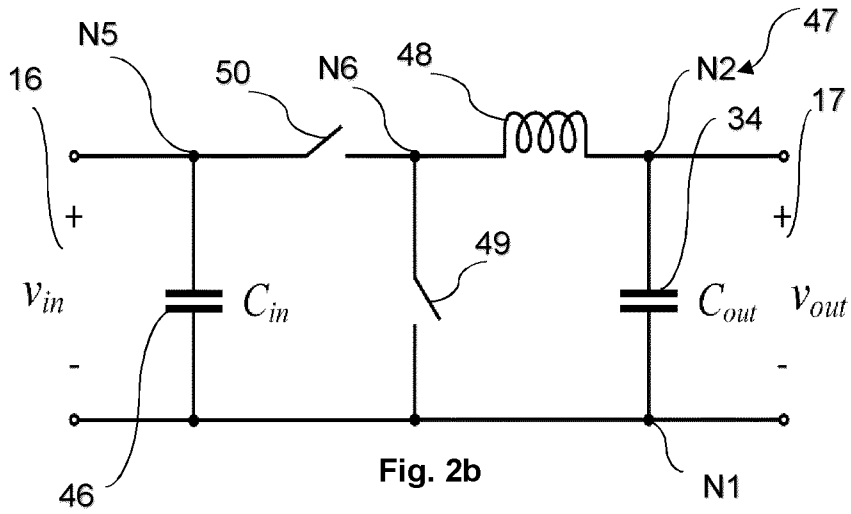



Fig. 2b

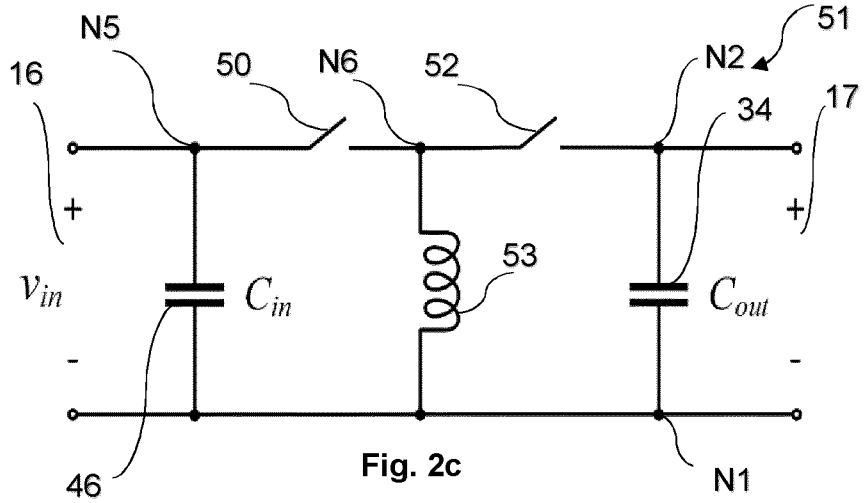



Fig. 2c

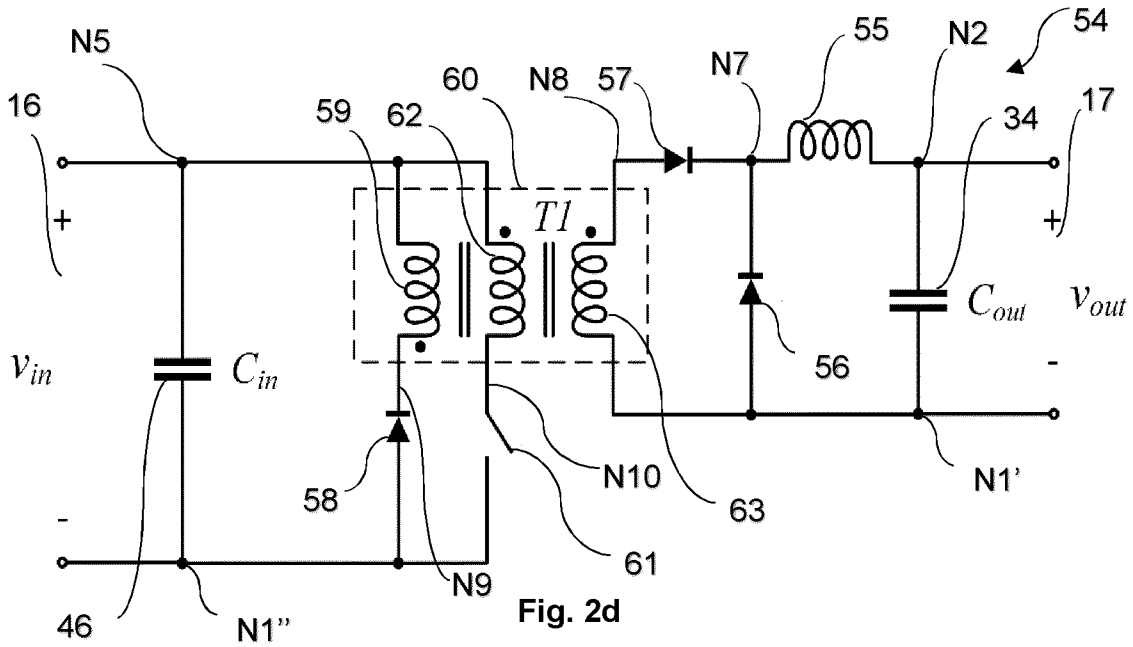



Fig. 2d

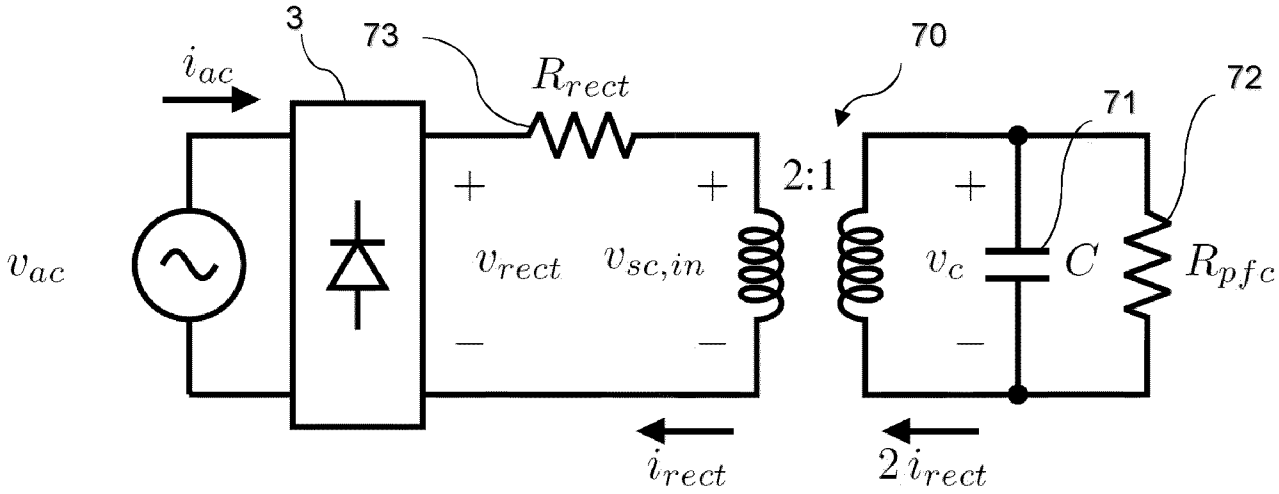
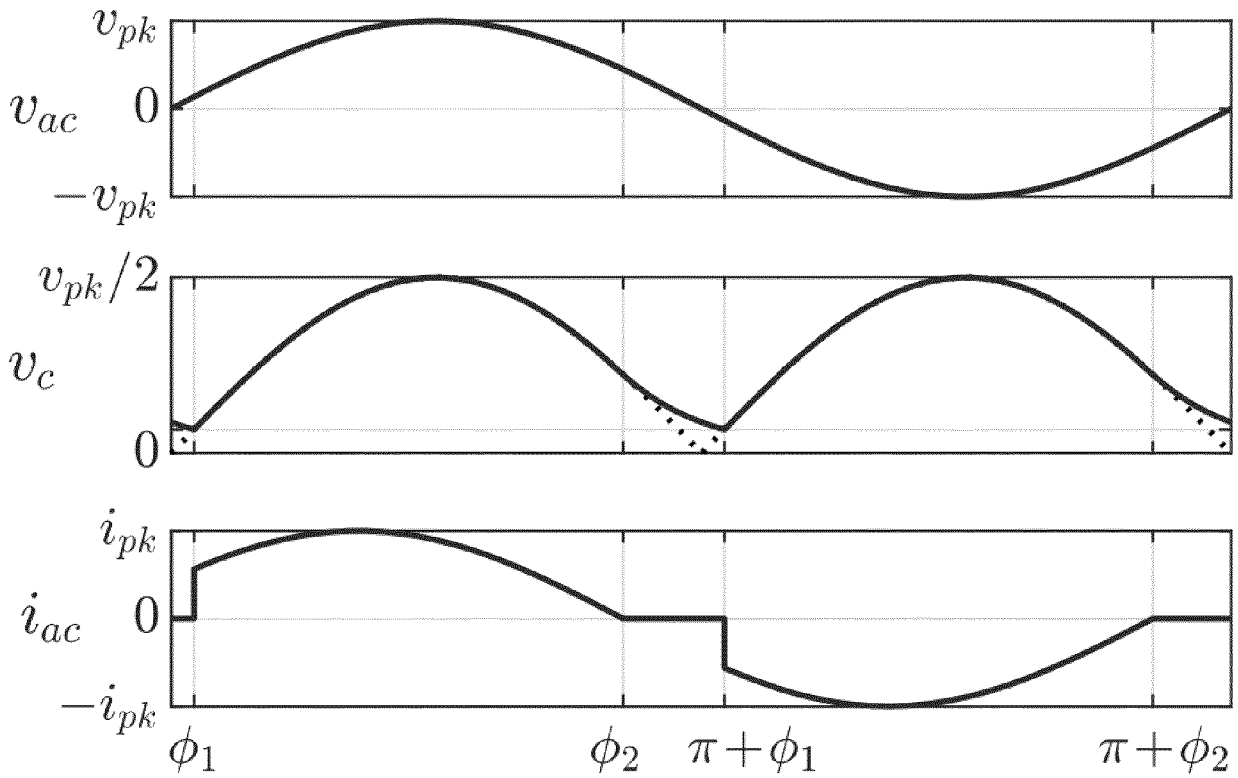

3
73
70
72
71
$i_{ac}$
$R_{rect}$
2:1
$v_{ac}$
$v_{rect}$
$v_{sc,in}$
$v_c$
$C$
$R_{pfc}$
$i_{rect}$
$2\,i_{rect}$

Fig. 3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$v_{ac}$
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$-v_{pk}$
$v_{pk}/2$
$v_c$
0
$i_{pk}$
$i_{ac}$
0
$-i_{pk}$
$\phi_1$
$\phi_2$
$\pi+\phi_1$
$\pi+\phi_2$

Fig. 4

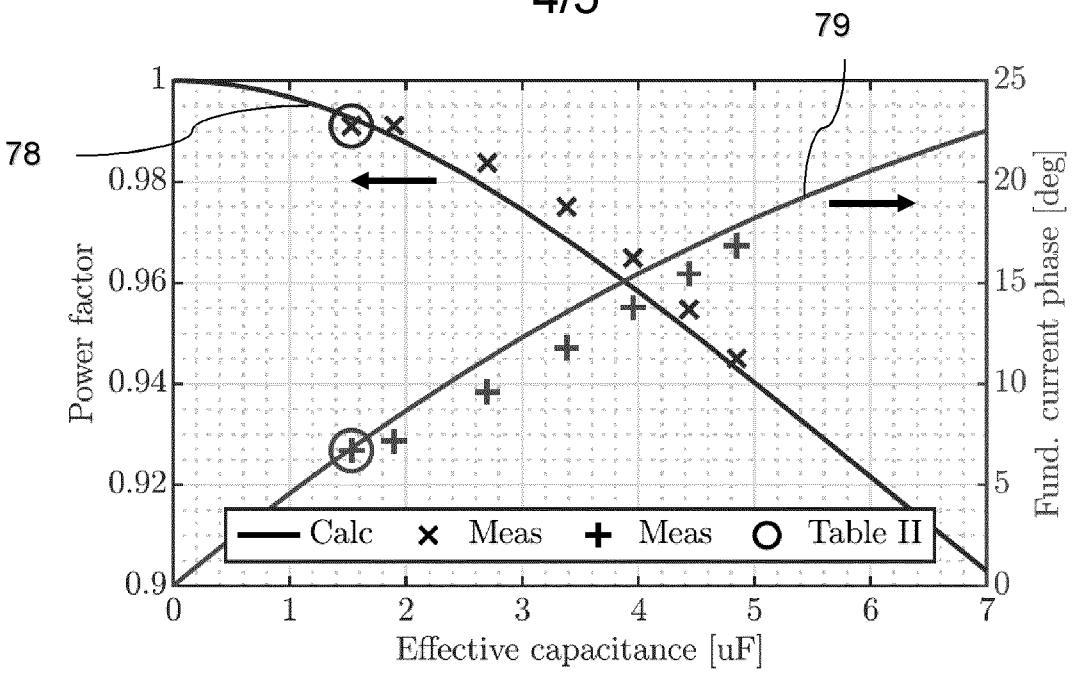
78
79
Power factor
Fund. current phase [deg]
Effective capacitance [uF]
Calc
Meas
Meas
Table II
1
0.98
0.96
0.94
0.92
0.9
25
20
15
10
5
0
0
1
2
3
4
5
6
7

**Fig. 5**

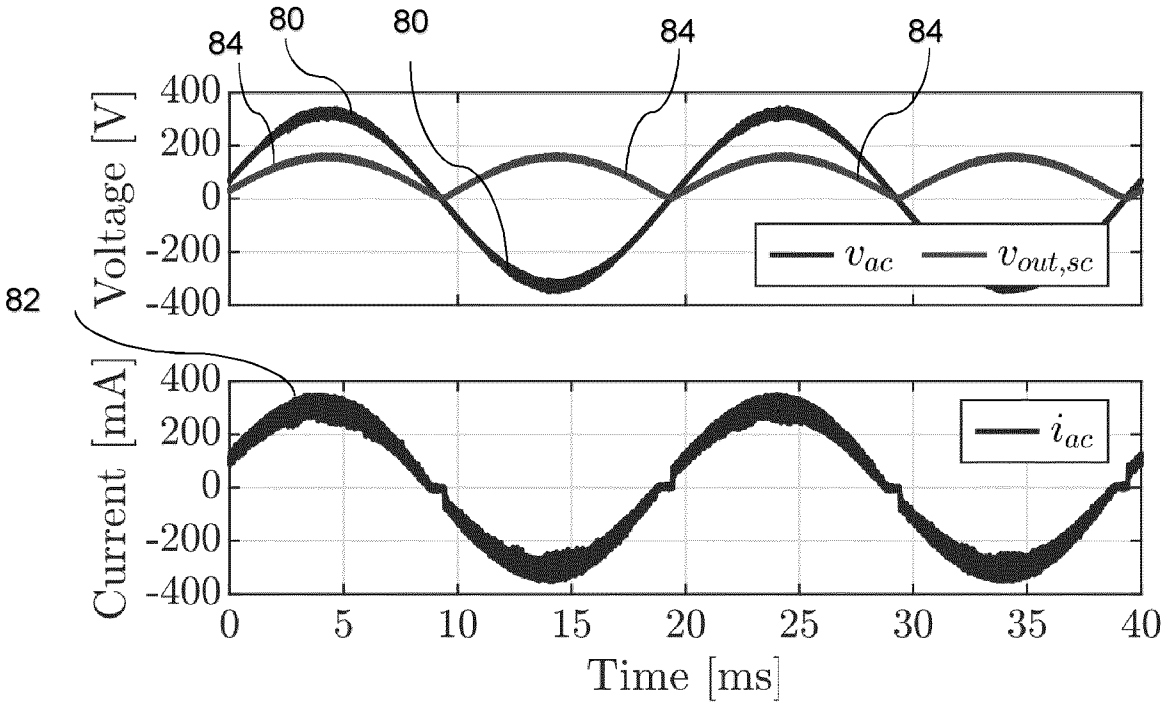
84
80
80
84
84
82
Voltage [V]
400
200
0
-200
-400
$v_{ac}$
$v_{out,sc}$
Current [mA]
400
200
0
-200
-400
$i_{ac}$
0
5
10
15
20
25
30
35
40
Time [ms]

**Fig. 6**

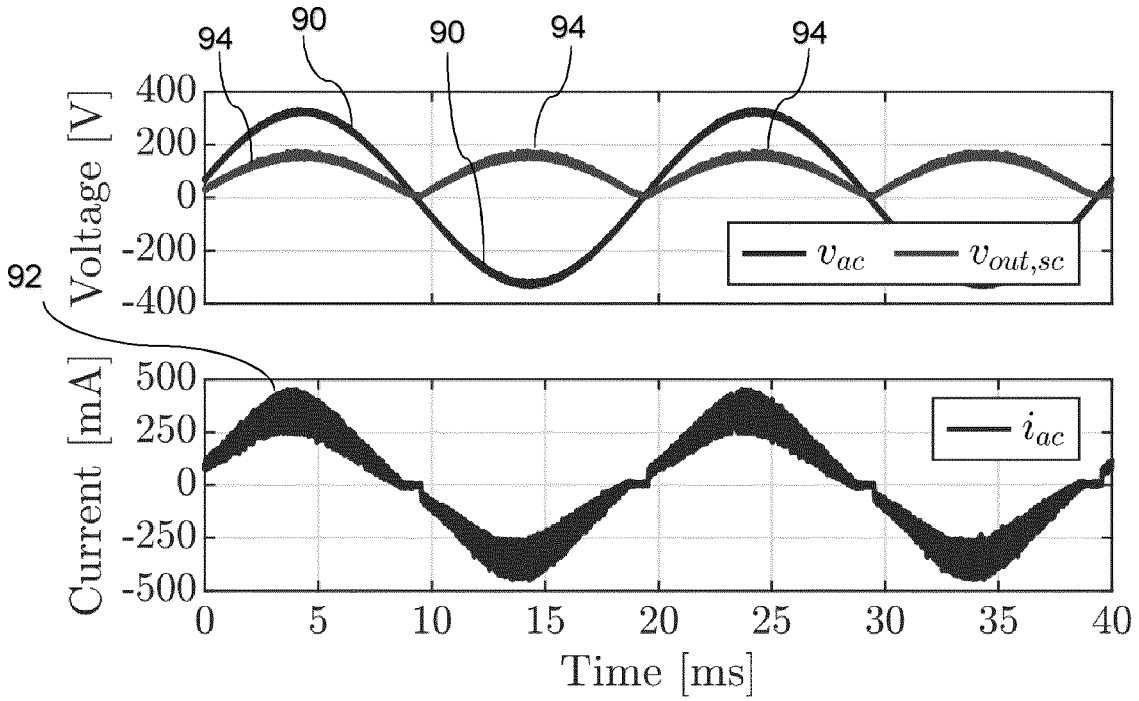
94
90
90
94
94
92
Voltage [V]
400
200
0
-200
-400
$v_{ac}$
$v_{out,sc}$
Current [mA]
500
250
0
-250
-500
$i_{ac}$
0
5
10
15
20
25
30
35
40
Time [ms]

**Fig. 7**

# INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2021/057952

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/42 H02M3/07 H02M7/06 H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2010/289423 A1 (YAO GANG [CN] ET AL) 18 November 2010 (2010-11-18) paragraph [0016] - paragraph [0021]; figures 1-3 | 1-17 |
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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