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Impedance Reshaping for Inherent Harmonics in PMSM Drives With Small DC-Link Capacitor

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***Abstract*—Sharp *LC* resonance peak may enlarge inherent harmonics, dominant harmonics of the supply voltage generated by a three-phase diode rectifier, around the resonance frequency, which will intensify fluctuations of the DC-link voltage and grid currents in motor drives with small DC-link capacitor. In this paper, a novel resonance suppression strategy based on inherent harmonics impedance shaping is proposed specially for three-phase input PMSM drives with small DC-link capacitor. Instead of increasing the damping of the whole system for resonance suppression, the motor side power disturbance can be reduced by designing the impedance for inherent harmonics around *LC* resonance frequency, based on the new model with the consideration of motor side characteristic. For damping current generation, the angle of the virtual admittance is modified to eliminate the influence of the DC-link voltage sampling delay. Experimental results show the effectiveness of the method on a prototype of electrolytic capacitorless PMSM drive.**

***Index Terms*—*LC* resonance, impedance reshaping, low power disturbance, small capacitor.**

I. Introduction

Permanent magnet synchronous motors (PMSMs) have been widely applied in home appliances, transportation and other industrial applications [1]-[2]. Large electrolytic capacitors (e-caps) are commonly used in the DC-link of switch mode inverters to maintain a stable DC-link voltage. However, in this topology, over 30% of inverter failure is attributed to e-caps [3]-[4]. On the other hand, film capacitors are especially suitable for power converters due to the higher reliability and longer lifetime [5]-[6]. The use of film capacitors in DC-link would reduce DC-link capacitance to about 1/50 of the original value which in turn extends the conduction time of the diode rectifier leading to improved total harmonic distortion (THD) of the grid side current. Therefore, this kind of inverter, which is the so-called electrolytic capacitorless motor drive, is especially suitable for the heating, ventilation and air conditioning (HVAC) scenario [7]-[9].

Though electrolytic capacitorless motor drives have many merits such as low cost, high reliability, and better power quality, the control of them is a big challenge. Major issues can be classified into performance of the motor side and suppression of the *LC* resonance. Considering the performance of the motor side, the inverse proportional correlation can be seen between the DC-link voltage utilization rate and the torque ripple constraints in the high-speed region [10]-[12]. With the demand of practical applications, DC-link overvoltage is another problem that needs to be considered in electrolytic capacitorless motor drives [13]-[15]. From the point view of *LC* resonance, it will intensify fluctuations of the DC-link voltage and grid currents, and the system may even become unstable [16]-[21]. The tightly regulated inverter for the motor currents and speed has constant power load (CPL) characteristic, which means the incremental input impedance is negative, and it tends to destabilize the drives. Meanwhile, the *LC* resonance caused by the input line inductor and the DC-link capacitor will stimulate the inherent harmonics around the resonance frequency. Researches have been carried out to damp the resonance of electrolytic capacitorless motor drives, and they can be classified into hardware-based solutions and control-based solutions.

For hardware-based solutions, some passive components were paralleled to the input inductor or the DC-link capacitor to suppress the resonance of CPL systems [22]. A controlled DC-link shunt compensator was designed to shape the grid current according to IEC61000-3-12 [23]. The merits of these hardware solutions are that they can suppress the resonance of CPL systems effectively no matter how the original system behaves. However, the increase of system volume and cost due to additional passive components and power devices are not preferred, in HVAC applications.

Thus, active damping methods are proposed by regulating the load power to change the system characteristics for *LC* resonance suppression. An effective active damping method was proposed in [16], which could control the DC-link voltage even in a rapid load changing condition with the properly designed source state estimator. A large-signal stabilization method was proposed by virtually paralleling a capacitor in the DC-link to suppress the *LC* resonance and increase the motor transient response [13]. A decoupled reference-voltage-based active DC-link stabilization method was utilized in [19] to solve the coupling among the active compensators. In [24], a negative input-resistance compensator was designed to

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stabilize the motor drive with CPL characteristic, in which the DC-link voltage variation was fed into the current loop to modify the system impedance. In [17], a feed-forward compensation voltage was generated to suppress the resonance by carefully considering the period of the *LC* oscillation and the rectifier continuous conduction time with the usage of three-phase inductors. In order to further improve the *LC* resonance suppression effect, the DC-link voltage sampling delay was taken into consideration for compensating voltage generation in [26].

Actually, many kinds of methods are developed as aforementioned above to suppress the *LC* resonance in electrolytic capacitorless motor drives based on the concept of increasing the system damping, which is an effective and universal solution for resonance suppression in power electronics. However, these methods still have potentials to be improved by considering the specific characteristics of the electrolytic capacitorless motor drives with three-phase input. In fact, only the dominant harmonics of the supply voltage generated by a three-phase diode rectifier, which is so-called inherent harmonics in this paper, around the resonance frequency are amplified. Instead of increasing the damping of the whole system to suppress the sharp resonance peak, the motor side power disturbance may be reduced by a careful design of the impedance at amplified inherent harmonics separately, which is the basic concept of the impedance reshaping method.

In this paper, an inherent harmonics suppression method based on impedance reshaping is proposed for electrolytic capacitorless PMSM drives. The system is modelled by accounting for the DC-link voltage delay and the bandwidth of the current loop. Based on the established system model, a novel impedance reshaping method is proposed. By paralleling virtual admittance, the inherent harmonics around the *LC* resonance frequency can be suppressed. The novelty of the proposed method, when compared to the existing solutions, is that it can design the impedance of the inherent harmonics separately, which is beneficial for the reduction of the motor power disturbance. Additionally, the DC-link voltage delay is considered for the design of virtual admittance to improve the accuracy of the damping current generation.

This paper proceeds as follows: the modelling of the drive system is presented in Section II. Section III introduces the proposed impedance reshaping method. The experimental results of the proposed method are presented and discussed in Section IV.

II. MODELLING OF ELECTROLYTIC CAPACITORLESS MOTOR DRIVES

A. Topology of Electrolytic Capacitorless Motor Drives

The topology of the three-phase input electrolytic capacitorless motor drive is shown in Fig. 1， which consists of a three-phase diode rectifier front end, an inductor *L*, a film capacitor *C*, and a three-phase inverter driving a PMSM. The model accounts for the equivalent line resistor with *R*. In HVAC application, the grid side inductor is always equipped for the purposed of improving the power quality of the grid current no matter in traditional drive with electrolytic capacitor or the investigated electrolytic capacitorless drive. It should be noted that, the value of the DC choke can also be reduced in the electrolytic capacitorless motor drive compared with the traditional drive. Normally, the inductance is several mH for drives of several kW [26].

The system faces the stability issue due to the *LC* resonance described with transfer function denoted as [25]

$$G(s)=\frac{u_{\mathrm{dc}}}{u_{\mathrm{rect}}}=\frac{u_{\mathrm{dc0}}^2}{u_{\mathrm{dc0}}^2LCs^2+\left(u_{\mathrm{dc0}}^2RC-P_{\mathrm{L}}L\right)s+u_{\mathrm{dc0}}^2-P_{\mathrm{L}}R} \quad (1)$$

where u_{dc} is the DC-link voltage, u_{rect} is the rectified voltage, u_{dc0} is the mean value of the DC-link voltage, and P_{L} is the load power.

The DC-link voltage and the input current are shown in Fig. 2 where there is no DC-link capacitor during the steady state load condition, and also compared with the case with DC-link capacitor of hundreds of μF and infinite value in the same figure. The load current is directly affected to the DC-link current (i_{g}) in this case. It is also fluctuating according to the DC-link voltage since the output power is constant. Along with the increase of DC-link capacitance, the conduction time of the DC-link current will be reduced. Under the extreme condition, the DC-link current shows a pulse wave. So, the DC-link capacitance should be as low as possible to achieve a better shape of the grid current.

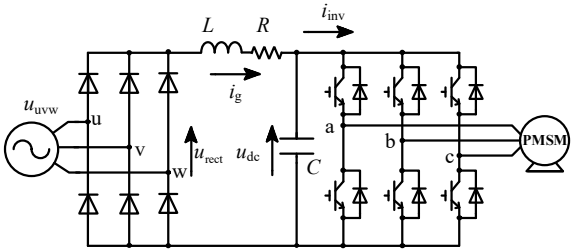


Fig. 1. Three-phase input diode rectifier PMSM drives with slim DC-link capacitor.

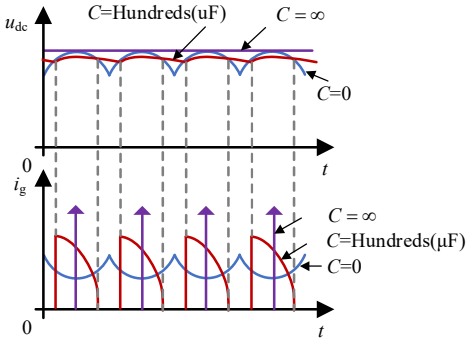


Fig. 2. DC-link voltage and input current with different capacitances.

The rectified voltage contains harmonics at six times the grid side frequency, which can be expressed as

$$u_{\mathrm{rect}}=u_{\mathrm{dN}}\left[1-\sum_{n=1}^{\infty}\frac{2}{(6n)^2-1}\cos\left(6\omega_{\mathrm{g}}nt\right)\right] \quad (2)$$

where n=1,2,3…, $u_{\mathrm{dN}}=3\sqrt{3}u_{\mathrm{peak}}/\pi$, u_{peak} is the peak value of the phase voltage, u_{rect} is the rectified voltage, and ω_{g} is the grid side frequency,

Fig. 3 shows the simulation results of the DC-link voltage u_{dc} responses when L=2.5 mH, and C=30 μF. The resonance frequency is 580 Hz as shown in Fig. 3(b), thus the inherent

harmonics at the frequency of $6\omega_g$ (300 Hz) and $12\omega_g$ (600 Hz) in u_{dc} as shown in Fig. 3(c) are amplified compared with those in u_{rect} as shown in Fig. 3 (a). Thus, it is important to reshape the impedance at these two frequencies.

B. Modelling Considering Motor Side Characteristics

The equivalent models of the drive are shown in Fig. 4. Normally, the motor side is treated as CPL as shown in Fig. 3(a) for easier understanding of the system [16]. However, the DC-link voltage sampling delay has great impact on damping performance as discussed in [26]. In this paper, the DC-link voltage sampling delay and the bandwidth of the current loop are considered in modelling for improving the harmonic suppression effect as shown in Fig. 4(b).

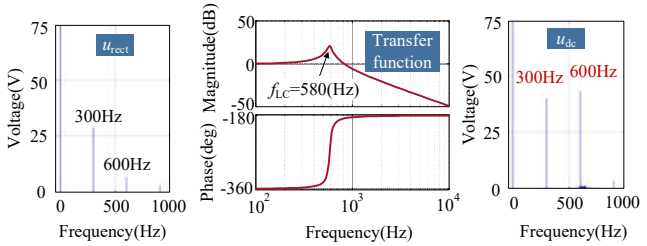


Fig. 3. Simulation of DC-link voltage response. (a) Inherent harmonics of u_{rect} at the frequencies of $6\omega_g$ and $12\omega_g$. (b) Bode diagram of system transfer function. (c) Inherent harmonics of u_{dc} at the frequencies of $6\omega_g$ and $12\omega_g$.

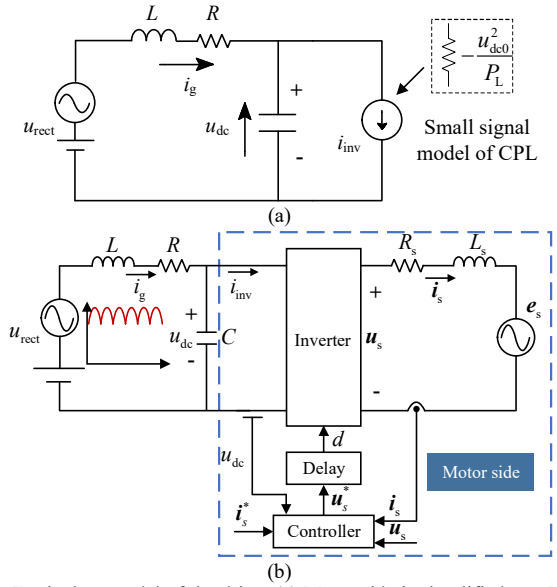


Fig. 4. Equivalent model of the drive. (a) Motor side is simplified as CPL. (b) Considering motor side characteristics.

Fig. 5 shows the typical time sequence of sampling, calculation and PWM output [27]. Control algorithms take a logical sequential step that yields the PWM signals after the execution. For the n^{th} sampling point, the DC-link voltage is obtained at the peak of the carrier. The control algorithm is executed between the nth and the $(n+1)^{th}$ sampling points, then the sampled DC-link voltage (u_{dc_s}) is kept as a constant at the beginning of the $(n+1)^{th}$ sampling point. When applying the typical time sequence, the PWM output is inherently delayed by $0.5T_s$. Therefore, the total DC-link voltage delay, which is the sum of calculation delay and PWM delay is $1.5T_s$, as shown in Fig. 5 where the corresponding voltage is represented as the equivalent sampled DC-link voltage (u_{dc_e}). Due to the large peak-to-peak DC-link voltage ripple, the voltage error caused by sampling can reach 9% [26].

Considering the DC-link voltage delay, the motor voltages can be expressed as [17]

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \frac{u_{dc}}{u_{dc\_e}} \begin{bmatrix} u_{dref} \\ u_{qref} \end{bmatrix} \tag{3}$$

where $u_{d,q}$ are the motor voltages at dq-axes, and $u_{d,qref}$ are the reference of the motor voltages at dq-axes.

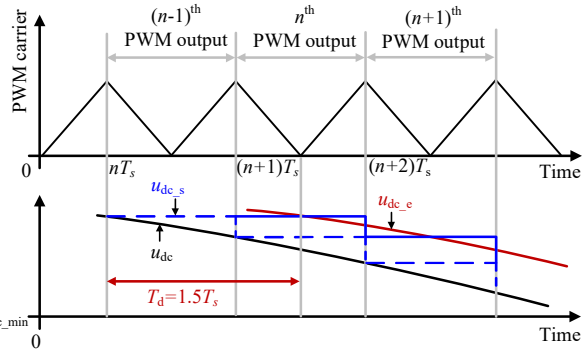


Fig. 5. Time sequence of sampling, calculation and PWM output.

Thus, the small-signal model of motor voltages can be derived as

$$\begin{bmatrix} \Delta u_d \\ \Delta u_q \end{bmatrix} = \frac{u_{dc0}}{u_{dc\_e0}} \begin{bmatrix} \Delta u_{dref} \\ \Delta u_{qref} \end{bmatrix} + \frac{\Delta u_{dc}}{u_{dc\_e0}} \begin{bmatrix} u_{dref0} \\ u_{qref0} \end{bmatrix} - \frac{u_{dc0}\Delta u_{dc\_e}}{u_{dc\_e0}^2} \begin{bmatrix} u_{dref0} \\ u_{qref0} \end{bmatrix} \tag{4}$$

where $\Delta u_{d,q}$ are the increments of the motor voltages, Δu_{dc} is the increment of the DC-link voltage, Δu_{dc_e} is the increment of the equivalent sampling DC-link voltage, u_{dc_e0} is the mean value of the equivalent sampling DC-link voltage, and $u_{d,qref0}$ are the mean values of the motor voltage references.

Neglecting the losses of the inverter, the power relationship between the grid side and the motor side can be denoted as

$$u_{dc} i_{inv} = \frac{3}{2}\left(u_d i_d + u_q i_q\right) \tag{5}$$

where $i_{d,q}$ are the motor currents at dq-axes, and i_{inv} is the inverter input current.

The small-signal model of (5) can be derived as

$$\Delta u_{dc} i_{inv0} + u_{dc0}\Delta i_{inv} = \frac{3}{2}\left(\Delta u_d i_{d0} + u_{d0}\Delta i_d + \Delta u_q i_{q0} + u_{q0}\Delta i_q\right) \tag{6}$$

where Δi_{dq} are the increments of the motor currents, Δi_{inv} is the increment of the inverter input current, i_{dq0} are the mean values of the motor currents, i_{inv0} is the mean value of the inverter input current, and $u_{d,q0}$ are the mean values of the motor voltages.

According to (6), the admittance of the motor side can be obtained as

$$Y_m = -\frac{i_{inv0}}{u_{dc0}} + \frac{3}{2}\left(\frac{u_d(s)}{u_{dc}(s)}\frac{i_{d0}}{u_{dc0}} + \frac{u_{d0}}{u_{dc0}}\frac{i_d(s)}{u_{dc}(s)} + \frac{u_q(s)}{u_{dc}(s)}\frac{i_{q0}}{u_{dc0}} + \frac{u_{q0}}{u_{dc0}}\frac{i_q(s)}{u_{dc}(s)}\right) \tag{7}$$

The relationship between the motor side and the DC side is described in the Appendix. Substituting (A7) and (A8) into (7), the admittance of the motor side can be finally expressed as (8).

$$Y_{\mathrm{m}}=-\frac{i_{\mathrm{inv0}}}{u_{\mathrm{dc0}}}+\frac{3}{2}\left(\begin{array}{l}\left[\left(R_{\mathrm{s}}+L_{\mathrm{d}}s\right)\dfrac{u_{\mathrm{dref0}}}{R_{\mathrm{s}}+L_{\mathrm{d}}s+G_{\mathrm{d}}}-\omega_{\mathrm{e}}L_{\mathrm{q}}\dfrac{u_{\mathrm{qref0}}}{R_{\mathrm{s}}+L_{\mathrm{q}}s+G_{\mathrm{q}}}\right]\dfrac{1-e^{-1.5T_{\mathrm{s}}s}}{u_{\mathrm{dc\_e0}}}\dfrac{i_{\mathrm{d0}}}{u_{\mathrm{dc0}}}+\dfrac{u_{\mathrm{dref0}}}{R_{\mathrm{s}}+L_{\mathrm{d}}s+G_{\mathrm{d}}}\dfrac{1-e^{-1.5T_{\mathrm{s}}s}}{u_{\mathrm{dc\_e0}}}\dfrac{u_{\mathrm{d0}}}{u_{\mathrm{dc0}}}\\+\left[\omega_{\mathrm{e}}L_{\mathrm{d}}\dfrac{u_{\mathrm{dref0}}}{R_{\mathrm{s}}+L_{\mathrm{d}}s+G_{\mathrm{d}}}+\left(R_{\mathrm{s}}+L_{\mathrm{q}}s\right)\dfrac{u_{\mathrm{qref0}}}{R_{\mathrm{s}}+L_{\mathrm{q}}s+G_{\mathrm{q}}}\right]\dfrac{1-e^{-1.5T_{\mathrm{s}}s}}{u_{\mathrm{dc\_e0}}}\dfrac{i_{\mathrm{q0}}}{u_{\mathrm{dc0}}}+\dfrac{u_{\mathrm{qref0}}}{R_{\mathrm{s}}+L_{\mathrm{q}}s+G_{\mathrm{q}}}\dfrac{1-e^{-1.5T_{\mathrm{s}}s}}{u_{\mathrm{dc\_e0}}}\dfrac{u_{\mathrm{q0}}}{u_{\mathrm{dc0}}}\end{array}\right). \tag{8}$$

The influence of the DC-link voltage delay T_{d} is illustrated in Fig.6 (a), where the current loop bandwidth ω_{cb} is set as 300 Hz. The motor side shows CPL characteristic when T_{d}=0s since the phase of Y_{m} maintains 180°. However, along with the increase of T_{d}, the phase of Y_{m} diverges from 180°.

The influence of the current loop bandwidth is shown in Fig. 6(b), where T_{d} is set as $1.5T_{\mathrm{s}}$. The motor side gets closer to CPL characteristic with the increase of ω_{cb}. As a result, the motor side does not match the CPL characteristic exactly.

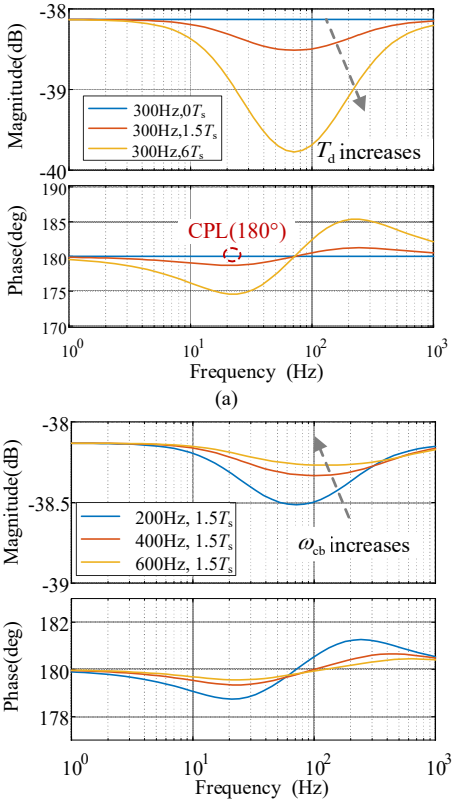


Fig. 6. Bode diagram of Y_{m}. (a) Influence of the DC-link voltage delay. (b) Influence of the current loop bandwidth.

The system transfer function can be obtained by applying Y_{m}, and denoted as

$$G(s)=\frac{1}{\left(Ls+R\right)\left(Cs+Y_{\mathrm{m}}\right)+1}. \tag{9}$$

The proposed impedance reshaping method is designed based on this model on the purpose of achieving better control performance.

III. Proposed Impedance Reshaping Method

A Theory of the Proposed Approach

Paralleling a virtual resistor [16], [28] or capacitor [13], [29] can increase the system damping, and some paralleling examples are shown in Fig. 7(a). Generally, the damping current is generated from the DC-link voltage without the requirement of additional sensors. The corresponding control block diagram is shown in Fig. 7(b), and the damping current can be denoted as

$$i_{\mathrm{damp}}=\begin{cases}\dfrac{1}{R_{\mathrm{damp}}}u_{\mathrm{dc}}, & \text{paralleling } R_{\mathrm{damp}}\\ C_{\mathrm{damp}}\dfrac{du_{\mathrm{dc}}}{dt}, & \text{paralleling } C_{\mathrm{damp}}\end{cases} \tag{10}$$

where i_{damp} is the damping current, R_{damp} is the damping resistor, and C_{damp} is the damping capacitor.

Different from increasing the system damping by paralleling virtual resistor or capacitor for resonance suppression as shown in Fig. 8, the proposed method tries to reshape the impedance of inherent harmonics around resonance frequency and the equivalent model is shown in Fig. 8(a). The system transfer function at inherent harmonic frequencies can be derived as

$$G_{\mathrm{damp\_n}}(s)=\frac{u_{\mathrm{dc\_n}}}{u_{\mathrm{rect\_n}}}=\frac{1}{\left(Ls+R\right)\left(Cs+Y_{\mathrm{m}}+Y_{\mathrm{d\_n}}\right)+1} \tag{11}$$

where $Y_{\mathrm{d\_n}}$ is the virtual admittance at the inherent harmonic frequency, $u_{\mathrm{dc\_n}}$ is the inherent DC-link voltage harmonic, and $u_{\mathrm{rect\_n}}$ is the inherent rectified voltage harmonic.

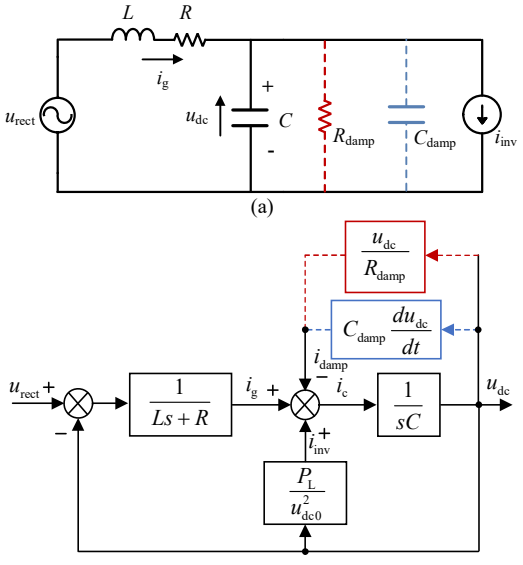


Fig. 7. Scheme of active damping control. (a) Equivalent model. (b) Control block diagram.

Also, the damping current can be expressed as

$$i_{\mathrm{damp\_n}}=u_{\mathrm{dc\_n}}Y_{\mathrm{d\_n}}. \tag{12}$$

The admittance can be expressed as

$$Y_{\mathrm{d\_n}}=\left|Y_{\mathrm{d\_n}}\right|\cos\theta_{\mathrm{d\_n}}+j\left|Y_{\mathrm{d\_n}}\right|\sin\theta_{\mathrm{d\_n}} \tag{13}$$

where $|Y_{d\_n}|$ and θ_{d_n} are the magnitude and angle of the virtual admittance, respectively.

Fig. 8(b) shows the block diagram of the proposed control. Firstly, the inherent harmonics in the DC-link voltage are extracted. Then, the paralleled impedance is carefully designed for each inherent harmonic. Actually, the design of the impedance is a key point in the proposed method, which will be discussed in part B.

The expanded control diagram is presented in Fig. 9, where the impedance reshaping strategy is integrated based on the rotor position sensorless control of PMSM [30]. Bandpass filters are used to extract the inherent harmonics of the DC-link voltage. Then, the virtual admittance Y_{d_n} is designed to suppress the inherent harmonics around LC resonance frequency according to Fig. 10 and Fig. 11. The damping voltages in the motor side are generated, as described in [16], and applied in the control scheme to realize the system impedance reshaping.

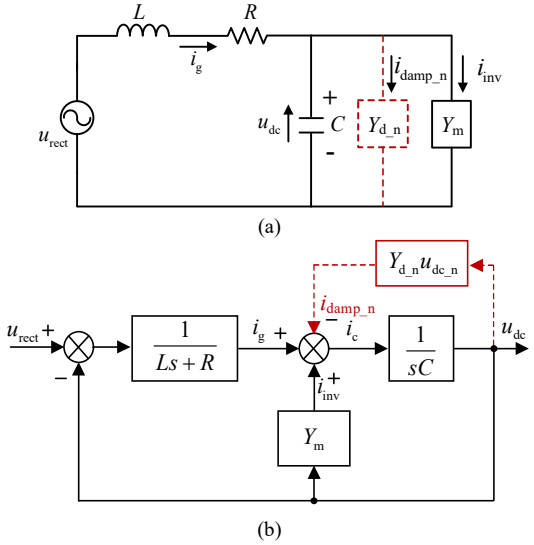


Fig. 8. Proposed impedance reshaping strategy. (a) Equivalent model. (b) Control block diagram.

B Theoretical Analysis of Virtual Admittance Design

The damping power is the product of damping current and DC-link voltage [18]. The conclusion can be derived by omitting the product of higher order terms, that lower damping current and inherent DC-link voltage harmonics means lower damping power generated in the motor side. As indicated in (12), the primary task is to design small Y_{d_n} as possible with effective DC-link voltage harmonic suppression. In order to analyze the virtual impedance for each inherent harmonic, the virtual admittance can be rewritten as

$$Y_{d\_n}=|Y_{d\_n}|\cos\theta_{d\_n}+\frac{|Y_{d\_n}|}{\omega_{d\_n}}\sin\theta_{d\_n}s \tag{14}$$

where ω_{d_n} is the frequency of the inherent harmonic.

Substituting (14) into (11), the system transfer function can be expressed as

$$G_{damp\_n}(s)=\frac{1}{(Ls+R)\left(\begin{array}{l}Cs+Y_{m\_n}+|Y_{d\_n}|\cos\theta_{d\_n}\\+\dfrac{|Y_{d\_n}|}{\omega_{d\_n}}\sin\theta_{d\_n}s\end{array}\right)+1}. \tag{15}$$

Considering the experimental platform, LC resonance frequency is 580 Hz. So, impedances at the frequencies of $6\omega_g$ and $12\omega_g$ need to be designed, since they are amplified by the LC resonance. Fig. 10 shows the magnitude of the Bode diagram at the frequency of $6\omega_g$ by applying different Y_{d_1} based on the proposed model. Lower $|G_{damp\_1}|$ and $|Y_{d\_1}|$ mean better harmonic suppression ability and less damping power generated in the motor, respectively. The surface is the results of paralleling virtual admittance with different magnitudes and angles. As can be seen, $|G_{damp\_1}|$ is relatively small when θ_{d_1} is set as -1.6 rad. Considering the harmonic suppression level and damping power, $|Y_{d\_1}|$ is chosen as 0.04. The dotted line plane is the result by paralleling virtual resistor with the value of 25 Ω as shown in Fig. 7(a). As can be seen, with the same magnitude of admittance, the proposed method can reduce $|G_{damp\_1}|$ to 0.63 dB, while the method in Fig. 7(a) just reduces $|G_{damp\_1}|$ to 2.55 dB. That means using the proposed method, the damping power at $6\omega_g$ can be reduced to 83.3% while the harmonic suppression level can be improved to 120%, theoretically.

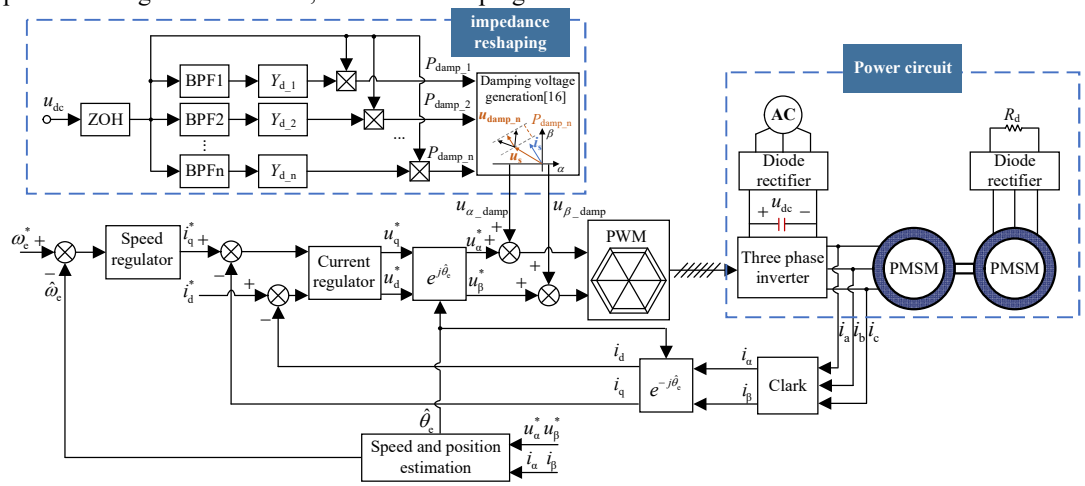


Fig. 9. Electrolytic capacitorless PMSM drive with impedance reshaping.

Similarly, Fig. 11 shows the results at the frequency of $12\omega_g$. Based on the same principle, $|Y_{d\_2}|$ and θ_{d_2} are chosen as 0.03 and -3.4 rad, respectively. The amplitude of the Bode diagram at the frequency of $12\omega_g$ can be reduced to 8.2 dB. The dotted line plane is the result by paralleling virtual resistor with the value of 33 Ω and $|G_{damp\_2}|$ can be suppressed to 13.8 dB.

The theoretical angles of the virtual admittances can be obtained through Fig. 10 and Fig. 11. However, it should be noted that the DC-link voltage delay needs to be considered when generating the damping current. As shown in (12), the DC-link voltage delay will cause the angle of virtual admittance to diverge from the theoretical value. Fig. 12(a) shows the angle of the virtual admittance considering the DC-link voltage delay. u_{dc_1} is the DC-link voltage component at the frequency of $6\omega_g$. u_{dc_e1} is the corresponding equivalent sampling value, which has a phase lag of φ_{e_1}. Consequently, the final value of the virtual admittance angle is obtained by subtracting the phase lag from the theoretical value of θ_{d_1} for precise impedance reshaping. The time delay between the DC-link voltage u_{dc} and the equivalent sampled DC-link voltage u_{dc_e} is $1.5T_d$. The phase delay between u_{dc_1} and u_{dc_e1} can be calculated using the following equation

$$\varphi_{e\_1} = \frac{6\omega_g}{f_s}. \tag{16}$$

Then the damping current can be expressed as

$$i_{damp\_n} = u_{dc\_en}\left|Y_{d\_n}\right|\angle\left(\theta_{d\_n}\text{-}\varphi_{e\_n}\right). \tag{17}$$

Fig. 12(b) and (c) shows the divergence of the magnitude of the system transfer function caused by the DC-link voltage delay. As can be seen, the DC-link voltage delay increases both $|G_{damp\_1}(s)|$ and $|G_{damp\_2}(s)|$, which will weaken the harmonic suppression ability of the method.

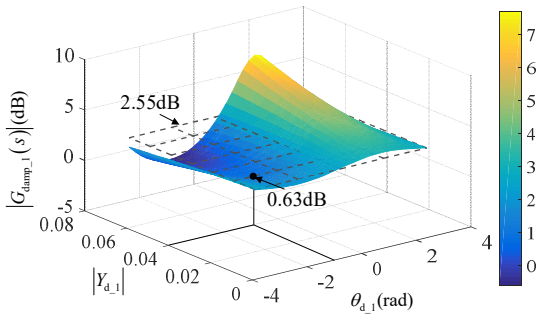


Fig. 10. Magnitude of the Bode diagram at the frequency of $6\omega_g$ with different virtual admittances.

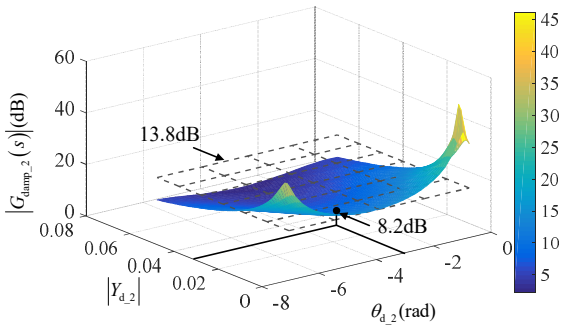


Fig. 11. Magnitude of the Bode diagram at the frequency of $12\omega_g$ with different virtual admittances.

The harmonics can be suppressed by connecting the damping term in parallel on the inverter side as shown in Fig. 8(a). This method needs to control the inverter input current of the drive system, but it contains harmonic components at the switching frequency, and the relationship between the direct-axis and quadrature-axis currents of the motor is complex. So, it is difficult to achieve effective control. Therefore, the damping term can be equivalent to the output power of the inverter. In this way, the equivalent damping power can be realized through the motor voltage instruction signal as shown in Fig. 13.

The damping voltage vector $\boldsymbol{u}_{\mathbf{damp\_n}}$ which produces the damping current i_{damp_n} can be directly calculated from the following equation since the output power of the inverter is equal to the inner production of the inverter voltage vector and the motor current vector

$$i_{damp\_n} = \frac{3}{2}\frac{\boldsymbol{u}_{\mathbf{damp\_n}}\cdot\boldsymbol{i}_s}{u_{dc}}. \tag{18}$$

There are infinite solutions of damping vector in (18) because the equation is not a scalar equation but a 2-D vector equation. The solutions lie on the line which is vertical to the current vector as shown in Fig. 14(a). The best solution is the vector with minimum amplitude because the damping voltage is to be added to the current controller [16]. Thus, the damping voltage vector on the axis where the motor current vector lies becomes the optimal solution.

So, the amplitude of damping voltage in the direction of motor current vector can be derived as the following equation

$$\left|\boldsymbol{u}_{\mathbf{damp\_n}}\right| = \frac{2}{3}\frac{u_{dc}i_{damp\_n}}{\left|\boldsymbol{i}_s\right|}. \tag{19}$$

In this study, θ_{d_1} is set as -1.6 rad, and the amplitude of damping voltage is the yellow solid sine wave as shown in Fig. 14(b). If θ_{d_1} deviates from -1.6 rad, the amplitude of damping voltage can be show as the yellow dash sine wave, which has larger peak to peak value and will cause more power disturbance in the motor side.

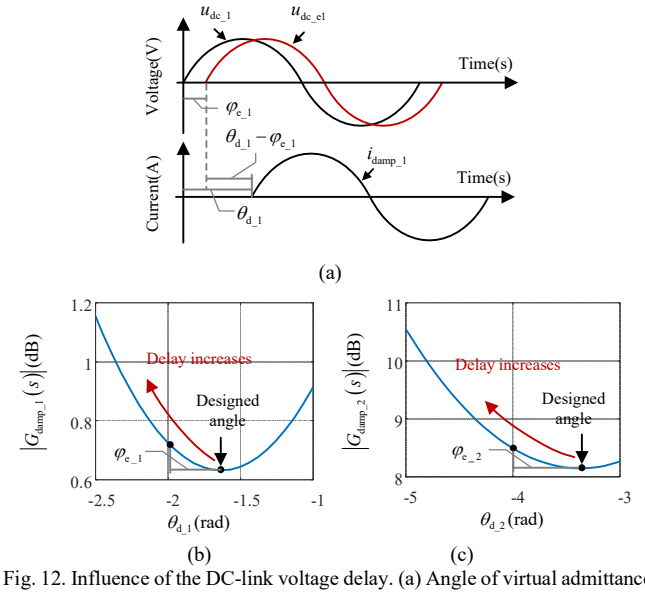


Fig. 12. Influence of the DC-link voltage delay. (a) Angle of virtual admittance. (b) Magnitude divergence due to voltage delay at the frequency of $6\omega_g$. (c) Magnitude divergence due to voltage delay at the frequency of $12\omega_g$.

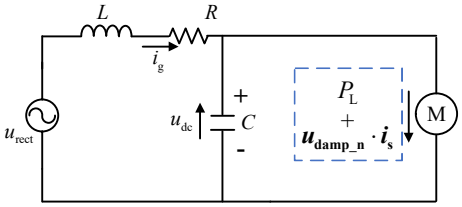
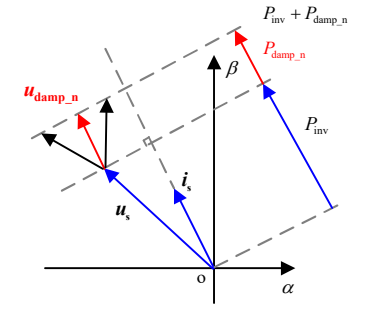
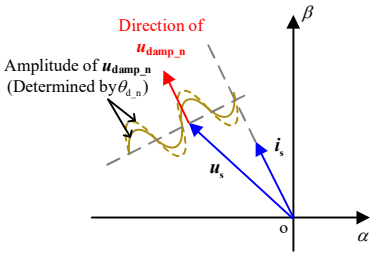


Fig. 13. Schematic diagram of damping control by motor power manipulation.



(a)



(b)

Fig. 14. Relation between the angle of virtual admittance and damping voltage. (a) Direction of damping voltage. (b) Amplitude of damping voltage.

This paper focuses on harmonic suppression due to the *LC* resonance in electrolytic capacitorless motor drives, which can also improve the power factor of the grid side.

The power factor can be expressed as

$$\mathrm{PF} = \frac{1}{\sqrt{1+\mathrm{THD}^2}}\cos\varphi \tag{20}$$

where φ is the phase difference between voltage and current.

As can be seen from (20), the reduction of THD can improve the power factor of the grid side.

C Design of Current Loop and Speed Loops

The open-loop transfer function of the d-axis current control loop can be shown as

$$C(s) = \frac{\left(k_{cp}s + k_{ci}\right)}{s}\frac{1}{R_s + sL_d}\frac{1}{T_s s + 1} \tag{21}$$

where k_{cp} and k_{ci} are the parameters of the current controller, respectively. R_s and L_d are the stator resistance and the d-axis inductance, respectively. T_s is the period of the PWM. Eq. (1.1) can be re-written as

$$C(s) = \frac{k_{cp}}{sL_d}\frac{\left(s + k_{ci}/k_{cp}\right)}{\left(s + R_s/L_d\right)}\frac{1}{T_s s + 1}. \tag{22}$$

In order to increase the dynamic performance of the current loop, the PI parameters should be set to eliminate the electromagnetism inertial element. So, the relation between k_{cp} and k_{ci} can be derived as

$$k_{ci} = \frac{R_s}{L_d}k_{cp}. \tag{23}$$

The closed-loop transfer function of the d-axis current control loop can be expressed as

$$G(s) = \frac{i_d}{i_d^*} = \frac{k_{cp}}{T_s L_d s^2 + L_d s + k_{cp}}. \tag{24}$$

Since $T_s L_d$ is very small compared with L_d, which can be ignored. The closed-loop transfer function of the d-axis current can be simplified as

$$G(s) = \frac{k_{cp}/L_d}{s + k_{cp}/L_d}. \tag{25}$$

As can be seen in (25), the bandwidth of the current loop is k_{cp}/L_d, which means the parameters of the PI controller can be determined by an expected bandwidth of the current loop. For example, if the expected bandwidth is ω_{cb}, then

$$\omega_{cb} = \frac{k_{cp}}{L_d}, \tag{26}$$

$$k_{cp} = \omega_{cb}L_d, \tag{27}$$

$$k_{ci} = \omega_{cb}R_s. \tag{28}$$

In order to achieve a better transient performance of the speed loop, the speed regulator should be carefully designed. The open-loop transfer function of the speed loop can be denoted as

$$H(s) = \left(k_{sp} + \frac{k_{si}}{s}\right)\frac{1}{T_{cb}s + 1}\frac{1}{Js} \tag{29}$$

where T_{cb} is the time constant of the current loop. k_{sp} and k_{si} are the coefficients of the speed regulator, respectively.

With the definition of the cutoff frequency ω_{sb} and the phase margin φ_m of the speed loop, the coefficients of the speed regulator can be derived as

$$k_{sp} = \sqrt{\left(1 + T_{cb}^2\omega_{sb}^2\right)\left(J^2\omega_{sb}^2\right)}\sin\left(\varphi_m - \arctan\left(\frac{1}{\omega_{sb}T_{cb}}\right) + \frac{\pi}{2}\right), \tag{30}$$

$$k_{si} = \omega_{sb}\sqrt{\left(1 + T_{cb}^2\omega_{sb}^2\right)\left(J^2\omega_{sb}^2\right)}\cos\left(\varphi_m - \arctan\left(\frac{1}{\omega_{sb}T_{cb}}\right) + \frac{\pi}{2}\right). \tag{31}$$

In order to simplify the calculation process, the following assumption is made that $T_{cb}\omega_{sb} \ll 1$. Therefore, the coefficients of the speed regulator can be obtained as follows

$$\begin{cases} k_{sp} = J\omega_{sb}\sin\varphi_m \\ k_{si} = J\omega_{sb}^2\cos\varphi_m \end{cases}. \tag{32}$$

IV. Experimental Results

The proposed impedance reshaping strategy is verified on a 5.5 kW electrolytic capacitorless PMSM drive as shown in Fig. 15. A 30 μF film capacitor and a 2.5 mH DC-link inductor are used. The AC input of the inverter is 380-Vrms (50 Hz). The motor parameters of L_d, L_q, R_s are 7.5 mH, 17.2 mH and 0.265 Ω, respectively. The controller parameters of the current loop are set as k_{cp}=14 and k_{ci}=500, respectively. The controller parameters of the speed loop are set as k_{sp}=2.6 and k_{si}=167, respectively. All the control algorithms are implemented in a TMS320F28075 chip. The inverter switching frequency is

fixed at 8 kHz, the same as the current and DC-link voltage sampling frequency as illustrated in Fig. 5. The test PMSM is connected with a load PMSM using a shaft. The load PMSM is working in the regenerating mode, and the regenerated power is consumed in a resistor.

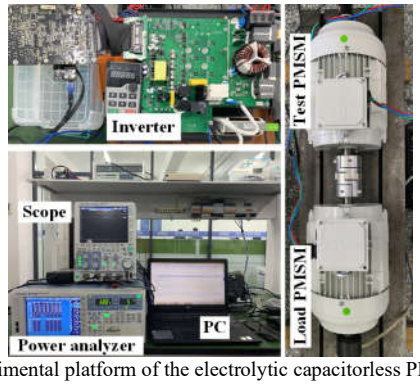


Fig.15. Experimental platform of the electrolytic capacitorless PMSM drive.

Fig. 16 shows the harmonic suppression at the frequency of $6\omega_g$ using the proposed strategy. The motor operating frequency is 70 Hz, and its output power is 5 kW. The system harmonic suppression effect and the motor side power disturbance are compared while changing the virtual admittance. Fig. 16(a), (b), and (c) show the results when θ_{d_1} is set as -2.4rad, -1.6rad, and -0.7rad, respectively, while $|Y_{d\_1}|$=0.04. Along with the increase of θ_{d_1}, the decrement of u_{dc_1} changes from 20.7% to 36.5% and finally to 27.9%. The tendency is consistent with the theoretical analysis as shown in Fig. 10. Meanwhile, the corresponding harmonics of the a-phase motor current changes from 17.7% to 27.6% and finally to 111.8%. Thus, setting $|Y_{d\_1}|$=0.04 and θ_{d_1}=-1.6 rad can suppress the harmonic effectively and will not distort the motor current excessively.

Similarly, the harmonic suppression at the frequency of $12\omega_g$ is shown in Fig. 17, and the motor operates under the same condition. Fig. 17(a), (b), and (c) show the results when θ_{d_2} is set as -2.6 rad, -3.4 rad, and -4 rad, respectively, while $|Y_{d\_2}|$=0.03. Along with the increase of θ_{d_2}, the decrement of u_{dc_2} changes from 5.6% to 31.6% and finally to 34.3%. The tendency can meet the theoretical analysis as shown in Fig. 11. Meanwhile, the corresponding harmonics of the a-phase motor current changes from 39.3% to 48.3% and finally to 84.0%. Thus, setting $|Y_{d\_2}|$=0.03 and θ_{d_2}=-3.4 rad can suppress the harmonic effectively and will not distort the motor current excessively.

Fig. 18 shows the grid current THD after applying the proposed impedance reshaping method. After enabling Y_{d_1}, THD can be improved from 51% to 39% by comparing Fig 18(b) and (c). By further enabling Y_{d_2}, THD can be improved to 35% as shown in Fig 18(d). It should be noted that, the power factor can also be improved from 0.87 to 0.93, after applying the proposed impedance reshaping method.

Fig. 19 shows the experimental results at the speed of 49 Hz and the load of 25 N·m. By comparing Fig. 19(a) and (b), the shape of the grid current can be improved effectively after applying the proposed impedance reshaping method. However, the torque ripple is improved from 5 N·m to 8 N·m.

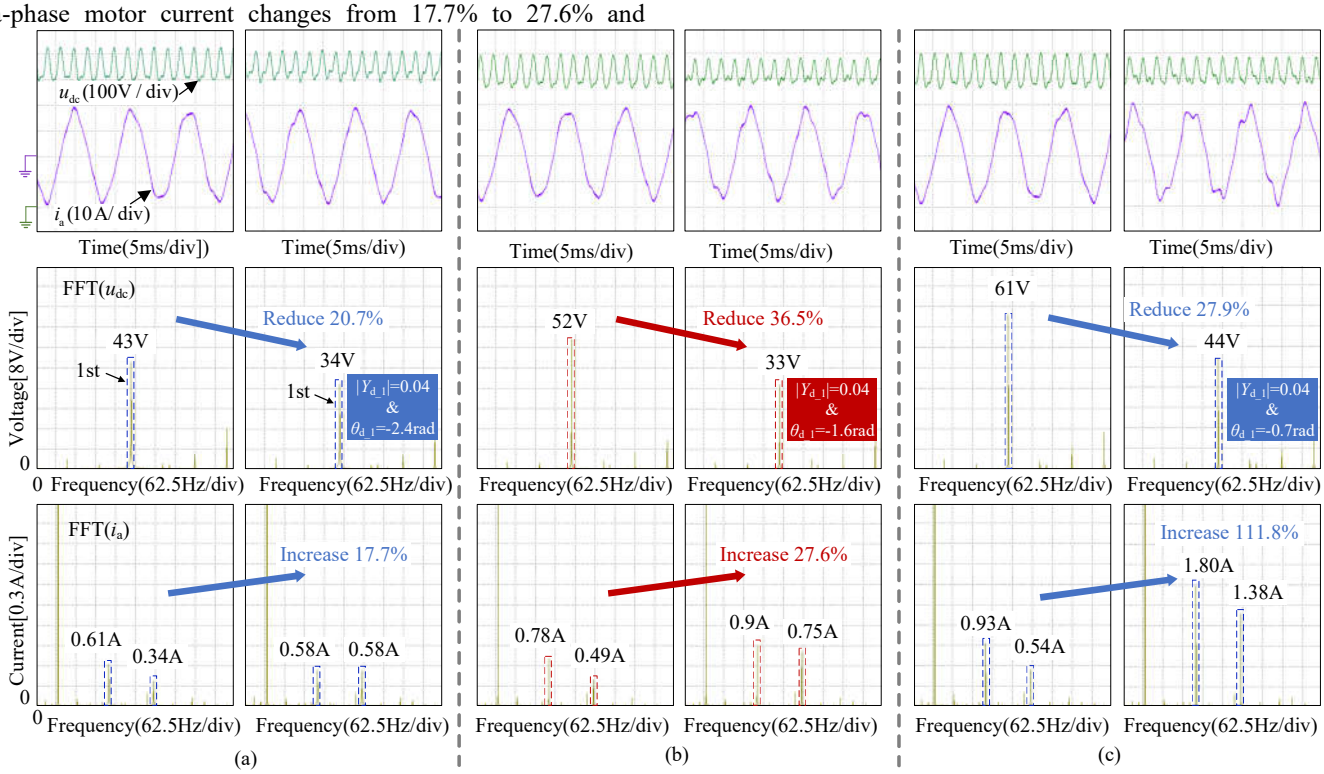


Fig. 16. Experimental results of harmonic suppression at the frequency of $6\omega_g$ using different virtual admittance. (a) $|Y_{d\_1}|$=0.04, and θ_{d_1}=-2.4 rad. (b) $|Y_{d\_1}|$=0.04, and θ_{d_1}=-1.6 rad. (c) $|Y_{d\_1}|$=0.04, and θ_{d_1}=-0.7 rad.

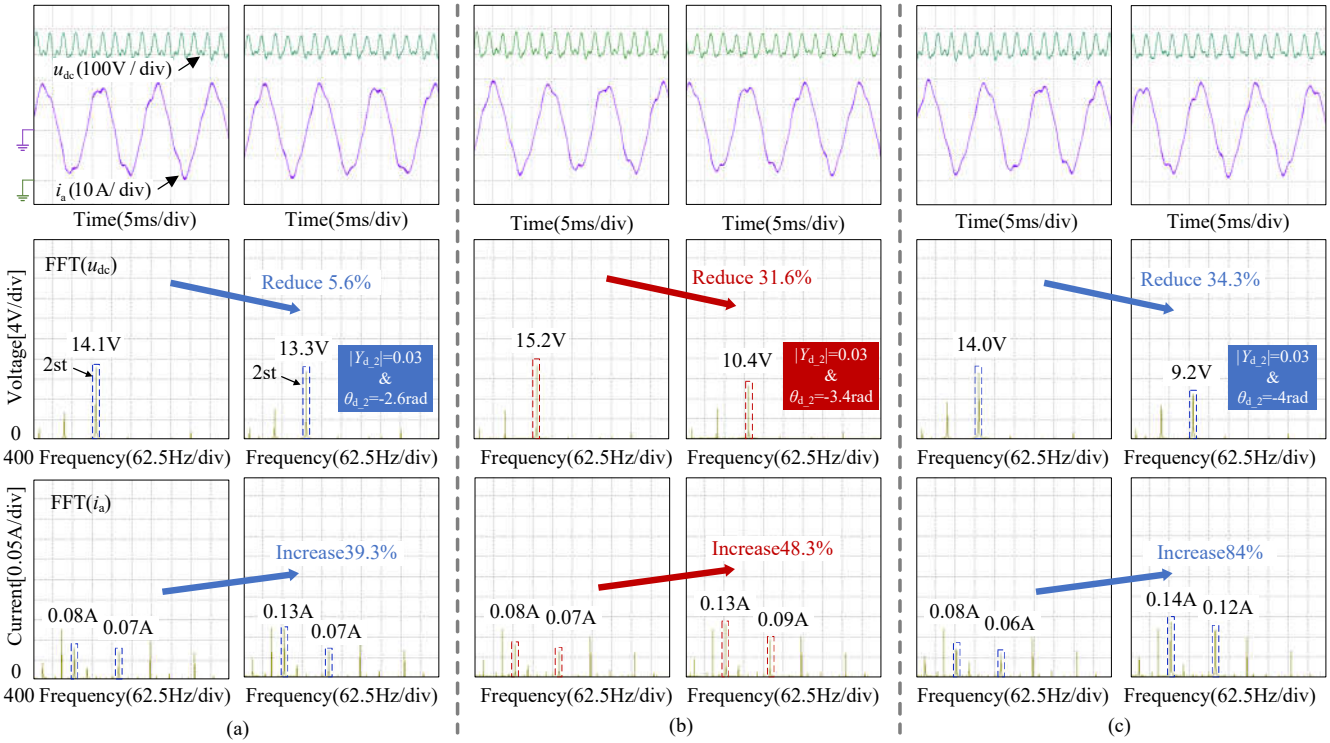
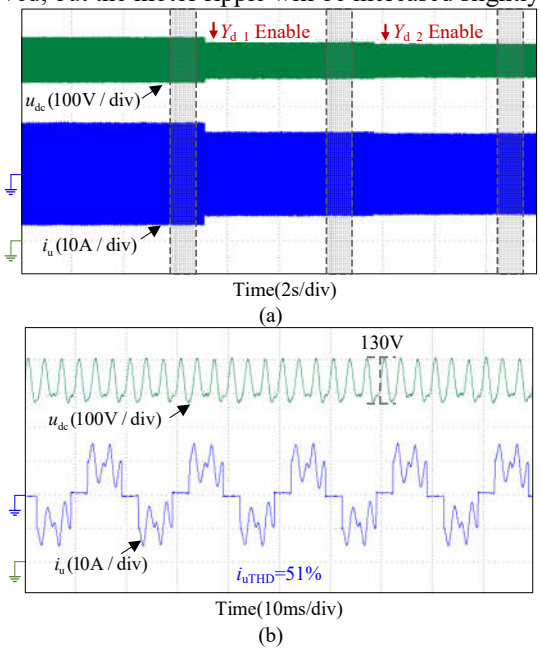


Fig. 17. Experimental results of harmonic suppression at the frequency of $12\omega_g$ using different virtual admittance. (a) $|Y_{d\_2}|$=0.03, and θ_{d_2}=-2.6 rad. (b) $|Y_{d\_2}|$=0.03, and θ_{d_2}=-3.4 rad. (c) $|Y_{d\_2}|$=0.03, and θ_{d_2}=-4 rad.

Fig. 20 shows the experimental results at the speed of 70 Hz and the load of 37 N·m. By comparing Fig. 20(a) and (b), the shape of the grid current can be improved effectively after applying the proposed impedance reshaping method. However, the torque ripple is increased from 10 N·m to 12 N·m. It can be concluded that after applying the proposed impedance reshaping method, the quality of the grid current can be improved, but the motor ripple will be increased slightly.



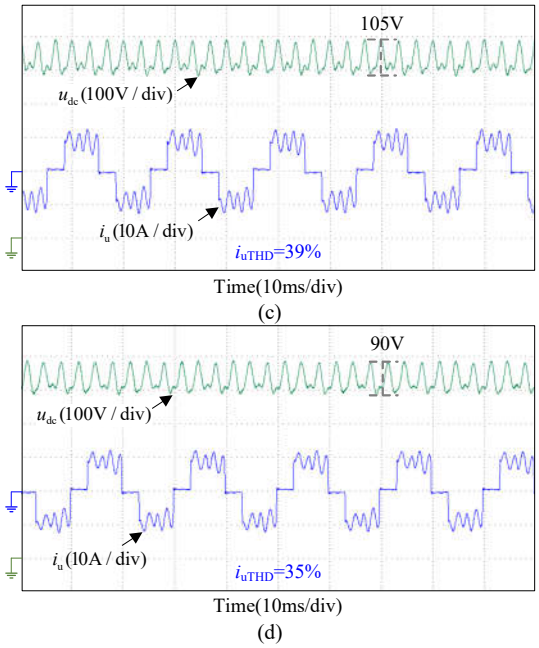


Fig. 18. Experimental waveforms of DC-link voltage and grid current. (a) Whole view. (b) Zoomed view before applying the impedance reshaping method. (c) Zoomed view after enabling Y_{d_1}. (d) Zoomed view after enabling Y_{d_2}.

Fig. 21 (a) and (b) show the experimental results at the motor frequency of 49 Hz before and after applying the proposed impedance reshaping method, respectively. As can be seen, the shape of the grid current can be improved after applying the impedance reshaping method, however, the speed ripple is increased to 2 Hz. Fig. 22 shows the similar results at

the motor speed of 70 Hz. As can be seen, the speed ripple is also around 2 Hz after applying the proposed method.

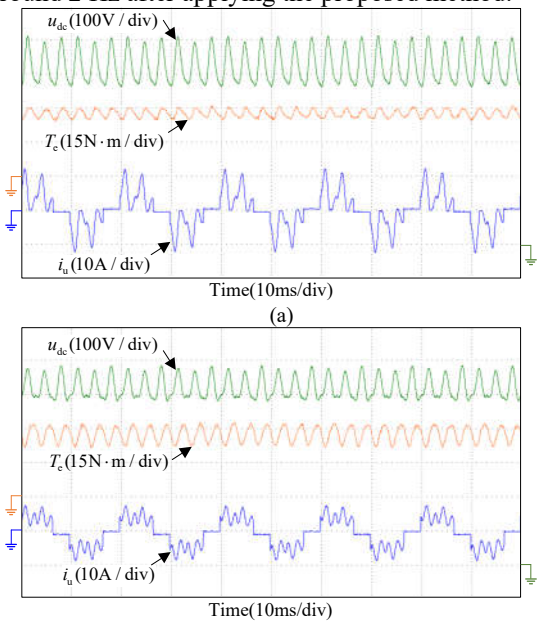


Fig. 19. Experimental results at the motor frequency of 49Hz and the load of 25 N·m. (a) Before impedance reshaping. (b) After impedance reshaping.

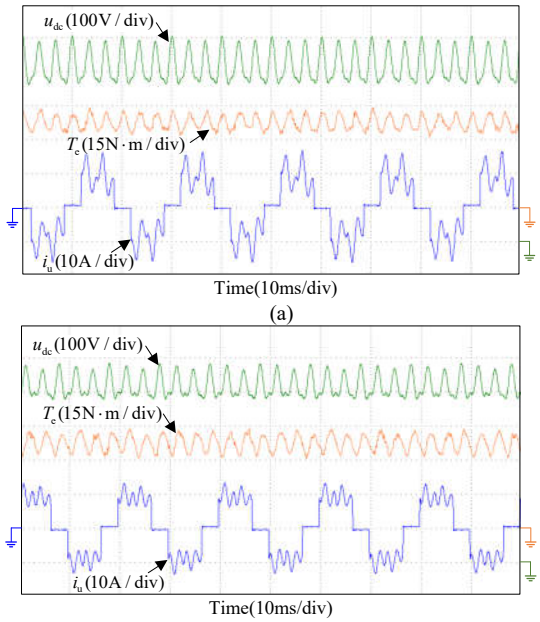


Fig. 20. Experimental results at the motor frequency of 70 Hz and the load of 37 N·m. (a) Before impedance reshaping. (b) After impedance reshaping.

Fig. 23(a) shows the dynamic process when the speed increases from 49 Hz to 70 Hz without using the proposed method, the DC-link voltage fluctuation reduces from 160 V to 140 V due to the increase of motor power. However, the DC-link voltage fluctuation is maintained at 90 V during the dynamic process by applying the proposed method as shown in Fig. 24(a). The comparison results show that, after applying the proposed method, the DC-link voltage fluctuation can be controlled effectively even in speed dynamic process.

Fig. 23(b) show the DC-link voltage, the torque, the speed and u-phase grid current at steady state. After applying the proposed impedance reshaping method, the torque contains the harmonics at the frequency of DC-link voltage as shown in Fig. 24(b). After applying the proposed impedance reshaping method, the quality of the grid current can be improved, but the torque ripple will increase. The same conclusion can be derived when comparing the results in Fig. 23(c) and Fig. 24(c).

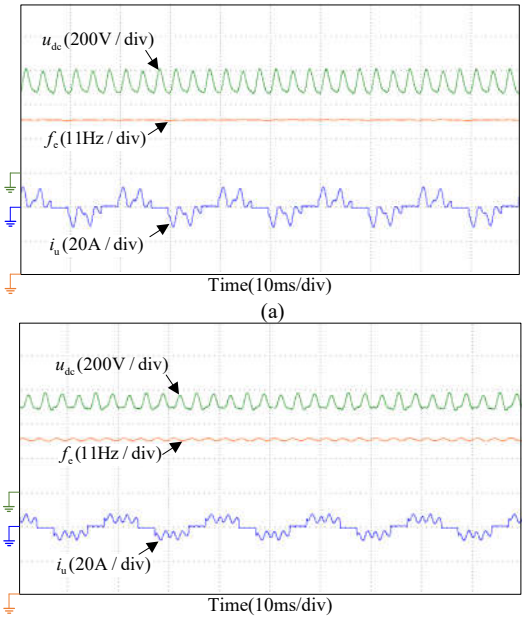


Fig. 21. Experimental results at the motor frequency of 49 Hz. (a) Before impedance reshaping. (b) After impedance reshaping.

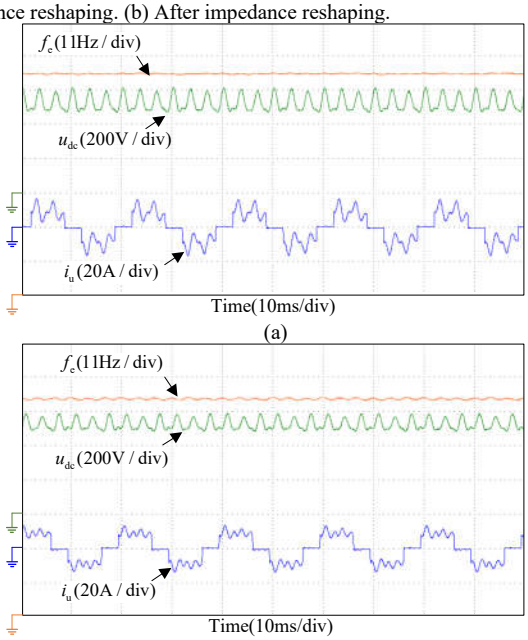


Fig. 22. Experimental results at the frequency of 70 Hz. (a) Before impedance reshaping. (b) After impedance reshaping.

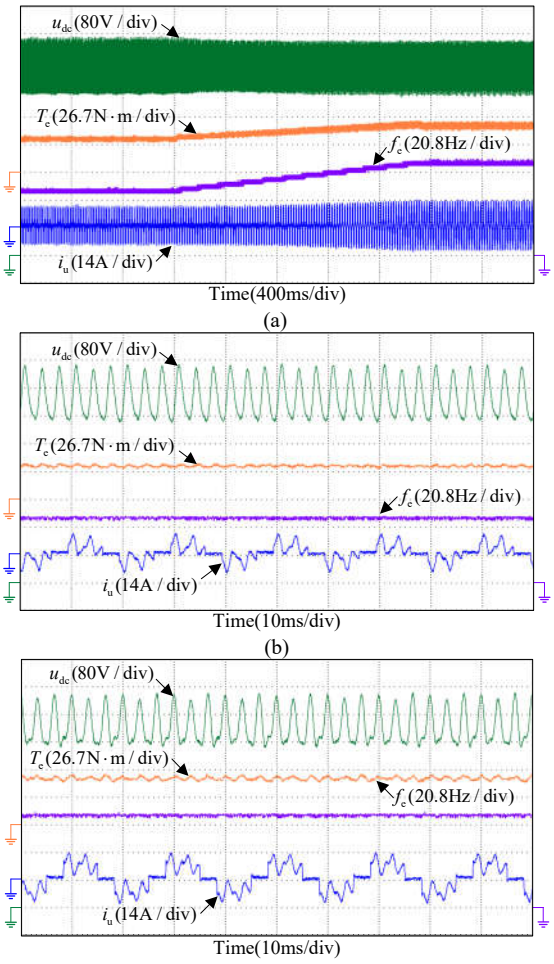
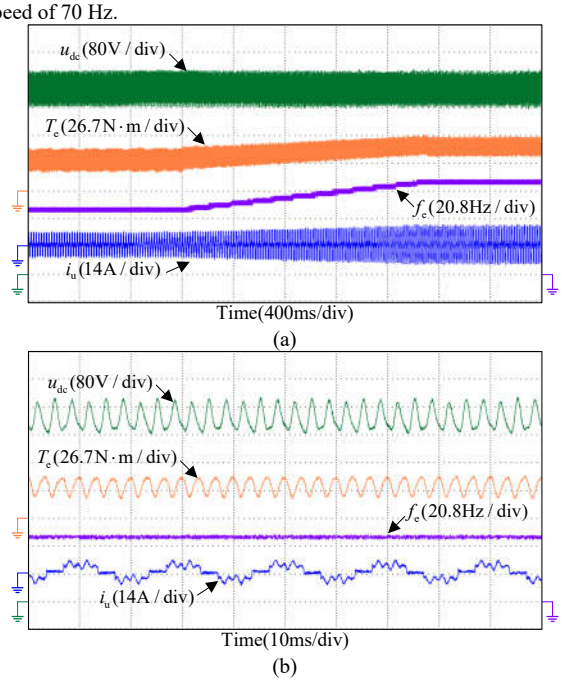


Fig.23. Experimental results of dynamic and stead-state performance without using the proposed method. (a) Speed increases from 49 Hz to 70 Hz. (b) Stead-state performance at the speed of 49 Hz. (c) Stead-state performance at the speed of 70 Hz.



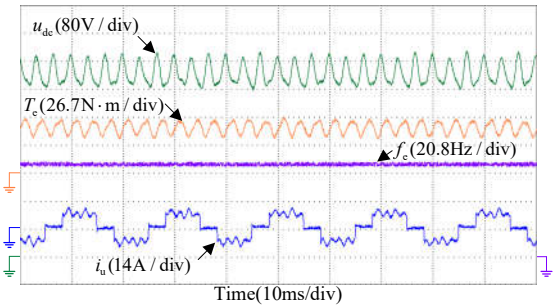
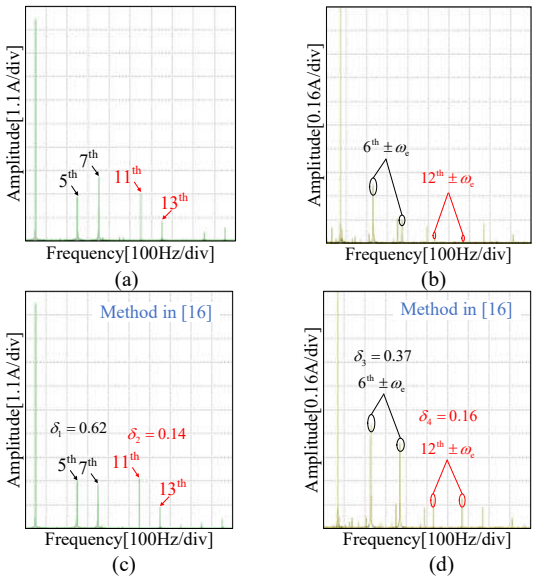


Fig.24. Experimental results of dynamic and stead-state performance by using the proposed method. (a) Speed increases from 49 Hz to 70 Hz. (b) Stead-state performance at the speed of 49 Hz. (c) Stead-state performance at the speed of 70 Hz.

Fig 25 shows the FFT analysis of the grid current and the motor current at the motor frequency of 70 Hz and power of 5 kW. Fig. 25 (b) and Fig. 25 (c) show the results with the grid side harmonic suppression method in [16], the grid harmonics can be suppressed when comparing Fig. 25 (a) with Fig. 25 (c). For sacrifice, harmonics in the motor are increased when comparing Fig. 25 (b) and Fig 25 (d). Fig. 25 (e) and Fig. 25 (f) show the experimental results using the proposed method, and the grid harmonics can be suppressed more effectively when comparing Fig. 25 (a) and Fig. 25 (e). δ represents the standard deviation of harmonics. In order to show the superiority of the proposed method, the ratio of standard deviation of the grid side and motor side harmonics after applying different strategies are compared. Taking the harmonics related to 6^{th} of the grid frequency as an example. As can be seen in Fig. 25 (c), Fig. 25 (d), Fig. 25 (e) and Fig. 25 (f), $\delta_1 / \delta_3 = 1.67$ and $\delta_5 / \delta_7 = 1.91$, which means the proposed method can achieve better grid side harmonics suppression effect with lower motor side disturbance.

The comparisons of the method in [16] and the proposed method are shown in Table I. The proposed method has satisfactory performance the grid current and the motor current.



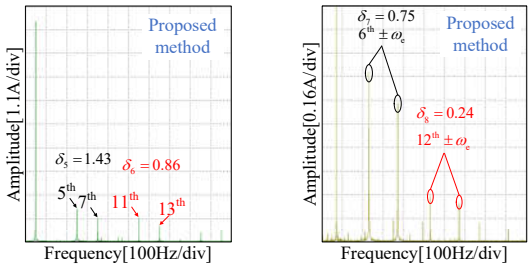


Fig. 25. FFT analysis of the grid current and the motor current. (a) Result of the grid current without using grid side harmonic suppression methods. (b) Result of the motor current without using grid side harmonic suppression methods. (c) Result of the grid current with the grid side harmonic suppression method in [16]. (d) Result of the motor current with the grid side harmonic suppression method in [16]. (e) Result of the grid current with proposed grid side harmonic suppression method. (f) Result of the motor current with proposed grid side harmonic suppression method.

TABLE I
COMPARISONS OF THE METHOD IN [16] AND THE PROPOSED METHOD

Items / Methods	Ratio of standard deviation of the grid side and motor side harmonics	
Method in [16]	$\delta_1/\delta_3=1.67$	$\delta_2/\delta_4=0.88$
Proposed method	$\delta_5/\delta_7=1.91$	$\delta_6/\delta_8=3.58$

Fig. 26 shows the statistics of the grid current THD under different inverter output powers. The conclusion can be obtained that, after enabling the proposed impedance reshaping method, THD can always be improved under different power conditions.

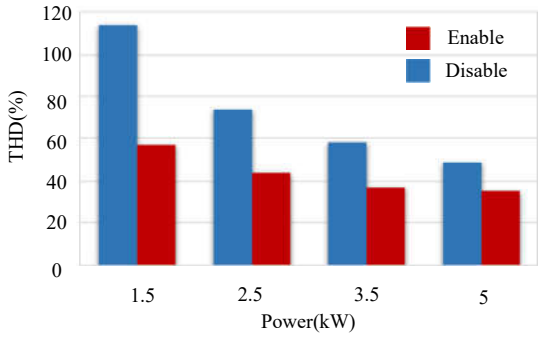


Fig. 26. Experimental results of the grid current THD under different output powers.

Fig. 27 shows the experimental results of the power factor in the grid side under different output power. The conclusion can be obtained that, the power factor can be improved using the proposed method under different power conditions.

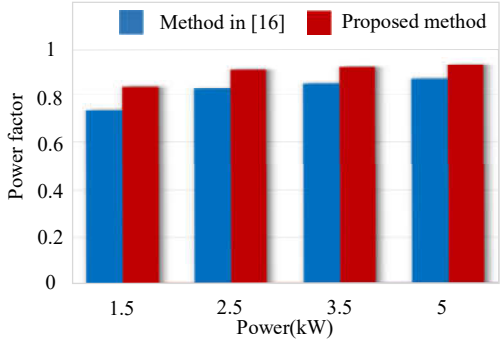


Fig. 27. Experimental results of the power factor in the grid side under different output powers.

V. CONCLUSION

This paper focuses on harmonic suppression due to the *LC* resonance in electrolytic capacitorless motor drives. The system model is derived by taking the DC-link voltage delay and the bandwidth of the current loop into consideration. Instead of increasing the system damping for *LC* resonance suppression, the motor side power disturbance can be reduced with more effective harmonic suppression by carefully tackling with the inherent harmonics around *LC* resonance frequency. Also, the angle of virtual admittance is compensated by taking the sampling delay of the DC-link voltage into consideration to achieve a more accurate damping current. The proposed algorithm integration is easy for industrial application and does not require additional hardware circuits. Experimental results show the effectiveness of the proposed method, the DC-link voltage fluctuation can be reduced from 130V to 90V, and THD of the grid currents can be improved from 51% to 35% at 5kW.

APPENDIX

Due to the sampling delay, the relationship between equivalent sampling DC-link voltage and DC-link voltage can be derived as

$$u_{dc\_e}(s)=u_{dc}(s)e^{-1.5sT_s}. \tag{A1}$$

The small-signal model of motor voltages in (4), the relationship between the DC-link voltage and motor voltages can be obtained

$$\begin{bmatrix}u_d(s)\\u_q(s)\end{bmatrix}=\frac{u_{dc0}}{u_{dc\_e0}}\begin{bmatrix}u_{dref}(s)\\u_{qref}(s)\end{bmatrix}+\frac{u_{dc}(s)}{u_{dc\_e0}}\begin{bmatrix}u_{dref0}\\u_{qref0}\end{bmatrix}-\frac{u_{dc0}u_{dc}(s)e^{-1.5T_ss}}{u_{dc\_e0}^2}\begin{bmatrix}u_{dref0}\\u_{qref0}\end{bmatrix}. \tag{A2}$$

The mathematical model of PMSM can be expressed as

$$\begin{bmatrix}u_d(s)\\u_q(s)\end{bmatrix}=\begin{bmatrix}R_s+L_ds & -\omega_eL_q\\ \omega_eL_d & R_s+L_qs\end{bmatrix}\begin{bmatrix}i_d(s)\\i_q(s)\end{bmatrix} \tag{A3}$$

where R_s is the stator resistance, $L_{d,q}$ are the inductance at dq-axes, and ω_e is the motor speed.

In this paper, the typical vector control method is applied, so the voltage references can be denoted as

$$\begin{bmatrix}u_{dref}(s)\\u_{qref}(s)\end{bmatrix}=\begin{bmatrix}-G_d & -\omega_eL_q\\ \omega_eL_d & -G_q\end{bmatrix}\begin{bmatrix}i_d(s)\\i_q(s)\end{bmatrix} \tag{A4}$$

in which G_d and G_q are current regulators, and can be expressed as

$$G_d=\omega_{cb}L_d+\frac{\omega_{cb}R_s}{s},\ G_q=\omega_{cb}L_q+\frac{\omega_{cb}R_s}{s} \tag{A5}$$

where ω_{cb} is the bandwidth of the current loop.

Consequently, the relationship between the motor currents and the DC-link voltage can be obtained as

$$\begin{bmatrix} R_s + L_d s + \dfrac{u_{dc0}}{u_{dc\_e0}} G_d & -\omega_e L_q + \dfrac{u_{dc0}}{u_{dc\_e0}} \omega_e L_q \\ \omega_e L_d - \dfrac{u_{dc0}}{u_{dc\_e0}} \omega_e L_d & R_s + L_q s + \dfrac{u_{dc0}}{u_{dc\_e0}} G_q \end{bmatrix} \begin{bmatrix} i_d(s) \\ i_q(s) \end{bmatrix} = \frac{u_{dc}(s)}{u_{dc\_e0}} \begin{bmatrix} u_{dref0} \\ u_{qref0} \end{bmatrix} - \frac{u_{dc0} u_{dc}(s) e^{-1.5T_s s}}{u_{dc\_e0}^2} \begin{bmatrix} u_{dref0} \\ u_{qref0} \end{bmatrix} \quad \text{(A6)}$$

The mean values of DC-link voltage and equivalent sampling DC-link voltage can be regarded as the same, so (A6) can be simplified to

$$\begin{bmatrix} i_d(s) \\ i_q(s) \end{bmatrix} = \frac{1 - e^{-1.5T_s s}}{u_{dc\_e0}} u_{dc}(s) \begin{bmatrix} \dfrac{u_{dref0}}{R_s + L_d s + G_d} \\ \dfrac{u_{qref0}}{R_s + L_q s + G_q} \end{bmatrix}. \quad \text{(A7)}$$

The relationship between the motor voltages and the DC-link voltage can also be obtained as

$$\begin{bmatrix} u_d(s) \\ u_q(s) \end{bmatrix} = \begin{bmatrix} R_s + L_d s & -\omega_e L_q \\ \omega_e L_d & R_s + L_q s \end{bmatrix} \begin{bmatrix} \dfrac{u_{dref0}}{R_s + L_d s + G_d} \\ \dfrac{u_{qref0}}{R_s + L_q s + G_q} \end{bmatrix} \frac{1 - e^{-1.5T_s s}}{u_{dc\_e0}} u_{dc}(s) \quad \text{(A8)}$$

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