Assessment and Augmentation of Power Converter Control Towards Enhanced Power System Stability

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Kongens Lyngby, Denmark

Center for Electric Power and Energy
Department of Electrical Engineering

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Center for Electric Power and Energy (CEE)
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Professor Campbell Booth,University of Strathclyde
Doctor Jay Ramachandran, National Grid ESO

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Preface

This thesis is prepared at the Department of Electrical Engineering of the Technical University of Denmark in partial fulfillment of the requirements for acquiring the degree of Doctor of Philosophy in Engineering. The Ph.D. project was funded by the project Phoenix project, funded by Ofgem under Network Innovation Competition programme, Project Direction ref: SPT / Phoenix / 16 December 2016 (https://www.spenergynetworks.co.uk/pages/phoenix.aspx).

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The thesis is composed of 5 scientific papers, 3 of which have been peer-reviewed and published, whereas the remaining one is currently under review, and one more to be submitted.

Kanakesh Vatta Kkuni
August 2021

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Your Name

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Abstract

Ambitious global carbon emission targets are driving a substantial increase in renewable energy. Most of the renewable generations are wind and solar, which utilizes a power converter-based interface for integration into the power system. In addition to renewable generation, the power converters are also the building blocks in other technology solutions such as High Voltage Direct Current (HVDC) transmission systems, Battery Energy Storage Systems (BESS), Flexible Alternating Current Transmission Systems (FACTS), and battery electric vehicles. Such massive integration of power converters into the system is transforming the power system dynamics. In contrary to synchronous machines/generator (SG), where dynamics and responses are affected by its physical characteristics, the control of the power converters directly determines the dynamics and responses within the hardware limits. As a consequence, the power converter control plays a significant role in power system operation and stability.

The power converter control is generally classified as grid following control with a current source characteristic and grid forming control with voltage source characteristics. While grid forming converter (GFC) possesses superior response and dynamics over grid following converter (GFL), particularly in weak grid conditions, the majority of the converters integrated into the system are GFL due to their mature technology. Consequently, the power system will in the future constitute a mix of GFC, GFL, and SG. Hence, it is now imperative to investigate the impact of GFC and GFL on system stability.

This thesis develops a comprehensive assessment of the GFL and GFC using time-domain, eigenvalues, and impedance-based analysis to address potential instabilities. Design considerations are derived for both converters to avoid instability originating due to the converter control derived. In addition, the interaction of the converter with the synchronous machine is assessed based on a simplified system model.

Besides the small-signal approach, a transient response evaluation of the GFC and GFL is conducted with focus on the synchronization block in GFC and GFL. In this thesis, an improved PLL model, (synchronization block in GFL) is proposed. Furthermore, a compensation method that improves the PLL dynamics during large voltage transients is also proposed. Likewise, for GFC, the response of the synchronization block during the transient events is investigated. The phenomena of loss of synchronization in GFC during different frequency, phase, and transient voltage events are demonstrated analytically and illustratively. The impact of the current limiter of the GFC's on the system synchronization stability during transient disturbances is presented, and a method is proposed for improvement. All the proposed solutions are validated in power hardware in the loop simulation.

Resumé

De ambitiøse globale CO2 mål driver en øget produktion og anvendelse af vedvarende energi. Med vedvarende produktion menes oftest vind og sol, som benytter sig af en konverterbaseret grænseflade i integrationen med el-systemet. Ud over vedvarende energiproduktion er konverterne også afgørende byggestenene i andre teknologiløsninger såsom HVDC-højspændings-DC-transmissionssystemer , BESS (Battery Energy Storage systems), fleksible vekselstrømstransmissionssystemer (FACTS) og batteri-elektrisk køretøjer (biler). En så massiv integration af (power) konverter i systemet ændrer hele el-systemets dynamik. I modsætning til en synkronmaskine (SG), hvor respons og dynamik hovedsageligt bestemmes af maskinens fysiske egenskaber, bestemmes konverterens dynamik og respons alene af konveterens hardwaregrænser. Som en konsekvens heraf, spiller konverterstyring en væsentlig rolle i driften og stabiliteten af el-systemet.

Konverterstyring klassificeres generelt (de fleste driftsformer) som frekvensfølger, hvor konverteren styres som en strømkilde eller som frekvensgiver-former, hvor konverteren styres som en spændingskilde. Mens frekvensgivende-konverter (GFC) har en overlegen respons og dynamik i forhold til frekvens følgende konvertere (GFL). Især svage el-net, er størstedelen af de anvendte konvertere af type GFL på grund af deres mere modne teknologi. Derfor indeholder el-nettet i dag en blanding af GFC, GFL og SG. Derfor er det nu bydende nødvendigt at undersøge indvirkningen af GFC og GFL på systemstabiliten.

Denne afhandling præsenterer en omfattende analyse af GFL og GFC ved hjælp af tidsdomæneanalyse, egenværdier og impedansbaseret metoder til at adressere potentielle ustabiliteter. For at undgå ustabilitet i el-nettet forårsaget af konverterstyringen, udledes, baseret på analysen, designregler for konverterstyring af begge konvertertyper. Derudover vurderes vekselvirkningen mellem konverteren og synkronmaskinen ud fra en forenklet systemmodel.

Udover analysen af småsignaler foretages en transientanalyse af responsen fra GFC og GFL med fokus på synkroniseringsblokken i GFC og GFL. I denne afhandling præsenteres en forbedret PLL-model, dvs. synkroniseringsblokken i GFL. Desuden foreslås en kompensationsmetode, der forbedrer PLL-dynamikken ved store spændingstransienter. Ligeledes undersøges for GFC responsen fra synkroniseringsblokken ved en kortvarig begivenhed. Fænomener med tab af synkronisering i GFC ved forskellige frekvens-, fase- og transiente spændingshændelser demonstreres analytisk og illustrativt. Virkningen på systemstabiliteten af strømbegrænsningen i GFC'erne ved forbigående forstyrrelser præsenteres, og en metode til forbedring af denne foreslås. Alle de foreslåede løsninger valideres i "power-hardware in the loop"-simuleringer.

Acronyms

ENTSOE European Network of Transmission System Operators for Electricity

MIMO Multiple-Input and Multiple-Output

SISO Single-Input and Single-Output

PE Power Electronic

PHIL Power Hardware-in-the-Loop

ITM Ideal Transformer Method

HUT Hardware Under Test

IGBT Insulated-gate bipolar transistor

NI National Instruments

GPIC General Purpose Inverter Controller

GTAO Gigabit Transceiver Analogue Output Card

GTAI GIGA-TRANSCEIVER ANALOGUE INPUT CARD

HVDC High Voltage Direct Current

PCC Point of Common Coupling

PWM Pulse Width Modulation

RE Renewable Energy

RTDS Real Time Digital Simulator

SG Synchronous Generator

STATCOM Static Synchronous Compensator

VSC Voltage Source Converter

BESS Battery Energy Storage systems

ENTSOE European Network of Transmission System Operators for Electricity

GFL Grid Following Control

GFC Grid Forming Control

PLL Phase Locked Loop

ITM Ideal Transformer Interface

EMT Electromagnetic Transient

RMS Root Mean Square

CHAPTER 1

Introduction

1.1 BACKGROUND

With an objective of sustainable earth, an agreement between the nations around the globe is in place to increase the share of Renewable Energy (RE). For most countries, several policies and clear time-bound RE targets are in place. For instance, from the scenarios outlined by Europe's Ten Year Network Development Plan published by European Network of Transmission System Operators for Electricity (ENTSOE), version 2020 [3], it is expected that in 2030 64% of the power demand will be met by renewable energy, and by 2040, that RE contribution is expected to rise to 78 %. Most of these RE sources are wind and solar, interfaced to the power system through Voltage Source Converter (VSC) base PE technology. In addition to integrating RE, the VSC are also being introduced into the power systems as technology solutions in the form of High Voltage Direct Current (HVDC) transmission systems, Battery Energy Storage systems (BESS), flexible alternating current transmission systems (FACTS), and battery powered vehicles. As a result of this significant increase in PE devices, it is now clear that Power Electronic (PE)-based devices, mainly VSC will increasingly influence power system dynamics. Differing from a synchronous machine, responses and dynamics of VSC based generation within the hardware capabilities are shaped by implemented control. Therefore, it is imperative to have a stable and secure power converter control for a reliable power system.

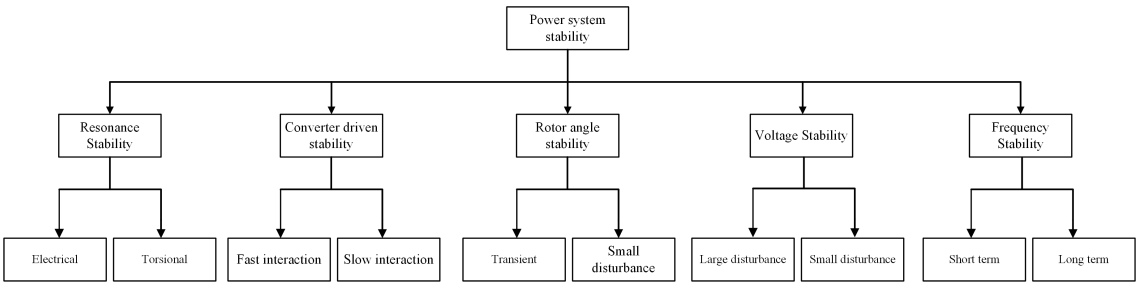

Figure 1.1: The power system stability classifications[1], the considered stability events are highlighted

The emergence of sizeable PE- based devices in the system has prompted a joint task force set up by IEEE Power System Dynamic Performance Committee and the CIGRE Study Committee to classify and define the new stability phenomena in the power system [1] as shown in Fig. 1.1. In addition, the progressive replacement of the conventional Synchronous Generator (SG) based generations with asynchronous RE and transition from a classical centralized power system towards a decentralized power system, is radically remodeling the existing power system architecture, which results in lower system strength and lower inertia. Such a transition presents several challenges[4–11] to the power system.

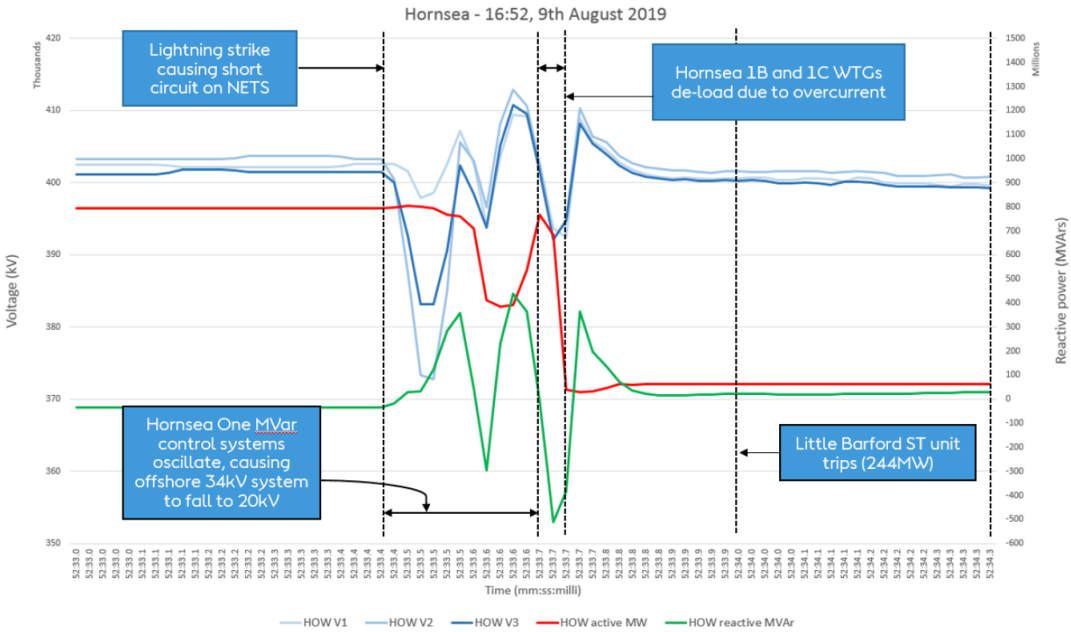

Figure 1.2: Measurements at the Hornsea offshore windfarm in response to voltage dip caused due to lightning strike on 9 August 2019

There have been multiple recent grid disturbances wherein the unanticipated responses from PE-based generation were the primary cause. For instance, Fig. 1.2 shows the measurements from the Hornsea offshore wind farm during a voltage dip event caused due to a lightning strike. The event subsequently resulted in the de-loading of the wind turbines due to overcurrent. The de-loading of wind turbines, together with the loss of steam turbine-based generation, resulted in major outages across Great Britain's electricity system [12]. It was also observed that the response of the wind farm was oscillatory even before the event. Similarly, there have been multiple real-world cases of unanticipated responses or interactions due to PE renewables worldwide [12–18]. Finally, most of these outages are unique, exemplifying the challenges introduced due to high PE penetration.

Therefore, there is a greater need to clearly understand the factors contributing to these new stability challenges introduced by massive integration of power electronics and develop methods that can mitigate such stability challenges. Since the power converter response and dynamics is control dominated, it is necessary to assess the existing control methods for power converters to increase system stability.

1.1.1 Power converter control functions

Among the PE configuration, the VSC are most widely employed. Unlike a synchronous machine control, several configurations exists in the control of a VSC. A General control architecture of the grid-connected VSC is shown in Fig. 1.3. A supervisory layer could have many tasks of high level in nature, including but not limited to

- Ensuring enough stored energy and power to meet system-level services (frequency support, voltage support) and accordingly calculate the possible system support parameters such as frequency droop, inertia, etc.

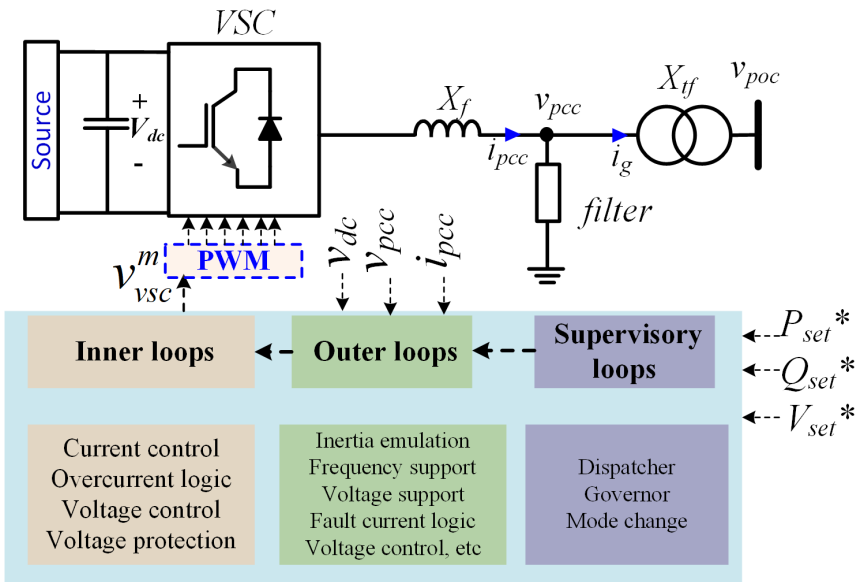

Figure 1.3: VSC control architecture

- Communicating with the external system to obtain the dispatch parameters (active and reactive power (P^*_{set}, Q^*_{set}) or voltage set point(V^*_{set}))
- supervising mode change events, for instance, determine when to enter exit fault ride through mode
- maximum power point tracking

The outer control typically includes the system level services and tasks expected of a power converter, the outer loop tasks could include

- Frequency services such as inertia emulation and fast frequency support
- Active power, reactive power control loop
- Voltage support
- Fault current logic
- DC voltage control

The inner loops receives the set points from the outer loop and attempts to regulate instantaneous voltage and/or currents, the crucial tasks of protecting the converters is also carried out by the inner control loops.

The non uniqueness of VSC control structures for different applications makes it difficult to classify. Conventionally, the power converters have an inner current control and are synchronized to the grid by employing a Phase Locked Loop (PLL). The VSC converters employing such control are termed as Grid Following Control (GFL) as they follows the grid voltage [19–21]. A simplified equivalent structure of a grid following converter is shown in Fig. 1.4. The current references are generated from the outer loops typically assigned to control the power and voltages. There is a

current limiter placed on the reference currents given to current control to ensure the operation of the converter within its operating capabilities. The triggering of these limiters presents a different control mode for the grid following converter. The GFL should also have fault ride through mode (FRT), which directs the converters' output currents to comply with grid operator standards during grid fault conditions. Grid supporting functionalities such as voltage support and frequency support can be programmed in the outer loops of grid following converter and is a requirement for converter interfaced generation and HVDC in some grid codes [22–24]. The dynamics of the PLL has been found to play a crucial role in defining the quality of the response from power converter as well as possible instabilities when the grid strength is weak [25–27].

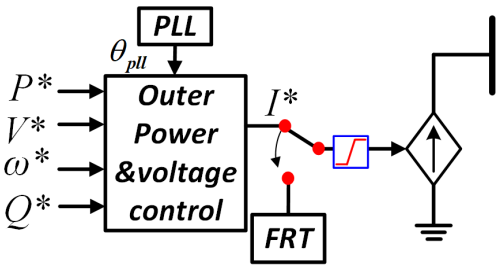

Figure 1.4: Grid following converter, simplified representation

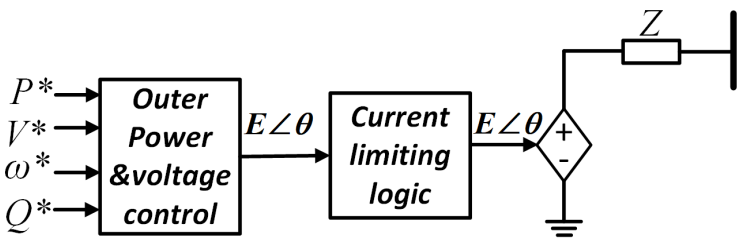

Figure 1.5: Grid forming converter, simplified representation

The Grid Forming Control (GFC) offer many advantages over GFL converters with faster, near-instantaneous response to external events and shown to have a larger stability range. The grid forming converters are controlled as voltage sources. The simplified equivalent circuit of the GFC's is shown in Fig. 1.5. The synchronization for grid forming converter is derived from the injected power[26, 28–32]. It is possible to emulate the dynamics of an SG by virtually programming the electromechanical model of the synchronous generator to the outer loop. The outer loop in GFC typically generates the reference voltage and angle. A current limit logic is necessary to be implemented in the GFC protection. However, the current limit logic is not straightforward as the GFC is controlled as a voltage source.

1.1.2 VSC key characteristics and differences with Synchronous generator

Before one can outline the challenges put forward by VSC technologies, it is necessary to understand the characteristics of SG that formed the backbone of the power system and ensured a very reliable supply for decades. Although there have been some stability challenges related to SG such as rotor angle stability, subsynchronous torsional oscillation, transient stability, and slow voltage/reactive power control. Such events have been well studied, and community knowledge exists in handling

such events by means of planning, protection, power system stabilizers, and by deploying FACTS [33]. The synchronous machine has high technology readiness, and modeling has matured. Furthermore, there is little difference in the behavior and response of the synchronous machine across the manufacturers. In addition, the SG has high thermal withstands capability, which allows high robustness in SG response. To illustrate, fig. 1.6 shows the field current limit for a typical SG [2], one could observe that for a few seconds, the field can be forced even beyond two times SG's rated excitation level. Similarly, the other limiters implemented on SG, such as the over-excitation limiter and stator current limiters, also ensure that the machine is within its thermal capability and acts very slowly. For this reason, the limiters are only necessary to be modeled for sustained events such as long-term voltage stability and not essential for transient or small-signal simulations.

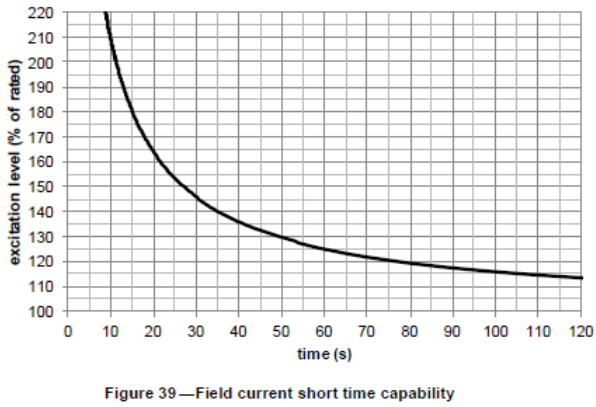

Figure 1.6: Field current capability [2]

On the other hand, VSC are built of fast switching semiconductor devices and thus have dynamics and harmonics at a much higher bandwidth. These low time constants of power converter present a significant change from the dynamics of large synchronous machines, which are typically slow and have been time-tested and shown to be robust. Hence IEEE task force on stability definitions has updated the time frame classification of power system dynamics shown in Fig. 1.7 to include power converter dynamics. Also from a hardware perspective the power converters have much lower overload capacity than SG due to the sensitive electronics.

From the control perspective, the current source behavior of the grid following converter restrict it from providing instantaneous inertial and fault current support [34, 35]. Several grid codes have imposed the GFL based solutions to provide system supporting functions such as fast frequency control and fast fault current injection [22–24]. And it has been shown that such extra function in GFL can reduce the rate of change of frequency (ROCOF) following a disturbance [36–39]. However, it is understood that the fault current contribution and fast frequency support from GFL cannot replicate the inertial and fault current contribution of SG, which is instantaneous and can be multiple times higher than its own rating citejia2018impact,NERC,ENTSO-E2019,liu2015comparison. Furthermore, the various control components in the GFL, such as inner current control, outer power, voltage control, and PLL, all have different bandwidths. If the grid strength is weak, these control components can lead to adverse interactions with the network in a wide frequency range, leading to oscillations [40]. Such characteristics of GFL has been shown to limit the overall GFL penetration level in the system [34]. The characteristic difference between the GFL converters and SG are summarized in Table. 1.1.

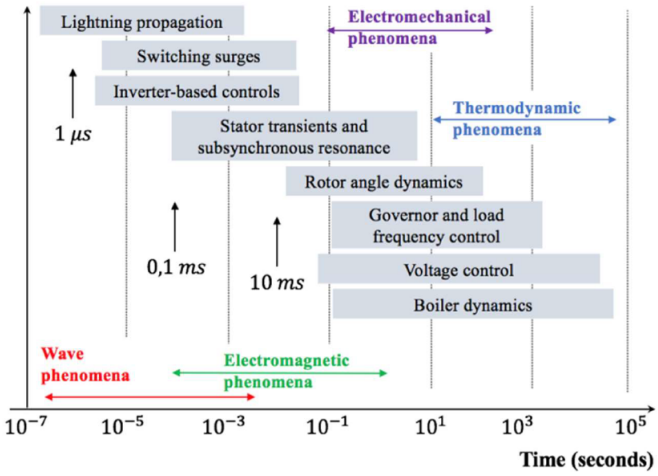

Figure 1.7: Power system times scales defined by IEEE task force on stability definitions [1]

Table 1.1: Differences between the synchronous generator and grid following converter

Synchronous generator	**Grid following converters**
Voltage source behind an impedance Characteristics	Current source characteristics
Instantaneous inertia	Possibility of synthetic inertia
High overload capacity (3-5 pu for short duration limited by thermal time constant)	Low over load, Constrained by the overcurrent limiter, typical values 1.1 - 1.3 pu
Low bandwidth controls	Bandwidths can be quite high
Can transfer power close to theoretical limits at low grid strength	Power transfer limited by PLL and controllers
Necessary to model limiters	Necessary to consider the limits for small signal and transient studies

A grid forming converter, on the other hand, has a voltage source behind an impedance characteristic [41]. Therefore, a near-instantaneous inertial and fault current contribution is possible from grid-forming converters. In addition, an active power-based synchronization is employed in GFC simillar to the SG, and this feature has been shown to extend the power transfer capacity in a weak grid closer to the theoretical limit [26, 42, 43]. Furthermore, by limiting the control bandwidths below 5 Hz, the control-related challenges for power converters, such as oscillations, can be reduced [44, 45]. However, because of the voltage source behavior, large current overshoots could occur in GFC during transients, and thus, GFC needs fast-acting effective current limiting algorithms to avoid the converter going into a protective tripping. The voltage source behavior also presents a hardware challenge in optimizing the GFC ratings to withstand sudden overshoots. During the protective limit triggering, the operational mode of GFC is transitioning to the current limited mode. Therefore, the operation of GFC in this mode also needs to be carefully studied.

1.1.3 Phoenix Project

The Ph.D. is a part of the project titled "Phoenix - System Security and Synchronous Compensators." in which DTU is involved along with project partners ABB, National Grid ESO, SP Transmission

(SPT), and the University of Strathclyde. The project also involved a live field trial of 140 MVA Hybrid Synchronous Condenser and Static Synchronous Compensator (STATCOM) in Scotland and aimed to investigate the hybrid solution based on SC and STATCOM. In addition, the project also investigated the potential of a hybrid solution based on SC and BESS, and PE converter, for alleviating the adverse effects of increased penetration of asynchronous renewable energy. As a part of the Phoenix project, this Ph.D. project investigated the interface VSC control strategies for the BESS.

1.2 Motivation and Objective

The energy transition towards renewables is introducing a significant amount of power converters in the power system. The substantial introduction of GFL converters in the form of RE interface, FACTS, HVDC and BESS, negatively influences the power system dynamics. Although GFC has superior stabilizing characteristics over GFL, a significant proportion of the power system composition will still be GFL owing to its maturity in technology, especially as an interface for RE. Therefore, it is evident that the power system's composition will consist of GFL and GFC and will coexist with SG. Thus the stability impact of substantial integration of GFL and GFC on power system stability must be well understood and is the key motivation for this project. The research gaps identified from the extensive literature review, are discussed in the following subsection. A detailed literature review is given in the subsequent chapters.

1.2.1 Stability Analysis of Power Converter Control

As discussed, the grid following control at considerable penetration level is a barrier in ensuring the stable operation of power system [29]. There has been considerable past research on extending the stable operating range of GFL. Most studies have pointed out that poor PLL design is a key contributor to the instability instigated due to GFL [46–49]. These studies suggest that potential instability caused due to PLL can be identified from the converter dynamic impedance, which manifests a negative incremental resistance behavior due to PLL. To that end, Ref. [50, 51] have suggested design guidelines for PLL of GFL and other control blocks to ensure a passivity behavior of converter impedances. Furthermore, the GFL interaction with an SG is studied in [52, 53] which also presents the influence of the VSC controller on stability and potential interactions with SG. However, interrelations between the control design guidelines for all the control blocks in a GFL, operating together with an SG are not well studied. Finally, as explained in the previous section, GFL has cascaded loops with outer and inner loops. The outer loops can saturate for extreme operating conditions, leading to mode change in GFL from power voltage control to a current-controlled converter. An analysis of the impact of such mode change on the system stability is also missing in the literature.

The stability challenges and slow response of GFL to grid events have raised significant interest in research on GFC's in recent years [26, 28, 29]. GFC was also the focus of some of the large European projects such as PROMOTioN and MIGRATE. A large number of studies focus on the different realizations of the electromechanical model, which also serves as the synchronizing block [54–57]. However, there has been limited assessment on the impact of inner loops on the grid forming behavior. It is not clear from the literature if the inner loops could lead to instability or corrupt the expected instantaneous response from the GFC. In addition, the interaction between the GFC and SG is also missing in the literature.

1.2.2 Transient Dynamics of Synchronization Control of Power Converters

Synchronization of GFL, realized by PLL, which measures the grid voltage phase, is key to ensuring the expected accurate operation of GFL. Several advanced PLL structures exist, enabling the GFL structure to be synchronized under distorted grid conditions [58]. In addition, there are also filtering stages, such as antialiasing filters placed before the PLL synchronization stage. However, the models of PLL existing prior to this work cannot accurately capture the phase of input voltage when there are large voltage magnitude disturbances, as in the case during grid faults. Furthermore, the performance of PLL during significant voltage transients needs improvement to ensure the GFL response as expected.

In contrast to GFL, synchronization of GFC utilizes measured active power as feedback. When the current limit is triggered due to an external transient event, the output power becomes unresponsive to power-based synchronization. Such a scenario presents unique transient stability challenges for GFC, particularly in low inertia systems with a high rate of change of frequency (RoCoF) and significant phase jumps. Recently many researches have explored the transient stability of GFC with and without current limit [59–62]. However, most of these studies have derived analogies from the transient stability of an SG during a power system fault and accompanied voltage dip case. However, the GFC based on power converter has different characteristics and limiters when compared to SG. Therefore, it is imperative to assess the GFC performance during all the transient event scenarios such as high RoCoF, phase jumps, and large voltage dip in a current limited operation.

1.2.3 Objective

The project objectives are

- Analysis of GFL and GFC to systematically investigate the stability of GFL and GFC coexisting with an SG and to derive design guidelines to mitigate instability.
- Study the impact of the current saturation of the GFL on system stability.
- Study the stability impact of inner loops in the GFC.
- Evaluate the transient performance of PLL, the synchronization unit of GFL and to develop accurate models and controls to augment PLL performance.
- Evaluate the transient performance of GFC when the GFC enters current limited operation and to propose control methods to improve the GFC synchronization
- Develop a PHIL platform for high fidelity validation of the power converter controls developed as a part of the Phoenix project.

1.3 Summary of Contribution

The main contribution of this thesis are

- A detailed analysis of the impact of the current limit in GFC on the GFC's ability to maintain transient stability is conducted. The various transients in a low inertia power system that can result in a loss of synchronism (LOS) of a GFC with a current limit are quantitatively analyzed. A novel solution based on virtual active power is proposed to improve the synchronization stability margin of the GFC with a current limit.

- It is revealed that a conventional SISO model of the PLL cannot capture the full dynamics when subjected to a significant transient in the terminal voltage magnitude and phase when a filtering stage is present before the control loop. Therefore, a generalized MIMO linear model of a PLL with a prefilter is proposed to overcome this deficiency. In addition, a compensation method is also proposed to improve the phase tracking of the performance of the PLL during transients.

- The impact of the inner loops on the stability of the GFC is analyzed in detail. The inner loops effect on the ability of GFC to behave like a voltage source behind an impedance is assessed using eigenvalue and impedance-based methods. The studies were conducted on an essential two-machine system composed of GFC and an SG with AVR. The stability analysis revealed that the inner loops in a GFC could potentially destabilize the system when the grid strength is low. In addition, it is revealed that the GFC inner loop can adversely affect the electromechanical mode of the SG.

- The stability impact of GFL on an essential two-machine system composed of SG and GFL is studied in detail using eigenvalue and impedance-based analysis. The analysis control design guidelines for all the control blocks in a GFL that can extend the small-signal stability of GFL are presented. It is revealed that when GFL outer power and voltage are saturated, additional stability challenges arise for GFL. The additional stability challenges due to current limit saturation are explained by impedance-based analysis.

- Developed an power hardware in the loop platform for high fidelity validation of power converter control methods proposed in this project. In addition, the stability margin of the PHIL simulation of the current controlled VSC is analyzed and methods to improve the stability margin is discussed.

- A full linear model of the essential system composed of SG system with AVR and governer and GFC is derived and is verified using time domain simulation. Similarly, the complete linear model of the system composed of SG and GFL is also derived.

- Developed a realtime simulation model low inertia IEEE 9 bus system by replacing 2 synchronous generators with GFL. The developed simulation model was used for evaluating the transient stability performance of hardware GFC interfaced to realtime simulation by PHIL

- A comparison between the single channel impedance-based stability analysis for GFL and an Eigen value-based analysis which is a more helpful tool in identifying and mitigating the origin of the problems is presented.

1.4 Approach and methodology

The following is the overview of the methodology followed to achieve the objectives of this Ph.D. project.

- **Literature review**

  An extensive literature is available on GFL and GFC, with several projects and publications addressing the challenges faced by the power grid due to the massive integration of power electronics. The literature review conducted during the Ph.D. period enabled identifying the

research gaps in the power converter-based stability in power systems. Also, the lessons learned in the previous research have enabled in better understanding of challenges and optimum methods in analyzing and understanding the unresolved problems. Further details of the conducted literature review are present in each of the chapters.

- **Modelling and simulation**

  Upon finding the research gaps, a hypothesis was formulated, followed by a basic theoretical analysis. Then, detailed analysis and preliminary validation of the assessment and proposed solution are conducted using small-signal analysis (when required) and time-domain simulations. More details on the modeling simulation and small-signal analysis used in this research are given in the methodology chapter.

- **Power Hardware in the Loop**

  Power Hardware in the Loop simulation is conducted for a high fidelity validation of the proposed solutions to augment the power converter control

1.5 Thesis outline

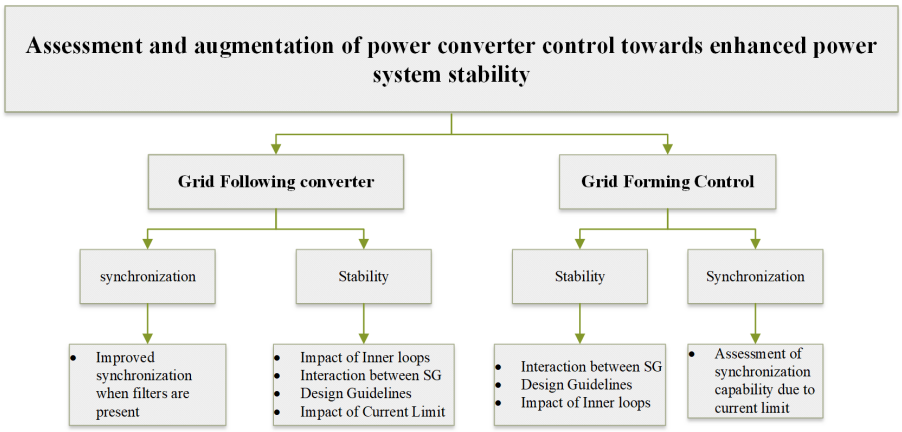

Figure 1.8: Thesis structure

A summary of the thesis structure is given in Fig. 1.8

In chapter 2, the methodology used for this research is detailed. The stability range of power hardware in the loop simulation of current controlled converter is derived analytically. In addition, the methods to improve the PHIL simulation of power converter is discussed.

In chapter 3, a comprehensive evaluation of GFL impact on system stability is conducted based on an essential system model composed of SG. The small-signal stability impact of series and parallel-connected GFL on the rest of the network using an intuitive impedance-based approach is presented. Control design guidelines to improve the stability of the GFL is also presented in this chapter.

In chapter 4, proposed an improved PLL modeling with the advanced filter that captures the complete PLL dynamics during symmetrical faults for a PLL equipped with any prefilter. The proposed model captures this undesirable coupling between the magnitude and phase of the input voltage. A compensation method that improves the PLL tracking performance during symmetrical

faults is also proposed. The PHIL validation of the proposed control is also presented in this chapter.

In chapter 4, Comprehensive analysis of different controls and impact of inner loops of GFC realization and its impact on system stability derived based on an essential system model composed of SG are presented. The small-signal, time domain and impedance analyses are conducted to compare the time domain and stability performance.

In chapter 5, The impact of the current limit on the transient stability of the system with GFC is assessed for multiple transient events, including phase jump and frequency change events, and voltage dip events are demonstrated analytically and illustratively. Furthermore, the methods that can be implemented in the GFC to ride through such transient events are discussed. Finally, a coordinated overload and current limit for grid forming converter employing virtual power, extending the transient stability margin for all the grid events, is proposed. PHIL study validation of the proposed method is also presented in this chapter

Chapter 6 A discussion on the possible future work and summary of the PhD work is given.

1.6 Limitations

- The assessment of converter controls for stability has been conducted based on an essential system model consisting of an SG and GFL/GFC. The analysis was limited to two machine systems to comprehensively analyze stability and derive conclusions intuitively. The study assumes that the conclusions drawn from the assessment of such a system are scalable to an extensive system with multiple components. Further investigation with a comprehensive system study is still needed.
- In practice, loads in the power system loads have different static and dynamic characteristics. The power converter-based loads such a motor drives and battery chargers introduce different dynamics to the power system loads and impact system stability. In this study, for the sake of brevity, the loads are considered only impedance type loads.
- The DC link dynamics and back end machine or converter dynamics, if any, are neglected. This is to simplify the complexity of the modeling and analysis.
- In this project, the term grid forming converter and grid following converters use a commonly used control architecture. In literature, there are several variations to the control architecture of GFL and GFC, and considering all the variations are beyond the scope of the project.

1.7 List of Publications

[Pub. A] Kanakesh Vatta Kkuni , Guangya Yang, Qiteng Hong, and Campbell Booth. "Improved MIMO modelling and enhanced transient performance of phase locked loop during grid fault." IEEE Transactions on Industrial Electronics (2021), doi: 10.1109/TIE.2021.3073307.

[Pub. B] Kanakesh Vatta Kkuni, and Guangya Yang. "Effects of current limit for grid forming converters on transient stability: analysis and solution." arXiv preprint, arXiv:2106.13555 (2021), *To be submitted*

[Pub. C] Kanakesh Vatta Kkuni, Sibin Mohan, Guangya Yang, and Wilsun Xu. "Comparative assessment of typical controlrealizations of grid forming converters based ontheir voltage source behaviour." arXiv preprint arXiv:2106.10048 (2021), *Submitted to Renewable and Sustainable Energy Reviews, under review*

[Pub. D] Kanakesh Vatta Kkuni, Mirza Nuhic and Guangya Yang. "Power System Stability Impact Assessment for the Current Limits of Grid Supporting Voltage-Source Converters." 2021 IEEE Power & Energy Society General Meeting

[Pub. E] Kanakesh Vatta Kkuni, Sujay Ghosh, Guangya Yang, and Campbell Booth. "Modelling and Passivity Analysis of VSC Output Impedance under SRF and $\alpha\beta$ Control Frames." *In IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, pp. 1856-1861. IEEE, 2019.

In addition, the following reports are also submitted as deliverable to the Phoenix project.

[Pub. F] Kanakesh Vatta Kkuni and Guangya Yang,. "Report on co-simulation for faster prototyping for new designs and controls." Phoenix project deliverable report, December 2020

[Pub. G] Kanakesh Vatta Kkuni and Guangya Yang "Co-simulation for faster prototyping for new designs and controls," Phoenix project deliverable report, November 2018

The following publications have also been prepared during the course of the Ph.D. study, but have been omitted from the thesis because they are not directly related to the primary objective,

[Pub. H] Sujay Ghosh, Kanakesh Vatta Kkuni, Guangya Yang, and Lukasz Kocewiak. "Impedance scan and characterization of Type 4 wind power plants through aggregated model." *In IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, pp. 1799-1804. IEEE, 2019.

[Pub. I] Mirza Nuhic, Kanakesh Vatta Kkuni, Guangya Yang and Jay Ramachandran, "Comparative study of hybrid synchronous condenser incorporating battery energy storage system for ancillary service provision," in Wind Integration Workshop, 2020.

CHAPTER 2

Methodology

The methodology chapter discusses the modeling and analysis employed in this thesis. First, the modeling approaches for the simulation and small-signal modeling of the components are discussed. Second, an approach to develop the full linearized system model based on the component interconnection of power and control component linear model is discussed. The approach for developing the small signal model followed in this thesis is scalable and has been in existence for developing the models of large dynamical systems composed of interconnected dynamic systems.

An overview of the analysis employed in this thesis is shown in Fig. 2.1. To begin with the analysis, steady-state analysis of the system is conducted using the load flow program. The steady-state values of the internal states of power and control components are then computed using the results from load flow. These steady-state values of the states are then used for initializing the simulation and small-signal analysis. Both impedance-based evaluation and Eigen value-based evaluation are employed to study the power converter-based system's small-signal stability. Both analysis methods has diverse pros and cons in the stability evaluation of power converter dominated power system, which will be discussed later in this chapter. The Impedance analysis subsection (Subsection 2.2.1) in this chapter is based on the content described in [**Pub. C**] and [**Pub. D**].

Finally, power hardware in the loop platform with a hardware VSC and power system simulated in real-time is employed to validate the proposed solutions to augment the control of power converters. An analysis of the key parameters and quantities that impact the stability range of power hardware in the loop simulation of the current-controlled converter is also presented in this chapter.

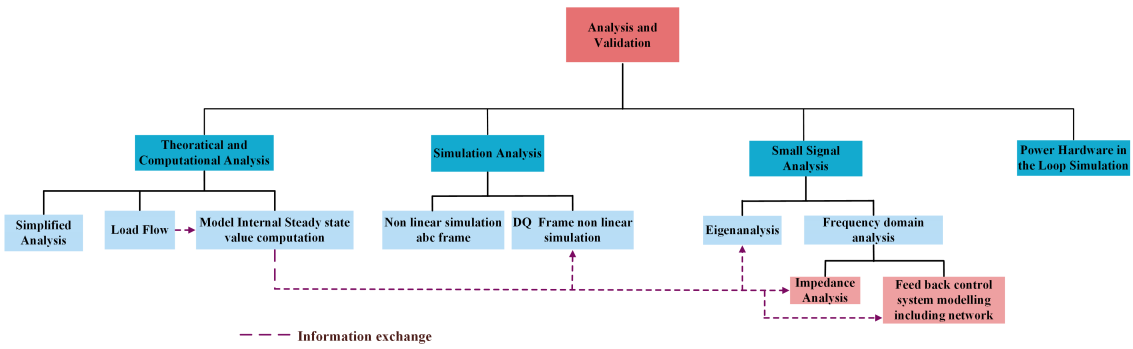

Figure 2.1: Overview of analysis and validation methods

2.1 Modelling

The modelling of the studied system is based on developing individual models of components such as power converters, synchronous generators and then interconnecting these components

to scale up to large power system. The modelling is primarily done in MATLAB/Simulink. The control system toolbox of the MATLAB/Simulink is extensively used for control design and small signal analysis.

2.1.1 Steady state model

Load flow calculation is used to determine the system states such as voltage, line flows, and active and reactive power generation for given operating conditions. Once the voltage,injected active and reactive power of the bus to which the power component is connected is calculated by load flow, the steady-state values of each internal states in the components can be back-calculated. These values are then used to initialize the states of nonlinear simulation models to eliminate the startup transients in time domain nonlinear simulations. Furthermore, steady-state values of the states are also needed in the small-signal models.

2.1.2 Nonlinear time domain Simulation model

The nonlinear time-domain model of each component is developed in MATLAB/Simulink. Typically nonlinear simulations considering the electromagnetic transient dynamics are realized in a stationary reference frame. However, such time-domain simulations have an ac form for the voltage and current, and thus there is no DC steady-state value. Hence it is challenging to ensure the system simulation start with state variables initialized to a steady-state. Furthermore, since the voltage and current have ac steady-state, it is also impossible to utilize the control system toolbox functionalities of MATLAB in deriving the small-signal model and tuning the control parameters. In this regard, each of the nonlinear models implemented in the stationary reference frame is modeled in a rotating reference frame. For this, the differential equation of the components are first converted to a rotating reference frame defined by the well-known Clarke and Park transformation [33], and the differential equations in the rotating frame are then implemented in a Simulink environment.

Clarke (abc to $\alpha\beta$) and park ($\alpha\beta$ to dq) transformation matrices used in this thesis are given by

$$[T_{\alpha\beta}] = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.1}$$

$$[T_{dq}] = \begin{bmatrix} \cos(\theta_f(t)) & \sin(\theta_f(t)) \\ -\sin(\theta_f(t)) & \cos(\theta_f(t)) \end{bmatrix} \tag{2.2}$$

Where θ_f is the angle between the stationary and rotating reference frames. The relation ship between the variables in rotating reference frame (x^{dq}) and the original variable in stationary frame (x^{abc}) are given by

$$x^{dq} = [T_{dq}][T_{\alpha\beta}]x^{abc} = [T_{vsc}]x^{abc} \tag{2.3}$$

Simillar to an SG, wherein the modeling is conventionally conducted in a rotating reference frame aligned with the rotor angle, rotating frame modeling of voltage source converter is convenient if defined in a frame aligned with synchronizing unit output (dq frame). The model of the network and the rest of the system is defined in the reference frame aligned with the system's fundamental frequency (DQ frame). In steady-state, both the reference frames rotate at the same speed.

Hereafter, all variables with a D or Q subscript or superscript denote direct and quadrature components of the system signals or state represented in DQ frame. Likewise, all variables with a d or q subscript or superscript denote direct and quadrature components of the system signals or state represented in dq frame. In addition, subscripts with appended 0 represent the steady-state value of the system signals or state. Phasor diagram of relation between the quantity x represented in stationary reference frame (abc), System rotating reference frame (DQ) and components rotating reference frame (dq) is shown in Fig. 2.2.

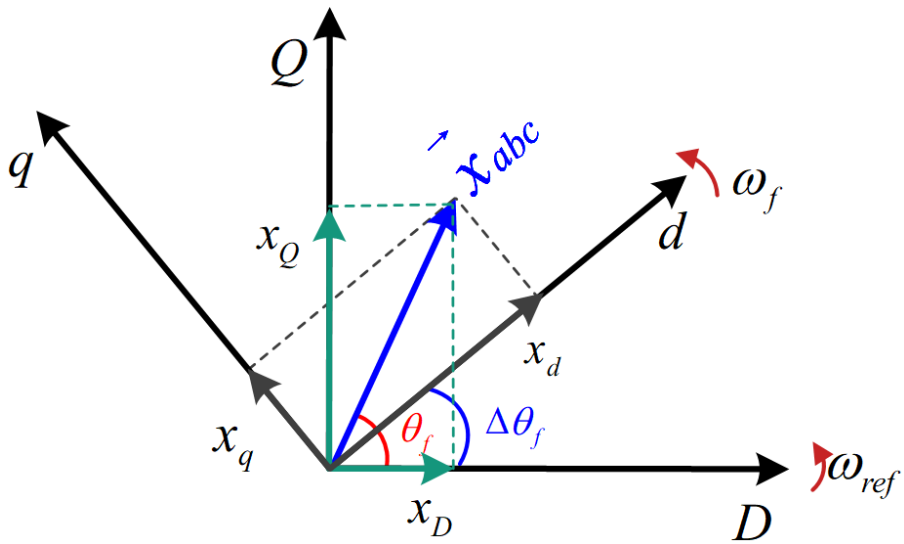

Figure 2.2: Phasor diagram of relation between the quantity x represented in stationary reference frame (abc), System rotating reference frame (DQ) and components rotating reference frame (dq)

There are several advantages for DQ simulation models over simulation models implemented in stationary frames, they are

- Able to link the with load flow program and the state steady-state value computation program so the simulation can be initialized to the steady state for any operating conditions
- Can use the Simulink model linearizer to derive an accurate small-signal model, which also serves as a validation for analytically derived models
- A vectorized simulation, where each parameter is a vector, can be performed. This functionality is useful in sensitivity analysis and scaling up the simulations when there are multiple parallel converters as in the case of a wind farm

However, it has to be noted that the zero sequence components are ignored in the DQ simulation model.

2.1.3 Small signal modelling

After the DQ nonlinear model of a component is developed, the analytical linearized model is derived. The differential equations defining the component are written and linearized to arrive at the small-signal model. The steady-state values required in formulating the linear model are derived from the load flow and steady-state analysis of the component model.

For components such as VSC, wherein the model comprises several control blocks and the physical system, each of the control and physical systems are interconnected based on the corresponding input and output to derive the full interconnected VSC dynamical system. The small-signal modeling of the VSC is shown in Fig. 2.3, the linear modes of the VSC control blocks and transformation matrices ($G_p(s), G_c(s), G_Q(s), G_(PLL)(s)$,$Mv2, Mi1$) are interconnected with the physical system to form the full dynamical model. MATLAB control system toolbox [63] is extensively used in this approach. It is possible to combine different model types such as transfer function or state-space model with this approach, while model transformation is handled internally by the MATLAB toolbox.

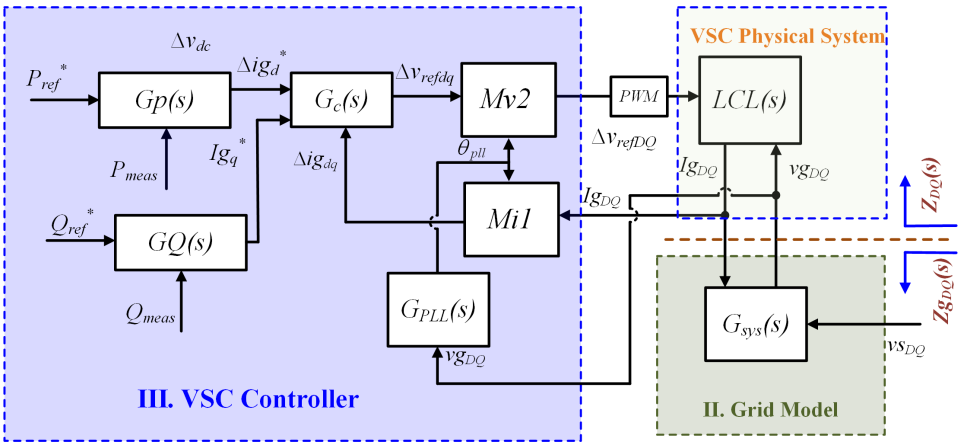

Figure 2.3: Overview of small signal modelling of VSC system by interconnecting the dynamical systems

Similarly, the component model interconnecting approach is used to derive the full system model composed of multiple components. A full state-space model can be extracted for eigenvalue and sensitivity analysis from the final interconnected model. An impedance model of the components and system, including the grid equivalent impedance calculated at any bus, is the appropriate open-loop transfer function between the voltage and currents. A full overview of the modelling approach is given in Fig. 2.4

Finally, the modeling approach allows incorporating the VSC physical system and the AC network model in a feedback loop which is ideal for VSC controller design [26] and [64] as shown in Fig. 2.5. Such an approach allows the design of VSC controllers while accounting for the full system dynamics.

The dynamic impedance of the VSC and the grid equivalent can be found from all the three models. For non linear models, the impedance can be measured by perturbing the voltage or current at the terminals of the developed model and measuring the current or voltage to construct the frequency response model which in this case is the dynamic impedance. For linearized small signal models the dynamic impedance is the transfer function between the terminal voltage and current of the component.

2.2 Analysis

2.2.1 Impedance Analysis

Impedance-based stability is evaluation is one of the small-signal stability evaluation methods for a power converter-based system. The stability of the converter grid can be evaluated at the

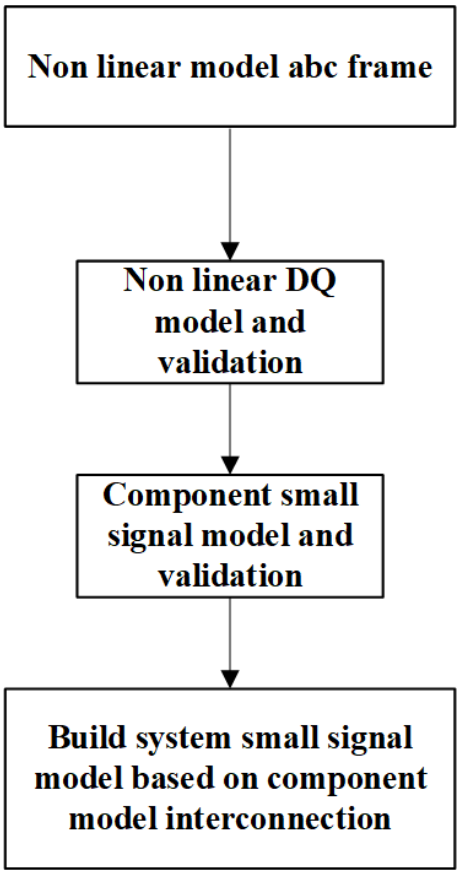

Figure 2.4: Overview of modelling methods

Figure 2.5: Feedback control system modelling for control design

interface bus by applying the Nyquist stability criterion on the ratio of thevenin grid impedance seen from the connection point, and converter impedances [65, 66]. The impedance-based stability can also be applied for black-box models, as the dynamic impedance can be constructed from measurements.

Background

Consider the small signal representation of a VSC connected to the network as shown in Fig. 2.6. The impedance $Z_{dut}(s)$ represent the impedance of the power converter and $Z_{ths}(s)$ the impedance of the thevenin network. Both the impedances are considered to be stable when taken individually. The Feedback loop representation of the system is shown in Fig. 2.7. A closed loop transfer function form of the feedback loop representation of the system can be written as

$$H(s) = \frac{Z_{th}(s)}{Z_{dut}(s)} \frac{1}{1 + \frac{Z_{th}(s)}{Z_{dut}(s)}} \tag{2.4}$$

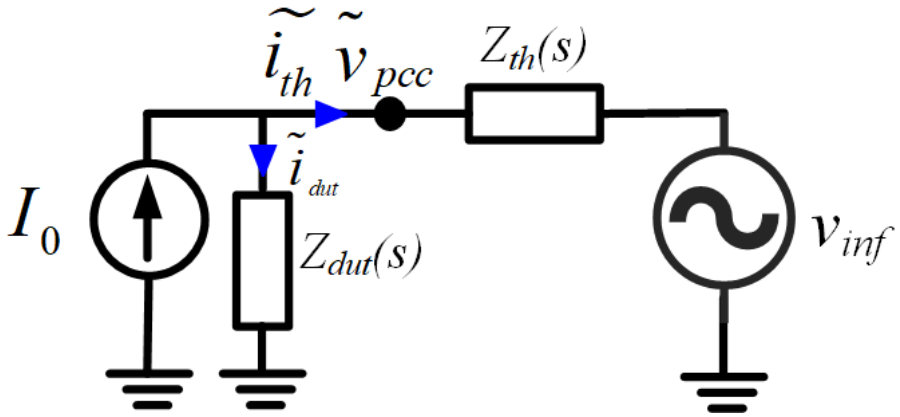

Figure 2.6: Small signal representation of the VSC connected to the network

Now, from linear control theory [67], the closed loop transfer function in (2.4) is stable if the ratio of grid and converter impedance ($\frac{Z_{th}(s)}{Z_{dut}(s)}$) satisfies the Nyquist stability criterion.

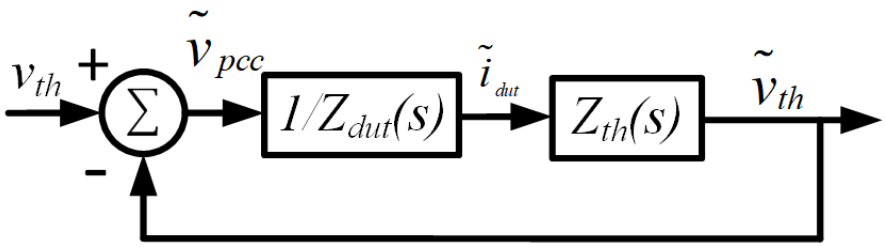

Figure 2.7: Feedback loop equivalent of the VSC system under consideration.

Impedance stability of three phase system

The impedance stability analysis was derived in the previous subsection by considering the impedance in a Single-Input and Single-Output (SISO) form. SISO impedance assumption is valid in DC system and single phase ac systems. The impedance of a three-phase system is instead a Multiple-Input and Multiple-Output (MIMO) transfer function; hence the impedance stability analysis needs to account for MIMO form. The impedance stability of the three-phase systems is discussed in this subsection.

The thesis is limited to studying the stability of three phase balanced system. In addition, the zero-sequence components are not considered in the studies. Thus the impedance of the three-phase ac converter can be expressed as 2X2 matrices in DQ domain, as shown in (2.5). The voltage source converter is a voltage input current output dynamic system. With the Point of Common Coupling (PCC) voltage being the input and VSC injected current is the output. Therefore, is dynamic impedance in DQ domain for a VSC is the inverse of the input-output transfer function of the derived linearized analytical model.

$$[Z_{DQ}(s)] = \begin{bmatrix} Z_{DD}(s) & Z_{DQ}(s) \\ Z_{QD}(s) & Z_{QQ}(s) \end{bmatrix} \tag{2.5}$$

If $[Z_{vscDQ}]$ is the impedance of the VSC and $[Z_{netDQ}]$ is the impedance transfer function matrices of the network seen at the PCC bus, the open loop gain of the overall system is given by

$$L_{DQ}(s) = [Z_{vscDQ}]^{-1} * [Z_{netDQ}] \tag{2.6}$$

The stability of the overall system for MIMO open loop gain can be evaluated by the Generalized Nyquist theorem which states "Let Pol denote the number of openloop unstable poles in L(s). The closed-loop system with loop transfer function L(s) and negative feedback is stable if and only if the Nyquist plot of determinant of (I + L(s)) [68]

1. makes Pol anti-clockwise encirclement's of the origin, and
2. does not pass through the origin."

Such an approach is excellent for analyzing the stability of black-box model of the VSC system provided by the manufacturer for stability analysis. The frequencies at which the stability margins are low corresponds well with underdamped oscillation mode frequency and thus could be used to study potential instability in the power system.

When the grid and VSC impedances are a SISO system, it is intuitive to identify the resonant point in the system that would correspond to the intersection of the VSC and grid impedances magnitude [66]. In addition, by measuring the phase difference between the impedances at the resonant point, it is also possible to assess the phase margin of the full system. However, such an intuitive approach is not feasible with MIMO impedances, and one would need to use the Nyquist plot of det(I + L(s)), which is not as intuitive as assessing the SISO impedances. In addition, using the full impedance matrix conceals some design guidelines that are visible from studying single channel impedance. However, an indicative stability assessment of MIMO impedance can be derived by only considering a single channel of the DQ impedance of both grid and VSC, so SISO based analysis can be applied. Nevertheless, it should be noted that a single-channel impedance-based analysis is indicative and might lead to wrong conclusions.

One of the main challenges in DQ impedance analysis is that the impedances are highly coupled, i.e., the off-diagonal elements of the impedance matrix shown in 2.5 is significant when compared to the diagonal elements [69]. The coupling is high even for a passive impedance such as a resistive, inductive impedance. Thus an intuitive SISO impedance approach looking at the intersection point of the impedances of the network and VSC can lead to wrong stability conclusions. In this regard, an impedance analysis in a modified positive-negative (pn) sequence frame is proposed in [69]. A modified pn frame impedance can be obtained by transforming the DQ domain impedance into a modified positive-negative sequence domain. The pn domain impedance equations are shown in Eqs. (2.7-2.8). One advantage of pn domain analysis is that typically the pn domain impedances are diagonally dominant. Therefore, impedance analysis can be approximated as two decoupled SISO systems, providing intuitive and interpretable means to assess the stability.

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = \underbrace{\begin{bmatrix} Z_{pp}(s) & Z_{pn}(s) \\ Z_{np}(s) & Z_{nn}(s) \end{bmatrix}}_{[Z_{pn}]_{2X2}} \begin{bmatrix} I_p \\ I_n \end{bmatrix} \tag{2.7}$$

Where V_p and V_n are positive sequence and negative sequence phasors at $\omega_{dq} + \omega_{ref}$ and $\omega_{dq} - \omega_{ref}$, respectively. The Z_{pn} can be represented by a linear combination of Z_{dq} and is given as:

$$[Z_{pn}]_{2X2} = [A_Z] \cdot [Z_{DQ}(s)] \cdot [A_Z]^{-1}$$
$$[A_Z] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ 1 & -j \end{bmatrix} \tag{2.8}$$

If the impedance are symmetric in nature, ie $Z_{DD}(s) = Z_{QQ}(s)$ and $Z_{DQ}(s) = -Z_{QD}(s)$, then the modified sequence domain impedance is completely diagonal with $Z_{pp}(s) = Z_{nn}(s) = Z_{DD}(s) + jZ_{QD}(s)$ and $Z_{pn}(s) = Z_{np}(s) = 0$. The impedance of passive elements is symmetrical in a balanced condition. Hence one can utilize the intuitive stability analysis with a single-channel approach using modified sequence domain much more accurately than the DQ domain impedances. However, it should be noted that analysis on only $Z_{pp}(s)$ channel still gives an indicative assessment of stability. This is because the impedances of the VSC and other active sources are not passive and can have off diagonal elements in 2.7. For active components such as VSC and SG, existense of off diagonal elements are high in low frequency range.

The sequence domain impedance, commonly used in converter-based system stability in the stationary frame, can be calculated by shifting the modified sequence domain impedance transfer function matrices. The impedance stability analysis based on DQ impedance, modified sequence domain, and sequence domain all can accurately capture the instability if the full MIMO analysis is applied. Moreover, all the impedances defined by indifference frames are interrelated by transformation and frequency shifting. However, for the sake of convenience and due to high similarity with DQ models compatible for eigenanalysis, a modified sequence domain impedance is utilized in this thesis for impedance assessment. In the rest of the thesis, the term dynamic impedance is used for $Z_{pp}(s)$.

Passivity of Impedance

The Passivity Theorem could be applied to analyze the VSC input impedance behavior [50, 70] and understand potential instability. A passive system can only dissipate the energy and cannot produce energy, thus an interconnected network composed of passive impedances, such as RLC network are passive and will never be unstable. In the frequency domain, the dynamic impedance is passive if,

$$Z_{pn}(j\omega) + Z_{pn}^{H}(j\omega) > 0, \forall \omega \in R \tag{2.9}$$

Where H is the Hermitian operator. The left hand side of (2.9) can be equated to

$$Z_{pn}(j\omega) + Z_{pn}^{H}(j\omega) = \begin{bmatrix} A & C^* \\ C & B \end{bmatrix} \tag{2.10}$$

Where,

$$A = 2\mathrm{Re}\{Z_{pp}(j\omega)\}, B = 2\mathrm{Re}\{Z_{nn}(j\omega)\}$$
$$CC^* = (Z_{pn}^*(j\omega) + Z_{np}(j\omega))(Z_{np}^*(j\omega) + Z_{pn}(j\omega)) \tag{2.11}$$

To check if the impedance is dissipative or passive, a simple positivity check could be done.

$$A > 0, B > 0, AB > CC^* \tag{2.12}$$

The modified sequence domain impedance is diagonally dominant, and hence the passivity could be verified simply by ensuring a positive real part of $Z_{pp}(jw)$ for all frequencies. We can improve the interconnection stability of a VSC by ensuring that VSC input impedances is passive, especially in the frequencies nearby critical grid resonances [50].

Suppose the VSC impedance and grid impedance interaction occurs in a range of frequencies where the VSC impedance has a nonnegative impedance real part, then it is more likely that the overall system can remain stable. However, ensuring the passivity in the critical frequency range is not straightforward because VSC consists of several control loops and physical filters and delays, and careful consideration of all of these must be designed to ensure a passive impedance in a critical range. Moreover, measures taken to create a passive impedance should not compromise the transient performance of the VSC's and time domain requirements.

2.2.2 Eigen value analysis

The eigenvalue analysis has been used in stability evaluation for decades and has been extensively used in stability analysis of conventional power systems [33]. The eigenvalues are obtained from the state-space matrices of the system. However, compared to impedance-based analysis, which can also be applied to black-box models from the manufacturers, the eigenvalue approach needs the information of the full system model. Thus, complexity-wise, the impedance-based approach is simple, and the passivity of the impedance can provide information on potential instability only by study the component impedance. On the other hand, impedance method may fail to capture the stability since it is a local method applied at one bus, but eigenvalue analysis always predicts stability accurately. Identifying the origin of the potential instability by utilizing participation factors is another additional advantage the eigen analysis has over the impedance analysis. In the analysis part of this, both eigen value and impedance analysis is utilized owing to their diverse advantages.

2.3 Power Hardware-In-the-Loop Validation

The validation of PE converter-based devices deployed in the power system is challenging. A high degree of accuracy and reliability is expected of the components integrated into the power system. The advent of newer technologies, primarily based on power electronic converters, necessitates novel testing procedures with reduced development times and higher fidelity. In this regard, the Power Hardware-in-the-Loop (PHIL) testing has gained a lot of interest in recent times [71–75]. PHIL testing blends the flexibility, scalability, and the ability to model an extensive system of numerical simulation which permits closer to reality scenario for Hardware Under Test (HUT).

The power hardware in the loop platform was developed in this Ph.D. project to validate the developed control methods for power electronic converter at high fidelity. The proposed control methodologies and analysis of the low-level control and the grid support functionalities by VSC presented in this paper are validated using the developed PHIL platform. The PHIL interfaces a realtime simulated model of the system with actual hardware component under test. Several of the past literature has studied the stability range of different PHIL interface algorithms by considering passive impedance for both simulated and hardware system [71, 72]. An analysis on the stability range of PHIL simulation for current controlled VSC is missing in literature. In this section the PHIL stability of current controlled VSC is presented and the key findings are discussed in this section.

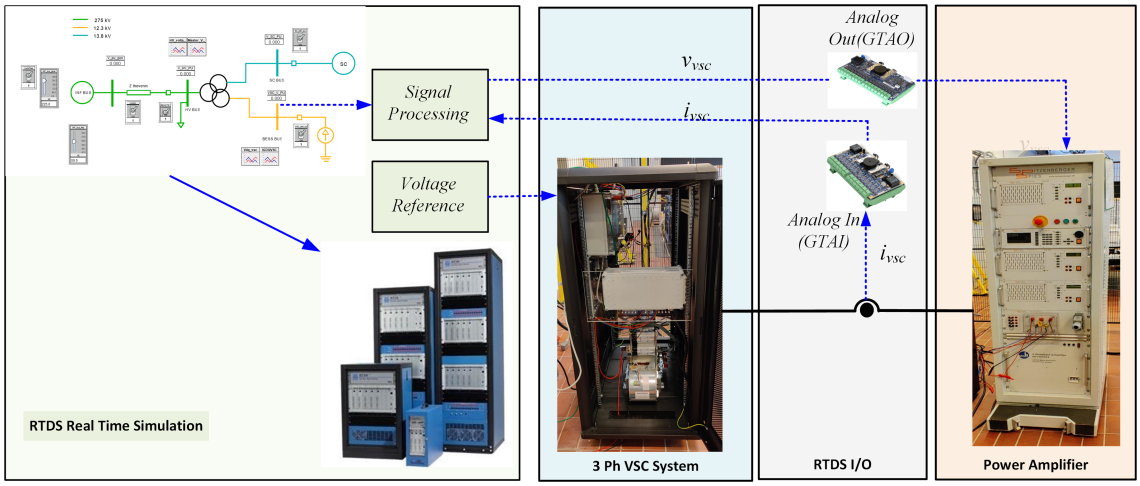

Figure 2.8: Overview of developed PHIL system structure. Adapted from [**Pub. G**]

Figure 2.9: Lab hardware setup

The overview of the PHIL setup developed in the DTU is as shown in Fig. 2.8. The system's hardware components consist of the Real Time Digital Simulator (RTDS), I/O cards to the RTDS, SPITZENBERGER SPIES PAS 2500 linear amplifier, and a SEMIKRON SkiiP based voltage converter platform connected to a DC source. The power system model is simulated in realtime in RTDS, the voltage of the bus to which the voltage source converter is to be connected is scaled and given as an input to the linear power amplifier by using RTDS Gigabit Transceiver Analogue Output Card (GTAO)cards, and the current coming into the amplifier from the hardware VSC is measured, scaled, send to RTDS using GIGA-TRANSCEIVER ANALOGUE INPUT CARD (GTAI) cards and injected to PCC bus in the real-time simulation as the current source. This current-voltage exchange ensures that the hardware VSC is part of the power system network simulated in RTDS,

thus ensuring a platform to validate the analysis and control performed on VSC in a power system network. The lab hardware setup in shown in Fig. 2.9.

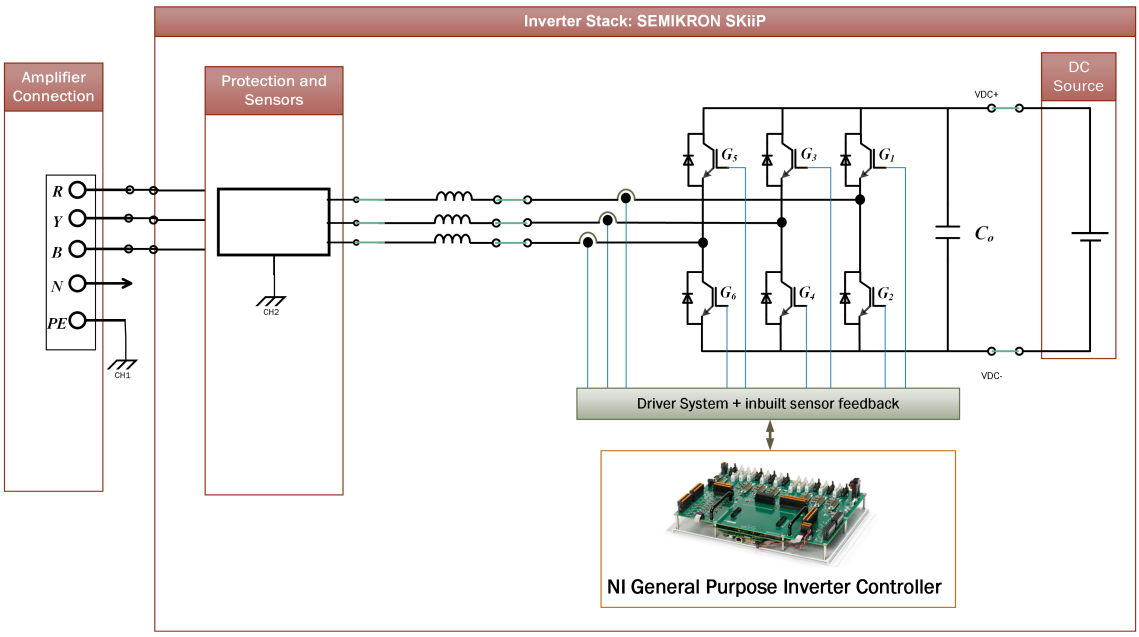

Figure 2.10: Three-phase VSC Converter Layout, Adapted from [**Pub. F**]

The layout of the three-phase VSC system is shown in Fig. 2.10. The core of VSC system is the SEMIKRON SkiiP stack which includes the Insulated-gate bipolar transistor (IGBT) and gate drivers. The VSC system placed in the cabinet also includes voltage and current sensors and filter reactors, precharge circuits, and contactors. FPGA based National Instruments (NI) General Purpose Inverter Controller (GPIC) with single board RIO-9607 is utilized to implement the converter controls.

A graphical user interface is developed for live data monitoring and capture of VSC variables such as voltage, current, and power of the VSC. The GUI also enables changing changing the control and operational parameters of the VSC without interfering with the low level program. The developed graphical user interface window for the GFC hardware is shown in Fig 2.11. The developed GUI is implemented in the realtime processor of the single board RIO , the GUI communicates with the low level control including the VSC control, sensing, and Pulse Width Modulation (PWM) implemented in the FPGA.

2.3.1 Interace Algorithm

The interface algorithm determines the signal interaction between the hardware device under test and the realtime simulation. Several interface algorithms are employed in literature, such as Transmission Line Method, Partial Circuit Duplication, Damping Impedance Method, and Ideal Transformer Method [72, 76]. The interface algorithm used in this project is Ideal Transformer Interface (ITM) dues to its low complexity and high accuracy. The overview of the ITM method is shown in Fig. 2.12. The impedances $Z_s(s)$ and $Z_H(s)$ represent the equivalent impedance of the network simulated in real time and the impedance of the hardware under test, respectively. As explained before, in ITM, the voltage-current exchange through the RTDS and amplifier I/O cards

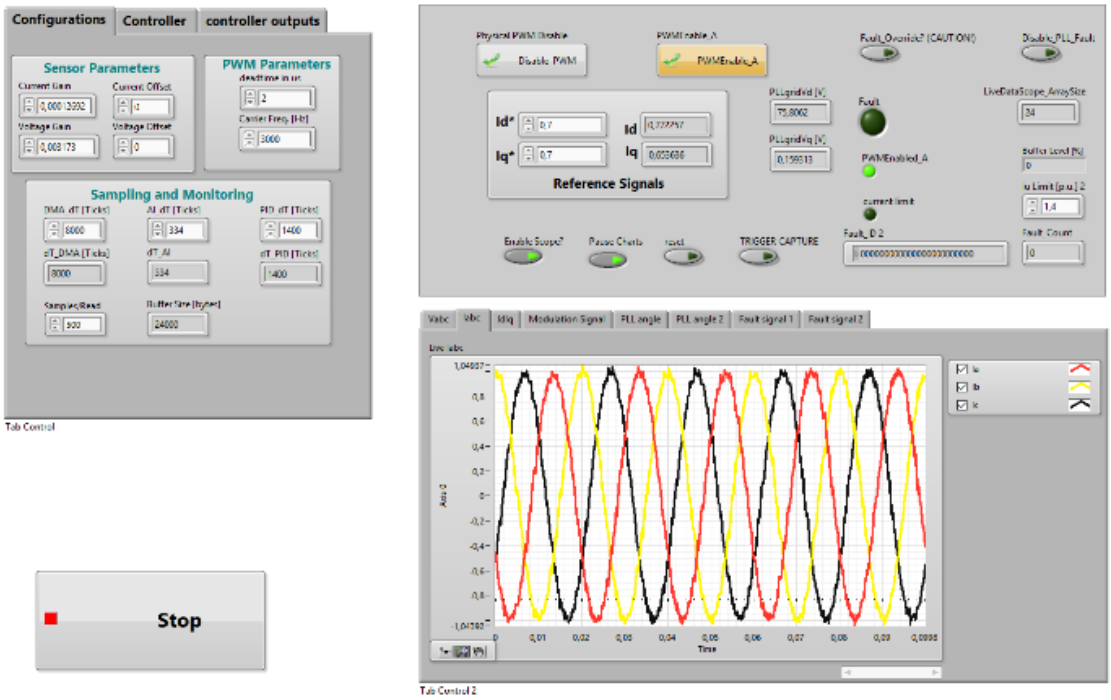

Figure 2.11: Developed LabVIEW user interface for the controller

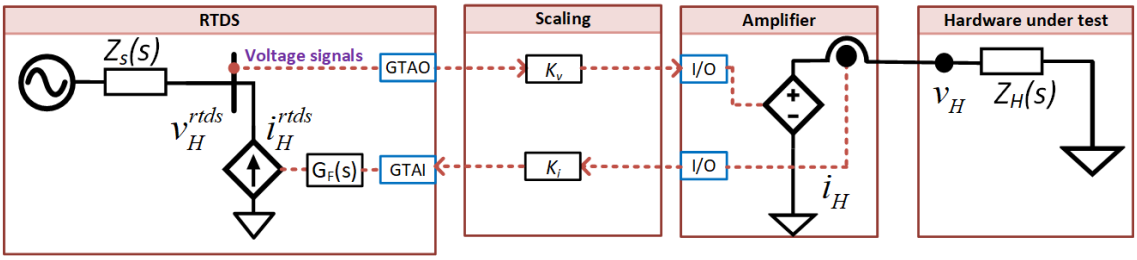

Figure 2.12: Ideal transformer interface algorithm

ensures that the current source connected in RTDS simulation emulates the hardware dynamics. In this section, the limitations and operational range of ITM interface algorithm when the hardware under test is a passive impedance are analyzed first. Then, the analysis is extended to include the VSC with current cotrol as the hardware under test.

Firstly, to simplify the understanding, the impact of scaling factors has to be considered, the voltage scaling factor (K_v) and the current scaling factor (K_i) are selected based on the rating of the hardware, i.e., if the hardware under test (HUT) is a scaled-down prototype of the original hardware for field testing, one must choose appropriate values of K_v and K_i such that the scaled-down version of the hardware is scaled up to actual rating in the real-time simulation environment. On the other hand, if the hardware is not a scaled-down prototype, the values of both K_v and K_i are chosen to be one. The relation between the voltages and current of the hardware measured at the hardware terminal(v_H, i_H) and the scaled voltages and current (v_H^{rtds}, i_H^{rtds}) at interface bus simulated in RTDS are given by

$$v_H^{rtds} = \frac{v_H}{K_v}, i_H^{rtds} = v_H * K_i \tag{2.13}$$

A generalized open loop transfer function of the ITM method negleting the dynamics of the amplifier, can be derived from Fig. 2.12 as

$$G_{ITM}^{ol} = \frac{Z_s(s)}{Z_H(s)} * G_F(s) * e^{(-s2T_d)} * K_v * K_i \tag{2.14}$$

Where, $G_F(s)$ is the signal processing filter implemented in RTDS, and $2 * T_d$ is the total time delay from both the forward and return path of the interface. The scaling factors can be eliminated in the analysis if the impedances are represented in the per unit form, then (2.14) is given by

$$G_{ITM}^{ol} = \frac{Z_s(s)^{pu}}{Z_H(s)^{pu}} * G_F(s) * e^{(-s2T_d)} \tag{2.15}$$

Where the $Z_s(s)^{pu}$ and $Z_H(s)^{pu}$ are the per unit impedance of the the equivalent impedance of the network simulated in realtime and the impedance of the hardware under test respectively. The relation between the base impedances of the network simulated in realtime (Z_base^{RTS}) and the base impedance of scaled hardware (Z_base^{H}) can be derived similar to calculating the base impedance of primary and secondary sides of a transformer and is given by

$$Z_{base}^{H} = Z_{base}^{RTS} * K_v * K_i \tag{2.16}$$

Finding out the stability range of PHIL based on ITM when both the $Z_s(s)^{pu}$ and $Z_H(s)^{pu}$ are passive impedance is recalled for a better understanding of the PHIL stability [71]. Firstly, consider the case that both the $Z_s(s)^{pu}$ and $Z_H(s)^{pu}$ are resistances and equal to $R_s(s)^{pu}$ and $R_H(s)^{pu}$ respectively. Simplified form of G_{ITM}^{ol} for resistive impedance can be obtained by neglecting the filter dynamics ($G_F(s) = 1$), and using first-order Padé approximation for the delay [67]

$$G_{ITM}^{ol} = \frac{R_s^{pu}}{R_H^{pu}} * \frac{1 - sT_d}{1 + sT_d} \tag{2.17}$$

One can apply the Routh–Hurwitz stability criterion on the open loop transfer function in (2.17) to find the condition for stability as

$$R_s^{pu} < R_H^{pu} \tag{2.18}$$

i.e, the stability condition is satisfied if the equivalent network resistance simulated in real time should be lower than the actual hardware resistance. The condition is independent of the delay term (T_d). If both the simulated and hardware impedance are in resistive inductive form, the stability condition is extended as

$$L_s^{pu} < L_H^{pu}, R_s^{pu} < R_H^{pu} + \frac{1}{Td}(L_s^{pu} + L_H^{pu}) \tag{2.19}$$

Where $L_s(s)^{pu}$ and $L_H(s)^{pu}$ are the inductance of the software and hardware impedance respectively. There are several methods discussed in the literature to increase the stable operating range[71, 72], the method used in this thesis to improve the stability margin of PHIL is to deploy a low pass filter ($G_F(s)$) on the feedback current. The feedback filter also eliminates the noise present in the converter current fed back to the real-time simulation. By utilizing a first-order low pass filter

on the feedback current and first-order Padé approximation of the delay, the open-loop transfer function of the ITM method can be rewritten as

$$G_{ITM}^{ol} = \frac{Z_s(s)^{pu}}{Z_H(s)^{pu}} * \frac{1 - sT_d}{1 + sT_d} * \frac{1}{1 + s * \tau_f} \tag{2.20}$$

where τ_f is the time constant of the first order feedback filter. With the use of first order low pass filter the stability condition for the resistive impedance case as in (2.18) is modified to

$$R_s^{pu} < R_H^{pu} + \frac{R_H^{pu} * \tau_f}{T_d} \tag{2.21}$$

Likewise, when both impedances are in resistive inductive form, the stability condition is modified to

$$\begin{aligned} L_s^{pu} &< L_H^{pu} + \frac{L_H^{pu} * \tau_f}{T_d} + R_H^{pu} * \tau_f \\ R_s^{pu} &< R_H^{pu} + \frac{1}{Td}(L_s^{pu} + L_H^{pu} + R_H^{pu} * \tau_f) \end{aligned} \tag{2.22}$$

From (2.21) and (2.22), one can see that the stability range for PHIL of hardware under test based on passive impedances can be increased by the use of a low pass filter on the current feedback. The stability range increases with larger time constants of the feedback low pass filter. However, a considerable time constant for the filter attenuates the hardware dynamics for a higher frequency range, reducing the accuracy of the PHIL simulation. Therefore, the filter time constant selection has to be made such that it is just high enough to meet stability conditions. In addition, it has to be noted that a first-order Padé approximation is used to derive the stability criterion and hence is not an exact condition for stability. Consequently, it is recommended to apply Nyquist stability criteria on (2.15) after the filter cutoff frequency is selected.

ITM for interfacing current controlled converter

The controls implemented on a power converter are diverse and specific to requirements. Hence it is challenging to derive a generalized operating stability margin for PHIL simulation of a power converter. A simplified analysis is conducted in this section when a current-controlled VSC is deployed in PHIL simulation for testing. A simplified block diagram of a current-controlled VSC connected to grid is shown in Fig. 2.13 [77]. The current references and feedback (i_{vsc}^*, i_{vsc}) are fed int to a proportional-integral (PI) current controller. The PI converter output is the VSC terminal voltage, and the difference between this terminal voltage and PCC voltage (v_{pcc}) is given to the filter reactor with inductance L_{vsc} and resistance R_{vsc}.

One of the design approaches for current controller design is to choose the PI control parameters such that the dynamics of the current controller and VSC filter reactor together would behave as a first-order filter with a time constant of τ_i. This first-order filter behavior can be achieved by choosing the control parameters as

$$\begin{aligned} KP &= \frac{L_{vsc}}{\tau_i} \\ KI &= \frac{R_{vsc}}{\tau_i} \\ \omega l &= \omega_{ref} * L_{vsc} \end{aligned} \tag{2.23}$$

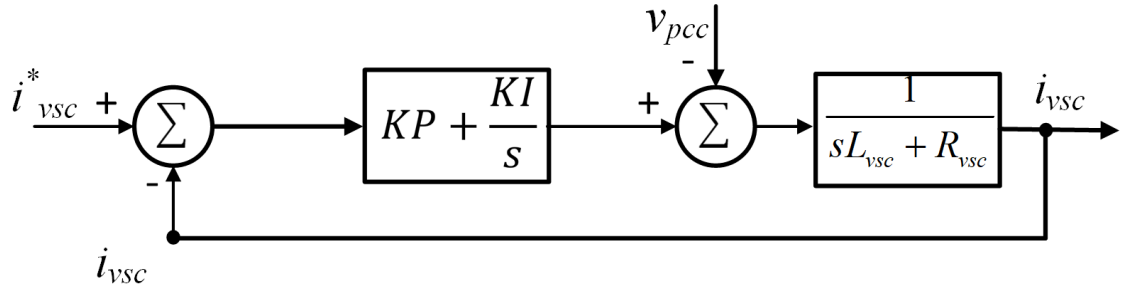

Figure 2.13: Simplified block diagram of VSC with current control and output filter

When VSC with the current control as shown in Fig. 2.13 and control parameters as shown in (2.23) is deployed as the hardware under test in PHIL simulation, the hardware impedance $Z_H(s)$ can be written as

$$Z_H(s) = -\frac{s\tau_i}{1 + s\tau_i}\frac{1}{sL_{vsc} + R_{vsc}} \tag{2.24}$$

Accordingly, the stability condition when the simulated thevenin grid impedance is in resistive inductive form, and hardware is a current controlled VSC can be written as

$$L_s^{pu} < L_{vsc}^{pu}, R_s^{pu} < R_{vsc}^{pu} + \frac{1}{Td}(L_s^{pu} + L_{vsc}^{pu}) + \frac{1}{\tau_i}L_{vsc}^{pu} \tag{2.25}$$

The condition $L_s^{pu} < L_{vsc}^{pu}$ is very challenging to satisfy, the typical per unit values of filter reactance may range anywhere from 0.05-0.3 pu depending upon the rating and switching frequency, as a result the simulated equivalent network reactance has to be quite low to ensure stability with ITM without any compensation. In other words, the short circuit ratio (SCR) at the simulate PCC bus must be greater than the inverse of the filter reactance value in pu. Thus, the PHIL simulation with ITM interface of VSC can only be stable when VSC is connected at a strong grid with SCR>5. On the other hand, the stability condition for resistances in (2.25) is quite easy to satisfy for PHIL studies on VSC hardware connected to transmission systems as the equivalent network resistance (R_s^{pu}) is quite low. This instability is not accurate and does not occur in reality and is a consequence of PHIL simulation. The addition of a low pass filter for the current feedback filter can increase the stable operation range of PHIL simulation. With the current feedback filter, the stability condition for current-controlled VSC can be modified to

$$L_s^{pu} < L_{vsc}^{pu} + L_{vsc}^{pu} * \frac{\tau_f}{T_d} + L_{vsc}^{pu} * \frac{\tau_f}{\tau_i} + R_{vsc}^{pu} * \tau_f \tag{2.26}$$

Typically the time constant for the feedback filter (τ_f) is quite lower than the current controller time constant. In addition, the product of resistance of filter reactor and filter time constant ($L_{vsc}^{pu} * \tau_f$) is also quite low compared to other terms. Hence, the stability condition in (2.26) can be simplified to

$$L_s^{pu} < L_{vsc}^{pu} + L_{vsc}^{pu} * \frac{\tau_f}{T_d} \tag{2.27}$$

From 2.27, it can be seen that the magnitude of $\frac{\tau_f}{T_d}$ is a significant factor that can accentuate the stability region of the PHIL simulation. As a case study, the Nyquist plot of G_{ITM}^{ol} for current-controlled VSC with 0.5 pu of software network reactance and 0.025 pu of VSC filter reactance

with different delay values are shown in Fig. 2.14. The software and hardware resistances are kept to be 0.01 pu, and a second-order Padé approximation is used for the delays. The τ_f is kept at 0.2 ms and delay is reduced to increase the ratio of $\frac{\tau_f}{T_d}$. Reducing the delay, or conversely, increasing the ratio of $\frac{\tau_f}{T_d}$ results in non-encirclement of the point (-1+j0), implying the increased stability of the PHIL simulation by delay reduction as seen from the Nyquist plot in Fig. 2.14.

Likewise, similar conclusion can be drawn by keeping the delay constant (T_d) at 200 μs and increasing the τ_f which essentially the same as increasing the magnitude of $\frac{\tau_f}{T_d}$. The stability of PHIL simulation increases as demonstrated in the Nyquist plot in Fig. 2.15.

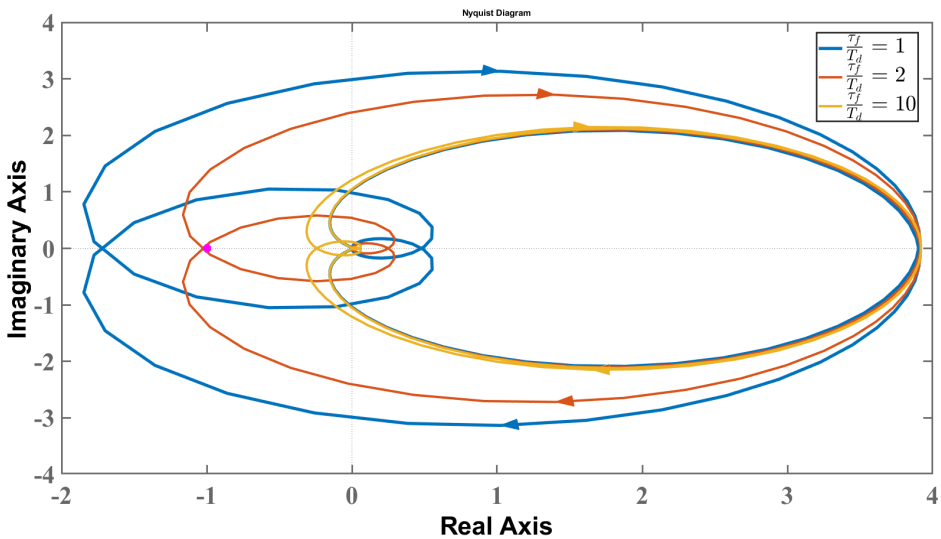

Figure 2.14: Nyquist plot of G^{ol}_{ITM} for current controlled VSC, the delay (T_d) is decreased by keeping same filter time constant(τ_f)

Although PHIL stability is increased by increasing the filter time constant, a downside is that the accuracy of the PHIL simulation is compromised at higher frequency range. The possible loss of accuracy is demonstrated in the frequency response of the hardware VSC measured from the interface bus of the simulation. The closer the measured admittance is to the admittance with no delay and filter, the more accurate the simulation is. Increase in filter time constant results in more considerable divergence between the admittance seen in simulation and actual hardware impedance.

To conclude, the stability region of the PHIL simulation can be increased by using a low pass filter on feed back filter. Larger the filter time constant, or alternatively smaller the cutoff frequency of the low pass filter the PHIL stability range can be increased. However, this comes at the cost of reduced accuracy at higher frequency range. The better way to increase the PHIL stability margin is to reduce the limits as much as the hardware configuration allows and select the low pass filter cutoff frequency as low as possible.

2.3.2 Delay characterization

In this section the delays in the developed PHIL test setup is studied. A simplified block diagram of the delays present in the PHIL loop are shown in Fig. 2.17. The amplifier used in the setup is

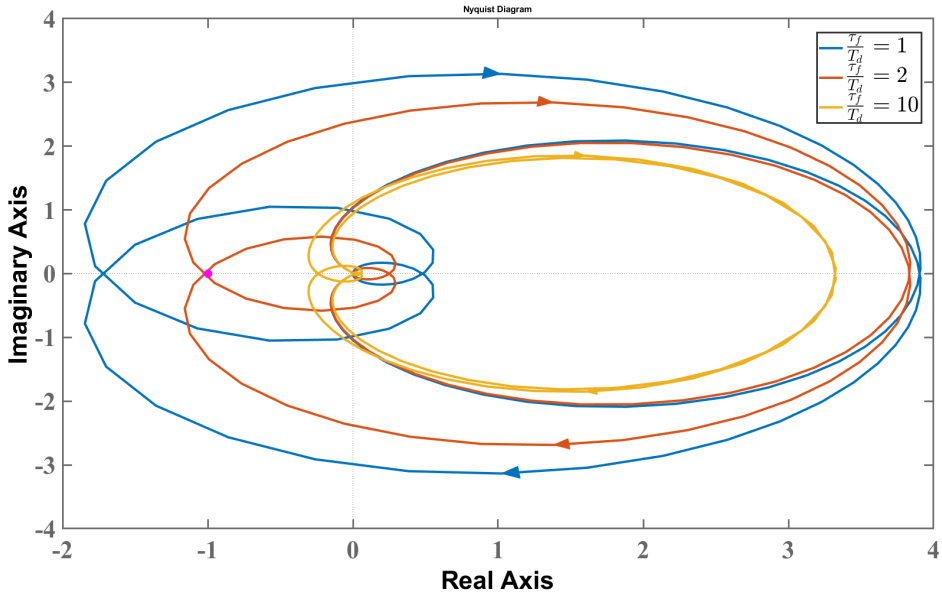

Figure 2.15: Nyquist plot of G^{ol}_{ITM} for current controlled VSC, the delay (T_d) is kept constant at μ and filter time constant is increased(τ_f)

SPITZENBERGER SPIES PAS 2500, a linear amplifier with a very high slew rate of SPITZENBERGER SPIES PAS 2500 linear amplifier. The response of the linear amplifier for a step input is shown in Fig. 2.18. The response confirms the datasheet rise time value (τ_{amp}) of < 5 μs. The sensed voltage value from the linear amplifier is delayed even more but still settles with 10 μs. The RTDS GTAO cards have a specified delay of 1 μs. In RTDS, the simulation can be run in two environments; a large time step simulation (typical time step 50 μs), and a small time step simulation (typical time step 2μs). Because of the computation constraints in small time step simulation, it is convenient to run the PHIL interface with large time step simulation. Also, a two-step interface to large time step is required if the PHIL interface is with small-time step simulation. Thus, the RTDS time step (typical time step 50 μs) dominated all the other delays due to analog/digital transformations. The time elapsed between a signal sent from realtime simulation and measured feedback value is shown in Fig. 2.19. It can be seen that the net total time delay is equivalent to 2 times the simulation step, and All the other delays occur in between the time steps and do not influence the overall delay. One must note that delays in the setup are dependent on the PHIL components such as realtime simulation platform and amplifier type. For instance, if the realtime simulation platform was newer NovaCor chassis, which can simulate a larger network at a much smaller time step (< 10 μs), the delay will be much smaller. Similarly, the amplifiers based on power converters have a much smaller bandwidth and hence a larger delay.

2.4 Summary

This chapter presents the methods utilized in the thesis for modeling, analysis, and validation. A discussion of modeling methods of the system components in a rotating reference frame for faster simulation and easier development of small-signal models of large systems is presented in this chapter. In addition, small-signal analysis methods utilized in this thesis such as impedance analysis and eigenvalue analysis are reviewed. The developed PHIL platform for validating

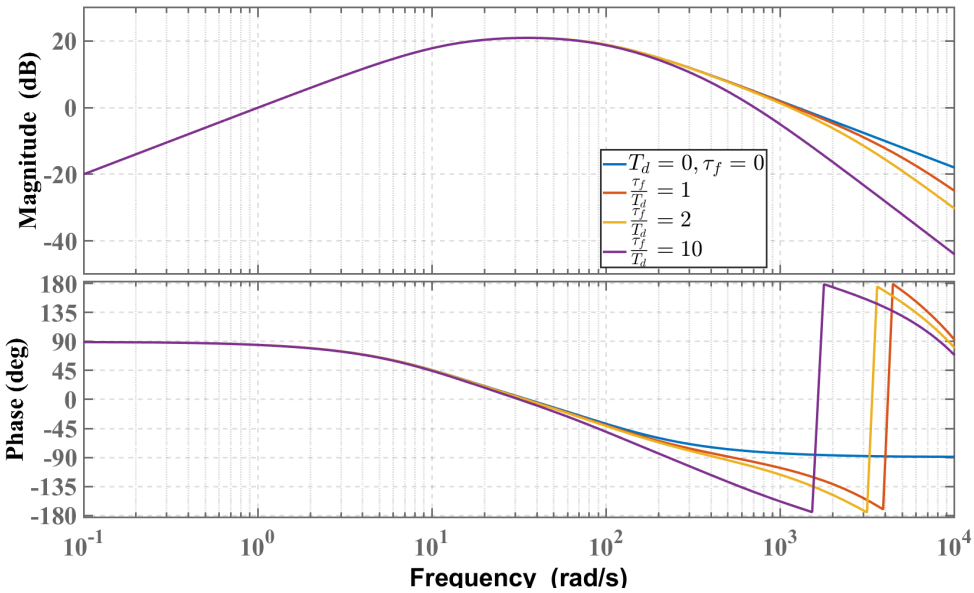

Figure 2.16: Frequency response of the hardware VSC measured from the interface bus of the simulation, the delay (T_d) is kept constant and filter time constant is increased(τ_f

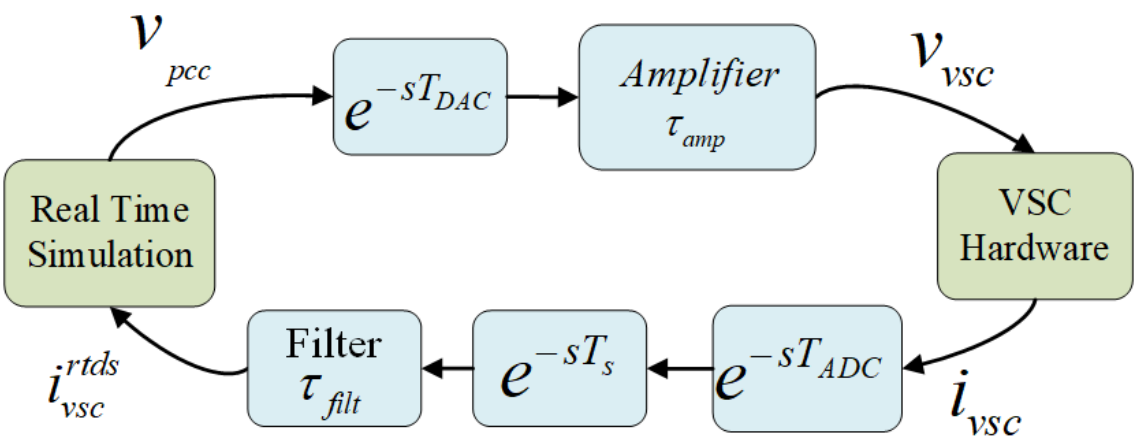

Figure 2.17: Delays in the PHL setup, Adapted from [**Pub. G**]

the control strategies proposed in the thesis is discussed in detail. A contribution of this thesis presented in this chapter is the assessment of the stability range of PHIL validation of VSC.

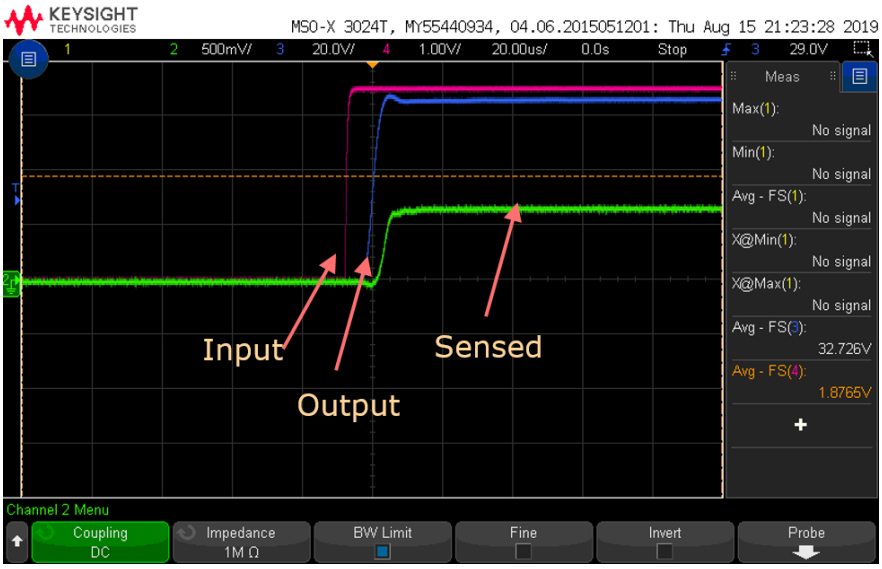

Figure 2.18: Delays in the PHL setup

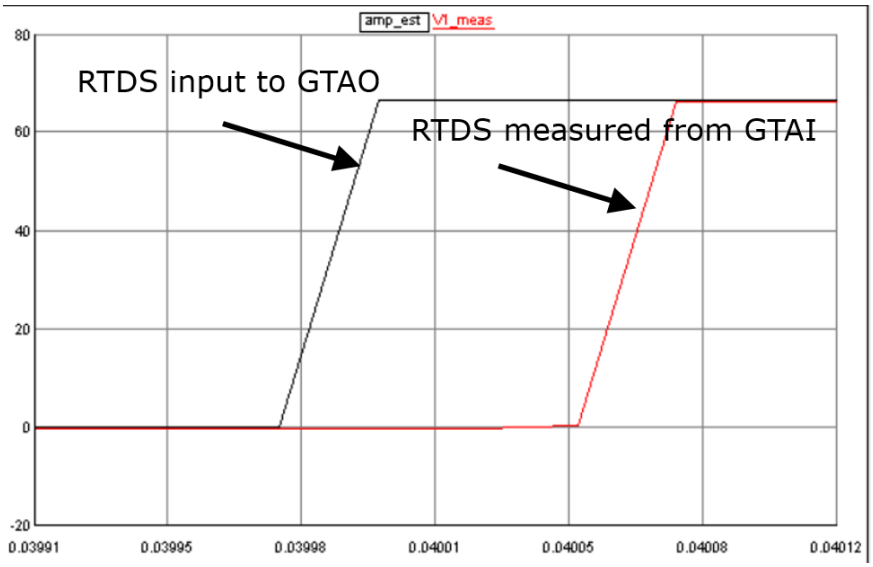

Figure 2.19: RTDS time elapsed between the signal sent to amplifier and signal feed back from amplifier

Part I

Grid Following Converter

CHAPTER 3

Grid Following Control: Stability Analysis

The grid following control applied to voltage source converters are termed as grid following converter (GFL). In this chapter, the stability impact of GFL is investigated in detail. The small-signal model building and background of the analysis, such as impedance analysis and eigenvalue analysis, are detailed in Chapter 2. Firstly, impact of the inner loops of GFL control on the stability is analyzed. Subsequently, the analysis is extended to include the GFL outer loops to derive control design guidelines for the GFL. The impact of the current reference saturation and interaction with SG is also investigated in this chapter. Finally, the consequence of the current reference saturation of a GFL connected in an intermediate bus of a radial network on the stability of the network is also analyzed in this chapter. The chapter is partly based on [**Pub. C**] and [**Pub. D**] with changes to fit into the framework of the thesis.

3.1 Introduction

The GFL is a mature technology that has been applied in VSC interfacing RE, HVDC, and BESS for decades. The current control and voltage-based synchronization embedded in the GFL control enables the GFL to ride through any disturbances and protect the sensitive power electronic and passive components of the GFL. In addition to the ease of control during transients, the GFL has advantages over GFC in scenarios where there is limited energy storage available in the DC side due to direct control of the power and current.

Although there are solutions for BESS with grid forming capabilities available in the market [78, 79], the market availability of GFC solutions for RE is nonexistent to the best of the author knowledge. It is expected that a significant GFC incorporation to the bulk power grids will begin between 10-30 years from now [80]. This implies that the GFL will be the dominant power converter technology deployed in the power grid for the short term (at least) and coexist with SG. Nevertheless, GFL has been identified as a potential barrier in RE penetration due to stability (and protection) challenges to the power system at significant GFL penetration [29]. Therefore, there is a necessity to analyze in detail the potential instabilities manifested by GFL to the power system and investigate the interaction of GFL with the SG.

Several past research has studied the stability of the GFL converters. The inner loops in GFL, including current control, and PLL have been the focus of many past studies. In [50, 51] design guidelines for control parameters are listed based on the passivity behavior of the power converter impedance. The key guidelines for extended stability is to limit the PLL BW. Likewise, [48], utilizing eigenvalue and time-domain analysis, showed that PLL also limits the power transfer capability of the GFL and suggests that the theoretical power transfer range can be achieved if the

PLL gains are limited. Similar conclusions are also drawn in [46, 47, 49] which showed that PLL design could result in negative incremental resistance behavior for VSC impedance. However, the interrelation between the response speed of all the inner loops are yet to identified. And the design guidelines for PLL and current controller based on detailed interrelation between the current controller and PLL design considering PLL bandwidth and phase margins needs to be derived.

GFL with outer loops for active power and voltage control with frequency and reactive power slope is the considered GFL structure utilized in this study. Converters with such control structures are also called grid supporting converter control in literature [81]. Past research have investigate the impact of outerloops on the stability of the GFL. Ref. [26] has demonstrated that the reactive power control at the grid interface point instead of ac voltage control significantly limits the ac power transfer capability of the GFL. The limitations of GFL control of active power and voltage due to high coupling between the active power and voltage in a weak grid are also discussed in [25, 82]. A decoupling of the power and voltage control based on nonlinear and lookup tables are presented in [25, 82] to increase the stability margin of the GFL in the weak grid. However, such advanced control requires knowledge of the system and adds complexity in realization. In this regard, a design guideline for the design of the conventional active power and voltage control when the grid is weak with a low short circuit ratio (SCR) could be useful in ensuring the stability of GFL under low grid strength. Furthermore any potential adverse interaction with the SG existing in the network also needs to be assessed.

The GFL has cascaded loops with outer and inner loops. The outer loops can saturate for extreme operating conditions, leading to a control mode change in GFL from power-voltage control to a current-controlled converter. An analysis of the impact of such mode change on the system stability and potential interaction with other VSC's during such a mode change is not detailed in the literature. Finally, the correlation between a simplified impedance-based analysis of stability results derived for GFL with an Eigen value-based analysis is also presented in this chapter. The main contributions of this chapter are

- A small-signal model of an essential system composed of GFL and SG is derived. The stability impact of GFL inner loops on an essential two-machine system composed of SG and GFL is studied in detail using a combination of eigenvalue and impedance-based analysis.
- The stability assessment of the outer active power and voltage control of GFL when the system strength is low is carried out.
- Design guidelines of inner and outer loops to increase the stability range are presented. Challenges of current saturation and accompanied control mode change from power voltage control to current control are evaluated, and the potential interaction between the SG and GFL is considered.
- The stability of the VSC-dominated system with GFL connected at both intermediate bus and end of a simplified radial network with a current limit saturation is studied. It is revealed that when GFL outer power and voltage are saturated, additional stability challenges arise for GFL, which are explained by impedance-based analysis.

The focus of the study is mainly on linear analysis, and thus study does not consider the fault ride through mode or fast fault current injection mode or any other supervisory control-based mode changes, including gain scheduling.

3.2 Grid Following Converter Description

The single line diagram of a three-phase GFL connected to an ac source is shown in Fig. 3.1 and the control implemented is shown in Fig. 3.2. The GFL filter circuit consists of reactor $L1$, its loss resistance R1, damping filter Rf, and the capacitor filter Cf. The interface to the grid via a transformer of reactance $XT1$ and the grid Thevenin impedance of Xg. The GFL control shown in Fig. 3.2 consists of outer active and reactive power loops with frequency droop (Rd_{vsc}) reactive power slope (K_{slope}). The active and reactive power control loops generate the direct and quadrature axis reference currents for the VSC (i^{d*}_{vsc},i^{q*}_{vsc}), which are then given to the decoupled current controller with PCC voltage feed-forward filter. There are also current reference saturation blocks on both d and q channels, limiting the converter from exceeding its maximum current capacity. The basic concept of the decoupled current control is to enable the VSC to control the active and reactive power separately. For this, the current control is implemented in the dq frame, where a PLL makes sure that the filter bus voltage v_{vsc} is aligned with the d axis. A decoupling term ωl is used to eliminate the coupling between the d and q axis currents. A phase-locked loop (PLL) is implemented to provide a synchronizing functionality to the GFL. The PLL tracks the phase of the voltage at the PCC point.

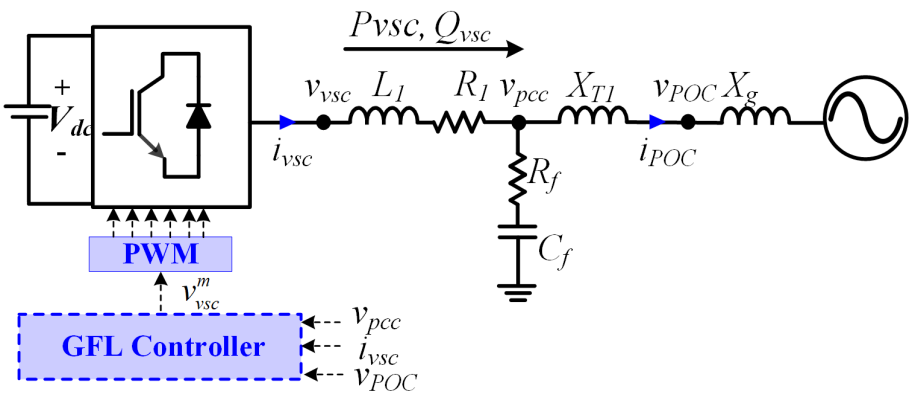

Figure 3.1: Grid following converter circuit connected to ac source

3.3 Steady State Analysis

Before beginning the detailed small-signal analysis, steady-state phasor analysis is conducted for GFL connected radially to an infinite voltage source via a Thevenin impedance of reactance Xg as shown in Fig. 3.3. For a given infinite bus voltage (E) and GFL terminal voltage (V), the active active power transferred between the GFL and the infinite voltage source in pu is given by

$$P_{vsc} = \frac{E.V}{Xg} sin(\theta_{GFL}) \tag{3.1}$$

Where the θ_{GFL} represent the angle between the GFL terminal and the infinite voltage source. Then the maximum possible active power that can be transferred is given by

$$P^{max}_{vsc} = \frac{E.V}{Xg} \tag{3.2}$$

Steady state analysis of two GFL outer loop configurations; active power and reactive power control, and active power and voltage control are analysed in this section.

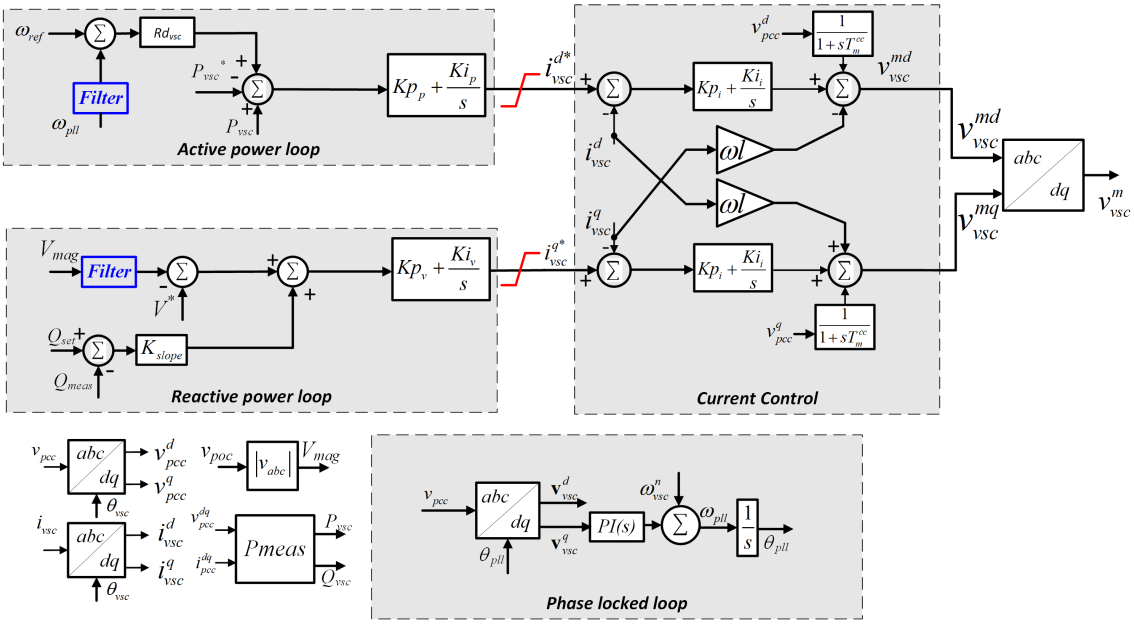

Figure 3.2: Control System of Grid following converter

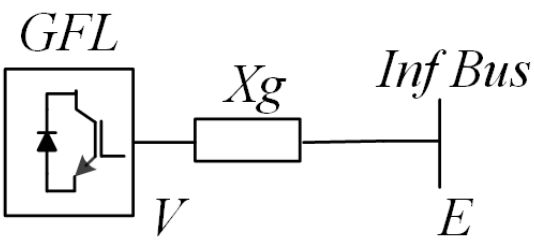

Figure 3.3: GFL connected to infinite bus for steady state phasor analysis

Reactive power control mode

Firstly the GFL is assumed to operate in the power factor control mode. Although this control mode is not further pursued in this thesis, several observations can be made from the power voltage curves of the GFL operated in the power factor control mode in a weak system.

The active power output scaled to the maximum possible power transfer(P_{vsc}^{max}) and its corresponding voltage at GFL terminal is plotted in Fig. 3.4. From the results, it can be seen that

- The active power transfer limit corresponds to the voltage-stability limit of the power system and corresponds to the critical point in the well-known P-V curve. At unity power factor, only approximately half of the maximum possible power can be transferred (P_{vsc}^{max})
- There is a considerable deviation in voltages when the power factor (capacitive reactive power) is changed. And the deviation in voltage increases as the active power is increased
- The slope of the P-V curve in Fig. 3.4 increases significantly when the active power is increased, indicating a strong coupling between the terminal voltage of the GFL and active power transfer

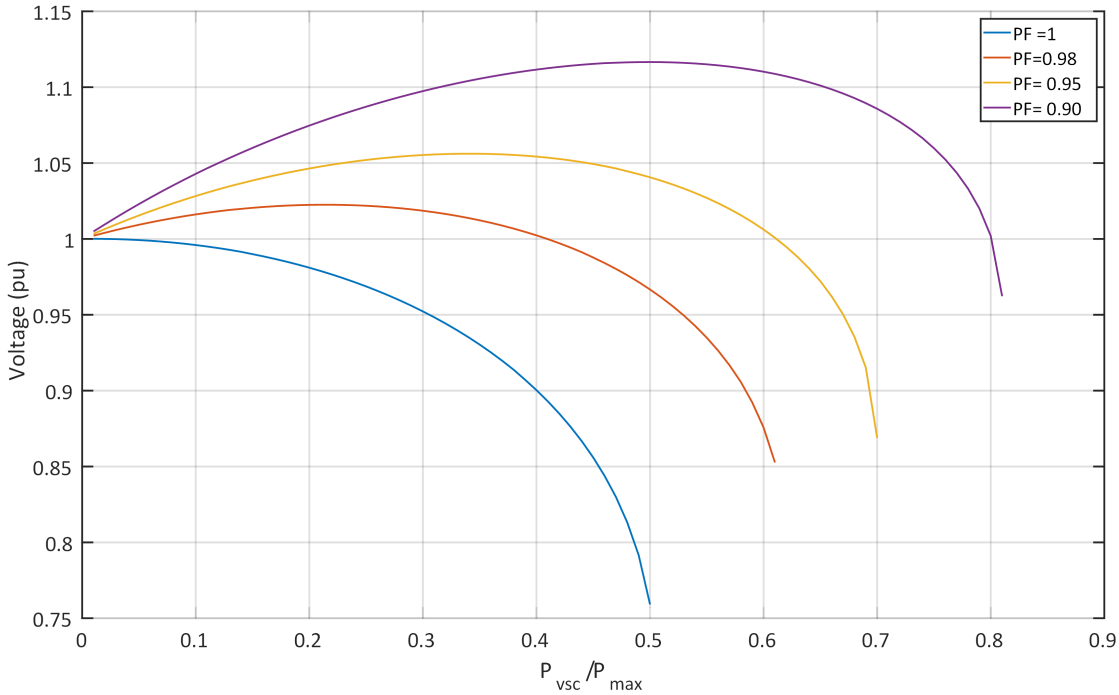

Figure 3.4: GFL output power and voltage when the converter is operating in power factor control mode

Voltage control mode

Now consider the GFL is operating in active and voltage control mode. The GFL active power output scaled to the maximum possible power transfer(P_{vsc}^{max}) and its corresponding voltage at GFL terminal with GFL operating in voltage control mode is plotted in Fig. 3.5. In practise the converter current limit need to be considered to evaluate the active power transfer limit. Three VSC ratings are chosen, such that at rated active power the VSC is capable of providing 0.9,0.95, and 0.98 power factors, and the reactive current saturation is adjusted accordingly. From the results in Fig. 3.5, it can be seen that

- The active power transfer limit can reach (P_{vsc}^{max}) for voltage control without reactive power slope. The active power transfer limit is slightly lower when a reactive power slope is implemented.
- Once the reactive current limit is hit, the voltage drops steeply with the increase in power
- The maximum active power export is slightly higher than the similarly rated GFL at power factor control.

Key Take Aways from the Steady State Analysis

The following are the key takeaways from the steady-state analysis.

- The stability limit with reactive power control mode is the voltage stability limit from the critical point in P-V curve. Whereas, for voltage control mode, the stability limit is the angle stability limit defined by the power angle curve and is much larger than the voltage stability limit. Thus, a voltage control mode is the priffered control mode in VSC over the reactive power control mode.

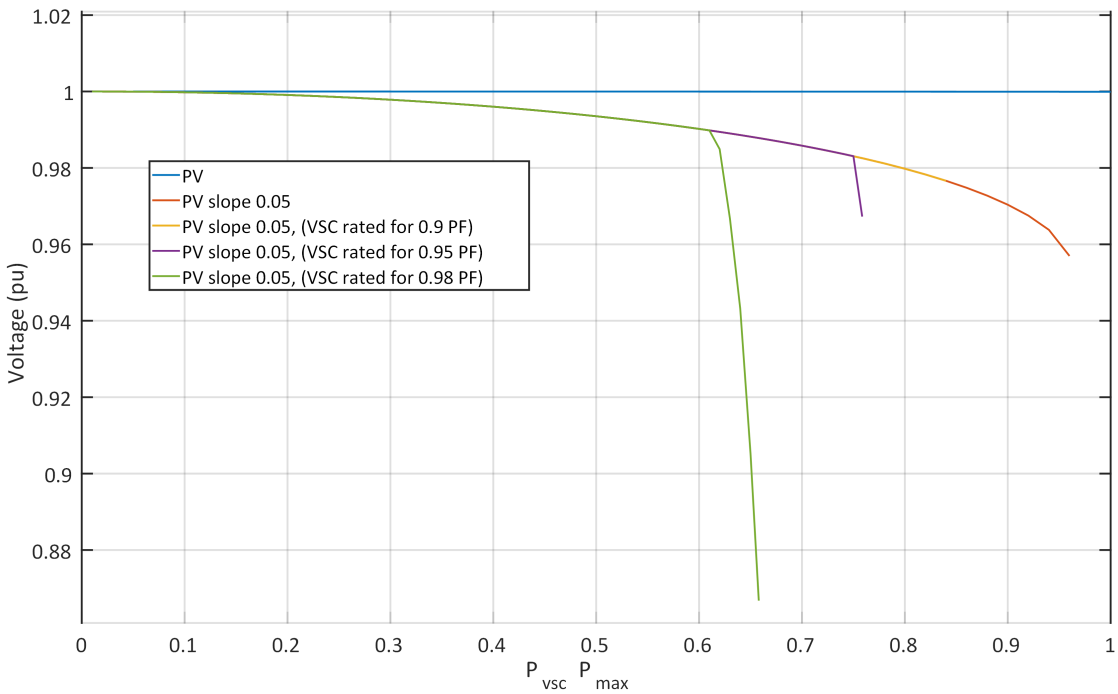

Figure 3.5: GFL output power and voltage when the converter is operating in voltage control mode with reactive power slope

- At high active power transfer range, the slope of power voltage curve is much larger. This significant coupling between the active power and voltage can be a significant challenge to dynamically control power and voltage.
- The current limits in the reactive power channel can play a significant role in potential converter stability and must always be considered when assessing the VSC stability.

The VSC employs multiply cascaded and parallel control blocks to control the power and voltage of the GFL. Hence the steady-state approach only presents the upper stability bound and does not fully capture the challenges for the VSC stability when operating in the stability limits.

3.4 Small Signal Analysis

A system consisting of SG, GFL, passive resistive loads($PL1, PL2$) ,transmission line (Z_{TL1},Z_{TL2}), load(Z_{Load}) and transformer (Z_{T1}) as shown in Fig. 3.6 is utilized to study the GFL dynamics and interaction with the SG. The control of the GFL is shown in Fig. 3.2.

A commonly used four winding electrical network representation of a salient pole synchronous machine [33], along with a simplified automatic voltage regulator (AVR) and speed Governor (GOV) used for the study. The simplified AVR model consists of cascaded PI control and a low pass filter which forms the excitation system model.

$$G_{AVR} = \frac{Kp_{AVR}s + Ki_{AVR}}{s} * \frac{1}{1 + sT_{AVR}} \tag{3.3}$$

where T_{AVR} is the time constant. The simplified governor is realized by a simplified model emulating the first-order response with an f-P droop.

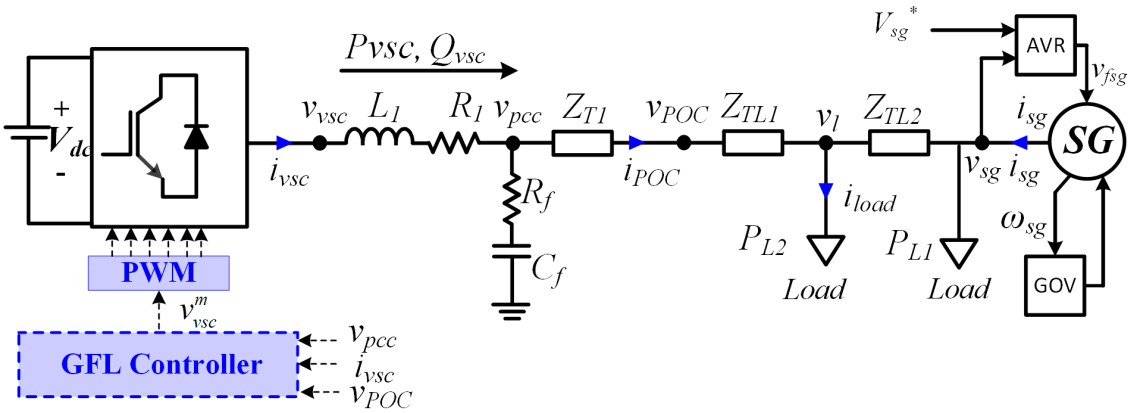

Figure 3.6: Simplified one-line diagram of studied system

$$G_{gov} = \frac{1}{R} * \frac{1}{1 + sT_{gov}} \tag{3.4}$$

where R is the p-f droop expressed in p.u.

In this study, the droop value is chosen to be 0.05 p.u.

As mentioned in methodology chapter, all lowercase variables with an appended superscript of D or Q represent the D or Q component of the original parameter defined in the D-Q frame. Whereas all lowercase variables with an appended superscript of d or q represent the d or q component of the actual parameter described in d-q frame. Variable superscripted with d-q or DQ are variable vectors of the direct and quadrature frame original parameters represented in the dq or the DQ frame, depending on the superscript. Also, variable with appended 0 represents the steady-state value of the parameter.

3.4.1 GFL Control System and Small Signal Modelling

The control block diagram of the GFL is shown in Fig. 3.2, the non linear elements in the control block diagram are the transformation matrices, power measurement block ($Pmeas$), voltage magnitude calculation block ($Vabs$) and the saturation blocks. Rest of the control components are also expressed in rotating dq frame. The linearized forms of the non linear control blocks are given in this subsection

Power measurement block ($Pmeas$)

The power measurement block is used in all the GFC's discussed in this section. First the input voltage and currents are transformed into dq domain. The $Pmeas$ block computes the active and reactive power as in (3.5) and (3.6)

$$P_{vsc} = v^d_{vsc} i^d_{vsc} + v^q_{vsc} i^q_{vsc} \tag{3.5}$$

$$Q_{vsc} = v^q_{vsc} i^d_{vsc} - v^d_{vsc} i^q_{vsc} \tag{3.6}$$

The linearized form of the power measurement block is

$$\Delta P_{vsc} = v_{vsc}^{d0}\Delta i_{vsc}^{d} + v_{vsc}^{q0}\Delta i_{vsc}^{q} + \Delta v_{vsc}^{d} i_{vsc}^{d0} + \Delta v_{vsc}^{q} i_{vsc}^{q0} \tag{3.7}$$

$$\Delta Q_{vsc} = v_{vsc}^{q0}\Delta i_{vsc}^{d} - v_{vsc}^{d0}\Delta i_{vsc}^{q} + \Delta v_{vsc}^{q} i_{vsc}^{d0} - \Delta v_{vsc}^{d} i_{vsc}^{q0} \tag{3.8}$$

Frame transformation matrix (T_{vsc})

The non linear transformation matrix (T_{vsc}) is utilized to translate the variables to the dq reference frame from stationary reference frame (abc) in which the GFL control is implemented. Firstly the frame transformation matrix is modified to link the parameters modelled in rotating reference frame aligned with the system frequency (DQ frame) and the controller frame(dq-frame).The linearized form of the transformation matrix is a function of steady state value of transformed variable and angle difference between the two frames. In addition to the original input variables, the linearized T_{vsc} also has additional input variable $\Delta\theta_{vsc}$. The linearized equation for frame transformation matrix T_{vsc} is given by

$$\Delta x^{dq} = T_{vsc}(x^{D0}, x^{Q0}, \Delta\theta_0)[\Delta x^{DQ}, \Delta\theta_{vsc}]^T \tag{3.9}$$

where, x^{dq} are the variables in VSC controller reference frame, x^{DQ} are the variables in the common reference frame and T_{vsc} is function of steady state operating point and is given by

$$T_{vsc} = \begin{bmatrix} \cos(\theta_0) & -\sin(\theta_0) & -x^{Q0}\sin(\theta_0) - x^{D0}\cos(\theta_0) \\ \sin(\theta_0) & \cos(\theta_0) & x^{D0}\cos(\theta_0) - x^{Q0}\sin(\theta_0) \end{bmatrix} \tag{3.10}$$

Similarly, the linearized transformation of variables in dq frame to DQ frame is given by

$$\Delta x^{DQ} = T_{vsc}^{-1}(x^{d0}, x^{q0}, \Delta\theta_0)[\Delta x^{dq}, \Delta\theta_{vsc}]^T \tag{3.11}$$

where,

$$T_{vsc}^{-1} = \begin{bmatrix} \cos(\theta_0) & \sin(\theta_0) & -x^{q0}\sin(\theta_0) + x^{d0}\cos(\theta_0) \\ -\sin(\theta_0) & \cos(\theta_0) & -x^{d0}\cos(\theta_0) - x^{q0}\sin(\theta_0) \end{bmatrix} \tag{3.12}$$

When the system reference frame is aligned with the rotor angle of the SG, the angle difference θ_0 between the reference frames is given as

$$\theta_0 = (\Delta\omega_{sg} - \Delta\omega_{vsc})/s \tag{3.13}$$

voltage magnitude calculation block (V_{abs}) :The voltage magnitude is computed by

$$V_{mag} = \sqrt{(V_{pcc}^{d})^2 + (V_{pcc}^{q})^2} \tag{3.14}$$

The linearised form of the voltage magnitude computation block is then given by

$$\Delta V_{mag} = \frac{(V_{pcc}^{d0})\Delta v_{pcc}^{d} + (V_{pcc}^{q0}\Delta v_{pcc}^{q})}{V_{mag0}} \tag{3.15}$$

3.4.2 Modelling Methodology and Analysis Overview

The small-signal model of the GFL is developed by interconnecting the linear model of each of the control components of GFL based on matching input and output signals. Similarly, the small-signal model of the SG system composed of SG, AVR, and GOV are derived in state-space format. Once the small-signal models of the three major building blocks of the system, the GFL, SG, and the Network, are formed individually, each model is subsequently interconnected with the respective input-output characteristics. The small-signal model of GFL is derived in dq frame is then interconnected to the rest of the system modeled in DQ frame using transformation matrices defined in Eq. (3.9) and (3.11). In this case, the system reference frame (DQ frame) is aligned with the rotor angle of the SG.

The network model includes the transformer impedance, load, and Network impedance. The linear model of the synchronous machine is well established [33] and therefore not shown in this thesis. The outline of the interconnection of the small-signal models of the system is shown in Fig. 3.7.

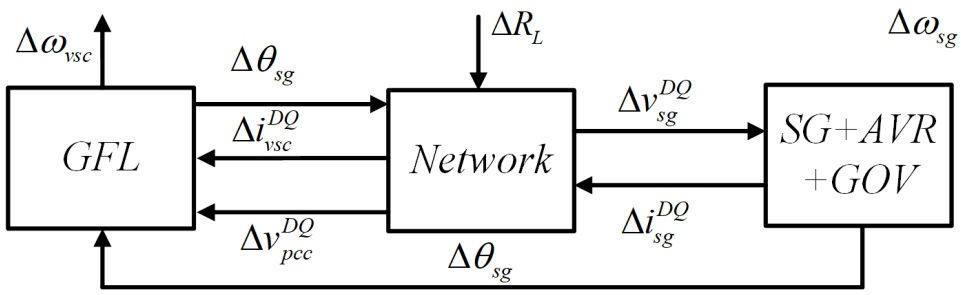

Figure 3.7: Small signal modelling methodology of the system

System Parameters for Analysis

The base case switching frequency is chosen to be 2 kHz which is typical for MW level systems. The filter parameters are designed for the base case switching frequency of 2 kHz. The electrical parameters of the system in the Fig. 3.6 for the base case scenario, represented in per unit at a base power of 70 MVA and voltage of 13.8 kV are shown in Table. 3.1. Both the GFL and SG is considered to be rated at 70 MVA. The control design of the outer loops is carried out in the base case scenario.

Table 3.1: GFL filter and network parameters for the base case scenario

Parameter	Per-unit (pu)	Parameter	Per-unit(pu)
L_1	0.2	R_1	0.02
R_f	0.3	C_f	0.05
Z_{TL1}	0.01+0.1j	Z_{TL2}	0.02+0.2j
Z_{T1}	0.1j	Z_{Load}	1.0

Small Signal Analysis Approach

First, the impact of inner loops of GFL stability is assessed. A screening study by varying system and control parameters is conducted to identify the critical eigenvalues. Then a detailed sensitivity

Table 3.2: State variables

State Names	Description
$\psi_{q'}, \psi_{d'}, \psi f_{d'}, \psi k_{d'}, \psi k_{q'}, \omega_{sg'},$	SG fluxes and rotor speed
$avr_{lp'}, avr_{PI'}, gov_{lp'},$	AVR and Governor states
$GFL_{Id'}, GFL_{Iq'}, GFL_{vgqf'}, GFL_{rd'}$ $GFL_{rq'}, GFL_{\theta PLL'}, GFL_{vgdf'}, GFL_{rpll'}$	GFL control and filter reactor states
$IgD_{TF1'}, IgQ_{TF1'}, VgD_{RC'} VgQ_{RC'}$ $, IgD_{TF2'}, IgQ_{TF2'}$	Network states

analysis is of the control parameters is carried out, and the mechanism of the origin of the critical mode is discussed. In addition, impedance analysis and passivity analysis is also utilized to investigate these modes, and a design guidelines for the inner loop control parameters are discussed. The outer loops are then added and the small-signal stability is evaluated by designing in the inner loops according to the developed guidelines. The interaction with SG is also assessed in small-signal analysis including the saturation of voltage control loop. A time domain non linear simulation results are presented to validate the small signal analysis results.

3.4.3 Assessment of GFL Inner Control Loop Impact on the System Stability

In this subsection the VSC connected to the synchronous machine is analysed by including the inner loop, i.e PLL and current control. Outer loops were included in steady state computation to obtain the operating point. The state variables in the full system and their description is given in Table. 3.2.

From the initial screening study using parameter variations, two key eigenvalues related to the VSC inner loops were identified; a *low-frequency inner loop eigenvalue* in the range of 5 to 20 Hz, and a *high-frequency inner loop eigenvalue* observed was observed in the 40 to 150 Hz.

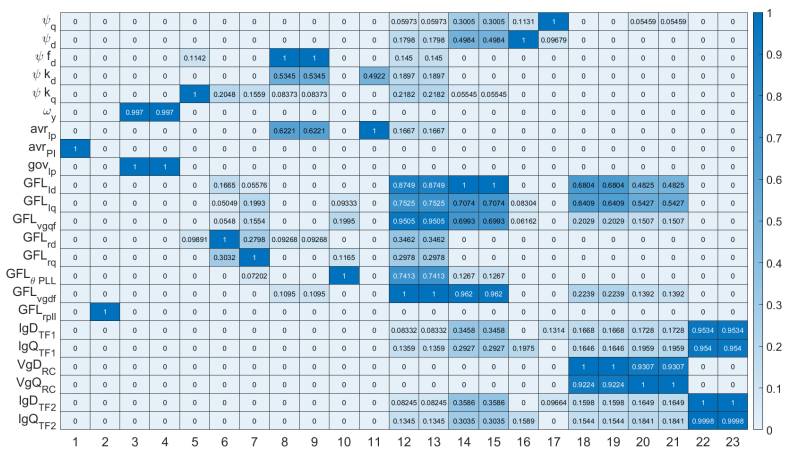

Figure 3.8: Participation factor of eigen values of the system with only inner loops considered for VSC

Low frequency inner loop eigen value

This eigenvalue are corresponds to mode 12 and 13 in Fig. 3.8. The states that participate the most in this mode are PLL ($GFL_{\theta PLL}$),feed-forward filter (GFL_{vgqf}, GFL_{vgdf}) as well as the VSC output current (GFL_{Id}, GFL_{Iq}) and current controller states (GFL_{rd}, GFL_{rq}). The participation of the network states is generally low in this mode. Also, the participation level of this low frequency mode was low (but present) for the synchronous machine states.

The origin of this eigenvalue can be studied by reducing the current control and VSC model. The conventional design approach for the decoupled current control is to choose the control parameters such that the dynamics of the current controller and VSC filter reactor current together would behave as a first-order filter. This first-order behavior can be achieved by choosing the control parameters as

$$\begin{aligned} KP_i &= \frac{L_{vsc}}{\tau_i} \\ KI_i &= \frac{R_{vsc}}{\tau_i} \\ \omega l &= \omega_{ref} * L_{vsc} \end{aligned} \tag{3.16}$$

Where L_{vsc}, R_{vsc} are the inductance and the resistance of the filter reactor, and τ_i is the desired rise time of the current control. By selecting the control parameters as shown in 3.16, in a loop transfer function ($L(s)$) which has a slope -1 throughout the frequency range

$$L(s) = \frac{1}{s\tau} \tag{3.17}$$

Thus current controlled VSC system with a feed-forward voltage filter of time constant Tm^{cc} without considering the PLL impact can be simplified as

$$\begin{aligned} i^d_{vsc} &= \frac{1}{1+s\tau_i} i^{d*}_{vsc} - \frac{s\tau}{1+s\tau}\frac{sT^{cc}_m}{1+sT^{cc}_m}\frac{1}{sL_{vsc}+R_{vsc}} v^d_{vsc} \\ i^q_{vsc} &= \frac{1}{1+s\tau_i} i^{q*}_{vsc} - \frac{s\tau}{1+s\tau}\frac{sT^{cc}_m}{1+sT^{cc}_m}\frac{1}{sL_{vsc}+R_{vsc}} v^q_{vsc} \end{aligned} \tag{3.18}$$

Fig. 3.9 shows a simplified control configuration of the GFL with current control. The block diagram structure has a classical control configuration with reference input i^{d*}_{vsc}, plant outputs i^d_{vsc}, and disturbance input as v^d_{vsc}. Also, $\frac{1}{sL_{vsc}+R_{vsc}}$ is the plant model and $\frac{sT^{cc}_m}{1+sT^{cc}_m}$ is the disturbance model with disturbances entering directly at the plant input.

The the relation between the disturbance input v^{dq}_{vsc} and output by including the closed loop can be written as

$$\begin{aligned} i^d_{vsc} &= S(s) * G_d(s) v^d_{vsc} \\ i^q_{vsc} &= S(s) * G_d(s) v^q_{vsc} \end{aligned} \tag{3.19}$$

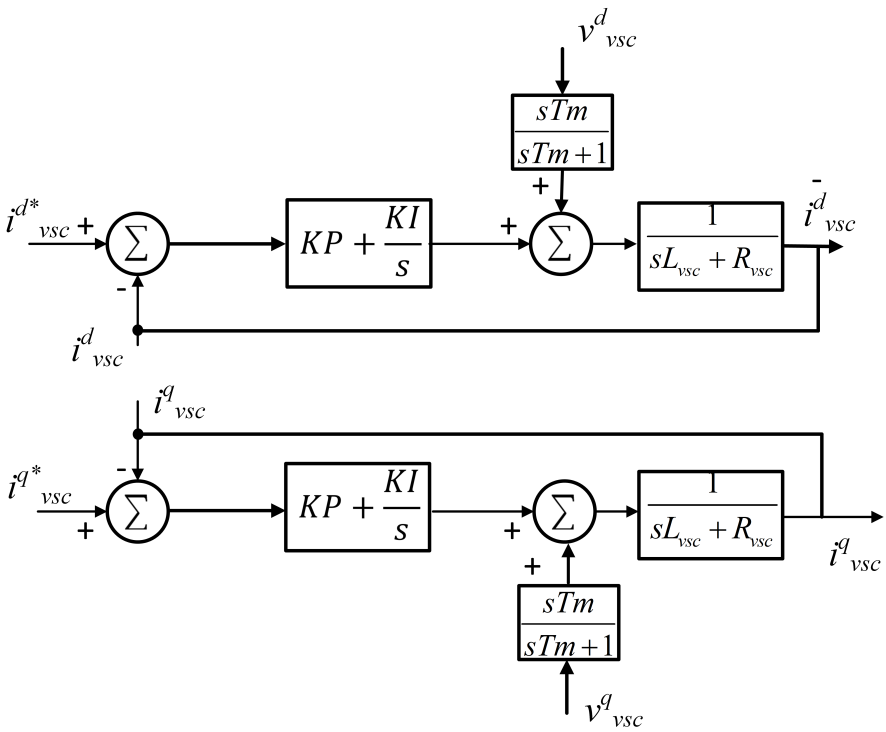

Figure 3.9: Simplified control diagram of current control and output filter

where $G_d(s)$ is the disturbance model which represent the effect on VSC output current i^{dq}_{vsc} due to the disturbances in VSC terminal voltage

$$G_d(s) = \frac{sT^{cc}_m}{1 + sT^{cc}_m} \frac{1}{sL_1 + R_1} \tag{3.20}$$

And $S(s)$ is the loop sensitivity function given by

$$S(s) = -\frac{1}{1 + L(s)} \tag{3.21}$$

When system strength is low, the filter terminal voltages (v^{dq}_{vsc}) become very sensitive to injected current, which can negatively influence the current controlled VSC twofold. Firstly the grid voltage variation is coupled through the feed-forward voltage to the current control as in 3.18, secondly through the phase-locked loop, which defines the controller rotating dq frame based on the filter input voltage. If the low pass filter is eliminated from the feed-forward filter terminal voltage to the current controller, the disturbance input from the filter voltage dq terms would have been absent from 3.18 current controller. However, such an approach is not practical due to the noise present in the filter voltages.

If the influence of the variation of filter terminal voltage under a weak grid scenario on VSC output current has to be limited, it should be ensured that

$$\left| \frac{G_d(j\omega)}{1 + L(j\omega)} \right| < 1, \forall\omega \tag{3.22}$$

or alternatively

$$|1 + L(j\omega)| > |G_d|, \forall\omega \tag{3.23}$$

While this can be achieved by the use of large loop gains (small τ, faster current control), due to the physical limits enforced by the switching frequency of the VSC, a high gain is not possible. The bode plot of $S(s) * G_d(s)$ with variation in feed-forward filter bandwidth is shown in Fig. 3.10. It is evident that as the feed-forward filter bandwidth is decreased, the condition for reducing the impact of grid voltage variation on VSC output current, given by (3.22) is violated. Such characteristics are not desirable and could give rise to potential synchronous oscillation when the full VSC system model, including the weak network and the PLL, is considered. From the Fig. 3.10 it can be seen that the disturbance input is amplified in the region around the frequency of $100 rad/sec$, coinciding with the low frequency inner loop eigen value frequency range. This amplification of the disturbance input under low current control and feed forward filter amplitude is one of the primary reason for unstable low frequency inner loop eigen value.

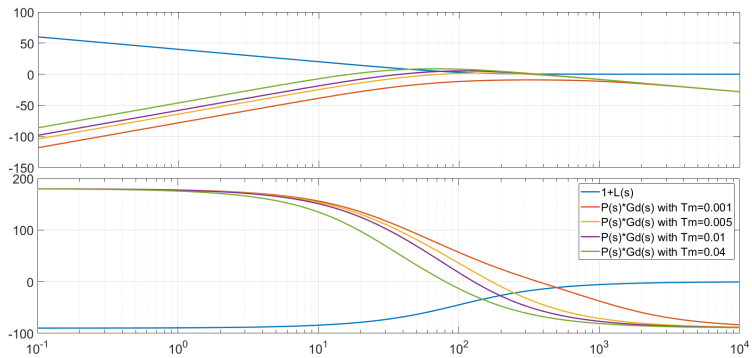

Figure 3.10: Bode plot of the closed loop transfer function between the input v_{vsc}^{dq} and output $P(s) * G_d(s)$ with variation in feed forward filter bandwidth

Parameter Sensitivity from the simplified explanation shown above it is noted that the low frequency inner loop eigen value is sensitive to current control and feed forward voltage filter bandwidth. To further investigate the impact of controllers, filters and network on the eigen value under consideration a parameter sensitivity analysis using eigen value approach is conducted. The parameter sensitivity is done with the full system including the synchronous machine. The power converter steady state analysis and the screening eigen value based analysis had shown that the inner loop low frequency mode is most affected while operating in inverter mode with maximum power, therefore the eigen value sensitivity study is conducted with an operating point corresponding to inverter mode with an active power transfer of 1.0 p.u. Also the load PL1 is drawing 1.0 p.u active power.

The feed forward filter bandwidth is varied from 1 kHz to 100 Hz while keeping the PLL to have a bandwidth and Phase margin of 200 rad/sec and 70 degrees respectively, the low frequency inner loop mode trajectory is as shown in Fig. 3.11. It is clearly evident that a high time constant for feed forward filter is detrimental for stability as expected and predicted from the simplified analysis

done in previous section. Further more, we can also see from Fig. 3.11 that a high band with current control can positively influence this eigen value.

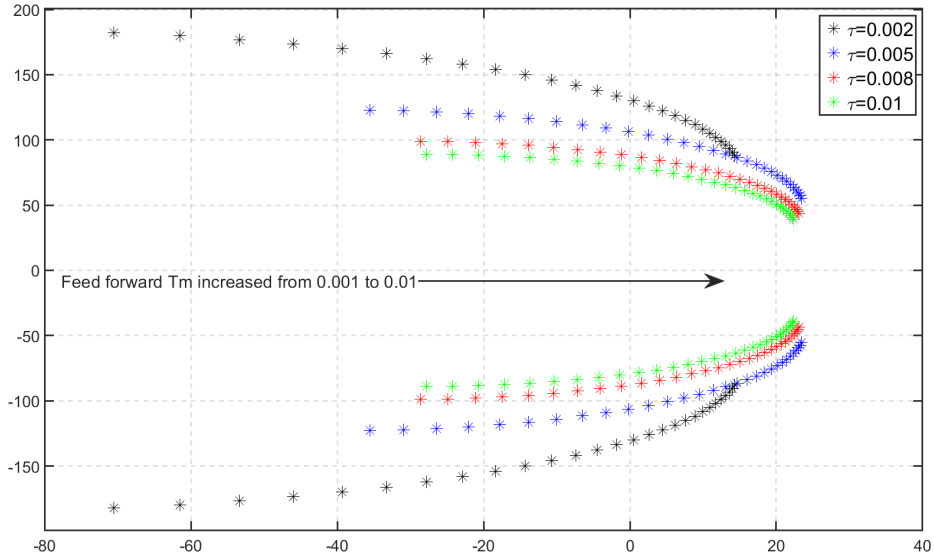

Figure 3.11: The *Low frequency inner loop eigen value* trajectory when the feed forward filter bandwidth is varied from 1 kHz to 100 Hz

The PLL design is carried out by only considering the PLL loop, the small signal linear model used for PLL control design are shown in Fig. 3.12.

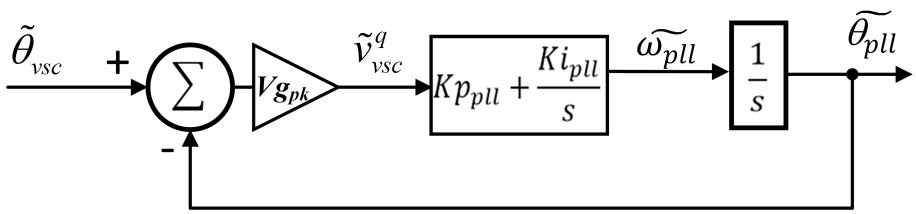

Figure 3.12: Small signal linear model of SRF PLL

The trajectory of low frequency inner loop mode is plotted by varying the PLL bandwidth and phase margin in Fig. 3.13. The PLL BW is varied from $40rad/sec$ to $1000rad/sec$, with 4 different designs for phase margins of $90°, 70°, 50°, 40°$. The feed forward filter time constant and current controller bandwidth has been fixed at $2ms, and 5ms$, respectively. Trajectory here is not straightforward to explain, as the poles for lower bandwidths initially moves towards the right half-plane as the interaction with the current controller and feed forward filter increases and after a certain value of bandwidth, the poles start moving towards the left half plane as the interaction between them reduces. Such a pole trajectory is because the speed of response of PLL and speed of response of forward feed filter are very distinct at very high and low frequencies, and therefore there are fewer interactions between them.

Impedance Assessment The Zpp(s) of GFL and the Thevenin network captures the possible instability with a decrease in the bandwidth of feedforward filter with PLL BW of 100 rad/s as

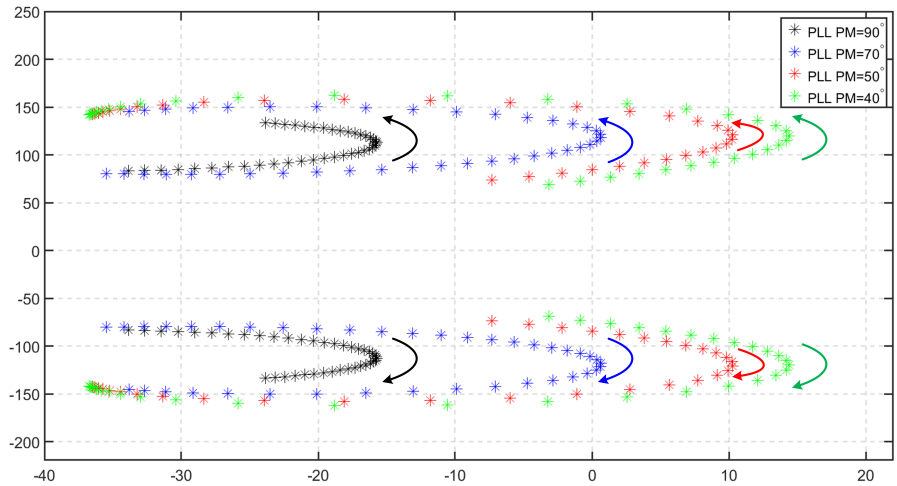

Figure 3.13: The trajectory of low frequency inner loop mode with varying PLL bandwidth and phase margin

shown in Fig. 3.14. At the frequency corresponding to the low-frequency inner loop eigenvalue, the phase of the impedance of the GFL is above 90 degrees suggesting a negative resistance behavior (non-passive) at this frequency range. As the feedforward filter time constant increases, the impedance magnitude drops and starts intersecting the network Thevenin impedance at lower frequencies where the GFL impedance phase is greater than 90 degrees. As observed from Fig. 3.14, at the resonant point, i.e., at the intersection between the GFL impedance and network, the phase difference can exceed or is close to 180 degrees which suggest an insufficient phase margin. This is also validated by the Nyquist plot of the impedance ratio $Z^{-1}_{VSCpp(s)} * Z_{nettpp}(s)$ of VSC and network, which shows that at the higher rise time of feedforward filter, the impedance ratio encircles the point (-1,0) showing instability according to Nyquist criteria as shown in Fig. 3.15.

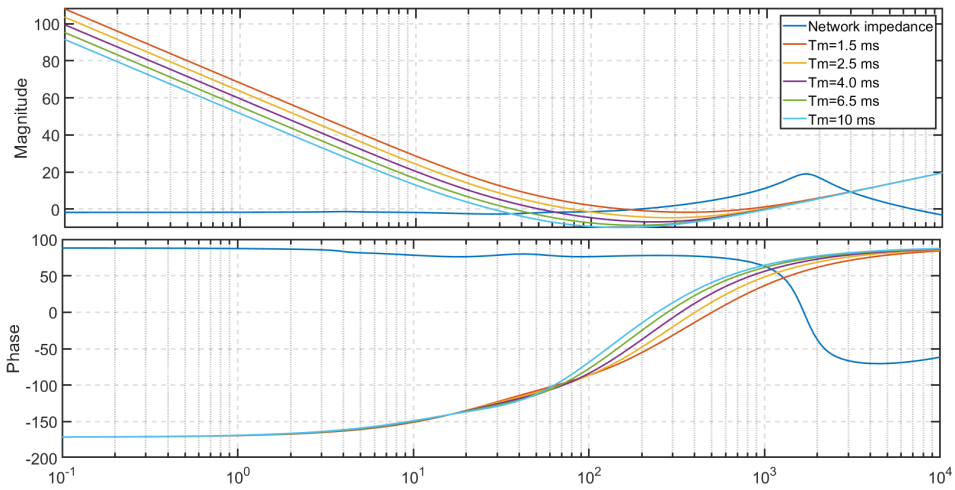

Figure 3.14: Zpp(s) of VSC and network for varying feed forward filter bandwidth

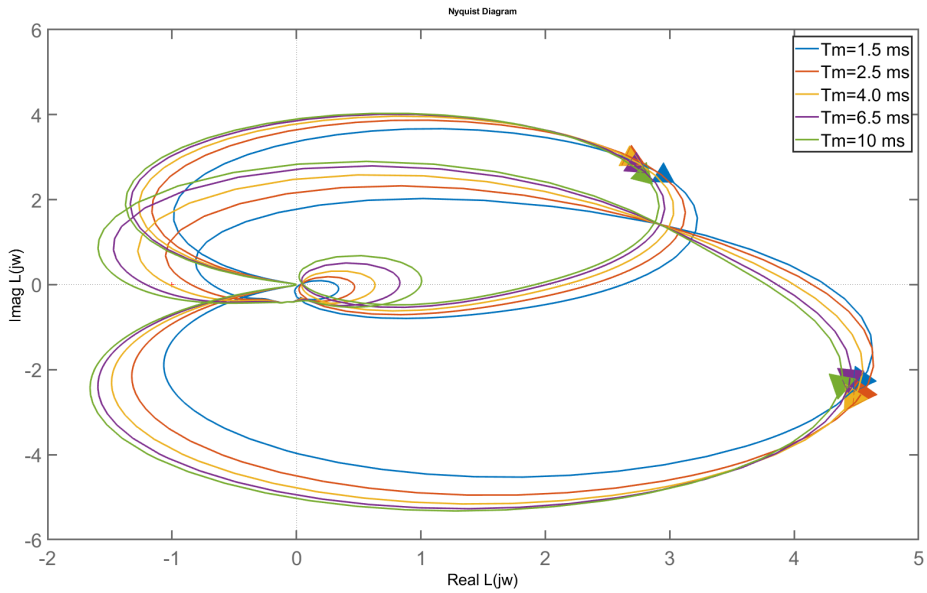

Figure 3.15: Nyquist plot of $Z^{-1}_{VSCpp(s)} * Z_{NEtpp}(s)$ of VSC and network for varying feed forward filter bandwidth

Sensitivity to Active Power Output A sensitivity analysis by varying active power output is conducted by only operating the inner loops. The PLL is designed for 200 Hz BW and 70 Degree PM. The current control rise time is adjusted to be 5 ms and the feed forward filter rise time is kept at 1 ms. The results of Zpp(s) is shown in Fig. 3.16, it can be seen that the impedance magnitude has limited variation with respect to increase in power output.

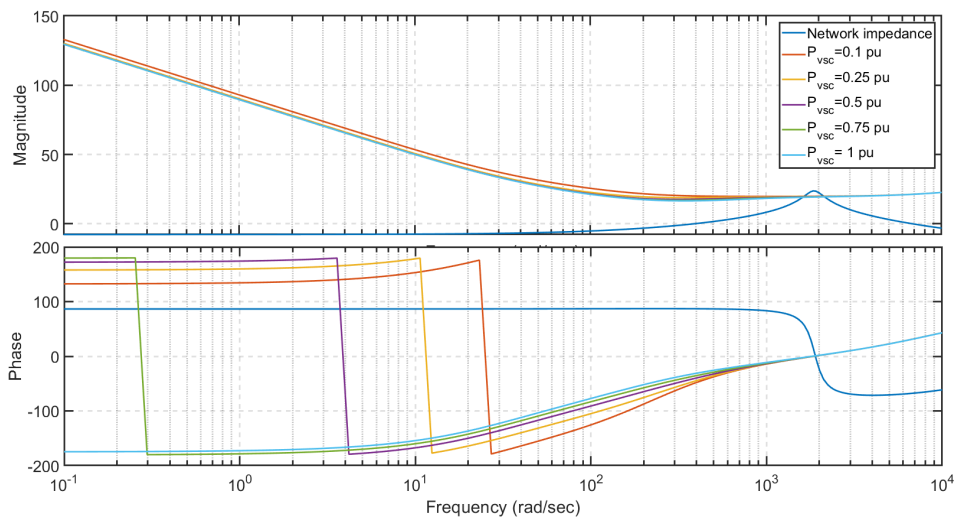

Figure 3.16: Dynamic impedance of VSC and network for varying Power output

Design Guidelines The following are the key design recommendation for avoiding the low-frequency inner loop eigenvalue from becoming unstable

1. Reduce the time constant of feedforward filter as much as the noises in the system permits
2. High proportional gain in current control, and reduce the time constant of the current control loop as much as the VSC switching permits
3. Keep maximum possible phase margin for the preliminary PLL design
4. Change the basic structure of the current controller and PLL. This may include using a controller such as H infinity controllers for current control. Alternatively, the current controller can be designed with simply a proportional gain if it is possible. Such approaches are not further investigated in this chapter, requires further study.

High frequency inner loop mode

These modes correspond to modes 14 and 15 in Fig. 3.8 and are in the frequency range of 40-100 Hz. The states that participate the most are PLL,feed-forward filter, and the VSC output current, also the participation of the network states is quite significant in this mode. The high participation in the network states makes it harder to simplify the system to capture and study this mode. However, a sensitivity study can reveal more details about this mode. The higher the power transfer, the mode moves towards the right half-plane in line with steady-state analysis. Therefore, the active power transfer from the GFL was fixed at 1 p.u with load PL1 drawing 1 pu active power. The PLL BW is varied from $40rad/sec$ to $2000rad/sec$, with 4 different designs for phase margins (PM) of $90°, 70°, 50°, 40°$,, the current control BW is kept at 5 ms and feedforward filter rise time at 1 ms. It can be seen that this mode becomes unstable only when the PLL bandwidth is very high at above 1000 rad/sec and phase margin is modest at $40°$. However, such high bandwidth is not normal for PLL design as it can amplify the harmonics and noises and interact with the current controller. Thus, this mode may not appear with a power system with high VSC-based generation.

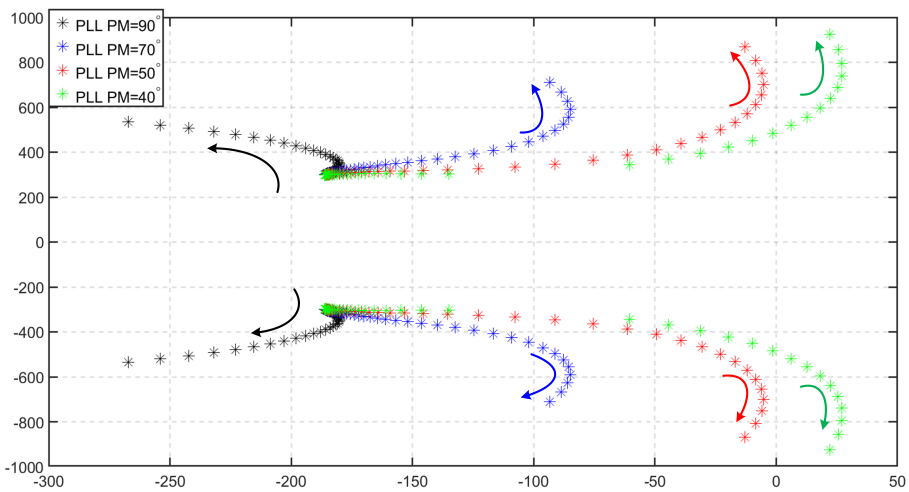

Figure 3.17: The trajectory of high frequency inner loop mode with varying PLL bandwidth and phase margin

3.4.4 Assessment of GFL Outer Control Loop Impact on the System Stability

Previous subsection studied the impact of the VSC inner control loops and possible instabilities due to the inner controller designs. This section investigates the effects of outer loops, namely the active power voltage (PV) control loop, on VSC stability. The whole control loop of the VSC is shown in Fig. 3.2. The inner loops are designed with the moderate stability margin considering the base case network conditions. The time constant for the current control and the feedforward filter is 5 ms and 1 ms. The PLL was designed for 200 rad/sec. The voltage control loop with the reactive slope of 0.05 pu is considered first. Also, it is standard practice to choose the voltage controller as a simple integrator [26], owing to the noise-related reason.

GFL Impedance with the inclusion of Outer loops The dynamic impedance of the GFL with only voltage control enabled and by varying the integrator gain ([10 40]) is shown in Fig. 3.18. The integrator gains are chosen such that the rise of the voltage controller varies from 50 ms to 400 ms. One pu active power is transferred by the GFL.

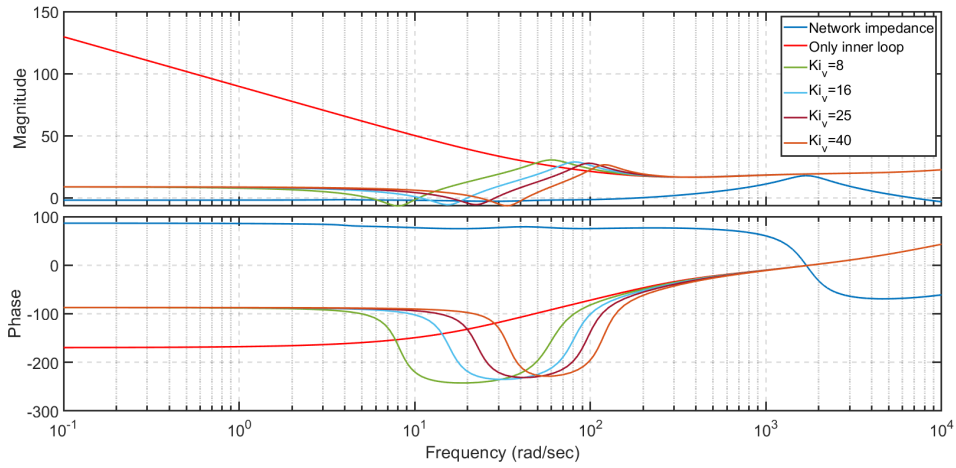

Figure 3.18: Zpp(s) of GFL and network for varying voltage control integral gain (Ki_v)

From Fig. 3.18, it can be seen that the addition of voltage control reduces the low-frequency impedance when compared to GFL with only current control. The inner loops shape the impedance magnitude and phase for frequencies beyond the voltage controller bandwidth.

The dynamic impedance of the GFL with both active power and voltage control loops with active power output is varied is shown in Fig. 3.19. The outer loop integrator gains are chosen to be 10. It can be seen that the low frequency impedance shaped by the bandwidth of active power and voltage controller are highly dependent on the operating point of the GFL. The low frequency impedances are quite low when the active power transfer from the GFL is close to one pu.

Participation Study participation factor of eigenvalues of the system with the addition of active power and the voltage control loop is shown in Fig. 3.20. The voltage control state (GFL_{Vloop}) and power control state (GFL_{Ploop}) participate in the *low frequency inner loop eigenvalue modes* identified during the small-signal analysis of the inner loop in the previous section. However, the outer loops

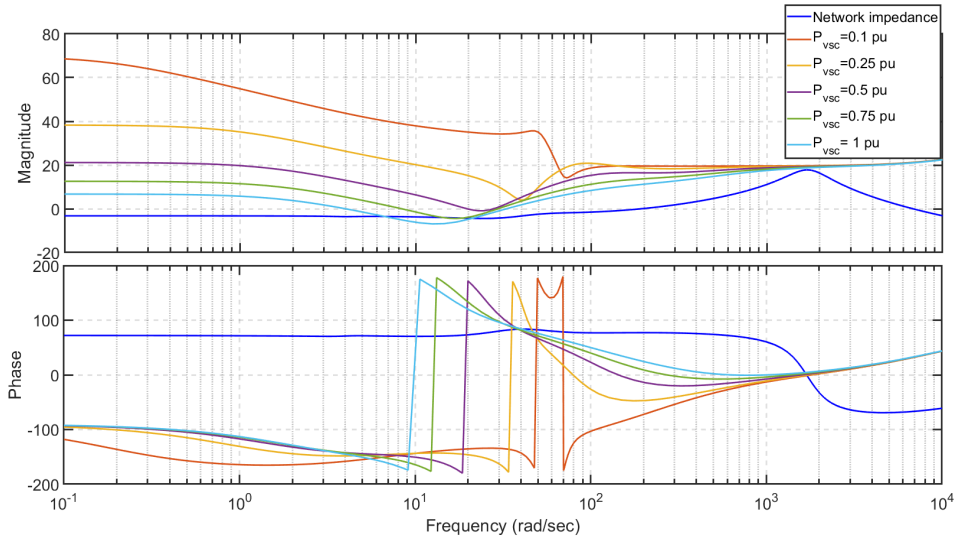

Figure 3.19: Zpp(s) of GFL with both active power and voltage control for varying power transfer

did not significantly impact the modes primarily generated by the presence of inner loops, as long as the design guidelines for the inner loop given in the previous subsection are followed. Also, the active power and voltage control loop have little to no participation in high-frequency mode inner loop mode. The voltage loop controller state represented by GFL_{Vloop}, and the power controller state (GFL_{Ploop}) are seen to participate in another low-frequency eigenvalue (mode 5 and 6 in Fig. 3.20), which in this chapter is termed as active power voltage coupling mode (*PV coupling mode*). This eigenvalue has a close association with voltage stability evaluated by PV curve of the system described in the Steady State Analysis section.

PV coupling mode

In the steady-state analysis section, it was discussed that the voltage of the GFL terminal becomes very sensitive to the active power injected at low system strength. Such high sensitivity between power and voltage makes it challenging to achieve independent control of voltage and power at high power for high SCR systems, and the system can be ill-conditioned. The cross-coupling effect is a typical problem for GFL and has been discussed in [26, 83]. This effect is also a known constraint in achieving a high power transfer for HVDC VSC systems at high SCR, is the primary reason for an unstable PV coupling mode. In this subsection, design guidelines for outer-loop design which minimizes the PV coupling mode from going unstable is discussed.

The frequency of this mode is very low, which can range from lower electromechanical mode and can reach in the range of 5 Hz. If the frequency of the PQ coupling mode was close to electromechanical mode, high coupling between electromechanical mode and PQ coupling mode is visible. Therefore, it is not possible to distinguish between the two modes when the frequencies of both modes are close. This mode coupling occurs when the outer loop is designed to be slow with a time constant of several hundreds of milliseconds.

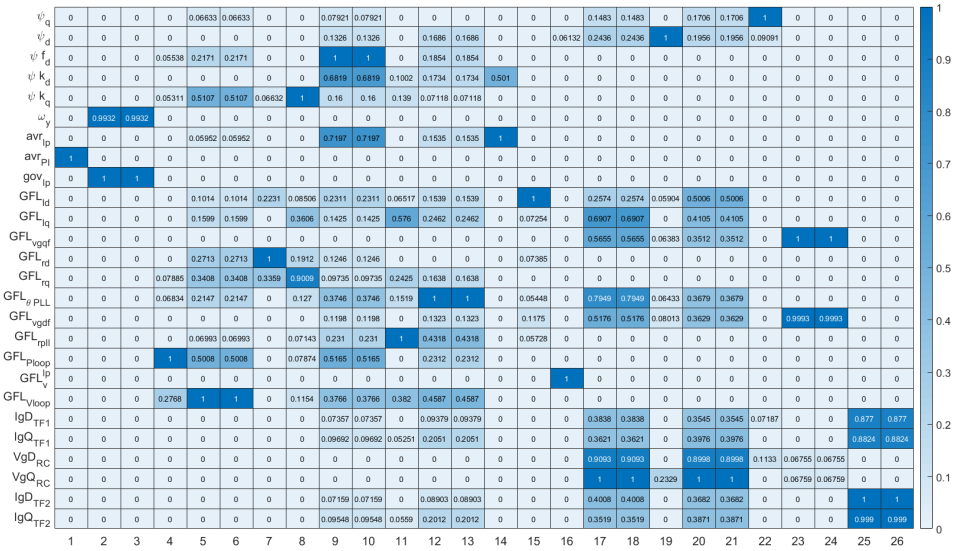

Figure 3.20: Participation factor of eigen values of the system with the addition of active power and voltage control outer loops

Sensitivity to Control Parameters the outer loop parameters were tuned considering the base case using MATLAB SYSTUNE command specifying the required rise time for active power and voltage control loop. The trajectory of PV coupling mode with variation in voltage control integral gain is shown in Fig. 3.21. The voltage controller integral gain (Ki_v) is varied from ([0.01 40]) with the highest value corresponds to a rise time of 40 ms for the voltage control loop in the base case. Three sets of active power controller gain are chosen ([10,15,20]) with the total network impedance (X_{net}) which is the sum of $Z_{TL1}, Z_{TL2} and Z_{T1}$ is increased to j0.7 pu to represent a low system strength scenario. It can be seen that a higher voltage control gain stabilized the PV coupling mode as the mode moves to the left half-plane, whereas higher integral gain is detrimental to the stability of the PV coupling mode.

Thus, the PV coupling mode can be stabilized by slow and faster voltage control. One can also explain the origin of PV control mode and control design using the voltage stability PV curves drawn using steady-state phasor analysis in Fig. 3.4 and 3.5. When the system strength is low, and at high power transfer in inverter mode, any small increase of active power will reduce the PCC voltage steeply, consequently reducing the measured active power. This reduction in active power will further result in the active power controller trying to increase the active power by increasing the direct axis current reference (id^*_{vsc}), which will again decrease the voltage and subsequently decrease the active power instead of increasing, thus resulting in instability. If the voltage controller response is much faster than the active power response, such a situation can be avoided.

Impedance analysis for PV coupling mode the positive sequence impedance, $Z_{pp}(s)$, of both network and VSC is shown in Fig. 3.22. It can be noticed that there is no interaction observed at a very low-frequency range where the PV coupling mode frequency lies. The approximate impedance analysis by using the single channel impedance element ($Z_{pp(s)}$) fails to capture the location of PV coupling mode. The frequency of the PV coupling mode which is extremely low

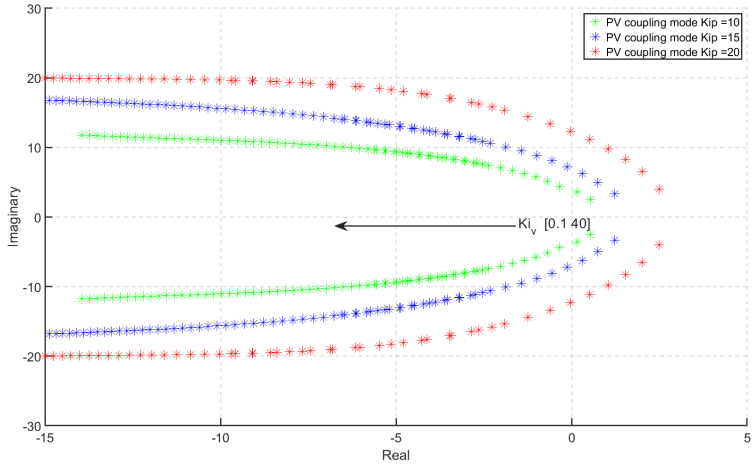

Figure 3.21: The trajectory of *PV coupling mode* with variable outer control loop gains and $X_{net} isequal to j0.7pu$

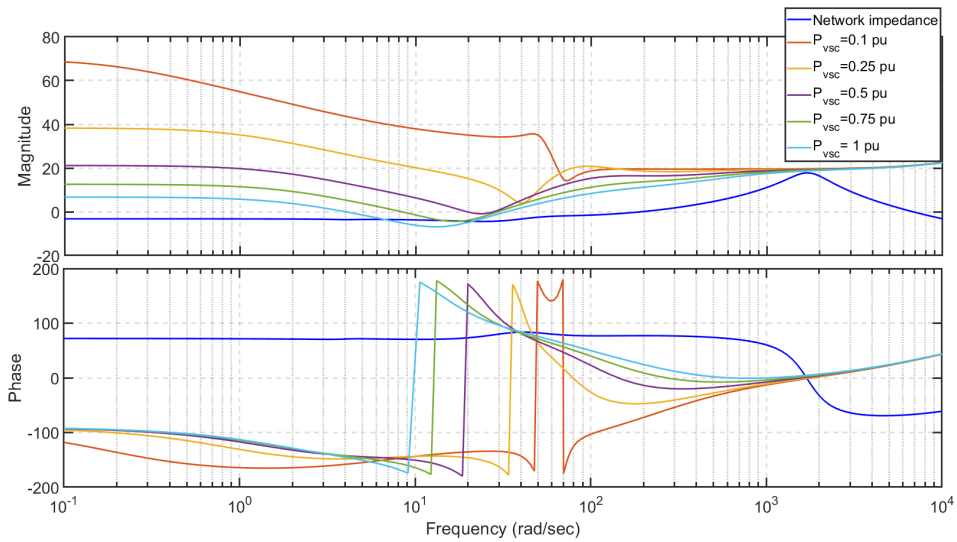

Figure 3.22: positive sequence impedance ($Z_{pp}(s)$) of the network and VSC for a case with unstable PV coupling mode

could be also a possible reason for failure of single channel impedance analysis to capture the unstable mode. The same can be observed in multiple plots of impedance. Although plotting the characteristic loci of the determinant of (I+L(s)) will give an accurate location of the unstable pole.

Reactive Current Limit Activation and GFL SG interaction

The saturation of reactive current reference which is the output of the voltage controller occurs when the reference voltage is cannot be reached with maximum possible designed reactive current limit. Typically the GFL is not necessitated to operate beyond a power factor of 0.95 in the normal

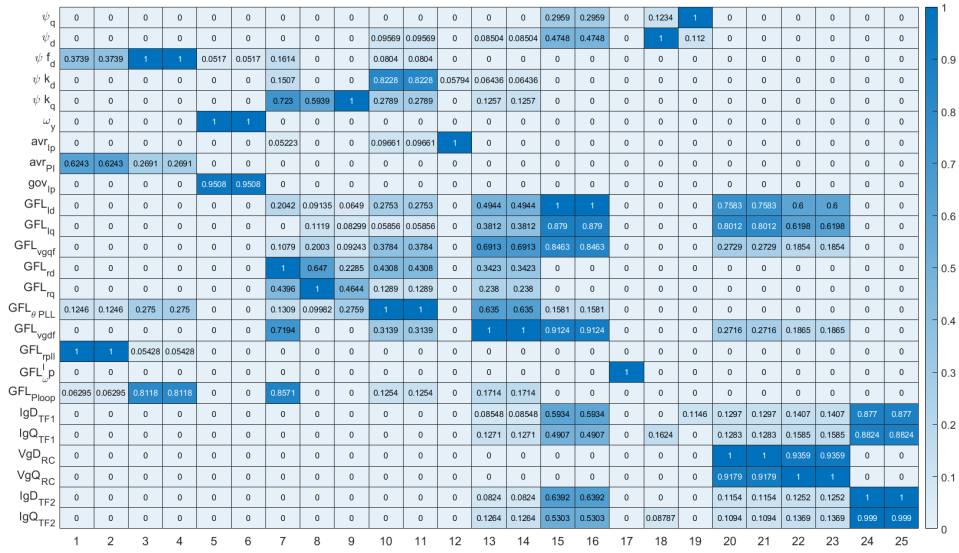

Figure 3.23: Participation factor of eigen values of the system when the reactive current is limited, the AVR and active power control participate in the underdamped oscillatory mode 3 and 4

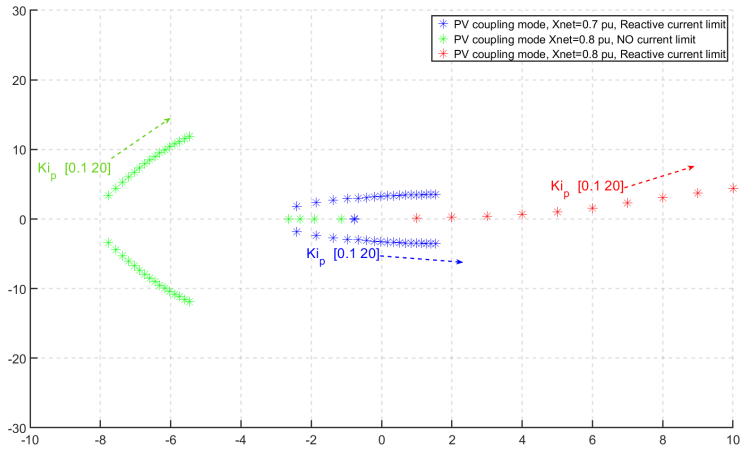

Figure 3.24: The trajectory of PV coupling mode with current limit activation

grid voltage range (0.9-1.1). Hence the saturation voltage control output is highly likely when the voltage reference is kept higher than the GFL can support. The GFL entering and exiting voltage control saturation is also usually seamless without causing a disturbance in the output variables. As explained in the previous subsection, when the system strength is low and high power transfer in inverter mode, active power and voltage are highly coupled. Therefore, any small increase of active power will reduce the PCC voltage steeply. The fast voltage controller is necessary to stabilize PV coupling mode in these scenario. The voltage controller saturation will eventually lead to nonoscillatory and follow voltage stability curve. However, at high active power control gain, the PV coupling mode,mode 3 and 4 in Fig. 3.23 can be oscillatory with high participation of

the AVR controller (AVR_{PI}) and active power loop controller (GFL_{Ploop}) states.

A sensitivity analysis of active power control gain is conducted to evaluate the PV coupling mode with reactive current limit the results are depicted in Fig. 3.24. It can be seen that when the reactive current is saturated the PV coupling mode moves towards more unstable region and can be oscillatory at high active power controller gain.

3.5 Simulation Results

A nonlinear time-domain analysis is conducted to validated the analysis presented in this chapter. First, the system shown in Fig. 3.6 is initialized to base case conditions with GFL transferring one pu active power with only inner loops, PLL is designed to have a BW of 200 rad/s and PM 50 degrees. Midway through the simulation, the forward filter time constant is increased from 1 ms to 2.5 ms. As predicted in the small signal studies the system becomes unstable due to RHP *low-frequency inner loop mode*, the results of voltage at the PCC bus, active (P_{vsc}) and reactive power (Q_{vsc}) output from the GFL confirm the oscillatory behavior due to unstable inner loop mode.

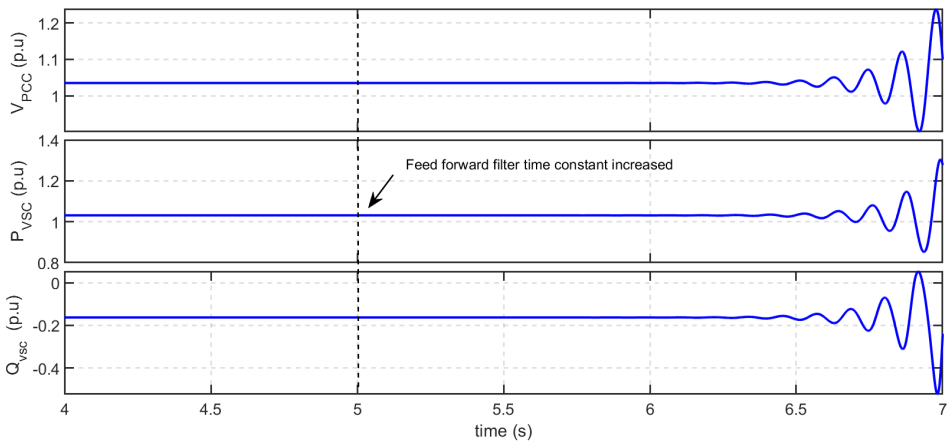

Figure 3.25: Time domain results when the feedforward filter time constant increased with only inner loops active network is in base case mode

The scenario showing the PV coupling mode becoming unstable when the network impedance is increased to 0.8 pu from 0.4 pu is shown in Fig. 3.26

The scene depicting the oscillatory PV coupling mode becoming unstable due to voltage control loop saturation is shown in Fig. 3.27. The network impedance is kept at 0.6 pu, and the inner loop is designed to be stable without the outer controls. When the voltage control reference is increased with reactive current (Iq^*_{vsc}) limit is 0.25 pu, the GFL transition from active power voltage control to active power- reactive current control, and a low-frequency oscillator instability associated with voltage stability limit with the participation of the AVR states is triggered as shown in Fig. 3.27. The response is highly nonlinear due to the limiter activation.

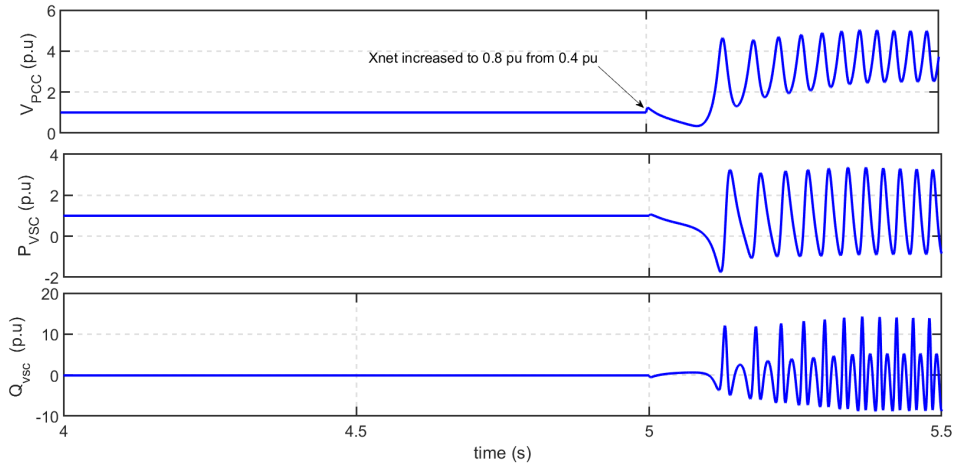

Figure 3.26: Time domain results showing the *PV coupling mode* instability when GFL Xnet is increased to 0.8 pu

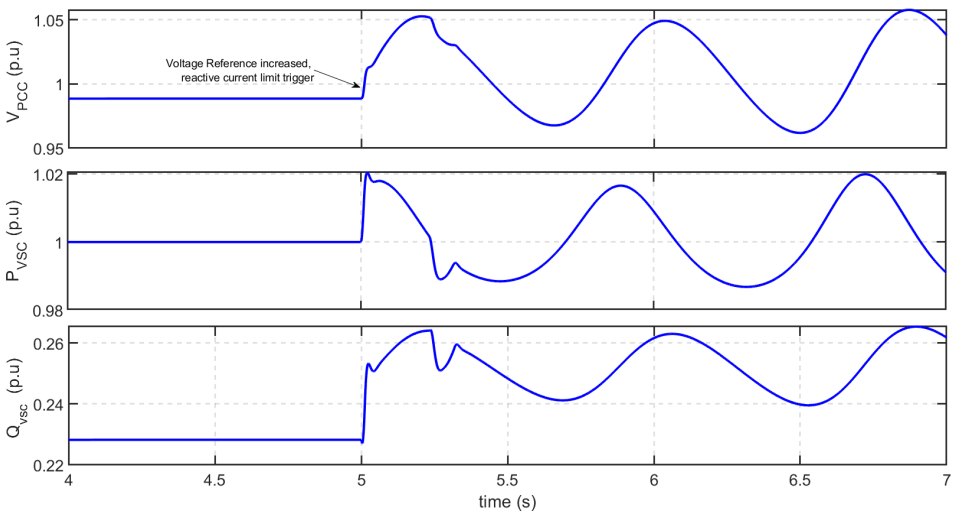

Figure 3.27: Time domain results showing the interaction between the SG and GFL when the reactive current is limited, non linear response due to limiters Xnet=0.7

3.6 GFL Connected at Intermediate Bus and Impact of Current Reference Saturation

In this section, a GFL is connected at an intermediate bus in a radial network consisting of another GFL connected at the end of the network. The study focuses on the impact of GFL connected in the intermediate bus on the Thevenin impedance seen by the rest of the network, and the consequent stability implications are analyzed. The stability implications of the current reference saturation of the intermediate connected GFL on the system are also analyzed.

3.6.1 Desirable characteristics of the Intermediate Connected Component's($Z_{sh}(s)$) Impedance

The impedance stability analysis is carried out at the terminal of a device under test (DUT) which in this case is a GFL connected at the end of the radial network. A simple equivalent impedance network, as shown in Fig. 3.28, can be used to explain the stability of DUT with another component $Z_{th}(s)$ connected at an intermediate bus. The DUT could also be any component with a dynamic impedance of ($Z_{dut}(s)$), such as a power converter or loads that are connected to or planned to be connected to the power system. The equivalent impedance of the network seen from the point of common coupling (PCC) of DUT is given by $Z_{th}(s)$

$$Z_{th}(s) = \frac{Z_{TL1}(s) * Z_{sh}(s)}{Z_{TL1}(s) + Z_{sh}(s)} + Z_{TL2}(s) \tag{3.24}$$

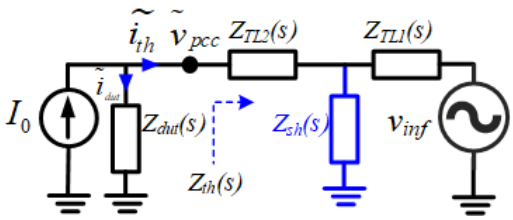

Figure 3.28: Impedance network of a radial system with a GFL connected at intermediate bus ($Z_{sh}(s)$).

Where $Z_{sh}(s)$ is the impedance of a parallel-connected GFL at the intermediate bus in the networks. I_0 is the steady state current injected by DUT and $Z_{TL1}(s)$, $Z_{TL2}(s)$ are the dynamic impedances of the transmission lines. From eqn. 3.24, it can be seen that the Thevenin impedance $Z_{th}(s)$ can be increasingly influenced by $Z_{sh}(s)$, for instance low values of $Z_{sh}(s)$ will result in a lower values of $Z_{th}(s)$.

The loop gain of the feedback equivalent diagram is $Z_{th}/Z_{dut}(s)$, and should satisfy the Nyquist criteria with sufficient margin to ensure stability. The phase margin of the loop can be found by first plotting both Z_{th} and $Z_{dut}(s)$ in a Bode diagram and then calculating the phase difference between the phase curves at each intersection of the magnitude curves. The farther the phase difference from $180°$ at the impedance magnitude intersection, the larger the stability margin.

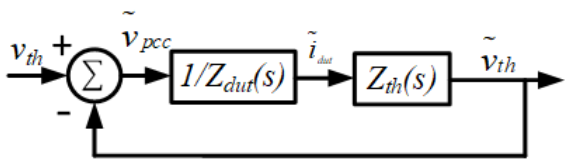

Figure 3.29: Feedback loop equivalent of the converter system under consideration.

Ideally, the $Z_{th}(s)$ should be low at all frequencies and without any resonance points in order to make v_{pcc} less sensitive to the current injected. To enable the $Z_{th}(s)$, which is a series-parallel combination of transmission line impedances and $Z_{sh}(s)$, to be close to the ideal characteristics, one can list the desired characteristics of the parallel impedance $Z_{sh}(s)$ which reduces adverse interaction with the impedance of converter under study ($Z_{dut}(s)$).

- Low impedance magnitude, particularly at low-frequency range (below 100 Hz) with no negative real part at any frequency.
- Inductive in nature to avoid resonance in $Z_{th}(s)$.
- Low variability and no discrete jumps in impedance magnitude for any change in the operating point.

In this section, the dynamic impedance of a GFL is further studied and compared with the desirable characteristics of $Z_{sh}(s)$ to analyze the impact of parallel connection of grid supporting VSC and synchronous generator on the stability of the rest of the system.

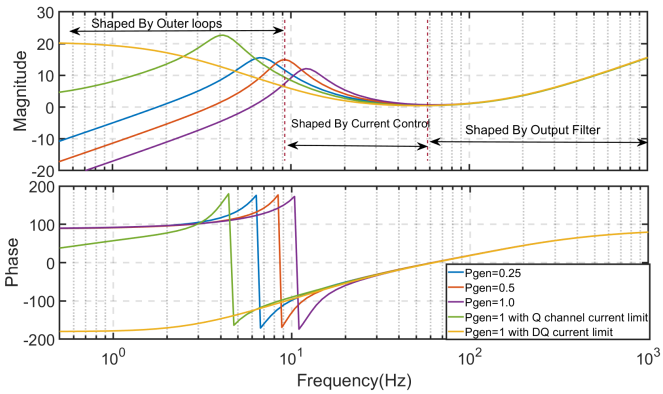

Figure 3.30: Dynamic impedance of Grid supporting BESS VSC at varying power generation at limit activation

3.6.2 Discussion Dynamic Impedance of the GFL

The dynamic impedances of GFL at varying active power setpoint and current limit activation are shown in Fig. 3.30. For perturbations in the terminal voltage, with a frequency below outer loop BW, the converter responds with a current adequate to maintain the active power and terminal voltage references. Therefore, the impedance is low within the BW of the active power and voltage control loops and is predominantly shaped by the outer loops. The terminal voltage perturbations with frequencies beyond the BW of outer loops are acted upon only by the inner current controller with little to no contribution from the outer loops. The current controller can reject or respond with a small current for the low-frequency perturbation in the terminal voltage falling in the current controller's influence range but beyond the outer-loops BW. Beyond the current controller BW, the converter impedance is simply the filter reactance. The converter responses at low frequencies are also influenced by PLL design, which is known to cause an additional phase shift [**Pub. E**],[51].

For a converter equipped with energy storage for active power support, the current limit sets available reactive power. For instance, a GFL system with active power support of 1 pu with 1.1 pu current limit can provide $\sqrt{1.1^2 - 1} = 0.45pu$ of reactive current at full load. Such low value of reactive current resource could often trigger the limiter in the reactive current channel. Furthermore, when the active power setpoint request by the outer loops is higher than the VSC capability at any instant, an active current limit can also be triggered. Such an event is often a consequence of a system contingency such as a loss of generation, leading to a shortage of reactive power resulting in

the GFL hitting both active and reactive current limits. The dynamic impedances with the reactive current limit or both active and reactive current limit activated are higher in magnitude than the no-limits activated case in the low-frequency range for the same operating point as depicted in Fig. 3.30. When the outer control loop is opened due to active or reactive current limit activation, the output impedance switches to the impedance curve corresponding to the current limit cases, resulting in a large upward jump in impedance magnitude in the low-frequency range.

The key characteristics of the dynamic impedance of the GFL are summarized below.

- The variability in the impedance for different operating points is high.
- Except within the bandwidth of voltage control loop, which is limited due to the cascaded nature of the control loop, the impedance is higher than 1 pu.
- The phase of the dynamic impedance is higher than 90 degrees in the low-frequency range, pointing towards negative resistance characteristics. However, unlike an SG, the range of negative resistance and its magnitude is dependent on control and operating parameters.
- The activation of limits in one or both active and reactive current channels can result in large discrete upward magnitude jumps in dynamic impedance.

3.6.3 Network impedance with Intermediate connected GFL (as $Z_{sh}(s)$)

The GFL impedance does not meet any of the desired characteristics expected of parallel-connected elements. The GFL impedance has high variability, discrete magnitude jumps during current limits, and negative impedance frequency range regions. Such characteristics of the GFL dynamic impedance can result in potential instability.

3.6.4 Simulation Results

Electromagnetic transient simulation results that verify the analysis given in this section is presented in this subsection. As shown in Fig. 3.31, a simple test power system ($S_{base} = 140\ MVA$) is simulated in RSCAD. The test power system consists of a parallel-connected 70 MVA synchronous condenser and a 70 MVA GFL connected transmission system at an intermediate bus of the radial network through a three winding transformer and a 140 MVA GFL at the end of the radial network. Both the parallel-connected 70 MVA GFL and SC could be connected or disconnected individually. IEEE AC7B excitation system model is used for the SC. The impedance stability evaluation is performed in the terminal of the 140 MVA GFL at full load conditions. Three test cases are performed; only parallel GFL and no current limit, only parallel GFL and with reactive current limit, with both parallel GFL and SC with reactive current limit. The dynamic impedance of the Thevenin network ($Z_{th}(s)$) and the 140 MVA GFL ($Zdut(s)$) are measured using a frequency scan of the network for all three cases, and are depicted in Fig. 3.32. The oscillatory frequency region of interest of this study has been limited to below 100 Hz.

As seen from Fig 3.32, the parallel-connected GFL at the intermediate bus with voltage control manages to keep the Thevenin network impedance seen by 140 MVA GFL low in the low-frequency range. Such low impedance in the low-frequency range ensures that the network impedance intersects with the 140 MVA GFL at a relatively higher frequency range where the phase difference (PD2) is lower than $180°$. However, the phase of the network impedance crosses $90°$ at a frequency

around 40 Hz, making it act as an active impedance and could pose a threat of oscillatory instability at that frequency. For the same operating conditions, if the current limit is activated on the reactive power channel (Iq_{lim}) on the parallel-connected GFL, the network impedance will increase and intersect the 140 MVA GFL impedance at around 9 Hz with a phase difference (PD1), which is close to $180°$, making the system marginally stable. The impedance of the network with a synchronous condenser provides a balance between maintaining low impedance at all frequencies and ensuring that the impedance phase is not much higher than $90°$. The time-domain results of the system with parallel-connected GFL and SC combinations are shown in Fig. 3.33. The impedance of Z_{TL2} is increased by 0.05 pu at 0.2 sec by opening a breaker in the parallel branch. As predicted from the impedance analysis, the 140 MVA GFL response with the current limited GFL at the intermediate bus becomes unstable. In contrast, the response remains stable when a parallel-connected synchronous condenser is present and when no current limit is triggered in GFL.

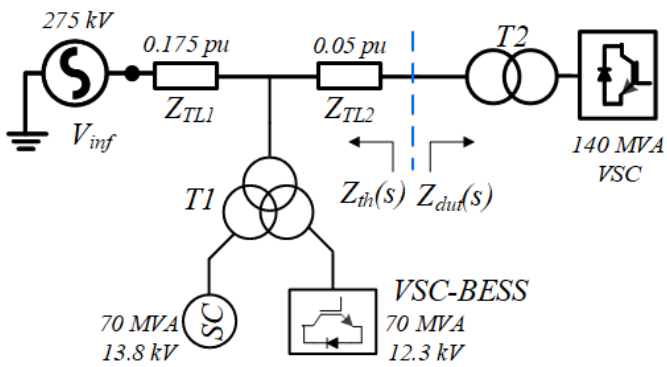

Figure 3.31: Test power System Base power 140 MVA

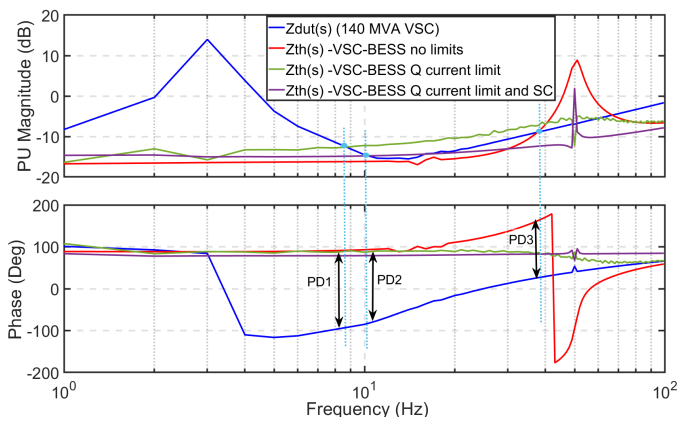

Figure 3.32: Frequency scan of the VSC ($Zdut(s)$) and Thevenin network impedance ($Zth(s)$) with parallel connected GFL and SC combinations at an intermediate bus($Z_{pp}(s)$

)

3.7 Conclusion

This chapter studied the stability impact of GFL on an essential two-machine system composed of SG and GFL in detail. A small-signal model of the two machine system is constructed for stability

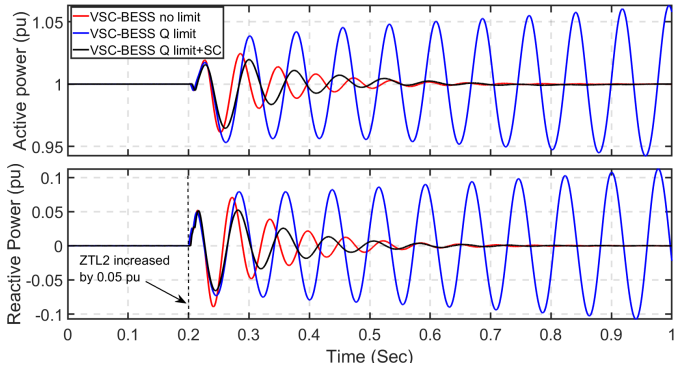

Figure 3.33: Active Power and Reactive power response of 140 MVA VSC when the Z_{TL2} increased by 0.05 pu with parallel connected GFL and SC combinations in the network

analysis. First, the stability implication of the inner loop design of the GFL, which includes the current control and PLL, are investigated. Eigenvalue, impedance analysis, and participation factor evaluation are employed to identify critical eigenvalues in the system with the origin linked to inner loops. It is revealed that the control design of inner loops could potentially give rise to an unstable low-frequency eigenvalue (4-30 Hz). It is shown that a low bandwidth of the voltage feedforward filter in the current controller coupled with low PM in the PLL design is the primary reason for an unstable low-frequency inner loop mode. If the hardware and noise level in the system permits, a high current controller bandwidth and good PM for PLL together with high bandwidth of feed forward filter can mitigate this unstable mode. The detailed design guidelines for the control design of the current control and phase-locked loop to increase the stability margin are presented in this chapter.

The stability impact of the outer active power control and voltage control is also assessed in this chapter. When the grid strength is weak with low SCR, the active power and voltage control is highly coupled and thus can lead to an ill-conditioned system which presents control design challenges. The outer loops in low grid strength scenarios and high power transfer can lead to a low-frequency unstable mode (PV coupling mode). This mode is closely related to the voltage stability of the system assessed using the PV curve. It was discovered that a much faster voltage control loop than a power controller could ensure a more significant stability margin. To that end, this chapter identifies the saturation of the reactive current reference and consequent control mode change of the GFL from active power voltage control to active power -reactive current control could result in instability associated with the voltage stability. Such saturation of the voltage control can also lead to interference with the AVR and SG and gives rise to unstable oscillatory mode. This chapter also investigates the GFL connected at an intermediate bus and the impact of the current reference saturation of this GFL.

Interaction between the GFL connected in the intermediate bus and another GFL connected at the radial network's end is analyzed using an impedance-based approach. It is shown that when a current limit is triggered in a reactive current channel, the GFL impedance experiences an upward jump in the terminal impedance, which will be reflected in the Thevenin impedance of the network seen by the other components in the networks. This upward jump in Thevenin impedance could give rise to the oscillation at the low-frequency range.

CHAPTER 4

Transient Performance of the Grid Following Converter Synchronization Unit

As explained in Chapter 3, GFL synchronizing with ac grid voltage is realized by a phase-locked loop (PLL). Therefore, the optimal transient performance of PLL is important for ensuring that the GFL responds accurately and as necessitated by the grid codes. In this chapter, the performance of PLL during fault scenarios is evaluated. The focus of the chapter is on the PLL types with an additional filtering stage. It is revealed that a conventional SISO model of the PLL is insufficient to capture the full dynamics of the PLL during fault. This chapter develops a (MIMO) linear model that captures the complete PLL dynamics during symmetrical faults for a PLL equipped with any prefilter. In addition, the chapter also augments the PLL performance by a proposed compensator. The chapter is based on [**Pub. A**], with minor changes to fit the framework of this thesis.

4.1 Introduction

With increased GFL penetration in the network the grid codes expect that the GFL resources quickly inject fast fault reactive current to the system to ensure the satisfactory protective relay system operation [84, 85]. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system. Central to the requirement for a fast fault current contribution is accurate detection of the phase of the point of common coupling (PCC) voltage, typically achieved by a phase-locked loop (PLL) based synchronization unit [86]. During the fault event, both the magnitude and phase of the PCC voltage are disturbed, making it challenging to estimate the phase of PCC voltage using PLL. A comprehensive modeling of the PLL is necessary in the fault scenario to design the control parameters to meet the strict time-domain performance requirements, such as a rise time for reactive fault current injection in tens of milliseconds as specified in the grid codes. Several variations of PLL's for power converters were proposed over recent years [87, 88]. Despite the differences in their names, most of them are structurally similar and are derived from a conventional synchronous reference frame PLL (SRF-PLL) shown in Fig. 4.1. These differences between PLL types are mainly due to the different types of filtering incorporated in the PLL. These filtering of the PCC voltages are implemented in mainly three stages: digital filters in the stationary reference frame (prefilter,$PF2(s)$), the digital filters embedded in the PLL control loop (in loop filters,$IF(s)$), and the physical filtering ($PF1(s)$) present due to anti-aliasing filter, as well as transducers and its associated circuits as shown in Fig. 4.1, [87]. Both prefilter and in-loop filters are incorporated in the PLL structure to enhance the disturbance rejection capability of PLL during non-ideal grid voltage conditions, such as in the case

of harmonics and unbalance in the PCC voltages. The classification of the most advanced PLL's is done based on the presence, absence, and types of prefilter and in-loop used in the PLL design. The PLL's with prefilter include, but not limited to, dual second-order generalized integrator based PLL (DSOGI-PLL) [86] multiple complex coefficient filters [86] based PLL both used to extract the positive sequence components of three-phase ac voltage before the PLL control loop. Further, even a simple lowpass or a bandpass filter implemented in the stationary reference frame can also be considered a prefiltered type PLL. Several PLL's and frequency-locked loops (FLL) with prefiltering has been proposed in the literature to estimate the phase of distorted PCC voltages with unbalances in both amplitudes and phase angles [89, 90].

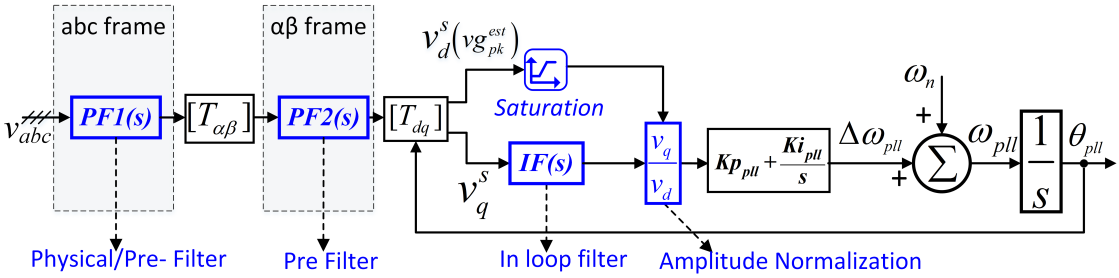

Figure 4.1: Common structure of three Phase SRF-PLL with disturbance rejection capabilities

For PLL controller parameter design, most of the past work utilizes a linear time-invariant single input single output (SISO) PLL model with the phase angle ($\theta_g(t)$) of the PCC voltage as input and its estimated phase angle ($\theta_{pll}(t)$) as its output [91]. Extension of such a model is straightforward for the PLL's with in-loop filters [91, 92]. However, obtaining a SISO model is not a trivial task for a prefiltered PLL since the filtering takes place in a stationary frame with time-varying sinusoidal voltages. When analysis PLL's with sudden large disturbance in voltage magnitude it is important to consider the PCC voltage magnitude change as in input in PLL modelling. An extended SISO model that consider the harmonic components of the PCC voltage as a disturbance input is presented by [92]. While such a model is sufficient to capture PLL dynamics during small disturbances and control design, this chapter shows that for PLL's equipped with additional filters for disturbances and harmonics elimination, the SISO modeling is inadequate. For studying large disturbances like power system faults, a multi-input multi-output (MIMO) dynamic model of the PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs is necessary to improve the modeling and control design. Such a MIMO model of the PLL could also improve synchronization stability assessment accuracy improvement during severe grid faults [93, 94]. Several recent studies have presented linear time-periodic (LTP) MIMO models of specific types of PLL's and frequency-locked loops (FLL). These MIMO models can account for the presence of harmonics and/or imbalance [58, 95]. In [90] modelling and an improvement in transient response and harmonic response for a second-order generalized integrator based FLL is presented. However, these MIMO models are specific to PLL/FLL types and cannot be generalized for prefiltered PLL types. In [96], a generalized method for converting the prefiltered section of the PLL's implemented in the stationary frame to a rotating reference frame is presented. Such a method could be used as the basis for establishing a generalized (MIMO) dynamic model of the prefiltered PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs.

In this chapter, a generalized MIMO model for prefiltered PLL, which captures the complete

dynamics of prefiltered PLL during faults, is proposed. From the developed nonlinear MIMO model, it is readily observable that unlike a PLL with in-loop filters, for the PLL's with prefilters implemented in the stationary frame (including physical filters), there exists a coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. Such a coupling is not a desirable attribute to a PLL as it is intended to only respond to the change in phase of the terminal ac voltage and could result in wrong estimates of frequency and phase during faults. Based on the derived nonlinear MIMO model, a linearized model is developed to aid the controller design. A supplementary control loop is proposed in the chapter to reduce the coupling effect of the instantaneous peak of the ac voltage to the estimated phase. Overall the contributions of the chapter are,

1. Develop a MIMO model of a prefiltered PLL which captures the complete dynamics of prefiltered PLL during faults. The model is useful in enforcing a strict time-domain requirement for converter response during fault cased. Further, the model can be used for converter control design as well as synchronization stability analysis;

2. A supplementary control loop is proposed for a prefiltered PLL, which not only reduces the transients in the estimated phase and frequency during fault but also eliminates the steady-state phase lag introduced by prefilters

The modeling and analysis in the chapter is generalizable for all types of prefiltered PLL. However, for the sake of brevity, the analysis presented in the chapter is restricted to three of the commonly used types of prefilters, (i) PLL with first-order lowpass filter as prefilter (LPF-PLL), (ii) PLL with bandpass filter as prefilter (BPF-PLL), (iii)PLL with DSOGI as prefilter (DSOGI-PLL). Additionally, to show the effectiveness of the proposed model and supplementary control on a cascaded prefilter as an example application of a PLL with both physical filter and a prefilter, a PLL with DSOGI as prefilter and a first-order lowpass filter as a physical filter (LPF-DSOGI-PLL) is also studied in this chapter.

4.2 Overview of PLL operations and Response to Voltage Transients

In SRF-PLL with prefilter is as shown in Fig. 4.1. The three phase instantaneous PCC voltages (v_{abc}) are first filtered and transformed into a rotating reference frame (dq frame) using estimated phase angle θ_{pll}. The q-axis voltage (v_q^s) of the the transformed voltages is then driven to zero in steady-state by a Proportional Integral (PI) controller with a proportional gain Kp_{pll}, and integral gain Ki_{pll}. In steady state, the magnitude of the d-axis voltage (v_d^s) is equal to the magnitude of the input PCC voltage (vg_{pk}), hence the v_d^s is also termed as estimated peak voltage of the PCC voltage (vg_{pk}^{est}). The PLL estimated frequency ω_{pll} is the sum of the nominal frequency (ω_n) and output of the PI controller ($\Delta\omega_{pll}$). A dynamic amplitude normalization is implemented in all the PLL's considered to ensure the loop gain of the PLL remain the same for all magnitude of the grid voltages. The $[T_{\alpha\beta}]$ and $[T_{dq}]$ in Fig. 4.1 are the Clarke (abc to $\alpha\beta$) and park ($\alpha\beta$ to dq) transformation matrices.

$$[T_{\alpha\beta}] = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{4.1}$$

$$[T_{dq}] = \begin{bmatrix} \cos(\theta_{pll}(t)) & \sin(\theta_{pll}(t)) \\ -\sin(\theta_{pll}(t)) & \cos(\theta_{pll}(t)) \end{bmatrix} \tag{4.2}$$

In a PLL, the physical filtering stage ($PF1(s)$) and prefilter stage ($PF2(s)$) could be present in abc frame or $\alpha\beta$ frame. However, most filtering action in the abc frame can also be represented in an equivalent $\alpha\beta$ frame model. For instance, a low pass filter or a bandpass filter implemented in abc frame is similar to the same filters implemented in $\alpha\beta$ frame [96]. Hence the PLL's with a filtering stage (both $PF1(s)$,$PF2(s)$) present in the stationary reference frame (abc and $\alpha\beta$), can be represented in a convenient generalized form as shown in Fig. 4.2 with no distinction between a prefilter or physical filter. The transfer functions $H1(s), H2(2)$ shown in Fig. 4.2, acts on the $\alpha\beta$ frame value of the terminal voltages (v_α, v_β) to give the filtered $\alpha\beta$ frame terminal voltages ($v_{\alpha f}, v_{\beta f}$). The transfer functions $H1(s), H2(2)$ could include

1. The 2×2 MIMO transfer function of a prefilter implemented in $\alpha\beta$ frame, which could include a DSOGI [92], a standard complex coefficient filter (SCCF) [97], or any other prefilter implemented in $\alpha\beta$ frame.

2. $\alpha\beta$ frame equivalent of the filtering action caused due to physical filter or anti-aliasing filter in abc frame.

3. A cascaded combination of the physical filter and prefilter in $\alpha\beta$ frame.

Table 4.1: Transfer functions and parameters of the filters used

Prefilter type	Transfer Function	Parameters
$Bandpass\ prefilter$	$H1(s) = \frac{2\,\omega_n\,s\,\zeta}{s^2+2\,\omega_n\,\zeta\,s+\omega_n}$	$\zeta = 0.707$
	$H2(s) = 0$	$\omega_n = 2\pi 50\ rad/\sec$
$Lowpass\ prefilter$	$H1(s) = \frac{\tau}{s+\tau}$	$\tau = 0.0005$
	$H2(s) = 0$	
$DSOGI\ prefilter$	$H1(s) = \frac{k\,s}{{\omega_n}^2+s^2+2\,\omega_p\,s}$	$\omega_n = 2\pi 50\ rad/\sec$
	$H2(s) = \frac{\omega_n\,k}{{\omega_n}^2+s^2+2\,\omega_p\,s}$	$k = \sqrt{2}$
$Lowpass\ Inloop$	$IF(s) = \frac{\tau}{s+\tau}$	$\tau = 0.0005$

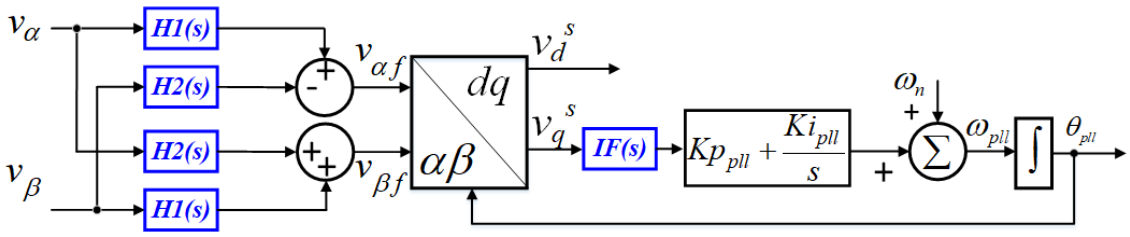

Figure 4.2: Generalized representation of prefiltered SRF PLL

In order to emphasize the main motivation of the chapter, the four types of prefiltered PLL's under consideration; LPF-PLL, BPF-PLL, DSOGI-PLL,LPF-DSOGI-PLL along with a PLL with no prefilter

but a low pass filter placed inside the control loop (LPF-Inloop-PLL), are subjected to symmetrical grid voltage sag to about 0.1 p.u and recovery. The parameters for the prefilters are typical to 50 Hz supply and is shown in Table 4.1. The PLL control parameters Kp_{pll} and Ki_{pll} are designed such that all the PLL's time-domain performances are equal for a change in the terminal voltage phase. The response of the considered PLL's to the sudden dip in PCC voltage is depicted in Fig. 4.3. The symmetrical voltage sag is of magnitude 0.1 p.u lasting for 0.1 seconds and a subsequent recovery to 1 pu, the terminal voltages' phases unchanged for the whole duration.

Ideally, as the name suggests, a PLL is only supposed to respond to a change in the terminal voltage phase. However, as seen from Fig. 4.3, except for the PLL with a filter placed inside the control loop (LPF-inloop-PLL), all the other three PLL's with prefilters show disturbances in the estimated phase ($\Delta\theta_{pll}$) and frequency (ω_{pll}), with varying degree of differences in performance. Moreover, for the case of a low pass filter in the prefilter stage as in LPF-DSOGI-PLL and LPF-PLL, there is also a steady-state phase error of approximately $10°$ as seen in Fig. 4.3. Such responses of the prefiltered PLL during grid faults cannot be explained or accounted for by a conventional linear SISO model. Therefore, to design the PLL's with prefilters and to capture and subsequently reduce the coupling effect of the instantaneous peak voltages and the estimated phase, an improved PLL model has to be developed.

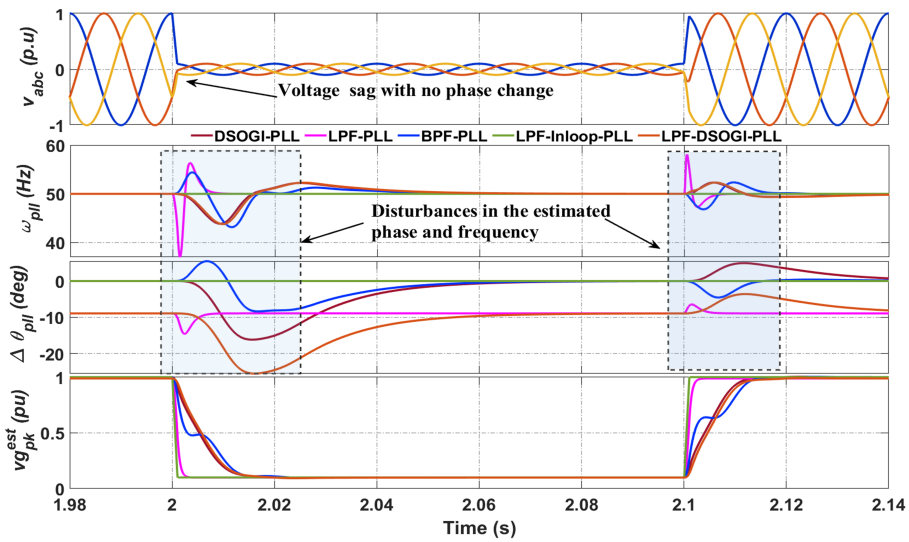

Figure 4.3: Comparative simulation results of different prefiltered and inloop filtered PLL under grid voltage magnitude change while keeping the phase constant

4.3 Phase Locked Loop Modelling

A small signal model of a basic SRF-PLL without filters is well explained in literature [87, 92]. All the variable in the PLL is transformed to rotating refernce frame for ease of analysis due to existence of DC steady state. One must note that the inverter system has two rotating reference frames; a controller d-q frame (dq frame) which is defined by PLL angular velocity ω_{pll} and a system d-q frame (DQ frame) defined by ω_{ref}, which in this chapter is the nominal system frequency ω_n. At steady-state condition, both frames rotate in synchronization, but during small-signal perturbations the frames can rotate at different speeds depending on the PLL's tracked angle and speed. The phasor relationship between the variables defined in DQ and dq domain are depicted

in Fig. 4.4. Assuming the voltages are balanced, the PCC voltage can be represented as a vector $\vec{v}_{abc}$ with a magnitude Vg_{pk} and phase of $\Delta\theta_g$ in DQ frame. The $\Delta\theta_{\text{pll}}$ is the difference in phase of the PLL dq frame and system DQ frame. Henceforth in the chapter, variables with the symbol $\sim$ represents small perturbed form of the respective variables, also variable with appended 0 represents its steady-state value.

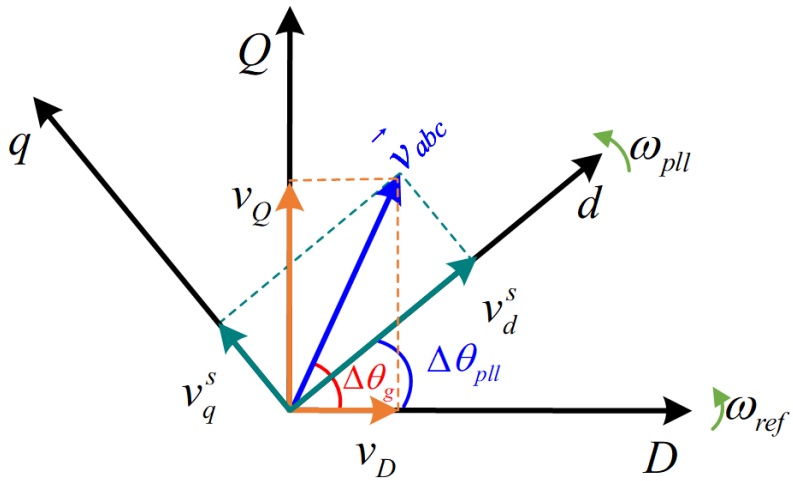

Figure 4.4: Phasor relationship between the variables for SRF-PLL without prefilter

4.3.1 PLL's with only inloop filter (IF(s))

The PLL with only inloop filter without a prefilter does not technically exist because there is almost always a physical prefilter present for signal processing $(PF1(s))$, however if the bandwidth of the prefilters is very high, the dynamics of these can be neglected and approximated as a unity gain. Therefore, among the three possible filtering positions in Fig. 4.1 only $IF(s)$ needs to be considered. Using the phasor diagram shown in Fig. 4.4 and the Fig. 4.1, the linearized model of the three phase PLL with an inloop filter around an operating point Vg_{pk0}, $\Delta\theta_{g0}$ can be derived and is shown in Fig. 4.5. The inputs of this model are $v\tilde{g}_{pk}$ and $\Delta\tilde{\theta}_g$, and outputs are the estimated phase of the terminal voltage ($\Delta\tilde{\theta}_{\text{pll}}$) and $v\tilde{g}_{pk}^{est}$.

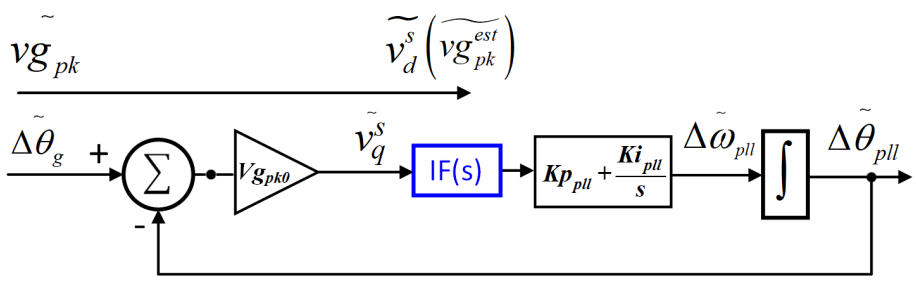

Figure 4.5: Linear model of SRF PLL with an in loop filter

As seen from Fig. 4.5 the linear small signal model of a SRF-PLL with an in loop filter is decoupled for the dynamics of $v\tilde{g}_{pk}$ and $\Delta\tilde{\theta}_g$. The model is simply an extension of the conventional SISO SRF-PLL linear model. The important point to note is that any disturbance in the instantaneous peak voltage will not have an impact on the estimated phase θ_{pll}, this conclusion is also confirmed from the simulation results shown in Fig. 4.3.

Table 4.2: Synchronous frame equivalent transfer functions of $H1(s)$ and $H2(s)$

$Synchronous\ frame\ equivalent\ transfer function$	
$Band\ pass$	
$H1_{DQ}(s)$	$\frac{2\,\omega_n\,\zeta\left(2\,\zeta\,{\omega_n}^3+2\,{\omega_n}^2\,s+2\,\zeta\,\omega_n\,s^2+s^3\right)}{4\,{\omega_n}^4\,\zeta^2+8\,{\omega_n}^3\,s\,\zeta+4\,{\omega_n}^2\,s^2\,\zeta^2+4\,{\omega_n}^2\,s^2+4\,\omega_n\,s^3\,\zeta+s^4}$
$H2_{DQ}(s)$	$-\frac{2\,{\omega_n}^2\,s^2\,\zeta}{4\,{\omega_n}^4\,\zeta^2+8\,{\omega_n}^3\,s\,\zeta+4\,{\omega_n}^2\,s^2\,\zeta^2+4\,{\omega_n}^2\,s^2+4\,\omega_n\,s^3\,\zeta+s^4}$
$Lowpass$	
$H1_{DQ}(s)$	$\frac{\tau\,(s+\tau)}{{\omega_n}^2+s^2+2\,s\,\tau+\tau^2}$
$H2_{DQ}(s)$	$\frac{-\omega_n\,\tau}{{\omega_n}^2+s^2+2\,s\,\tau+\tau^2}$
$DSOGI$	
$H1_{DQ}(s)$	$\frac{k\,\omega_n\left(2\,k\,{\omega_n}^3+4\,{\omega_n}^2\,s+k\,\omega_n\,s^2+s^3\right)}{2\,k^2\,{\omega_n}^4+2\,k^2\,{\omega_n}^2\,s^2+8\,k\,{\omega_n}^3\,s+4\,k\,\omega_n\,s^3+8\,{\omega_n}^2\,s^2+2\,s^4}$
$H2_{DQ}(s)$	$\frac{k^2\,{\omega_n}^3\,s}{2\,k^2\,{\omega_n}^4+2\,k^2\,{\omega_n}^2\,s^2+8\,k\,{\omega_n}^3\,s+4\,k\,\omega_n\,s^3+8\,{\omega_n}^2\,s^2+2\,s^4}$

4.3.2 PLL's with prefilters (PF1(s) and PF2(s))

In the generalized model of prefiltered SRF-PLL is depicted in Fig. 4.2. The major challenge in modelling the prefilter PLL is that the control/filter action on the voltages occurs in stationary reference frame as well as synchronous reference frame. This imposes challenges on developing a linear time invariant model, as there is no dc steady-state in the stationary reference frame which is required for modelling the equations in dq reference frame. The methods shown in [50, 98] is used to transform the prefilters represented in frequency domain ($H1(s), H2(s)$) shown in Fig. 4.2 to its equivalent transfer function ($H1_{DQ}(s), H2_{DQ}(s)$) in the system synchronous rotating reference frame (DQ frame). The synchronous frame equivalent (SFE) transfer function matrix of the prefilter is given by $H_{DQ}(s)$

$$[H_{DQ}(s)] = \begin{bmatrix} H1_{DQ}(s) & -H2_{DQ}(s) \\ H2_{DQ}(s) & H1_{DQ}(s) \end{bmatrix} \tag{4.3}$$

where

$$H1_{DQ}(s) = \frac{H1(s-j\omega_{ref})}{2} + \frac{H1(s+j\omega_{ref})}{2} - j\frac{H2(s-j\omega_{ref})}{2} + j\frac{H2(s+j\omega_{ref})}{2} \tag{4.4}$$

$$H2_{DQ}(s) = j\frac{H1(s-j\omega_{ref})}{2} - j\frac{H1(s+j\omega_{ref})}{2} + \frac{H2(s-j\omega_{ref})}{2} + \frac{H2(s+j\omega_{ref})}{2} \tag{4.5}$$

The elements of SFE transfer funtion matrix of the prefilters considered in the chapter is given in Table. 4.2. For cascaded prefilters such as the LPF-DSOGI-PLL considered in this chapter, the synchronous frame equivalent can be found by first obtaining the individual SFE transfer function matrix for each prefilter separately and then multiplying to get the final SFE transfer funtion matrix.

The variables defined in system DQ frame can be rotated to the control frame (dq frame) using transformation matrix $[T_{\Delta dq}]$, for instance

$$[v_{dq}] = [T_{\Delta dq}][v_{DQ}] \tag{4.6}$$

where

$$[T_{\Delta dq}] = \begin{bmatrix} \cos(\Delta\theta_{pll}(t)) & \sin(\Delta\theta_{pll}(t)) \\ -\sin(\Delta\theta_{pll}(t)) & \cos(\Delta\theta_{pll}(t)) \end{bmatrix} \tag{4.7}$$

The nonlinear model of prefiltered PLL in rotating reference frame by utilizing the SFE transfer funtion matrix is shown in Fig. 4.6, the DQ frame voltage of terminal voltages (v_{DQ}) v_D, v_Q are given as input signals to the DQ frame transfer function of the prefilter. The non linear model has the inputs as terminal voltage phase $\Delta\theta_{\mathrm{g}}$ and instantaneous peak $vg_{pk}(t)$, and outputs are the estimated phase of the terminal voltage $\Delta\theta_{\mathrm{pll}}$ and estimated magnitude vg_{pk}^{est}. This non linear model can also be used to extend the loss of synchronization study power converter dominated power systems [93, 99, 100].

The time domain equation of $v_{DQ}(t)$ and subsequently of $v_{dq}(t)$ (vector of v_d^s, v_q^s) can be written as

$$[v_{DQ}(t)] = \begin{bmatrix} vg_{pk}(t)\cos(\Delta\theta_{\mathrm{g}}(\mathrm{t})) \\ vg_{pk}(t)\sin(\Delta\theta_{\mathrm{g}}(\mathrm{t})) \end{bmatrix} \tag{4.8}$$

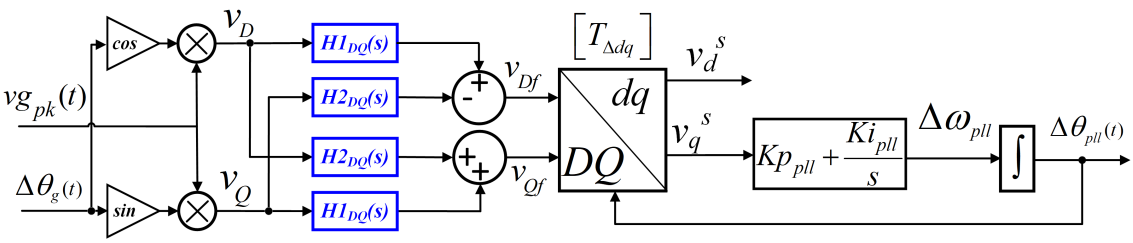

Figure 4.6: Non linear model of a general prefiltered PLL in rotating reference frame

$$[v_{dq}^s(t)] = [T_{\Delta dq}] \cdot [[H_{DQ}(t)] * [v_{DQ}(t)]] \tag{4.9}$$

where the asterisk $*$ denotes the convolution operation, and dot $\cdot$ denotes multiplication. The linearized model can be derived by finding the first order approximation of Eq. (4.9) around an operating point Vg_{pk0}, $\Delta\theta_{g0}$, $\Delta\theta_{pll0}$.

$$\begin{bmatrix} \tilde{v}_d^s & \tilde{v}_q^s \end{bmatrix}^T = [Cl(s)] \begin{bmatrix} \tilde{v}g_{pk} & \Delta\tilde{\theta}_g & \Delta\tilde{\theta}_{pll} \end{bmatrix}^T \tag{4.10}$$

where

$$Cl(s) = \begin{bmatrix} H1_{DQ}(s) & -Vg_{pk0}H2_{DQ}(s) & 0 \\ H1_{DQ}(s) & Vg_{pk0}H2_{DQ}(s) & Vg_{pk0} \end{bmatrix} \tag{4.11}$$

Using (4.10) and the non linear model shown in Fig. 4.6 the linearized model of the prefiltered PLL as shown in Fig. 4.7 can be derived. Unlike a PLL with only inloop filter where $\tilde{v_q}$ was decoupled from $\widetilde{vg_{pk}}$, in prefiltered PLL, $\widetilde{vg_{pk}}$ is coupled to $\tilde{v_q^s}(s)$ via ($H2_{DQ}(s)$) as shown in 4.7. This coupling effect can be significant during the large disturbances in PCC voltage for some PLL's with prefilter, but it is usually ignored in the existing PLL models. It is also important for controller design as the underlying couplings is evident as opposed to a SISO model of the PLL. The MIMO model helps us in designing an efficient controller and thus ensures a better time domain performance, especially when there is a simultaneous large disturbances in both terminal voltage magnitude and phase as in the case of power system faults. The MIMO model also allow us to capture the disturbances in estimated phase of prefiltered PLL's for a symmetrical disturbance in the PCC voltage.

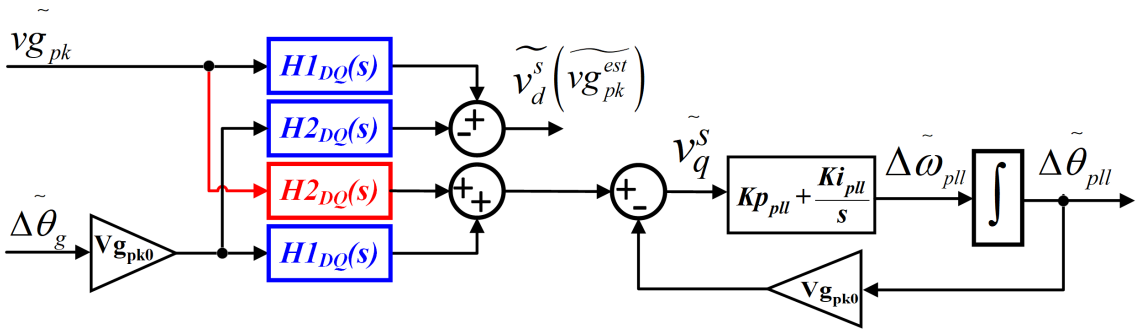

Figure 4.7: Linear model of SRF PLL with pre filter

4.4 Proposed Control to reduce coupling

In this section a supplementary control structure is proposed to reduce the coupling between the phase and instantaneous peak of the terminal voltage. The coupling effect is highlighted in Fig. 4.7, the obvious choice for a perfect decoupling would be to include a inverse based controller which inverts the plant dynamics, which in this case is the transfer function matrix $H_{DQ}(s)$. However, the computational burden associated with such a controller can be extremely high as it involves inverting the MIMO transfer function matrix. Moreover, such controls will also overturn the advantages of using a prefilter such as harmonic. Hence, for practical purpose, a pure inverse based controller may not be desirable in this case.

Based on the insights derived from the linearized model and also from the characteristics of DQ equivalent frequency response of the common prefilters, a compensator of the same order as the respective prefilter transfer functions shown in Table. 4.1 is proposed. The approach followed is to make the forward path gain from $\tilde{v}g_{pk}$ to the input of the PI control to zero, which is achieved with the addition of a compensator ($\frac{H2_{DQ}(s)}{H1_{DQ}(s)}$) as shown in Fig. 4.8. The compensator is realizable for any filter type as long as the filter types have no non minimum phase behaviour. The decoupling effect of the addition of compensator can be cleary seen from Fig. 4.9, which depicts the linearized model of the PLL with prefilter. The compensator types for the prefilters considered in this chapter is shown in Table. 4.3. To test the effectiveness of the compensator, the study shown in Fig. 4.3 is repeated with added compensator, the parameters of the prefilter remained the same as in Table. 4.1. As anticipated, the disturbance in peak voltage did not have any effect on the estimated phase and frequency of the PLL with prefilter as shown in Fig. 4.10. Furthermore, the steady-state phase offset caused due to a first order low pass filter as the prefilter is also eliminated by the use of compensator.

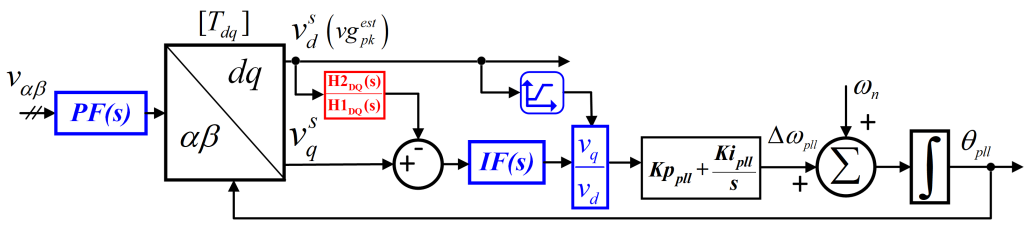

Figure 4.8: The general implementation of compensator for a prefiltered PLL

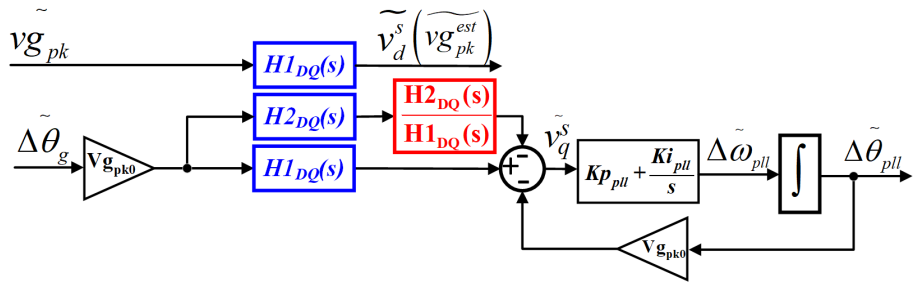

Figure 4.9: The simplified linear model of prefiltered PLL including the proposed compensator

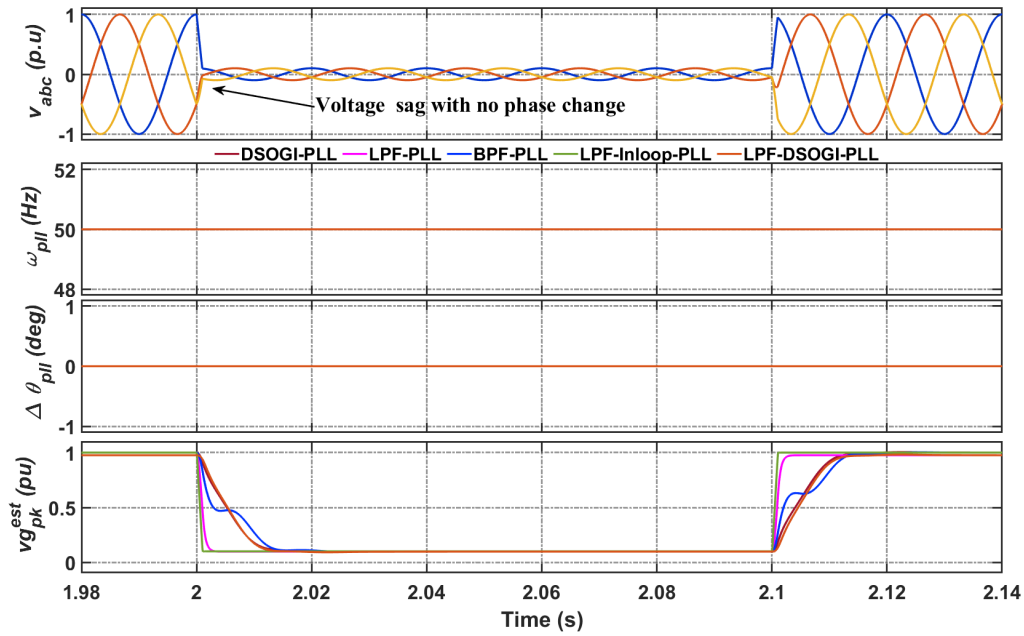

Figure 4.10: Simulation results of prefiltered PLL's with the proposed supplimentay compensator for grid voltage magnitude change while keeping the phase constant

The chapter's focus is on PLL response and compensation for balanced voltage dips and phase jump. Nevertheless, the feasibility of the proposed compensator is also investigated in an unbalanced sag case. Among the considered PLL, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the negative sequence voltage generated by unbalanced sag [87]. Therefore the results for unbalanced cases are only demonstrated on those two PLL's against PCC volage sag typical for Double line to ground fault while keeping the phase constant. The results of the unbalanced sag study is shown in Fig. 4.11. It can be seen that the compensation reduces the disturbance in estimated phase and frequency of the PLL as well as it removes any steady state error caused due to low pass filter in LPF-DSOGI-PLL.

The procedure for obtaining the compensator for any prefiltered PLL is summarized below for readers convenience

1. Convert to generalized representation as in Fig. 4.2 and obtain transfer functions $H1(s)$, $H2(s)$.
2. Obtain the (SFE) transfer function matrix components $H1_{DQ}(s)$, $H2_{DQ}(s)$ using algebraic combination of frequency shifted $H1(s)$, $H2(s)$ as shown in eqn (4.4) and (4.5)

3. The compensator is $\frac{H2_{DQ}(s)}{H1_{DQ}(s)}$ and its generalized implementation is shown in Fig. 4.8.

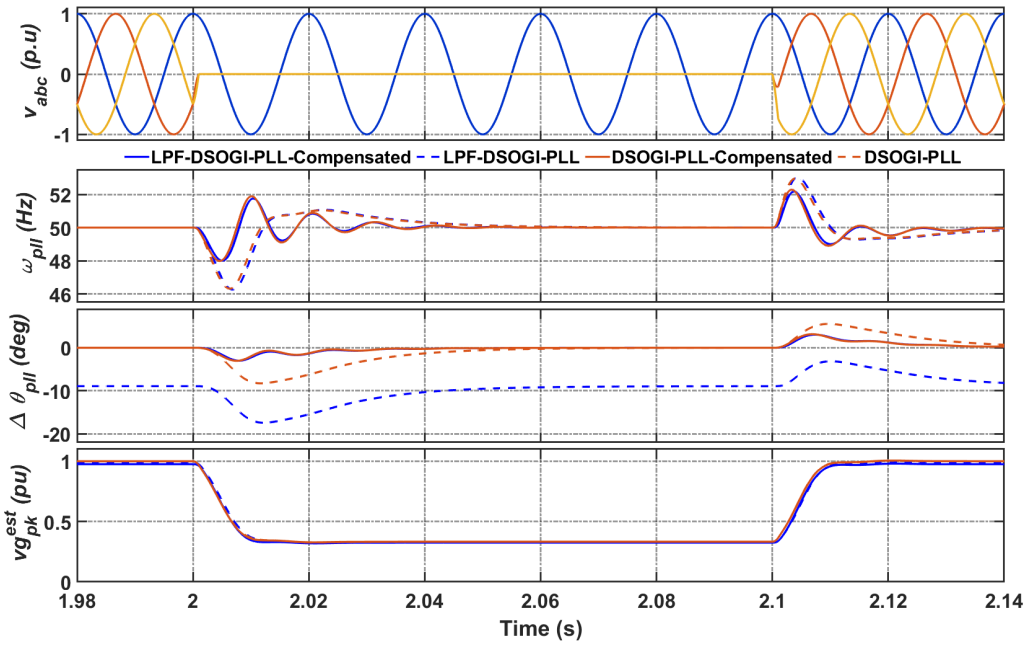

Figure 4.11: Simulation results of DSOGI-PLL and LPF-DSOGI-PLL with and without compensation for unbalanced grid voltage sag while keeping the phase constant

Table 4.3: The transfer functions of the proposed compensators

$Prefilter$Type	$Compensator$
$Bandpass$	$-\frac{\omega_n\ s^2}{2\,\zeta\,\omega_n{}^3+2\,\omega_n{}^2\ s+2\,\zeta\,\omega_n\ s^2+s^3}$
$Lowpass$	$-\frac{\omega_n}{s+\tau}$
$DSOGI$	$\frac{k\,\omega_n{}^2\ s}{2\,k\,\omega_n{}^3+4\,\omega_n{}^2\ s+k\,\omega_n\ s^2+s^3}$

4.5 SIMULATION RESULTS

A simulation study of the three prefilter types and its compensation was carried out to verify the advantages of the proposed compensation. To ensure a fair design, all the three PLL's were designed to have 2 cycle settling time while limiting the overshoot to 10%. The design was carried out using the linear model derived in the previous section. The control parameters of a PLL type was retained when compensation was added. It should be noted that, as the PLLs as the PLL input voltage magnitude coupling is eliminated with the proposed compensator, control performance can be improved. To simulate symmetrical fault, we considered a positive sequence voltage sag to 0.3 p.u for 100 ms duration accompanied by a positive phase jump of $15°$. The positive effects of compensation is evident from the results shown in Fig. 4.12. The net error in estimated angle of the PLL and the actual angle ($\Delta\theta_{error}$=$\theta_{pll} - \theta_g$) is reduced. To further quantify the impact of compensation, a normalized root mean square (NRMS) of $\Delta\theta_{error}$ is computed for all the PLL

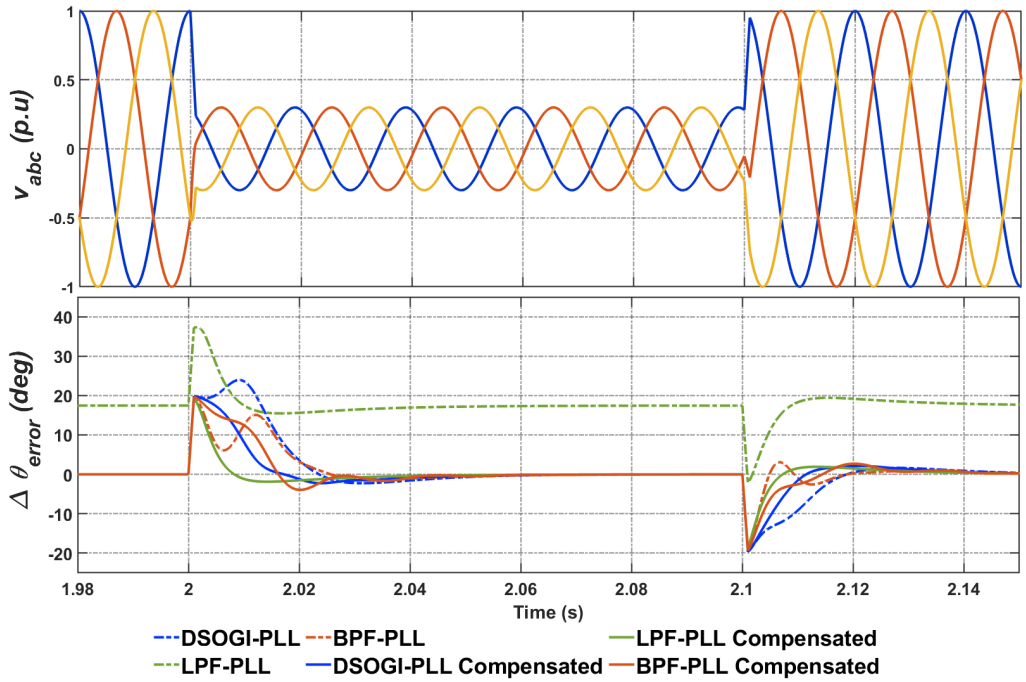

Figure 4.12: Simulation results for a dip in positive sequence voltage magnitude for 100 ms duration accompanied by a positive phase jump of $15°$

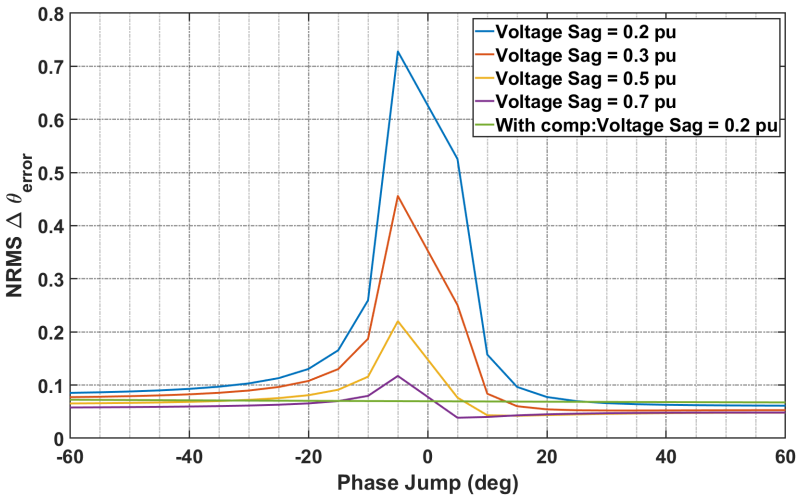

Figure 4.13: NRMS of $\Delta\theta_{error}(deg)$ during variable voltage sag and simultaneos phase jump for 100 ms period for BPF PLL

types considered with varying level of voltage dip and phase jump. The NRMS of $\Delta\theta_{error}$ for a PLL under a input phase jump of θ_{fault} during the period of fault related dynamics is defined by

$$NRMS\Delta\theta_{error} = \frac{\sqrt{\frac{1}{T2-T1}\int_{T1}^{T2}\Delta\theta_{error}(t)^2}}{\overline{\theta_{fault}}} \tag{4.12}$$

where T1 is the fault initiation time and T2 is two cycles after the fault clearing time when all dynamics of induced by the fault is settled. The NRMS of $\Delta\theta_{error}$ is computed by running the time

domain simulation for a dip in positive sequence voltages for a period of 100 ms, a phase jump is also accompanied with this dip. It can be seen from Fig. 4.13- 4.15 that the net error in estimated phase for all uncompensated PLL's is dependent on the magnitude of dip in voltage where as a compensation makes NRMS of $\Delta\theta_{error}$ independent of the voltage dip. The NRMS is not relevant for LPF prefilter as the phase shift introduced is constant regardless of the dip in voltage.

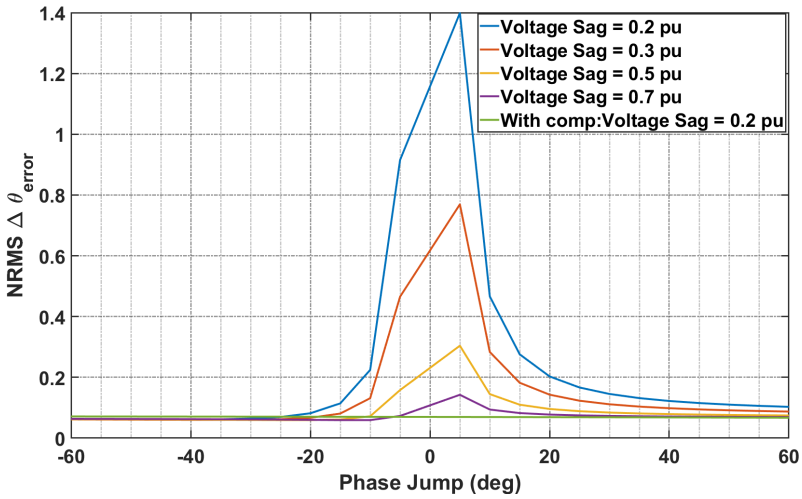

Figure 4.14: NRMS of $\Delta\theta_{error}(deg)$d during variable voltage sag and simultaneous phase jump for 100 ms period for DSOGI PLL

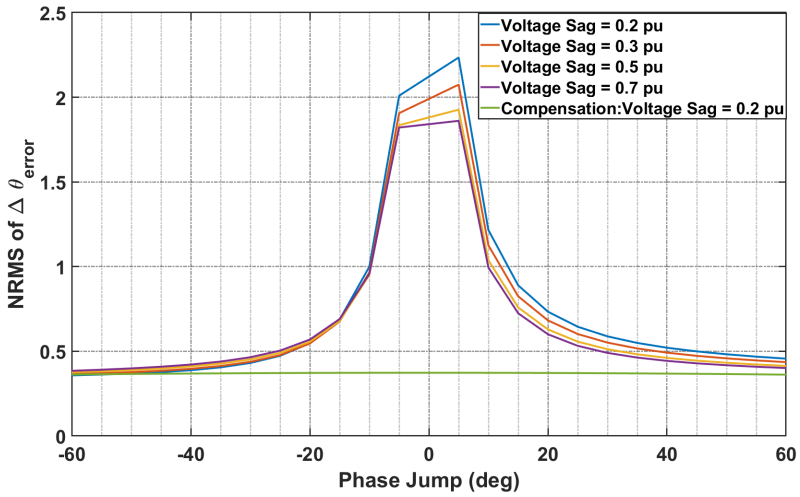

Figure 4.15: NRMS of $\Delta\theta_{error}(deg)$d during variable voltage sag and simultaneous phase jump for 100 ms period for LPF-DSOGI-PLL

4.6 Power Hardware In The Loop Results

The proposed compensation and MIMO modeling can be applied in any grid-connected converter system which employs a prefiltered PLL for grid frequency and phase detection for protection and control. One of the applications where the advantage of the PLL compensation is inherently visible is to enable fast fault current injection in GFL effectively. The grid codes expect that the PE resources quickly inject as much reactive current to the system to ensure the satisfactory protective

relay system operation [84, 85]. The protection system in the high voltage grid requires a sufficient amplitude of fault current in the first 20-30 ms after the fault to operate correctly. Further, the fault level contribution from PEIPS (PE connected equipment) mitigates the severity of maximum voltage depression seen by other assets (especially more distant from the fault). It can prevent tripping due to under-voltage protection and help keep the power system stable. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system.

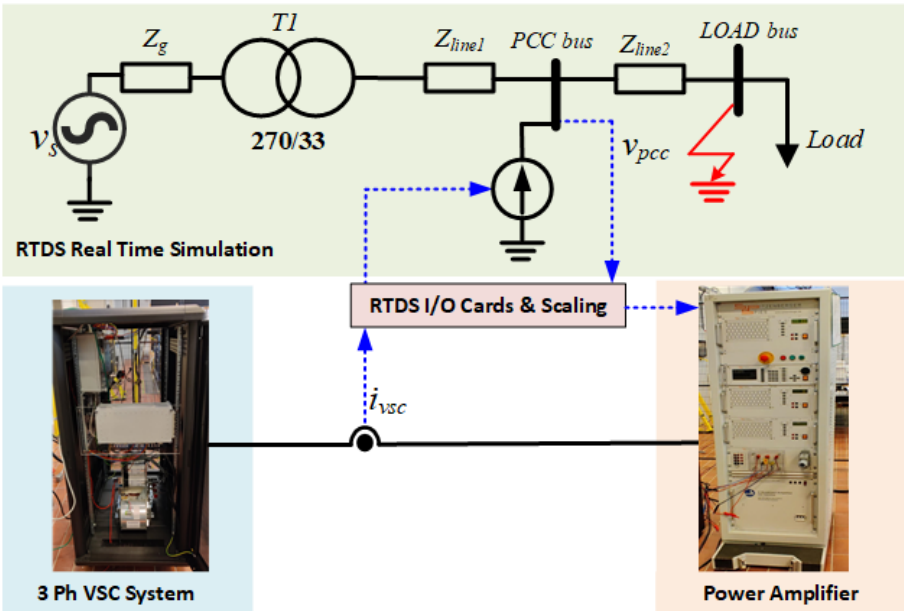

Figure 4.16: Power hardware in the loop test

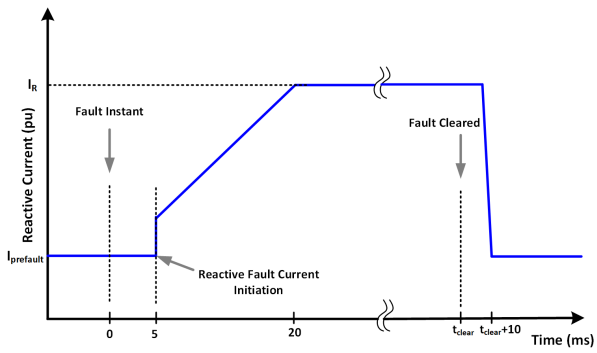

Figure 4.17: The positive sequence fault current reference

The advantages of using proposed compensation for prefiltered PLL is confirmed through power hardware in the loop (PHIL) simulation. The PHIL test setup is shown in Fig. 4.16. The setup includes a simplified power system model implemented in Real-Time Digital Simulator (RTDS), RTDS I/O cards, two-level VSC hardware which is a SEMIKRON SkiiP stack with inductive filter, and current and voltage sensors, a 2.5 kVA SPITZENBERGER & SPIES PAS 2500 linear amplifier. The VSC switching frequency is set to 10 kHz, and the inductive filter for the VSC stack is 8 mH. The PHIL interface is by ITM algorithm as explained in Chapter. 2.The current feedback signal is

Table 4.4: PHIL Scaling for the VSC hardware

Symbol	Description	Physical Value	Scaled to Simulation
V_{vsc}	Amplifier voltage	100 V	33kV
I_{vsc}	VSC Current	7A	150 A
P_{vsc}	VSC power	2 kVA	5 MVA

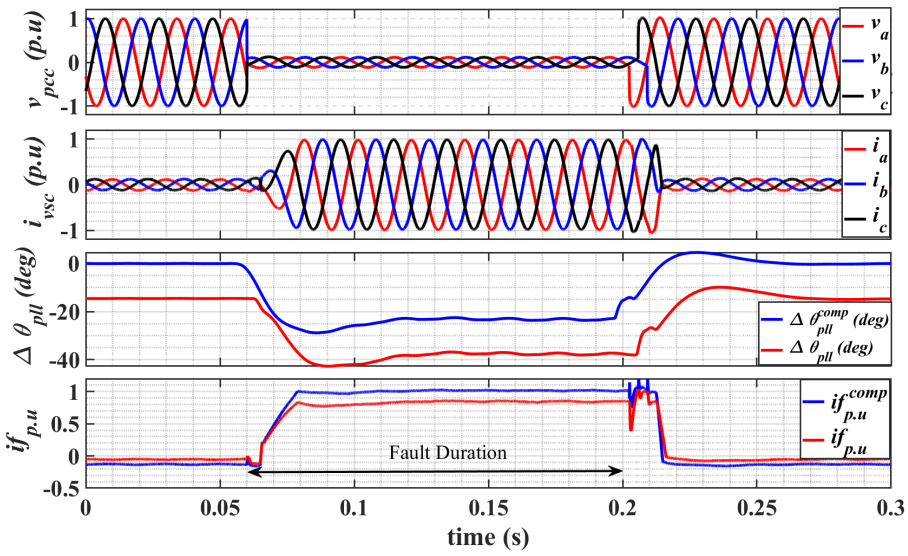

Figure 4.18: Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a low pass filter as prefilter and its compensation

conditioned with a first order low pass filter with a time constant of 250 μs to eliminate noise and ensure the PHIL simulation's stability.

The VSC control system, including the current control and the PLL's discussed in the chapter and their compensation strategies, are implemented on a FPGA based digital controller from National Instruments (NI). The PLL's are set to track the amplifier voltage phase, which is the simulated PCC bus's scaled voltage. The sampling time for the control loop is 40 μs. The controller is discretized using the trapezoidal method. The fault reactive current reference is as shown in Fig. 4.17. The reactive reference fault current is initiated 5 ms after the fault instant. The reference rate is limited to 1 pu in a cycle during the fault current initiation stage. The PLL compensation performance is then evaluated first for a symmetrical fault with a fault impedance of 0.2 ohm at the load bus. The VSC performance with and without compensation for balanced fault is shown in Fig. 4.18-4.20. All the plots captured in the NI controller and RTDS interface is exported to MATLAB and replotted for enhanced clarity. The plots for three-phase PCC voltage and the injected three-phase current is shown only for compensated case. The fault reactive current at the PCC without compensator($if_{p.u}$) and with compensator ($if_{p.u}^{comp}$) are found by scaling the reactive power measured at the PCC with the PCC voltage and dividing by base current (150 A) in real-time simulation. The PLL estimated phase of the terminal voltage with and without compensator $\Delta\theta_{pll}, \Delta\theta_{pll}^{comp}$ are captured in NI

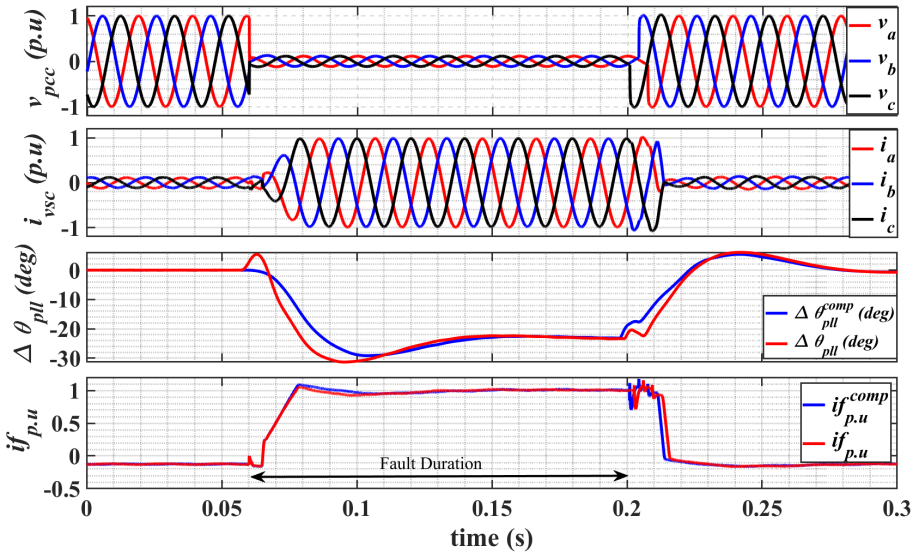

Figure 4.19: Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a 50 Hz BPF prefilter and compensation

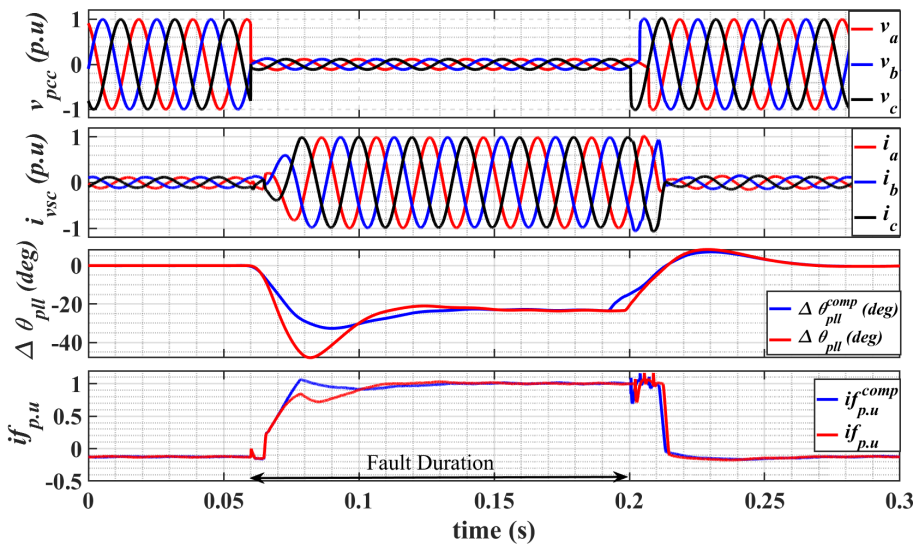

Figure 4.20: Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a DSOGI prefilter and compensation

controller.

Fig. 4.18, shows the VSC's response for balanced fault equipped with a fist order low pass filter, with a time constant of 1 ms. The first order low pass filter, albeit with a low time constant, introduces a phase delay of $17.4\,\mathrm{deg}$ at the fundamental frequency. This open-loop delay also results in a difference in the required reactive current injected and the measured reactive current at the PCC bus, as depicted in Fig. 4.18. The open-loop delay and the resulting difference in fault current are eliminated using the proposed PLL compensation. Fig. 4.19 and Fig. 4.20 depicts VSC's balanced fault response with BPF and DSOGI prefilter as well as the response with proposed compensation. The reactive current injected in the prefilter compensated cases are closer to the reference reactive current because the compensation decouples the dynamics of voltage magnitude

from the measured phase.

Among the PLL's considered in the chapter, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the negative sequence voltage generated by unbalanced sag [87]. Therefore the results for unbalanced sag cases are only demonstrated on those two PLL's against Double line to ground fault at the load bus. During unbalanced fault, a balanced reactive current injection strategy is utilized in this chapter, the positive sequence reactive fault current reference is as shown in Fig. 4.17. Fig. 4.21 shows the VSC's output with DSOGI-PLL during double line to ground fault. It can be seen that the compensation reduces the disturbance in the estimated PLL phase (θ_{pll}). However, the difference between the estimated phases for compensated and uncompensated case is not significant in this case. Therefore the injected reactive current during compensated and uncompensated cases are similar. Fig. 4.22 depicts the results of the VSC with LPF-DSOGI-PLL under double line to ground fault. The low pass filter in the LPF-DSOGI-PLL introduces a phase delay, which is compensated with the use of the proposed compensator. Therefore the reactive current injected in the prefilter compensated cases are closer to the reactive reference current and better cater to the grid requirements.

This application example of reactive fault current injection by VSC demonstrates the advantage of the proposed compensation.

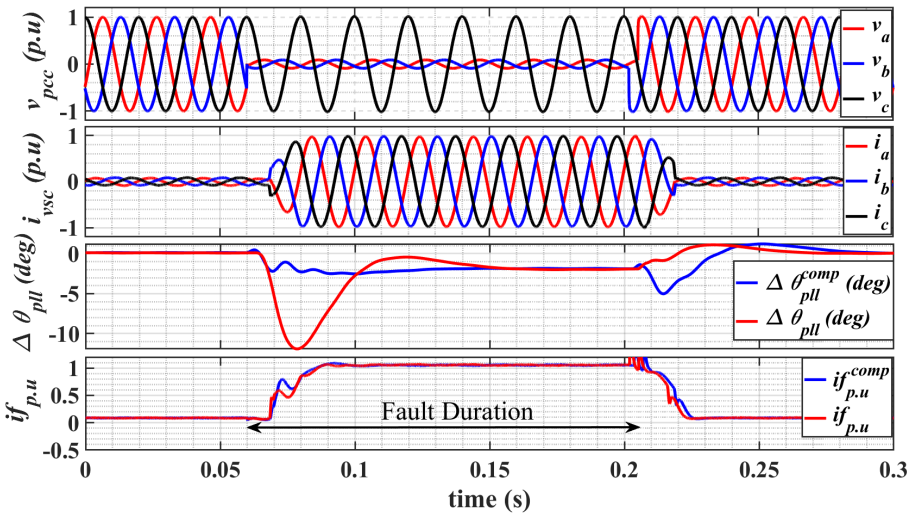

Figure 4.21: Results from PHIL study of the VSC under under double line to ground fault case, for a PLL with a DSOGI prefilter and compensation

4.7 Conclusion

The fast detection of the PCC voltage phase is necessary for GFL to comply with reactive current injection requirements during a fault. It is well known that the three-phase balanced ac voltages can be represented by two instantaneous quantities, namely, the peak of the voltages and its phase angle. During symmetrical fault, there could be large disturbance in both these quantities. In this chapter, it is shown that during a fault in the power system, the traditionally used SISO model cannot capture the complete dynamics of the PLL with a prefiltering stage. The chapter proposes a non-linear MIMO model of a general prefiltered PLL, which during a power system fault more accurately captures the transients of prefiltered PLL. The developed non-linear model

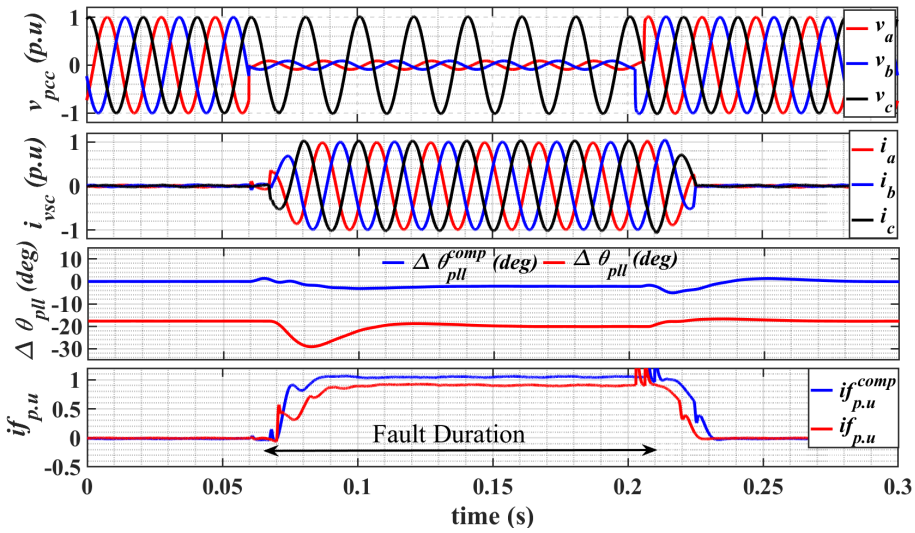

Figure 4.22: Results from PHIL study of the VSC under double line to ground fault case, for a PLL with a cascaded LPF and DSOGI prefilter and compensation

of the prefiltered PLL captures the undesirable coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. The chapter proposes a compensator to reduce this coupling, and the prefiltered PLL is made to act only on changes in the phase of PCC voltage. The proposed compensator is demonstrated with three commonly used prefiltered PLL's and on a cascaded prefilter case to show the effectiveness. The proposed control ensures an accurate current phase control and injection during faults to fulfill fault ride-through requirements.

Part II

Grid Forming Converter

CHAPTER 5

Grid Forming Control: Stability Analysis

This chapter presents the stability evaluation of the GFC. The focus of the small studies is on the inner loops of the GFC. Multiple realizations of GFC exist in the literature, differed based on the type of inner loops present in the GFC. GFC has a near voltage source behind an impedance characteristic for the response to grid events. The three GFC structures based on the inner loop realization, 1) GFC with cascaded voltage and current control, 2) with inner current control, 3) with no inner loop, are chosen for the comparison. The stability analysis using the eigenvalue and impedance approaches revealed that the inner loops for high power converters switching at low frequency can negatively impact the stability and response quality of the GFC. The chapter also identifies potential interaction with SG and GFC due to GFC inner loops. The chapter is based on [**Pub. C**], with minor changes to fit the framework of this thesis.

5.1 Introduction

One of the methods which can potentially help addressing the challenges for the large scale integration of renewable sources, is to replace some of the grid following inverters with inverters operating as a voltage source that electrically it mimics the behaviour of a synchronous generator [26, 28–32]. This type of inverter is called Grid Forming Converter (GFC) or Virtual Synchronous Machine (VSM). The Ref. [34, 101] have shown that RES penetration limit could be potentially raised to 100% by deploying sufficient GFC in the transmission system. The advantages of Grid forming control in terms of inertial support has been demonstrated in wind park and battery energy storage system in MW level projects [102–104].

In one of the first and latest attempts to define the requirements for a GFC, the UK system operator, National Grid, came up with the following requirements [44].

- Behave as a voltage source behind a constant Thevenin impedance in the frequency range of 5 Hz - 1 kHz.
- Instantaneous response for faults and load changes
- Operate as a sink/source for harmonics and unbalance current.

It is expected that the requirements from other utilities will be also similar[41]. The requirement of GFC to behave as a voltage source behind a constant Thevenin impedance in the frequency range of 5Hz-1kHz is for the following reasons [41, 105],

- It allows a higher fidelity for aggregated and RMS models used in system studies.

- It prevents the adverse control interaction in a wide frequency range thereby highest possible stability in the higher frequency range.

Multiple studies classified the GFC's based on the characteristics of outer control loop (the inertia emulation loop) design and have compared their performance against each other [30, 106–108]. Yet another way to classify the GFC is based on the inner control loop (current management) structures, where three common topologies based on different inner loop designs have been widely reported in the literature (i) Without any inner loop current control, (ii) with inner loop current control, (iii) With inner current control and cascaded voltage control. There are opposing arguments presented in literature about the benefits of different topologies. Some studies recommended that inner loop controllers such as valve current controller and PCC voltage controllers are required as the power electronic converters are sensitive to disturbances, and it is easier to implement the current limits on converters with inner loops. Furthermore, the inner loops can provide additional damping for the filters [109, 110]. Whereas, the other studies mentioned that inner controller loops are not recommended, because (i) it can impair the instantaneous response time of the GFC (ii) the presence of controller could cause undesirable controller interactions and thus unstable operation [29]. Furthermore, some latest studies conclude that an increase in grid impedance is better for the stability of the GFC with cascaded voltage control which is in contrast to the behaviour of an SG or an ideal GFC [110–112]. As opposing arguments are presented in literature, a detailed comparative analysis of various GFC topology are required.

Thus this chapter presents a detailed analysis of the three topologies, supplemented by detailed small-signal and time domain analysis of the three different controls. The results of the comparison provide better understanding of the effects of different inner loops. The main contributions of this chapter are as follows,

- Small signal analysis of different controls to identify the impact of GFC impact on system stability.
- Passivity analysis to find the impedance behaviour for frequency range of 5Hz-1kHz as required by National Grid requirements.
- The impact of GFC inner loop on the electromechanical mode of the SG is investigated
- Detailed time domain analysis to compare the performance and GFC's ability to provide instantaneous response for faults and load changes.

5.2 System Description

Fundamentally, a GFC should behave like a voltage source behind an impedance. The voltage amplitude of a GFC is determined by a droop-based reactive power loop. The phase angle of the voltage is set by the inertia loop. The GFC currently is predominantly realized by three inner control methods, which are classified based on the necessity of inner control loops in maintaining the voltage source characteristics.

- GFC structure implemented without any inner current or voltage control and transient and steady state virtual impedance as shown in Fig. 5.1 [28, 29, 45, 54, 113]

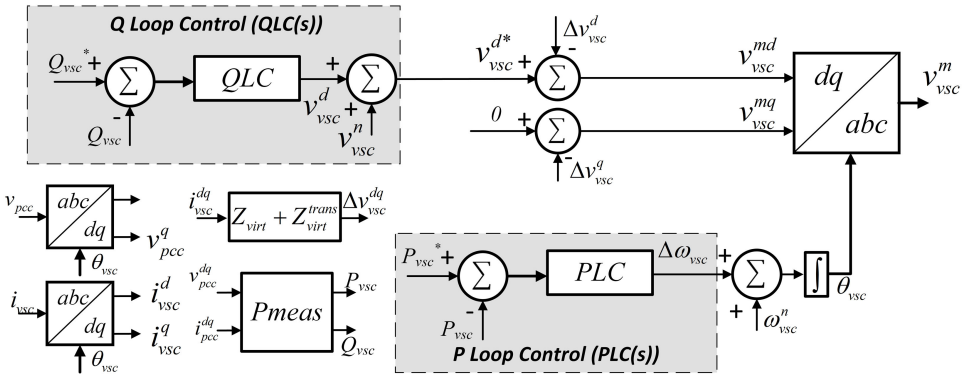

Figure 5.1: General Control System of GFC without an inner loop

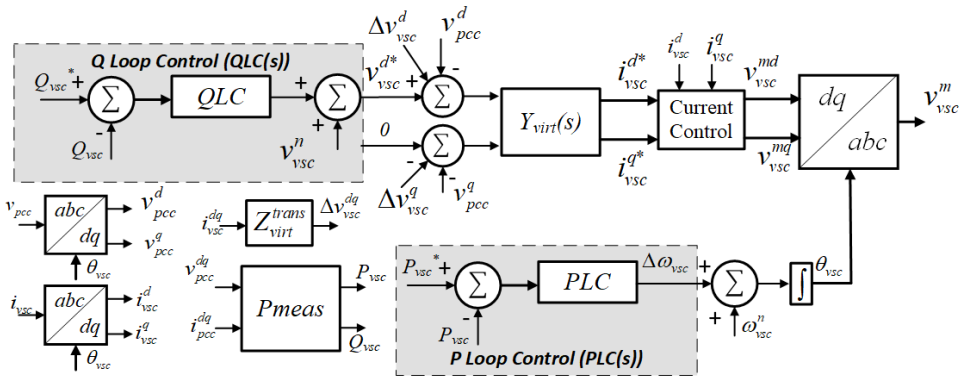

Figure 5.2: General Control System of GFC with current control inner loop and virtual admittance

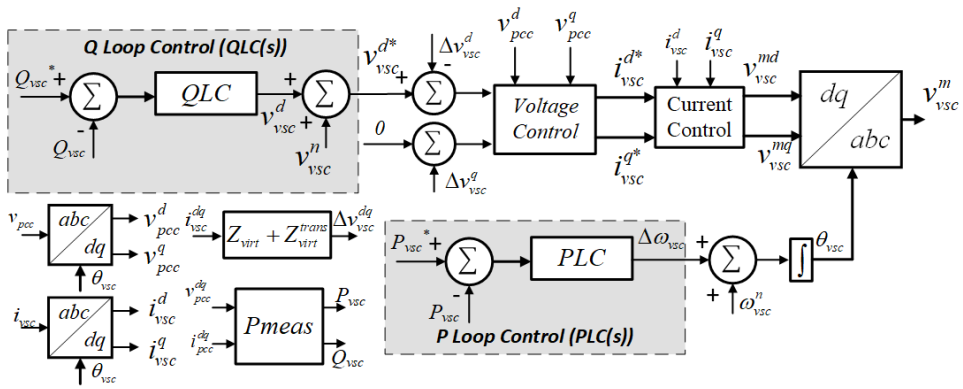

Figure 5.3: General Control System of GFC with cascaded voltage and current control inner loop

- GFC structure implemented with an inner current control and transient virtual impedance, with the current references generated by a virtual dynamic admittance as shown in Fig. 5.2 [57, 109, 114–116]

- GFC structure implemented with cascaded voltage and current control and transient and steady state virtual impedance as shown in Fig. 5.3 [56, 116–119]

A two-source model, as shown in Fig. 5.4 consisting of an SG , GFC, transmission line (Z_{TL1},Z_{TL2}),

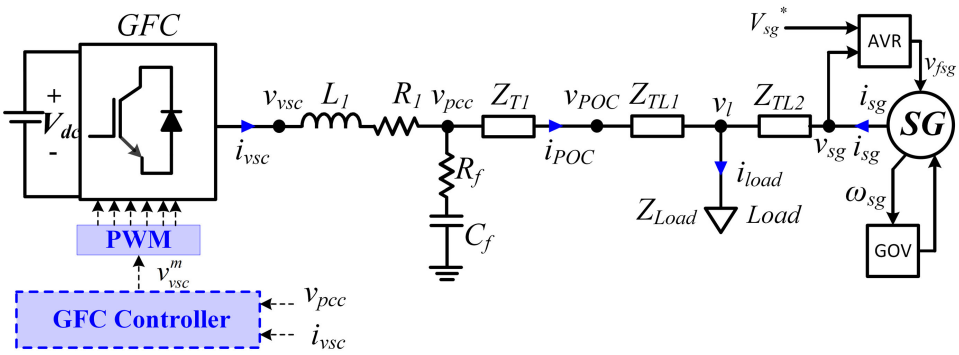

Figure 5.4: Simplified one-line diagram of studied system

load(Z_{Load}) and transformer (Z_{L1}) is the system used to study in this chapter. This system is sufficient enough to capture the dynamic interaction between an SG and GFC while allowing to draw definite conclusions [52]. The GFC filter is modelled by a reactor $L1$, and its loss resistance $R1$, and capacitance filter C_f and damping resistor Rf.

The network model includes passive network impedances, filters, transformers and the load modelled as a resistance. The transformer and network impedance is modelled as RL equivalent. For the purpose of small signal analysis the full system is modelled in rotating reference frame. The network, including the filter reactor, capacitance, load, and the grid impedance, is modeled in D-Q frame, which is defined by the speed of the synchronous machine and is aligned with the swing bus terminal voltage (v_{sg}). The VSC is modelled in a d-q frame (d-q frame) defined by the VSC's power loop output ω_{vsc}.

In the rest of the chapter, all lowercase variables with an appended superscript of D or Q represent the D or Q component of the original parameter defined in the D-Q frame. Whereas all lowercase variables with an appended superscript of d or q represent the d or q component of the actual parameter described in d-q frame. For instance, i_{vsc}^D represent the direct axis component of the VSC current in DQ frame. Variable superscripted with d-q or DQ are variable vectors of the direct and quadrature frame original parameters represented in the dq or the DQ frame, depending on the superscript. Also, variable with appended 0 represents the steady-state value of the parameter.

A commonly used four winding electrical network representation of a salient pole synchronous machine [33], along with a simplified automatic voltage regulator (AVR) and speed Governor (GOV) used for the study. The simplified AVR model consists of cascaded PI control and a low pass filter which forms the excitation system model.

$$G_{AVR} = \frac{Kp_{AVR}s + Ki_{AVR}}{s} * \frac{1}{1 + sT_{AVR}} \tag{5.1}$$

where T_{AVR} is the time constant. The simplified governor is realized by a simplified model emulating a first order response with a f-p droop.

$$G_{gov} = \frac{1}{R} * \frac{1}{1 + sT_{gov}} \tag{5.2}$$

where R is the p-f droop expressed in p.u.

In this study, it is chosen to be same as that of GFC at 0.05 p.u.

5.3 GFC control system and small signal modelling

The GFC control structures analysed in this chapter is shown in Fig. 5.1-5.3. The converter control is implemented in the reference frame (d-q frame) defined by ω_{vsc} (dq). Therefore, in all the GFC structures, the voltage and current parameters are first transformed into (d-q frame) using a frame transformation matrix T_{vsc}. All the transformation blocks, active and reactive power loops and power measurement blocks are common for the three GFC types are discussed in this section. The developed small signal models of the three types of GFC's considered in the chapter is also presented in this section.

5.3.1 GFC control system components

The control components of the GFC controls and their linear models are described below.

Reactive power loop, Q loop control (QLC(s))

The GFC are voltage sources with a nominal voltage of v_{vsc}^{n}. A reactive power slope, $Kslope$ is employed for steady state reactive power sharing.

$$QLC = Kslope * \frac{1}{1 + sT_{QLC}} \tag{5.3}$$

A typical value of 5% is chosen for $Kslope$ and 0.5 seconds time constant is chosen for reactive power loop parameters.

Active power loop, P loop control (PLC(s))

The active power control emulates the SG's electromechanical behavior. The implementation for the power loop controller could vary substantially depending on the amount of damping and inertia output required from the GFC [120]. For instance, the active power controller can be a simple gain to provide response similar to a a conventional P-f droop, or a second order function to mimic inertial constant of a synchronous machine. The active power controller is realised a cascaded combination of gain and low pass filter as given in 5.4, which mimics the swing equation of a synchronous machine. The inertia constant and droop gain are set as 6s and 5% respectively in this chapter.

$$PLC = R * \omega_b * \frac{1}{1 + sT_{inert}} \tag{5.4}$$

where are R is the P-f droop represented in p.u with a typical value of 0.05, and ω_b is the base frequency in rad/sec, and emulated inertial constant can be written as

$$H = \frac{T_{inert}}{R} \tag{5.5}$$

Virtual impedance and transient virtual impedance ($Z_{virt}, Z_{virt}^{trans}$)

The Virtual impedance and transient virtual impedance ($Z_{virt}, Z_{virt}^{trans}$) is applicable for GFC without inner loop as shown in Fig. 5.1 and for GFC with cascased control shown in Fig. 5.3. The virtual impedance block emulates the static voltage drop across a resistive and inductive circuit. The transient virtual impedance ,Z_{virt}^{trans}, realized by a high pass filtered GDC dq current, is typically resistive to provide enough damping for the network resonance modes [26]. The high pass filter cutoff frequency should cover most of the sub-synchronous frequencies to eliminate the network

resonance modes. The combined realization of virtual and transient virtual impedance are shown in Eq. (5.6).

$$\Delta v_{vsc}^{dq} = \underbrace{(R_{virt} + j\omega_b L_{virt})}_{Z_{virt}} i_{vsc}^{dq} + \underbrace{(R_{virt}^{trans} * H_{hp}(s)}_{Z_{virt}^{trans}} i_{vsc}^{dq} \tag{5.6}$$

where v_{vsc}^{dq}, and i_{vsc}^{dq} are the voltage and current at the inverter terminals. $H_{hp}(s)$ is the high pass filter represented as

$$H_{hp}(s) = \frac{s\tau_{hp}}{(1 + s\tau_{hp})} \tag{5.7}$$

The parameters of the virtual impedances are different for the case with cascaded inner control and GFC without inner loop control, because for the GFC with cascaded case the voltage is controlled at the PCC and for no inner loop case the voltage is controlled at the converter terminal.

Virtual admittance ($Y_{virt}(s)$)

The virtual admittance is utilized in the GFC control with only inner loop as shown in Fig. 5.2. The virtual admittance is used to create the current references from the terminal voltage and PCC voltage as shown in (5.8)

$$i_{vsc}^{dq*} = \frac{v_{vsc}^{dq} - v_{pcc}^{dq}}{(R_{virt} + sL_{virt} + j\omega L_{virt})} \tag{5.8}$$

where v_{pcc}^{dq} is the pcc voltage of the GFC.

Current controller

A decoupled dq current control as shown in Fig.5.5 is utilized in both GFC with current control and GFC with cascaded control.

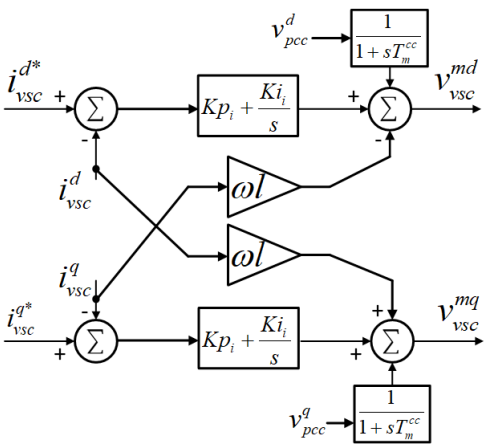

Figure 5.5: Decoupled dq current controller

The control is implemented in dq frame, T_m^{cc} is the time constant of the feed forward filter, the decouple term ωl is given in (5.9).

$$\omega l = \omega_{ref}(L_1) \tag{5.9}$$

Decoupled voltage controller

The decoupled voltage controller is implemented for the GFC with cascaded control loops, as shown in Fig. 5.6

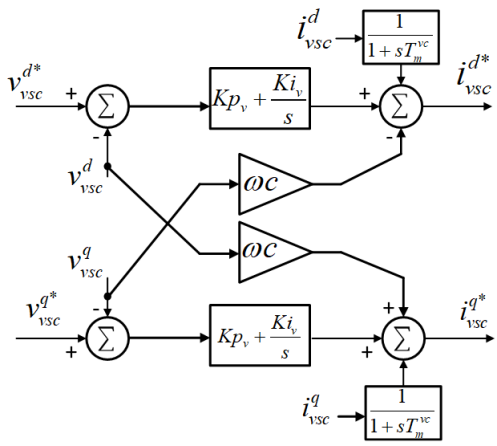

Figure 5.6: Decoupled dq voltage controller

The decoupling term is defined as

$$\omega c = \omega_{ref}(C_f) \tag{5.10}$$

The time constant of the feed forward filter is T_m^{vc}.

Power measurement block ($Pmeas$)

The power measurement block is used in all the GFC's discussed in this chapter. The $Pmeas$ block computes the active and reactive power as in (5.11) and (5.12)

$$P_{vsc} = v_{vsc}^{D} i_{vsc}^{D} + v_{vsc}^{Q} i_{vsc}^{Q} \tag{5.11}$$

$$Q_{vsc} = v_{vsc}^{Q} i_{vsc}^{D} - v_{vsc}^{D} i_{vsc}^{Q} \tag{5.12}$$

The linearized form of the power measurement block is

$$\Delta P_{vsc} = v_{vsc}^{D0} \Delta i_{vsc}^{D} + v_{vsc}^{Q0} \Delta i_{vsc}^{Q} + \Delta v_{vsc}^{D} i_{vsc}^{D0} + \Delta v_{vsc}^{Q} i_{vsc}^{Q0} \tag{5.13}$$

$$\Delta Q_{vsc} = v_{vsc}^{Q0} \Delta i_{vsc}^{D} - v_{vsc}^{D0} \Delta i_{vsc}^{Q} + \Delta v_{vsc}^{Q} i_{vsc}^{D0} - \Delta v_{vsc}^{D} i_{vsc}^{Q0} \tag{5.14}$$

Frame transformation matrix (T_{vsc})

The non linear transformation matrix (T_{vsc}) is utilized to translate the variables to the dq reference frame in which the GFC control is implemented. The linearized form of the transformation matrix is a function of steady state value of transformed variable and angle difference between the two

frames. In addition to the original input variables, the linearized T_{vsc} also has additional input variable $\Delta\theta_{vsc}$. The linearized equation for frame transformation matrix T_{vsc} is given by

$$\Delta x^{dq} = T_{vsc}(x^{D0}, x^{Q0}, \Delta\theta_0)[\Delta x^{DQ}, \Delta\theta_{vsc}]^T \tag{5.15}$$

where, x^{dq} are the variables in VSC controller reference frame, x^{DQ} are the variables in the common reference frame and T_{vsc} is function of steady state operating point and is given by

$$T_{vsc} = \begin{bmatrix} \cos(\theta_0) & -\sin(\theta_0) & -x^{Q0}\sin(\theta_0) - x^{D0}\cos(\theta_0) \\ \sin(\theta_0) & \cos(\theta_0) & x^{D0}\cos(\theta_0) - x^{Q0}\sin(\theta_0) \end{bmatrix} \tag{5.16}$$

Similarly, the linearized transformation of variables in dq frame to DQ frame is given by

$$\Delta x^{DQ} = T_{vsc}^{-1}(x^{d0}, x^{q0}, \Delta\theta_0)[\Delta x^{dq}, \Delta\theta_{vsc}]^T \tag{5.17}$$

where,

$$T_{vsc}^{-1} = \begin{bmatrix} \cos(\theta_0) & \sin(\theta_0) & -x^{q0}\sin(\theta_0) + x^{d0}\cos(\theta_0) \\ -\sin(\theta_0) & \cos(\theta_0) & -x^{d0}\cos(\theta_0) - x^{q0}\sin(\theta_0) \end{bmatrix} \tag{5.18}$$

The angle difference θ_0 between the reference frames is given as

$$\theta_0 = (\Delta\omega_{sg} - \Delta\omega_{vsc})/s \tag{5.19}$$

PWM and computation delay

To account for the PWM and computation, a delay corresponding to switching frequency has to be accounted. The delay Td, is chosen considering a single updated PWM [51]. A third order Pade approximation of the delay is used for small signal state space analysis.

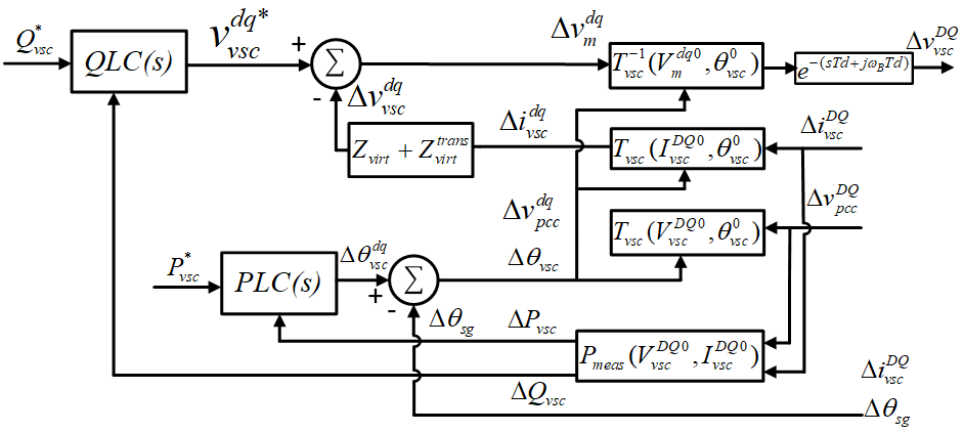

Figure 5.7: Small signal model of the GFC with no inner loop

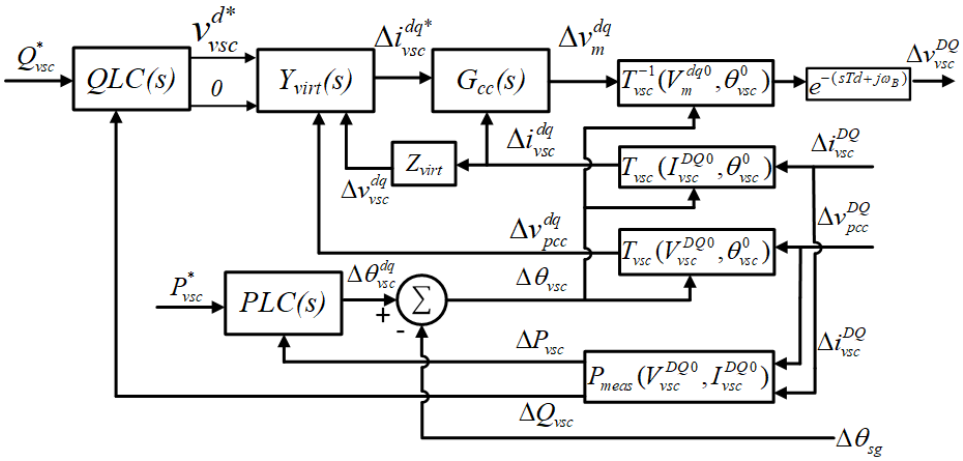

Figure 5.8: Small signal model of the GFC with current control inner loop

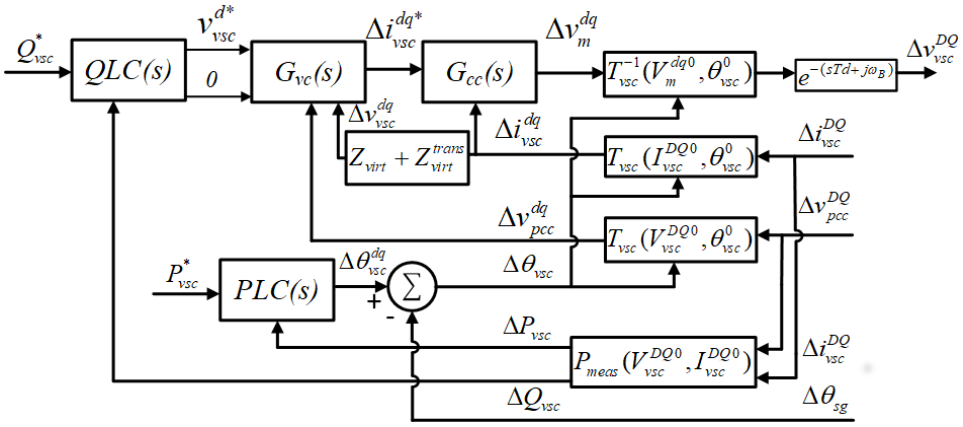

Figure 5.9: Small signal model of the GFC with cascaded voltage and current inner loop

5.3.2 Small signal model of GFC's

The small signal model of the GFC's are developed by interconnecting the linear model each of the control component of GFC explained in the above subsections based on matching input and output signals. The small signal model of the GFC without an inner loop is shown in Fig. 5.7. Similarly the small signal model of the GFC with cascaded voltage and current control and GFC with only inner current control is shown in Fig. 5.9 and Fig. 5.8 respectively.

The $G_{cc}(s)$ is the current controller transfer function as shown in Fig. 5.5, and $G_{vc}(s)$ is the voltage controller as shown in Fig. 5.6.

5.4 Modelling methodology and analysis overview

An overview of the modeling and analysis conducted in the subsequent section of the chapter is presented in this section. Furthermore, the parameters for the comparative analysis are also shown in this section.

Firstly, to ensure a fair comparison, the three GFC models should have the same steady-state performance. As presented in the previous section, the controller structures are different for the

three GFC models. For instance, the GFC with the cascaded control loop regulates the voltage at PCC or the GFC filter bus (v_{pcc}), whereas the GFC with no inner loop controls the inverter terminal voltage (v_{vsc}). On the other hand, the GFC with current control regulates the voltage at a virtual point defined by the virtual admittance ($Y_{virt}(s)$). Therefore, in addition to ensuring the parameters of active and reactive power loops to be the same, each of the GFC's virtual impedance or admittance are designed to provide the same steady-state characteristics without considering the outer power loops. In this study, GFC's virtual impedance or admittance is designed such that the steady-state reactance of all GFC's (X_{GFC}) are 0.15 pu with an equivalent circuit as shown in Fig. 5.10. The values of virtual impedances or admittance chosen for the base case scenario is shown in Table. 5.1.

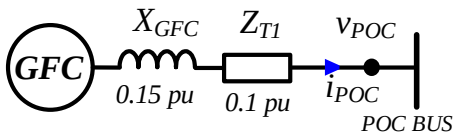

Figure 5.10: Simplified electrical equivalent circuit of the considered GFC's

Table 5.1: GFC's virtual impedance or admittance for the base case

GFC Type	Parameter	Per-unit(pu)
GFC no inner loop	Z_{virt}	-0.05j
GFC with current control	$Y_{virt}(s)$	$\frac{1}{s*0.15+0.15j}$
GFC with cascaded control	Z_{virt}	0.15j

5.4.1 Parameters of the GFC for the comparative analysis

The base case switching frequency is chosen to be 2 kHz which is typical for MW level systems. The filter parameters are designed for the base case switching frequency of 2 kHz. The electrical parameters of the system in the Fig. 1 are for the base case scenario, represented in per unit at a base power of 70 MVA and voltage of 13.8 kV are shown in Table. 5.2.

Table 5.2: GFC filter and network parameters for the base case scenario

Parameter	Per-unit (pu)	Parameter	Per-unit(pu)
L_1	0.2	R_1	0.02
R_f	0.3	C_f	0.05
Z_{TL1}	0.01+0.1j	Z_{TL2}	0.02+0.2j
Z_{T1}	0.1j	Z_{Load}	1.0

The current control parameters for the GFC with current control are designed to meet the time constants of 5 ms for base case. Furthermore, to ensure a reduced transients during network

voltage changes, a upper constraint of 5 ms is considered for voltage feed forward filter (T_m^{cc}) in the tuning process. To emphasize the importance of switching frequency, a second case with the GFC's switched at 10 kHz is also studied in this chapter. While such high switching frequency is not typical for MW level converter, analysis is necessary to study the impact of switching frequency and thereby understand how well the conclusion from past studies conducted at kW level GFC's at microgrid level translate to MW level systems. For the case with a GFC switching at a frequency of 10 kHz, the time constant of the current control for the GFC with current control is decreased to 1 ms from 5 ms.

For GFC with cascaded control three different control design objectives as shown in Table. 5.3 is chosen for analysis. The first design with GFC switching at 2 kHz shown in the Table. 5.3 is the base case for GFC with cascaded control. The different designs are chosen to analyze the impact of control design methodologies. To ensure better transient performance, an upper constraint on the time constant is placed on the voltage feed-forward low pass filter time constant on the first two design objectives. Additionally, one must note that the control design is carried out with the network parameters specified in Table. 5.2, and the performance could vary if the network parameters change which is investigated in this chapter.

Table 5.3: Control Designs considered for cascaded control based GFC

Design 1	PWM delay (T_d)=0.5 ms Voltage control time constant= 20 ms Current control time constant=5 ms voltage feed forward filter (T_m^{cc})$\leq$ 5 ms
Design 2	PWM delay (T_d)=0.1 ms Voltage control time constant= 20 ms Current control time constant=1 ms voltage feed forward filter (T_m^{cc})$\leq$ 5 ms
Design 3	PWM delay (T_d)=0.1 ms Voltage control time constant= 20 ms Current control time constant=1 ms

5.4.2 Small signal modelling methodology

The small signal model of the three major building blocks, the GFC, SG and the Network are formed individually and subsequently interconnected with the respective input output characteristics. The small signal model of each of the three GFCs which are derived in dq frame are then interconnected to the rest of the system modeled in DQ frame using transformation matrices defined in Eq. (5.15) and (5.17). The network model includes the converter filters as well as the transformer impedance, load and network impedance. The linear model of the synchronous machine is well established [33] and therefore not shown in this chapter. The outline of the interconnection of small signal model of the system is shown in Fig. 5.11.

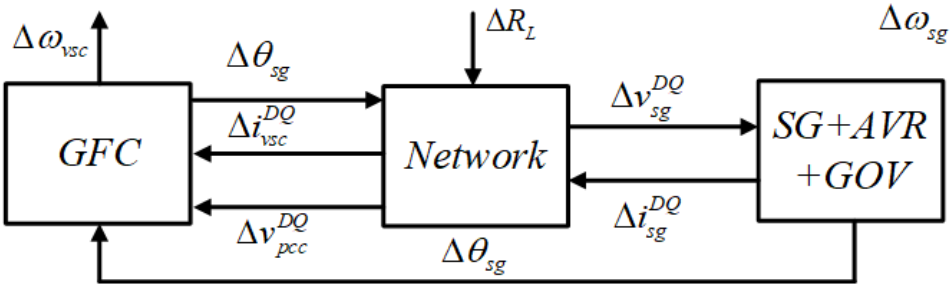

Figure 5.11: Small signal modelling methodology of the system

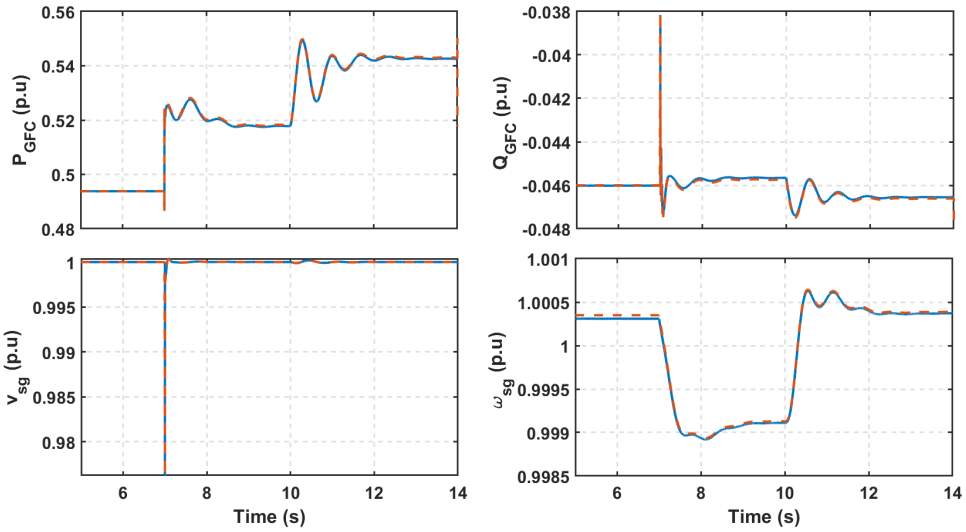

Figure 5.12: Verification of system model with no inner loop based GFC

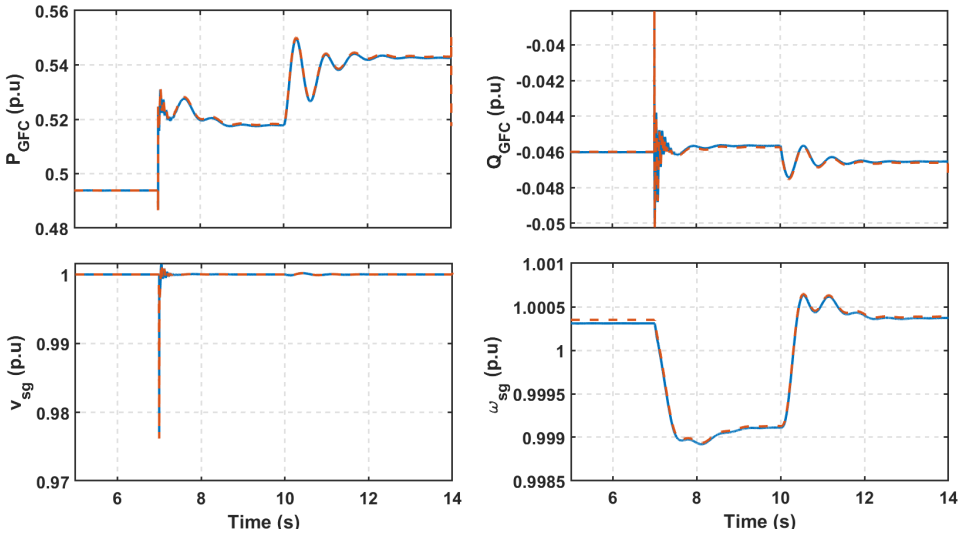

Figure 5.13: Verification of system model with current control loop based GFC

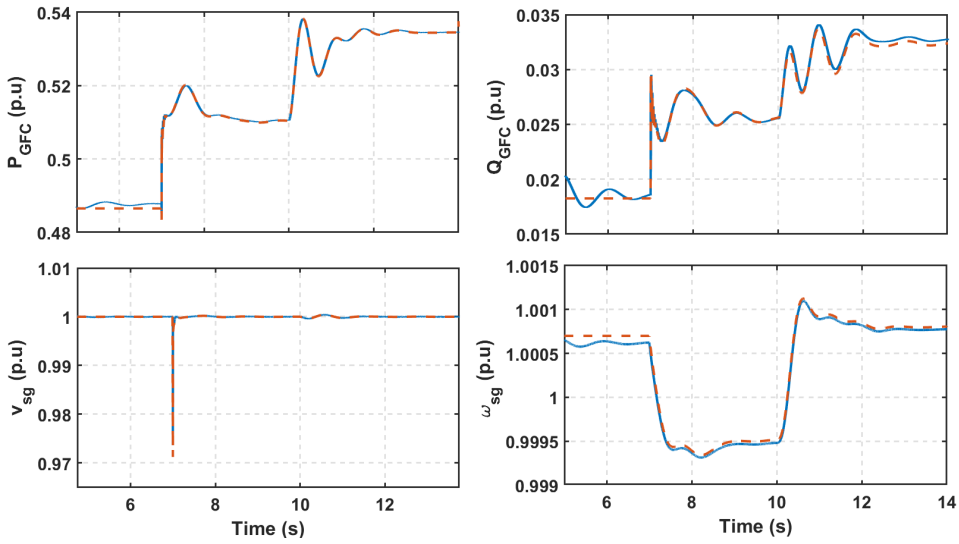

Figure 5.14: Verification of system model with cascaded control loop based GFC

5.5 Small Signal analysis

The small-signal model of the full system shown in Fig. 5.4 for all the three GFC configurations is developed by interconnecting linear dynamical models of GFC, SG, and the network. Analysis conducted on the derived small-signal model of the GFC system, including impedance and passivity analysis and eigenvalue analysis, is presented in this section.

5.5.1 Model verification

The three separate linear models of the complete system with the considered GFC are Verified against the nonlinear time-domain model shown in Fig. 5.4. The response of the full system model with no inner loop-based GFC for 5% step change in the load at 7 sec and 5% step change in the reference power at 10 sec is shown in Fig. 5.12. The response of the system for the same events with cascaded control loop based GFC and inner current control based GFC are shown in Fig. 5.14, and 5.13 respectively. These figures show that the developed linear model provides the same transient response as the nonlinear model, thus confirming the developed linear model's accuracy.

5.5.2 Impedance characteristics without the outer active and reactive power loop

The GFC is expected to provide a response similar to that of a voltage source behind an impedance for load changes and faults as well as to behave as a passive impedance between 5-1 kHz. Furthermore the impact of virtual impedance on the output impedance also needs to be assessed. Therefore, a dynamic impedance assessment of the GFC's without considering the outer loops are carried out derive insightfull information of the impedance's of the GFC. The comparison of the GFC's output impedance ($Z_{pp}(s)$) at POC with base case scenario without the outer loops is shown in Fig. 5.15. The impedance of an ideal voltage source with 0.15 pu reactance for X_{GFC} is also plotted in Fig. 5.15. At very low frequencies, all the GFCs have similar impedance as expected. However, it is seen that the GFC with cascaded control has the highest deviation from the impedance of the ideal voltage source. The virtual impedance for cascaded control is realized by changing the voltage control loop's reference voltage values with a value equivalent to a

drop across a virtual impedance (Z_{virt}). The slow dynamics of cascaded control are reflected in the outer impedance, and the output impedance shape follows the ideal impedance only in the low-frequency range. The GFC with no inner loop follows the ideal impedance closely, and the slight difference is due to sampling and PWM delay. The GFC's impedance with only current control is significantly closer to the ideal impedance for a more extended frequency range than the GFC cascaded control.

One key conclusion drawn from the impedance plot is that a virtual impedance-based current limiting scheme that provides a larger transient stability margin [56] lack fast response speed to protect the converter sufficiently for a GFC with cascaded control [119]. The limitation is even more prominent in large power converters, where the low switching frequency prohibits a high control bandwidth. On the other hand, the virtual impedance method could be sufficiently fast to ensure proper protection for both GFC with only current control and no inner loop case. The implications of the difference in output impedance's during transients also has to be carefully studied.

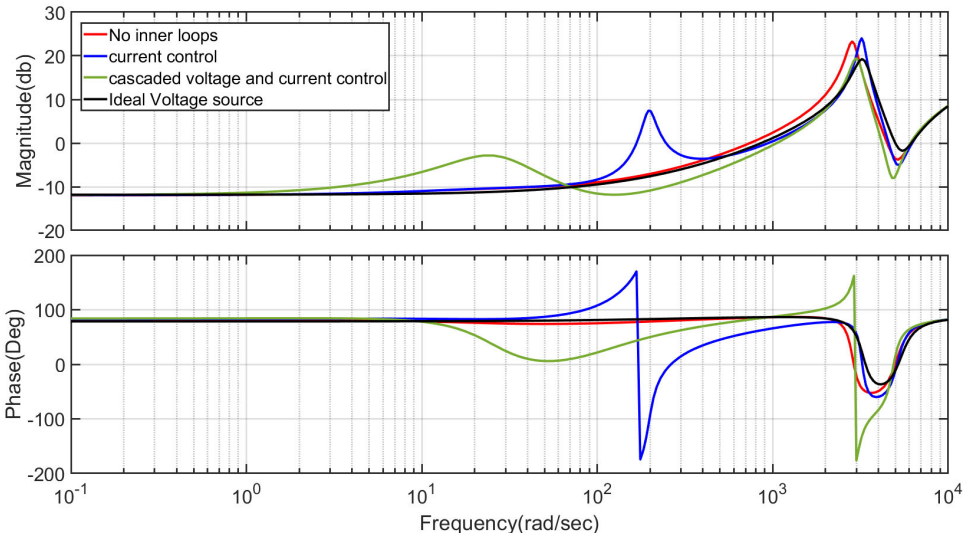

Figure 5.15: Dynamic impedance of the GFC's and of the ideal voltage source and impedance

5.5.3 Passivity analysis of the GFC's impedances

In this section, the dynamic impedance ($Z_{pp}(jw)$) of the three GFC's including the outer loops are analysed in the frequency range of 5 Hz - 1 kHz for passivity check. Background on Impedance analysis and passivity analysis is explained in Chapter 2.

However, just like an SG, a VSC can never be made entirely passive at all the frequency range [41]. SG's are nonpassive only in the low-frequency range due to slow control and dynamics. Therefore the conventional power system composed mainly of SG-based generation had predominantly low-frequency instabilities [33]. The impedance range of nonpassive operation could span a wide bandwidth depending on the control system implemented for VSC. Therefore, the national grid specification of enforcing a passive impedance behavior in the frequency range of 5 Hz-1kHz [44] for GFC's can reduce the negative interactions between the converters and limit the interaction with the network to a low-frequency range. Furthermore, this also comes with an added benefit of the ease of modeling and analyzing large systems.

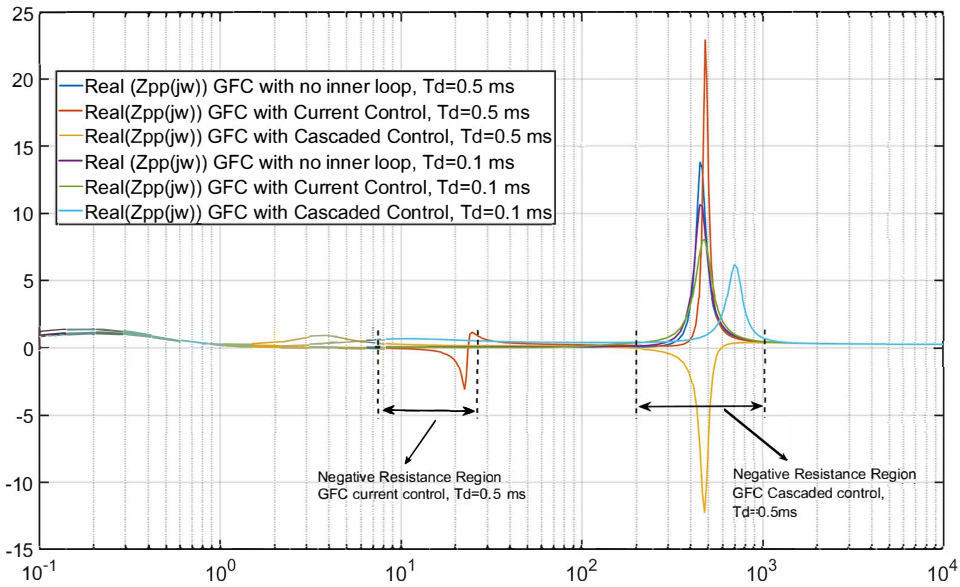

Figure 5.16: Real part of the dynamic impedance of the three type of GFC's considered.

The real part of the modified positive sequence impedance is shown in Fig. 5.16. It can be seen from both the figures that the GFC without any inner loop behaves as passive impedance in the frequency of interest as it does not have a nonnegative real part. Whereas the ($Z_{pp}(jw)$ for both GFC with current control as well as the GFC with cascaded control has a negative real part in the frequency range of 10-15 Hz and 300-600 Hz, respectively, for the designed control parameters. However, when the time constant of the current control is increased to 1 ms for a 10 kHz switched converter, there is no negative resistance region in the output impedance of the GFC. This implies that the presence of an inner loop in low switching frequency converters, as is the case with high power converters, could result in unstable oscillations. The result is nis similar to the results derived from impedance-based passivity analysis conducted on PLL-based VSC. Ref. [46, 51] reported that the current control and feed-forward filters, along with the PLL, also contribute to VSC's nonpassive behavior. Therefore, merely eliminating the PLL alone is not enough to ensure the converter impedance behaves passively, as it is demonstrated in Fig. 5.16.

Although, refs. [50, 70, 118] discuss design techniques and controls for increasing the passivity behavior of VSC with LCL filter and current control. The techniques and controls have to be carefully considered before adapting to GFC. Similarly, ref [121] also discusses the challenges and methods in ensuring passivity until the Nyquist frequency range ($0 - fs/2$)for cascaded voltage-controlled converters. In conclusion to this section, it can be said that the requirement of GFC behaving as a voltage source behind an impedance in the frequency range of interest is satisfied for GFC without inner loops, whereas it is not straightforward for GFC's with inner loop to ensure passivity. Furthermore, as the converter is rated for high power, the switching frequency reduces, thus aggravating the stability issues due to the nonpassive behavior of power converter impedances.

5.5.4 Impact of inner loop on electromechanical mode

The future power system will be composed of a mix of SG and VSC, hence it is important to study the interaction between GFC and SG. For SG, the damping is realized through damper

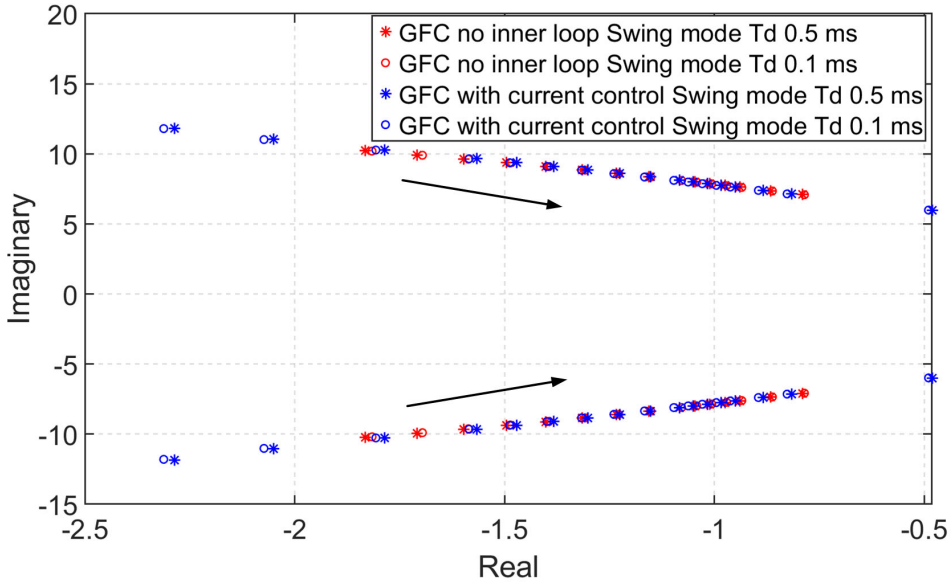

Figure 5.17: Trajectory of swing mode of GFC with no inner loop and GFC with current control by simultaneously increasing transmission line impedance's (Z_{TL1}, Z_{TL2}) from 0.01 to 0.5 pu

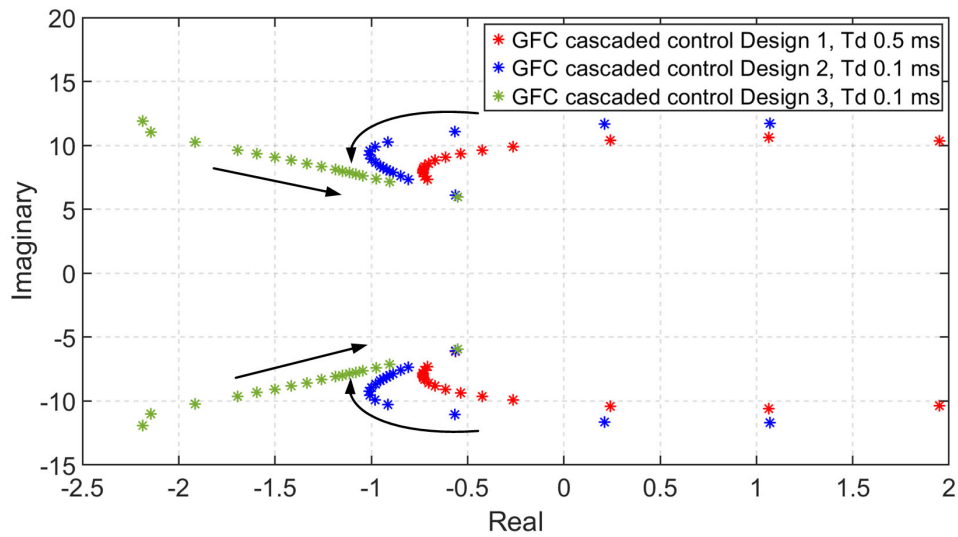

Figure 5.18: Trajectory of swing mode of GFC with cascaded inner loop with simultaneously increasing transmission line impedance's (Z_{TL1}, Z_{TL2}) from 0.01 to 0.5 pu for control designs specified in Table. 5.3

windings and is typically low, whereas the damping effect for GFC can be easily programmed and is constrained only by the size of the dc energy storage. Consequently, it is essential to ensure that the inner loops do not adversely affect electromechanical mode. Such study should be conducted in a test system consisting of both SG and GFC. Most recent publications [110–112] that investigated GFC with cascaded inner loop did not consider a SG in the studies. Therefore, the local electromechanical oscillation typically in the frequency of 0.7-2 Hz is not present in any of these studies. Thus the impact of inner loops on the electromechanical mode of SG has not been evaluated. Furthermore, ref. [111, 112] has no inertia programmed in control, hence an oscillatory

mode arising due to virtual inertia is absent.

In this section, a small-signal analysis is carried to evaluate the difference in impact on the electromechanical mode by the three considered GFC's. First, an eigenanalysis is conducted on the derived small-signal model, and the electromechanical modes are identified from the participation factors. Major participants of the swing modes are the SG's rotor speed and active power control loop of the GFC's. In the case of SG, the swing mode moves towards RHP when the grid strength is reduced [33], and one would expect similar behavior with the GFC. However, unlike an SG where additional damping has to be provided by indirect means such as power system stabilizers, the GFC can be damped using control paramaters.

The trajectory of swing mode of GFC with no inner loop and GFC with current control by simultaneously increasing transmission line impedance's (Z_{TL1}, Z_{TL2}) from 0.01 to 0.5 pu is shown in Fig. 5.17, the case is repeated for GFC switching at 2 kHz and 10 kHz. Compared to GFC without inner loop GFC, the swing modes in GFC with current control are slightly more sensitive to change in grid impedance. However, GFC with current control can provide slightly higher damping in low grid impedance scenarios, but the differences in the trajectory and position of the eigenvalues are not significantly different from each other. It can also be seen that the change in the switching frequency hardly affects the swing modes in both the GFC with current control and GFC with no inner loop.

The electromechanical mode in both cases moves to the right as the grid impedance is increased; however, it is quite possible to ensure sufficient damping even at very low grid strength. Compared to GFC without inner loop GFC, swing modes in the case of GFC with current control are slightly more sensitive to change in grid impedances. However, GFC with current control can provide slightly higher damping in low grid impedance scenarios, but the differences in the trajectory and position of the eigenvalues are not significantly different from each other. It can also be seen that the change in PWM delay hardly affects the swing modes in both the GFC with current control and GFC with no inner loop. From these studies, it can be observed that the presence of an current control alone in GFC with current control does not negatively impact the damping of the electromechanical mode.

The swing modes of GFC with cascaded inner control by simultaneously increasing transmission line impedance's (Z_{TL1}, Z_{TL2}) from 0.01 to 0.5 pu for all the three control design objective is shown in Fig. 5.18. The results of the Eigen trajectory design one and two shown in Table. 5.3, which seems to be moving left initially as the transmission line impedances (Z_{TL1}, Z_{TL2}) are increased before shifting the trajectory back towards RHP.

On the other hand the eigenvalues consistently move towards RHP as the network impedance is increased when design parameters of the GFC are corresponding to design 3 in Table. 5.3. This trajectory is similar to how electromechanical mode would move as in the case of the other two GFC's or an SG. Furthermore, electromechanical eigenvalues with design 1 and 2 are always underdamped compared to the electromechanical eigenvalue results with GFC with no inner loop and GFC with current control inner loop at similar grid strength. On the other hand GFC with cascaded control provided equivalent damping to the electromechanical mode as the GFC with no inner loop and GFC with current control inner loop with design three parameters.

The Ref.[110–112], concludes that an increase in grid impedance is better for the stability of the GFC with cascaded voltage control. Although the test system and outer loop parameters are different

with Ref.[110–112], the eigen analysis presented in this chapter shows that such a conclusion is not unconditionally true and can depend on the system considered, control design, power rating, and structure of the cascaded voltage control.

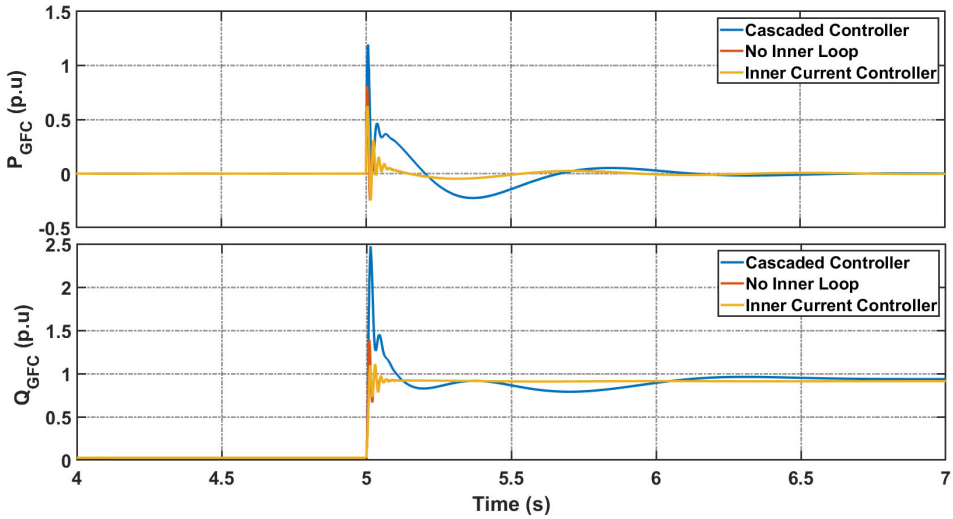

Figure 5.19: Response for a infinite bus voltage dip to 0.5 p.u

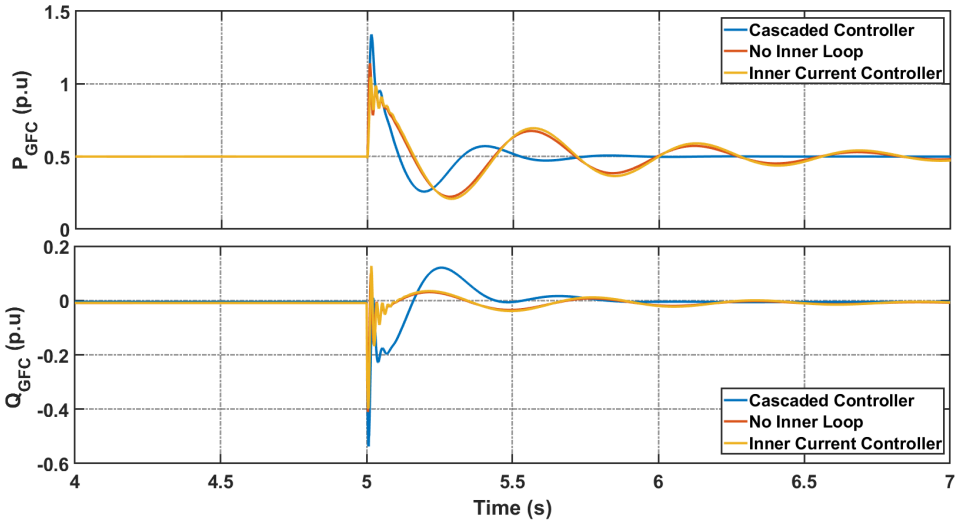

Figure 5.20: Response for a infinite bus angle jump of 10 degree

5.6 Time Domain Simulation Study

The focus on the time-domain analysis presented in this section is to verify the conclusions drawn in small-signal analysis and verify if the response from all the three GFC types is simillar to a voltage source. It is concluded in the small-signal analysis that the GFC types with inner loops for MW level converter could be nonpassive in certain frequency ranges. It is also concluded that the GFC with cascaded control could negatively impact the electromechanical damping when system strength improves. The time-domain simulation results presented validate this conclusion.

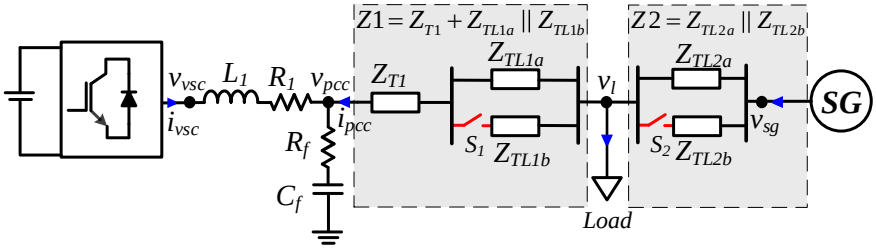

Figure 5.21: The test system to evaluate the implication of different impedance behaviour and robustness of the three GFC's against a network impedance change

5.6.1 Response of the GFC's connected to an infinite bus

The grid forming capability of the GFC is first evaluated against an infinite voltage source, the responses of interest here are active and reactive power output of the GFC's against a step change in infinite bus voltage and step change in angle of the infinite bus. The GFC POC bus is connected to the infinite bus through a 0.1 p.u reactance. The net steady state impedance between the infinite bus and the voltage source representing GFC will include the physical network impedance of 0.2 p.u and the impedance of 0.15 p.u of GFC internal impedance. It has to be noted that the GFC internal impedance is emulated using virtual impedance as in the case of GFC with inner loop, or adjusted with filter impedance to get total of 0.15 p.u for GFC with no inner loops.

The output response of a voltage source behind an impedance against a grid event depends on the total impedance and the magnitude of the voltage, which in this case is similar for all the three converter in steady state. For instance, smaller the impedance, larger the expected reactive power exchange during voltage dip. Similarly, smaller the impedance, larger the active power exchange expected during voltage phase shift. Therefore, provided that the GFC's have similar impedance, the responses are also expected to be same. For a dip in infinite bus voltage to 0.5 p.u, the considered GFC's have similar responses from the three GFC's considered in steady-state as seen in Fig. 5.19. However, the GFC with a cascaded inner loop has a larger than expected spike immediately after the dip in voltage compared to the other two. Such spike can be attributed to the cascaded loop's slow dynamics, resulting in an emulated impedance that is relatively slow and presents a varying impedance than a constant impedance. The impact of this slow dynamics of the virtual impedance for cascaded control is also seen in response to the phase jump of the infinite bus voltage, as seen in Fig.5.20. The slow varying impedance is an undesirable characteristic as it can trigger the current limit and presents a problem in dynamic power-sharing under parallel connection of voltage sources.

5.6.2 Case Study

A time domain Case study to evaluate the implication of different impedance behaviour and robustness of the three GFC's against a network impedance change are conducted. The GFC with time delay corresponding to PWM frequency of 2 kHz is chosen for the study. The time domain study is closely aligned with the small signal analysis presented in Section 5.5. A test system as shown in Fig. 5.21 is implemented in MATLAB/SIMULINK. The impedance Z1 is the the net impedance between PCC bus and load bus, and Z2 is the net impedance between load and SG

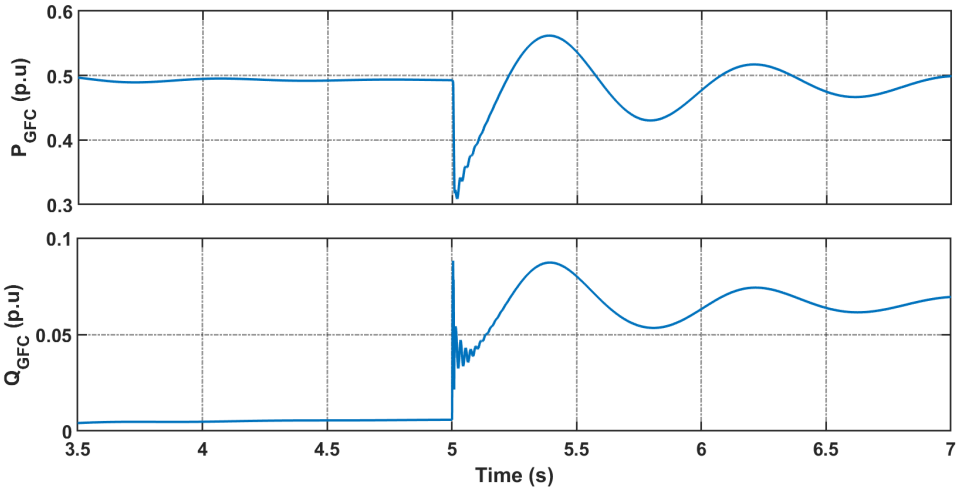

Figure 5.22: Active and reactive power time domain response of the GFC with no inner loop under network impedance impedance Z1 increase from 0.15 pu to 0.6 pu

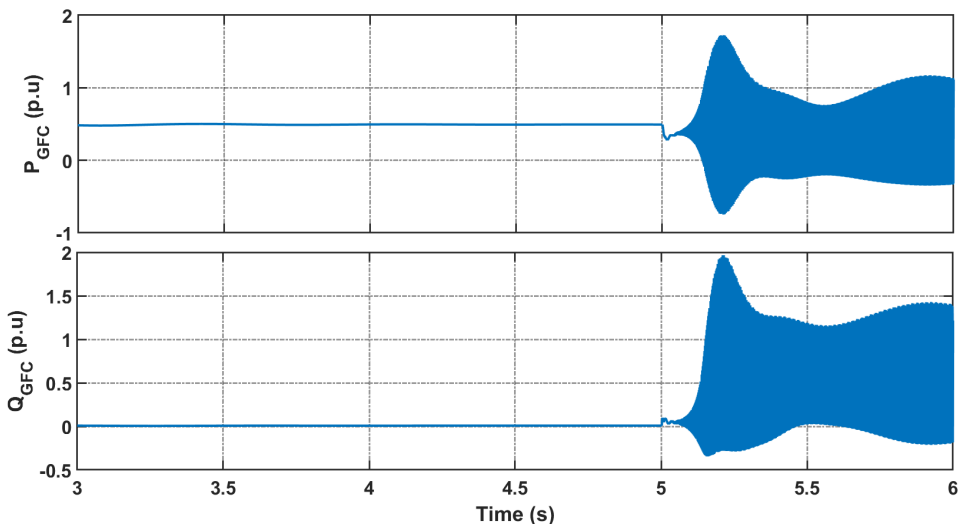

Figure 5.23: Active and reactive power time domain response of the GFC cascaded inner loop under network impedance impedance Z1 increase from 0.15 pu to 0.6 pu

bus. For the first case, the three GFC's are evaluated against an increase in network impedance change event. During pre-network impedance change event, the switch S2 is off and S1 is on, ensuring both Z1 and Z2 to be 0.2 pu. Also, both the SG and the GFC's are sharing 1 pu load equally between the them. Switch S1 is opened at 5 seconds, increasing impedance between the PCC bus and the load bus (Z1) to 0.6 pu. The test case is repeated for systems with all the three GFC's. As seen in Fig. 5.22, the GFC without inner loop behaves as voltage source behind an impedance and settling to steady state as soon as the swing mode are damped out. The results align with that of Section 5.5, which predicted the GFC with no inner loop is passive and swing modes are also damped for all possible network impedance combinations.

The investigating on swing modes and network impedance revealed that the high power GFC with cascaded control, switching at low frequency could have underdamped or undamped electromechanical mode when the network impedances are reduced. Such a characteristics is

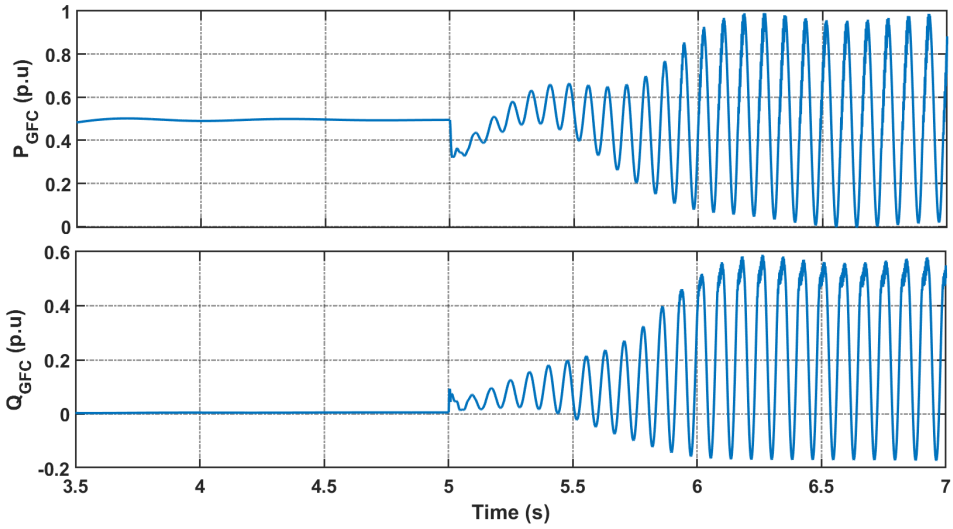

Figure 5.24: Active and reactive power time domain response of the GFC with current control inner loop under network impedance impedance Z1 increase from 0.15 pu to 0.6 pu

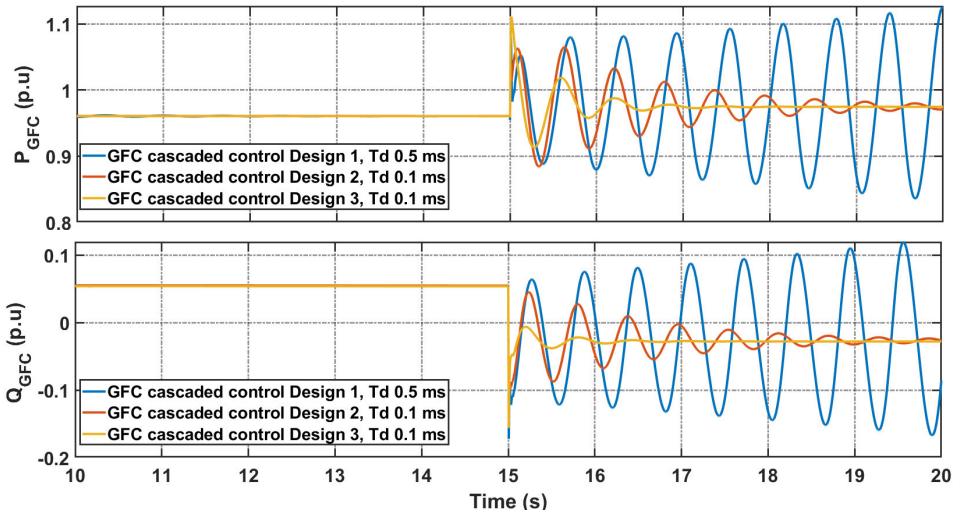

Figure 5.25: Active and reactive power time domain response of the GFC with cascaded control under network impedance impedance Z1 and Z2 decreased from 0.2 pu to 0.1 pu

unlike an SG or the other configuration of GFC's and is unique to GFC with cascaded control. The simulations are conducted with GFC cascaded control with the three design shown in Table.5.3 with the network impedance impedance Z1 and Z2 decreased from 0.2 pu to 0.1 pu at 15 seconds. The results are depicted in Fig. 5.25. It can be seen that for design one with lower switching frequency the swing modes get undamped at 15 seconds, whereas, if the switching frequency was higher as in the case of design 2 and 3 the electromechanical mode is still stable.

The behaviour of the GFC for a 3-phase fault case is shown in Fig. 5.26, which demonstrates a fast fault current contribution from all the three cases, with cascaded inner loop GFC a larger current contribution in the beginning of the fault can be seen due to the slow dynamics of the virtual impedance. One of the main advantage of a synchronous machine, being a voltage source is that it can contribute to load sharing instantly without relying on control or measurements. The

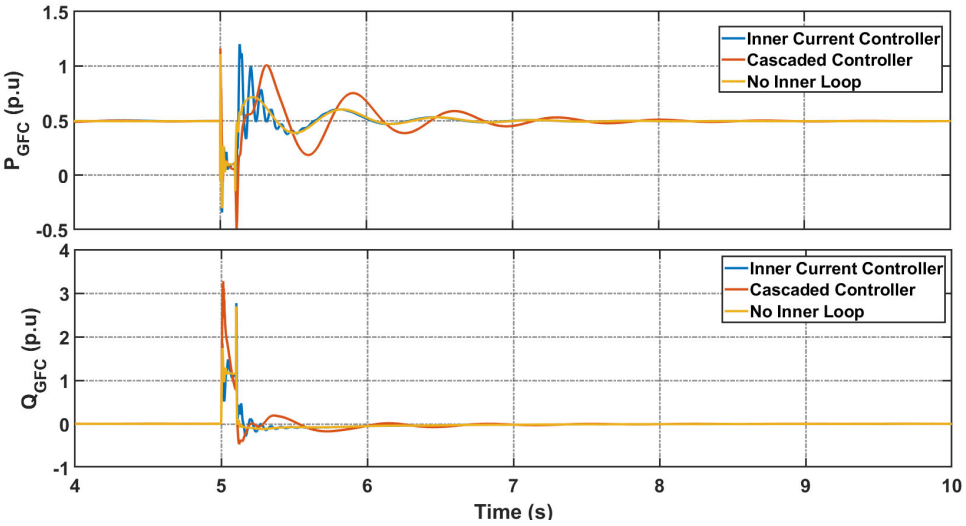

Figure 5.26: Response of the GFC's for a 3L-G fault

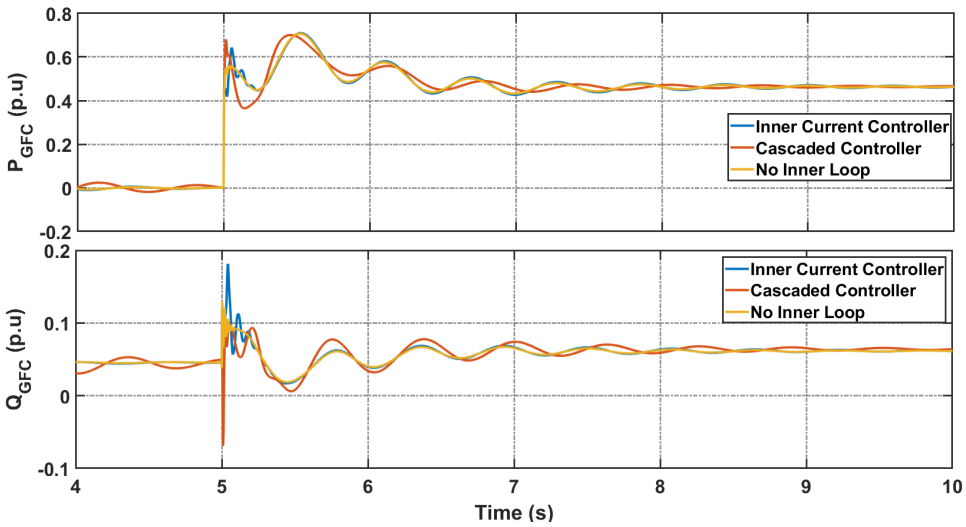

Figure 5.27: Response of the GFC's for a 0.5 p.u load switching

results for a 0.5 p.u load turn on and off when the net impedance between PCC and load is 0.15 p.u is shown in Fig. 5.27 and 5.28. The response shows that all the three GFC have voltage source characteristics as the load is shared instantly by the GFC's. On closer examination it can be seen that power shared at the load switching instant is slightly higher for cascaded inner loop GFC case due to slow dynamics of the virtual impedance.

5.7 Summary

A comprehensive study on the inner loop's impact on the ability of GFC to behave as a voltage source behind an impedance is presented in this chapter. Three of the most popular GFC structures, (i) GFC with cascaded voltage control and current control, (ii) with inner current control only, (iii) with no inner loop, are compared in this chapter. A small-signal model of a GFC connected to an SG system was derived to assess the dynamic impedances of the three GFC'a and study the

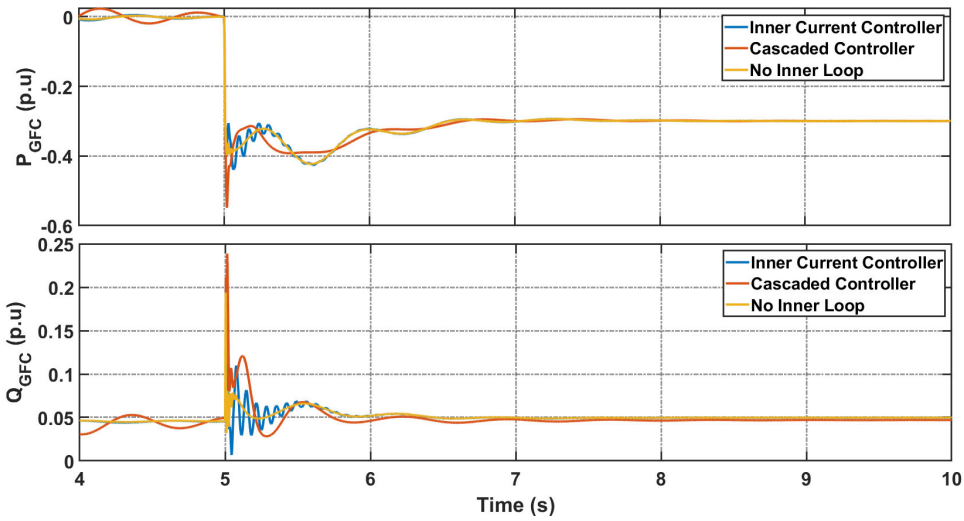

Figure 5.28: Response of the GFC's for a 0.5 p.u load disconnection

Table 5.4: Summary of GFC comparisons

	GFC with no inner loop	**GFC with inner current control**	**GFC with cascaded voltage control**
Passivity Beyond outer control Bandwidth	Passive	Possibility for not passive at frequency determined by feed forward filter and control bandwidth	Possibility for not Passive around resonant frequency range
Constraint on network impedance	No constraint	Upper limit in non passive region	Both upper and lower limit
Dynamic power-sharing	Behaves like a voltage source behind a fixed reactance	Behaves like a voltage source behind a fixed reactance	Behaves like a voltage source behind a time varying reactance due to slow acting virtual impedance
Virtual impedance current limiting	Possible	Possible	Limited application due to slow acting virtual impedance
Electro-mechanical eigen value	No negative impact on damping	No negative impact on damping	Negative impact on damping, depends on control design

impact of inner loops on elctromechanical mode. Assessing the dynamic impedance of the three GFC's derived from the small-signal showed that it is challenging to ensure a passive impedance behavior in a broad frequency range for GFC with the inner loop. This is particularly true for high power GFC's with low switching frequency because of the PWM delay. Because of this, unstable oscillations may arise for a system composed of GFC with inner loops under weak grid conditions.

Also, the time domain studies performed in the chapter showed that the GFC configuration with the inner current control and no inner loop could respond similar a voltage source under a strong grid scenario. Whereas, for the GFC with a cascaded inner loop, the impedance is found to be slow-acting and only effective in very low frequency range because of the loop delays. This slow acting virtual impedance of the cascaded GFC results in higher than expected instantaneous active power

and reactive power for a grid event, which may trigger unexpected overcurrent protection as the semiconductor devices are sensitive to over current. Moreover, this slow-acting virtual impedance is seen as a slowly changing time-varying impedance in the GFC's terminal characteristics with cascaded control, causing problems in dynamic reactive power-sharing. Furthermore, the slow acting virtual impedance can also limits the application of virtual impedance based current limiting in GFC with cascaded controller.

Additionally, a study on the electromechanical oscillation mode of the SG was conducted with the three GFC configurations. It was found that the impact of PWM delays for GFC configuration with no inner loop or only inner current controller is marginal.The damping of the electromechanical mode for GFC configuration with no inner loop or only inner current controller is better than GFC with cascaded control at all network strength. The electromechanical oscillation mode for GFC with cascaded control is sensitive to the inner loop. And unlike an SG or the other configurations of GFC, it is found that a high power converter with low switching can be unstable with low network impedance. And the electromechanical oscillation mode can move towards a more stable region as the network impedance is increased. Consequently, GFC with cascaded control could have both an upper bound on the network impedance due to passivity-related high-frequency oscillations and a lower bound for network impedance to ensure damping for electromechanical mode. Furthermore, this chapter shows that weakening of the electromechanical mode damping with an increase in grid strength is control design and converter-specific, and converse could be true for a different control design for converters with higher switching frequency. With an other control design objective and higher switching frequency, one can achieve similar damping for electromechanical mode with the GFC with cascaded control as that of GFC with no inner loop.

CHAPTER 6

Assessment of GFC Synchronization Capability Under Transient Events

The studies on the response of GFC for transient events, particularly when the GFC enters the current limit operation, have been limited. The GFC operation during significant frequency and phase jump events, typical for low inertia systems, are not described in the literature. The primary concern during transient events for the GFC in current limited operation is that the current limiter influences the measured active output power, which is also used for synchronization. This chapter presents a quantitative and illustrative analysis of the impact of the current limit in GFC on the transient stability of a system comprising of GFC. Furthermore, a solution based on virtual active power is proposed to improve the transient stability margin of the GFC when the GFC enters the current limit. Finally, the analysis and the proposed method to enhance the transient stability are verified by Power hardware in the loop (PHIL) experimental tests.The chapter is based on [**Pub. B**], with minor changes to fit the framework of this thesis.

6.1 Introduction

The SG has an overload capacity of several times its rated value during short-term overload and grid faults. Such high overload capability is not typical for a power electronic converter-based GFC, which emulates SG. Therefore, GFC needs to have a robust overload and fault current limiter for protecting and ensuring reliable GFC operation during significant transient events. Yet, implementing the power or current limiters for GFC is challenging as an instantaneous response is expected similar to a voltage source and can distort the responses of GFC during transient events[60, 122].

Switching to control that employs voltage-based phase-locked loop (PLL) synchronization and controls the active and reactive current control during overload and grid fault scenarios is an option for GFC [123]. However, the solution is not robust as there is a need to preserve a complete additional control set in the same digital control. Furthermore, the mode switching and stability issues caused due to PLL is also undesirable [60]. The backup PLL is not required in the current limit methods employed in [62, 62, 109] or with the virtual impedance-based current limit method discussed in [56, 124]. In GFC, the active power control also acts as the synchronization control. Therefore, it is challenging to ensure the synchronization for the GFC during the current limit triggering transient events[56].

Recently many studies have analyzed the transient stability of GFC [59–62]. Some of these studies were conducted on GFC with no current limit implemented [59, 60]. A current limit is likely to be

triggered in a practical transient event scenario. Therefore studying the GFC for transient events requires the inclusion of the current limit for an practical understanding. The transient stability of a droop-based grid forming converter with the current limit is studied in [61, 62] and methods are discussed for improving the transient stability, however, discussed approaches are not intuitive and requires tuning of parameters. In addition, all the transients studies have been restricted only to a voltage dip event when connected to an infinite voltage source. A GFC, when operated in a microgrid in parallel with an SG and virtual impedance current limit, can avoid the wind-up effect of the outer loop for load change events [56]. However, only a limited evaluation of droop control-based GFC only for load change events has been shown. The frequency and phase jump events are significant in the present context for the power system with a significant renewable share. Therefore transient events such as a change of frequency and phase jump can cause current limit triggering for GFC. An detailed studies on GFC under such transient events or in the presence of an SG is missing in the literature. Furthermore, a quantitative analysis on the transient stability of GFC for all the possible events are also missing literature.

This chapter first demonstrates the scenarios in which the current limit could be triggered in a GFC working in a low inertia power system and outlines the challenges in maintaining the GFC synchronism with the rest of the grid when the current limit is triggered for each scenario. Then, to clarify the stability phenomena when the current limiter is activated, a quantitative analysis of transient stability for events such as phase jump and frequency change events and voltage dip events when the current limiting algorithm is employed in a GFC is presented in this chapter. The transient stability margins such as maximum phase jump, maximum rate of change of frequency, critical fault clearing time, and methods to improve the synchronization stability for all the three events described in this chapter are described from the conducted analysis. Finally, a coordinated overload and current limit for grid forming converter employing virtual power, extending the transient stability margin for all the grid events, are proposed in this chapter. Conducted analysis and the proposed solution to improve the transient stability of the GFC is validated using power hardware in the loop (PHIL) experimental tests are presented. The PHIL evaluation is conducted in a simplified equivalent circuit and a modified IEEE 9 bus system.

6.2 Grid Forming Converter Configuration

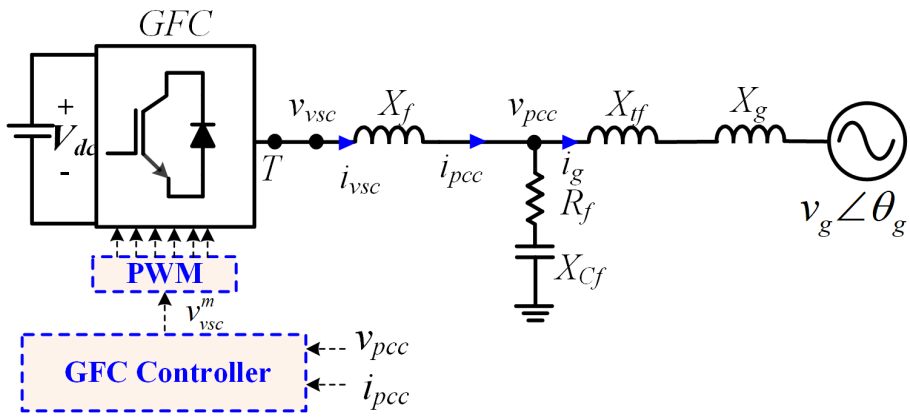

Figure 6.1: The configuration of 3 phase grid connected GFC system

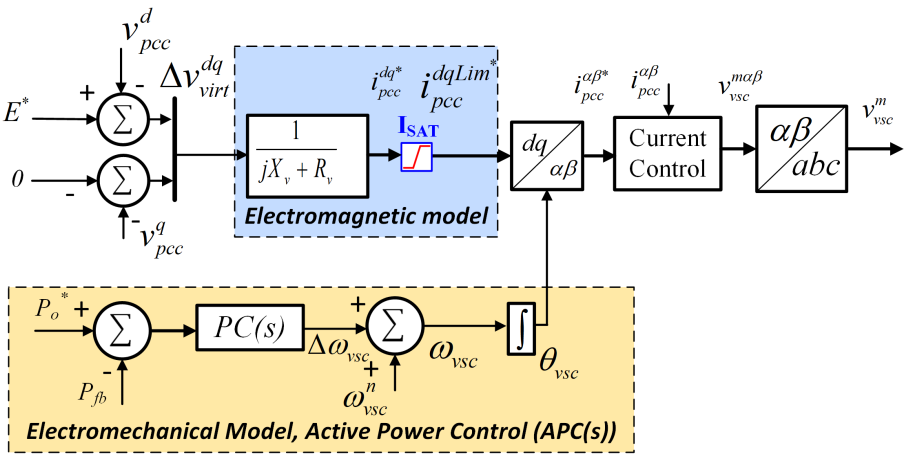

Figure 6.2: General Control System of GFC with current control inner loop and virtual admittance

The single line diagram of the GFC considered in the chapter is shown in Fig. 6.1. All the parameters are represented in their per unit form. The filter circuit comprises reactor X_f, capacitor of reactance X_{Cf}, and damping resistor R_f. The point of common coupling (PCC) is at the terminal of the filter capacitor, where measurements v_{pcc}, i_{pcc}, and i_g are taken. The reactance X_{tf}, X_g represents the reactance of transformer and grid impedance, respectively. The grid forming control with an inner current control loop with current references derived from virtual admittance is used in this chapter is as shown in Fig. 6.2 [55, 57, 109, 125]. The power control system consists of inertia, frequency droop, and damping emulation through active power control ($APC(s)$) with active power setpoint (P_o^*). The power output from the GFC measures at the PCC (P_{pcc}) is typically chosen as the feedback power (P_{fb}) to the active power control loop. Variable superscripted with d-q are variable vectors of the direct and quadrature frame original parameters represented in the synchronously rotating reference frame defined by the virtual rotor of the GFC (θ_{vsc}).

A lead-lag compensator-based power controller ($PC(s)$) is employed to emulate the synchronous machine behavior [57]. The compensator is given as

$$\Delta\omega_{vsc} = \underbrace{\frac{K_{pp}s + K_{ip}}{s + K_{gp}}}_{\text{PC(s)}} *(P_o^* - P_{fb}) \tag{6.1}$$

Where P_{fb} is the feedback power for power control loop. The compensator $PC(s)$ is similar to the swing equation-based electromechanical model can realize virtual inertia constant, H, and frequency droop R_d. In addition, LL-based electromechanical model, unlike swing-based electromechanical model discussed in the previous chapter, has an additional degree of freedom to increase the power control's damping coefficient (ζ). The parameters (K_{pp}, K_{ip}, K_{gp}) can be calculated from a given virtual inertia constant H in seconds, and power-frequency droop gains R_d in pu and damping coefficient (ζ).

$$K_{ip} = \frac{\omega_B}{2 * H}, K_{gp} = \frac{K_{droop}}{2 * H} \text{ where } K_{droop} = \frac{1}{R_d} \tag{6.2}$$

$$K_{pp} = \zeta\sqrt{\frac{2\omega_B}{P_{max}H}} - \frac{K_{droop}}{2 * H * P_{max}} \tag{6.3}$$

Where ω_B is the base frequency of the system, P_{max} is the maximum static power transfer possible between the GFC and an infinite voltage source. If the power-frequency droop is not required, the parameter K_{droop} is to be set to zero in (6.2)-(6.3). For the GFC electromagnetic model, a quasi-stationary model has been shown superior to a dynamic electromagnetic model model for GFC [125]. The electromagnetic model consists of the internal voltage source (E) in series with an algebraic representation of an impedance. It is realized by multiplying the difference between the internal voltage source (E^*) of the GFC and PCC voltage (v_{pcc}^{dq}) with virtual phasor admittance resulting in reference unsaturated stator current (I_{pcc}^{dq*})

$$I_{pcc}^{dq*} = \frac{E - v_{pcc}^{dq}}{R_v + jX_v} \tag{6.4}$$

where R_v, X_v are the virtual internal virtual resistance and reactance of the GFC. The virtual impedance is chosen such that the output impedance is predominantly inductive with an X/R ratio of 10. The electromagnetic model of the GFC also includes the current limiting algorithm. Implementing current limiters for GFC is critical as the GFC response to grid events is nearly instantaneous. A circular current limit on I_{pcc}^{dq*}, as shown in (6.5) is an ideal choice as it precisely limits current and preserves the angle of the injected current and thus limiting the interaction with the active power-based synchronization [109, 126].

The limited current vector $i_{pcc}^{dqLim^*}$

$$i_{pcc}^{dqLim^*} = \frac{1}{KC_{lim}} * I_{pcc}^{dq*}, \text{ where } KC_{lim} = \frac{\left|I_{pcc}^{dq*}\right|}{I^{Lim}} \tag{6.5}$$

$\left|I_{pcc}^{dq*}\right|$ is the magnitude of the unsaturated reference current vector and is equal to $\sqrt{(I_{pcc}^{d*})^2 + (I_{pcc}^{d*})^2}$ and I^{Lim} is the nominal maximum peak current, and thus the vector I_{pcc}^{dqLim} is of the magnitude I^{Lim} during current limited operation.

The chapter's focus is on the interaction between the current limit and active power control and its consequences on the transient stability of GFC. Therefore, to preserve the chapter's brevity, the outer reactive power control or voltage control is assumed to be slow. Thus, the voltage control and reactive power control dynamics are not accounted for in this work. Also, the DC link dynamics and other supervisory controls are not considered in this chapter for the sake of easier understanding.

6.3 GFC quasistatic analysis under current limit

The analysis assumes that the dynamics of the employed current limit are faster than other control and thus time scale separated from the stability study considered in the chapter. Additionally, the chapter's focus is applying the GFC on large power systems with a low R/X ratio; therefore, only the reactances of the virtual impedances and grid impedances are considered in the quasistatic analysis.

The per unit active power (P_{GFC}) and the reactive power (Q_{GFC}) at the internal voltage source (E) is given by

$$P_{GFC} = \frac{E * Vg * \sin\delta}{X_T}, Q_{GFC} = \frac{E^2 - E * Vg * \cos\delta}{X_T} \tag{6.6}$$

Where X_T is the total reactance of the system from between the internal voltage (E) and is equal to sum of X_{tf}, X_g and X_v, and the infinite voltage source and δ is the angle difference between the

internal voltage source and infinite voltage source and is equal to difference between θ_{vsc} and θ_g. The active and reactive power at the internal virtual voltage source E in the rotating dq frame defined by GFC virtual angle (θ_{vsc}) can also be written as

$$P_{GFC} = E * I_{pcc}^{d*}, Q_{GFC} = -E * I_{pcc}^{q*} \tag{6.7}$$

The magnitude of the current vector I_{pcc}^{dq*} can then also be written as

$$|I_{pcc}^{dq*}| = \frac{\sqrt{P_{GFC}^2 + Q_{GFC}^2}}{E} = \frac{M_v}{X_T} \tag{6.8}$$

where M_v is equal to $\sqrt{Vg^2 + E^2 - 2 * Vg * E * \cos(\delta)}$

The generalized power transfer equation for the GFC can then be calculated from (6.5),(6.6),(6.8)

$$P_{GFC} = \begin{cases} \frac{E*Vg*\sin\delta}{X_T}, & |i_{pcc}| \leq I^{Lim} \\ \frac{E*Vg*\sin\delta}{\sqrt{Vg^2+E^2-2E*Vg*\cos(\delta)}} * I^{Lim}, & |i_{pcc}| > I^{Lim} \end{cases} \tag{6.9}$$

It can be observed that the power transfer under current limited case is independent of the network reactance. When the drop across the virtual resistance (R_v) is neglected the active power at the internal voltage terminal is same as P_{pcc}. The power angle curves for the GFC with and without limiter activation at different grid voltage conditions are shown in Fig. 6.3. It could be seen that the unstable operating points occurs at much lower phase angle (δ) and maximum power transfer possible is greatly reduced when under current limit.

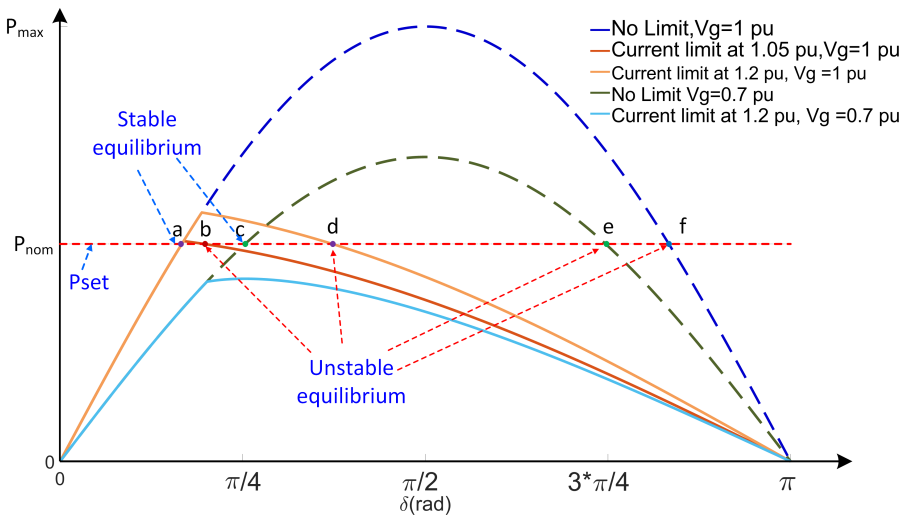

Figure 6.3: Power angle curves for GFC with and without limiter activation at different grid voltage conditions

6.3.1 Internal impedance of GFC during current limit

Recalling from (6.4) and (6.5) under current limit case is equivalent to the internal impedance Z_{in}^{cc} as shown below

$$Z_{in}^{cc} = KC_{lim} * (R_v + jX_v) \tag{6.10}$$

The value for KC_{lim} is automatically set due to control objective in (6.5) to ensure the value of peak value of the GFC current is equal to I^{Lim}. Therefore for a given sustained disturbance at the PCC the, the input reactance (X_{in}^{cc}) for the current controlled GFC in current limited case can be written as

$$X_{in}^{cc} = K_{lim} * X_v^{cc} \tag{6.11}$$

6.3.2 GFC with virtual impedance based current limit

The virtual impedance-based current limit has been demonstrated to be an effective method and is typically applied to GFCs with cascaded voltage control [56, 124]. A simplified electrical model of the GFC with voltage control and virtual impedance current limiting is shown in Fig. 6.4. The X_c is a combination of the filter impedance and virtual steady-state impedance, if any. For the same sustained disturbance, the internal impedance of GFC with voltage control and virtual impedance current limiting the internal impedance should be the same as in the GFC structure considered in this chapter with current control and circular current limiting as shown in Eq. (6.10). The final internal impedance of voltage control GFC may vary marginally depending on the type of controller employed in place of $K_{lim}(s)$ shown in Fig. 6.4. One can write the total internal reactance of the voltage-controlled GFC under sustained disturbance at PCC.

$$X_{in}^{vc} = K_{lim}^{vc} * X_v^{vc} + X_c \approx K_{lim} * X_v^{cc} \tag{6.12}$$

Hence one could conclude that neglecting the dynamics of the current limiting algorithm, the virtual impedance limitation in GFC converters are equivalent to circular current limiting case and the limited current follows Eq. (6.5). Therefore, the analysis presented in the chapter for the current controlled GFC with circular limiter is also applicable for GFC with voltage control and impedance-based current limiting, provided the virtual impedance-based current limit is fast-acting.

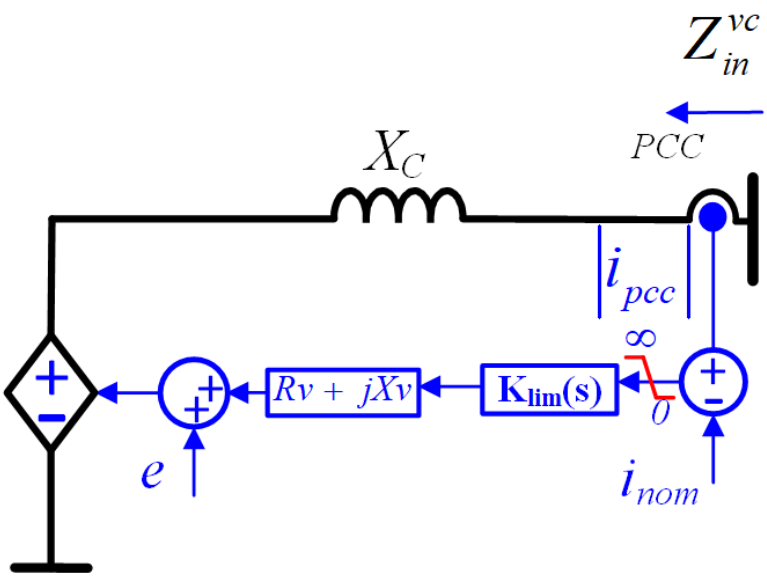

Figure 6.4: Simplified quasi-static electrical model of forming converter model with voltage control and virtual impedance current limit

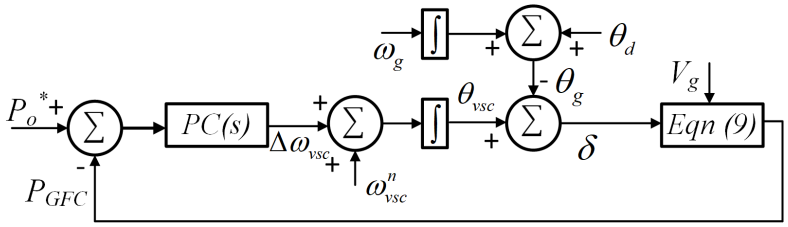

Figure 6.5: Simplified quasi-static GFC connected to infinite bus

6.4 Transient stability of GFC evaluation against system events

The synchronous generator (SG) transient stability focusing on rotor dynamics is evaluated typically for fault cases. If the rotor angle of the SG is not diverging with the rest of the system after the fault event, the SG is stable against transient events. The transient stability of GFC with no current limit during under-voltage dip events has been extensively studied [59, 60]. However, GFC's synchronization ability has not been evaluated for other large system transients such as phase jumps. Furthermore, few studies have investigated the response of GFC with the current limit during large disturbances. In this section, the transient performance of GFC with the current limit implemented is analyzed during system events such as voltage dips, phase shift, and a RoCof event, and conditions for GFC to maintain synchronism for each event is qualitatively described. All events typically co-occur but are studied separately here for an intuitive understanding. The quasi-static model shown in Fig. 6.5 is solved numerically. The total reactance (X_T), including the internal reactance of 0.3 pu, is chosen at 0.5 pu, both the internal GFC voltage and infinite bus voltage are assumed to be 1 pu for the analysis, and the current limit is set to be 1.1 pu. The damping coefficient (ζ) has been set to 0.4 to study underdamped control. It is assumed that the adaptive change in setpoint power (P_{set}) and inertia or dynamic breaking by freezing the power loop is not modelled analyze the main control of GFC during tranisent events.

6.4.1 GFC response against RoCoF of infinite voltage source

The infinite voltage source frequency ω_g is varied from 50 Hz to 48 Hz at a rate of change of -1 Hz/s. The response of the GFC against the specified RoCof with inertia constant H of 10 s is shown in Fig. 6.6.

When the infinite voltage source is decelerating, a similar deceleration is required from the virtual rotor of the GFC to stay in synchronism. The necessary deceleration power in pu (P_{dec}) for the virtual GFC rotor is given by

$$P_{dec} = -1 * \frac{2 * H}{f_{vsc}^n} * RoCof = 0.4pu \tag{6.13}$$

Where the f_{vsc}^n is the nominal frequency of the GFC. When the GFC with no current limits and operating at a power setpoint of 0.8 pu with an operating point at point 1 (Fig. (6.6)) is presented with a RocoF event, the rotor angle moves in the trajectory 1-2-3 and settles at point 3 such that a deceleration power of 0.4 pu is impressed on the virtual rotor according to (6.13). However, point 3 is not reachable for the current limited case as shown in Fig. 6.6. Therefore the trajectory on the power angle curve with current limit follows 1-4-5, and beyond point 5, an unstable operating

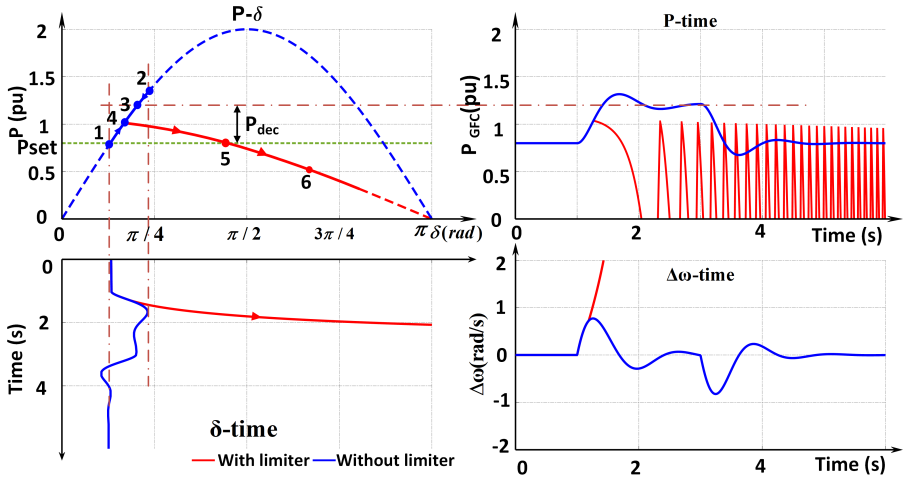

Figure 6.6: GFC response for a 1 Hz/s ROCOF

point is reached, and synchronism is lost, which is reflected in all the curves in Fig. 6.6. When the GFC is also programmed to provide frequency droop (Rd) the condition in (6.13) is modified to

$$P_{dec} = -1 * \frac{2 * H}{f_{vsc}^{n}} * RoCof + \frac{\Delta\omega_{vsc}}{Rd * \omega_{vsc}^{n}} \tag{6.14}$$

From (6.14) one can also conclude that dynamically reducing P_{set}, H, Rd are some of the options to ensure P_{dec} on the virtual rotor and maintain synchronism.

6.4.2 GFC response against phase jump of infinite voltage source

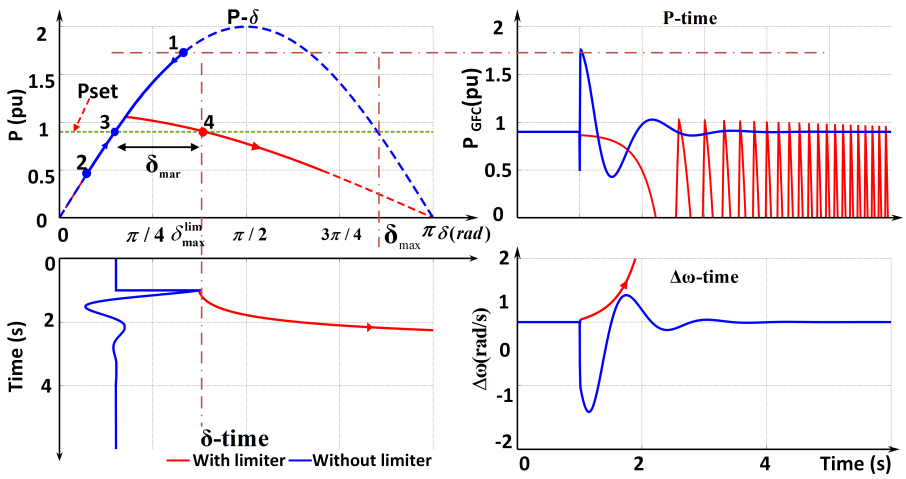

Figure 6.7: GFC response for a phase jump of 40 deg

The GFC is expected to respond instantly to phase jumps in line with a voltage source behavior expected of GFC. The GFC response to simulated infinite voltage phase jump of $40°$ is shown in Fig. 6.7 with power set point at 0.9 pu P_{set}. The grid phase jump is simulated by changing θ_d in Fig. 6.5. From the power angle curve ($P - \delta$) of current limited and no limit cases, it is seen that the maximum phase shift between the infinite voltage source and GFC internal voltage is significantly

reduced from δ_{max} to δ_{max}^{lim}. For the simulated phase shift, the trajectory without limiter shifts from point 3 to 1 instantly and then falls back to 3. Whereas for GFC with the current limit, the trajectory instantly moves from 3-4 and thus marginally beyond the stable operating point 4 and loses synchronism. For a given P_{set} the maximum phase shift margin possible (δ_{mar}) can be solved from (6.9).

The inertia and damping parameters do not impact the stability margin as the instability expected is the instantaneous response.

6.4.3 GFC response voltage dip of infinite voltage source

The event simulates a power system fault case. The infinite bus voltage is reduced to 0.5 pu for 0.3 s with a P_{set} at 0.8 pu. The power angle curve reduces in magnitude with the reduction in infinite bus voltage, causing the virtual rotor to accelerate. For the unlimited case, the power angle trajectory is 1-2-5-7 and back to 1. The conventional equal area criterion for transient stability is applicable in this case, and the acceleration area 1-2-5-7 is well less than the decelerating area 5-7-9. However, the accelerating area 1-2-3-5 is higher for the current limited case than the available decelerating area 5-6-8 and the momentum gained during acceleration results in rotor angle crossing the unstable equilibrium point 8 and instability.

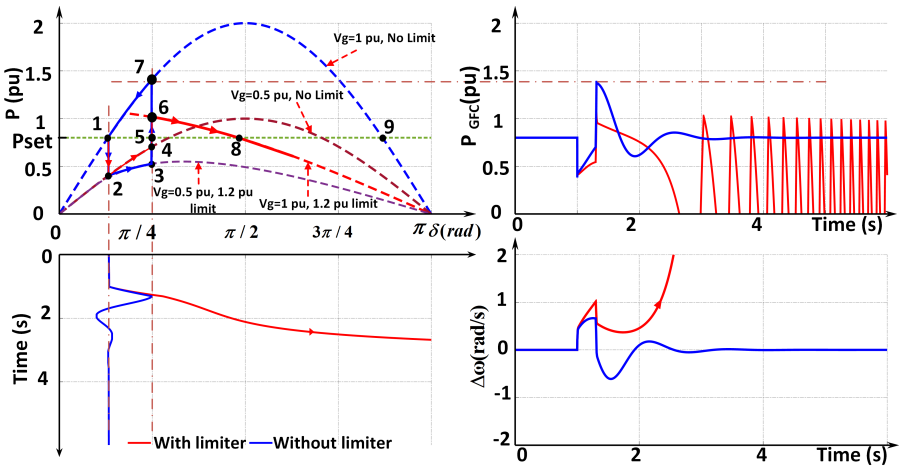

Figure 6.8: GFC response for a voltage dip of 0.5 pu

Most of the existing studies have only evaluated the transient stability of the GFC for fault cases. In practise, GFC is not a rotational rigid body as SG, wherein it is difficult to achieve the mechanical power input reduction during fault cases through fast valving or by dynamic braking resistors, thereby limiting the acceleration torque. However, both fast valving and dynamic braking can be easily implemented in a GFC by dynamically changing the power reference or simply freezing the power-based synchronization for a short duration [127, 128], provided there are sufficient capacity for energy dissipation. Another possibility is to increase in P-F droop Rd, increase programmed inertia H, the stability margin improves as the rotor acceleration is reduced with higher inertia and damping, unlike the RoCof case.

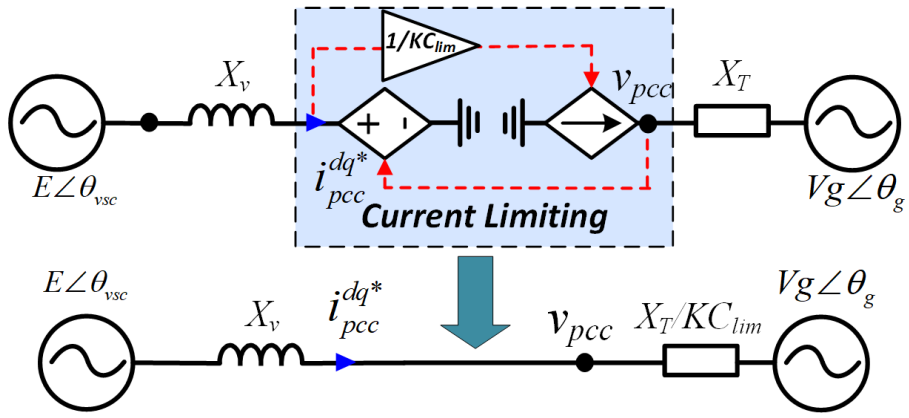

Figure 6.9: Electrical equivalent circuit of the GFC with unsaturated active power feedback as synchronisation during current limit

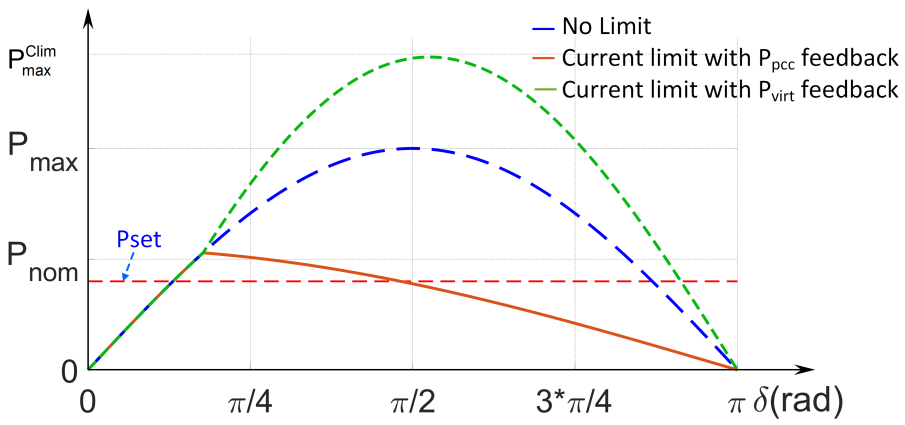

Figure 6.10: Power angle curves for GFC with and without limiter activation with virtual unsaturated power feedback for power synchronism loop

6.5 Proposed virtual power based GFC

The challenge with saturating current is that the active power output becomes insensitive to change of phase, thereby rendering the synchronization control ineffective and could need a backup voltage-based synchronization to operate stably. This chapter proposes utilizing the unsaturated current references (I_{pcc}^{dq*}) for power measurements for the synchronization loop instead of active power measurements at the PCC, i.e. the active power feedback to $APC(s)$ is chosen as

$$P_{fb} = P_{virt} = \frac{3}{2}(V_{pcc}^{d}.I_{pcc}^{d*} + V_{pcc}^{q}.I_{pcc}^{q*}) \tag{6.15}$$

One could also measure the virtual unsaturated power at the GFC virtual internal voltage terminals. Utilizing the virtual unsaturated power as the feedback or controlled parameters for the power synchronization is analysed in this section.

6.5.1 Analysis of virtual power based GFC

For calculation of the virtual power, the unsaturated current references are used, whereas the GFC actual output current when GFC enters the current limit is the saturated current defined by Eq.

(6.5). When the GFC is not in the current limit operation, there is no difference between the P_{virt} and P_{pcc} as long as the current dynamics are neglected. In practice, the current controller is much faster than the power control loop, and thus the impact of current control dynamics on the choice of power feedback is minimal. Hence an equivalent electrical circuit as shown in Fig. 6.9 can be drawn to represent the GFC employed with virtual power feedback. During the current limit operation with virtual power feedback, dividing the current reference by KC_{lim} is equivalent to dividing the net grid side reactance by KC_{lim} as shown in Fig. 6.9.

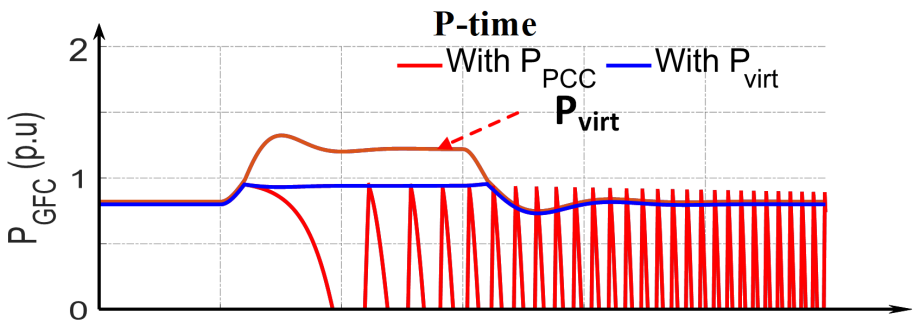

Figure 6.11: GFC response for a 1 Hz/s ROCOF with virtual power feedback

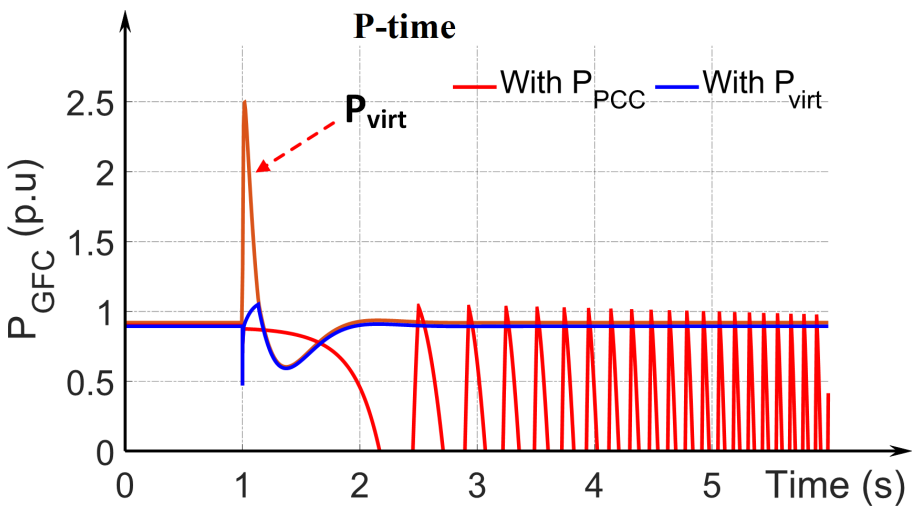

Figure 6.12: GFC response for a phase jump of 40 deg with virtual power feedback

From the equivalent circuit shown in Fig. 6.9 the unsaturated active and reactive power when when $|i_{pcc}| > I^{Lim}$ can be calculated

$$P_{unsat} = \frac{E * Vg * \sin\delta}{Xv + X_T/KC_{lim}}, Q_{unsat} = \frac{E^2 - E * Vg * \cos\delta}{Xv + X_T/KC_{lim}} \tag{6.16}$$

The KC_{lim} can be calculated similar to (6.8)

$$KC_{lim} = \frac{\sqrt{Vg^2 + E^2 - 2 * Vg * E * \cos(\delta)}}{Xv + X_T/KC_{lim}} * 1/I^{lim} \tag{6.17}$$

simplifying one can write

$$KC_{lim} = (\frac{Mv}{I^{lim}} - X_T)/Xv \tag{6.18}$$

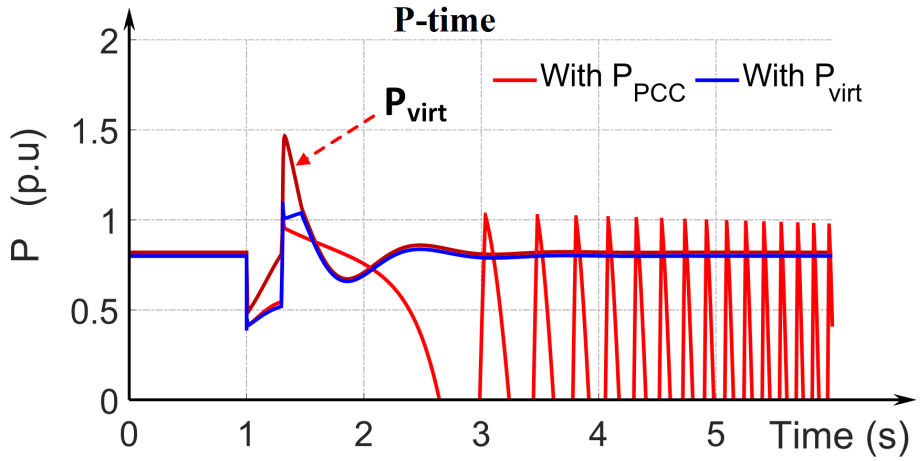

Figure 6.13: GFC response for a voltage dip of 0.5 pu with virtual power feedback

Table 6.1: PHIL Scaling for the VSC hardware

Symbol	Description	Physical Value	Scaled to Simulation
V_{vsc}	Amplifier voltage	123 V	12.3kV
P_{vsc}	VSC power	1.5 kVA	70 MVA

Thus virtual unsaturated power when $|i_{pcc}| > I^{Lim}$ for can be simplified and written as independent of KC_{lim} as

$$P_{virt} = P_{unsat} = \frac{E * Vg * \sin\delta}{X_v + Xv.XT/(Mv/I^{lim} - XT)} \tag{6.19}$$

From (6.16) and (6.19) one can easily observe that the current limit activation inherently extend the peak of the power angle characteristics when virtual power P_{virt} is utilized as the feedback variable even beyond the power transfer limit for unlimited case. This can be verified by plotting the power angle curve for GFC with virtual power feedback. This feature greatly increases the synchronization stability margin of all the cases discussed in the previous section.

The cases studies conducted in the previous section are repeated with virtual power feedback and the results are as depicted Fig. 6.11-6.13. As shown in the figures the GFC with virtual power feedback when in current limited operation can sustain all the large transient events discussed in this chapter.

6.6 Experimental results

The analysis presented in the previous section is validated through power hardware in the loop (PHIL) simulation. The configuration of the power hardware in the loop study is as shown in Fig. 6.14. Firstly, the PHIL study is conducted for GFC connected to an infinite voltage source to validate the analysis presented in section IV. The 230 kV infinite voltage source with Thevenin grid impedance and 230/12.3 kV transformer is simulated in Realtime Digital Simulator (RTDS). The per unit values of the grid impedances and tranformer impedances remain the same as in section

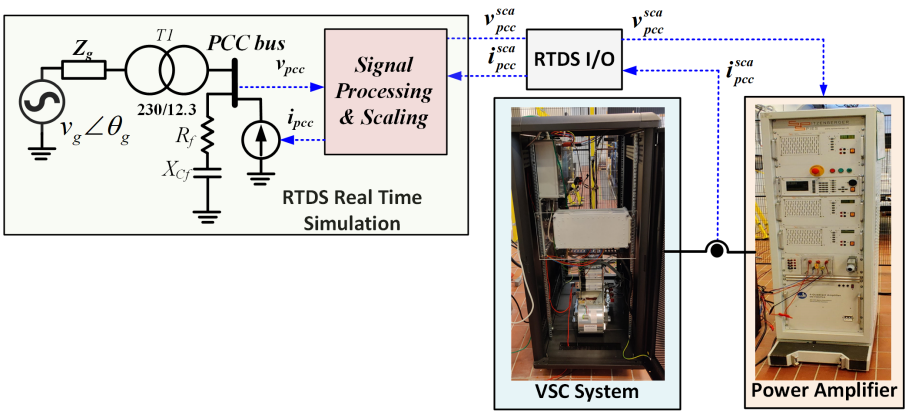

Figure 6.14: Power hardware in the loop configuration for GFC testing

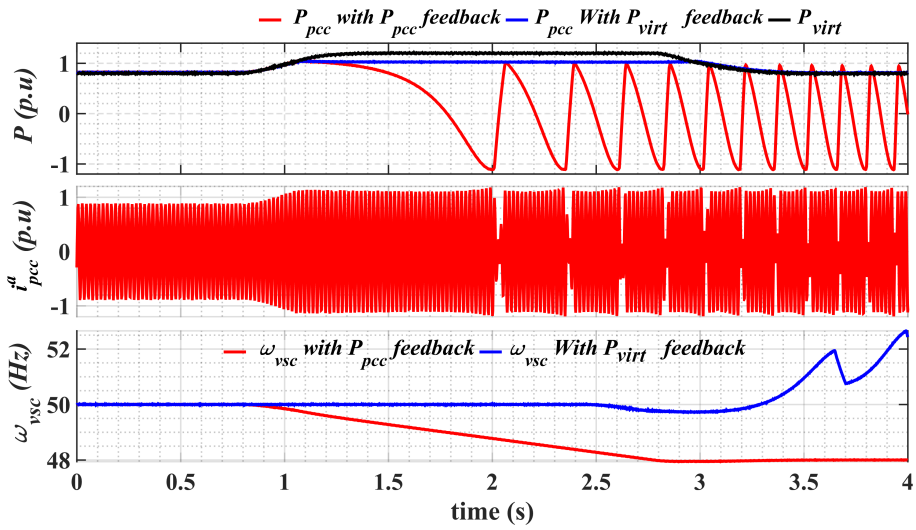

Figure 6.15: PHIL GFC connected to infinite voltage source, response for a 1 Hz/s ROCOF

IV with a base power of 100 MVA. A SEMIKRON SkiiP VSC stack with an inductive filter and current and voltage sensors and a 2.5 kVA SPITZENBERGER SPIES PAS 2500 linear amplifier are the hardware elements used in the experimental study. An Ideal Transformer interface method is used to interface the real-time simulation, and the hardware via the amplifier [76]. The RTDS I/O cards are used to exchange the PCC voltage from RTDS to the amplifier and the current coming into the amplifier to the RTDS. This exchange ensures that the VSC is part of the power system network. The voltage and current signal between the RTDS and the hardware is scaled, and the scaling ratio is shown in Table. 6.1. The current feedback signal is conditioned with a first-order low pass filter with a time constant of 250 μs to eliminate noise and ensure the stability of the PHIL. The VSC switching frequency is set to 10 kHz, and the inductive filter for the VSC stack is 8 mH. The GFC control with a proportional inner current control and the current limit discussed in the chapter is implemented on an FPGA-based digital controller from National Instruments (NI). The control is discretized using a trapezoidal integration method with a sampling time of 40 μs. The internal control variables such as P_{virt}, ω_{vsc} are captured in the NI controller and transferred to the real-time controller via direct memory access (DMA) first-in-first-out (FIFO) buffers and then saved to a file upon a configurable trigger event. The waveforms at the PCC are captured in the

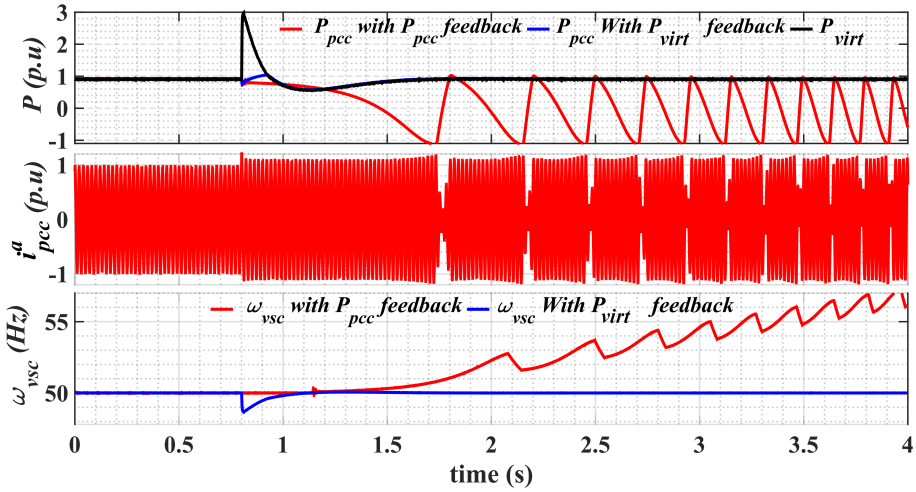

Figure 6.16: PHIL GFC connected to infinite voltage source, response for a phase jump of 40 deg

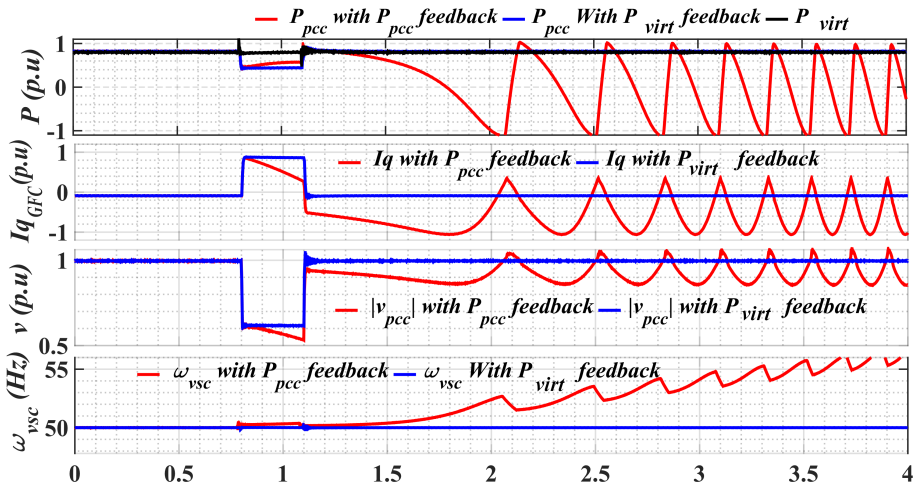

Figure 6.17: PHIL GFC connected to infinite voltage source, response for a voltage dip of 0.5 pu

RTDS run time interface. Both sets of data are exported to MATLAB and replotted for enhanced clarity. The PHIL results for the infinite bus case are shown in Fig. 6.15-6.17. The PHIL results shown for RoCoF, phase jump, and fault events are in good agreement with the analysis presented in Section IV. The reactive current at the PCC (Iq_{GFC}) is also plotted for the voltage dip case.

The PHIL study is expanded to a modified IEEE-9 system representative of future low inertia system with limited SG as shown in Fig. 6.18. Two of the synchronous generators of the at bus IEEE-9 bus system (at bus 3 and bus 1) are replaced with a commonly used 100 MVA grid following VSC's with active and reactive power control [129]. The parameters of the modified IEEE system is given in Appendix. The hardware GFC is connected to the IEEE 9 bus system at bus 9, the scaling and method of the PHIL interface remain the same as discussed before. The transmission line parameters are the same as the original IEEE 9 bus system [130]. The dispatch power of the SG in the system is adjusted to set the system frequency to 50 Hz. Also, the P-f droop of the SG governer is by default 5%. A generation disconnection event of the grid following VSC1 generating 100 MW is considered in this study. Two cases with different droop parameters and dispatch power from grid forming converter are considered in this study. The rotor of the synchronous generator has

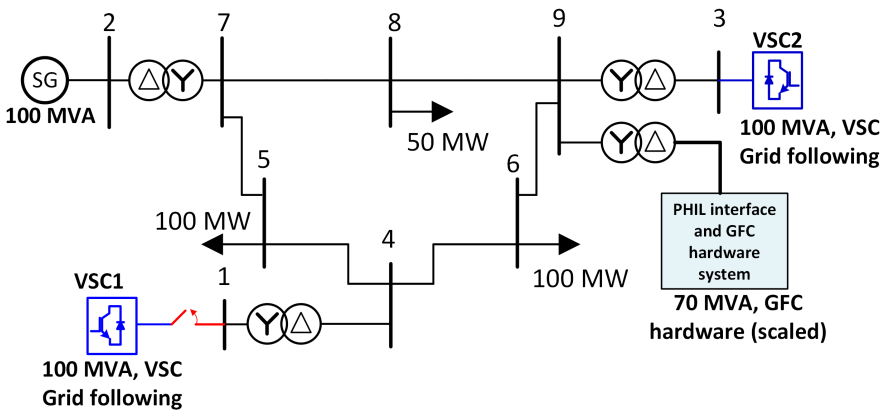

Figure 6.18: Power hardware in the loop with RTDS simulated modified IEEE-9 bus system

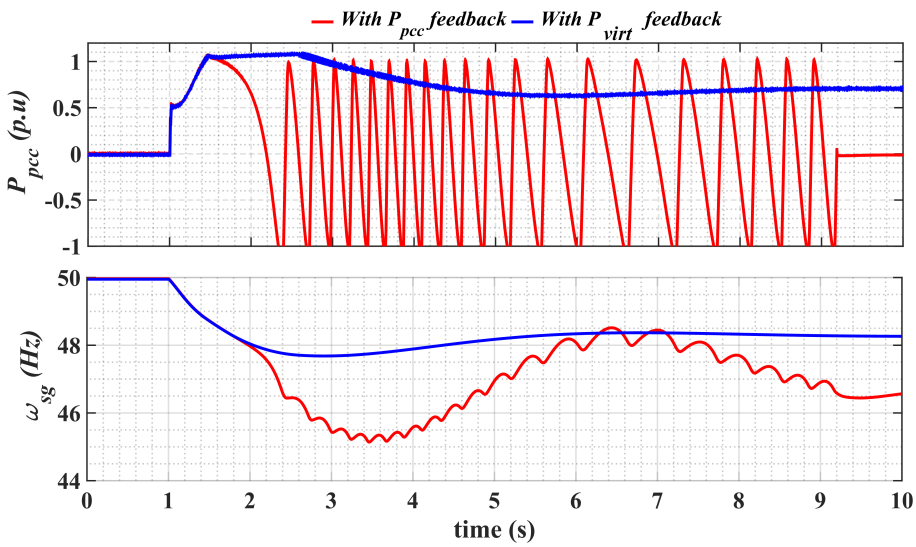

Figure 6.19: The response from GFC for the VSC1 disconnection event,H is 10 s, $P_{set}$of 0.0 pu, and P-f frequency droop R_d of 5%

under damped oscillatory behavior for a load or generation disconnection event. The response from GFC for the VSC1 disconnection event when the programmed inertia constant is 10 s and power setpoint of 0.5 pu is shown in Fig. The active power response of GFC, as well as the rotor speed of the SG(ω_{sg}), is shown in Fig. 6.19. And the response from GFC for the VSC1 disconnection event when the programmed inertia constant is 10 s and power setpoint of 0.0 pu, and P-f frequency droop R_d of 5% is shown in Fig.6.20 In both cases, GFC, when utilizing measured active power, loses synchronism. In contrast, a seamless entry to the current limiting and a seamless exit from the current limit is achieved when virtual active power is used for synchronization

6.7 Conclusion

The analysis presented in this chapter has revealed the potential loss of synchronisation of GFC is greatly accentuated when the GFC enters a current limited operation under different system transient events. This chapter presents the necessity to evaluate the transient stability problem with transients such as large frequency events, phase jumps, and voltage dips instead of limiting

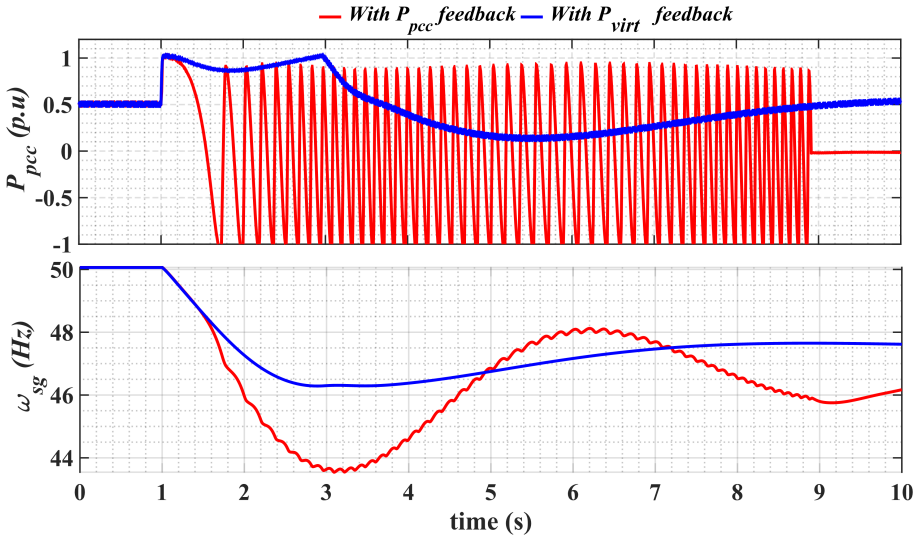

Figure 6.20: The response from GFC for the VSC1 disconnection event,H is 10 s, $P_{set}$of 0.5 pu, and no P-f frequency droop

the transient stability analysis just to a fault conditions. A quantitative and illustrative study for the GFC with current control operating against large transient is presented. The chapter proposes utilizing the internal virtual power derived from unsaturated current references for ensuring the synchronization under large transients when output GFC current is limited.

The results from the Power hardware in the loop (PHIL) experimental tests both on a single GFC connected to an infinite bus as well as on a modified IEEE-9 bus system demonstrates the transient stability challenges for a GFC and the validates of enhanced transient stability of using a virtual power for GFC synchronization.

Part III

Conclusions

CHAPTER 7

Conclusion and future work

7.1 Conclusion

The control system implemented in the power converters determines the dynamics and responses of the power converter. Thus, the converter control have potential to shape the overall power system dynamics with a substantial power converter presence in the power system. To that end, it is necessary to assess the converter controls to ensure a stable and reliable power supply. Therefore, this project evaluates the power converter controls, grid following, and grid forming controls for potential stability issues. Furthermore, possible interactions with the synchronous generator are identified, and control design guidelines based on the small-signal assessment are presented to increase the stability margin.

In this thesis, a detailed stability evaluation of GFC and GFL connected to an SG is performed and identified the challenges for the synchronization of GFC and GFL during transient events. In addition, control solutions to augment the synchronization of the converter control are also proposed in this thesis. Finally, the identified challenges in power converter synchronization blocks and proposed solutions are validated in developed power hardware in the loop platform. The conclusion of the dissertation is shown in detail in the following subsections.

7.1.1 Stability Challenges

A systematic stability evaluation of GFL connected to an SG has been conducted. Firstly, the stability analysis was conducted with only inner loops of the GFL, and it was revealed that a faster bandwidth of the current control and feedforward filter could mitigate the potential of oscillatory instability. In contrast, slower BW and higher PM of PLL are beneficial to a higher stability margin. The stability assessment, including outer active power and voltage control at low grid strength, identified a low-frequency oscillatory mode closely related to the voltage stability of the system. It is identified that a faster voltage control compared to the active power control can alleviate this oscillatory mode. To that end, it is revealed that in scenarios where the reactive current reference gets saturated, consequently disconnecting the voltage controller can trigger instability related to system voltage stability and also result in an adverse interaction with the SG. The current limit saturation can significantly change the GFL dynamics in the low-frequency range. Such changes in the dynamics can also be captured in the impedances of the GFL, which exhibits an increase in the low-frequency impedance. It is revealed that such an increase in the impedances due to limit triggering can adversely impact other components in the network, which in normal operation is stable. The presented design guidelines and stability evaluation of the GFL conducted with a focus on limit saturation can increase the understanding of the stability of power systems with significant GFL penetration and develop best practices for control design and identification of potential instabilities.

The focus of the small-signal study was the GFC's ability to behave like a voltage source behind an impedance. There are three GFC structures based on the difference in inner loop structures reported in the literature, (i) GFC with cascaded voltage control and current control, (ii) with inner current control only, (iii) with no inner loop. All the three GFC's are comprehensively evaluated in this thesis. A detailed small-signal analysis of two machine systems consisting of GFC and an SG is performed. Analyzing the GFC impedance revealed that MW level GFC with inner loops could have a nonpassive behavior in a specific frequency range depending on the control design. This nonpassive behavior can result in unstable oscillation in the system when the system's short circuit ratio is low. In addition, the interaction of GFC with SG electromechanical mode was assessed, which revealed that damping of the electromechanical mode could be reduced if GFC with cascaded voltage control is employed when compared to GFC with no inner loop or GFC with only current control. The electromechanical mode in SG was also found to be very sensitive to the control design of GFC inner loops. The passivity-based analysis and impedance analysis can reliably capture the potential instabilities and is an ideal tool for assessing black-box models. However, in the low-frequency range, especially within the bandwidth of the outer loops, the impedance matrix is not diagonally dominant. Thus the impedance assessment based on single-channel positive sequence impedance alone to assess the potential oscillations in the low-frequency range can lead to a wrong conclusion.

7.1.2 Transient Performance of Synchronization Unit

The GFL employs PLL which determines the phase of the PCC voltage as the synchronization unit. This thesis assessed the performance of the PLL under transient grid events. It is revealed that an undesirable coupling between the magnitude and phase of the input voltage is present for PLL's equipped with advanced filtering stages. Such coupling cannot be capture by the conventional linear PLL models and thus cannot be accounted for in the controller design. Therefore, a MIMO linear model of the PLL is proposed, which captures the full PLL dynamics during grid faults and voltage dips. This MIMO model can be used in PLLcontrol design and studies related to the transient performance of GFL. Furthermore, a generalized compensator that reduces the coupling between the estimated magnitude and phase of all PLL's with an advanced filtering stage is proposed. A demonstration of hardware GFL employed with the proposed compensation in PHIL simulation is evaluated when subjected to power system faults. It is demonstrated that the compensator ensures an accurate, current phase control and injection during faults to fulfill fast fault current injection requirements. The presented models and compensator for the PLL of GFL can enable the control designers to account for the dynamics of all the filters, (analog and digital) and thus improve the accuracy of the response of GFL during grid faults.

In contrast, a GFC utilizes the output active power for synchronization, which presents unique challenges when subjected to transients. Transient stability of synchronous machines and loss of synchronism during power system faults are well studied in the past. The GFC, which emulates inertia simillar to electromechanical implementation of the SG, is also prone to loss of synchronization during transient events. However, the GFC loss of synchronization is accentuated by the current limiters which are not typical for SG. This thesis studied the impact of these current limits on the ability of the GFC to maintain synchronism during transients. This thesis also revealed that transient events apart from the power system fault, such as phase jumps and a constant rate of frequency change, challenge GFC's ability to maintain synchronism. A detailed analysis of the GFC response for each transient event with current limit activation is presented. It is proposed

that utilizing the internal virtual power derived from unsaturated current references can ensure the synchronization under large transients when output GFC current is limited. It is also shown that the internal virtual power-based synchronism method can provide a much higher transient stability range during the current limited operation than the original system without the current limit.

7.1.3 Power Hardware in The Loop Study of VSC

Power hardware in the loop was developed as a part of this project as a high fidelity validation platform for the converter control developed in this project. Power hardware in the loop simulation for VSC allows the validation of VSC responses for system events. However, the delays in PHIL can limit the stable operating range. Therefore, this thesis evaluated the stability margin of the PHIL simulation of the current controlled VSC, and an analytical stability range of VSC-PHIL is derived.

7.2 Discussion and Future work

7.2.1 Discussion

The project outlined the small signal and large signal challenges due to VSC controls. The conducted analysis shows that the limiters in both GFC and GFL can pose small signal and large signal issues. Furthermore, in the event of such limit triggering in the converters, the Thevenin impedance is seen by the rest of the network can have high variabilities and negative resistances over a wide frequency range. Therefore, such current limit scenarios need to be carefully considered when SG is phased out, reducing system strength.

Although there are limiters such as field current and armature current limiters are present in the synchronous machine, these limiters are slow-acting. In addition, the synchronous machine field and armature windings have very high overload capacities and can sustain currents of magnitude multiple times their rated capacity. Therefore synchronous machines have a true voltage source characteristics, providing system strength, inertia, and resilience at all operating conditions. Thus when conventional SG's are replaced with a PE-based generation, challenges may arise.

Deploying large GFL with frequency GFC in a bulk power system is a solution to this problem. However, the technology readiness and market availability of the GFC in the near future is still a concern. MW level GFC-BESS is already providing fast frequency ancillary services installed in Australia [102] and MW level commercial GFC options for BESS are now available from manufacturers such as Hitachi ABB [78], SMA [79], and Tesla [131]. These GFC's internal controls and parameters are unknown due to Intellectual property rights. The same applies to the type of limiters and control mode changes internal to the converters. Thus to ensure system stability, one can use the black box models provided by the manufacturers, but care must be taken to capture all possible conditions such as internal reference saturation triggering of GFC/GFL. To that end, a unified testing framework to fully capture all the possible dynamics of the converters need to be developed.

In addition, the market availability of GFC solutions for RE integration is still limited(based on publicly available information). Although there have been MW-level field trials on the applicability of GFC for the wind farm [103], it is not known of the market availability of GFC wind turbines.

Thus one can still expect a large proportion of incoming RE and even BESS to be GFL while SG's are phased out. Thus services such as large inertia, fault current level, could be exclusively procured to be installed in the bulk grid to support this transition. The GFC with short/long term energy storage is one technology solution that can provide these services.

Another highly market-ready solution which can provide the inertial and short circuit current is the synchronous condenser (SC). Several European projects such as SCAPP [132] have verified the advantages of SC to provide inertia and shortcircuit level in system-level studies of the converter-dominated power system. The SC solution is also considered economically competent. For instance, the Stability Pathfinder – Phase 1 project by National Grid ESO aimed to procure inertia and fault current stability services to facilitate the GB electricity system to transition zero carbon by 2025 have awarded the tender to majorly SC-based solution even though the tender was for technology-neutral solution[133]. Also, the inertial constant of SC can be significantly boosted by mechanically coupling with flywheels (from 1-2 s to 10 s typical) is now available in the market[134].

A hybrid solution based on STATCOM and SC [135] which is the focus of the phoenix project with 140 MVA field trials, has also demonstrated that the economic and technical advantages in using a hybrid SC- and power converter solution for system services. A hybrid solution, including storage-based GFL-SC and GFC-SC, can maximize the complimentary benefits of VSC and SC and is also expected to play a key role in future power systems [136].

To summarize, the massive integration of GFC-based RE solution in bulk power grids is still some years away due to technology readiness level. Hence the bulk power system will compose of both GFC (in BESS) and GFL's will still form the majority of power converter based solutions in the near future. One can expect a significant level of the synchronous condensers to facilitate the energy transition at least during the short term.

7.2.2 Future Work

- A large number of GFC and GFL in the system presents challenges in the modeling and simulation perspective. Typically large system studies are conducted in RMS simulation. With the power converter's potential to instigate unstable oscillations at a large frequency range, as explained in this thesis, the system studies employing Root Mean Square (RMS) simulation will fail to capture these oscillations. One of the workarounds for this challenge is to define limits on the converters bandwidths, simillar to the one suggested by the National grid in the draft grid code for GFC. However, such an approach may pose practical difficulties due to complexities in converter control. More studies on RMS model development and a framework and test power systems for validating the RMS model against Electromagnetic Transient (EMT) model is missing in the literature.

- The GFL consists of several saturation blocks such as the current reference limit, modulation limit, frequency limiter in PLL, etc. As explained in the thesis, triggering one of the limiters changes the GFL system states as some loops become inactive, instantly changing the differential equations used to model the GFL. This thesis showed that limit triggering of active and reactive reference current and consequent mode changes in GFL could result in adverse interaction of GFL with the rest of the system. However, the analysis was conducted with linear methods such as small-signal analysis and impedance analysis, whereas these

limiter are highly non linear. Therefore, the nonlinear stability evaluation tools could provide more insight into these instabilities and suggest solutions to mitigate any potential instabilities. The GFL mode change could also be triggered due to fault ride through logic or supervisory controls, which increases the non linearity of the GFL system.

- The load dynamics are not considered in the study. The study could be expanded by including dynamic loads such as induction machine loads and constant power loads. The system study with dynamic loads would be particularly interesting during the fault recovery periods where there is high probability for one or more limiters in the GFL and GFC to be activated.

- The GFC virtual impedance-based current limit and circular current limit logic discussed in this thesis protect the GFC during transients. However, it introduces an additional impedance to do so. For sustained system events such as the fault-induced delayed recovery of the power system, it could be more beneficial to introduce other current limiting strategies such as reference voltage and power changes.

- This thesis does not consider dc-link dynamics. However, implementing the grid forming control on VSC with limited storage can be challenging since GFC has no direct control over power output. For emulating inertia, lack of direct power control can result in a significant drop in dc voltages in solutions such as STATCOM, which has only the limited stored energy in the capacitor to act as an energy buffer. In such cases, further study is necessary with regards to dc-link voltage management.

- For power system faults, which results in a large phase shift and voltage dip, the GFC can rides through the disturbance, however the response is unlike a voltage source with internal impedance due to current limit protection. A control strategy for GFC needs to implemented to deliver the necessary reactive power during such events.

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A. Appendix Modified IEEE 9 bus system data

The transmission line data parameters are the same as the original IEEE 9 bus system, the line and generator parameters are listed below at 100 MVA base. The developed RTDS runtime interface is shown in Fig. 1

Table 1: Transmission line parameters of IEEE 9 bus system

Line		R [pu/m]	X [pu/m]	B [pu/m]
From Bus	To Bus			
4	5	0.0100	0.0680	0.1760
4	6	0.0170	0.0920	0.1580
5	7	0.0320	0.1610	0.3060
6	9	0.0390	0.1738	0.3580
7	8	0.0085	0.0576	0.1490
8	9	0.0119	0.1008	0.2090

Table 2: Generator Data

GEN	Xa (pu)	Xd (pu)	Xd' (pu)	Xd" (pu)	Xq (pu)	Xq' (pu)	Xq" (pu)
1	0.08958	0.8958	0.1198	0.11	0.8645	0.1969	0.11

Table 3: Generator data continued

GEN	Ra (pu)2	Tdo' (s)	Tdo" (s)	Tqo' (s)	Tqo" (s)	H (s)	D(pu/pu)
1	0.000125	6.00	0.01	0.535	0.01	6.40	0.0

Table 4: Exciter Data-1 (IEEE Type DC1A)

GEN	KA	TA	VRmin	VRmax	KE	TE	KF	TF	EX1	S(EX1)	EX2	S(EX2)
1	20.0	0.2	-5.0	5.0	1.0	0.314	0.063	0.35	3.3	0.6602	4.5	4.266

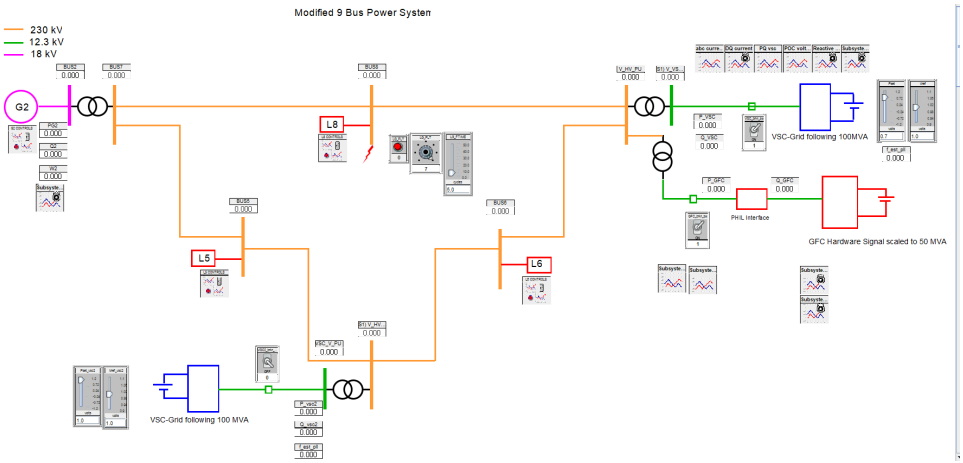

Figure 1: Developed RTDS runtime interface

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