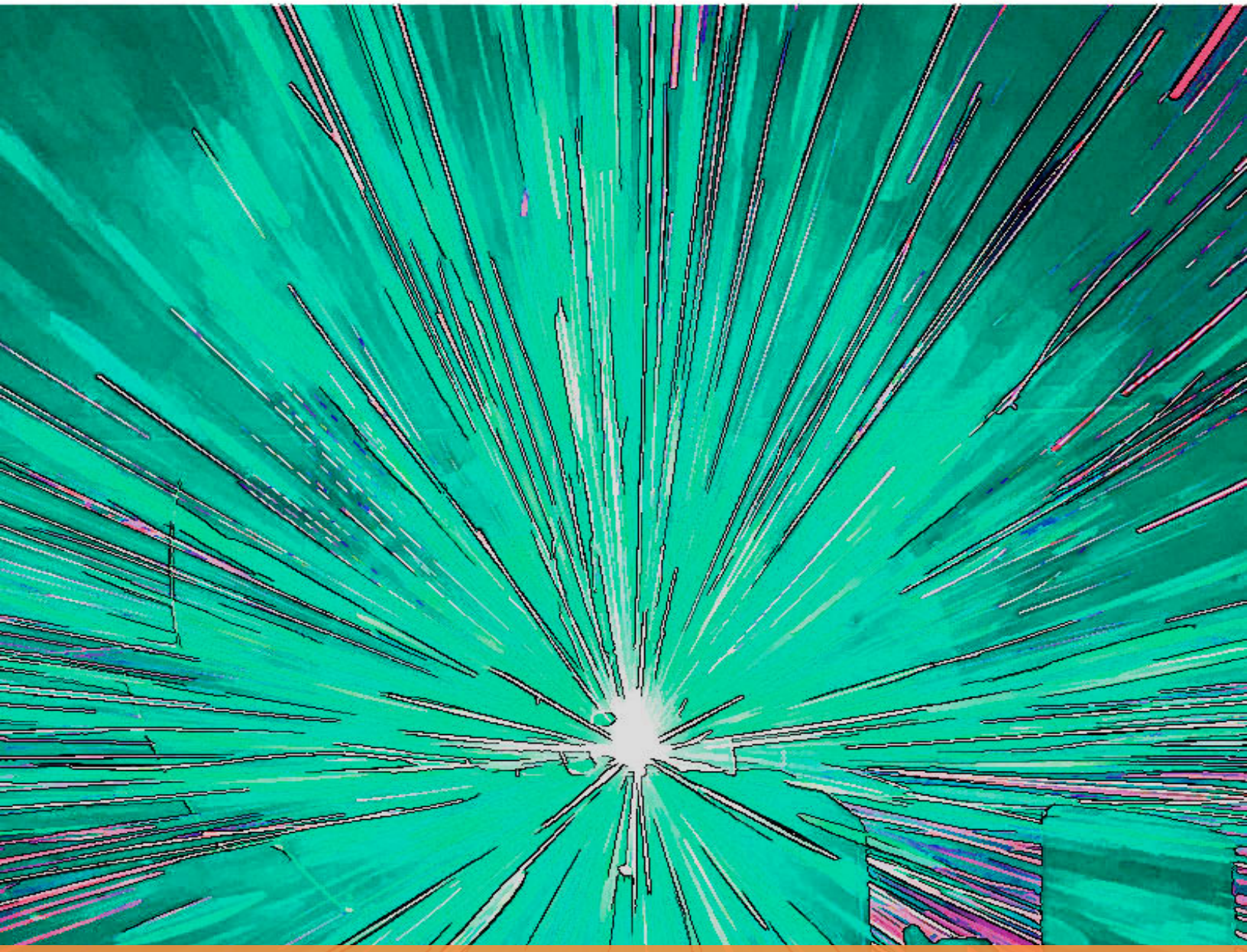
bookboon
LEARNING



CMOS Analog IC Design: Problems and Solutions

Erik Bruun

ERIK BRUUN

CMOS ANALOG IC DESIGN

PROBLEMS AND SOLUTIONS

CMOS Analog IC Design: Problems and Solutions
3rd edition

ISBN 978-87-403-4248-2

CONTENTS

Preface

This book contains the end-of-chapter problems for each of the chapters in the book 'CMOS Analog IC Design: Fundamentals' (3rd Edition, 2022, also published by Bookboon) and provides solutions to the problems.

Often, there is not just one possible way of solving the problems. Many problems may be solved using hand calculations, computer calculations or simulations. For calculations, different computer programs may be used. Many students prefer to use tools such as Maple or Matlab when solving equations. For simulations of analog CMOS circuits, Spice is the generally accepted simulation program and it is available in many different versions, including PSpice, HSPICE, LTspice and several others.

For 'CMOS Analog IC Design: Fundamentals', LTspice has been chosen as the circuit simulation program and the solutions presented in this book are based on LTspice simulations whenever appropriate. LTspice is freely available for download from
http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

For mathematical solutions, no computer tools have been applied. The problems have been designed to result in equations which are sufficiently simple to be solved merely by hand calculations.

The problems are reprinted from 'CMOS Analog IC Design: Fundamentals', and table and figure references given in the problems are to tables and figures from this book. Several problems use transistor parameters from 'CMOS Analog IC Design: Fundamentals', and for convenience, these are reprinted in the Appendix in this book. Also, figures from 'CMOS Analog IC Design: Fundamentals' referred to in the problems are reprinted in this book.

Erik Bruun
Department of Electrical Engineering, Technical University of Denmark.

Chapter 1 – Introduction

Multiple-choice test

1. Completed statements:

A-11:	CMOS is an abbreviation for complementary metal-oxide-semiconductor.
B-17:	Modern CMOS processes normally use minimum device dimensions in range 1 - 1000 nm.
C-4:	The most commonly used material for CMOS technology is silicon.
D-13:	Gordon Moore presented his first prediction of semiconductor device scaling in 1965.
E-16:	According to Moore's law, the number of devices per die increases exponentially with time.
F-10:	Device downscaling is mostly beneficial for digital circuits.
G-1:	In analog integrated circuit design, the schematic design and analysis is verified through circuit simulation.
H-14:	SPICE is an abbreviation for Simulation Program with Integrated Circuit Emphasis.

2. According to Moore's law from 1975, what is the expected factor of increase in device count per die per 10 years?

   A: 10
   B: 32
   C: 1024

Solution:

Moore's law from 1975 states that the device count per die increases by a factor of two for every second year. Thus, in 10 years, the factor of increase is $2^5 = 32$.

3. Assuming a constant die area and a device count increase by a factor of two in two years, what is the scaling factor per year of the linear device dimensions?

   A: 0.84
   B: 0.71
   C: 0.50

Solution:

With a constant die area, a device count increase by a factor of two per two years require a scale factor of the linear device dimensions of $1/\sqrt{2}$ in two years, i.e., a scale factor of $\sqrt{1/\sqrt{2}} = 0.84$ per year.

4. Assuming a linear scaling factor of 0.84 per year, what would be a typical device dimension in 2024 if 28 nm is a typical device dimension in 2019?

   A: 7 nm
   B: 12 nm
   C: 20 nm

Solution:

With a linear scaling factor of 0.84 per year, the scaling factor for 5 years is $0.84^5 = 0.42$, so with a typical device dimension of 28 nm in 2019, the typical device dimension in 2024 is $0.42 \times 28\ \text{nm} = 11.8\ \text{nm} \simeq 12\ \text{nm}$.

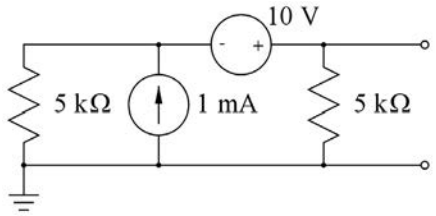
Chapter 2 – Basic Concepts

Multiple-choice test

1. Completed statements:

A-3:	Kirchhoff's current law (KCL) states that the algebraic sum of currents flowing into a node equals zero.
B-1:	Kirchhoff's voltage law (KVL) states that the algebraic sum of voltages across circuit elements equals zero for any closed path (loop) in an electric circuit.
C-9:	Kirchhoff's laws are valid for both linear and nonlinear circuits.
D-6:	The device equation for a resistor is known as Ohm's law.
E-8:	The device equation for a capacitor is $i = C(dv/dt)$.
F-15:	In a dc analysis, an inductor is replaced by a short circuit.
G-11:	A Thévenin equivalent circuit is an independent voltage source in series with an impedance.
H-16:	A small-signal device model is a linearized device model.
I-14:	When an independent current source is reset, it corresponds to an open circuit.
J-10:	The superposition principle is valid for linear circuits only.

2. The Thévenin resistance for the circuit shown below is



A: 2.5 kΩ
B: 5 kΩ
C: 10 kΩ

Solution:

We find the Thévenin resistance by resetting the current source and the voltage source and calculating the resistance between the terminals. When the voltage source and the current source are reset, the circuit is reduced to a parallel connection of two resistors of 5 kΩ, so the Thévenin resistance is $R_t = 5\ \text{k}\Omega \parallel 5\ \text{k}\Omega = 2.5\ \text{k}\Omega$.

3. The contribution to the Thévenin voltage from the 1 mA current source in the circuit above is

A: 2.5 V
B: 5 V
C: 10 V

Solution:

For finding the contribution to the Thévenin voltage from the 1 mA current source, we use the superposition principle and calculate the voltage between the terminals when the 10 V voltage source is reset. The voltage is $V_{t1} = 1\text{ mA} \times (5\text{ k}\Omega \parallel 5\text{ k}\Omega) = 2.5\text{ V}$.

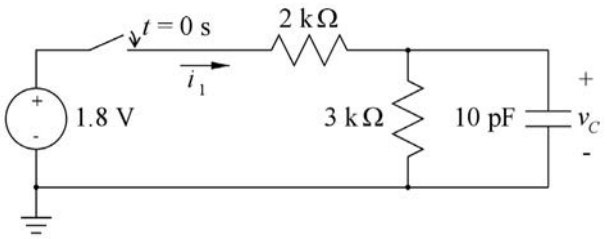
4. The contribution to the Thévenin voltage from the 10 V voltage source in the circuit above is

   A: 2.5 V
   B: 5 V
   C: 10 V

Solution:

For finding the contribution to the Thévenin voltage from the 10 V voltage source, we use the superposition principle and calculate the voltage between the terminals when the 1 mA current source is reset. Using Ohm's law, we find the current through the resistors and the voltage source to be $I = 10\text{ V}/(5\text{ k}\Omega + 5\text{ k}\Omega) = 1\text{ mA}$, and using Ohm's law, we find the voltage between the terminals to be $V_{t2} = 1\text{ mA} \times 5\text{ k}\Omega = 5\text{ V}$.

5. In the circuit shown below, the switch is closed at time $t = 0$. Immediately after the switch is closed, the current i_1 is



   A: 0.36 mA
   B: 0.90 mA
   C: 1.5 mA

Solution:

Immediately after the switch is closed, the voltage across the capacitor is $v_C = 0$, so the voltage across the 2 kΩ resistor is 1.8 V and the current i_1 is $i_1 = 1.8\text{ V}/2\text{ k}\Omega = 0.9\text{ mA}$.

6. When the switch is re-opened in the circuit above, the capacitor discharges with a time constant of

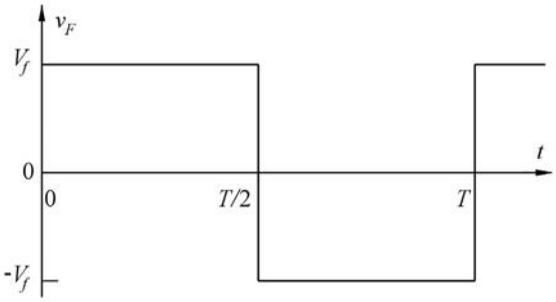
   A: 12 ns
   B: 30 ns
   C: 50ns

Solution:

When the switch is re-opened, the capacitor is discharged through the 3 kΩ resistor connected in parallel with the capacitor. No current flows in the 2 kΩ resistor. This gives a time constant for discharging of $\tau = 3\text{ k}\Omega \times 10\text{ pF} = 30\text{ ns}$.

Problems

Problem 2.1



A symmetric square-wave voltage signal $v_F(t)$ as shown above is described by the Fourier series

$$v_F(t) = \frac{4V_f}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin((2n+1)\omega t)$$

where $\omega = (2\pi)/T$. Assume that $v_F(t)$ is connected across a resistor R. Find an expression for the total average power dissipated in the resistor. What fraction of the power is in the fundamental frequency? What fraction of the power is in the 3rd harmonic and in the 5th harmonic?

Solution:

Total average power:

$$P_{\text{avg}} = \frac{1}{R}\frac{1}{T}\int_0^T v_F(t)^2 dt = \frac{1}{R}\frac{1}{T}V_f^2 T = \frac{V_f^2}{R}$$

Power in fundamental frequency, $n = 0$:

$$P_{\text{fund}} = \frac{1}{R}\frac{1}{T}\int_0^T \left(\frac{4V_f}{\pi}\right)^2 \sin^2(\omega t)dt = \frac{1}{2R}\left(\frac{4V_f}{\pi}\right)^2$$

Fraction of power in fundamental frequency:

$$\frac{P_{\text{fund}}}{P_{\text{avg}}} = \frac{8}{\pi^2}\times 100\% = 81\%$$

Power in 3rd harmonic, $n = 1$:

$$P_{3\text{rd}} = \frac{1}{R}\frac{1}{T}\int_0^T \left(\frac{4V_f}{\pi}\right)^2\left(\frac{1}{3}\right)^2 \sin^2(3\,\omega t)dt = \frac{1}{2R}\left(\frac{4V_f}{3\,\pi}\right)^2$$

Fraction of power in 3rd harmonic:

$$\frac{P_{3\text{rd}}}{P_{\text{avg}}} = \frac{8}{9\pi^2}\times 100\% = 9\%$$

Power in 5th harmonic, $n = 2$:

$$P_{5\text{th}} = \frac{1}{R}\frac{1}{T}\int_0^T \left(\frac{4V_f}{\pi}\right)^2\left(\frac{1}{5}\right)^2 \sin^2(5\,\omega t)dt = \frac{1}{2R}\left(\frac{4V_f}{25\,\pi}\right)^2$$

Fraction of power in 5th harmonic:

$$\frac{P_{5\text{th}}}{P_{\text{avg}}} = \frac{8}{25\,\pi^2} \times 100\% = 3.2\%$$

Problem 2.2

A sinusoidal voltage signal v_A is characterized as follows: The frequency is 3 kHz. The maximum value is 700 mV. The minimum value is 300 mV. The value for time $t = 0$ is 400 mV. Find V_A, V_a, ω and θ for describing the signal in the time domain using the expression $v_A = V_A + V_a \cos(\omega t + \theta)$.

Solution:

The dc value V_A may be found as the average of the maximum value and the minimum value,
i.e., $V_A = (700\text{ mV} + 300\text{ mV})/2 = 500\text{ mV}$.
The amplitude V_a may be found as the maximum value minus the dc value,
i.e., $V_a = 700\text{ mV} - 500\text{ mV} = 200\text{ mV}$.
The angular frequency ω is $\omega = 2\,\pi\,f = 2\,\pi \times 3\text{ kHz} = 18.85 \times 10^3$ rad/s.
The phase angle θ may be found from the value of v_A at $t = 0$,
i.e., $400\text{ mV} = 500\text{ mV} + 200\text{ mV}\cos\theta \Rightarrow \cos\theta = -1/2 \Rightarrow \theta = 120°$.

Problem 2.3

A signal $V_o(j\omega)$ is described in the frequency domain by the following the relation:

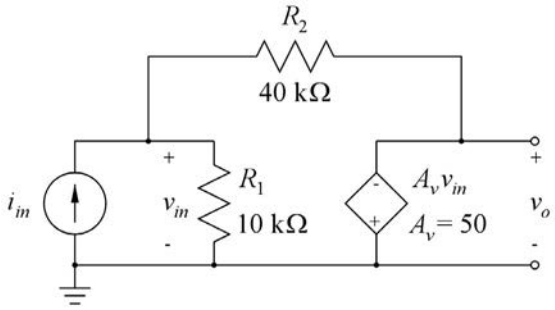
$$V_o(j\omega) = \frac{V_i(j\omega)}{1 + j\omega/\omega_0}$$

The signal $V_i(j\omega)$ is a sinusoid with an amplitude $|V_i(j\omega)| = V_a$ and a phase angle $\theta = 0°$.
For a frequency $\omega = 2\,\omega_0$, find the amplitude and phase of $V_o(j\omega)$ and find an expression for $v_O(t)$ in the time domain.

Solution:

From $V_o(j\omega) = \dfrac{V_i(j\omega)}{1 + j\omega/\omega_0}$, we find for $\omega = 2\,\omega_0$:
$|V_o(j\omega)| = \dfrac{|V_i(j\omega)|}{|1 + j2|} = \dfrac{V_a}{\sqrt{1+2^2}} = V_a/\sqrt{5} = 0.447\,V_a$;
$\angle V_o(j\omega) = -\arctan(\omega/\omega_0) = -\arctan(2) = -63.4°$;
$v_O(t) = |V_o(j\omega)|\cos(\omega t + \angle V_o(j\omega)) = 0.447\,V_a\cos(2\,\omega_0 t - 63.4°) = 0.447\,V_a\cos(2\,\omega_0 t - 1.107\text{ rad})$.

Problem 2.4



The circuit shown above is a transresistance amplifier built from an inverting voltage amplifier with an input resistance of $R_1 = 10\,\text{k}\Omega$ and an inverting voltage gain of $A_v = 50$ V/V. The feedback resistor $R_2 = 40\,\text{k}\Omega$ turns it into a transresistance amplifier with a transresistance $R_m = v_o/i_{in}$.
Find the transresistance R_m and the input resistance $R_{in} = v_{in}/i_{in}$ as functions of R_1, R_2 and A_v and calculate numerical values for the specified values of R_1, R_2 and A_v.
Verify your results by simulating the circuit with LTspice.

Solution:

A node equation at the input gives

$$i_{in} = \frac{v_{in}}{R_1} + \frac{v_{in} - v_o}{R_2}$$

Inserting $v_{in} = -v_o/A_v$ results in

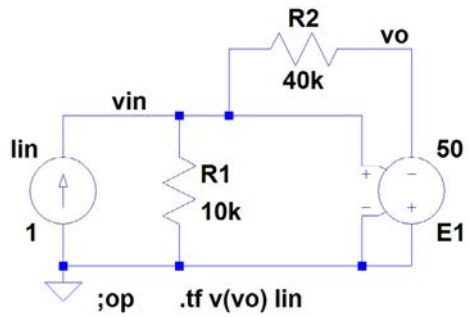
$$\begin{aligned} i_{in} &= -\frac{v_o}{A_v R_1} - \frac{v_o(1/A_v + 1)}{R_2} \\ &= -v_o\left(\frac{1}{A_v}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{1}{R_2}\right) \\ \Rightarrow\ R_m = \frac{v_o}{i_{in}} &= -\left(\frac{1}{A_v}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{1}{R_2}\right)^{-1} = -R_2 \parallel [A_v(R_1 \parallel R_2)] \end{aligned}$$

The input resistance is found from

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{-v_o/A_v}{i_{in}} = -\frac{R_m}{A_v} = (R_1 \parallel R_2) \parallel (R_2/A_v)$$

Inserting $R_1 = 10\,\text{k}\Omega$, $R_2 = 40\,\text{k}\Omega$ and $A_v = 50$, we find $R_m = -36.4\,\text{k}\Omega$ and $R_{in} = 727\ \Omega$.

The numerical results may be verified by simulation. The following figure shows an LTspice schematic corresponding to Problem 2.4. From a '.op' simulation with '`Iin = 1`', we find R_m as the value of '`vo`' and R_{in} as the value of '`vin`'. Alternatively, a '.tf' simulation with '`v(vo)`' as the output and '`Iin`' as the source directly results in R_m as the transfer function and R_{in} as the input impedance.

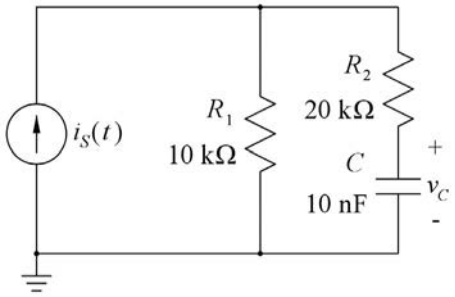


Results from '.tf' simulation.

```
        --- Transfer Function ---

Transfer_function:          -36363.6  transfer
iin#Input_impedance:          727.273  impedance
output_impedance_at_V(vo):          0  impedance
```

Problem 2.5



For the circuit shown above, $i_S(t)$ is a current source with the value 0 for $t \leq 0$ and 1 mA for $t > 0$. Find the value of v_C at time $t = 0$. Find the value of v_C for $t \to \infty$. Find the time constant for the charging of the capacitor C. Sketch the voltage $v_C(t)$ as a function of time t for $0 \leq t \leq 1$ ms.
Verify your results by simulating the circuit with LTspice.

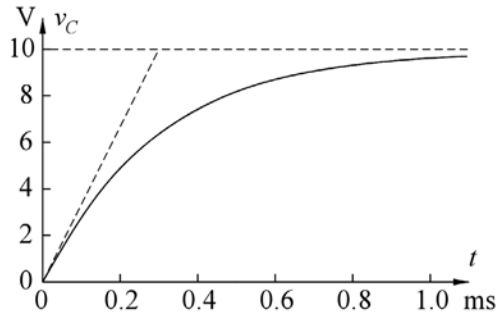
Solution:

For $t \leq 0$, the current source i_S is 0 and the capacitor C is discharged by the series connection of R_1 and R_2, so $v_C(t \leq 0) = 0$.

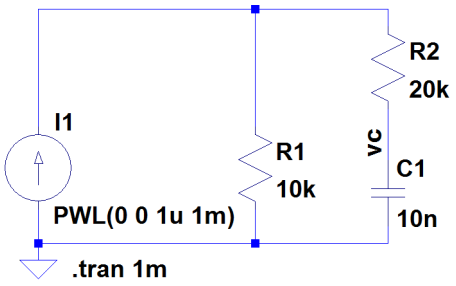
For $t \to \infty$, the circuit approaches a dc steady state, so the current in C is 0. This implies that also the current in R_2 is 0, and a node equation at the top end node connecting i_S, R_1 and R_2 shows that the current i_S flows through R_1, creating a voltage across R_1 of $i_S R_1 = 10$ V. Since the voltage across R_2 is 0, it follows from Kirchhoff's voltage law that the voltage v_C across C is also 10 V, i.e., $v_C(t \to \infty) = 10$ V.

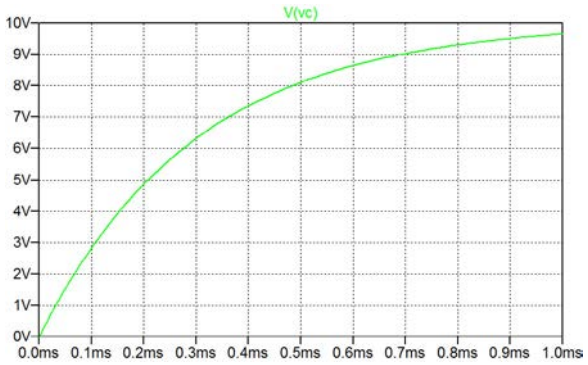
Replacing i_S and R_1 by a Thévenin equivalent circuit with $V_t = i_S R_1$ and $R_t = R_1$, we see that C is charged from V_t through the series connection of R_1 and R_2, so the time constant for charging is $\tau = (R_1 + R_2)C = 0.3$ ms.

The following figure shows a plot of $v_C(t)$ versus time t.

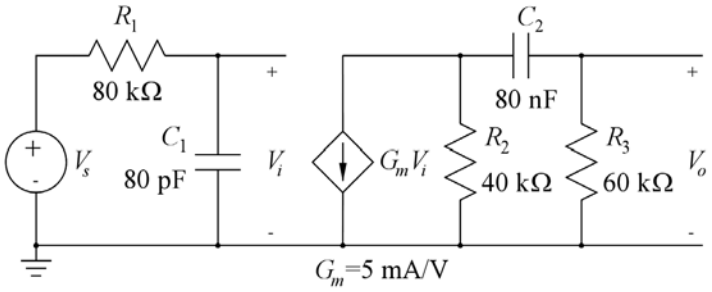


For verification by LTspice, an LTspice schematic and the resulting output plot from a '.tran' simulation is shown below. For the specification of the current source, a piecewise linear current with a rise time of 1 µs, i.e., $\ll \tau$, has been used. The similarity to the analytically derived plot is apparent.





Problem 2.6



For the circuit shown above, find the transfer function $H(s) = V_o(s)/V_s(s)$ and find the -3 dB cutoff frequencies. Sketch the magnitude of the transfer function in a Bode plot.
Hint: Find $H(s)$ as the product of $(V_i(s)/V_s(s))$ and $(V_o(s)/V_i(s))$.
Verify your results by simulating the circuit with LTspice.

Solution:

Using voltage division, we find $\dfrac{V_i(s)}{V_s(s)} = \dfrac{1/(sC_1)}{R_1 + 1/(sC_1)} = \dfrac{1}{1+sC_1R_1}$

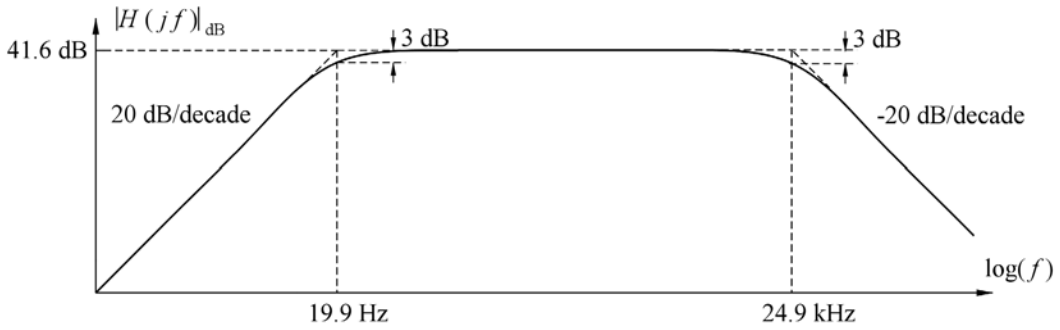
Next, $(G_mV_i(s)) \parallel R_2$ can be replaced by a Thévenin equivalent circuit with $V_t = -G_mV_i(s)R_2$ and $R_t = R_2$. Using voltage division, we find

$$V_o(s) = V_t \frac{R_3}{R_t + 1/(sC_2) + R_3} = -G_mV_i(s)R_2 \frac{R_3sC_2}{1+sC_2(R_2+R_3)} \Rightarrow \frac{V_o(s)}{V_i(s)} = -\frac{G_mR_2R_3sC_2}{1+sC_2(R_2+R_3)}$$

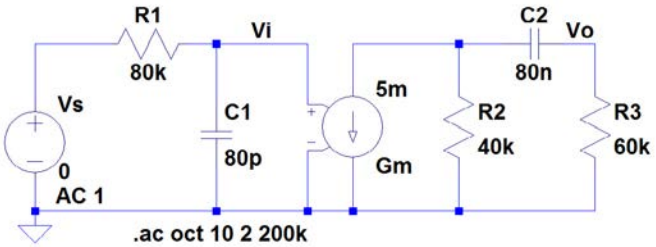
Finally, $H(s) = \dfrac{V_o(s)}{V_s(s)} = \dfrac{V_o(s)}{V_i(s)}\dfrac{V_i(s)}{V_s(s)} = -\dfrac{G_mR_2R_3sC_2}{(1+sC_2(R_2+R_3))(1+sC_1R_1)}$

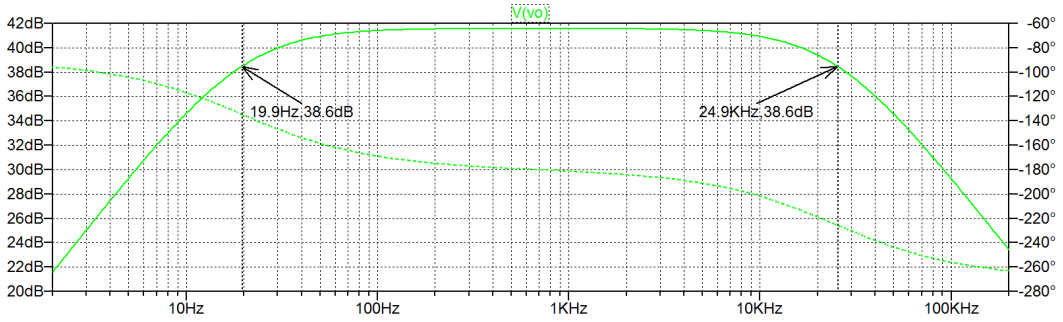
We notice that there are two poles in the transfer function and a zero at $s = 0$. The pole frequencies, corresponding to the -3 dB cutoff frequencies, are $f_{p\,\text{low}} = (2\pi C_2(R_2+R_3))^{-1} = 19.9$ Hz and $f_{p\,\text{high}} = (2\pi C_1R_1)^{-1} = 24.9$ kHz.

For plotting the magnitude, we also calculate the midband gain as the gain with C_1 replaced by an open circuit and C_2 replaced by a short circuit, i.e., $|H_{\text{midband}}| = G_m(R_2 \parallel R_3) = 120$ V/V ~ 41.6 dB. A Bode plot of the magnitude of the frequency response is shown below.

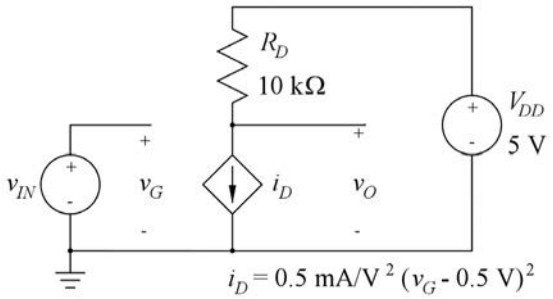


For verifying the results by simulation, we use the LTspice schematic shown below and run a '.ac' simulation. The plot from the simulation is also shown, clearly verifying the analytically derived results.





Problem 2.7

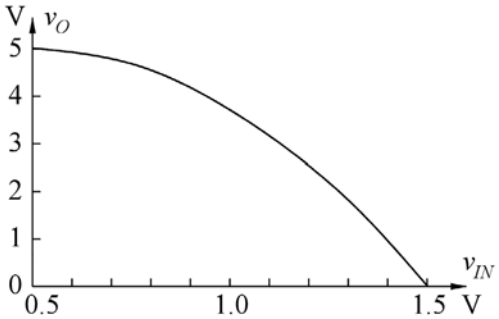


Shown above is a nonlinear transconductance amplifier. Find the values of bias voltages and currents for an input bias voltage (quiescent voltage) of $V_{IN} = 1.0$ V. Sketch the output voltage v_O versus the input voltage v_{IN} for 0.5 V $\leq v_{IN} \leq$ 1.5 V. Find the small-signal voltage gain v_o/v_{in} versus the input bias voltage V_{IN} for 0.5 V $\leq V_{IN} \leq$ 1.5 V and calculate the value of the small-signal gain for $V_{IN} = 1.0$ V. Verify your results by simulating the circuit with LTspice.

Solution:

With $V_{IN} = 1.0$ V, we find $V_G = V_{IN} = 1.0$ V, $I_D = 0.5\ \text{mA/V}^2\,(1.0\ \text{V} - 0.5\ \text{V})^2 = 0.125$ mA, and $V_O = V_{DD} - R_D I_D = 3.75$ V.

The output voltage is $v_O = V_{DD} - R_D\, i_D = 5\ \text{V} - 5\ \text{V}^{-1}(v_{IN} - 0.5\ \text{V})^2$, and this relation is sketched below.



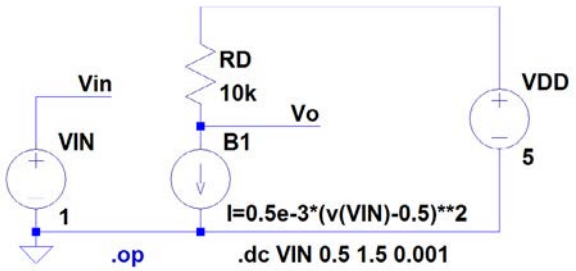
Small-signal gain:

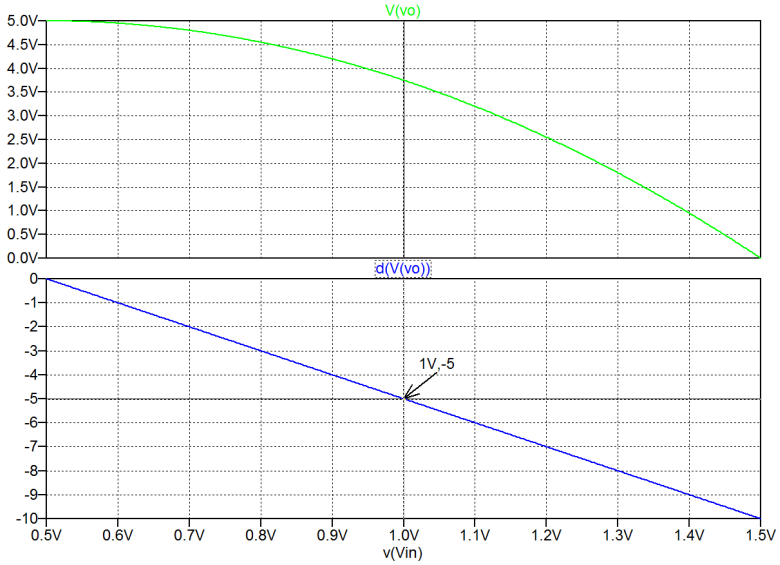
$$\frac{v_o}{v_{in}} = \left.\frac{\partial v_O}{\partial v_{IN}}\right|_{v_{IN}=V_{IN}} = \left.\frac{\partial}{\partial v_{IN}}(V_{DD} - R_D\, i_D)\right|_{v_{IN}=V_{IN}} = -R_D \left.\frac{\partial i_D}{\partial v_{IN}}\right|_{v_{IN}=V_{IN}}$$

$$= -10\ \text{V}^{-1}(V_{IN} - 0.5\ \text{V}) = 5\ \text{V/V} - 10\ \text{V}^{-1} \cdot V_{IN}$$

For $V_{IN} = 1.0$ V, we find $\dfrac{\partial v_O}{\partial v_{IN}} = -5$ V/V.

When simulating the circuit using LTspice, the controlled current source i_D may be modeled by an arbitrary behavioral current source, device type 'bi', as shown in the schematic below. Using a '.op' simulation, the bias point may be verified, and using a '.dc' simulation, the sketch of the relation between input voltage and output voltage may be verified, see plot below.





Problem 2.8

Derive an expression for the small-signal voltage gain v_o/v_{in} for an amplifier with the nonlinear transfer function

$$v_O = \frac{10\text{ V}}{1+\exp(-5\text{ V}^{-1}\cdot v_{IN})}.$$

Calculate the small-signal voltage gain for $V_{IN} = -0.3$ V, 0 V and +0.3 V.

Solution:

We find the gain as

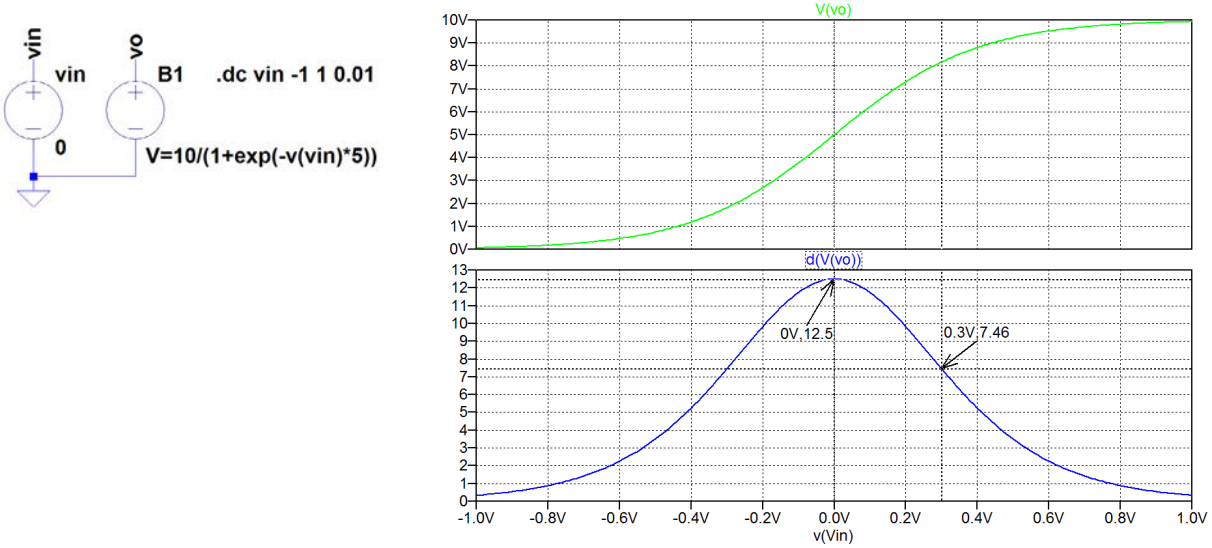
$$\frac{v_o}{v_{in}} = \left.\frac{\partial v_O}{\partial v_{IN}}\right|_{v_{IN}=V_{IN}} = \frac{\partial}{\partial v_{IN}}\left(\frac{10\text{ V}}{1+\exp(-5\text{ V}^{-1}\cdot v_{IN})}\right)\Bigg|_{v_{IN}=V_{IN}} = \frac{50\exp(-5\text{ V}^{-1}\cdot V_{IN})}{(1+\exp(-5\text{ V}^{-1}\cdot V_{IN}))^2}$$

$$= \frac{50}{\exp(5\text{ V}^{-1}\cdot V_{IN})(1+\exp(-5\text{ V}^{-1}\cdot V_{IN}))^2} = \frac{50}{2+\exp(5\text{ V}^{-1}\cdot V_{IN})+\exp(-5\text{ V}^{-1}\cdot V_{IN})}$$

For $V_{IN} = 0$ V, we find $v_o/v_{in} = 12.5$ V/V.

For $V_{IN} = \pm 0.3$ V, we find $v_o/v_{in} = 7.46$ V/V.

The small-signal gains may also be verified using LTspice. In the LTspice schematic shown below, the amplifier is modeled as an arbitrary behavioral voltage source with the specified relation between input voltage and output voltage. The plot from a '.dc' simulation shows both v_O versus v_{IN} (top trace) and $\partial v_O/\partial v_{IN}$ versus v_{IN} (bottom trace). From the plot of $\partial v_O/\partial v_{IN}$, we find the small-signal gains $v_o/v_{in} = 12.5$ V/V for $V_{IN} = 0$ V and $v_o/v_{in} = 7.46$ V/V for $V_{IN} = \pm 0.3$ V.



Problem 2.9

An amplifier with a right-half-plane zero at the frequency f_z and two left-half-plane poles at the frequencies f_{p1} and f_{p2} has the transfer function shown below where the gain A_0 at low frequencies is assumed to be positive.

$$H(jf) = \frac{A_0(1 - jf/f_z)}{(1 + jf/f_{p1})(1 + jf/f_{p2})}$$

Find an expression for the gain function $|H(jf)|$ and the phase function $\angle H(jf)$ and sketch a Bode plot using piecewise-linear approximations for the frequency range 10 kHz - 1 GHz, assuming that $f_z = 200$ MHz, $f_{p1} = 200$ kHz, $f_{p2} = 40$ MHz and $A_0 = 100$ V/V.
Calculate the gain and the phase at the frequencies $f = 0.4$ MHz, $f = 4$ MHz, $f = 40$ MHz and $f = 400$ MHz.

Solution:

With the transfer function shown in Problem 2.9, the gain function is

$$|H(jf)| = A_0 \frac{\sqrt{1 + (f/f_z)^2}}{\sqrt{(1 + (f/f_{p1})^2)(1 + (f/f_{p2})^2)}}$$

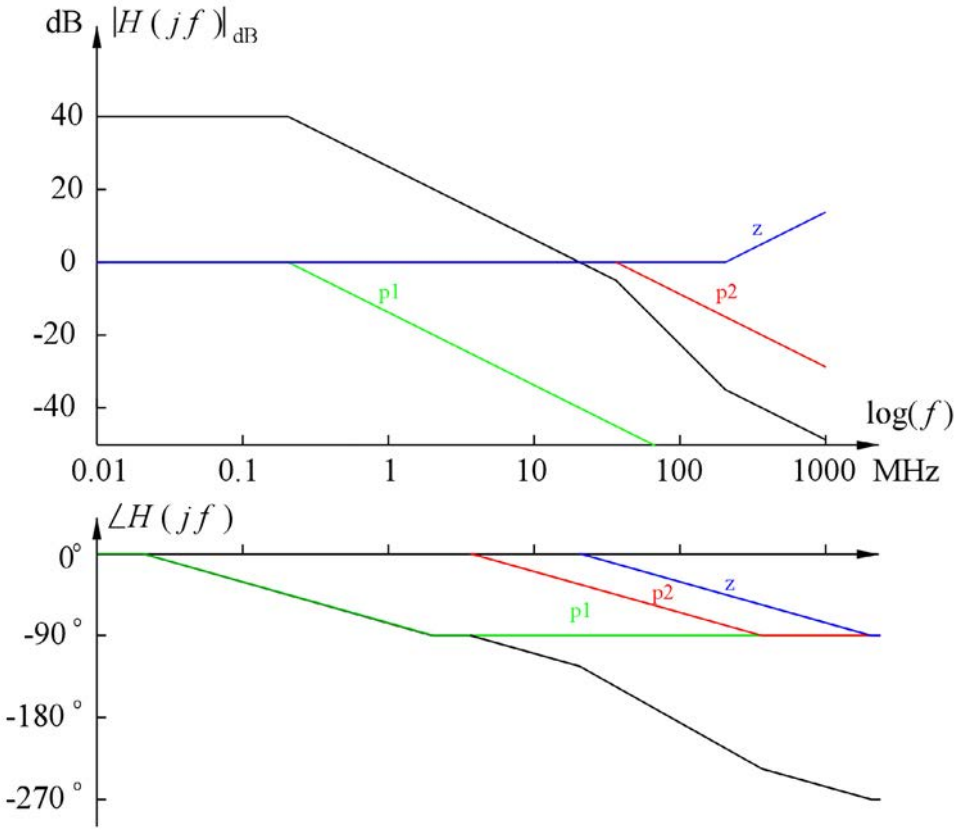
and the phase function is

$$\angle H(jf) = -\arctan(f/f_z) - \arctan(f/f_{p1}) - \arctan(f/f_{p2})$$

Notice that since the zero in the transfer function is a right-half-plane zero, the contribution to the phase from the zero is negative.

The following figure shows a Bode plot using piecewise linear approximations for both gain plot and phase plot. The low-frequency gain is $100 \sim 40$ dB and each of the two poles changes the slope of the gain by -20 dB/decade while the zero change the slope by $+20$ dB/decade as shown by the green, red and blue line segments respectively. The final gain plot, shown in black, is the sum of 40 dB and the green, red and blue plots.

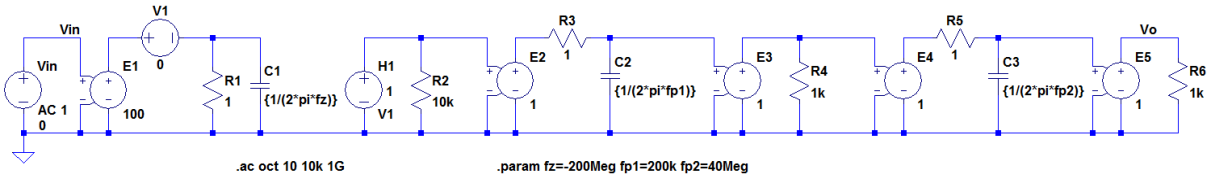
For the phase, the term $-\arctan(f/f_{p1})$ is shown in green, the term $-\arctan(f/f_{p2})$ is shown in red and the term $-\arctan(f/f_z)$ is shown in blue. The sum of these terms gives the phase $\angle H(jf)$, shown in black.



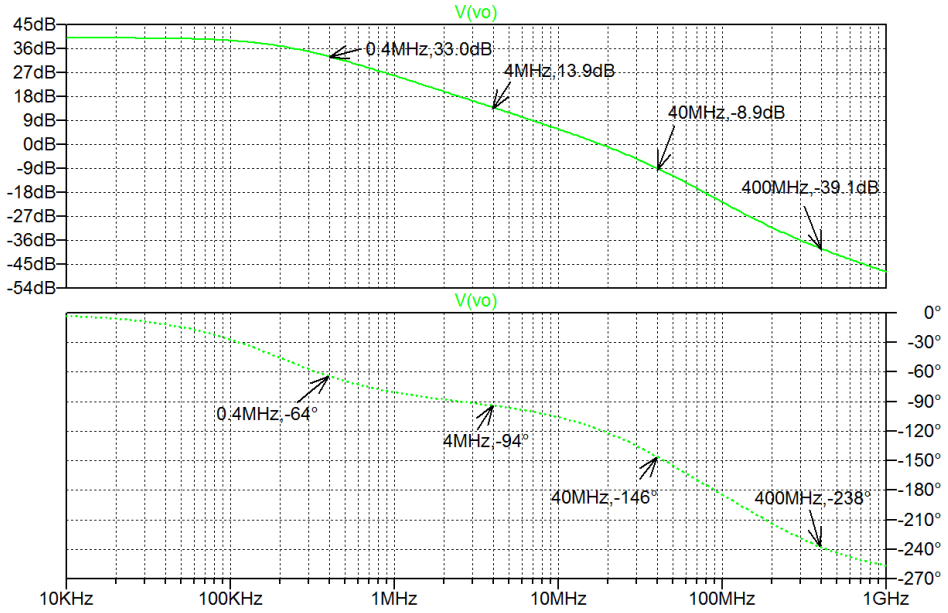
Gain and phase for the frequencies $f = 0.4$ MHz, $f = 4$ MHz, $f = 40$ MHz and $f = 400$ MHz are calculated using the expressions for $|H(jf)|$ and $\angle H(jf)$, resulting in the following values:

$f = 0.4$ MHz: $|H(jf)| = 44.7$ V/V $\sim$ 33.1 dB; $\angle H(jf) = -63.9°$
$f = 4$ MHz: $|H(jf)| = 5.0$ V/V $\sim$ 13.9 dB; $\angle H(jf) = -94.0°$
$f = 40$ MHz: $|H(jf)| = 0.36$ V/V ~ -8.9 dB; $\angle H(jf) = -146,0°$
$f = 400$ MHz: $|H(jf)| = 0.011$ V/V ~ -39.1 dB; $\angle H(jf) = -237.7°$

The results may be verified using LTspice. For the schematic, we use the filter blocks defined in Bruun (2020, Tutorial 5.3). Shown below is the LTspice schematic for simulating the transfer function. As the zero is in the right-half-plane, the parameter specifying the zero frequency is negative.



The Bode plot resulting from the simulation is shown in the following figure with gain and phase indicated for the frequencies $f = 0.4$ MHz, $f = 4$ MHz, $f = 40$ MHz and $f = 400$ MHz. The simulation results closely match the calculated results and the simulated Bode plot clearly resembles the piecewise linear approximation shown above.



References

Bruun, E. 2020, *CMOS Integrated Circuit Simulation with LTspice*, Third Edition, bookboon. Available from: http://bookboon.com/en/cmos-integrated-circuit-simulation-with-ltspice-ebook

Chapter 3 – The MOS Transistor

Multiple-choice test

1. Completed statements:

A-4:	The mobile electric carriers in the channel of an NMOS transistor are electrons.
B-9:	The drain and source regions of a PMOS transistor are p-doped regions.
C-7:	The channel in an NMOS transistor is formed when the gate-source voltage is larger than the threshold voltage.
D-11:	When the gate-source voltage for a PMOS transistor is positive, the transistor is in the cut-off region.
E-14:	For an NMOS transistor in the triode region, the drain current is $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2(v_{GS}-V_t)v_{DS}-v_{DS}^2\right)(1+\lambda v_{DS})$.
F-16:	The channel-length modulation in a MOS transistor causes the transistor to have a drain current depending on the drain-source voltage.
G-20:	The body effect in a MOS transistor occurs when source and bulk have different voltages.
H-6:	The small-signal parameter g_m for a MOS transistor describes a linearized relation between the drain current and the gate-source voltage.
I-1:	The small-signal parameter g_{ds} for a MOS transistor describes a linearized relation between the drain current and the drain-source voltage.
J-8:	The Shichman-Hodges model describes a nonlinear relation between the drain current, the gate-source voltage and the drain-source voltage.

2. For an NMOS transistor with $V_t = 0.4$ V, $\mu_n C_{ox} = 180$ µA/V^2, $W/L = 10$, $\lambda = 0$, $v_{GS} = 1.2$ V and $v_{DS} = 1.0$ V, the drain current is

   A: 0 mA
   B: 0.540 mA
   C: 0.576 mA

Solution:

As $v_{DS} > v_{GS} - V_t$, the transistor is in the active region and we find the drain current I_D using the Shichman-Hodges model $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = 0.576$ mA.

3. For a PMOS transistor in the active region with $V_t = -0.42$ V, $\mu_p C_{ox} = 45$ µA/V^2, $W/L = 10$, $\lambda = 0$, and $i_D = 324$ µA, the gate-source voltage is

   A: -1.62 V
   B: -1.20 V
   C: $+1.62$ V

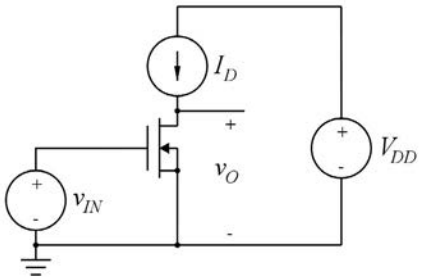
Solution:

For a PMOS transistor in the active region and with $\lambda = 0$, the Shichman-Hodges model gives

$$i_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(v_{GS} - V_t)^2 \Rightarrow |v_{GS} - V_t| = \sqrt{\frac{2i_D}{\mu_p C_{ox}(W/L)}} = 1.2 \text{ V}$$

Since $v_{GS} - V_t$ is negative for a PMOS transistor in the active region, we find $v_{GS} - V_t = -1.2$ V, resulting in $v_{GS} = -1.2 \text{ V} + V_t = -1.62$ V.

4. For the circuit shown below, assume that the transistor is in the active region. The transistor has a threshold voltage $V_t = 0.4$ V and a channel-length modulation parameter $\lambda = 0.2 \text{ V}^{-1}$. The bias current I_D is 200 μA and the bias values of v_{IN} and v_O are both 0.9 V.



The transconductance of the transistor is

A: 0.4 mA/V
B: 0.8 mA/V
C: 1.6 mA/V

Solution:

With $V_{IN} = V_O$, we have $V_{DS} > V_{GS} - V_t$ so the transistor is in the active region and using Eq. (3.69) in Bruun (2022), we find $g_m = 2I_D/(V_{GS} - V_t) = 0.8$ mA/V.

5. The small-signal output resistance of the transistor in the circuit above is

A: 15.0 kΩ
B: 29.5 kΩ
C: 59.0 kΩ

Solution:

Using Eq. (3.68) in Bruun (2022), we find $r_{ds} = (1 + \lambda V_{DS})/(\lambda I_D) = 29.5$ kΩ.

6. The small-signal voltage gain in the circuit above is

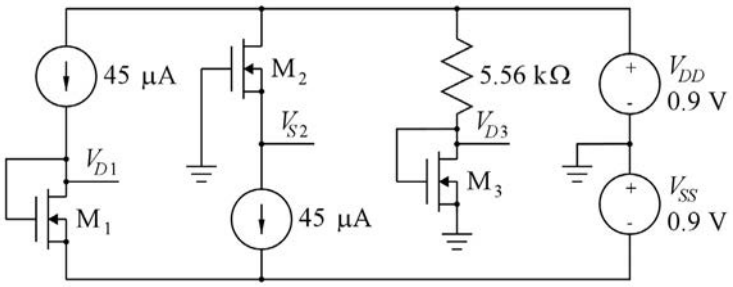
   A: -23.6 V/V
   B: $+23.6$ V/V
   C: -12.0 V/V

Solution:

We find the voltage voltage gain as $A_v = -g_m r_{out}$ and since the transistor is biased by an ideal dc current source, $r_{out} = r_{ds}$, so $A_v = -0.8$ mA/V $\times$ 29.5 kΩ $= -23.6$ V/V.

Problems

Problem 3.1



For the transistors in the circuit shown above, assume $W/L = 8$, $\mu_n C_{ox} = 180\ \mu\text{A/V}^2$, $V_t = 0.4$ V and $\lambda = 0$.
Calculate the voltages V_{D1}, V_{S2} and V_{D3}.

Solution:

We notice that M_1 has drain and source connected, so it is in the active region. Using the Shichman-Hodges transistor model, we find

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_t)^2 \;\Rightarrow\; V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W_1/L_1)}} = 650\ \text{mV}$$

Using Kirchhoff's voltage law, we find $V_{D1} = -V_{SS} + V_{DS1} = -V_{SS} + V_{GS1} = -250$ mV.

Transistor M_2 has $V_{D2} = V_{DD} = 900\ \text{mV} > V_{G2} = 0$ V, so it is in the active region. As the current in M_2 is equal to the current in M_1 and the transistors have the same size, no channel-length modulation, and they both have source and bulk connected, i.e., no bulk effect, the gate-source voltage for M_2 is equal to the gate-source voltage for M_1, i.e., $V_{GS2} = V_{GS1}$.

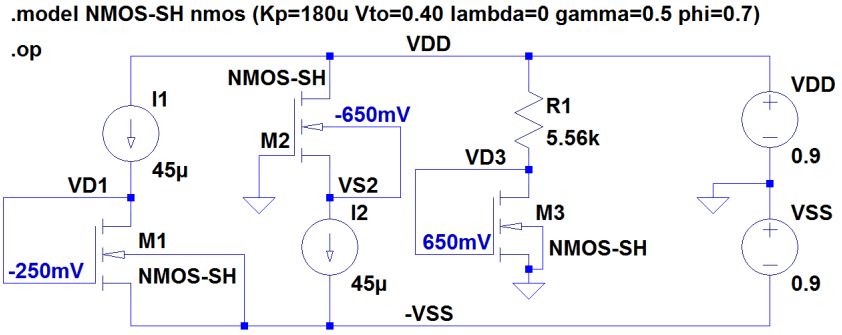
Using Kirchhoff's voltage law, we find $V_{S2} = V_{G2} - V_{GS2} = V_{G2} - V_{GS1} = 0\ \text{V} - 650\ \text{mV} = -650$ mV.

Transistor M_3 is also in the active region as gate and drain are connected. Using Kirchhoff's current law at the drain node, we find

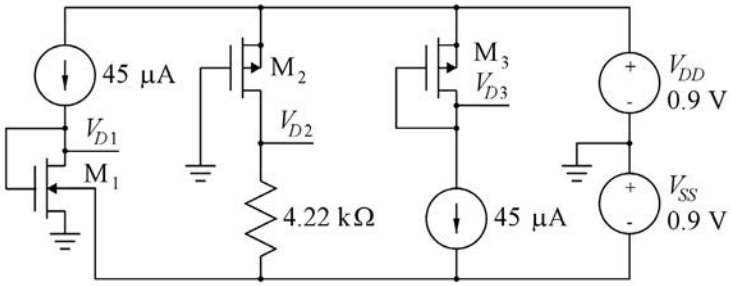
$$(V_{DD} - V_{D3})/5.56\ \text{k}\Omega = I_{D3} = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L_3}(V_{GS3} - V_t)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L_3}(V_{D3} - V_t)^2$$

This is a quadratic equation from which V_{D3} can be found. The two solutions are $V_{D3} = 650$ mV and $V_{D3} = -100$ mV. As we know that $V_{D3} > V_t = 400$ mV, we select the solution $V_{D3} = 650$ mV.

The solutions are easily verified using LTspice. The LTspice schematic corresponding to Problem 3.1 is shown in the following figure, and running a '.op' simulation, the simulation results confirming the analytically derived results for V_{D1}, V_{D2} and V_{D3} are given in the output file. The results can also be shown directly in the schematic by pointing to a node and using a right-click to open the command 'Place .op Data Label'.



Problem 3.2



For the NMOS transistor in the circuit shown above, assume $W/L = 8$, $\mu_n C_{ox} = 180\ \mu A/V^2$, $V_{to} = 0.4$ V, $\lambda = 0$, $\gamma = 0.5\sqrt{V}$ and $|2\Phi_F| = 0.7$ V.

For the PMOS transistors in the circuit, $W/L = 32$, $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda = 0$. Calculate the voltages V_{D1}, V_{D2} and V_{D3}.

Solution:

We notice that M_1 has drain and source connected, so it is in the active region. Using the Shichman-Hodges transistor model, we find

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_t)^2 \quad \Rightarrow \quad V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W_1/L_1)}}$$

Since source and bulk are not connected for M_1, we calculate the threshold voltage using Eq. (3.17) in Bruun (2022) with $V_{SB} = V_{SS} = 900$ mV, i.e., $V_t = V_{to} + \gamma(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_f|}) = 614$ mV.

Inserting this value for V_t in the expression for V_{GS1} results in $V_{D1} = V_{GS1} = 864$ mV.

For the PMOS transistor M_2, we have $V_{G2} = 0$ and $V_{S2} = V_{DD} = 900$ mV, so $|V_{GS}| = 900$ mV. Assuming that M_2 is in the active region, we find using the Shichman-Hodges transistor model

$$I_{D2} = \frac{1}{2}\mu_p C_{ox}\frac{W_2}{L_2}(|V_{GS2}| - |V_t|)^2 = 165.9\ \mu\text{A}$$

Using Kirchhoff's voltage law and Ohm's law, we then find $V_{D2} = -V_{SS} + I_{D2} \times 4.22\ \text{k}\Omega = -200$ mV.

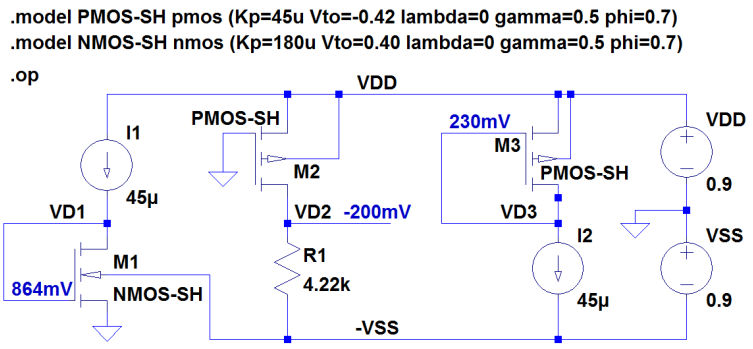
We notice that $|V_{DS2}| = 1.1$ V is larger than $|V_{GS2}| - |V_t| = 0.48$ V, so M_2 is in the active region as assumed.

For M_3, drain and gate are connected, so it is in the active region. Using the Shichman-Hodges model, we find

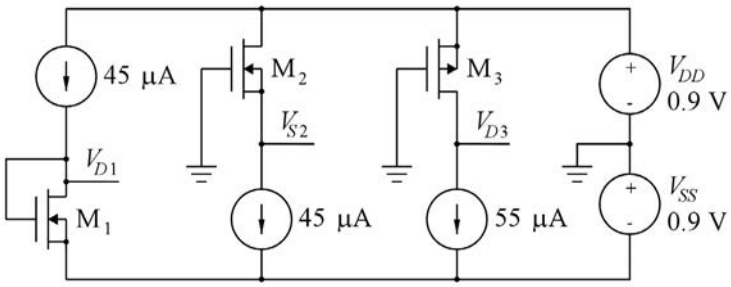
$$I_{D3} = \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(|V_{GS3}| - |V_t|)^2 \quad \Rightarrow \quad |V_{GS3}| = |V_t| + \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W_3/L_3)}} = 670\ \text{mV}$$

Using Kirchhoff's voltage law, we find $V_{D3} = V_{DD} - |V_{GS3}| = 230$ mV.

The solutions are easily verified using LTspice. The LTspice schematic corresponding to Problem 3.2 is shown below and running a '.op' simulation, the simulation results confirming the analytically derived results for V_{D1}, V_{D2} and V_{D3} are given in the output file and shown in the schematic below.



Problem 3.3



For the NMOS transistors shown in the circuit above, assume $W = 16$ µm, $L = 2$ µm, $\mu_n C_{ox} = 180$ µA/V^2, $V_t = 0.4$ V and $\lambda L = 0.1$ µm/V.
For the PMOS transistor, assume $W = 30$ µm, $L = 3$ µm, $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda L = 0.14$ µm/V.
Calculate or simulate the voltages V_{D1}, V_{S2} and V_{D3}.

Solution:

We notice that M_1 has drain and source connected, so it is in the active region. Using the Shichman-Hodges transistor model, we find

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_t)^2(1 + \lambda V_{DS1}) = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{DS1} - V_t)^2(1 + \lambda V_{DS1})$$

This is a cubic equation for finding V_{DS1}. It may be solved using a math program. However, we may also notice that the bias conditions for M_1 are the same as for M_1 in Problem 3.1. Also, W_1/L_1 is the same, so assuming that the channel-length modulation only gives a slight change in the result, we may use the result from Problem 3.1 to find an approximate value for $(1 + \lambda V_{DS1})$. Using $L_1 = 2$ µm and $\lambda L = 0.1$ µm/V, we find $\lambda = 0.05$ V^{-1}, and from Problem 3.1, we have $V_{DS1} \simeq 650$ mV, so $(1 + \lambda V_{DS1}) \simeq 1.0325$. Inserting this value in the Shichman-Hodges model, we find

$$45\ \mu\text{A} = \frac{1}{2} \times 180\ \mu\text{A/V}^2 \times \frac{16\ \mu\text{m}}{2\ \mu\text{m}} \times (V_{DS1} - 0.4\ \text{V})^2 \times 1.0325 \quad \Rightarrow V_{DS1} = 646\ \text{mV}$$

Using Kirchhoff's voltage law, we find $V_{D1} = -V_{SS} + V_{DS1} = -254$ mV.

Transistor M_2 has $V_{D2} = V_{DD} = 900$ mV $> V_{G2} = 0$ V, so it is in the active region. Using the Shichman-Hodges transistor model, we find

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS2} - V_t)^2(1 + \lambda V_{DS2}) = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(-V_{S2} - V_t)^2(1 + \lambda (V_{DD} - V_{S2}))$$

This is a cubic equation for finding V_{S2}. It may be solved using a math program. However, we may also notice that I_{D2} is the same as I_{D1} and the transistors have identical dimensions, so neglecting the channel-length modulation, we find $V_{S2} = V_{G2} - V_{GS2} \simeq -650$ mV. Using this value to find an approximate value for $(1 + \lambda V_{DS2})$, we find $(1 + \lambda V_{DS2}) \simeq (1 + 0.05\ \text{V}^{-1} \times (0.9\ \text{V} + 0.65\ \text{V})) = 1.0775$. Inserting this value in the Shichman-Hodges model, we find

$$45\ \mu\text{A} = \frac{1}{2} \times 180\ \mu\text{A/V}^2 \times \frac{16\ \mu\text{m}}{2\ \mu\text{m}} \times (-V_{S2} - 0.4\ \text{V})^2 \times 1.0775 \quad \Rightarrow V_{S2} = -641\ \text{mV}$$

For transistor M_3, the gate-source voltage is $|V_{GS3}| = V_{DD} = 900$ mV. Assuming that the transistor is in the active region, the Shichman-Hodges model gives

$$I_{D3} = \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(|V_{GS3}| - |V_t|)^2(1 + \lambda|V_{DS3}|)$$

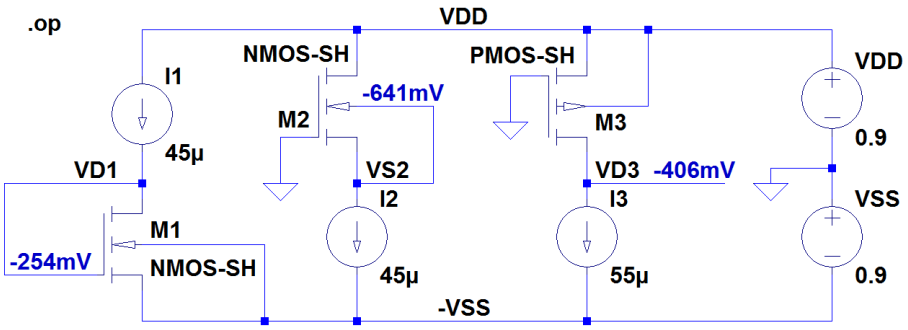
Inserting numerical values, we find

$$55\ \mu\text{A} = \frac{1}{2} \times 45\ \mu\text{A/V}^2 \times \frac{30\ \mu\text{m}}{3\ \mu\text{m}} \times (0.9\ \text{V} - 0.42\ \text{V})^2 \times (1 + \frac{0.14\ \mu\text{m/V}}{3\ \mu\text{m}} \times |V_{DS3}|) \ \Rightarrow\ |V_{DS3}| = 1.306\ \text{V}$$

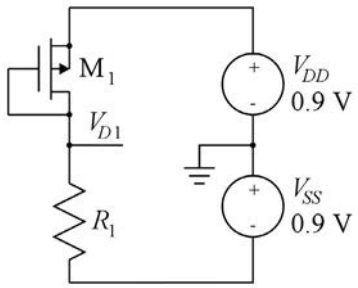
We notice that $|V_{DS3}| > |V_{GS3}| - |V_t|$, so the assumption that M_3 is in the active region is correct.
Using Kirchhoff's voltage law, we find $V_{D3} = V_{DD} - |V_{DS3}| = -0.406$ V.

The solutions are easily verified using LTspice. The LTspice schematic corresponding to Problem 3.3 is shown below and running a '.op' simulation, the simulation results confirming the analytically derived results for V_{D1}, V_{D2} and V_{D3} are given in the output file and shown in the schematic below.

```
.model PMOS-SH pmos (Kp=45u Vto=-0.42 lambda={0.14/3} gamma=0.5 phi=0.7)
.model NMOS-SH nmos (Kp=180u Vto=0.40 lambda={0.1/2} gamma=0.5 phi=0.7)
```



Problem 3.4



For the circuit shown above, find the resistor R_1 and the transistor width W_1 so that $V_{D1} = 0.2$ V and $I_{D1} = 10$ µA. Assume $L_1 = 3$ µm, $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda = 0$.
Repeat for $\lambda L = 0.14$ µm/V.

Solution:

The voltage across R_1 is $V_{R1} = V_{D1} + V_{SS} = 1.1$ V, so by using Ohm's law, we find $R_1 = V_{R1}/I_{D1} = 110$ kΩ.

For M_1, we have $|V_{GS1}| = |V_{D1} - V_{DD}| = 0.7$ V.

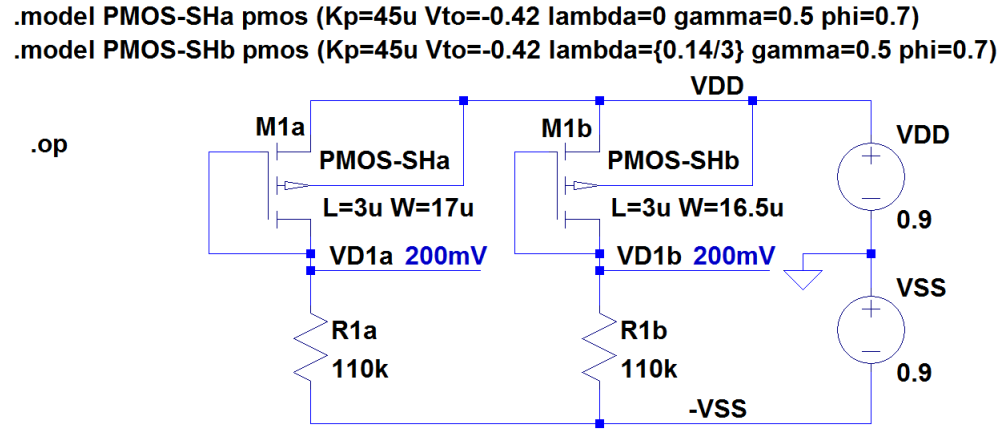
For $\lambda = 0$, the Shichman-Hodges transistor model gives

$$I_{D1} = \frac{1}{2}\mu_p C_{ox}\frac{W_1}{L_1}(|V_{GS1}| - |V_t|)^2 \ \Rightarrow\ W_1 = L_1\frac{2I_{D1}}{\mu_p C_{ox}(|V_{GS1}| - |V_t|)^2} = 17\ \mu\text{m}$$

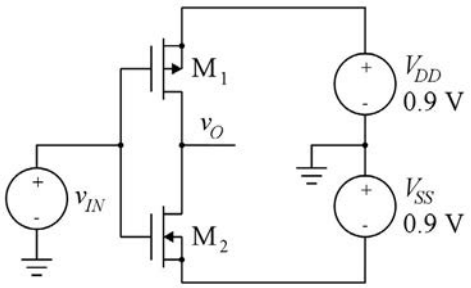
For $\lambda L = 0.14$ µm/V $\Rightarrow \lambda = 0.0467$ V^{-1}, the Shichman-Hodges transistor model gives with $|V_{DS1}| = V_{DD} - V_{D1} = 0.7$ V

$$I_{D1} = \frac{1}{2}\mu_p C_{ox}\frac{W_1}{L_1}(|V_{GS1}| - |V_t|)^2(1+\lambda|V_{DS1}|) \Rightarrow W_1 = L_1\frac{2I_{D1}}{\mu_p C_{ox}(|V_{GS1}| - |V_t|)^2(1+\lambda|V_{DS1}|)} = 16.5\ \mu\text{m}$$

The results may be verified by a '.op' simulation using the LTspice schematic shown below. Notice the different transistor models for '`M1a`' and '`M1b`'.



Problem 3.5



For the circuit shown above, design the width of transistor M_1 so that the output voltage v_O is 0 for an input voltage $v_{IN} = 0$. Assume $L_1 = L_2 = 0.5$ µm and $W_2 = 0.5$ µm.
For the PMOS transistor, assume $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda L = 0.14$ µm/V.
For the NMOS transistor, assume $\mu_n C_{ox} = 180$ µA/V^2, $V_t = 0.4$ V and $\lambda L = 0.1$ µm/V.
Simulate and plot the output voltage v_O versus the input voltage for -0.9 V $\leq v_{IN} \leq 0.9$ V.
Find the output voltage for $v_{IN} = -0.2$ V and for $v_{IN} = 0.2$ V.

Solution:

For $v_{IN} = v_O = 0$, we have $|v_{GS1}| = |v_{DS1}| = V_{DD} = 0.9$ V and $v_{GS2} = v_{DS2} = V_{SS} = 0.9$ V. Thus, both transistors are in the active region and the Shichman-Hodges model gives

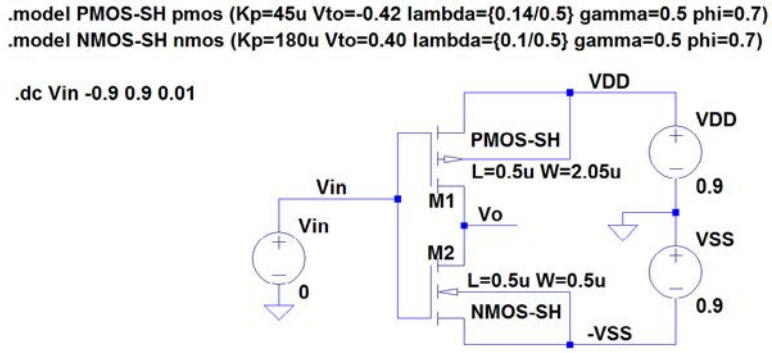
$$i_{D1} = \frac{1}{2}\mu_p C_{ox}\frac{W_1}{L_1}(|v_{GS1}| - |V_{t1}|)^2(1+\lambda_1|v_{DS1}|) = i_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(v_{GS2} - V_{t2})^2(1+\lambda_2 v_{DS2})$$

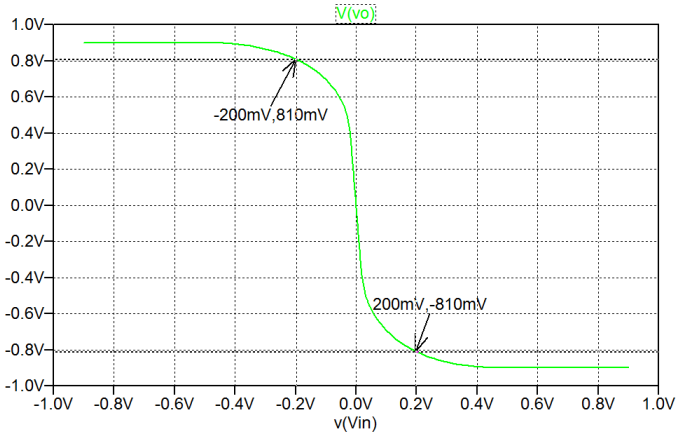
Inserting numerical values, we find

$$\frac{1}{2}\times 45\ \mu\text{A/V}^2 \times \frac{W_1}{0.5\ \mu\text{m}} \times (0.9\ \text{V} - 0.42\ \text{V})^2 \times (1 + \frac{0.14}{0.5}\ \text{V}^{-1} \times 0.9\ \text{V}) =$$

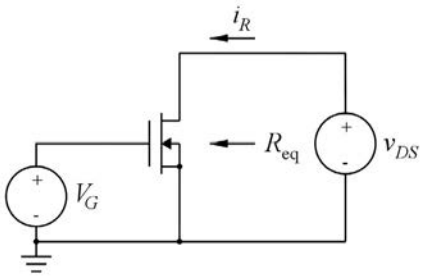
$$\frac{1}{2}\times 180\ \mu\text{A/V}^2 \times \frac{0.5\ \mu\text{m}}{0.5\ \mu\text{m}} \times (0.9\ \text{V} - 0.4\ \text{V})^2 \times (1 + \frac{0.1}{0.5}\ \text{V}^{-1} \times 0.9\ \text{V}) \Rightarrow W_1 = 2.05\ \mu\text{m}$$

The following figure shows an LTspice schematic of the circuit and the result of a '.dc' simulation. The plot shows that $v_O = 810$ mV for $v_{IN} = -200$ mV and $v_O = -810$ mV for $v_{IN} = 200$ mV.





Problem 3.6



An NMOS transistor biased in the triode region can be operated as a voltage-controlled linear resistor R_{eq} for very small values of v_{DS} as shown above. The voltage V_G controls the value of the resistance between drain and source.

Assume the following transistor parameters: $W = 2$ µm, $L = 20$ µm, $\mu_n C_{ox} = 180$ µA/V^2, $V_t = 0.4$ V and $\lambda = 0$. What is the range of resistance values which can be obtained for $0.9\text{ V} \leq V_G \leq 1.8\text{ V}$?

For $V_G = 1.2$ V, what is the maximum value of v_{DS} which can be applied if the error in calculating i_R from v_{DS}/R_{eq} should be less than 5% ?

Solution:

For finding the resistance R_{eq} with the transistor in the triode region, we use Eq. (3.62) in Bruun (2022):

$$R_{eq} = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_t)} = \frac{1}{\mu_n C_{ox}(W/L)(V_G - V_t)}$$

The maximum value of R_{eq} is found for the minimum value of V_G, i.e., $V_G = 0.9$ V. Inserting numerical values, we find $R_{\text{eq, max}} = 111.1\ \text{k}\Omega$.

The minimum value of R_{eq} is found for the maximum value of V_G, i.e., $V_G = 1.8$ V. Inserting numerical values, we find $R_{\text{eq, min}} = 39.7\ \text{k}\Omega$.

The current i_R calculated using Ohm's law is $i_{R,\text{Ohm}} = \mu_n C_{ox}(W/L)(V_G - V_t)v_{DS}$.

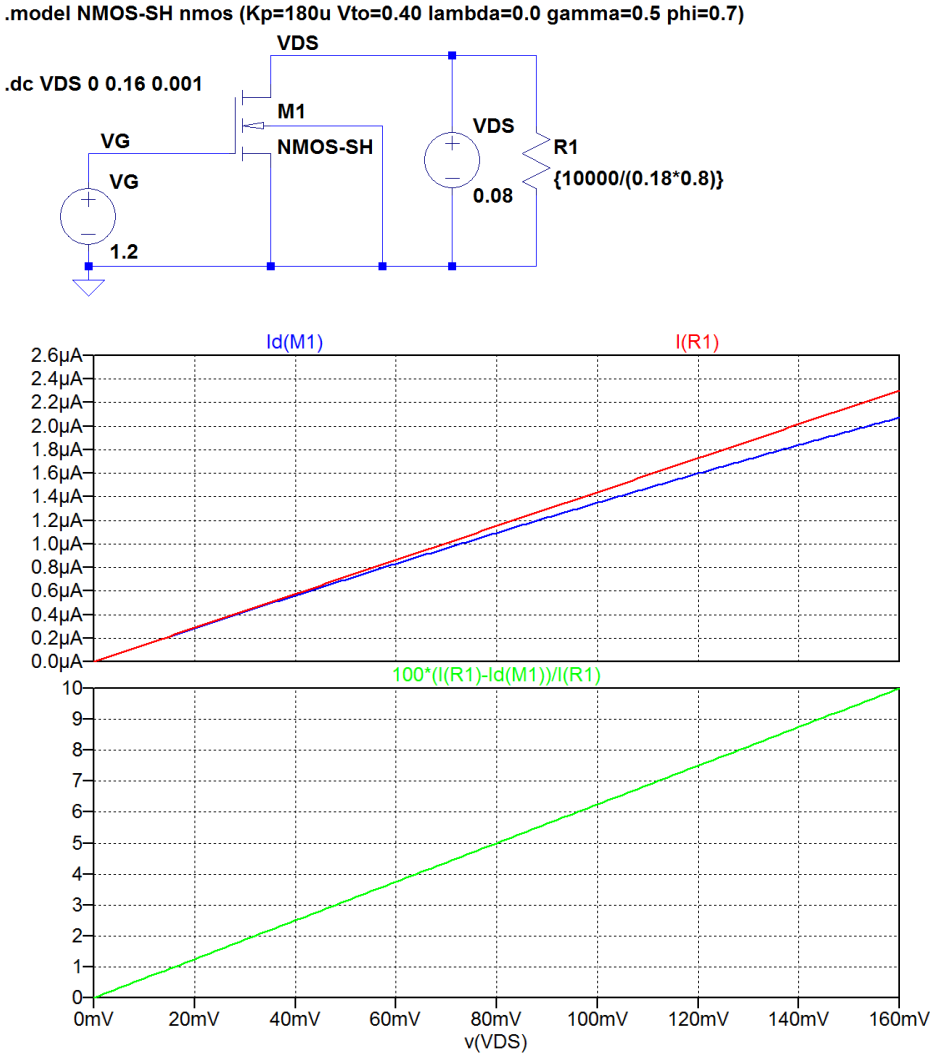
The current i_R calculated using the Shichman-Hodges model is
$i_{R,\text{SH}} = \mu_n C_{ox}(W/L)[(V_G - V_t)v_{DS} - v_{DS}^2/2]$.

The relative error in $i_{R,\text{Ohm}}$ is

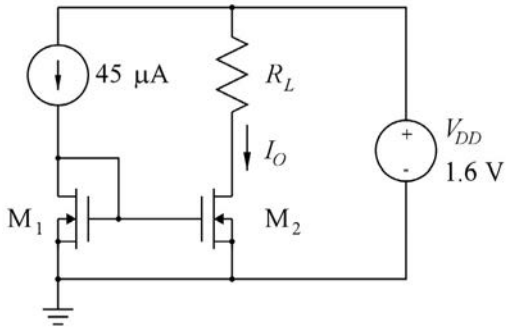
$$\varepsilon = \frac{i_{R,\text{Ohm}} - i_{R,\text{SH}}}{i_{R,\text{SH}}}\,100\% \simeq \frac{i_{R,\text{Ohm}} - i_{R,\text{SH}}}{i_{R,\text{Ohm}}}\,100\% = \frac{\mu_n C_{ox}(W/L)v_{DS}^2/2}{\mu_n C_{ox}(W/L)(V_G - V_t)v_{DS}}\,100\% = \frac{v_{DS}}{2(V_G - V_t)}\,100\%$$

For $\varepsilon \leq 5\%$ and $V_G = 1.2$ V, we find $v_{DS} \leq (\varepsilon/100)\,2(V_G - V_t) = 80$ mV.

The circuit may also be simulated using LTspice. Shown below is an LTspice schematic also including a resistor '`R1`' to model the ideal resistor R_{Ohm} for $V_G = 1.2$ V. A '.dc' simulation is run with $V_G = 1.2$ V and v_{DS} swept from 0 to 160 mV. The plot from the simulation shows $i_{R,\text{Ohm}}$, $i_{R,\text{SH}}$ and ε calculated as $100\% \times (i_{R,\text{Ohm}} - i_{R,\text{SH}})/i_{R\text{Ohm}}$. We see that $\varepsilon = 5\%$ is reached for $v_{DS} = 80$ mV.



Problem 3.7



Design the current mirror shown above to provide an output current of $I_O = 90$ μA for $0 \leq R_L \leq 15$ kΩ. Assume the following transistor parameters: $L_1 = L_2 = 1$ μm, $\mu_n C_{ox} = 180$ μA/V^2, $V_t = 0.4$ V and $\lambda = 0$. Use a supply voltage $V_{DD} = 1.6$ V and use minimum values of W_1 and W_2 for which the current mirror fulfills the specifications.
Now, assume that $\lambda = 0.1$ V^{-1} for both transistors. Draw a small-signal equivalent circuit for the circuit and find the small-signal output resistance of the current mirror, assuming a bias value of 0.65 V at the output of the current mirror.

Solution:

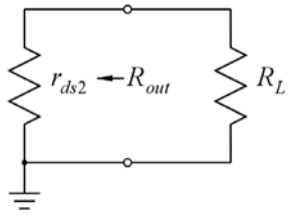
Transistor M_2 should be designed to be in the active region, even for the largest value of R_L, causing the smallest value of V_{DS2}. With $R_L = 15$ kΩ and $I_O = 90$ μA, we find $V_{DS2} = V_{DD} - R_D I_O = 250$ mV.

Thus, in order to ensure M_2 in the active region,

$$\begin{aligned} V_{GS2} - V_t &\leq 250 \text{ mV} \\ \sqrt{\frac{2I_o}{\mu_n C_{ox}(W_2/L_2)}} &\leq 250 \text{ mV} \\ W_2 &\geq L_2 \frac{2I_o}{\mu_n C_{ox}(250 \text{ mV})^2} = 16 \text{ μm} \end{aligned}$$

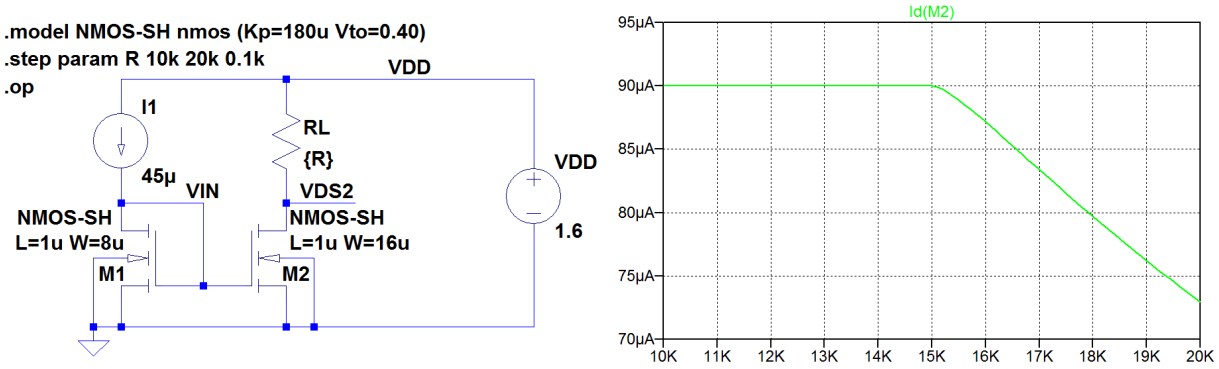
The minimum value for W_2 is $W_2 = 16$ μm and as $L_1 = L_2 = 1$ μm and $I_{D1} = I_{D2}/2$, we find $W_1 = W_2/2 = 8$ μm.

With $\lambda = 0.1$ V^{-1}, the small-signal equivalent circuit corresponding to Problem 3.7 is shown below, compare to Fig. 3.43 in Bruun (2022).

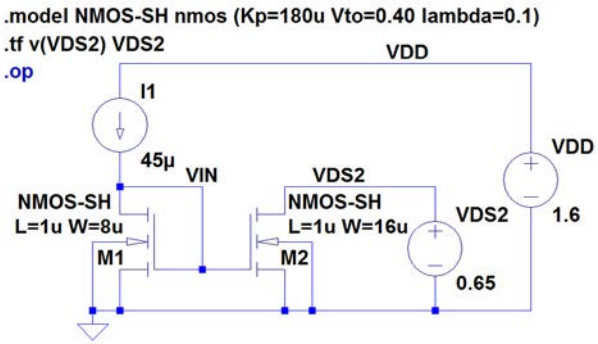


The output resistance of the current mirror is $R_{out} = r_{ds2} = \dfrac{1 + \lambda V_{DS2}}{\lambda I_O}$. With $V_{DS2} = 0.65$ V, we find $R_{out} = 118$ kΩ.

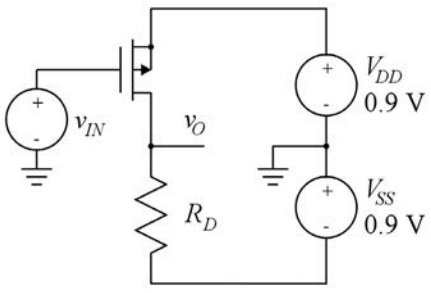
The circuit may also be analyzed using LTspice. Shown below is an LTspice schematic corresponding to Problem 3.7 with the transistors specified to have the dimensions calculated above and $\lambda = 0$. The load resistor R_L is specified as a parameter which is stepped from 10 kΩ to 15 kΩ. Running a '.op' simulation, we may plot $I_O = I_{D2}$ versus the load resistor as shown below. From the plot, we verify that $I_O = 90$ µA for $R_L \leq 15$ kΩ.



Also the output resistance may be verified by an LTspice simulation. The figure below shows the LTspice schematic with the transistors specified to have $\lambda = 0.1$ V^{-1}. Running a '.op' simulation, we find $g_{ds2} = 8.46$ µA/V, corresponding to $r_{ds2} = 1/g_{ds2} = 118$ kΩ. Alternatively, a '.tf' simulation with '`VDS2`' as the source and '`v(VDS2)`' as the output directly gives the output resistance as 118248 Ω ≃ 118 kΩ.



Problem 3.8

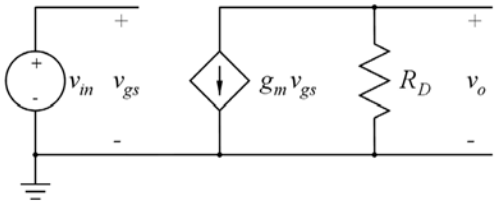


Shown above is an inverting amplifier implemented by a PMOS transistor and a drain resistor R_D. Assume the following transistor parameters: $L = 1$ µm, $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda = 0$. The output voltage has a bias value of 0, and the input voltage v_{IN} is the sum of a bias voltage V_{IN} and a small-signal voltage v_{in}.

Draw a small-signal equivalent circuit for the amplifier and derive an expression for the small-signal voltage gain v_o/v_{in}. Calculate the input bias voltage so that a small-signal gain of -6 V/V is obtained. Calculate R_D and W so that a bias current of 80 μA is obtained. Use LTspice to simulate and plot the output voltage for a sinusoidal input with an amplitude of 30 mV and a frequency of 1 kHz. Repeat the simulation with an input amplitude of 300 mV.

Solution:

The small-signal diagram for an inverting amplifier with a PMOS transistor is the same as the small-signal diagram for an inverting amplifier with an NMOS transistor. The following figure shows the small-signal diagram. Since $\lambda = 0$, the output resistance r_{ds} of the transistor is infinite, so it is omitted in the small-signal diagram.



The small-signal gain is $v_o/v_{in} = -R_D g_m$ where g_m may be found from

$$g_m = \frac{2I_D}{|V_{GS} - V_t|} = \frac{2I_D}{|V_{IN} - V_{DD} - V_t|}$$

and R_D is found from $R_D = \dfrac{V_O + V_{SS}}{I_D} = \dfrac{V_{SS}}{I_D}$ where we have used $V_O = 0$.

Combining the expressions for g_m and R_D, we find

$$\frac{v_o}{v_{in}} = -\frac{2V_{SS}}{|V_{IN} - V_{DD} - V_t|}$$

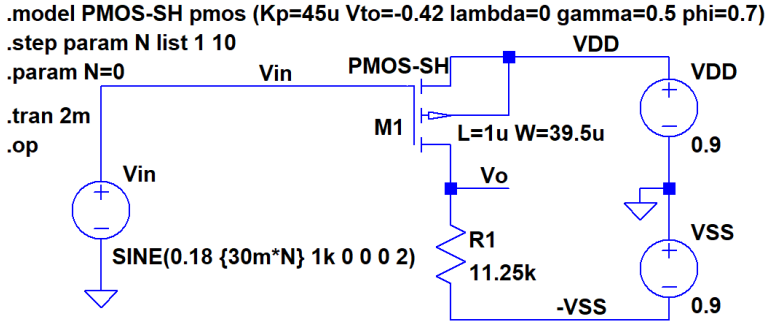
For a small-signal gain of -6 V/V, we find $|V_{IN} - V_{DD} - V_t| \times 6 = 2V_{SS} \Rightarrow -V_{IN} + 0.48 \text{ V} = 0.3 \text{ V} \Rightarrow V_{IN} = 0.18$ V.

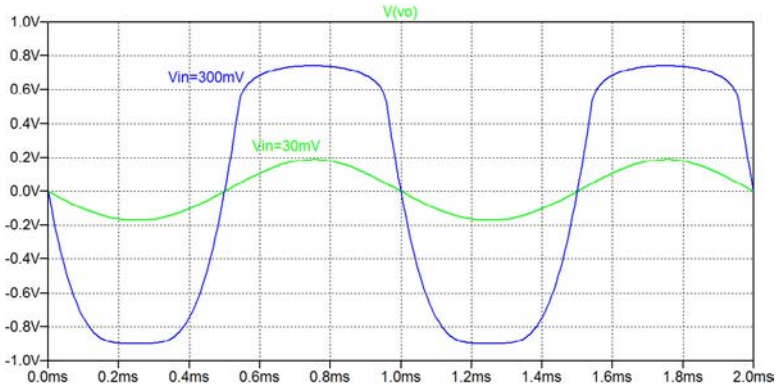
For a bias current $I_D = 80$ μA, we find $R_D = V_{SS}/I_D = 11.25$ kΩ, and using the Shichman-Hodges model, we find

$$W = L\frac{2I_D}{\mu_p C_{ox}(|V_{GS}| - |V_t|)^2} = 1 \text{ μm} \times \frac{2 \times 80 \text{ μA}}{45 \text{ μA/V}^2 \times (0.72 \text{ V} - 0.42 \text{ V})^2} = 39.5 \text{ μm}$$

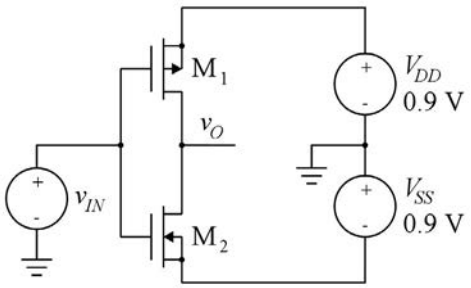
The following figure shows an LTspice schematic corresponding to Problem 3.8. The specification for V_{IN} is a sinusoid with a frequency of 1 kHz, a dc value of 0.18 V, an amplitude of 30 mV when the step parameter N is equal to 1 and an amplitude of 300 mV when the step parameter N is equal to 10. Running a '.op' simulation with the '.tran' directive and the '.step' directive changed to comments will verify the bias conditions of $V_O = 0$ and $I_D = 80$ μA for $V_{IN} = 0.18$ V.

Running the '.tran' simulation results in the following plot. Apparently, the transistor does not remain in the active region for $V_{in} = 300$ mV.





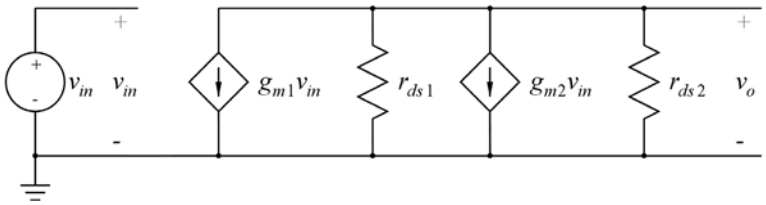
Problem 3.9



Shown above is an inverting amplifier implemented by a PMOS transistor and an NMOS transistor. Assume the following transistor geometries: $L_1 = L_2 = 0.5$ µm, $W_1 = 4$ µm and $W_2 = 1$ µm.
For the PMOS transistor, assume $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda L = 0.14$ µm/V.
For the NMOS transistor, assume $\mu_n C_{ox} = 180$ µA/V^2, $V_t = 0.4$ V and $\lambda L = 0.1$ µm/V.
Draw a small-signal equivalent circuit for the amplifier and calculate the values of the small-signal parameters for an input bias voltage of $V_{IN} = 0$. Use LTspice to verify that both transistors are in the active region for $V_{IN} = 0$ and to check the values of the small-signal parameters.
Calculate the small-signal gain of the amplifier and verify the calculation with LTspice.

Solution:

The small-signal model for a PMOS transistor is the same as for an NMOS transistor. In the small-signal diagram, M_1 and M_2 are connected in parallel. The small-signal diagram is shown below.



An approximate value for the drain current can be found from the Shichman-Hodges model, assuming $1+\lambda|V_{DS}| \simeq 1$. With $V_{GS2} = V_{SS}$, we find

$$I_D \simeq \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS2}-V_{tn})^2 = 45\ \mu\text{A}$$

Using this value for I_D, we find $g_{m2} = 2I_D/(V_{GS2}-V_{tn}) = 0.18$ mA/V and $g_{m1} = 2I_D/|V_{GS1}-V_{tn}| = 0.1875$ mA/V.

For finding the small-signal output resistances r_{ds1} and r_{ds2}, we use the approximate relation $r_{ds} \simeq (\lambda I_D)^{-1}$. For M_1, we find $\lambda_1 = 0.14\ \mu\text{m/V}/0.5\ \mu\text{m} = 0.28\ \text{V}^{-1}$, giving $r_{ds1} \simeq 79\ \text{k}\Omega$. For M_2, we find $\lambda_2 = 0.1\ \mu\text{m/V}/0.5\ \mu\text{m} = 0.2\ \text{V}^{-1}$, giving $r_{ds2} \simeq 111\ \text{k}\Omega$.

More accurate values can be found by using a node equation at the output node. Assuming M_1 and M_2 in the active region, we find

$$\begin{aligned} \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS2}-V_{tn})^2(1+\lambda_2 V_{DS2}) &= \frac{1}{2}\mu_p C_{ox}\frac{W_1}{L_1}(|V_{GS1}|-|V_{tp}|)^2(1+\lambda_1|V_{DS1}|) \\ \Rightarrow \mu_n\frac{W_2}{L_2}(V_{SS}-V_{tn})^2(1+\lambda_2(V_O+V_{SS})) &= \mu_p\frac{W_1}{L_1}(V_{DD}-|V_{tp}|)^2(1+\lambda_1(V_{DD}-V_O)) \end{aligned}$$

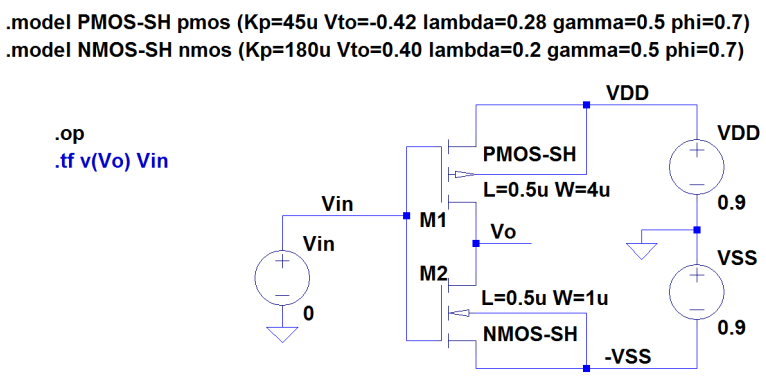
Inserting numerical values and solving for V_O, we find $V_O = -57$ mV. Thus, both transistors have $|V_{DS}| > |V_{GS}| - |V_t|$ so they are both in the active region. We find

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{SS}-V_{tn})^2(1+\lambda_2(V_O+V_{SS})) = 52.6\ \mu\text{A}$$

giving $g_{m1} = 2I_D/(V_{DD}-|V_{tp}|) = 0.219$ mA/V and $g_{m2} = 2I_D/(V_{SS}-V_{tn}) = 0.210$ mA/V.

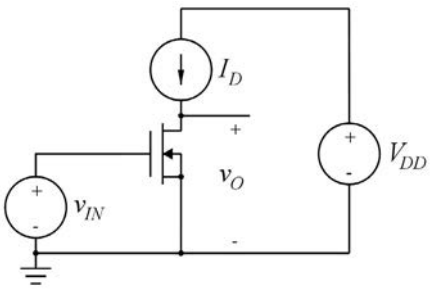
For the output resistances, we find $r_{ds1} = (1+\lambda_1(V_{DD}-V_O))/(\lambda_1 I_D) = 86\ \text{k}\Omega$
and $r_{ds2} = (1+\lambda_2(V_O+V_{SS}))/(\lambda_2 I_D) = 111\ \text{k}\Omega$.

For checking the results, we run a '.op' simulation using the LTspice schematic shown below. From the output file, we find $V_O = -57.1$ mV, corresponding to the result found above. From the error log file, we find $g_{m1} = 0.219$ mA/V and $g_{m2} = 0.210$ mA/V. The error log file gives $g_{ds1} = 11.6\ \mu$A/V, corresponding to $r_{ds1} = 86.2\ \text{k}\Omega$, and $g_{ds2} = 9.00\ \mu$A/V, corresponding to $r_{ds2} = 111.1\ \text{k}\Omega$. Thus, also the values of the small-signal parameters are confirmed.



From the small-signal diagram, we find the small-signal gain $v_o/v_{in} = -(g_{m1}+g_{m2})(r_{ds1} \parallel r_{ds2}) = -20.8$ V/V. The small-signal gain may be verified by a '.tf' simulation with '`v(Vo)`' as the output and '`Vin`' as the input. From the output file, we find a small-signal gain of -20.83 V/V, confirming the analytically derived result.

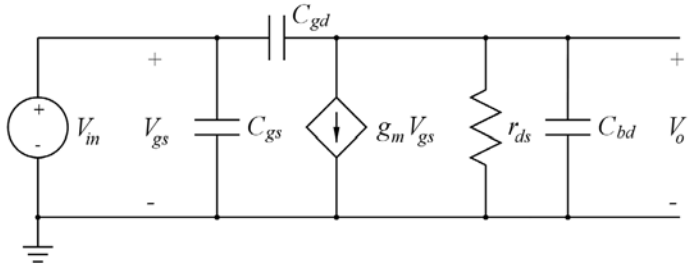
Problem 3.10



Draw a small-signal equivalent circuit for the inverting amplifier shown above, including the transistor capacitances C_{gs}, C_{gd} and C_{bd}. Find an expression for the transfer function $A_v(j\omega) = V_o(j\omega)/V_{in}(j\omega)$ and sketch the frequency response in a Bode plot, assuming the following values: $g_m = 1.0$ mA/V, $r_{ds} = 75$ kΩ, $C_{gs} = 120$ fF, $C_{gd} = 6$ fF and $C_{bd} = 60$ fF. Find the low-frequency gain and the -3 dB cutoff frequency.

Solution:

The small-signal diagram is shown below.

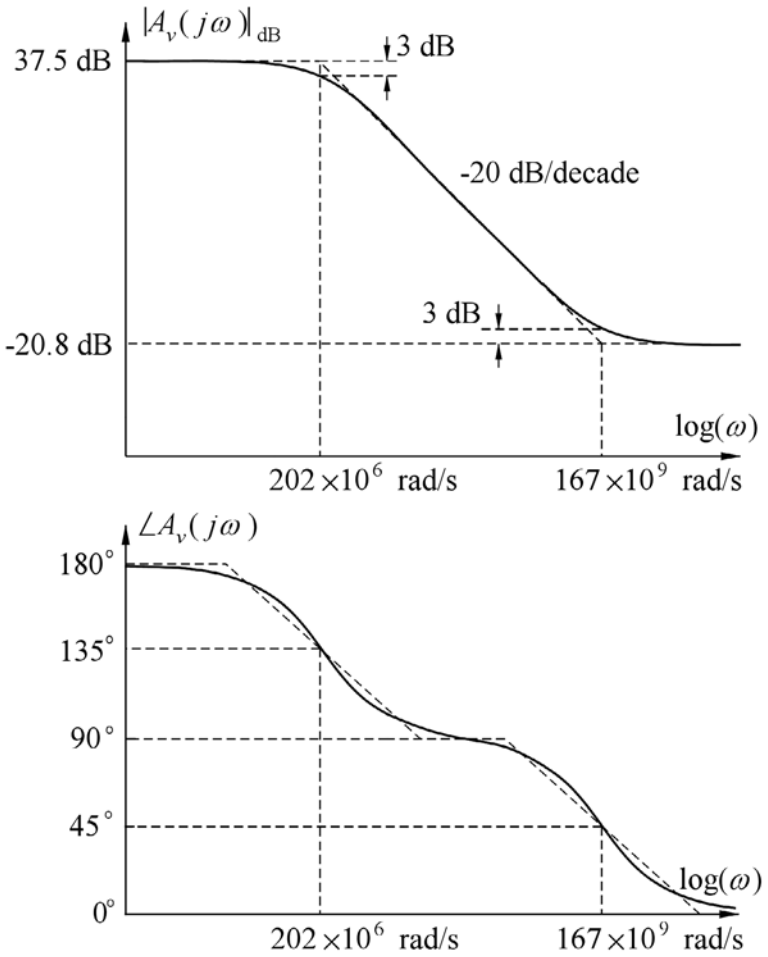


Using a node equation at the output node, we find

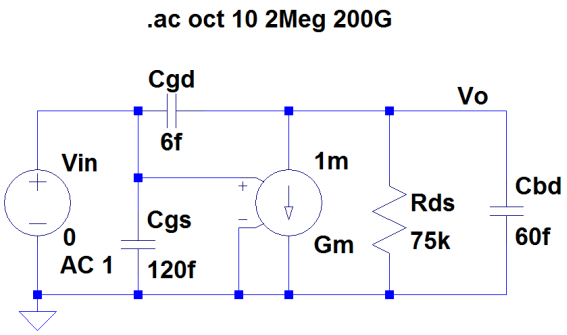
$$\begin{aligned} (V_{in}-V_o)\,j\omega C_{gd} &= g_m V_{in} + \frac{V_o}{r_{ds}} + V_o\, j\omega C_{bd} \\ \Rightarrow\quad A_v(j\omega) = \frac{V_o(j\omega)}{V_{in}(j\omega)} &= -\frac{(g_m - j\omega C_{gd})\, r_{ds}}{1 + j\omega\,(C_{gd}+C_{bd})\, r_{ds}} \end{aligned}$$

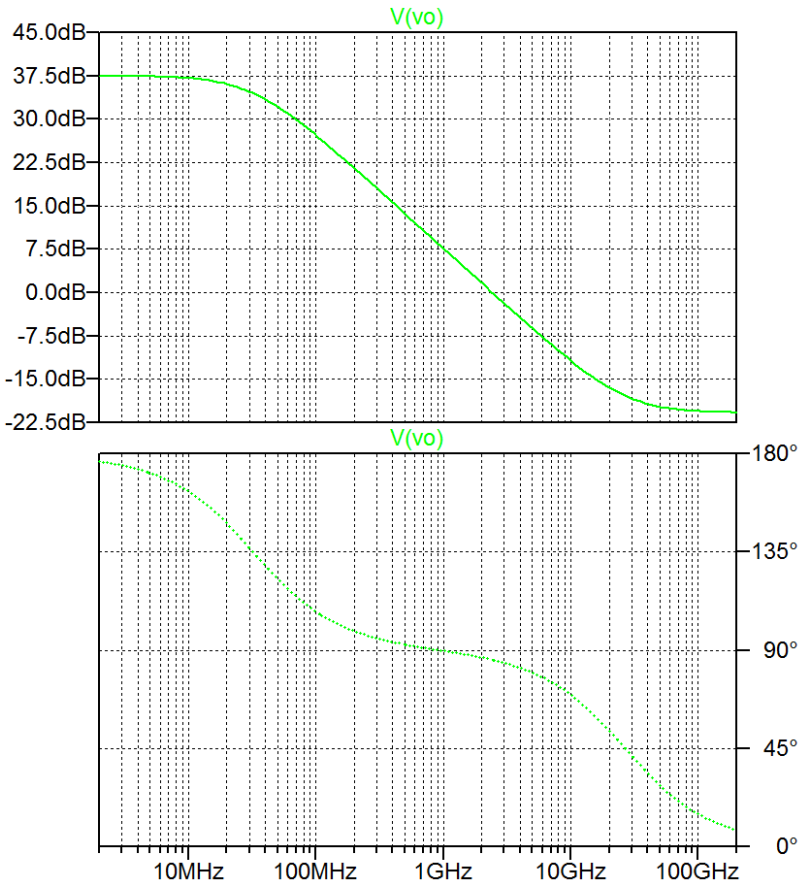
From the transfer function, we find the low-frequency gain $A_0 = -g_m r_{ds} = -75$ V/V ~ 37.5 dB and the pole frequency, equal to the -3 dB frequency, $\omega_p = ((C_{gd}+C_{bd})\, r_{ds})^{-1} = 202\times 10^6$ rad/s, corresponding to $f_p = 32.2$ MHz. We also find a right half-plane zero at the frequency $\omega_z = g_m/C_{gd} = 167\times 10^9$ rad/s, corresponding to $f_z = 26.5$ GHz. For $\omega \to \infty$, we find $A_v \to C_{gd}/(C_{gd}+C_{bd}) = 0.091$ V/V ~ -20.8 dB.

The following figure shows a sketch of the frequency response.

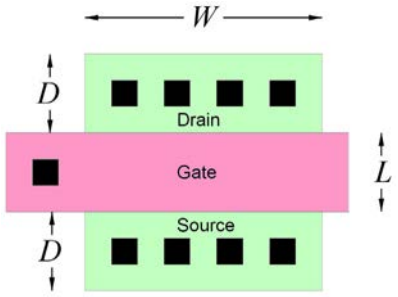


The frequency response may also be verified using LTspice. The following figure shows an LTspice schematic of the small-signal diagram and also a plot from a '.ac' simulation is shown. The similarity to the analytically derived Bode plot is apparent.





Problem 3.11



Shown above is the layout of an NMOS transistor. The green areas are the drain and source diffusions and the pink area is the polysilicon layer forming the gate. The transistor has the following dimensions: $W = 1.8$ µm, $L = 0.6$ µm and $D = 0.6$ µm. Assume a gate oxide capacitance of $C_{ox} = 8.5$ fF/(µm)^2 and calculate the capacitance C_{gs}, neglecting gate overlap capacitances. Also assume a junction capacitance of 3.65 fF/(µm)^2 for the bottom and 0.79 fF/µm for the sidewall of the drain diffusion at zero reverse bias voltage and calculate C_{bd} for a drain-bulk voltage of 0.9 V.

Next, assume an overlap capacitance from gate towards drain and source of 0.3 fF/µm and calculate C_{gd} and C_{gs}, including the overlap capacitance from gate to source.

Calculate the transconductance of the transistor for an effective gate-source voltage of 0.4 V and a drain-source voltage of 0.9 V, assuming $\mu_n C_{ox} = 180$ µA/V^2 and $\lambda = 0.10$ µmV$^{-1}/L$.

Finally, calculate the transition frequency f_T.

Solution:

When neglecting the overlap capacitance, C_{gs} is calculated from Eq. (3.85) in Bruun (2022):

$$C_{gs} = \frac{2}{3} WLC_{ox} = 6.12 \text{ fF}$$

The bulk-drain capacitance at zero bias is calculated from

$$C_{j0} = DW \cdot 3.65 \text{ fF/(µm)}^2 + (2D + W) \cdot 0.79 \text{ fF/µm} = 6.312 \text{ fF}.$$

When the bulk-drain junction is reverse biased by $V_R = V_{db} = 0.9$ V, the bulk-drain capacitance is reduced according to Eq. (3.1) in Bruun (2022). Using $\phi_0 = 0.8$ V and $m_j = 0.5$, we find

$$C_{bd} = C_{j0}(1 + V_R/\phi_0)^{-m_j} = 4.33 \text{ fF}.$$

Including the gate overlap capacitances, we find C_{gs} from Eq. (3.86) in Bruun (2022):

$$C_{gs} = \frac{2}{3} WLC_{ox} + C_{gs\text{ov}} = \frac{2}{3} WLC_{ox} + W \cdot 0.3 \text{ fF/µm} = 6.66 \text{ fF}.$$

The gate-drain capacitance is found from

$$C_{gd} = C_{gd\text{ov}} = W \cdot 0.3 \text{ fF/µm} = 0.54 \text{ fF}.$$

The transconductance is found from Eq. (3.64) in Bruun (2022):

$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)(1 + \lambda V_{DS}) = 248 \text{ µA/V}$$

where λ is found as $\lambda = 0.10 \text{ µmV}^{-1}/L = 0.167 \text{ V}^{-1}$.

The transition frequency f_T is found from Eq. (3.92) in Bruun (2022):

$$f_T \simeq \frac{g_m}{2\pi (C_{gs} + C_{gd})} = 5.5 \text{ GHz}.$$

Problem 3.12

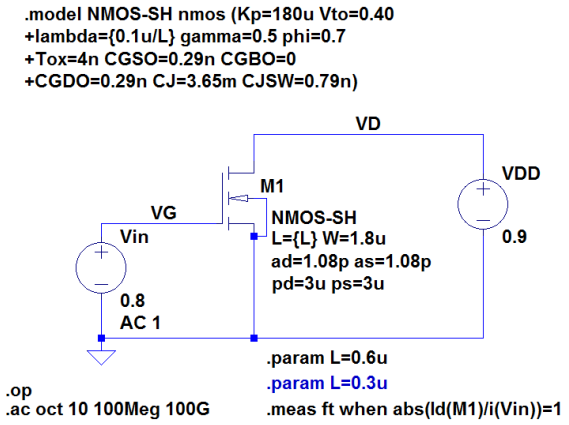
```
.model NMOS-SH nmos (Kp=180u Vto=0.40
+lambda={0.1u/L} gamma=0.5 phi=0.7
+Tox=4n CGSO=0.29n CGBO=0
+CGDO=0.29n CJ=3.65m CJSW=0.79n)
```

Use LTspice with the transistor model shown above to simulate the transistor capacitances and the transition frequency f_T of the transistor from Problem 3.11.
Suggest a change in the layout of the transistor which will increase the transition frequency f_T by a factor of 4.

Solution:

For simulating the circuit, we use the following LTspice schematic. We run both a '.op' simulation and a '.ac' simulation in order to find both the small-signal parameters from the '.op' simulation and the transition frequency using the '.meas' directive with the '.ac' simulation.

From the error log file, we find the following results: The gate-source capacitance without overlap is `Cgs` = 6.22 fF. The bulk-drain capacitance is `Cbd` = 4.33 fF. The gate-source capacitance including overlap is `Cgs` + `Cgsov` = 6.74 fF. The gate-drain overlap capacitance is `Cgdov` = 0.52 fF. The transconductance is `Gm` = 248 µA/V. The transition frequency is $f_T = 5.28588 \sim 5.3$ GHz.



From the SPICE Error Log.

```
Semiconductor Device Operating Points:
                          --- MOSFET Transistors ---
Name:           m1
Model:          nmos-sh
Gm:             2.48e-04
Gds:            7.20e-06
Gmb:            7.42e-05
Cbd:            4.33e-15
Cbs:            6.31e-15
Cgsov:          5.22e-16
Cgdov:          5.22e-16
Cgbov:          0.00e+00
Cgs:            6.22e-15
Cgd:            0.00e+00
Cgb:            0.00e+00

ft: abs(id(m1)/i(vin))=1 AT 5.28588e+009r
```

The transition frequency may be increased by reducing the channel length L. According to Eq. (3.93) in Bruun (2022), f_T is approximately inversely proportional to L^2, so f_T may be increased by a factor of 4 by reducing the channel length with a factor of 2. An LTspice simulation with $L = 0.3$ µm shows a value of 21.1 GHz for f_T.

References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Chapter 4 – Basic Gain Stages

Multiple-choice test

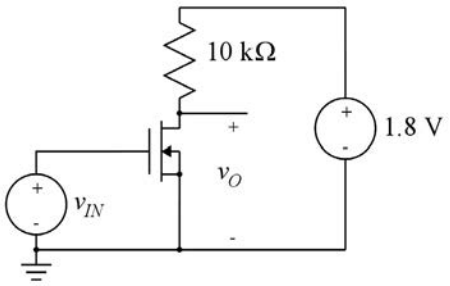
1. Completed statements:

A-7:	The low-frequency voltage gain in a common-source stage is always negative.
B-8:	The magnitude of the low-frequency voltage gain in a common-drain stage is smaller than one.
C-5:	The low-frequency voltage gain in a common-gate stage is always positive.
D-1:	The maximum output voltage from an NMOS common-source stage with an active load is less than the positive supply voltage by approximately $\lvert V_{\text{eff}}\rvert$.
E-2:	The output resistance of a common-drain stage where the gain transistor has source and bulk connected is on the order of $1/g_m$.
F-11:	The output resistance of a common-source stage biased by an active load is on the order of r_{ds}.
G-10:	The maximum output voltage from an NMOS common-drain stage is less than the positive supply voltage by approximately $\lvert V_{GS}\rvert$.
H-15:	A source follower is the same as a common-drain stage.
I-17:	A folded cascode is a combination of a common-source stage and a common-gate stage using different transistor types (NMOS/PMOS or PMOS/NMOS).
J-6:	The output resistance for a telescopic cascode biased by an ideal current source is on the order of $g_m r_{ds}^2$.

2. Completed statements:

A-8:	The common-mode input voltage to a differential pair is the average of the input voltages.
B-1:	The differential input voltage to a differential pair is the difference between the input voltages.
C-7:	A differential pair with a current mirror as an active load provides a single-ended output.
D-2:	For an ideal differential stage, the output voltage depends only on the differential input voltage.
E-3:	The dominant pole for a common-source stage driven by an ideal voltage source comes from the output node.
F-10:	For a common-source stage, the Miller effect causes an increased influence of C_{gd}.
G-6:	For a source follower, the Miller effect causes a reduced influence of C_{gs}.
H-16:	For a common-source stage, the dominant pole may come from the input node when the common-source stage is driven from a voltage source with a large series resistance.
I-17:	The gain-bandwidth product of a cascode stage with a transconductance of g_{m1} for the common-source stage and a load of $R_L \lvert\rvert (1/(sC_L))$ is $g_{m1}/(2\pi C_L)$.
J-11:	The input capacitance to a cascode stage with a load of $R_L \lvert\rvert (1/(sC_L))$ may be reduced by decreasing R_L.

3. For the circuit shown below, assume that the transistor has a bias overdrive voltage of 0.3 V and a bias current of 69 μA. Also assume that the channel-length modulation for the transistor can be neglected.



The bias value of the output voltage is

A: 0.69 V

B: 0.90 V

C: 1.11 V

Solution:

The voltage drop across the 10 kΩ load resistor is $V_{R_L} = 69\ \mu\text{A} \times 10\ \text{k}\Omega = 0.69$ V. With a supply voltage of $V_{DD} = 1.8$ V, this gives an output bias voltage of $V_O = 1.8\ \text{V} - 0.69\ \text{V} = 1.11$ V.

4. The small-signal gain v_o/v_{in} for the previous circuit is

A: $+2.3$ V/V

B: -2.3 V/V

C: -4.6 V/V

Solution:

The small-signal gain is $A_v = -g_m R_L$. With $I_D = 69$ μA and a bias overdrive input voltage $V_{IN} - V_t = 0.3$ V, we find $g_m = 2I_D/(V_{IN} - V_t) = 0.46$ mA/V, so $A_v = -0.46\ \text{mA/V} \times 10\ \text{k}\Omega = -4.6$ V/V.

5. The minimum output voltage obtainable from the previous circuit with the transistor in the active region is approximately

A: 0.30 V

B: 0.42 V

C: 0.69 V

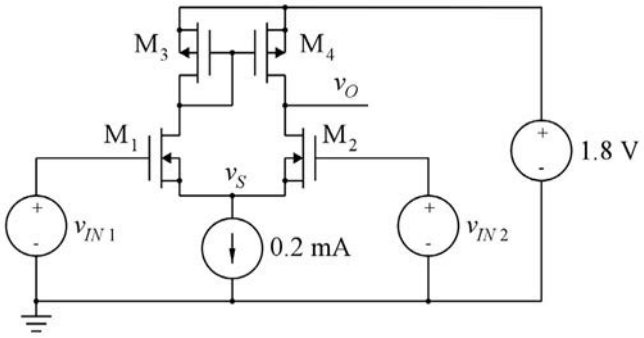
Solution:

The minimum output voltage is obtained for $v_{IN} - V_t = v_{DS} = v_{O\min}$, i.e., when the transistor is at the border between the triode region and the active region. For an overdrive voltage of 0.30 V, we have a drain current of 69 μA, giving a drain-source voltage (equal to the output voltage) of 1.11 V which is obviously different from the overdrive voltage of 0.30 V, so this is not the correct solution.

From the Schichman-Hodges model, we notice that the drain current with the transistor in the active region is proportional to the square of the overdrive voltage, so with an overdrive voltage of 0.42 V, we find a drain current of $I_D = (0.42/0.30)^2 \times 69\ \mu\text{A} \simeq 138\ \mu\text{A}$, giving a drain-source voltage of $V_{DS} = 1.8\ \text{V} - 138\ \mu\text{A} \times 10\ \text{k}\Omega = 0.42\ \text{V}$, i.e., a value equal to the overdrive voltage, so 0.42 V is the minimum output voltage obtainable with the transistor in the active region.

For an overdrive voltage of 0.69 V, the Shichman-Hodges model gives $I_D = (0.69/0.30)^2 \times 69\ \mu\text{A} \simeq 365\ \mu\text{A}$ when assuming the transistor in the active region. This would create a voltage drop of 3.65 V across the 10 kΩ resistor which is obviously not possible, so the transistor is not in the active region but in the linear region.

6. For the differential gain stage shown below, assume that all transistors are in the active region and have a channel-length modulation parameter $\lambda = 0.1\ \text{V}^{-1}$.



The small-signal output resistance of the differential gain stage is approximately

A: 50 kΩ

B: 100 kΩ

C: 200 kΩ

Solution:

The small-signal output resistance is $r_{out} = r_{ds2} \parallel r_{ds4}$. The transistor output resistances are given by $r_{ds} \simeq 1/(\lambda I_D)$. As the tail current to the differential pair is 0.2 mA, the current in each of the transistors in differential pair is $I_D = 0.2\ \text{mA}/2 = 0.1\ \text{mA}$, and with $\lambda = 0.1\ \text{V}^{-1}$ for all transistors, we find $r_{ds2} = r_{ds4} \simeq 100\ \text{k}\Omega$ and $r_{out} \simeq 50\ \text{k}\Omega$.

7. With all transistors in the differential gain stage shown before having an effective gate voltage of $|V_{GS} - V_t| = 0.25\ \text{V}$, the small-signal differential gain is approximately

A: 20 V/V

B: 40 V/V

C: 80 V/V

Solution:

The small-signal differential gain is $A_d \simeq g_{m1} r_{out}$. The transconductance g_{m1} is $g_{m1} = 2I_{D1}/(V_{GS1} - V_{tn}) = 0.8\ \text{mA/V}$, so with $r_{out} \simeq 50\ \text{k}\Omega$, we find $A_d \simeq 40\ \text{V/V}$.

8. For the differential gain stage shown before, assume that the threshold voltage for the PMOS transistors is -0.42 V. With a bias voltage of 0.9 V for both input voltages, the bias value of the gate voltage for the PMOS transistors is

   A: 0.67 V
   B: 1.13 V
   C: 2.22 V

Solution:

With an effective gate voltage of $|V_{GS} - V_{tp}| = 0.25$ V and a threshold voltage of $V_{tp} = -0.42$ V for the PMOS transistors, we find $V_{GS} = -0.67$ V for the PMOS transistors. The source voltage of the PMOS transistors is $V_{S3} = V_{S4} = V_{DD} = 1.8$ V, so the gate voltage of the PMOS transistors is $V_{G3} = V_{G4} = V_{GS3} + V_{S3} = 1.13$ V. We notice that $V_{D1} = V_{G3} > V_{G1}$, so M_1 and M_2 are in the active region.

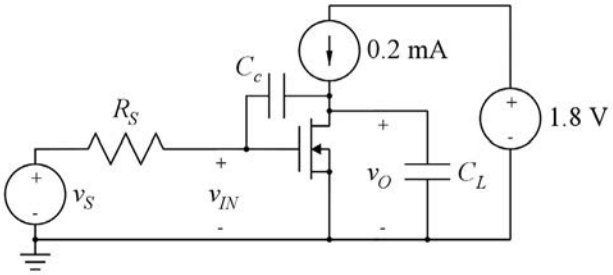
9. If the input voltages for the differential gain stage shown before are changed so that all of the bias current flows in M_1 - M_3, the gate voltage of the PMOS transistors is changed to approximately

   A: 0.63 V
   B: 0.77 V
   C: 1.03 V

Solution:

If the bias current in M_3 is increased by a factor of 2, the effective gate-source voltage of M_3 is increased by a factor of $\sqrt{2}$ according to the Shichman-Hodges model. With $|V_{GS3} - V_{tp}| = 0.25 \times \sqrt{2}$ V, we find $V_{GS3} \simeq -0.77$ V, so the gate voltage of the PMOS transistors is $V_{G3} = V_{G4} = V_{GS3} + V_{S3} = 1.03$ V.

10. For the circuit shown below, assume that the transistor is in the active region with $r_{ds} = 40$ kΩ and $g_m = 0.5$ mA/V. Also assume that all transistor capacitances are negligible compared to C_L and C_c.



   With $C_c = 0.1$ pF, $C_L = 0.1$ pF and $R_S = 40$ kΩ, the dominant time constant
   A: originates from the output and is about 4 ns.
   B: originates from the input and is about 4 ns.
   C: originates from the input and is about 80 ns.

Solution:

The small-signal low-frequency gain in the common-source stage is $A_v = -g_m r_{ds} = -20$ V/V. Thus, using the Miller theorem, we find the input capacitance as $C_{in} \simeq (1 - A_v)C_c \simeq |A_v|C_c = 2$ pF and with

$R_S = 40$ kΩ, we find a time constant of approximately $\tau_{in} = R_S C_{in} \simeq 80$ ns. We notice that for $\omega = 1/\tau_{in}$, $R_S = 40$ kΩ is much smaller than $1/(\omega C_c) = \tau_{in}/C_c \simeq 800$ kΩ, so when estimating the time constant from the output, we may use Eq. (4.83) from Bruun (2022), giving $\tau_{out} \simeq r_{ds} C_L = 4$ ns.
As $\tau_{in} \gg \tau_{out}$, the dominant time constant originates from the input and is about 80 ns.

11. With $C_c = 0.01$ pF, $C_L = 2$ pF and $R_S = 40$ kΩ, the dominant time constant

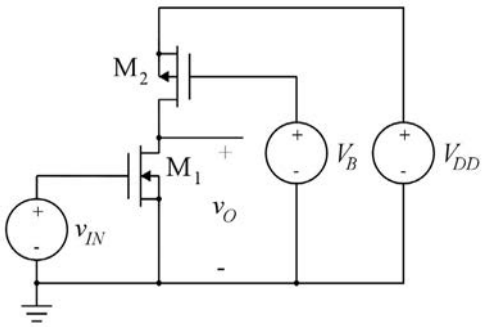
    A: originates from the output and is about 80 ns.
    B: originates from the input and is about 0.4 ns.
    C: originates from the input and is about 80 ns.

Solution:

Using the Miller theorem, we find the input capacitance as $C_{in} \simeq g_m r_{ds} C_c = 0.2$ pF and with $R_S = 40$ kΩ, we find a time constant of approximately $\tau_{in} = R_S C_{in} \simeq 8$ ns. Using Eq. (4.83) from Bruun (2022), we find a time constant from the output of approximately $\tau_{out} \simeq r_{ds} C_L = 80$ ns. We notice that for $\omega = 1/\tau_{out}$, $R_S = 40$ kΩ is much smaller than $1/(\omega C_c) = \tau_{out}/C_c \simeq 8$ MΩ, so using Eq. (4.83) from Bruun (2022) is reasonable for frequencies close to $1/\tau_{out}$. As $\tau_{out} \gg \tau_{in}$, the dominant time constant originates from the output and is about 80 ns.

Problems

Problem 4.1



For both transistors M_1 and M_2 in the common-source stage shown above, assume $W/L = 3$. Further, assume that the channel-length modulation can be neglected for both transistors and that $\mu_n C_{ox} = 180\ \mu A/V^2$, $\mu_p C_{ox} = 45\ \mu A/V^2$, $V_{tn} = 0.4$ V and $V_{tp} = -0.42$ V. The supply voltage is $V_{DD} = 1.8$ V and the bias voltage V_B is $V_B = 980$ mV.
Calculate the bias current in M_1 and M_2, assuming that they are both in the active region and find the bias value of the input voltage for which the transistors are in the active region.
Find the output voltage range for which the transistors are in the active region.

Problem 4.2 is a follow-up to this problem.

Solution:

Transistor M_2 is connected as a dc current source providing the bias current for M_1. The bias current is found using the Shichman-Hodges model:

$$I_{D1} = I_{D2} = \frac{1}{2}\mu_p C_{ox}\frac{W_2}{L_2}(V_{GS} - V_{tp})^2 = \frac{1}{2} \times 45\ \mu A/V^2 \times 3 \times (0.98\ V - 1.8\ V - (-0.42\ V))^2 = 10.8\ \mu A$$

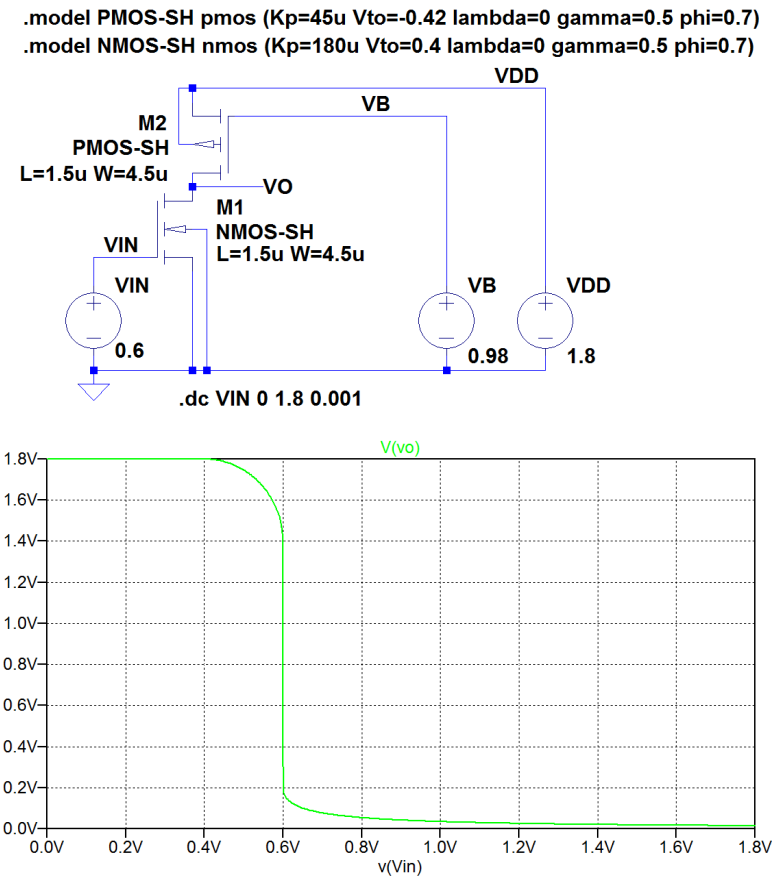
For M_1, we find the bias voltage V_{IN} as

$$V_{IN} = V_{GS1} = V_{tn} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W_1/L_1)}} = 0.4\ V + \sqrt{\frac{2 \times 10.8\ \mu A}{180\ \mu A/V^2 \times 3}} = 0.6\ V$$

For M_1 to be in the active range, we require $v_{DS1} \geq v_{GS1} - V_{tn} \Rightarrow v_O \geq V_{IN} - V_{tn} = 0.2$ V.

For M_2 to be in the active range, we require $|v_{DS2}| \geq |v_{GS1}| - |V_{tp}| \Rightarrow V_{DD} - v_O \geq V_{DD} - V_B - |V_{tp}| \Rightarrow v_O \leq V_B + |V_{tp}| = 1.4$ V.

For verifying the result, we run a '.dc' simulation from the following LTspice schematic. The transistor geometries have been chosen to be $L_1 = L_2 = 1.5\ \mu$m and $W_1 = W_2 = 4.5\ \mu$m. The output plot from the simulation shows that $v_{IN} = 0.6$ V for $0.2\ V \leq v_O \leq 1.4$ V as expected. With $\lambda = 0$ (no channel-length modulation), the gain is infinite when the transistors are in the active region.



Problem 4.2

For the common-source stage from Problem 4.1, assume now that the channel-length modulation is defined by the parameters specified in Table 3.1. The channel length is $L = 1.5$ µm for both transistors. Calculate the small-signal voltage gain $A_v = v_o/v_{in}$. You may use reasonable approximations when calculating the small-signal parameters.
Also use LTspice to find the value of $A_v = v_o/v_{in}$.

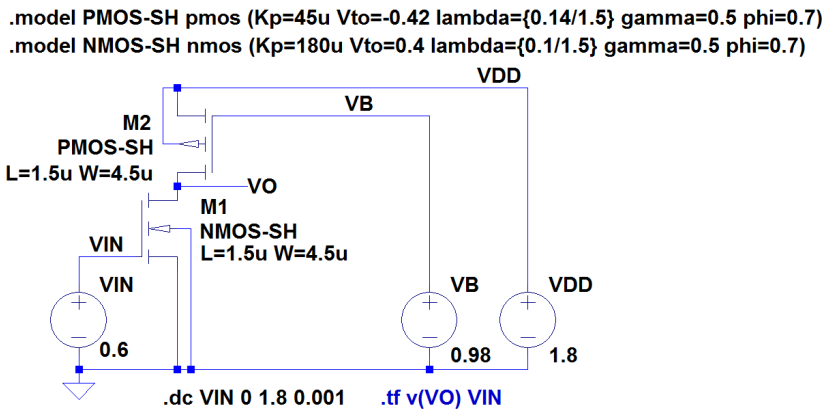
For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

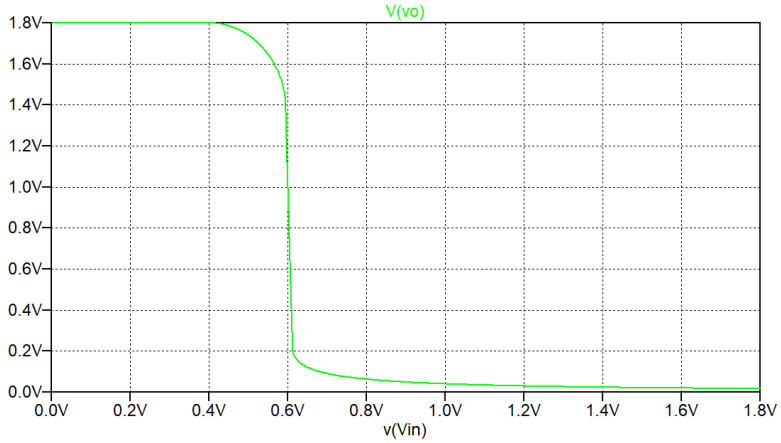
The small-signal gain is $A_v = v_o/v_{in} = -g_{m1}\,(r_{ds1} \parallel r_{ds2}) = -g_{m1}/(g_{ds1} + g_{ds2})$ where g_{m1} is found from Eq. (3.69) and approximate values for g_{ds1} and g_{ds2} are found from Eq. (3.72) in Bruun (2022).
We find, using $I_{D1} = I_{D2}$ and $\lambda_1 = 0.1$ µm/V/1.5 µm and $\lambda_2 = 0.14$ µm/V/1.5 µm

$$A_v \simeq -\left(\frac{2I_{D1}}{(V_{IN} - V_{tn})}\right)\left(\frac{1}{(\lambda_1 + \lambda_2)I_{D1}}\right) = -\frac{2}{(V_{IN} - V_{tn})(\lambda_1 + \lambda_2)} = -62.5 \text{ V/V}$$

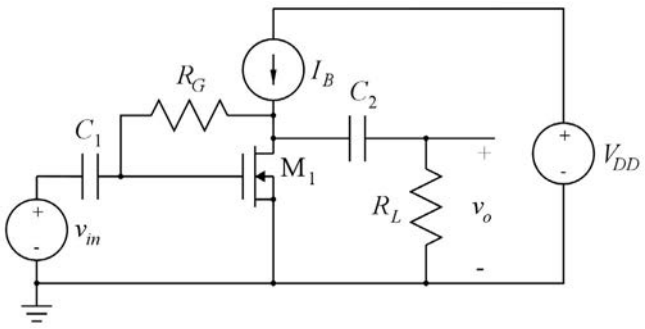
We may find the gain using a '.tf' simulation in LTspice. The schematic for this is shown below. From the output file, we find $A_v = -66.9$ V/V with an input bias voltage $V_{IN} = 0.6$ V. This value is slightly larger than the calculated value because the factor $(1 + \lambda V_{DS})$ has been neglected in the calculation of g_{ds1} and g_{ds2}.



Running a '.dc' simulation, we may plot v_O versus v_{IN} as shown in the following figure. We notice that the slope of v_O now has a finite value for $V_{IN} = 0.6$ V, so the gain is no longer infinite as in Problem 4.1.



Problem 4.3



For the common-source stage shown above, we assume $R_G = 1$ MΩ, $I_B = 20$ μA and $R_L = 100$ kΩ. The capacitors C_1 and C_2 are very large and can be treated as short circuits for ac currents but open circuits for dc currents. Transistor M_1 has $V_t = 0.4$ V and $\mu_n C_{ox}(W/L) = 0.6$ mA/V^2. The channel-length modulation can be neglected.

Find the bias voltages V_{GS1} and V_{DS1}.

Find an expression for the small-signal gain v_o/v_{in} for frequencies where C_1 and C_2 are ac short circuits and the transistor capacitances can be neglected.

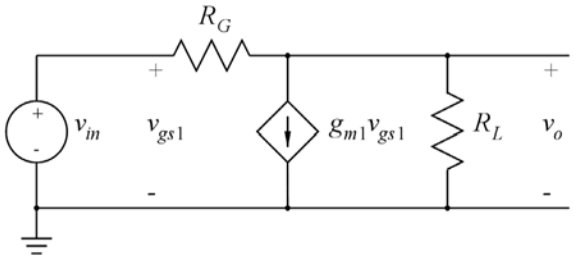
Calculate the numerical value of the small-signal gain.

Solution:

We notice that there is no dc current flowing in R_G, so $V_{G1} = V_{D1} = V_{GS1} = V_{DS1}$. Also, there is no dc current flowing in R_L, so $I_{D1} = I_B$. The bias voltage is found from the bias current using the Shichman-Hodges transistor model, i.e.,

$$V_{DS1} = V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W_1/L_1)}} = 0.658 \text{ V}.$$

For finding the small-signal gain, we draw a small-signal schematic as shown below where C_1 and C_2 are replaced by short circuits.



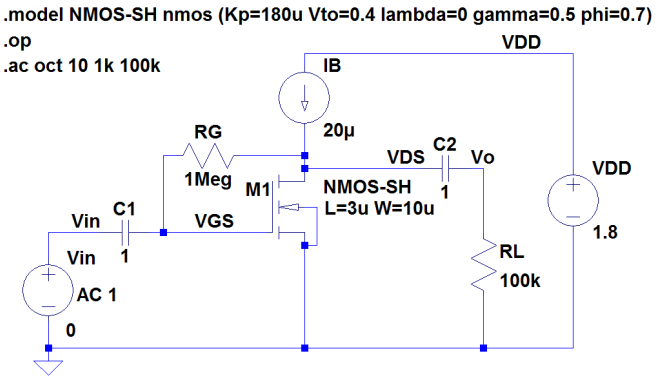
A node equation at the output node gives

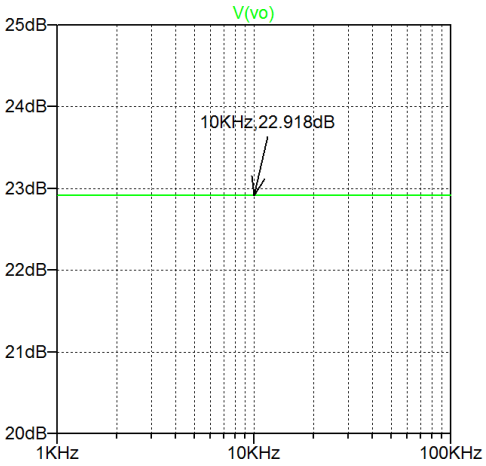
$$\begin{aligned} \frac{v_{in} - v_o}{R_G} &= g_{m1}v_{in} + \frac{v_o}{R_L} \\ \Rightarrow \quad \frac{v_o}{v_{in}} &= -\left(g_{m1} - \frac{1}{R_G}\right)(R_L \parallel R_G) \end{aligned}$$

where $g_{m1} = \dfrac{2I_{D1}}{V_{GS1} - V_t} = 155$ µA/V.

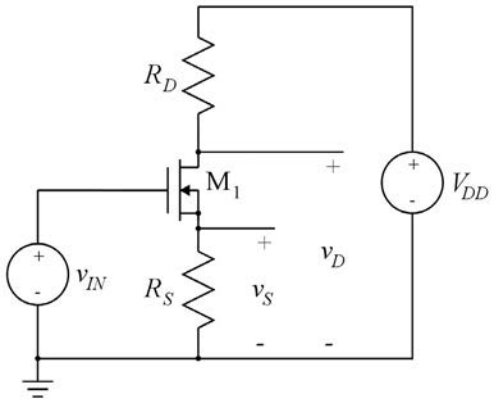
Inserting numerical values in the expression for v_o/v_{in}, we find $v_o/v_{in} = -14$ V/V.

The result may be verified using LTspice. The LTspice schematic is shown below. The capacitors have been selected to $C_1 = C_2 = 1$ F and the transistor geometries have been selected to $W_1 = 10$ µm and $L = 3$ µm, giving $\mu C_{ox}(W/L) = 0.6$ mA/V^2 with $\mu C_{ox} = 180$ µA/V^2. From a '.op' simulation, we find $V_{DS1} = \texttt{v(VDS)} = 0.6582$ V, closely matching the calculated value. The small-signal gain is found from a '.ac' simulation which is run from 1 kHz to 100 kHz where C_1 and C_2 can be considered as short circuit. The output plot shows a gain of 22.918 dB, corresponding to -14 V/V. It may be noted that since the circuit uses coupling capacitors, a '.tf' simulation cannot be used to find the gain.





Problem 4.4



Shown above is a gain stage with two outputs, v_D and v_S. The resistors R_D and R_S have the values $R_D = 10\ \text{k}\Omega$ and $R_S = 5\ \text{k}\Omega$. The supply voltage is $V_{DD} = 1.8$ V. The transistor has $V_t = 0.4$ V and $\mu_n C_{ox} = 180\ \mu\text{A/V}^2$. The channel-length modulation and the body effect can be neglected.

Design the transistor to have a transconductance of 0.6 mA/V and to give a bias value of 1.2 V for V_D. Use a channel length of $L = 3\ \mu$m.

Calculate the bias values of v_S and v_{IN}.

Draw a small-signal equivalent circuit and find expressions for the small-signal gains v_d/v_{in} and v_s/v_{in}. Find numerical values for the small-signal gains.

Solution:

With $V_D = 1.2$ V, we find the drain current $I_D = (V_{DD} - V_D)/R_D = 60\ \mu$A.

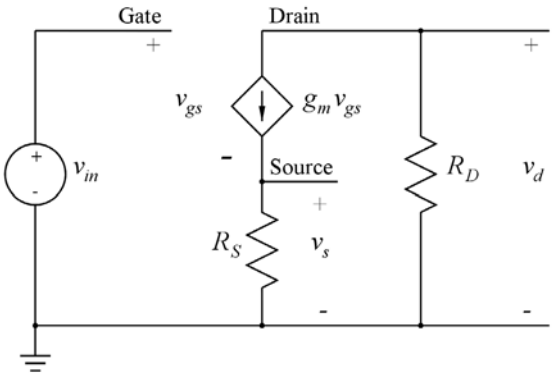
From $g_m = \dfrac{2I_D}{V_{GS} - V_t}$, we find $V_{GS} - V_t = \dfrac{2I_D}{g_m} = 0.2$ V.

From $g_m = \mu_n C_{ox} \left(\dfrac{W}{L}\right)(V_{GS} - V_t)$, we find $W = L\dfrac{g_m}{\mu_n C_{ox}(V_{GS} - V_t)} = 50\ \mu$m.

The bias value of v_S is found from Ohm's law: $V_S = R_S I_S = R_S I_D = 0.3$ V.

The bias value of v_{IN} is found as $V_{IN} = V_S + V_{GS} = V_S + (V_{GS} - V_t) + V_t = 0.3\ \text{V} + 0.2\ \text{V} + 0.4\ \text{V} = 0.9\ \text{V}$.

The small-signal diagram corresponding to Problem 4.4 is shown in the following figure.



A node equation at the source of the transistor gives $g_m v_{gs} = g_m(v_{in} - v_s) = \dfrac{v_s}{R_S}$.

Rearranging, we find $v_s\left(\dfrac{1}{R_S} + g_m\right) = g_m v_{in} \Rightarrow \dfrac{v_s}{v_{in}} = \dfrac{R_S g_m}{1 + R_S g_m}$.

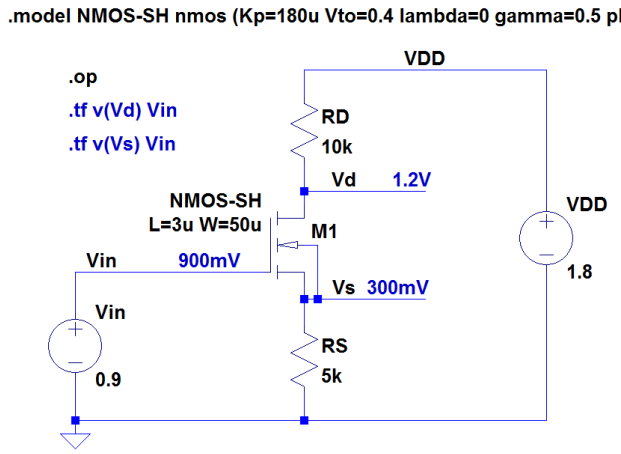
Inserting numerical values, we find $\dfrac{v_s}{v_{in}} = 0.75$ V/V.

The drain voltage is found from

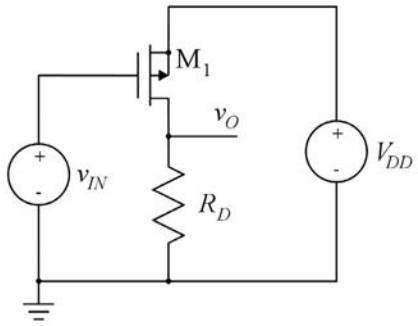
$$v_d = -R_D g_m v_{gs} = -R_D \frac{v_s}{R_S} = -\left(\frac{R_D}{R_S}\right)\left(\frac{R_S g_m}{1 + R_S g_m}\right) v_{in} \Rightarrow \frac{v_d}{v_{in}} = -\frac{R_D g_m}{1 + R_S g_m}.$$

Inserting numerical values, we find $\dfrac{v_d}{v_{in}} = -1.5$ V/V.

The numerical results may be verified using LTspice. The following figure shows the LTspice schematic corresponding to Problem 4.4. From a '.op' simulation, we find the bias values of v_{IN}, v_D and v_S (shown in the schematic), and from the error log file, we verify $g_m = 0.6$ mA/V. Using the '.tf' simulations shown as comments in the schematic, we verify $v_d/v_{in} = -1.5$ V/V and $v_s/v_{in} = 0.75$ V/V.



Problem 4.5



Design the common-source stage shown above to have a low-frequency small-signal gain of 17 dB. For the transistor, use $V_t = -0.42$ V, $\mu_p C_{ox} = 45$ µA/V^2 and $\lambda = 0$. Use a channel length of 2 µm. The supply voltage is $V_{DD} = 1.8$ V, and you should design for a bias value of the output voltage of $V_{DD}/2$ and a bias current in M_1 of 50 µA.
Calculate the bias value of the input voltage for your design.

Solution:

With a bias current $I_{D1} = 50$ µA and a bias value of the output voltage of $V_O = V_{DD}/2 = 0.9$ V, we find from Ohm's law $R_D = V_O/I_{D1} = 18$ kΩ.

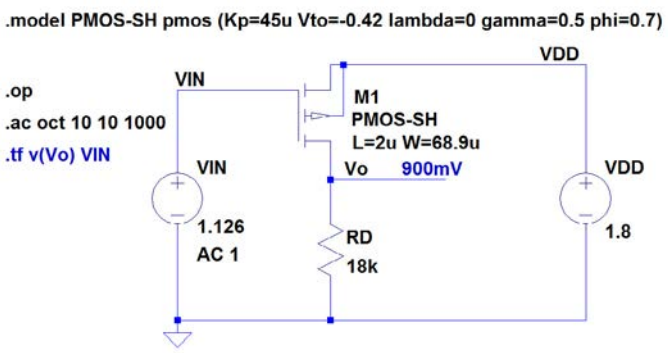
The small-signal gain of the stage is $A_d = -g_{m1}R_D$ and with $A_d = 17$ dB ~ -7.08 V/V, we find $g_{m1} = -A_d/R_D = 393$ µA/V.

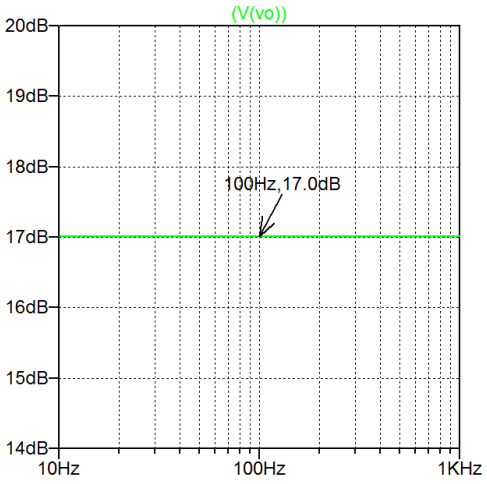
Using $g_{m1} = 2I_{D1}/|V_{GS1} - V_t| = 2I_{D1}/|V_{\text{eff1}}|$, we find $|V_{\text{eff1}}| = 254$ mV.

From $g_{m1} = \mu C_{ox}\left(\frac{W_1}{L_1}\right)|V_{\text{eff1}}|$, we find $W_1 = L_1\frac{g_{m1}}{\mu C_{ox}|V_{\text{eff1}}|} = 68.9$ µm.

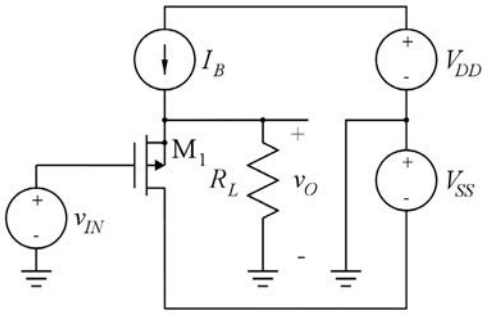
The bias value of the input voltage is found using Kirchhoff's voltage law:
$V_{IN} = V_{DD} - |V_{GS1}| = V_{DD} - |V_{\text{eff1}}| - |V_t| = 1.8\text{ V} - 0.254\text{ V} - 0.42\text{ V} = 1.126$ V.

The result may be verified using LTspice. The following figure shows the LTspice schematic corresponding to Problem 4.5. Using a '.op' simulation, the bias point is verified and using a '.ac' simulation, the gain is verified. Alternatively, the gain may be verified using a '.tf' simulation (shown as a comment in the LTspice schematic).





Problem 4.6



Shown above is a common-drain stage with a PMOS transistor. Assume the following transistor parameters: $L = 1$ µm, $W = 80$ µm, $\mu_p C_{ox} = 45$ µA/V^2, $V_t = -0.42$ V and $\lambda = 0.14$ V^{-1}. The bias current I_B has a value of 125 µA and the supply voltages are $V_{DD} = V_{SS} = 0.9$ V.
Find the bias value of v_{IN} which gives a bias value of 0 V for v_O.
Find the small-signal open-circuit voltage gain A_{voc} and output resistance r_{out}.
Find the small-signal voltage gain $A_v = v_o/v_{in}$ with $R_L = 5$ kΩ.
Use LTspice to find the output voltage range for $R_L = 5$ kΩ, assuming that the voltage across the current source I_B must be at least 0.3 V.

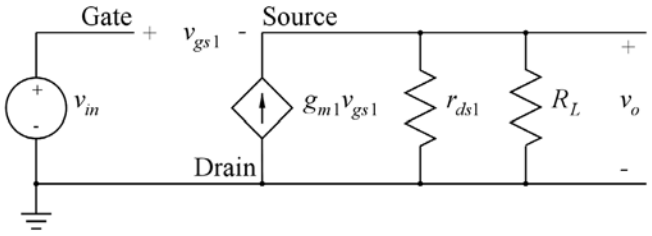
Solution:

We have $V_{IN} = V_O - |V_{GS1}|$, so with $V_O = 0$, we find using the Shichman-Hodges model

$$\begin{aligned} V_{IN} = -|V_{GS1}| &= -\left(|V_t| + \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W_1/L_1)(1+\lambda|V_{DS1}|)}}\right) \\ &= -\left(|V_t| + \sqrt{\frac{2I_B}{\mu_p C_{ox}(W_1/L_1)(1+\lambda V_{SS})}}\right) = -0.668 \text{ V} \end{aligned}$$

For finding the small-signal gain and output resistance, we draw the small-signal diagram shown below corresponding to Problem 4.6. The small-signal parameters are:

$g_{m1} = \sqrt{2\mu_p C_{ox}(W_1/L_1) I_{D1}(1+\lambda|V_{DS1}|)} = 1.007$ mA/V and $r_{ds1} = (1+\lambda|V_{DS1}|)/(\lambda I_{D1}) = 63.3$ kΩ.



The small-signal open-circuit voltage gain A_{voc} is found as v_o/v_{in} with $R_L = \infty$, i.e., R_L omitted from the small-signal diagram.

Using a node equation at the output, we find

$$g_{m1}(v_{in} - v_o) = \frac{v_o}{r_{ds1}} \quad \Rightarrow \quad A_{voc} = \frac{v_o}{v_{in}} = \frac{g_{m1}\, r_{ds1}}{1 + g_{m1}\, r_{ds1}} = 0.985 \text{ V/V}$$

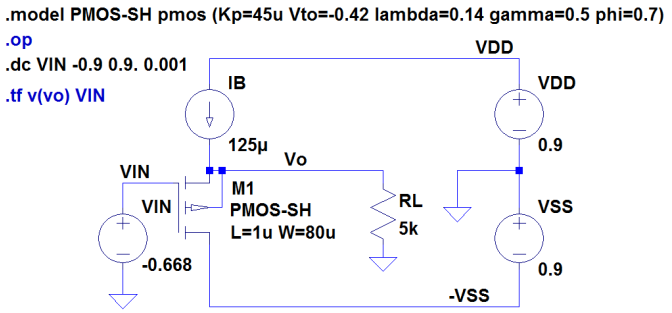
The output resistance may be found by applying a current i_o to the output with $v_{in} = 0$ and calculating v_o/i_o, still with R_L omitted (Bruun 2022). We find

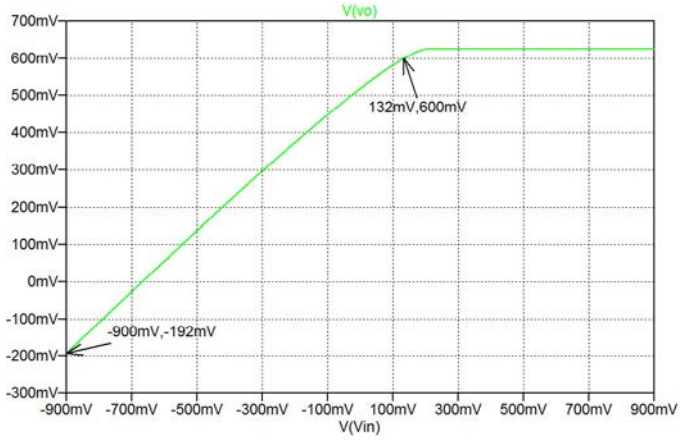
$$i_o + g_{m1}v_{gs1} = i_o - g_{m1}v_o = \frac{v_o}{r_{ds1}} \quad \Rightarrow \quad r_{out} = \frac{v_o}{i_o} = \frac{1}{g_{m1} + 1/r_{ds1}} = 978\ \Omega$$

The small-signal gain with $R_L = 5$ kΩ is found from $A_v = A_{voc}\,(R_L/(R_L + r_{out})) = 0.824$ V/V.

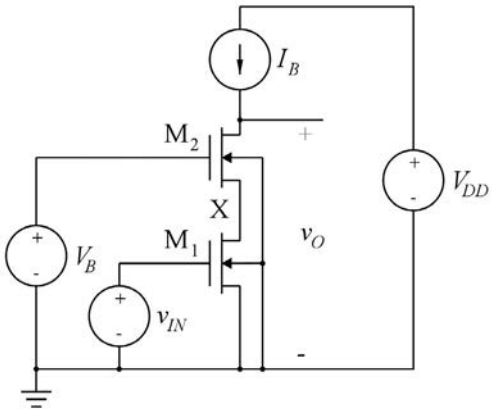
An LTspice schematic corresponding to Problem 4.6 is shown below. Using a '.op' simulation, the bias point may be verified and using a '.tf' simulation with 'RL' deleted, the values of A_{voc} and r_{out} may be verified. The value of the gain A_v may be verified using a '.tf' simulation with 'RL' included in the schematic.

Running a 'dc' simulation results in the following plot of the output voltage. From the plot, we find the minimum value of the output voltage to be $v_{O\min} = -0.192$ V, and from the requirement that the voltage across the current source I_B must be at least 0.3 V, we find the maximum output voltage to be $v_{O\max} = 0.6$ V.





Problem 4.7



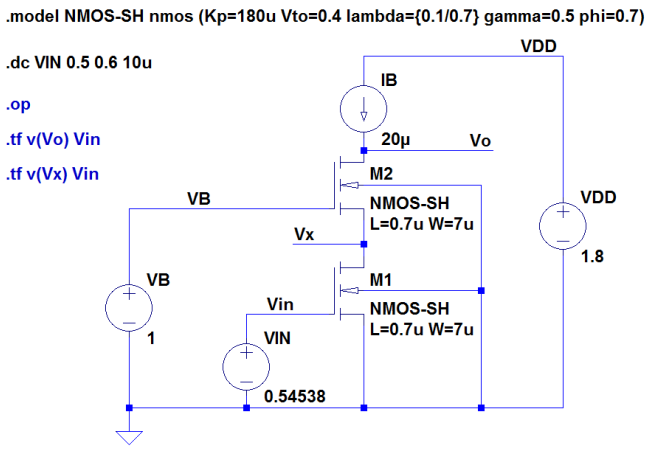
For the telescopic cascode shown above, use LTspice to find the bias value V_{IN} of the input voltage required to give an output bias voltage of 0.9 V. Assume $V_{DD} = 1.8$ V, $V_B = 1.0$ V, $I_B = 20$ µA, $L_1 = L_2 = 0.7$ µm, $W_1 = W_2 = 7$ µm and use transistor parameters as specified in Table 3.1.
Also find the small-signal gain A_{voc} and output resistance r_{out}.
Find the small-signal resistance r_x to ground from the node X between the source of M_2 and the drain of M_1 and find the small-signal voltage gain from the input to node X.

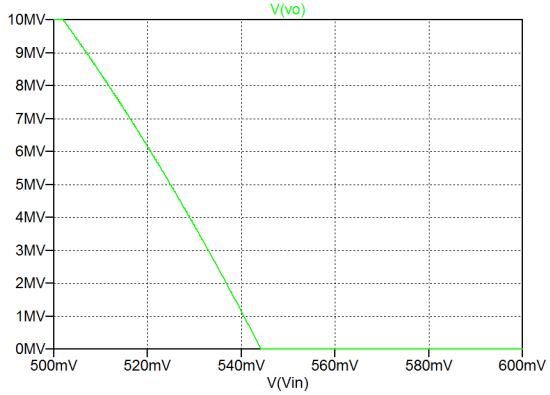
For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

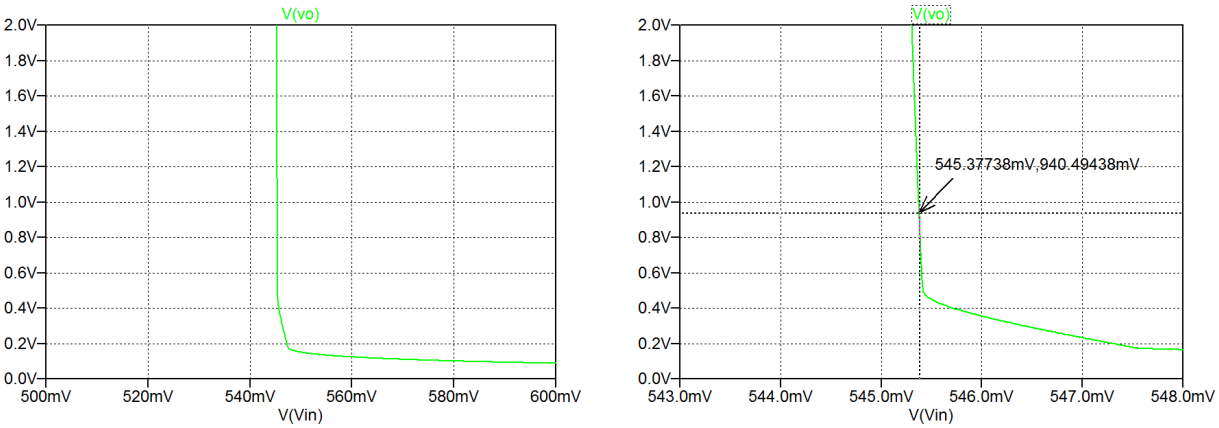
The following figure shows an LTspice schematic corresponding to Problem 4.7. From the Shichman-Hodges model with $\lambda = 0$, we find that with $W_1/L_1 = 10$, the input bias voltage V_{IN} required for a bias current of 20 µA is about $V_{IN} \simeq V_t + \sqrt{\dfrac{2I_B}{\mu C_{ox}(W_1/L_1)}} = 549$ mV.

In order to find the exact value of the input bias voltage, we run a '.dc' simulation with V_{IN} swept from 500 mV to 600 mV, i.e., around the estimated value. The resulting plot of the output voltage is shown below. Apparently, the simulation generates unrealistically high output voltages, several MV. This is due to the fact that the drain of M_2 is connected directly to an ideal dc current source.





In order to see '`V(vo)`' in a realistic range of output voltages, we set the range of the y-axis to 2 V, either by the command 'Plot Settings → Manual Limits' or by moving the cursor to the y-axis and using a right-click on the mouse. The resulting plot is shown below, left plot. We see that the output voltage changes abruptly for an input voltage of about 545 mV, and in order to find the exact input voltage, we zoom in on a small part of the plot, see right plot below. From this, we find $V_{IN} = 545.38$ mV.

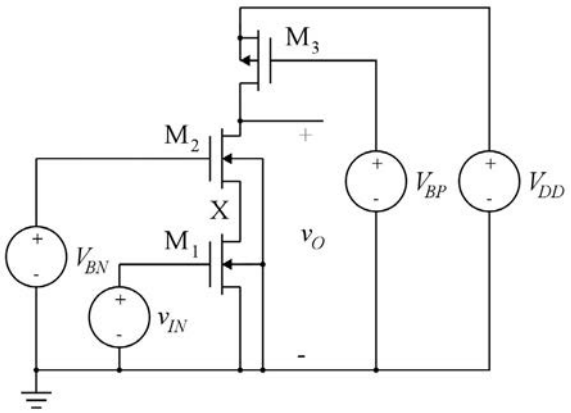


In order to verify the bias point, we run a '.op' simulation with a dc value of V_{IN} specified to 545.38 mV. From the output file, we find $V_O = 905$ mV which is sufficiently close to 0.9 V.

With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a '.tf' simulation with '`V(Vo)`' as the output and '`Vin`' as the source. The output file from this '.tf' simulation shows a gain of -13326 V/V ~ 82.5 dB and an output resistance of 48.8 MΩ.

For finding the small-signal resistance r_x to ground from the node X between the source of M_2 and the drain of M_1 and the small-signal gain from the input to node X, we run a '.tf' simulation with '`V(Vx)`' as the output and '`Vin`' as the source. From this, we find a resistance r_x of 368 kΩ and a gain of $A_{vx} = -101$ V/V ~ 40.1 dB.

Problem 4.8



For the telescopic cascode shown above, use LTspice to find the bias value V_{IN} of the input voltage required to give an output bias voltage of 0.9 V. Assume $V_{DD} = 1.8$ V, $V_{BN} = 1.0$ V, $V_{BP} = 1.25$ V, $L_1 = L_2 = L_3 = 0.7$ µm, $W_1 = W_2 = 7$ µm, $W_3 = 28$ µm and use transistor parameters as specified in Table 3.1. Also find the small-signal gain A_{voc} and output resistance r_{out}.

Find the small-signal resistance r_x to ground from the node X between the source of M_2 and the drain of M_1 and find the small-signal voltage gain from the input to node X.

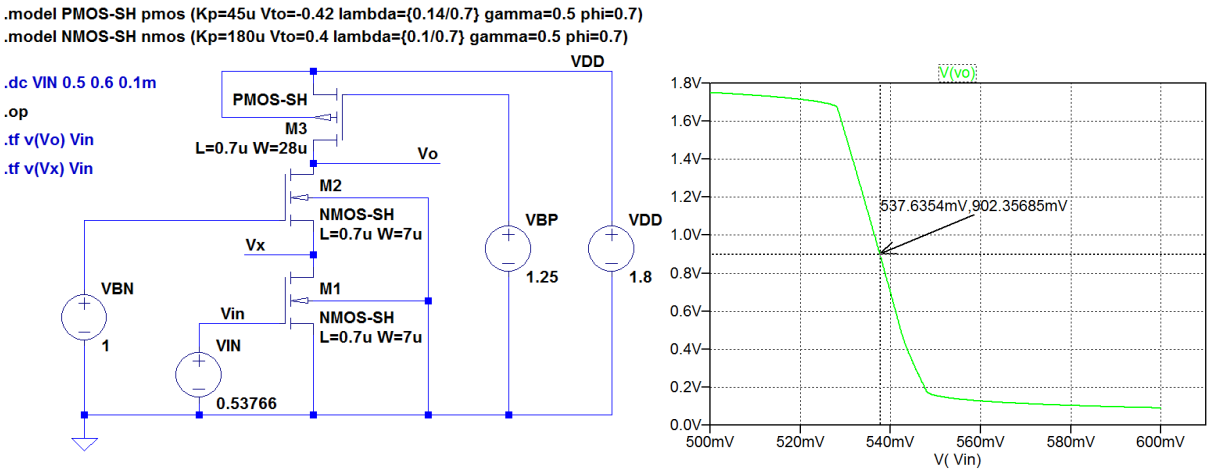
For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

The following figure shows an LTspice schematic corresponding to Problem 4.8. From the Shichman-Hodges model with $\lambda = 0$, we find that with $W_3/L_3 = 40$, the bias current for M_1, M_2 and M_3 is about $I_D \simeq \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(|V_{GS3}| - |V_{t3}|)^2 = \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(V_{DD} - V_{BP} - |V_{t3}|)^2 = 15.2\ \mu A$.

From the Shichman-Hodges model with $\lambda = 0$, we find that with $W_1/L_1 = 10$, the input bias voltage V_{IN} required for a bias current of 15 µA is about $V_{IN} \simeq V_t + \sqrt{\frac{2I_D}{\mu_n C_{ox}(W_1/L_1)}} = 529$ mV.

In order to find the exact value of the input bias voltage, we run a '.dc' simulation with V_{IN} swept from 500 mV to 600 mV, i.e., around the estimated value. The following figure shows the resulting plot of the output voltage. From this, we find $V_{IN} \simeq 537.6$ mV.

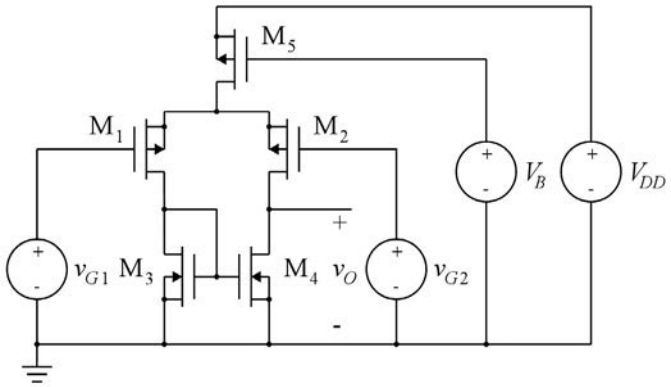


In order to verify the bias point, we run a '.op' simulation with a dc value of V_{IN} specified to 537.6 mV. From the output file, we find $V_O = 905$ mV. A few iterations show that with $V_{IN} = 537.66$ mV, the bias value of the output voltage is 900 mV.

With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a '.tf' simulation with '`V(Vo)`' as the output and '`Vin`' as the source. The output file from this '.tf' simulation shows a gain of -84.6 V/V ~ 38.5 dB and an output resistance of 327 kΩ.

For finding the small-signal resistance r_x to ground from the node X between the source of M_2 and the drain of M_1 and the small-signal gain from the input to node X, we run a '.tf' simulation with '`V(Vx)`' as the output and '`Vin`' as the source. From this, we find a resistance r_x of 5.33 kΩ and a gain of $A_{vx} = -1.39$ V/V ~ 2.9 dB.

Problem 4.9



The figure above shows a PMOS differential pair. For all transistors, assume $L = 1$ µm and $W = 20$ µm and transistor parameters as specified in Table 3.1. The supply voltage is $V_{DD} = 1.8$ V and the bias voltage V_B is $V_B = 1.1$ V.

Neglecting the channel-length modulation in M_5, calculate the bias current in each transistor, assuming all transistors to be in the active region.
Calculate the small-signal parameters g_m and r_{ds} for each transistor, using reasonable approximations and assuming all transistors to be in the active region.
Calculate the differential small-signal gain $A_d = v_o/(v_{g1} - v_{g2})$.
Check your results with LTspice and explain differences between simulated and calculated results.
Use LTspice to find the input common-mode voltage range where all transistors are in the active region.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

The bias current in M_5 is calculated using the Shichman-Hodges model with $\lambda = 0$, i.e.,

$$I_{D5} \simeq \frac{1}{2}\mu_p C_{ox}\frac{W_5}{L_5}(|V_{GS5}| - |V_{t5}|)^2 = \frac{1}{2}\mu_p C_{ox}\frac{W_5}{L_5}(V_{DD} - V_B - |V_{t5}|)^2 = 35.3\ \mu\text{A}.$$

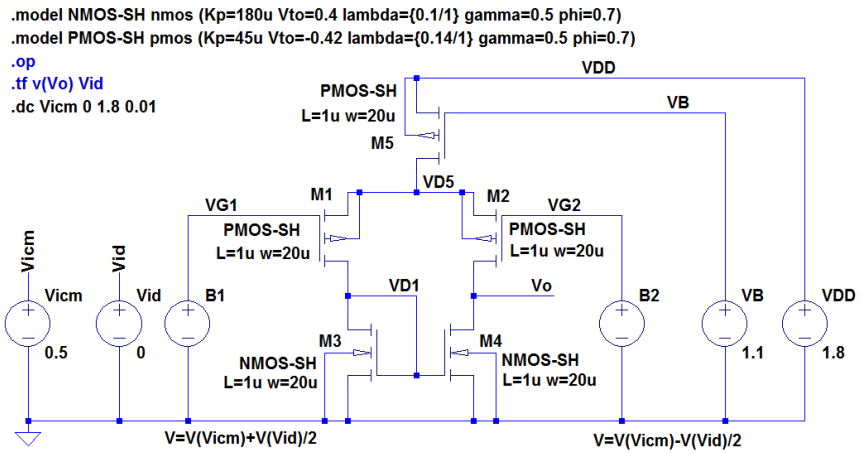
For the other transistors, we find $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2 = 17.6$ µA.

Using the approximations given by Eqs. (3.71) and (3.72) in Bruun (2022), we find, using $\lambda_1 = \lambda_2 = \lambda_5 = 0.14\ \text{V}^{-1}$ and $\lambda_3 = \lambda_4 = 0.1\ \text{V}^{-1}$

$$\begin{aligned}
g_{m1} = g_{m2} &\simeq \sqrt{2\,\mu_p C_{ox}(W/L)I_{D1}} = 178\ \mu\text{A/V} \\
g_{m3} = g_{m4} &\simeq \sqrt{2\,\mu_n C_{ox}(W/L)I_{D3}} = 356\ \mu\text{A/V} \\
g_{m5} &\simeq \sqrt{2\,\mu_p C_{ox}(W/L)I_{D5}} = 252\ \mu\text{A/V} \\
r_{ds1} = r_{ds2} &\simeq 1/(\lambda_1 I_{D1}) = 406\ \text{k}\Omega \\
r_{ds3} = r_{ds4} &\simeq 1/(\lambda_3 I_{D3}) = 568\ \text{k}\Omega \\
r_{ds5} &\simeq 1/(\lambda_5 I_{D5}) = 203\ \text{k}\Omega
\end{aligned}$$

From Eq. (4.71) in Bruun (2022), the differential small-signal gain is found as $A_d = g_{m1}(r_{ds2} \parallel r_{ds4}) = 42.1$ V/V.

The following figure shows the LTspice schematic corresponding to Problem 4.9. The input voltages are split into a differential input voltage and a common-mode input voltage with $v_{G1} = V_{ICM} + v_{id}/2$ and $v_{G1} = V_{ICM} - v_{id}/2$ where V_{ICM} is the common-mode input voltage and v_{id} is the differential (small-signal) input voltage. This is achieved by connecting an arbitrary behavioral voltage source to each of the two inputs as shown in the schematic.



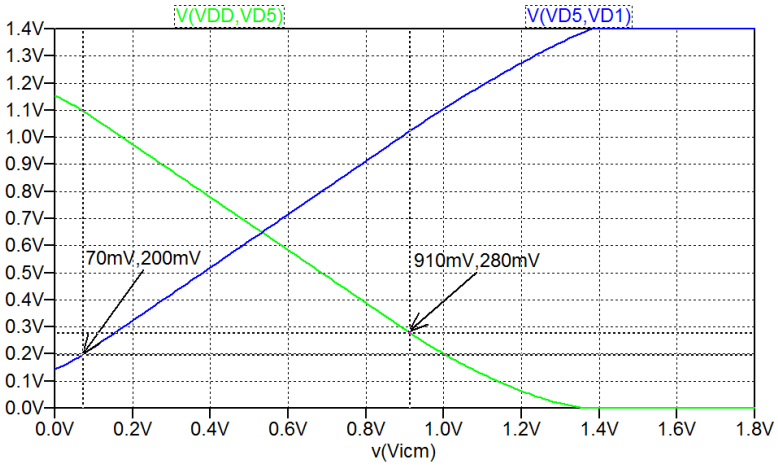
Running a '.op' simulation with $V_{ICM} = 0.5$ V, we find the bias currents $I_{D5} = 38.6$ µA and $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2 = 19.3$ µA and we notice that all transistors are in the active region. The small-signal parameters are found from the error log file, giving the following values:
$g_{m1} = g_{m2} = 194$ µA/V, $g_{m3} = g_{m4} = 382$ µA/V, $g_{m5} = 276$ µA/V,
$r_{ds1} = r_{ds2} = 402$ kΩ, $r_{ds3} = r_{ds4} = 543$ kΩ and $r_{ds5} = 202$ kΩ.

Running a '.tf' simulation with '`v(Vo)`' as the output and '`Vid`' as the input, we find a differential gain of 44.8 V/V.

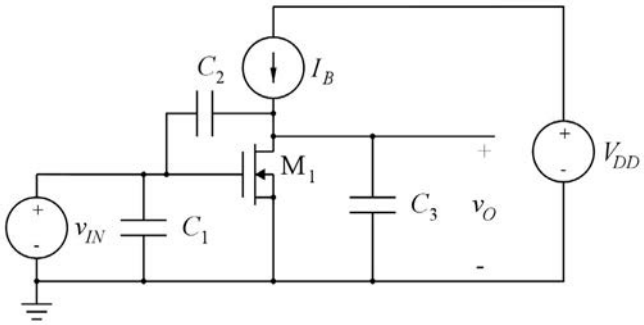
We notice that LTspice gives slightly larger values of bias currents and transconductances due to the channel-length modulation which has been neglected in the hand calculations. Also simulated r_{ds} values are slightly different due to the factor $(1 + \lambda V_{DS})$ and the larger values of I_D. The differences cause the simulated value of the small-signal gain to be slightly larger than the calculated value.

The input common-mode range is the voltage range for V_{ICM} where the differential stage has all transistors operating in the active region so that the small-signal gain is almost constant over this range of V_{ICM}. The upper limit is defined by M_5 which enters the triode region when V_{ICM} increases, implying that M_5 can no longer supply the required bias current to M_1 and M_2. The lower limit is defined by M_1 which will enter the triode region when V_{ICM} is so low that there is no longer headroom for the gate-source voltage of M_3. From the error log file from the '.op' simulation, we find $|V_{GS}| - |V_t| = |V_{DSsat}|$ to be 0.28 V for M_5 and 0.20 V for M_1. In order to check the voltage levels for the drain-source voltages of M_5 and M_1, we run a dc sweep from 0 V to 1.8 V with V_{ICM} as the source.

The following figure shows the plot of $|V_{DS5}|$ (green trace) and $|V_{DS1}|$ (blue trace), respectively. From this, we find a common-mode input range from about 0.07 V to about 0.91 V.



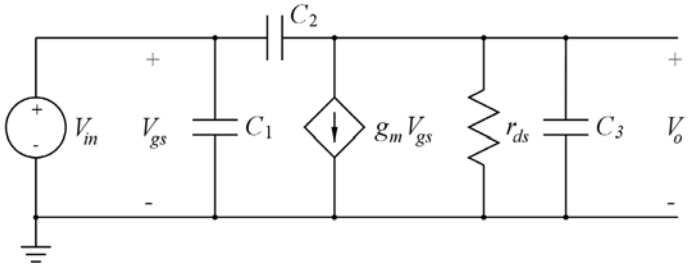
Problem 4.10



For the common-source stage shown above, we assume that the transistor has the small-signal parameters g_m and r_{ds} and that all transistor capacitances can be neglected compared to the capacitors C_1, C_2 and C_3. Draw a small-signal equivalent circuit for the stage and use a node equation to find the small-signal transfer function V_o/V_{in}. Find expressions for poles and zeros in the transfer function.

Solution:

The small-signal diagram is shown below.

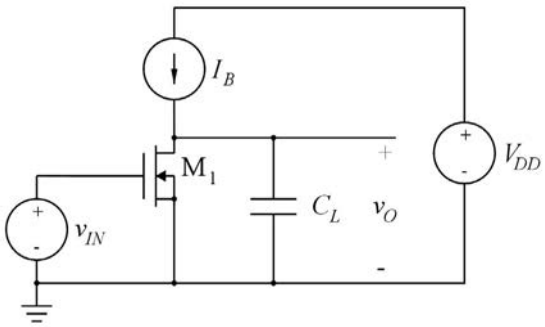


Using a node equation at the output node, we find

$$(V_{in}-V_o)\,sC_2 = g_m V_{in} + \frac{V_o}{r_{ds}} + V_o\,sC_3 \quad \Rightarrow \quad A_v(s) = \frac{V_o(s)}{V_{in}(s)} = -\frac{(g_m - sC_2)\,r_{ds}}{1+s\,(C_2+C_3)\,r_{ds}}$$

From the transfer function, we find the pole $p = -((C_2+C_3)\,r_{ds})^{-1}$ and the (right half-plane) zero $z = g_m/C_2$.

Problem 4.11



The figure above shows a common-source stage with a capacitive load $C_L = 5$ pF which is much larger than the transistor capacitances. The transistor is biased in the active region and it has the small-signal parameters $g_{m1} = 0.20$ mA/V and $r_{ds1} = 250$ kΩ.
Calculate the output resistance, the small-signal voltage gain at low frequencies, the -3 dB bandwidth and the gain-bandwidth product of the amplifier stage.

Problems 4.12 and 4.13 are follow-ups to this problem.

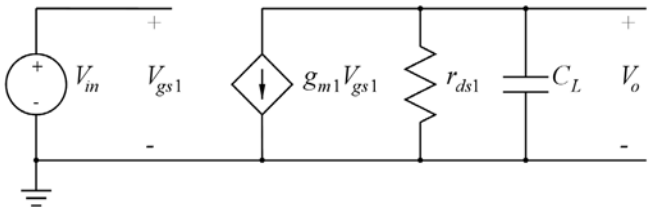
Solution:

The figure below shows a small-signal diagram corresponding to Problem 4.11. From this, we immediately see that the output resistance is $r_{out} = r_{ds1} = 250$ kΩ. Using a node equation at the output, we find

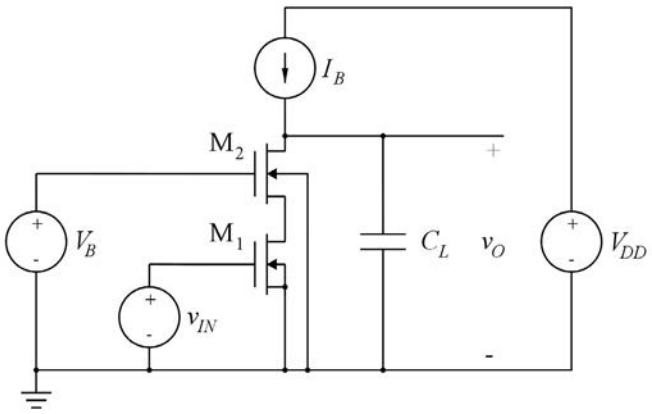
$$\frac{V_o(s)}{V_{in}(s)} = -g_{m1}\left(r_{ds1} \parallel \frac{1}{sC_L}\right) = \frac{-g_{m1}\, r_{ds1}}{1 + s\, r_{ds1}\, C_L}$$

From the transfer function, we find the low-frequency gain $A_v = -g_{m1}\, r_{ds1} = -50$ V/V and the -3 dB frequency $f_{\text{-3 dB}} = (2\pi\, r_{ds1} C_L)^{-1} = 127.3$ kHz.

The gain-bandwidth product is GBW $= |A_v|\, f_{\text{-3 dB}} = 6.37$ MHz.



Problem 4.12



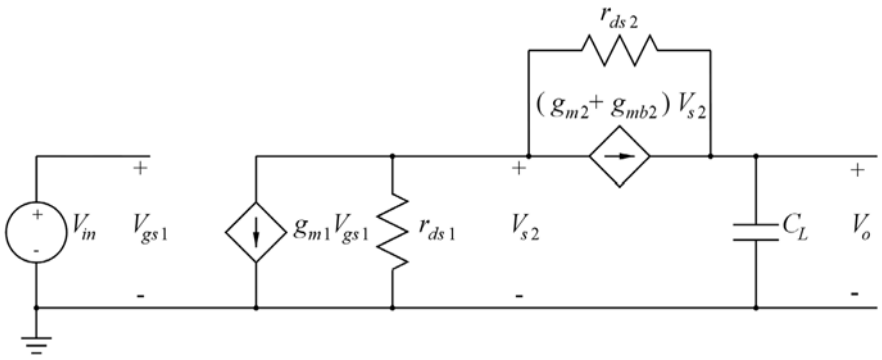
In order to increase the gain of the amplifier from Problem 4.11, a cascode transistor M_2 is inserted as shown above. The cascode transistor is assumed to be identical to M_1 and it has a bulk transconductance of $g_{mb2} = 0.04$ mA/V. Both M_1 and M_2 are biased in the active region with an unchanged bias current I_B.

Calculate the output resistance, the small-signal voltage gain at low frequencies, the -3 dB bandwidth and the gain-bandwidth product of the cascode amplifier.

Solution:

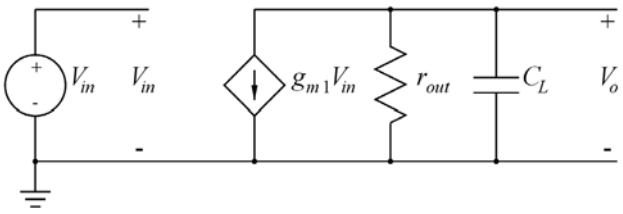
The figure below shows a small-signal diagram corresponding to Problem 4.12, compare to Fig. 4.24 in Bruun (2022). Using Eq. (4.27) from Bruun (2022), we find

$$r_{out} = r_{ds1} + (1 + (g_{m2} + g_{mb2})r_{ds1})\, r_{ds2} \simeq (g_{m2} + g_{mb2})r_{ds2}\, r_{ds1} = 15\ \text{M}\Omega$$



The small-signal model may be simplified to the following model, compare to Fig. 4.25 in Bruun (2022). From this, we find

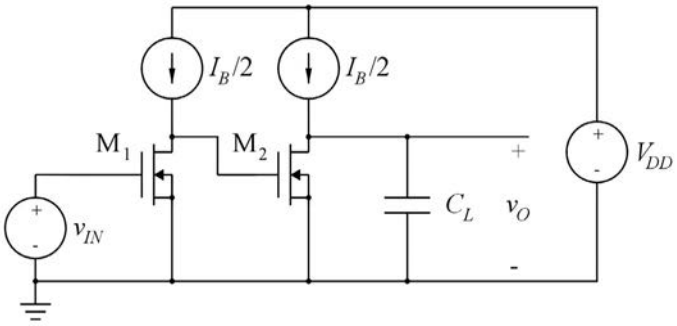
$$\frac{V_o(s)}{V_{in}(s)} = -g_{m1}\left(r_{out} \parallel \frac{1}{sC_L}\right) = \frac{-g_{m1}\, r_{out}}{1 + s\, r_{out} C_L}$$



From the transfer function, we find the low-frequency gain $A_v = -g_{m1}\, r_{out} = -3000$ V/V and the -3 dB frequency $f_{\text{-3 dB}} = (2\pi\, r_{out}\, C_L)^{-1} = 2.12$ kHz.

The gain-bandwidth product is GBW $= |A_v|\, f_{\text{-3 dB}} = 6.37$ MHz.

Problem 4.13



An alternative to the cascode amplifier from Problem 4.12 is a two-stage amplifier using common-source stages as shown above. The two transistors are assumed to be identical and identical to the transistors in Problems 4.11 and 4.12 and they are both biased in the active region, however with a bias current which is half of the bias current used in Problems 4.11 and 4.12. The reduction in bias current affects the small-signal parameters of the transistors.

Calculate the new values of g_m and r_{ds} using the Shichman-Hodges model with reasonable approximations.

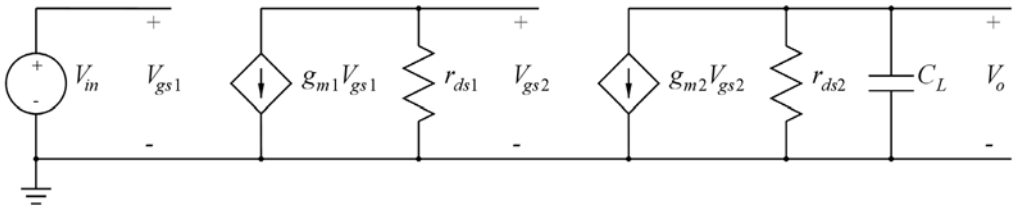
Calculate the output resistance, the small-signal voltage gain at low frequencies, the -3 dB bandwidth and the gain-bandwidth product of the two-stage common-source amplifier.

Solution:

The following figure shows a small-signal diagram for the two-stage amplifier. For the two-stage amplifier, the values of the small-signal parameters change because the bias current is reduced.

From $g_m \simeq \sqrt{2\,\mu_n C_{ox}(W/L)I_D}$, we see that when the current is multiplied by a factor of 0.5, the transconductance is multiplied by a factor of $\sqrt{0.5} = 0.707$, so the new value of the transconductance is $g_{m1} = g_{m2} = 0.141$ mA/V.

From $r_{ds} \simeq 1/(\lambda I_D)$, we see that when the current is multiplied by a factor of 0.5, the output resistance is multiplied by a factor of $1/0.5 = 2$, so the new value of the output resistance of the transistors is $r_{ds1} = r_{ds2} = 500\ \text{k}\Omega$.



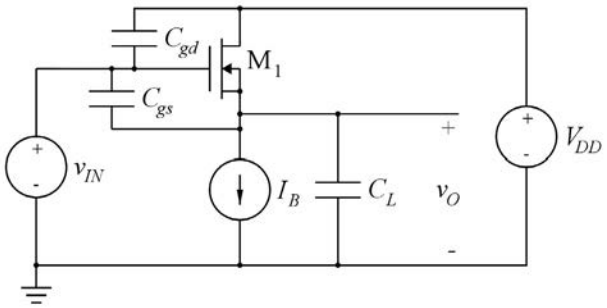
From the small-signal diagram, we immediately see that the output resistance is $r_{out} = r_{ds2} = 500\ \text{k}\Omega$. Using node equations at the outputs of stage 1 and stage 2, we find

$$\frac{V_o(s)}{V_{in}(s)} = (-g_{m1}\, r_{ds1}) \left(\frac{-g_{m2}\, r_{ds2}}{1 + s\, r_{ds2} C_L} \right)$$

From the transfer function, we find the low-frequency gain $A_v = g_{m1}\, r_{ds1}\, g_{m2}\, r_{ds2} = 5000$ V/V and the -3 dB frequency $f_{\text{-3 dB}} = (2\pi\, r_{ds2}\, C_L)^{-1} = 63.7$ kHz.

The gain-bandwidth product is $\text{GBW} = A_v\, f_{\text{-3 dB}} = 316$ MHz.

Problem 4.14

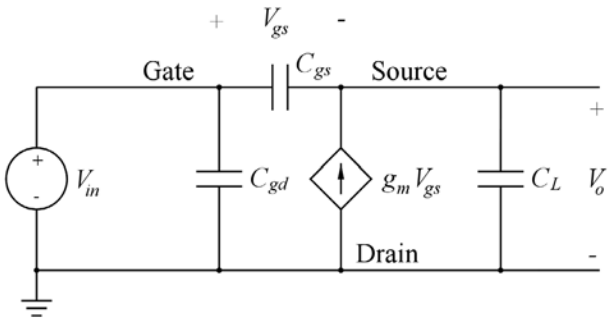


For the common-drain stage shown above, we assume that the transistor has the transconductance g_m and that the channel-length modulation and body effect can be neglected. Also, only the transistor capacitances shown in the figure above and the load capacitance C_L need to be considered.
Draw a small-signal equivalent circuit for the stage and use a node equation to find the small-signal transfer function V_o/V_{in}. Find expressions for poles and zeros in the transfer function.

Solution:

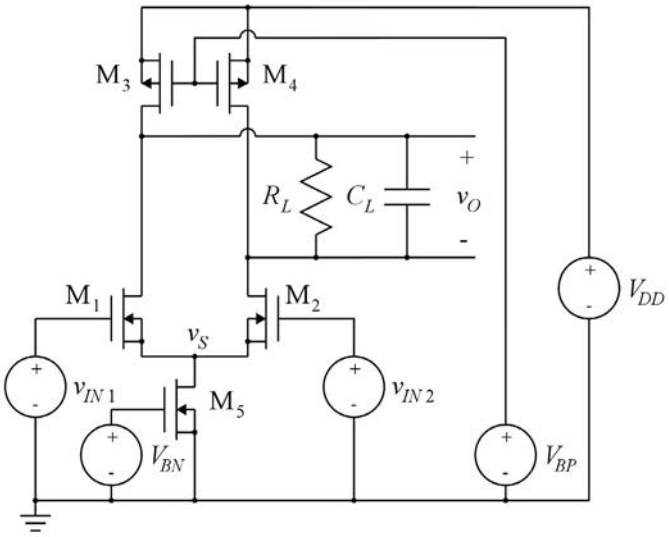
The small-signal diagram is shown in the following figure. Using $V_{gs} = V_{in} - V_o$, a node equation at the output gives

$$g_m V_{gs} = g_m(V_{in} - V_o) = V_o\, s C_L + (V_o - V_{in})\, s C_{gs} \quad \Rightarrow \quad \frac{V_o}{V_{in}} = \frac{g_m + s C_{gs}}{g_m + s(C_L + C_{gs})}$$



From the transfer function, we find the pole $p = -g_m/(C_L + C_{gs})$ and the zero $z = -g_m/C_{gs}$.

Problem 4.15



The figure above shows a differential pair with a differential output v_O. The load resistor R_L and capacitor C_L and the supply voltages have the following values: $R_L = 20$ kΩ, $C_L = 2$ pF, $V_{DD} = 1.8$ V, $V_{BN} = 0.7$ V and $V_{BP} = 1.08$ V.

All transistors have a channel length of 1 μm, are in the active region, and have transistor parameters as specified in Table 3.1, except the channel-length modulation can be neglected.

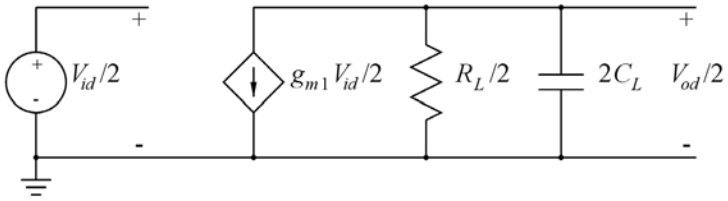
Draw a small-signal differential half-circuit for the differential pair and find the small-signal parameters such that a gain-bandwidth product of 25 MHz for the differential gain $V_o/(V_{in1} - V_{in2})$ is obtained. Calculate the low-frequency small-signal gain.

Find the required bias current for all transistors using an effective gate voltage of 0.3 V. Find the channel widths of all transistors.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

The figure below shows the small-signal differential half-circuit. The load resistor is split into two series-connected resistors, each with a value of $R_L/2$, i.e., one for each half-circuit. Likewise, the load capacitor is split into two series-connected capacitors, each with a value of $2C_L$, i.e., one for each half-circuit.



From the small-signal diagram, we find the transfer function $\frac{V_o}{V_{id}} = \frac{-g_{m1}R_L}{2(1+sR_LC_L)}$.

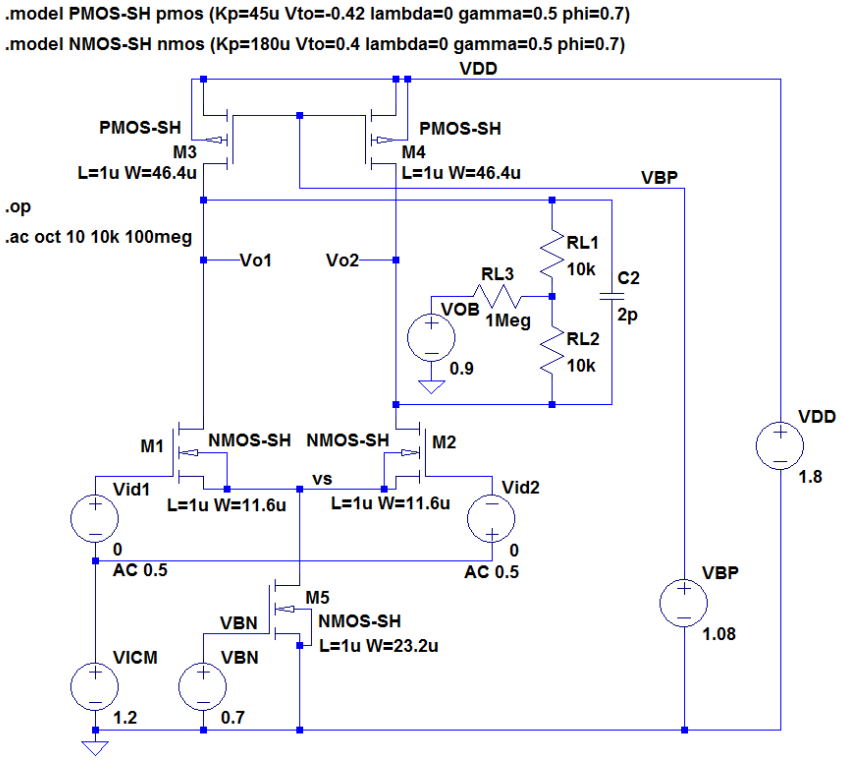
The low-frequency gain is $|A_0| = g_{m1}R_L/2$ and the -3 dB bandwidth is $f_{\text{-3 dB}} = (2\pi R_L C_L)^{-1}$, so the gain-bandwidth product is GBW $= g_{m1}/(4\pi C_L)$. For GBW $= 25$ MHz and $C_L = 2$ pF, we find $g_{m1} = 0.628$ mA/V and $A_0 = -6.28$ V/V ~ 15.95 dB.

With an effective gate voltage $V_{GS1} - V_{tn} = 0.3$ V, we find $I_{D1} = g_{m1}(V_{GS1} - V_{tn})/2 = 94$ µA. The other bias currents are $I_{D4} = I_{D3} = I_{D2} = I_{D1} = 94$ µA and $I_{D5} = 2I_{D1} = 188$ µA.

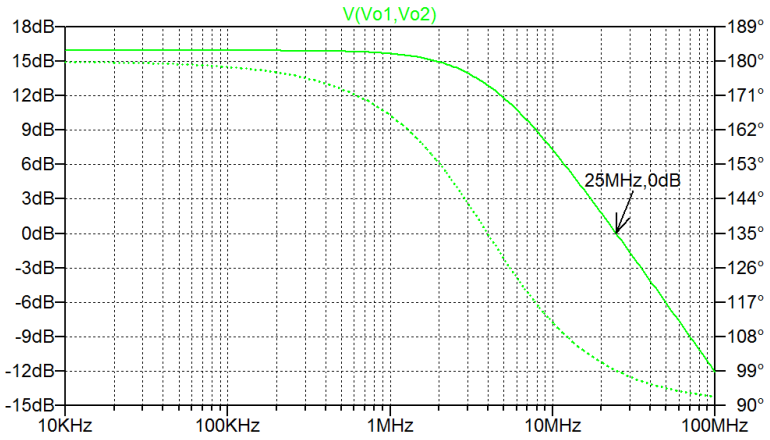
From the Shichman-Hodges transistor model, we find $W = L\frac{2I_D}{\mu C_{ox}(V_{GS} - V_t)^2}$.

Inserting the transistor parameters, we find $W_1 = W_2 = 11.6$ µm, $W_3 = W_4 = 46.4$ µm and $W_5 = 23.2$ µm.

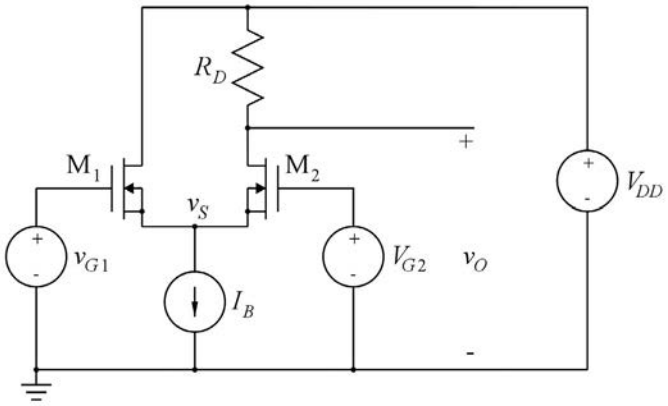
The results may be verified using LTspice. The following figure shows an LTspice schematic corresponding to Problem 4.15. Notice that the load resistor is split into two and there is an extra resistor connected to a common-mode output voltage 'VOB'. With $\lambda = 0$, the transistors have infinite output resistance, so the output nodes are left floating unless a dc path to a common-mode output voltage is established. The value of the extra resistor is so large that it does not affect the small-signal frequency response. The output common-mode voltage has been selected to 0.9 V and the common-mode input voltage has been selected to 1.2 V in order to ensure that all transistors are in the active region.



The bias current values may be verified from a '.op' simulation and the gain-bandwidth product may be verified from a '.ac' simulation. The figure below shows the plot from the '.ac' simulation and GBW is found as the unity-gain frequency.



Problem 4.16



The circuit shown above with the gate of M_2 connected to a dc bias voltage V_{G2} can be used as an amplifier with a single-ended input $v_{IN} = v_{G1}$ and a single-ended output v_O.

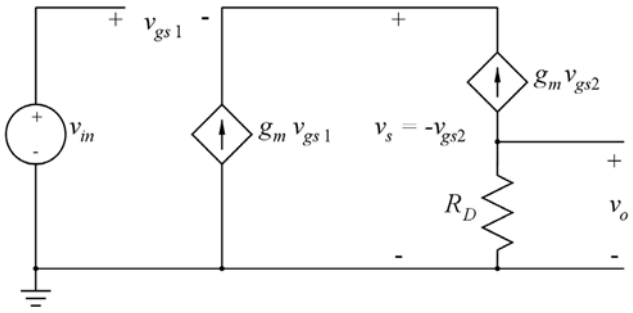
Neglect the channel-length modulation and assume that both transistors are in the active region and have a transconductance of g_m.

Find an expression for the low-frequency small-signal gain v_o/v_{in} and the low-frequency small-signal gain v_s/v_{in} where v_S is the source voltage of M_1.

Find an expression for the input capacitance of the amplifier, assuming that the only capacitances to be considered are C_{gs} and C_{gd} for the transistors.

Solution:

The figure below shows a small-signal diagram corresponding to Problem 4.16. In the small-signal diagram, we have $v_{gs1} = v_{in} - v_s$ and $v_{gs2} = 0 - v_s = -v_s$.



A node equation at v_s gives

$$g_m v_{gs1} + g_m v_{gs2} = 0 \;\Rightarrow\; v_{gs1} + v_{gs2} = 0 \Rightarrow v_{in} - v_s - v_s = 0 \;\Rightarrow\; v_s = v_{in}/2 \;\Rightarrow\; v_s/v_{in} = 1/2$$

A node equation at the output gives

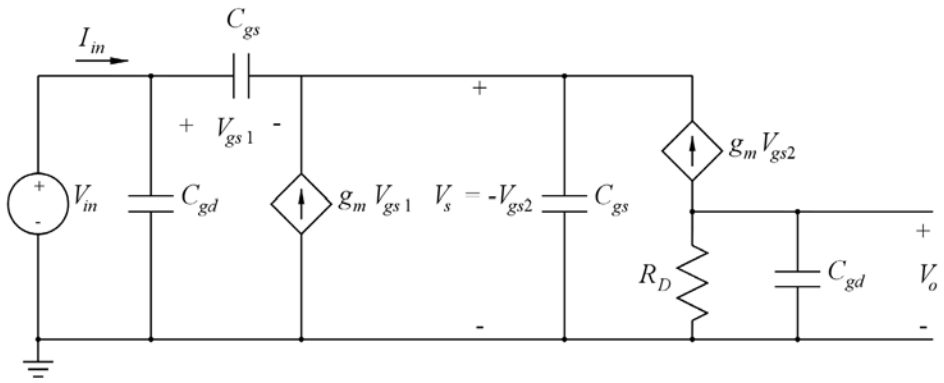
$$v_o/R_D + g_m v_{gs2} = 0 \;\Rightarrow\; v_o = -R_D g_m v_{gs2} = R_D g_m v_s = R_D g_m v_{in}/2 \;\Rightarrow\; v_o/v_{in} = R_D g_m/2$$

In order to find the input capacitance C_{in}, we draw the following small-signal diagram including the capacitors C_{gs} and C_{gd}. With a capacitive input, the relation between input voltage and input current is $I_{in}(s) = sC_{in}V_{in}(s)$. From the small-signal diagram, we find $I_{in}(s) = sC_{gd}V_{in}(s) + sC_{gs}(V_{in}(s) - V_s(s))$.

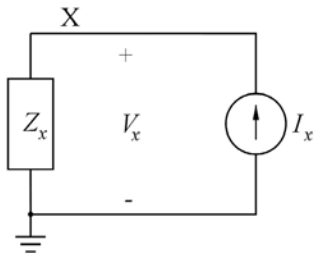
In order to find $V_s(s)$, we use a node equation at V_s:

$$(V_{in}(s) - V_s(s))sC_{gs} + g_m(V_{in}(s) - V_s(s)) = sC_{gs}V_s(s) + g_m V_s(s) \Rightarrow V_s(s) = V_{in}(s)/2$$

Hence, $I_{in}(s) = sC_{gd}V_{in}(s) + sC_{gs}(V_{in}(s) - V_s(s)) = s(C_{gd} + C_{gs}/2)V_{in}(s)$, so $C_{in} = C_{gd} + C_{gs}/2$.



Problem 4.17



The small-signal impedance to ground from a node X can be found by applying an ac current I_x to the node and measuring the voltage V_x while all other independent sources in the circuit are reset, see the

The small-signal impedance to ground from a node X can be found by applying an ac current I_x to the node and measuring the voltage V_x while all other independent sources in the circuit are reset, see the figure above. If Z_x can be approximated by a parallel combination of a resistor R_x and a capacitor C_x, R_x and C_x can be found from $R_x = |V_x|^2/(I_x \mathrm{Re}\,(V_x))$ and $C_x = -(I_x \mathrm{Im}\,(V_x))/(2\pi f\,|V_x|^2)$ where f is the frequency (Bruun 2020, Tutorial 2.6).

With the ac value of I_x defined to be 1 and the dc value defined to be 0 in LTspice, we can find R_x and C_x from a plot of the expressions `Rx=Abs(v(Vx))**2/Re(v(Vx))` and `Cx=-Im(v(Vx))/(2*pi*frequency*Abs(v(Vx))**2)` after having run a '.ac' simulation over a suitable frequency range.

Use this method to find the output resistance and output capacitance of the common-source stage shown in Fig. 4.72 with $C_f = 0$ and $R_S = 0$. Insert a decoupling capacitor in parallel with R_B to ensure that V_B can be treated as a dc voltage for the frequencies of interest. Compare to the values found using the small-signal parameters from a '.op' simulation.

Repeat for the cascode stages shown in Fig. 4.81 with $R_S = 0$.

Solution:

Common-source stage:

For convenience, Figs. 4.72 and 4.73 from Bruun (2022) are shown in the following.

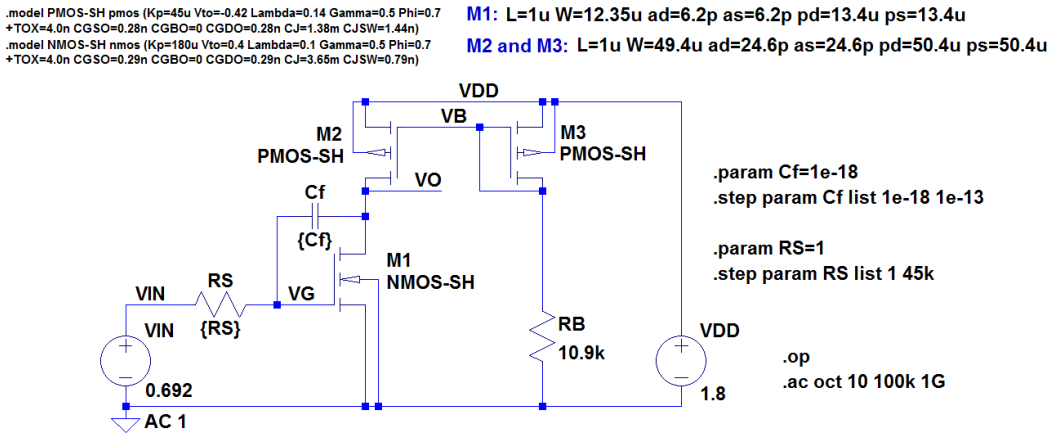


Figure 4.72: LTspice schematic for simulating the frequency response of a common-source stage with an active load.

Error log file

```
Semiconductor Device Operating Points:
                  --- MOSFET Transistors ---
Name:           m3           m2           m1
Model:       pmos-sh      pmos-sh      nmos-sh
Id:       -1.00e-04    -1.03e-04     1.03e-04
Vgs:      -7.07e-01    -7.07e-01     6.92e-01
Vds:      -7.07e-01    -9.23e-01     8.77e-01
Vbs:       0.00e+00     0.00e+00     0.00e+00
Vth:      -4.20e-01    -4.20e-01     4.00e-01
Vdsat:    -2.87e-01    -2.87e-01     2.92e-01
Gm:        7.00e-04     7.19e-04     7.06e-04
Gds:       1.28e-05     1.28e-05     9.48e-06
Gmb:       2.09e-04     2.15e-04     2.11e-04
Cbd:       7.77e-14     7.27e-14     2.29e-14
Cbs:       1.07e-13     1.07e-13     3.32e-14
Cgsov:     1.38e-14     1.38e-14     3.58e-15
Cgdov:     1.38e-14     1.38e-14     3.58e-15
Cgbov:     0.00e+00     0.00e+00     0.00e+00
Cgs:       2.84e-13     2.84e-13     7.11e-14
Cgd:       0.00e+00     0.00e+00     0.00e+00
Cgb:       0.00e+00     0.00e+00     0.00e+00
```

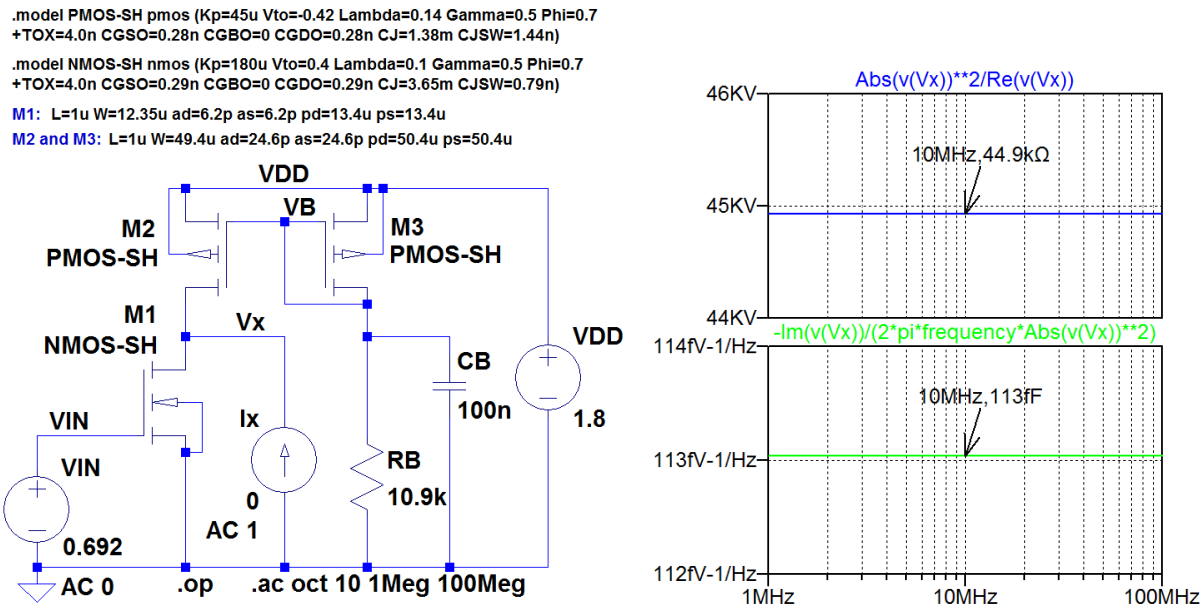
Figure 4.73: Results from the error log file from a '.op' simulation of the gain stage shown in Fig. 4.72.

Using the small-signal parameters from Fig. 4.73, we can calculate r_{out} and C_{out}:

$$\begin{aligned} r_{out} &= (g_{ds1}+g_{ds2})^{-1} = 44.9\ \text{k}\Omega \\ C_{out} &= C_{gd1}+C_{gdov1}+C_{bd1}+C_{gd2}+C_{gdov2}+C_{bd2} = 0.113\ \text{pF} \end{aligned}$$

From the calculated values of r_{out} and C_{out}, we find a time constant $\tau_{out} = r_{out}C_{out} \simeq 5$ ns so when simulating r_{out} and C_{out}, we select a frequency range around $1/(2\pi\tau_{out}) \simeq 30$ MHz, for instance a range from 1 MHz to 100 MHz. In order to ensure that V_B can be treated as a dc voltage in this frequency range, we insert a decoupling capacitor C_B in parallel with R_B of 100 nF, giving a time constant for the node V_B of $\tau_B \simeq C_B(R_B \parallel (1/g_{m3})) \simeq 126$ µs, corresponding to a frequency of about 1.2 kHz, i.e., much lower than the frequency range of interest.

Shown below is Fig. 4.72 modified with a current source '`Ix`' connected to the output and a decoupling capacitor connected in parallel with R_B. Also, the ac value of the input voltage '`VIN`' is reset and C_f and R_S are removed. The result of a '.ac' simulation is shown and from the simulation, we find $r_{out} = 44.9$ kΩ and $C_{out} = 0.113$ pF, exactly matching the values calculated from the small-signal parameters.



Cascode stages:

For convenience, Fig. 4.81 from Bruun (2022) is shown in the following and also a table with the small-signal parameters from the error log file from a '.op' simulation is shown.

Results from Error log file

Semiconductor Device Operating Points:

--- MOSFET Transistors ---

Name:	m3	m8	m5	m4	m7	m6	m2	m1
Model:	pmos-sh	pmos-sh	pmos-sh	pmos-sh	nmos-sh	nmos-sh	nmos-sh	nmos-sh
Id:	-9.63e-05	-1.02e-04	-1.00e-04	-9.63e-05	1.02e-04	1.02e-04	9.63e-05	9.63e-05
Vgs:	-7.90e-01	-7.10e-01	-7.10e-01	-7.10e-01	7.81e-01	6.98e-01	7.74e-01	6.90e-01
Vds:	-5.79e-01	-9.01e-01	-7.10e-01	-3.10e-01	5.80e-01	3.19e-01	5.85e-01	3.26e-01
Vbs:	3.10e-01	0.00e+00	0.00e+00	0.00e+00	-3.19e-01	0.00e+00	-3.26e-01	0.00e+00
Vth:	-5.04e-01	-4.20e-01	-4.20e-01	-4.20e-01	4.86e-01	4.00e-01	4.88e-01	4.00e-01
Vdsat:	-2.86e-01	-2.90e-01	-2.90e-01	-2.90e-01	2.94e-01	2.98e-01	2.86e-01	2.90e-01
Gm:	6.73e-04	7.02e-04	6.90e-04	6.64e-04	6.92e-04	6.83e-04	6.73e-04	6.65e-04
Gds:	9.10e-06	9.34e-06	9.34e-06	9.34e-06	9.62e-06	9.86e-06	9.10e-06	9.32e-06
Gmb:	1.67e-04	2.10e-04	2.06e-04	1.99e-04	1.71e-04	2.04e-04	1.66e-04	1.99e-04
Cbd:	1.02e-13	1.02e-13	1.08e-13	1.26e-13	2.28e-14	2.81e-14	2.27e-14	2.80e-14
Cbs:	1.26e-13	1.49e-13	1.49e-13	1.49e-13	2.81e-14	3.32e-14	2.80e-14	3.32e-14
Cgsov:	1.94e-14	1.94e-14	1.94e-14	1.94e-14	3.58e-15	3.58e-15	3.58e-15	3.58e-15
Cgdov:	1.94e-14	1.94e-14	1.94e-14	1.94e-14	3.58e-15	3.58e-15	3.58e-15	3.58e-15
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgs:	5.57e-13	5.57e-13	5.57e-13	5.57e-13	7.11e-14	7.11e-14	7.11e-14	7.11e-14
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

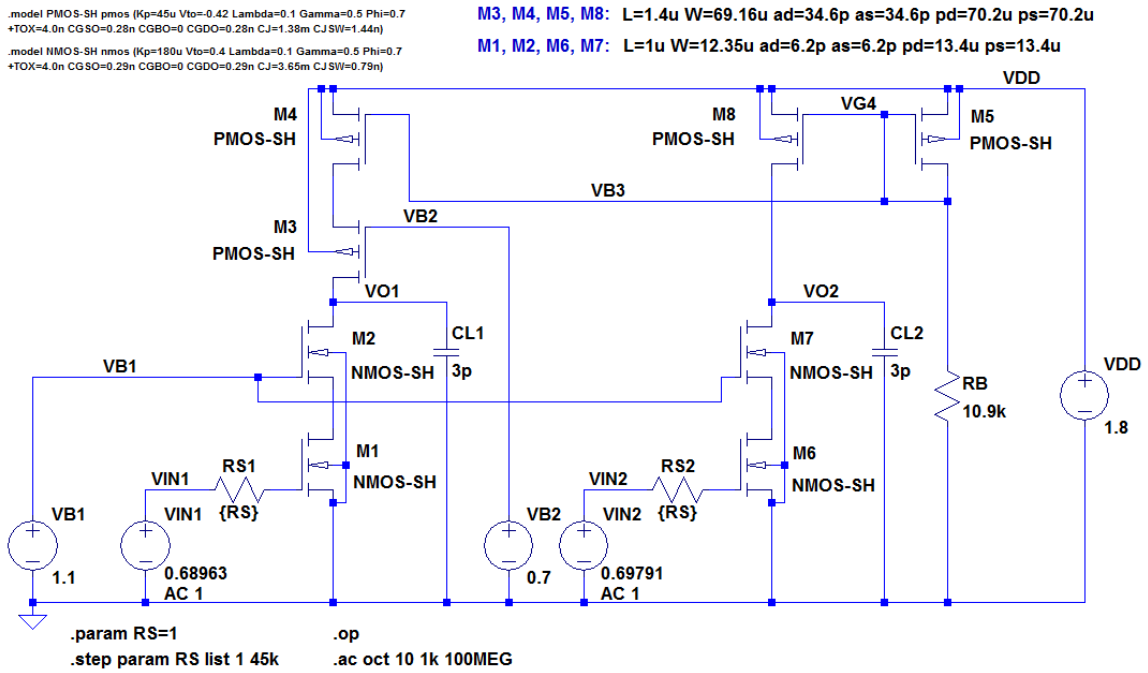


Figure 4.81: LTspice schematic for simulating the frequency response of cascode stages with different bias current sources.

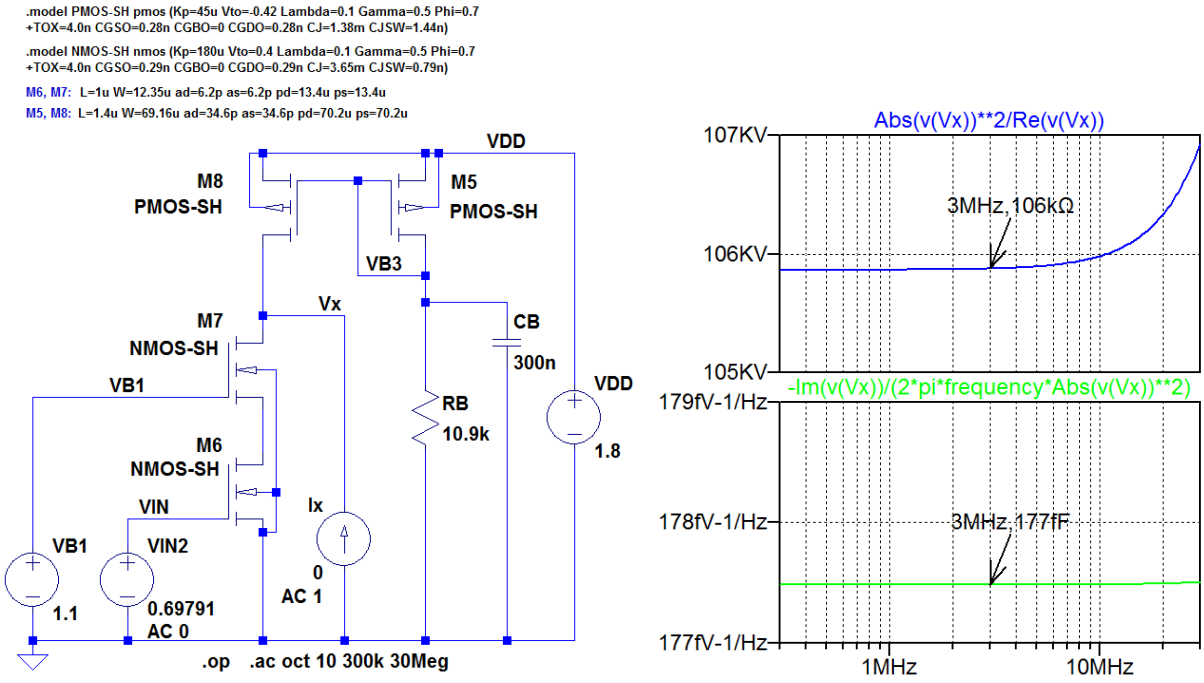
Low-gain cascode:

Using the small-signal parameters from the error log file, we can calculate r_{out} from Eq. (4.27) in Bruun (2022):

$$r_{out} \simeq \left(\left(g_{m7} + g_{mb7}\right) r_{ds7}\, r_{ds6}\right) \parallel \left(r_{ds8}\right) = 106\ \text{k}\Omega$$

The output capacitance is not so easy to calculate. It includes the contribution from $C_{gd7} + C_{gdov7} + C_{bd7} + C_{gd8} + C_{gdov8} + C_{bd8} = 0.148$ pF but also a term from the capacitance from the node connecting drain of M_6 and source of M_7 contributes to the output capacitance. This capacitance is $C_{gd6} + C_{gdov6} + C_{bd6} + C_{gs7} + C_{gsov7} + C_{bs7} = 0.134$ pF. However, since the impedance level at this node is multiplied by $(g_{m7} + g_{mb7})/g_{ds7} \simeq 90$ (compare to Eq. (4.25) in Bruun (2022)), the capacitance from this node is divided by a factor of 90, resulting in a total calculated output capacitance of $C_{out} \simeq 0.15$ pF. Thus, we find that the time constant from the output node is about a factor of 3 larger than the time constant for the common-source stage, so we may change the frequency interval for the simulation by a factor of 3 and the decoupling capacitor C_B by a factor of 3.

The following figure shows the LTspice schematic for simulating r_{out} and C_{out}. From the simulation, we find $r_{out} = 106$ kΩ and $C_{out} = 0.177$ pF. We notice that the simulated value of the output resistance matches the calculated value and that the output capacitance is somewhat larger than the value calculated above. This is due to the difference between the simple capacitor modeling used for the hand calculations and the advanced capacitor modeling used in LTspice (Bruun 2022). It shows that the hand calculations can only be considered as a rough approximation.



High-gain cascode:

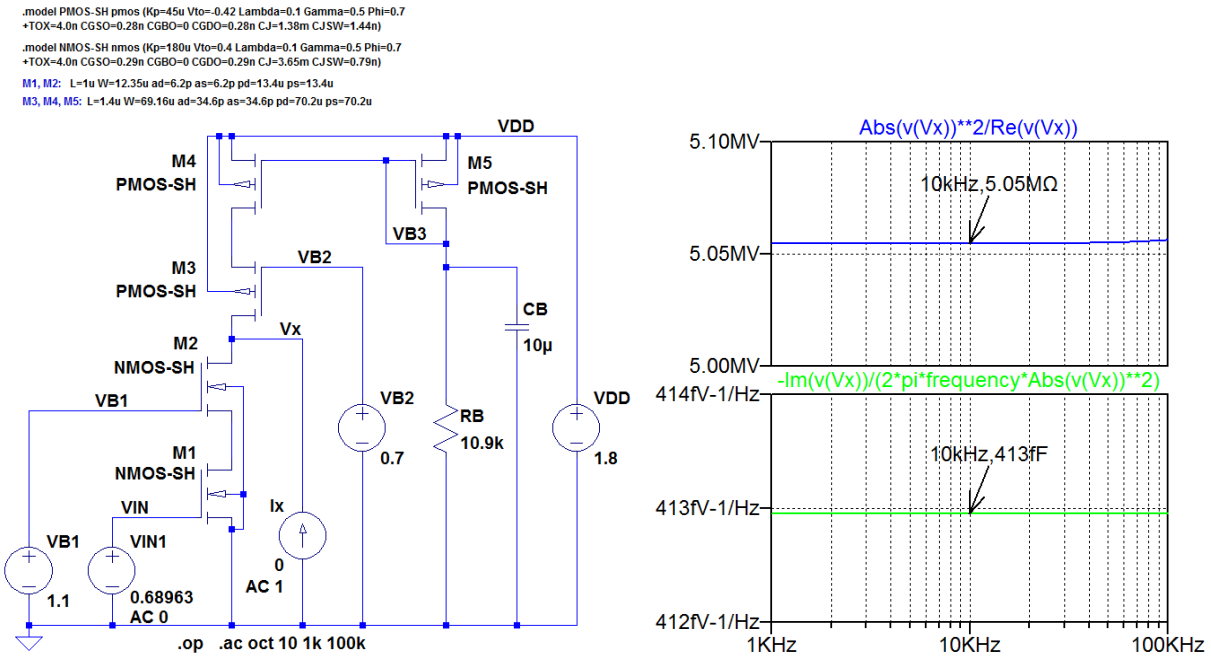
Using the small-signal parameters from error log file, we can calculate r_{out} from Eq. (4.27) in Bruun (2022):

$$r_{out} \simeq ((g_{m2} + g_{mb2})\, r_{ds2}\, r_{ds1}) \parallel ((g_{m3} + g_{mb3})\, r_{ds3}\, r_{ds4}) \simeq 5.0 \text{ MΩ}$$

Again, the output capacitance is not so easy to calculate. It includes the contribution from $C_{gd2} + C_{gdov2} + C_{bd2} + C_{gd3} + C_{gdov3} + C_{bd3} = 0.148$ pF but also terms from the capacitance from the node connecting drain of M_1 and source of M_2 and drain of M_4 and source of M_3 contribute to the output capacitance. From the node connecting drain of M_1 and source of M_2, we find $C_{gd1} + C_{gdov1} + C_{bd1} + C_{gs2} + C_{gsov2} + C_{bs2} = 0.134$ pF. From the node connecting drain of M_4 and source of M_3, we find $C_{gd4} + C_{gdov4} + C_{bd4} + C_{gs3} + C_{gsov3} + C_{bs3} = 0.848$ pF. As for the low-gain cascode, these capacitances are divided by the gains of M_2 and M_3, $A_{M_2} \simeq (g_{m2} + g_{mb2})/g_{ds2} \simeq 92$ and $A_{M_3} \simeq (g_{m3} + g_{mb3})/g_{ds3} \simeq 92$, respectively, so their contribution to the output capacitance is small, about 10 fF, resulting in a total calculated output capacitance of $C_{out} \simeq 0.16$ pF.

Thus, we find that the time constant from the output node is about two orders of magnitude larger than the time constant for the common-source stage, so we may change the frequency interval for the simulation by a factor of 100 and the decoupling capacitor C_B by a factor of 100.

The following figure shows the LTspice schematic for simulating r_{out} and C_{out}. From the simulation, we find $r_{out} = 5.05$ MΩ and $C_{out} = 0.413$ pF. We notice that the simulated value of the output resistance matches the calculated value and that the output capacitance is somewhat larger than the value calculated from the small-signal parameters. This is due to the difference between the simple capacitor modeling used for the hand calculations and the advanced capacitor modeling used in LTspice (Bruun 2022). It shows that the hand calculations can only be considered as a rough approximation.



References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Bruun, E. 2020, *CMOS Integrated Circuit Simulation with LTspice*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-integrated-circuit-simulation-with-ltspice-ebook

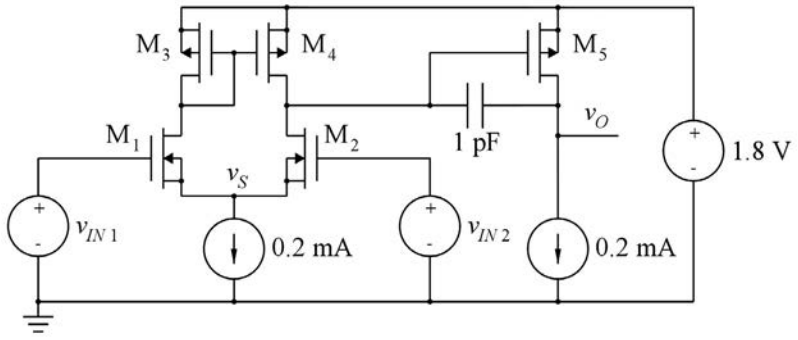
Chapter 5 – Multistage Amplifiers

Multiple-choice test

1. Completed statements:

A-5:	The input stage in a CMOS opamp is normally a differential pair.
B-2:	The second stage in a two-stage opamp is normally a common-source stage.
C-6:	For a folded-cascode opamp with a differential pair using NMOS input transistors, the folded-cascode transistors are PMOS transistors.
D-11:	The dominant pole in a folded-cascode opamp normally comes from the output node.
E-7:	For a two-stage opamp with a differential pair as the input stage and a common-source stage with a PMOS transistor for providing gain, the input transistors are NMOS transistors.
F-14:	For an opamp with a differential pair using PMOS input transistors, the maximum common-mode input voltage is less than the positive supply voltage by approximately $\|V_{GS}\| + \|V_{\text{eff}}\|$.
G-18:	The dominant pole in a two-stage opamp normally comes from the input to the second stage.
H-3:	In order to obtain a small output resistance from a CMOS opamp, an output buffer may be added. It should be configured as a common-drain stage.
I-12:	The frequency of the dominant pole in a two-stage opamp may be reduced by inserting a capacitor between gate and drain of the common-source stage.
J-20:	A circuit using an opamp with feedback may show instability if the feedback signal is inverted with respect to the input signal.

2. For the two-stage opamp shown below, assume that all transistors are in the active region and have a channel-length modulation parameter $\lambda = 0.1\ \text{V}^{-1}$ and an effective gate voltage $|V_{\text{eff}}| = 0.3$ V.



The channel-width-to-length ratio W_5/L_5 is equal to

A: $0.5 \times W_4/L_4$

B: $1.0 \times W_4/L_4$

C: $2.0 \times W_4/L_4$

Solution:

The drain current of M_4 is 0.1 mA which is half the drain current of M_5, so with the same effective gate voltage for M_4 and and M_5, the channel-width-to-length ratio of M_5 is twice the channel-width-to-length ratio of M_4, i.e., $W_5/L_5 = 2.0 \times W_4/L_4$.

3. The small-signal low-frequency output resistance of the opamp shown above is approximately

   A: 50 kΩ
   B: 100 kΩ
   C: 200 kΩ

Solution:

The small-signal low-frequency output resistance is $r_{out} = r_{ds5} \simeq 1/(\lambda I_{D5}) = 50$ kΩ.

4. The small-signal low-frequency differential gain of the opamp shown above is approximately

   A: 61 dB
   B: 67 dB
   C: 73 dB

Solution:

The small-signal low-frequency gain is

$$\begin{aligned} A_d &\simeq g_{m2}(r_{ds2} \parallel r_{ds4}) g_{m5} r_{ds5} \\ &\simeq (2I_{D2}/V_{\text{eff}})(1/(\lambda I_{D2} + \lambda I_{D4}))(2I_{D5}/V_{\text{eff}})(1/(\lambda I_{D5})) \\ &= (2/V_{\text{eff}})(1/(2\lambda))(2/V_{\text{eff}})(1/\lambda) = 2/(V_{\text{eff}}\lambda)^2 = 2222 \text{ V/V} \sim 67 \text{ dB}. \end{aligned}$$

5. Assuming that all transistor capacitances are much smaller than 1 pF, the frequency of the dominant pole in the opamp shown above is approximately

   A: 47 kHz
   B: 295 kHz
   C: 3.18 MHz

Solution:

The dominant pole is caused by the capacitor $C_c = 1$ pF connected between gate and drain of M_5. Using the Miller theorem, we find the pole frequency as

$$\begin{aligned} f_p &\simeq \frac{1}{2\pi (r_{ds2} \parallel r_{ds4}) C_c (1 + g_{m5} r_{ds5})} \\ &\simeq \frac{1}{2\pi (1/(2\lambda I_{D2})) C_c (1 + 2/(\lambda V_{\text{eff}}))} = 47 \text{ kHz} \end{aligned}$$

6. Assuming that all zeros and non-dominant poles are at frequencies above 1 GHz, the unity-gain frequency of the opamp shown above is approximately

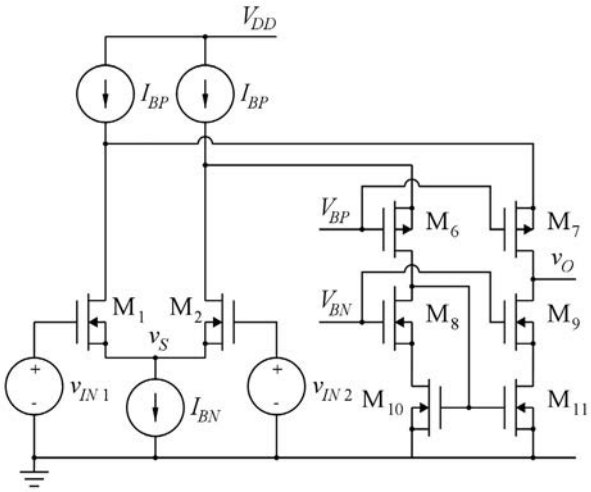
   A: 31.8 MHz
   B: 104 MHz
   C: 654 MHz

Solution:

With all zeros and non-dominant poles at frequencies much higher than the gain-bandwidth product, the unity-gain frequency is approximately equal to the gain-bandwidth product GBW $= A_d\, f_p \simeq 104$ MHz.

Problems

Problem 5.1



For the folded-cascode opamp shown above, assume that all transistors have a channel length $L = 1$ µm and a channel width $W = 20$ µm. Assume transistor parameters as specified in Table 3.1. The bias currents are $I_{BP} = 0.3$ mA and $I_{BN} = 0.4$ mA. Assume that the bias voltages V_{BP} and V_{BN} and the common-mode input bias voltage have values ensuring that all transistors are in the active region.
Calculate the low-frequency small-signal differential gain and the -3 dB bandwidth for a load capacitance of $C_L = 1.5$ pF which is much larger than the parasitic transistor capacitances. Use reasonable approximations when calculating small-signal parameters.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

The low-frequency small-signal gain A_d is found from $A_d = g_{m1}\, r_{out} = g_{m1}/g_{out}$ where r_{out} is found from Eq. (5.4) in Bruun (2022). The -3 dB frequency is found from $f_{\text{-3 dB}} = 1/(2\,\pi\, r_{out}\, C_L) = g_{out}/(2\,\pi C_L)$. Since M_3 and M_4 in Fig. 5.3 in Bruun (2022) are replaced by ideal current sources I_{BP}, we may use Eq. (5.4) with $r_{ds3} = \infty$ to find r_{out}:

$$r_{out} \simeq (g_{m9}\, r_{ds9}\, r_{ds11}) \parallel (g_{m7}\, r_{ds7}\, r_{ds1}) \;\Rightarrow\; g_{out} = \frac{1}{r_{out}} = \frac{g_{ds9}\, g_{ds11}}{g_{m9}} + \frac{g_{ds7}\, g_{ds1}}{g_{m7}}$$

The small-signal parameters are found using the approximations given by Eqs. (3.71) and (3.72) in Bruun (2022):

$$\begin{aligned} g_m &\simeq \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_D} \\ g_{ds} &\simeq \lambda I_D \end{aligned}$$

From the transistor parameters and dimensions, we find $W/L = 20$, $\mu_n C_{ox} = 180\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 45\ \mu\text{A/V}^2$, $\lambda_n = 0.10\ \text{V}^{-1}$ and $\lambda_p = 0.14\ \text{V}^{-1}$.

For transistors M_1 and M_2, we have $I_D = I_{BN}/2 = 200$ µA. For transistors M_7, M_9 and M_{11}, we have $I_D = I_{BP} - I_{BN}/2 = 100$ µA.

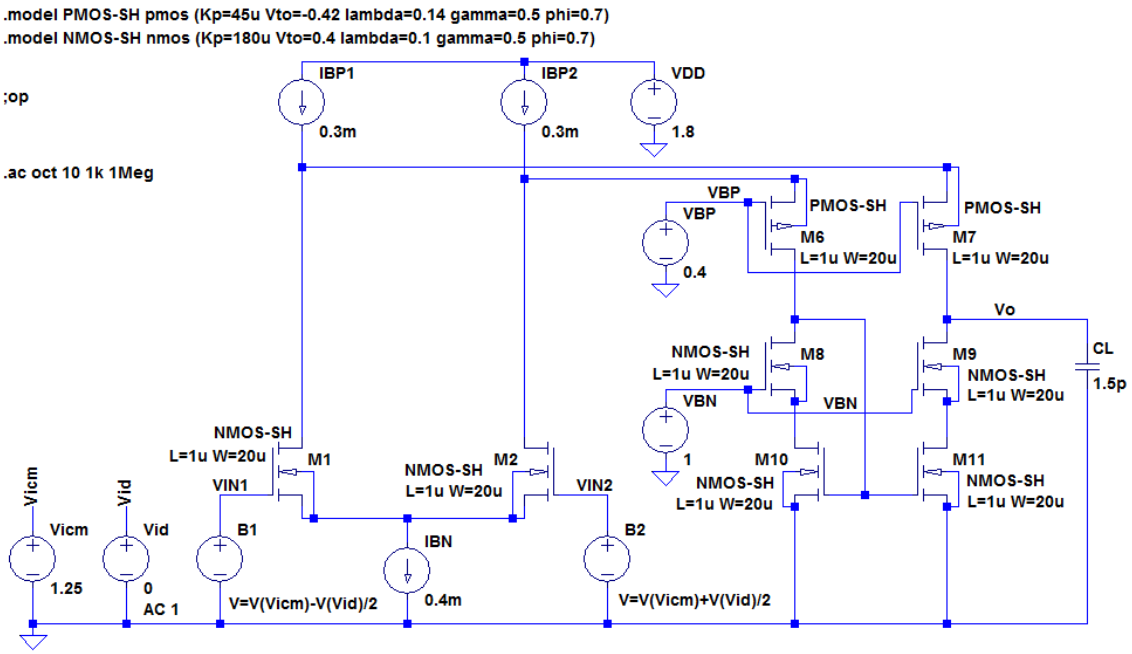
Inserting the numerical values, we find $g_{m1} \simeq 1.2$ mA/V, $g_{m7} \simeq 424$ µA/V, $g_{m9} \simeq 849$ µA/V, $g_{ds1} \simeq 20$ µA/V, $g_{ds7} \simeq 14$ µA/V and $g_{ds9} = g_{ds11} \simeq 10$ µA/V.

Using these values to calculate r_{out}, we find $r_{out} \simeq 1.29$ MΩ, giving a low-frequency small-signal gain $A_d \simeq 1540$ V/V ~ 63.8 dB. With $C_L = 1.5$ pF, we find the -3 dB bandwidth to be $f_{\text{-3 dB}} \simeq 82$ kHz.

We may use LTspice to analyze the circuit. The following figure shows an LTspice schematic corresponding to Problem 5.1. In order to find suitable values for V_{BN} and V_{BP} and the common-mode input voltage, we estimate the values of V_{GS1}, V_{GS7} and V_{GS9} using the Shichman-Hodges relation without considering the channel-length modulation, i.e.,

$$|V_{GS}| = |V_t| + \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}}$$

We find $V_{GS1} \simeq 0.75$ V, $|V_{GS7}| \simeq 0.90$ V and $V_{GS9} \simeq 0.65$ V. Allowing a drain-source voltage of 0.35 V for M_{10} and M_{11}, we select $V_{BN} = 1.0$ V. Allowing a voltage of 0.50 V across I_{BP}, we select $V_{BP} = 0.4$ V when using $V_{DD} = 1.8$ V. Allowing a voltage of 0.50 V across I_{BN}, we select a common-mode input voltage of 1.25 V.

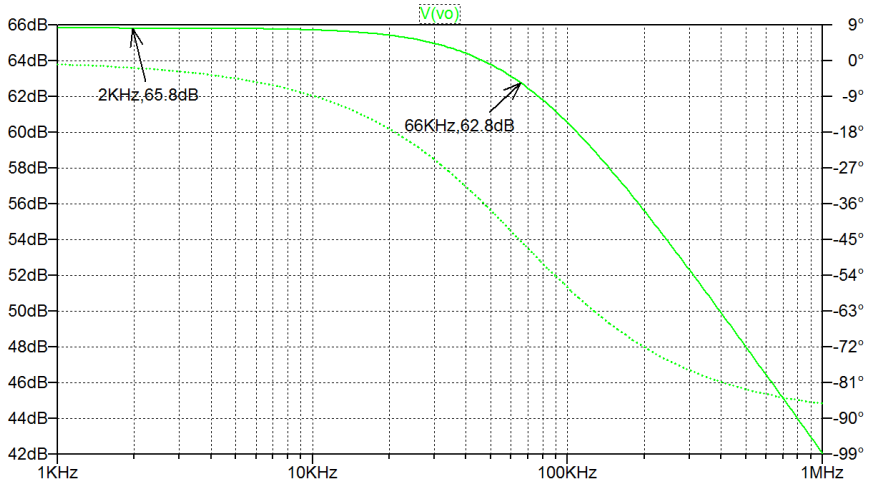


We first run a '.op' simulation to ensure that all transistors are in the active region. Shown below are results from the error log file. We notice that all transistors have $|V_{DS}| > |V_{DS\,\text{sat}}|$, so they are in the active region. From the error log file, we can also find the small-signal parameters. We find $g_{m1} = 1.24$ mA/V, $g_{m7} = 443$ µA/V, $g_{m9} = 860$ µA/V, $g_{ds1} = 18.6$ µA/V, $g_{ds7} = 12.8$ µA/V, $g_{ds9} = 9.74$ µA/V and $g_{ds11} = 9.65$ µA/V. We notice that the transconductance values are somewhat larger and that the output conductance values are somewhat smaller than the approximate values found from the hand calculation. This leads to a larger value of output resistance and gain and a smaller value of the -3 dB frequency. From the simulated small-signal parameters, we find $r_{out} = 1.55$ MΩ, $A_v = 1920$ V/V ~ 65.7 dB and $f_{\text{-3 dB}} = 68$ kHz.

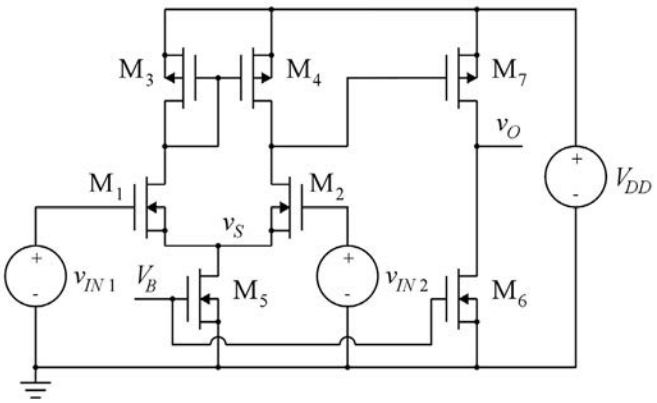
Results from Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m7          m6          m9          m8          m11         m10         m2          m1
Model:         pmos-sh     pmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:         -1.00e-04   -1.00e-04    1.00e-04    1.00e-04    1.00e-04    1.00e-04    2.00e-04    2.00e-04
Vgs:        -8.72e-01   -8.72e-01    6.33e-01    6.33e-01    6.31e-01    6.31e-01    7.22e-01    7.22e-01
Vds:        -6.40e-01   -6.40e-01    2.64e-01    2.64e-01    3.67e-01    3.67e-01    7.43e-01    7.43e-01
Vbs:         0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:        -4.20e-01   -4.20e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:      -4.52e-01   -4.52e-01    2.33e-01    2.33e-01    2.31e-01    2.31e-01    3.22e-01    3.22e-01
Gm:          4.43e-04    4.43e-04    8.60e-04    8.60e-04    8.64e-04    8.64e-04    1.24e-03    1.24e-03
Gds:         1.28e-05    1.28e-05    9.74e-06    9.74e-06    9.65e-06    9.65e-06    1.86e-05    1.86e-05
Gmb:         1.32e-04    1.32e-04    2.57e-04    2.57e-04    2.58e-04    2.58e-04    3.72e-04    3.72e-04
```

The result concerning gain and bandwidth may be confirmed by a '.ac' simulation. The following figure shows a plot from this simulation and we find values of gain and bandwidth which are very close to the values calculated from the simulated small-signal parameters.



Problem 5.2



Design the two-stage opamp shown above to have a differential small-signal gain of 30 dB in the first stage and a small-signal gain of 26 dB in the second stage. Use a channel length of $L = 0.8$ µm for all transistors and design M_5 and M_6 to give bias currents of $I_{D5} = I_{D6} = 0.1$ mA with a bias voltage $V_B = 0.7$ V. Assume transistor parameters as specified in Table 3.1 and use reasonable approximations in the design equations for the transistors. Assume that all transistors are in the active region.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

Transistors M_5 and M_6 may be designed from the specification of $I_{D5} = I_{D6} = 100$ µA and $V_B = 0.7$ V. From the Shichman-Hodges relation, we find when neglecting the channel-length modulation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_B - V_t)^2 \;\Rightarrow\; W = L\frac{2I_D}{\mu_n C_{ox}(V_B - V_t)^2}$$

Inserting numerical values, we find $W_5 = W_6 = 9.88$ µm.

Transistors M_1 and M_2 may be designed from the gain specification for the differential stage. Using the approximations given by Eqs. (3.71) and (3.72) in Bruun (2022), the gain is

$$A_1 = g_{m2}(r_{ds2} \parallel r_{ds4}) = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \simeq \frac{\sqrt{2\,\mu_n C_{ox}(W_2/L_2)I_{D2}}}{(\lambda_2 + \lambda_4)I_{D2}} \;\Rightarrow\; W_2 = L_2\frac{A_1^2(\lambda_2 + \lambda_4)^2 I_{D2}}{2\,\mu_n C_{ox}}$$

The gain is 30 dB, corresponding to $A_1 = 31.62$ V/V. I_{D2} is $I_{D2} = I_{D5}/2 = 50$ µA and with $L = 0.8$ µm, we find $\lambda_2 = 0.125$ V^{-1} and $\lambda_4 = 0.175$ V^{-1}. Inserting numerical values, we find $W_2 = W_1 = 10$ µm.

Transistor M_7 may be designed from the gain specification for the second stage. Using the approximations given by Eqs. (3.71) and (3.72) in Bruun (2022), the gain is

$$|A_2| = g_{m7}(r_{ds7} \parallel r_{ds6}) = \frac{g_{m7}}{g_{ds7} + g_{ds6}} \simeq \frac{\sqrt{2\,\mu_p C_{ox}(W_7/L_7)I_{D7}}}{(\lambda_7 + \lambda_6)I_{D7}} \;\Rightarrow\; W_7 = L_7\frac{|A_2|^2(\lambda_7 + \lambda_6)^2 I_{D7}}{2\,\mu_p C_{ox}}$$

The gain is 26 dB, corresponding to $|A_2| = 20$ V/V. I_{D7} is $I_{D7} = I_{D6} = 100$ µA and with $L = 0.8$ µm, we find $\lambda_6 = 0.125$ V^{-1} and $\lambda_7 = 0.175$ V^{-1}. Inserting numerical values, we find $W_7 = 32$ µm.

Finally, M_3 and M_4 may be designed using Eq. (5.6) in Bruun (2022) and $I_{D7} = I_{D6} = I_{D5}$, i.e.,

$$\frac{I_{D7}}{W_7/L_7} = \frac{I_{D3}}{W_3/L_3} = \frac{I_{D5}}{2(W_3/L_3)} \;\Rightarrow\; W_3/L_3 = (W_7/L_7)/2 \;\Rightarrow W_3 = W_7/2 = 16\ \mu\text{m}.$$

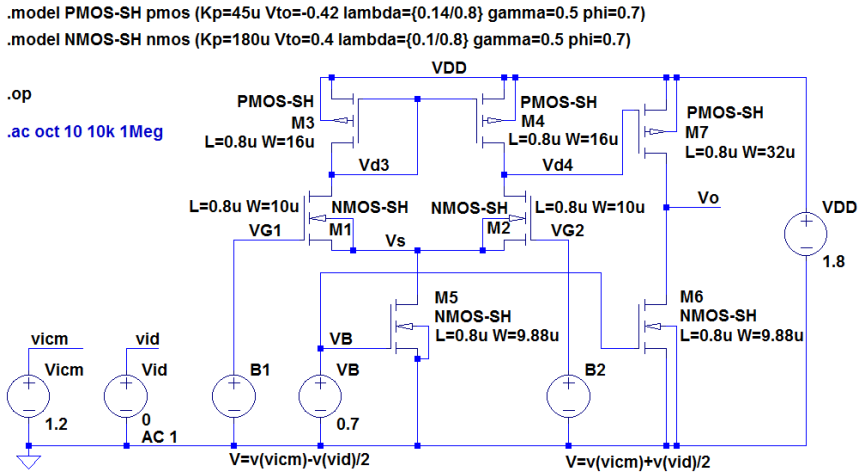
Transistor M_4 has the same channel width as M_3, so $W_4 = 16$ µm.

Problem 5.3

Use LTspice to simulate your design from Problem 5.2. Use $V_{DD} = 1.8$ V and find simulated values for the differential small-signal gain in the first stage and the small-signal gain in the second stage. Explain the differences between the simulated values and the values given in Problem 5.2.

Solution:

An LTspice schematic corresponding to Problem 5.2 is shown below with the transistor geometries found in Problem 5.2. For the common-mode input voltage, a value of 1.2 V is selected which ensures that all transistors in the input stage are in the active region. This is confirmed by a '.op' simulation. From the output file, we find a bias value of 0.85 V for the output voltage, so also the transistors in the output stage are in the active region. From the error log file, we notice that all transistors have $|V_{DS}| > |V_{DS\,\text{sat}}|$, confirming that they are in the active region. Results from the error log file are also shown below.



Results from Error log file

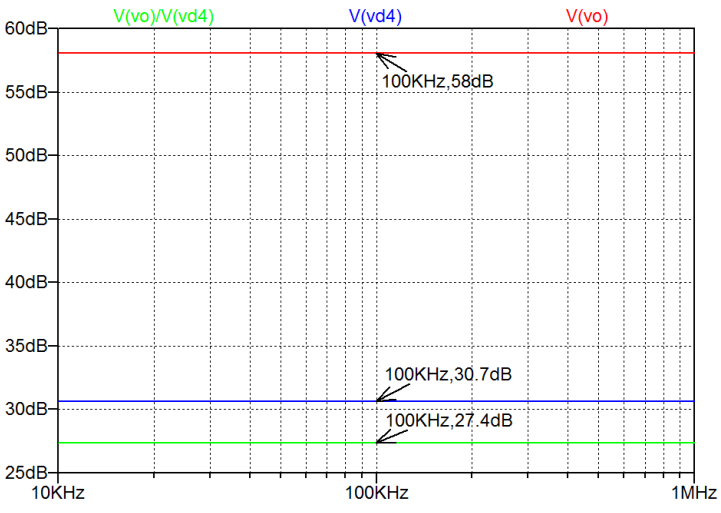
```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m7          m4          m3          m6          m5          m2          m1
Model:      pmos-sh     pmos-sh     pmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:      -1.11e-04   -5.37e-05   -5.37e-05    1.11e-04    1.07e-04    5.37e-05    5.37e-05
Vgs:     -7.45e-01   -7.45e-01   -7.45e-01    7.00e-01    7.00e-01    6.12e-01    6.12e-01
Vds:     -9.46e-01   -7.45e-01   -7.45e-01    8.54e-01    5.88e-01    4.67e-01    4.67e-01
Vbs:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:     -4.20e-01   -4.20e-01   -4.20e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:   -3.25e-01   -3.25e-01   -3.25e-01    3.00e-01    3.00e-01    2.12e-01    2.12e-01
Gm:       6.82e-04    3.31e-04    3.31e-04    7.38e-04    7.16e-04    5.06e-04    5.06e-04
Gds:      1.66e-05    8.31e-06    8.31e-06    1.25e-05    1.25e-05    6.34e-06    6.34e-06
Gmb:      2.04e-04    9.88e-05    9.88e-05    2.21e-04    2.14e-04    1.51e-04    1.51e-04
```

From the error log file, we find $g_{m2} = 506\ \mu A/V$, $g_{ds2} = 6.34\ \mu A/V$ and $g_{ds4} = 8.31\ \mu A/V$, so $A_1 = g_{m2}/(g_{ds2} + g_{ds4}) = 34.5\ V/V \sim 30.7\ dB$.

We also find $g_{m7} = 682\ \mu A/V$, $g_{ds7} = 16.6\ \mu A/V$ and $g_{ds6} = 12.5\ \mu A/V$, so $A_2 = g_{m7}/(g_{ds7} + g_{ds6}) = 23.4\ V/V \sim 27.4\ dB$.

The values for A_1 and A_2 are slightly larger than 30 dB and 26 dB because the factor $(1 + \lambda V_{DS})$ has been neglected in the calculations in Problem 5.2.

The gain may also be analyzed using a '.ac' simulation. Shown below is a plot from the '.ac' simulation. A_1 is the blue plot. A_2 is the green plot and the total gain is shown by the red plot.



Problem 5.4

Insert a capacitor $C_c = 1.5$ pF between gate and drain of M_7 in your design from Problem 5.2 and calculate the frequency of the dominant pole, assuming that C_c is much larger than the transistor capacitances. Simulate the -3 dB bandwidth and compare the simulated result to your calculated result.

Solution:

A capacitor C_c inserted between gate and drain of M_7 results in a dominant pole at the frequency

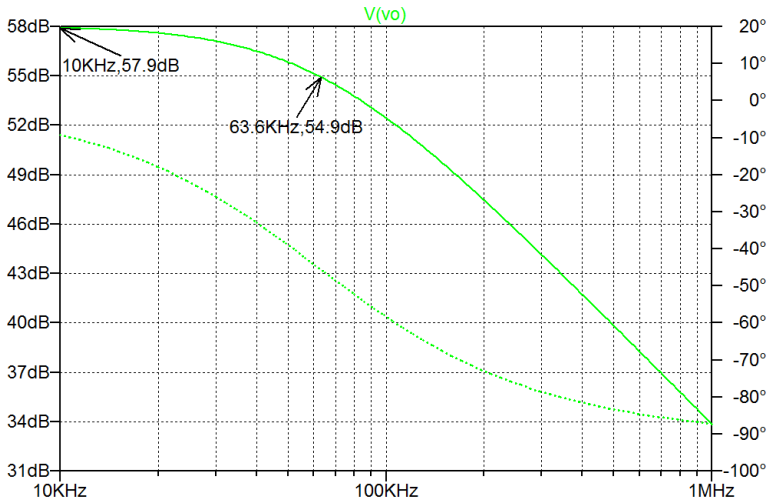
$$f_{p1} \simeq \frac{1}{2\pi(r_{ds2} \parallel r_{ds4})C_c(1+|A_2|)} = \frac{g_{ds2}+g_{ds4}}{2\pi C_c(1+|A_2|)},$$

compare to Eq. (5.9) in Bruun (2022).

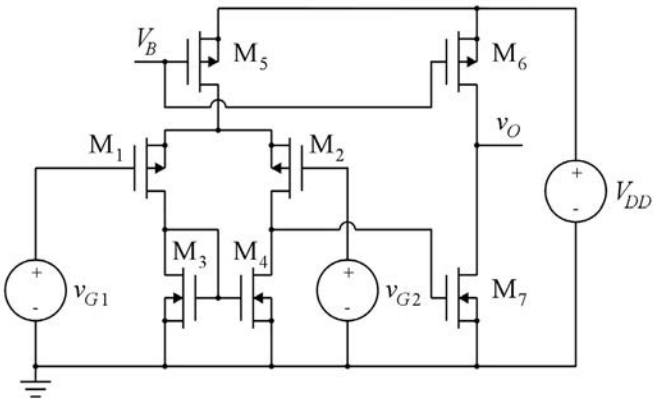
We may use the approximate relation Eq. (3.72) in Bruun (2022) to find $g_{ds2}+g_{ds4}$. With $I_{D2} = I_{D5}/2 = 50$ µA and with $L = 0.8$ µm, resulting in $\lambda_2 = 0.125$ V^{-1} and $\lambda_4 = 0.175$ V^{-1}, we find $g_{ds2}+g_{ds4} \simeq (\lambda_2+\lambda_4)I_{D2} = 15$ µA/V. Inserting this value and $C_c = 1.5$ pF and $|A_2| = 20$ V/V in the expression for f_{p1}, we find $f_{p1} = 75.8$ kHz.

Inserting $C_c = 1.5$ pF in the LTspice schematic from Problem 5.3 and running a '.op' simulation results in the output plot shown below. From this, we find $f_{p1} \simeq 63.6$ kHz. The difference between calculated value and simulated value is due to the factor $(1+\lambda V_{DS})$ which has been neglected in the calculations.

We note that using the simulated values of A_2, g_{ds2} and g_{ds4} found in Problem 5.3, we may calculate $f_{p1} = (g_{ds2}+g_{ds4})/(2\pi C_c(1+|A_2|)) = 64$ kHz, closely matching the simulated value for f_{p1}.



Problem 5.5



The figure above shows a two-stage opamp using a PMOS differential pair for the input stage. Design the opamp using transistors with parameters as specified in Table 3.1 and use a channel length of $L =$ 0.9 µm and an effective gate voltage $|V_{\text{eff}}| = |V_{GS} - V_t| = 0.3$ V for all transistors. The supply voltage is $V_{DD} = 1.8$ V.
Design the opamp to provide $g_{m1} = 0.3$ mA/V and $g_{m7} = 10\,g_{m1}$. Assume that all transistors are in the active region and use reasonable approximations in the design equations for the transistors.
Calculate the low-frequency differential small-signal gain and output resistance of the opamp.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

Transistors M_1 and M_2 are designed from the requirement that $g_{m1} = g_{m2} = 0.3$ mA/V. Using $g_m = 2I_D/|V_{\text{eff}}|$, we find $I_{D1} = I_{D2} = g_{m1}|V_{\text{eff}}|/2 = 45$ µA. From the Shichman-Hodges model, we find when neglecting the channel-length modulation

$$I_{D1} = \frac{1}{2}\mu_p C_{ox}\frac{W_1}{L_1}V_{\text{eff}}^2 \;\Rightarrow\; W_1 = L_1\frac{2I_{D1}}{\mu_p C_{ox}V_{\text{eff}}^2} = 20\ \mu\text{m}.$$

Transistor M_2 has the same channel width as M_1, so $W_2 = 20$ µm.

Transistor M_5 has $I_{D5} = 2I_{D1} = 90$ µA and the same effective gate voltage as M_1, so $W_5 = 2W_1 = 40$ µm.

For transistor M_7, we have $g_{m7} = 10\,g_{m3} = 3.0$ mA/V. From this, we find $I_{D7} = g_{m7}|V_{\text{eff}}|/2 = 450$ µA. From the Shichman-Hodges model, we find when neglecting the channel-length modulation

$$I_{D7} = \frac{1}{2}\mu_n C_{ox}\frac{W_7}{L_7}V_{\text{eff}}^2 \;\Rightarrow\; W_7 = L_7\frac{2I_{D7}}{\mu_n C_{ox}V_{\text{eff}}^2} = 50\ \mu\text{m}.$$

Transistor M_6 has $I_{D6} = 5I_{D5}$ and the same effective gate voltage as M_5, so $W_6 = 5W_5 = 200$ µm.

Transistors M_3 and M_4 have $I_{D3} = I_{D4} = I_{D7}/10$ and the same effective gate voltage as M_7, so $W_3 = W_4 = W_7/10 = 5$ µm.

The bias voltage V_B is calculated using Kirchhoff's voltage law:
$V_B = V_{DD} - |V_{GS5}| = V_{DD} - (|V_{\text{eff}}| + |V_{tp}|) = 1.08$ V.

The small-signal gain is calculated from Eq. (5.7) in Bruun (2022):

$$A_d \simeq g_{m1}\left(r_{ds2} \parallel r_{ds4}\right) g_{m7}\left(r_{ds6} \parallel r_{ds7}\right) = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m7}}{g_{ds6}+g_{ds7}}\right)$$

Using Eqs. (3.69) and (3.72) in Bruun (2022), we find

$$A_d \simeq \left(\frac{2I_{D1}}{|V_{\text{eff}}|(\lambda_2+\lambda_4)I_{D2}}\right)\left(\frac{2I_{D7}}{|V_{\text{eff}}|(\lambda_6+\lambda_7)I_{D7}}\right) = \left(\frac{2}{|V_{\text{eff}}|(\lambda_2+\lambda_4)}\right)\left(\frac{2}{|V_{\text{eff}}|(\lambda_6+\lambda_7)}\right)$$

With $L = 0.9$ µm, we have $\lambda_2 = \lambda_6 = 0.1/0.9$ V^{-1} and $\lambda_4 = \lambda_7 = 0.14/0.9$ V^{-1}. Inserting these values and $|V_{\text{eff}}| = 0.3$ V in the expression for A_d, we find $A_d \simeq 625$ V/V ~ 56 dB.

The output resistance is found from Eq. (5.8) in Bruun (2022):

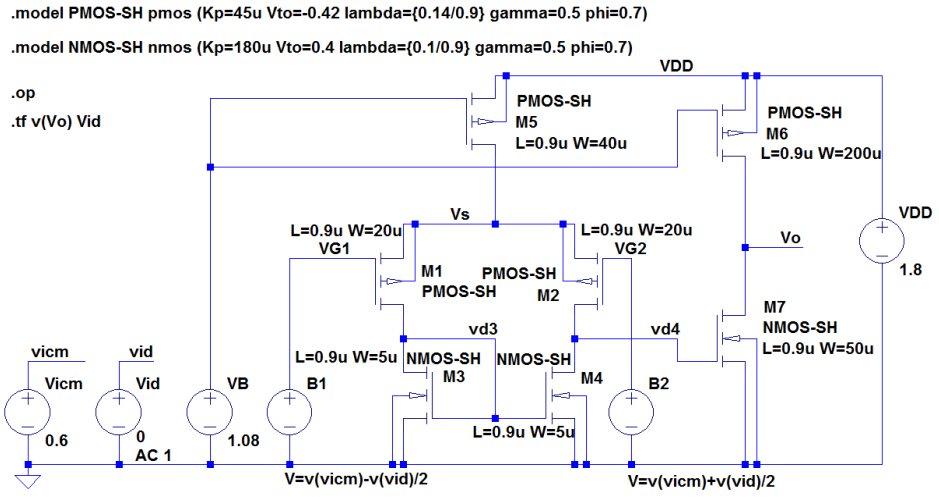
$$r_{out} = r_{ds6} \parallel r_{ds7} = \frac{1}{g_{ds6}+g_{ds7}} \simeq \frac{1}{(\lambda_6+\lambda_7)I_{D6}} = 8.33\ \text{k}\Omega$$

Problem 5.6

Use LTspice to simulate your design from Problem 5.5. Find simulated values for g_{m1} and g_{m7} and the differential small-signal gain and output resistance. Explain the differences between the simulated values and the values given in Problem 5.5.

Solution:

The following figure shows an LTspice schematic corresponding to Problem 5.6 with the transistor geometries found in Problem 5.5. For the common-mode input voltage, a value of 0.6 V is selected which ensures that all transistors in the input stage are in the active region. This is confirmed by a '.op' simulation. From the output file, we find a bias value of 1.06 V for the output voltage, so also the transistors in the output stage are in the active region. From the error log file, we notice that all transistors have $|V_{DS}| > |V_{DS\,\text{sat}}|$, confirming that they are in the active region. Results from the error log file are also shown.



Results from Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m2          m1          m6          m5          m7          m4          m3
Model:      pmos-sh     pmos-sh     pmos-sh     pmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:        -4.84e-05   -4.84e-05   -5.02e-04   -9.68e-05    5.02e-04    4.84e-05    4.84e-05
Vgs:       -7.17e-01   -7.17e-01   -7.20e-01   -7.20e-01    7.00e-01    7.00e-01    7.00e-01
Vds:       -6.17e-01   -6.17e-01   -7.40e-01   -4.83e-01    1.06e+00    7.00e-01    7.00e-01
Vbs:        0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:       -4.20e-01   -4.20e-01   -4.20e-01   -4.20e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:     -2.97e-01   -2.97e-01   -3.00e-01   -3.00e-01    3.00e-01    3.00e-01    3.00e-01
Gm:         3.26e-04    3.26e-04    3.35e-03    6.45e-04    3.35e-03    3.23e-04    3.23e-04
Gds:        6.87e-06    6.87e-06    7.00e-05    1.40e-05    4.99e-05    4.99e-06    4.99e-06
Gmb:        9.73e-05    9.73e-05    1.00e-03    1.93e-04    1.00e-03    9.65e-05    9.65e-05
```

From the error log file, we find $g_{m1} = 0.326$ mA/V and $g_{m7} = 3.35$ mA/V. These values are somewhat larger than the target values of 0.3 mA/V and 3.0 mA/V. This is due to the channel-length modulation where the factor $(1+\lambda V_{DS})$ causes the drain current of the bias current transistors M_5 and M_6 to be larger than the values of 90 µA and 450 µA, respectively, which were assumed in the calculation of the transconductances.

The gain and the output resistance may be simulated using a '.tf' simulation with '`v(Vo)`' as the output and '`Vin`' as the source. From this, we find a gain of 762 V/V and an output resistance of 8.34 kΩ. The gain is somewhat larger than the value found when using the approximations from Problem 5.5 because the transconductances g_{m1} and g_{m7} are larger than the target values as explained above. The simulated output resistance is very close to the calculated output resistance. Taking the factor $(1+\lambda V_{DS})$ into account, the small-signal transistor output resistance is given by $r_{ds} = (1+\lambda V_{DS})/(\lambda I_D)$. In this expression, the factor $(1+\lambda V_{DS})$ causes an increase in the value of r_{ds} but the larger value of I_D causes a decrease, thus cancelling the effect of the factor $(1+\lambda V_{DS})$.

Problem 5.7

Insert a capacitor C_c between gate and drain of M_7 in your design from Problem 5.5 and calculate the value of C_c required to obtain a gain-bandwidth product of 40 MHz. Assume that C_c is much larger than the transistor capacitances. You may also assume that the gain in the second stage is much larger than 1. Simulate the gain-bandwidth product and compare the simulated result to your calculated result.

Solution:

A capacitor C_c inserted between gate and drain of M_7 results in a dominant pole at the frequency

$$f_{p1} \simeq \frac{1}{2\pi\,(r_{ds2} \parallel r_{ds4})C_c(1+g_{m7}(r_{ds6} \parallel r_{ds7}))} \simeq \frac{1}{2\pi\,(r_{ds2} \parallel r_{ds4})C_c\,g_{m7}(r_{ds6} \parallel r_{ds7})}$$

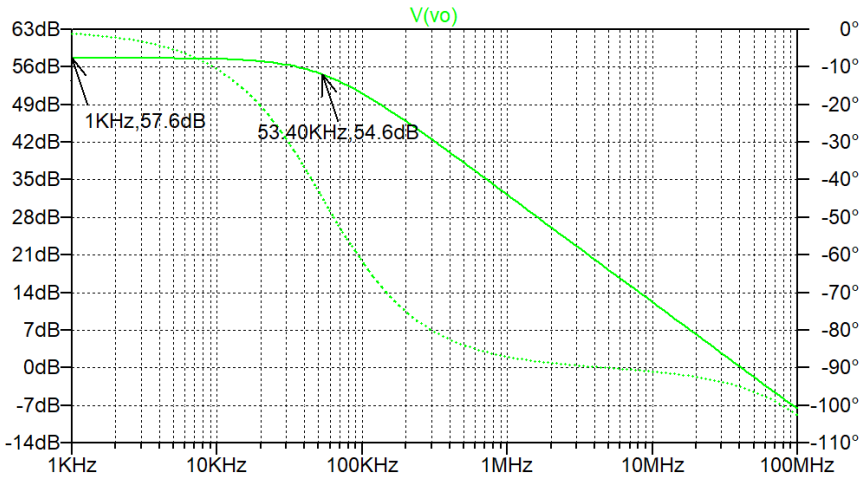
compare to Eq. (5.9) in Bruun (2022).

With the low-frequency gain given by Eq. (5.7) in Bruun (2022), we find the gain-bandwidth product

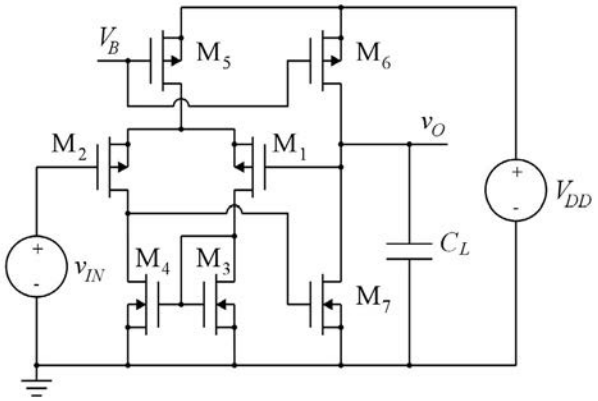
$$\text{GBW} = g_{m1}(r_{ds2} \parallel r_{ds4})g_{m7}(r_{ds6} \parallel r_{ds7})\frac{1}{2\pi\,(r_{ds2} \parallel r_{ds4})C_c\,g_{m7}(r_{ds6} \parallel r_{ds7})} = \frac{g_{m1}}{2\pi C_c}$$

From this relation, we find $C_c = g_{m1}/(2\pi\,\text{GBW})$. Inserting $g_{m1} = 0.3$ mA/V and GBW = 40 MHz, we find $C_c = 1.2$ pF.

Inserting $C_c = 1.2$ pF in the LTspice schematic from Problem 5.6 and running a '.ac' simulation results in the following output plot. From the plot, we find a low-frequency gain of 57.6 dB corresponding to 762V/V and a -3dB bandwidth of 53.4 kHz, resulting in a gain-bandwidth product of 40.7 MHz, i.e. close to the calculated value.



Problem 5.8




```
.model NMOS-SH nmos (Kp=180u Vto=0.40
+lambda={0.1u/L} gamma=0.5 phi=0.7
+Tox=4n CGSO=0.29n CGBO=0
+CGDO=0.29n CJ=3.65m CJSW=0.79n)
.model PMOS-SH nmos (Kp=45u Vto=-0.42
+lambda={0.14u/L} gamma=0.5 phi=0.7
+Tox=4n CGSO=0.28n CGBO=0
+CGDO=0.28n CJ=1.38m CJSW=1.44n)
```

The figure above shows the opamp from Problem 5.5 with the output fed back to the inverting input and a capacitor $C_L = 1$ pF connected to the output. Find the low-frequency small-signal gain. Use the transistor models shown above including capacitances to simulate the frequency response and find the frequency of the peak in the response. Use a bias value of the input voltage ensuring that all transistors are in the active region.

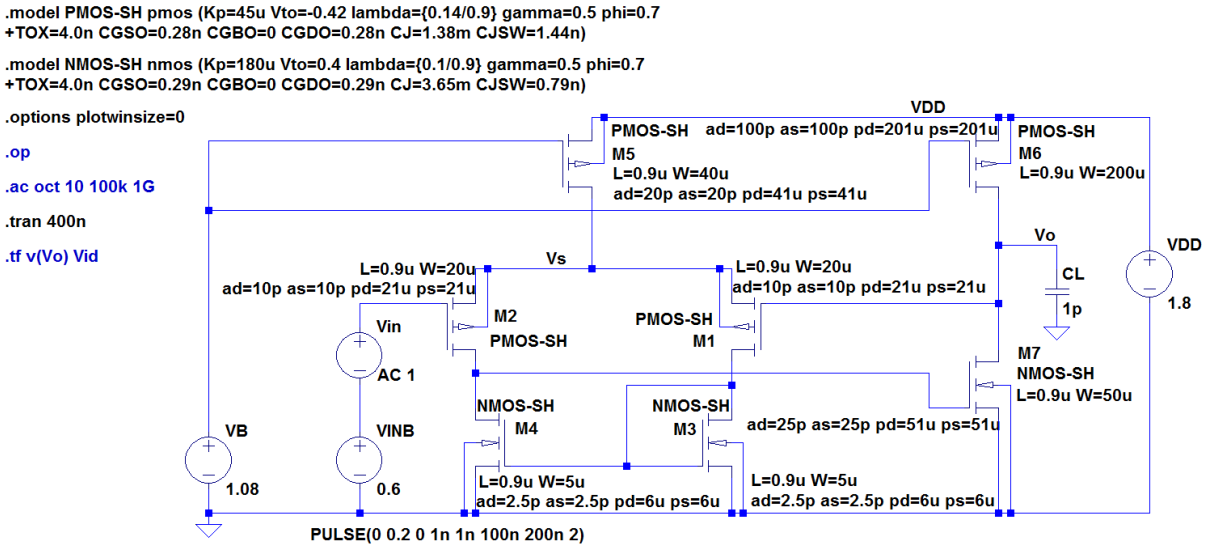
Simulate the transient response with a pulse input with a value of 0.2 V, a duration of 100 ns, rise time and fall time of 1 ns and a period of 200 ns. What is the frequency of oscillation?

Insert a capacitor $C_c = 1.2$ pF between gate and drain of M_7 and repeat the simulations.

What is the -3 dB bandwidth? Find the low-frequency output resistance.

Solution:

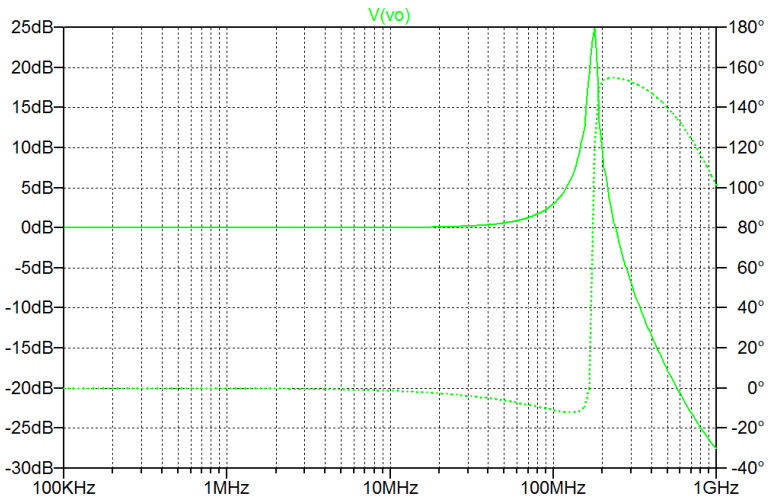
The following figure shows an LTspice schematic corresponding to Problem 5.8.



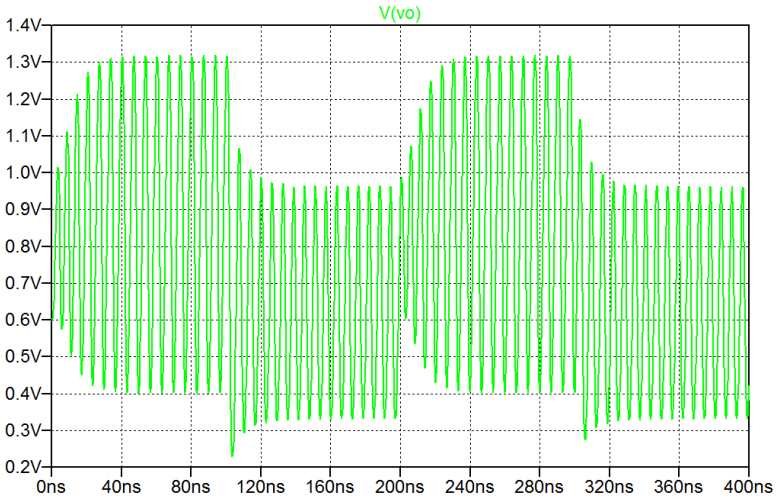
In this problem, we are concerned with the effects of higher-order poles and zeros in the circuit so we cannot assume that the external capacitors are the only capacitors which should be taken into account. Therefore we use transistor models where the capacitive transistor parameters are included. The values of lambda must be modified corresponding to a channel length of 0.9 µm. In the schematic, we must also specify areas and perimeters of drain and source for each transistor. The drain and source areas may be calculated as $W \times 0.5$ µm and the perimeters may be specified as $W + 1$ µm (Bruun 2022; Sedra & Smith 2016, Appendix B).

The bias value of the input voltage has been specified to 0.6 V, i.e., the same value as used for the common-mode input voltage in Problem 5.5. The bias point may be verified by a '.op' simulation. We find that all transistors are in the active region and that the output voltage is (almost) equal to the input voltage.

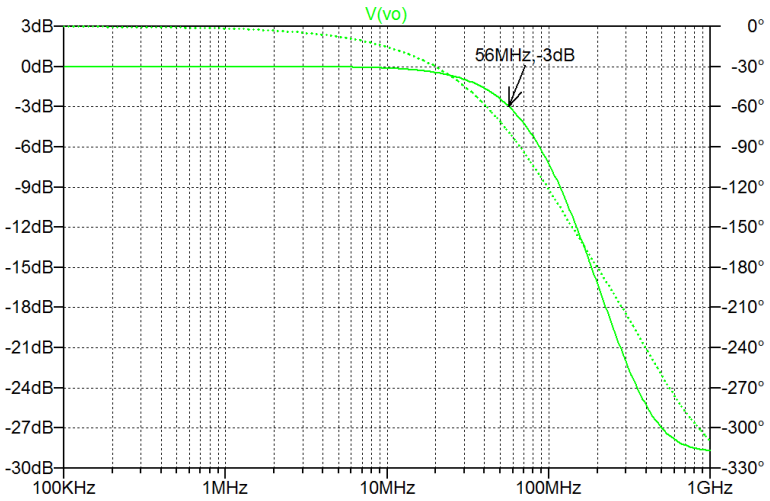
Next, a '.ac' simulation is run. The following plot shows the output voltage from this simulation. From this, we find that the low-frequency gain is 0 dB or 1 V/V. We also see that the frequency response has a peak at a frequency of about 180 MHz, indicating a potential instability.



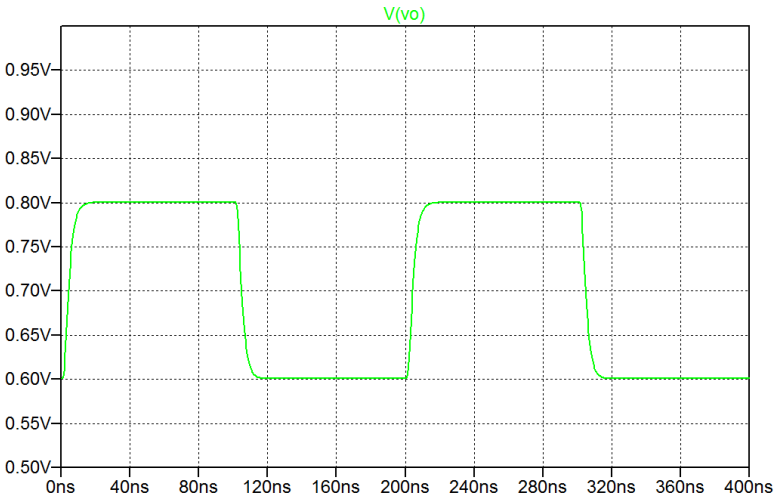
Next, we run a '.tran' simulation with the input voltage specified as a pulse with a value of 0.2 V, a duration of 100 ns, rise time and fall time of 1 ns and a period of 200 ns. The resulting plot of the output voltage is shown below. We see that the circuit oscillates at a frequency of about 150 MHz.



Finally, we insert a capacitor $C_c = 1.2$ pF between gate and drain of M_7 in the LTspice schematic and repeat the '.ac' simulation. The following figure shows a plot of the output voltage from this simulation. From the plot, we find the -3 dB bandwidth to be 56 MHz. The low-frequency output resistance may be obtained from a '.tf' simulation with '`v(Vo)`' as the output and '`Vin`' as the source. From this simulation, we find $r_{out} = 10.9\ \Omega$. We also find a low-frequency gain of 0.99925 V/V or 0 dB.



We may also repeat the transient simulation in order to check if the circuit is now stable. The output plot from the transient simulation is shown below. The stability of the circuit is confirmed.



References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Sedra, AS. & Smith, KC. 2016, *Microelectronic Circuits*, International Seventh Edition, Oxford University Press, New York, USA.

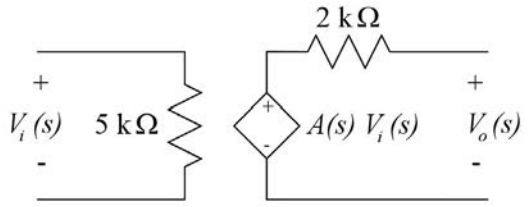
Chapter 6 – Feedback

Multiple-choice test

1. Completed statements:

A-4:	In an amplifier with feedback, the feedback network is called the β-network.
B-4:	For an amplifier built from an ideal opamp and a feedback network, the closed-loop gain is determined by the β-network.
C-7:	The product of the feedback factor and the open-loop gain is called the loop gain.
D-6:	For an amplifier with series-shunt feedback, the output resistance is reduced compared to the amplifier without feedback.
E-13:	For an amplifier with series-shunt feedback, the bandwidth is increased compared to the amplifier without feedback.
F-7:	The stability of an amplifier with feedback is determined by the loop gain.
G-10:	The phase margin in a first-order feedback system is larger than 90°.
H-18:	The sign of the phase margin in a stable feedback system is positive.
I-12:	A second-order feedback system with a phase margin between 65.5° and 76.3° shows overshoot in the transient response.
J-19:	A method for modifying the frequency response of the loop gain involves the insertion of a Miller capacitor. The Miller capacitor is inserted from input to output of an inverting gain stage.

2. The amplifier shown below has a transfer function $A(s) = 40/(1 + s/10^4 \text{ s}^{-1})$.



When inserted in an amplifier with series-shunt feedback and $\beta = 0.1$, the resulting closed-loop gain at low frequencies is

A: 4 V/V

B: 8 V/V

C: 40 V/V

Solution:

The closed-loop gain at low frequencies is calculated from $A_{CL} = \dfrac{A}{1+\beta A} = \dfrac{40 \text{ V/V}}{1+0.1\times 40} = 8 \text{ V/V}$.

3. When the amplifier shown above is inserted in an amplifier with series-shunt feedback and $\beta = 0.1$, the resulting -3 dB frequency is

A: 8 kHz
B: 10 kHz
C: 50 kHz

Solution:

The closed-loop bandwidth is calculated as the open-loop bandwidth multiplied by the amount of feedback, $1+\beta A = 1+0.1\times 40 = 5$. The open-loop bandwidth is $f_p = 10^4 \text{ s}^{-1}/(2\pi) = 1.59$ kHz, so the closed-loop bandwidth, equal to the -3 dB frequency, is $f_{pCL} = 5\times 1.59 \text{ kHz} = 7.96 \text{ kHz} \simeq 8$ kHz.

4. When the amplifier shown above is inserted in an amplifier with series-shunt feedback and $\beta = 0.1$, the resulting input resistance is

   A: 1 kΩ
   B: 5 kΩ
   C: 25 kΩ

Solution:

The closed-loop input resistance is calculated as the open-loop input resistance multiplied by the amount of feedback, i.e., $r_{inCL} = 5 \text{ k}\Omega \times 5 = 25 \text{ k}\Omega$.

5. When the amplifier shown above is inserted in an amplifier with series-shunt feedback and $\beta = 0.1$, the resulting output resistance is

   A: 200 Ω
   B: 400 Ω
   C: 500 Ω

Solution:

The closed-loop output resistance is calculated as the open-loop output resistance divided by the amount of feedback, i.e., $r_{inCL} = 2 \text{ k}\Omega/5 = 400 \ \Omega$.

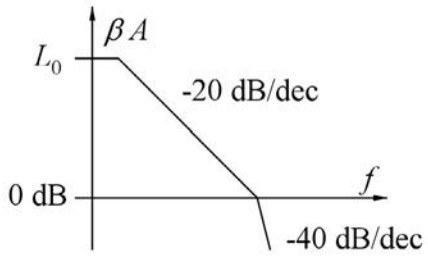
6. Using the amplifier shown above in a series-shunt feedback configuration, the feedback factor required to give a resulting closed-loop gain of 10 V/V at low frequency is

   A: 0.025
   B: 0.075
   C: 0.100

Solution:

From $A_{CL} = \dfrac{A}{1+\beta A}$, we find $\beta = 1/A_{CL} - 1/A = 1/10 - 1/40 = 0.075$.

7. A feedback amplifier is assumed to have a loop gain as shown below where $L_0 = \beta A_0 \gg 1$.



The phase margin, estimated from the piecewise linear Bode plot approximation, is

A: 45°
B: 52°
C: 65°

Solution:

From the piecewise linear Bode plot approximation, we notice that the loop gain $|L(j\omega)| = 0$ dB $= 1$ for $f = f_{p2}$ which is the frequency of the second pole. For $f = f_{p2}$, the phase of the loop gain is $\angle L(j\omega) = -135°$ so the phase margin is PM $= 180° - (-\angle L(j\omega)) = 45°$.

8. For the feedback amplifier with the loop gain shown above, the phase margin, estimated from the actual Bode plot (without using the piecewise linear approximation), is

A: 45°
B: 52°
C: 65°

Solution:

From the Bode plot shown, we find that the frequency f_{p2} of the second pole equals the gain-bandwidth product f_{tl} of the loop gain. Using Fig. 6.35(a) in Bruun (2022), we find that for $f_{p2} = f_{tl}$, the phase margin is PM $= 52°$.

9. For the amplifier shown above, the ratio between the closed-loop bandwidth and the frequency of the non-dominant pole is

A: 1
B: 1.27
C: 1.41

Solution:

With $f_{p2} = f_{tl}$, we find from Fig. 6.30(a) in Bruun (2022) that the closed-loop bandwidth is 1.27 times the gain-bandwidth product, so with the frequency of the non-dominant pole equal to the gain-bandwidth product, the closed-loop bandwidth is 1.27 times the frequency of the non-dominant pole.

10. The amplifier shown above may be compensated using a dominant-pole compensation. In order to achieve a phase margin of 65.5°, the dominant-pole compensation should reduce the frequency of the dominant pole by a factor of

    A: 2
    B: 3
    C: 4

Solution:

For achieving a phase margin of 65.5°, the ratio between the frequency f_{p2} of the non-dominant pole and the gain-bandwidth product f_{tl} of the loop gain should be 2, see Fig. 6.35(a) in Bruun (2022). Thus, the dominant-pole frequency compensation should reduce the gain-bandwidth product by reducing the frequency of the dominant pole by a factor of 2.

11. When the amplifier with the loop gain shown above is compensated to have a phase margin of 65.5°, the closed-loop bandwidth is reduced by a factor of approximately

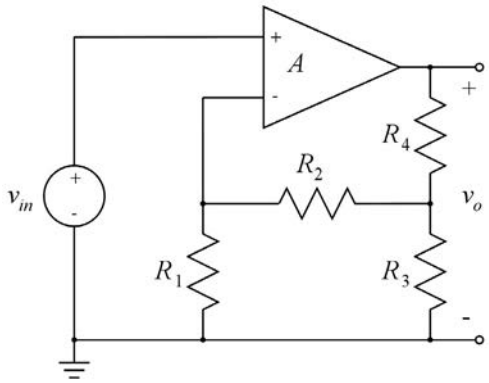
    A: 0.25
    B: 0.33
    C: 0.56

Solution:

For a system with $f_{p2} = 2\,f_{tl}$, we find from Fig. 6.30(a) in Bruun (2022) that the closed-loop bandwidth is 1.41 times the gain-bandwidth product f_{tl}, corresponding to $1.41/2 = 0.707$ times the frequency f_{p2} of the non-dominant pole. From Problem 9 above, we found that the closed-loop bandwidth of the uncompensated amplifier is 1.27 times the frequency f_{p2} of the non-dominant pole. Thus, the closed-loop bandwidth of the compensated amplifier is reduced by a factor of $0.707/1.27 = 0.56$.

Problems

Problem 6.1



For the feedback amplifier shown above, find an expression for the feedback factor β and the closed-loop gain v_o/v_{in}, assuming that the amplifier A is an ideal opamp.
Calculate the closed-loop gain for $R_1 = 1$ kΩ, $R_2 = 10$ kΩ, $R_3 = 2$ kΩ and $R_4 = 8$ kΩ.
Calculate the closed-loop gain, assuming that the opamp has a finite gain of $A = 100$ V/V.

Solution:

The feedback amplifier in Problem 6.1 is a feedback amplifier with a β-circuit consisting of the resistors R_1 - R_4 and an A-circuit consisting of the amplifier A. The feedback signal is the voltage v_f at the inverting input of the amplifier and the feedback factor is defined as $\beta = v_f/v_o$. Using the notation v_3 for the voltage at the node connecting R_2, R_3 and R_4, i.e., the voltage across across R_3, we find by repeated use of the voltage-divider rule Eq. (2.24) from Bruun (2022):

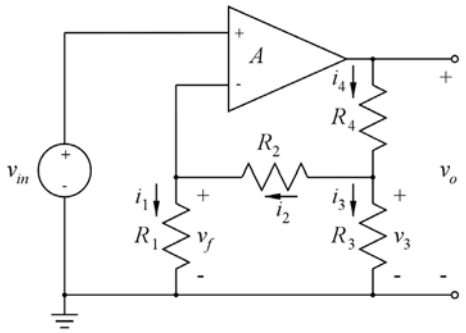
$$\beta = \frac{v_f}{v_o} = \left(\frac{v_3}{v_o}\right)\left(\frac{v_f}{v_3}\right) = \left(\frac{R_3 \parallel (R_2+R_1)}{R_3 \parallel (R_2+R_1)+R_4}\right)\left(\frac{R_1}{R_1+R_2}\right)$$

For an ideal opamp, we have an infinite gain, so we can find the closed-loop gain using Eq. (6.2) from Bruun (2022), i.e., $A_{CL} = v_o/v_{in} = 1/\beta$. Inserting numerical values, we find $A_{CL} = 63$ V/V.

With $A = 100$, we must use Eq. (6.1) from Bruun (2022) to find the closed-loop gain, i.e.,

$$A_{CL} = \frac{A}{1+\beta A} = \left(\frac{1}{\beta}\right)\left(\frac{A}{1/\beta + A}\right) = 63 \text{ V/V} \times \frac{100}{63+100} = 38.65 \text{ V/V}$$

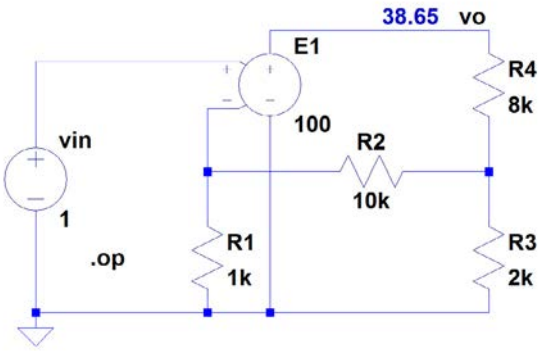
An alternative to the use of the voltage-divider rule for finding β is the use of Kirchhoff's laws and Ohm's law. In the following figure, we show the circuit with a notation of voltages and currents indicated for each resistor and we derive the output voltage v_o as a function of the feedback voltage v_f, working our way backwards through the feedback network.



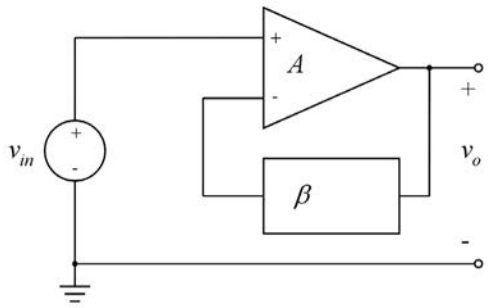
By repeated use of Kirchhoff's laws and Ohm's law, we find

$$
\begin{aligned}
i_2 &= i_1 = \frac{v_f}{R_1} \\
v_3 &= v_f + i_2 R_2 = v_f + v_f \frac{R_2}{R_1} = v_f \left(1 + \frac{R_2}{R_1}\right) \\
i_3 &= \frac{v_3}{R_3} = \left(\frac{v_f}{R_3}\right)\left(1 + \frac{R_2}{R_1}\right) \\
i_4 &= i_2 + i_3 = \frac{v_f}{R_1} + \left(\frac{v_f}{R_3}\right)\left(1 + \frac{R_2}{R_1}\right) = v_f \left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{R_2}{R_1 R_3}\right) \\
v_o &= v_3 + i_4 R_4 = v_f \left(1 + \frac{R_2}{R_1}\right) + v_f \left(\frac{R_4}{R_1} + \frac{R_4}{R_3} + \frac{R_4 R_2}{R_1 R_3}\right) = v_f \left(1 + \frac{R_2 + R_4}{R_1} + \frac{R_4}{R_3} + \frac{R_4 R_2}{R_1 R_3}\right) \\
&\Rightarrow \\
\beta &= \frac{v_f}{v_o} = \left(1 + \frac{R_2 + R_4}{R_1} + \frac{R_4}{R_3} + \frac{R_4 R_2}{R_1 R_3}\right)^{-1} \Rightarrow A_{CL} = \frac{1}{\beta} = \left(1 + \frac{10+8}{1} + \frac{8}{2} + \frac{8 \times 10}{1 \times 2}\right) = 63 \text{ V/V}.
\end{aligned}
$$

The numerical results may be verified using LTspice. Shown below is an LTspice schematic corresponding to Problem 6.1 with $A = 100$ V/V. From a '.op' simulation, we find the closed loop gain as the output voltage when the input voltage has a value of 1 V. From the output file, we find an output voltage of 38.65 V. In order to find the closed-loop gain when A is an ideal opamp, we select a very high gain for the voltage-controlled voltage source '`E1`'. With a gain of 10^6, we find an output voltage of 62.996 V, confirming the calculated gain of 63 V/V.



Problem 6.2



For the feedback amplifier shown above, assume that the amplifier is a voltage amplifier with a gain A, an infinite input resistance and an output resistance of 0. With A infinite, the closed-loop gain is $G_0 = v_o/v_{in} = 1/\beta$.
Show that the relative reduction in closed-loop gain caused by a finite value of A is $G_0/(A+G_0)$.

For the circuit from Problem 6.1, find the minimum value of A required to obtain a closed-loop gain which deviates at most 2% from the value obtained with an ideal opamp.

Solution:

With a finite gain A, the closed-loop gain is $A_{CL} = \dfrac{A}{1+\beta A}$. With A infinite, the closed-loop gain is $G_0 = 1/\beta$. Thus, the relative reduction in closed loop gain caused by the finite value of A is

$$\frac{G_0 - A_{CL}}{G_0} = 1 - \frac{A}{G_0(1+\beta A)}$$

Inserting $\beta = 1/G_0$, we find

$$\frac{G_0 - A_{CL}}{G_0} = 1 - \frac{A}{G_0(1+\beta A)} = 1 - \frac{A}{G_0 + A} = \frac{G_0}{G_0 + A} \quad \text{q.e.d.}$$

For the circuit from Problem 6.1, we have $G_0 = 63$ V/V, so for $\dfrac{G_0 - A_{CL}}{G_0} \leq 2\%$, we find

$$\frac{63}{63+A} \leq 0.02 \;\Rightarrow\; A \geq \frac{63 - 63 \times 0.02}{0.02} = 3087 \text{ V/V}$$

This result may also be confirmed by LTspice using the same schematic as for Problem 6.1 with the gain of the voltage-controlled voltage source '`E1`' specified to 3087. With this gain, the simulated output voltage is 61.74 V which is 98% of 63.00 V as required.

Problem 6.3

An amplifier with a specified gain of $A = 1000$ V/V is used to implement a feedback amplifier with a closed-loop gain of 100 V/V. Assuming a 30% tolerance in the specification of A, what is the tolerance of the closed-loop gain? What is the tolerance of the closed-loop gain if it is reduced to 10 V/V ?
What is the total gain and the tolerance of the total gain for an amplifier using two cascade-connected stages where each stage provides a closed-loop gain of 10 V/V ?

Solution:

With a closed-loop gain of 100 V/V and an open-loop gain of 1000 V/V, the amount of feedback is $(1+\beta A) = A/A_{CL} = 10$.

Using Eq. (6.5) from Bruun (2022), we find $\dfrac{dA_{CL}}{A_{CL}} = \left(\dfrac{1}{1+A\beta}\right)\dfrac{dA}{A} = \left(\dfrac{1}{10}\right)30\% = 3\%$.

With a closed-loop gain of 10 V/V and an open-loop gain of 1000 V/V, the amount of feedback is $(1+\beta A) = A/A_{CL} = 100$, resulting in $\dfrac{dA_{CL}}{A_{CL}} = \left(\dfrac{1}{1+A\beta}\right)\dfrac{dA}{A} = \left(\dfrac{1}{100}\right)30\% = 0.3\%$.

For two cascade-connected gain stages with gains A_1 and A_2, the resulting gain is $G = A_1A_2$, so with $A_1 = A_2 = 10$ V/V, we find $G = 100$ V/V.
With each gain being $A_{CL} + \Delta A_{CL}$, we find $G = (A_{CL} + \Delta A_{CL})^2 = A_{CL}^2 + 2A_{CL}\Delta A_{CL} + (\Delta A_{CL})^2$. For $\Delta A_{CL} \ll A_{CL}$, we find $(\Delta A_{CL})^2 \ll 2A_{CL}\Delta A_{CL}$, so $G \simeq A_{CL}^2 + 2A_{CL}\Delta A_{CL}$, implying $\Delta G = 2A_{CL}\Delta A_{CL}$ and

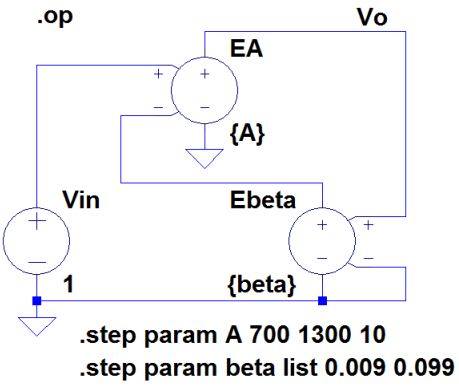
$$\frac{\Delta G}{G} \simeq \frac{2A_{CL}\Delta A_{CL}}{A_{CL}^2} = 2\frac{\Delta A_{CL}}{A_{CL}}$$

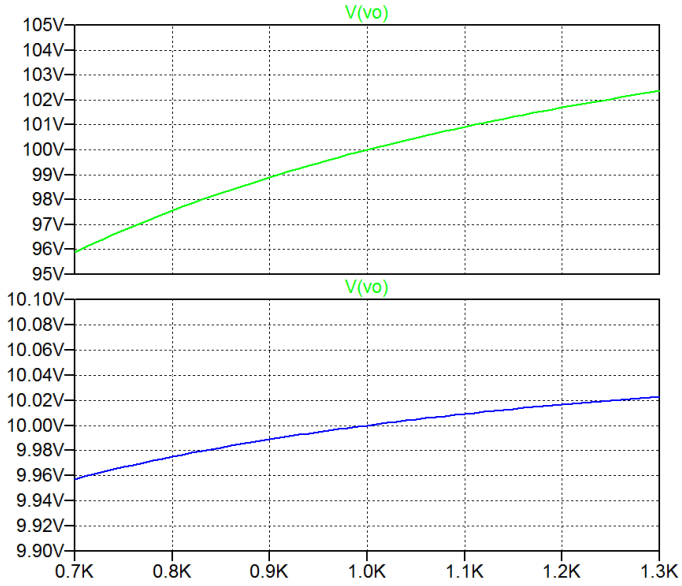
With $\Delta A_{CL}/A_{CL} = 0.3\%$, we find $\Delta G/G \simeq 0.6\%$.

We may investigate the problem using LTspice. The following figure shows an LTspice schematic with a voltage-controlled voltage source '`EA`' as the A-circuit and a voltage-controlled voltage source '`Ebeta`' as the β-circuit. The value of β is found from

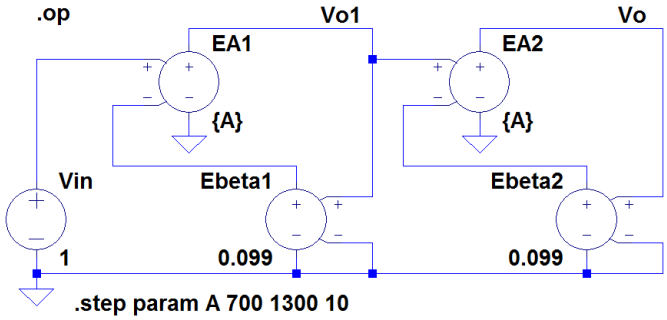
$$A_{CL} = \frac{A}{1+A\beta} \;\Rightarrow\; \beta = \frac{1}{A}\left(\frac{A}{A_{CL}} - 1\right) = \frac{1}{A_{CL}} - \frac{1}{A}$$

With $A_{CL} = 100$ and $A = 1000$, we find $\beta = 0.009$ and with $A_{CL} = 10$ and $A = 1000$, we find $\beta = 0.099$. In the schematic, the gain of '`Ebeta`' is stepped between these two values and the gain of '`EA`' is stepped from 700 to 1300, i.e., $1000 \pm 30\%$. Running a '.op' simulation, we may obtain a plot of the closed-loop gain versus the open-loop gain. From the plots, we find that the relative variation in closed-loop gain reaches its maximum value for the minimum value of open-loop gain. For the closed-loop gain of 100 V/V, we find an error of about 4% and for a closed-loop gain of 10 V/V, we find an error of about 0.4%, i.e., values which are somewhat higher than the values calculated from the expression given by Eq. (6.5). The reason for this is that in the derivation of Eq. (6.5), it was assumed that $\Delta A \ll A$ and with ΔA being 30% of A, this condition is not really fulfilled.

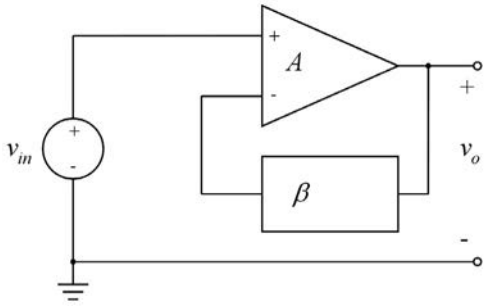




Also the two-stage amplifier may be analyzed using LTspice. The following figure shows an LTspice schematic corresponding to the two-stage amplifier with $\beta = 0.099$ for each of the amplifiers. From the plot of the closed-loop gain versus the open-loop gain, we find a maximum error of about 0.85%, i.e., again somewhat larger than the value found from the equations where it was assumed that $\Delta A \ll A$.



Problem 6.4



For the feedback amplifier shown above, assume that the amplifier is a voltage amplifier with a gain $A = 200$ V/V, an infinite input resistance and an output resistance of 10 kΩ. Also assume that the β-network does not load the amplifier.

What is the maximum closed-loop gain that can be achieved if the closed-loop output resistance must not be larger than 1 kΩ ?

Which value of β is required to give the maximum closed-loop gain?

Solution:

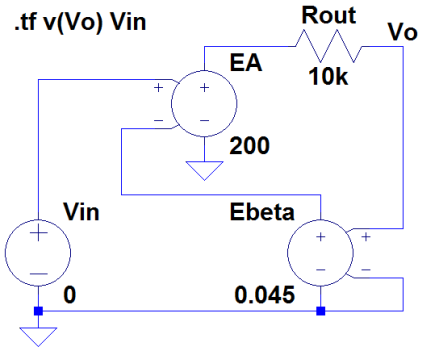
With an output resistance of the basic amplifier of $r_{out} = 10$ kΩ and an output resistance of the amplifier with feedback of $r_{out\,CL} \leq 1$ kΩ, we find from Eq. (6.13) in Bruun (2022):

$$(1+\beta A) \geq \frac{r_{out}}{r_{out\,CL}} = 10$$

The closed-loop gain is given by $A_{CL} = A/(1+\beta A)$, so with $(1+\beta A) \geq 10$, we find $A_{CL} \leq A/10 = 20$ V/V.

From $A_{CL} = A/(1+\beta A)$, we find $\beta = 1/A_{CL} - 1/A$, and for $A = 200$ V/V and $A_{CL} = 20$ V/V, we find $\beta = 0.045$ V/V.

The result may be verified using LTspice. Shown below is an LTspice schematic corresponding to Problem 6.4 with $\beta = 0.045$ V/V. From the output file from a '.tf' simulation, we find a gain of 20 V/V and an output resistance of 1000 Ω.

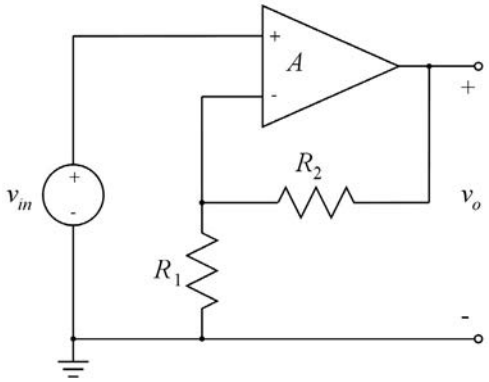


Results from '.tf' simulation.

```
        --- Transfer Function ---

Transfer_function:              20              transfer
vin#Input_impedance:            1e+020          impedance
output_impedance_at_V(vo):      1000            impedance
```

Problem 6.5

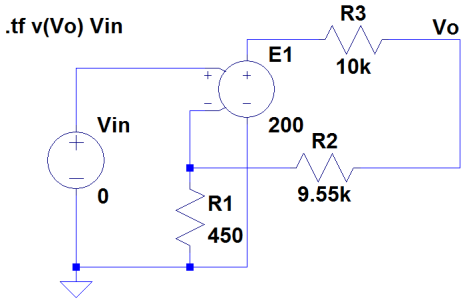


For the feedback amplifier shown above, assume that the amplifier is a voltage amplifier with a gain $A =$ 200 V/V, an infinite input resistance and an output resistance of 10 kΩ. Also assume that $R_1 = 0.45$ kΩ and $R_2 = 9.55$ kΩ.

Find the closed-loop gain v_o/v_{in} and the closed-loop output resistance. You may use LTspice for this.

Solution:

Using LTspice to solve the problem, we run a '.tf' simulation from the LTspice schematic shown below. From the '.tf' simulation, we find $A_{CL} = v_o/v_{in} = 18.18$ V/V and $r_{out\,CL} = 909\ \Omega$.



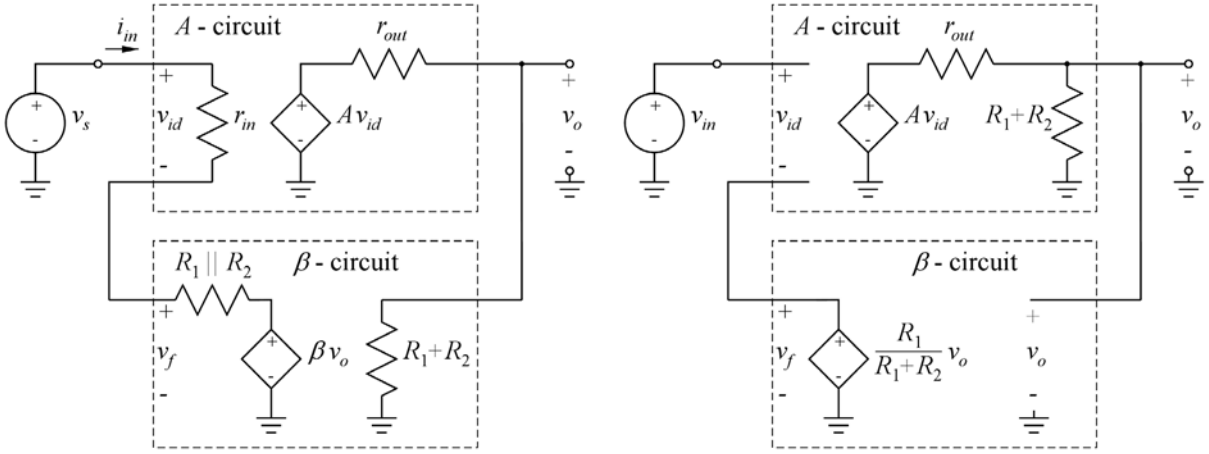
Results from '.tf' simulation.

```
        --- Transfer Function ---

Transfer_function:              18.1818         transfer
v1#Input_impedance:             1e+020          impedance
output_impedance_at_V(vo):      909.091         impedance
```

The results found using LTspice may be compared to results calculated using feedback theory. For calculating the results, a first approximation may be to neglect r_{out} when calculating the amount of feedback. Thus, $A = 200$ V/V and $\beta = R_1/(R_1 + R_2) = 0.045$ V/V. From this, we find $A_{CL} = A/(1 + \beta A) = 20$ V/V and $r_{out\,CL} = r_{out}/(1 + \beta A) = 1$ kΩ. Clearly, these results do not match the simulated values exactly.

In order to find exact analytical results, we must modify the circuit as shown in Fig. 6.14 from Bruun (2022). The following figure shows a redrawn version of the circuit (left). With $r_{in} = \infty$, we may simplify the circuit as shown in the right part of the figure. From the A-circuit, we find the open-loop gain to be $A' = v_o/v_{id} = A(R_1 + R_2)/(r_{out} + R_1 + R_2) = 100$ V/V and we find the open-loop output resistance to be $r'_{out} = r_{out} \parallel (R_1 + R_2) = 5$ kΩ. From the β-circuit, we find $\beta = R_1/(R_1 + R_2) = 0.045$ V/V. Using the modified values of open-loop gain and open-loop output resistance, we find the closed-loop gain $A_{CL} = A'/(1 + \beta A') = 18.18$ V/V and the closed-loop output resistance $r_{out\,CL} = r'_{out}/(1 + \beta A') = 909\ \Omega$, i.e., values exactly matching the simulated values.



An exact solution for the closed-loop gain may also be found simply by the use of Kirchhoff's laws. A node equation at the output node results in

$$\frac{A(v_{in}-v_f)-v_o}{r_{out}} = \frac{v_o}{R_1+R_2}$$

and with $v_f = \dfrac{R_1}{R_1+R_2}\, v_o$, we find

$$\begin{aligned} A(v_{in}-\frac{R_1}{R_1+R_2}\, v_o)-v_o &= \frac{r_{out}}{R_1+R_2}\, v_o \\ \Rightarrow \quad \frac{v_o}{v_{in}} &= \frac{A(R_1+R_2)}{r_{out}+R_1+R_2+AR_1} = 18.18 \text{ V/V.} \end{aligned}$$

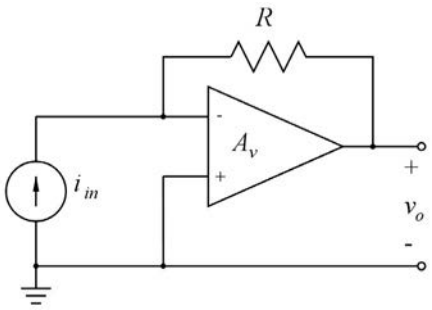
For finding the closed-loop output resistance, we reset the input voltage, apply a current i_o to the output and calculate the output voltage v_o. Using a node equation at the output, we find

$$i_o = \frac{v_o}{R_1+R_2} + \frac{v_o - A\, v_{id}}{r_{out}}$$

and with $v_{id} = v_{in} - v_f = -v_f = -\dfrac{R_1}{R_1+R_2} v_o$, we find

$$\begin{aligned} i_o &= \frac{v_o}{R_1+R_2} + \frac{v_o + A\, v_o R_1/(R_1+R_2)}{r_{out}} \\ \Rightarrow \quad r_{out\,CL} &= \frac{v_o}{i_o} = \left(\frac{1}{R_1+R_2} + \frac{1+AR_1/(R_1+R_2)}{r_{out}} \right)^{-1} \\ &= (R_1+R_2) \parallel \left(\frac{r_{out}}{1+AR_1/(R_1+R_2)} \right) = 909\ \Omega \end{aligned}$$

Problem 6.6



For the feedback amplifier shown above, assume that the amplifier is a voltage amplifier with a gain A_v, an infinite input resistance and an output resistance of 0. Use node equations and loop equations to find an expression for the closed-loop gain $A_{CL} = v_o/i_{in}$ and the closed-loop input resistance r_{inCL}. Calculate the values of closed-loop gain and input resistance for $A_v = 20$ V/V and $R = 10$ kΩ.
Repeat the problem, assuming a non-zero output resistance of $r_{out} = 100\ \Omega$ for the amplifier.

Solution:

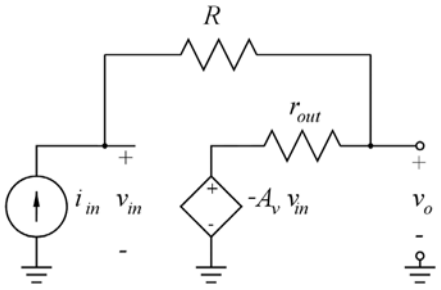
The following figure shows a circuit model for the amplifier. With $r_{out} = 0$, a node equation at the input node results in

$$i_{in} = \frac{v_{in} - v_o}{R} = \frac{v_{in} + A_v v_{in}}{R} \quad \Rightarrow \quad r_{inCL} = \frac{v_{in}}{i_{in}} = \frac{R}{1 + A_v}$$

Using a loop equation, we find

$$v_o = v_{in} - R\,i_{in} = r_{inCL}\,i_{in} - R\,i_{in} \quad \Rightarrow \quad A_{CL} = \frac{v_o}{i_{in}} = r_{inCL} - R = \frac{R}{1 + A_v} - \frac{R + RA_v}{1 + A_v} = -\frac{RA_v}{1 + A_v}$$

Inserting $A_v = 20$ V/V and $R = 10$ kΩ, we find $A_{CL} = -9.524$ kΩ and $r_{inCL} = 476\ \Omega$.



For a non-zero value of r_{out}, we find

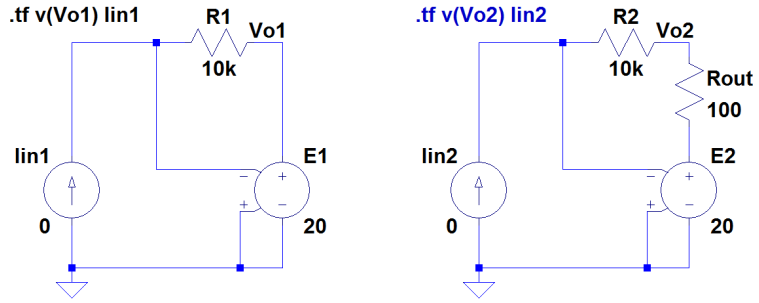
$$i_{in} = \frac{v_{in} + A_v v_{in}}{R + r_{out}} \quad \Rightarrow \quad r_{inCL} = \frac{v_{in}}{i_{in}} = \frac{R + r_{out}}{1 + A_v}$$

Using a loop equation, we find

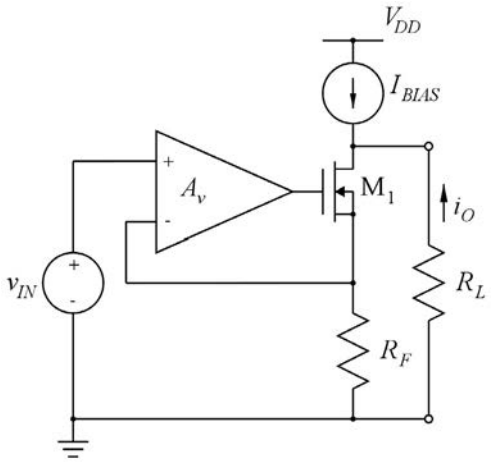
$$v_o = v_{in} - R\,i_{in} = r_{inCL}\,i_{in} - R\,i_{in} \quad \Rightarrow \quad A_{CL} = \frac{v_o}{i_{in}} = r_{inCL} - R = \frac{R + r_{out}}{1 + A_v} - \frac{R + RA_v}{1 + A_v} = -\frac{R(A_v - r_{out}/R)}{1 + A_v}$$

Inserting $A_v = 20$ V/V, $r_{out} = 100\ \Omega$ and $R = 10$ kΩ, we find $A_{CL} = -9.519$ kΩ and $r_{inCL} = 481\ \Omega$.

The numerical results may be verified using LTspice. The LTspice schematic below shows two versions of the circuit, one with $r_{out} = 0$ and one with $r_{out} = 100\ \Omega$. Running '.tf' simulations for each of the circuits, we find the numerical values of closed-loop gain and closed-loop input resistance calculated above.



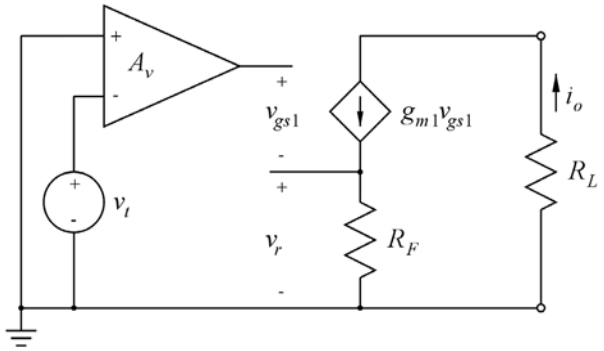
Problem 6.7



The figure above shows a transconductance amplifier with series-series feedback in order to obtain a well-defined small-signal transconductance i_o/v_{in}. The amplifier is a voltage amplifier with $A_v = 60$ V/V, infinite input resistance and an output resistance of 0. Transistor M_1 is biased to have $g_{m1} = 1$ mA/V. The small-signal output resistance of M_1 can be neglected. The resistor R_F has a value of 5 kΩ.
Find the small-signal loop gain $A\beta$, the feedback factor β and the closed-loop transconductance i_o/v_{in}.

Solution:

For finding the loop gain, we break the feedback loop at the negative input of the voltage amplifier and apply a test voltage v_t to the negative amplifier input while resetting the input voltage to the positive amplifier input. Using Eq. (6.46) from Bruun (2022), the loop gain is found as $A\beta = -v_r/v_t$ where v_r is the returned voltage at the breakpoint.
Shown below is a circuit for calculating v_r. The transistor has been replaced by a small-signal model.



Using a node equation at the return node, we find

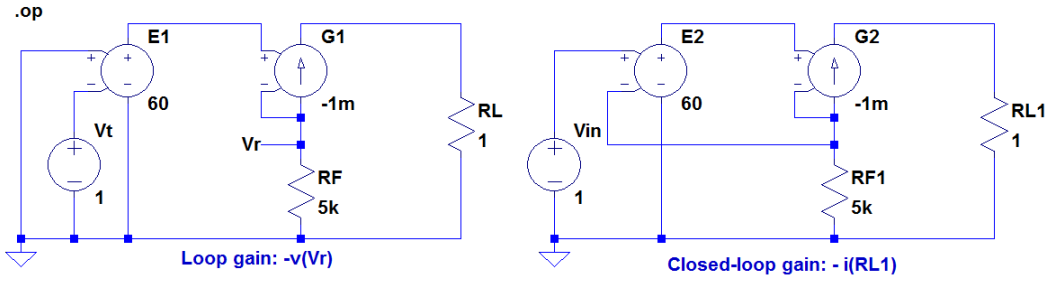
$$\frac{v_r}{R_F} = g_{m1}v_{gs1} = g_{m1}(-A_v v_t - v_r) \quad \Rightarrow \quad A\beta = -\frac{v_r}{v_t} = A_v \frac{g_{m1}R_F}{1+g_{m1}R_F} = 50 \text{ V/V}$$

The feedback factor β is found as $\beta = \dfrac{v_r}{i_o} = R_F = 5 \text{ k}\Omega$.

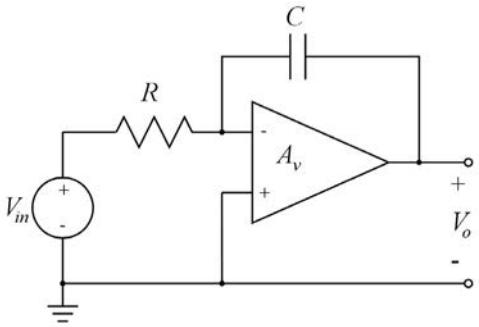
The closed-loop transconductance is found as

$$A_{CL} = \frac{i_o}{v_{in}} = \frac{A}{1+A\beta} = \frac{1/\beta}{1+1/(A\beta)} = \left(\frac{1}{R_F}\right)\left(\frac{A_v g_{m1}R_F}{(A_v+1)g_{m1}R_F+1}\right) = \left(\frac{1}{5 \text{ k}\Omega}\right)\left(\frac{300}{306}\right) = 0.196 \text{ mA/V}$$

The numerical results may be verified using LTspice. The LTspice schematic shown below includes a version for finding the loop gain (left) and a version for finding the closed-loop gain (right) using a '.op' simulation with the relevant input voltage set to a value of 1 V. The load resistor has been selected to 1 Ω. From the output file, we find $A\beta =$ `-v(Vr)` $= 50$ V/V and $A_{CL} =$ `-i(RL1)` $= 0.196078$ mA/V.



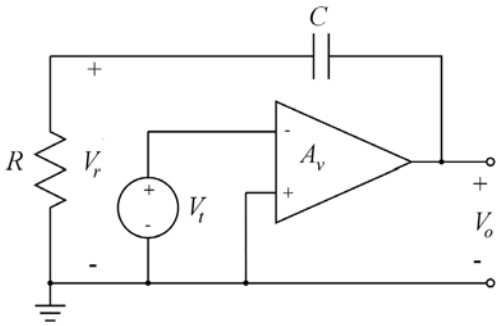
Problem 6.8



The figure above shows an inverting integrator built from an opamp, a resistor $R = 10$ kΩ and a capacitor $C = 16$ pF. The opamp has infinite input resistance, an output resistance of 0, and the transfer function $A_v(s)$ has a low-frequency gain of 1000 V/V and a single pole causing a gain-bandwidth product of 100 MHz.
Find an expression for the loop gain $L(s)$ and find the phase margin of the system.

Solution:

For finding the loop gain, we break the feedback loop at the negative input of the voltage amplifier and apply a test voltage V_t to the negative amplifier input while resetting the input voltage to the integrator. Using Eq. (6.46) from Bruun (2022), the loop gain is found as $L(s) = -V_r/V_t$ where V_r is the returned voltage at the breakpoint. Shown below is a figure for calculating V_r.



From this figure, we find

$$L(s) = -\frac{V_r}{V_t} = A_v(s)\frac{R}{R+1/(sC)} = A_v(s)\frac{sRC}{1+sRC}$$

The transfer function $A_v(s)$ has a low-frequency gain of $A_0 = 1000$ V/V and a gain-bandwidth product of GBW = 100 MHz, implying that it has a single pole at the frequency $f_{p1} = \text{GBW}/A_0 = 100$ kHz.

In the s-domain, this corresponds to an angular pole frequency $\omega_{p1} = 2\pi\,\text{GBW}/A_0$, so the transfer function $A_v(s)$ is

$$A_v(s) = \frac{A_0}{1+s/\omega_{p1}} = \frac{A_0}{1+sA_0/(2\pi\,\text{GBW})}$$

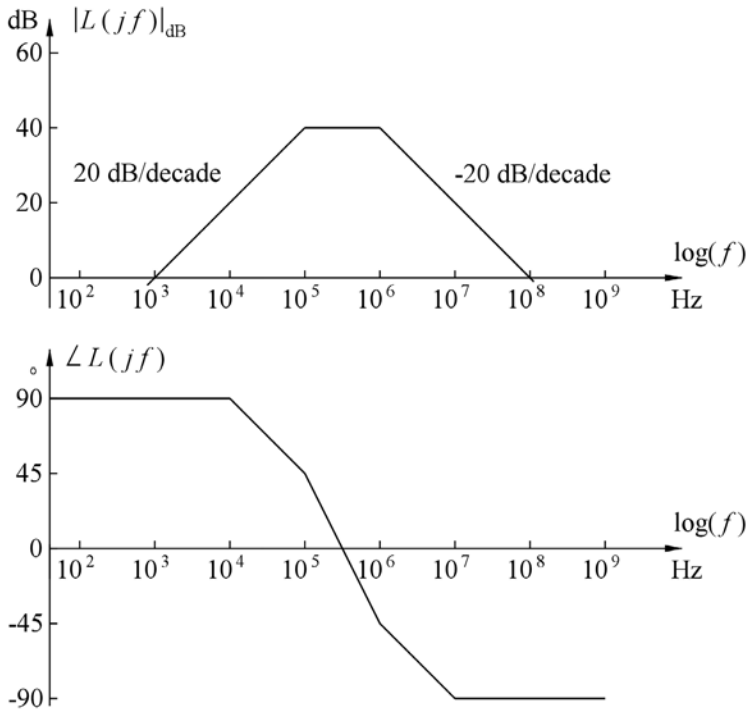
Inserting this in the expression for the loop gain, we find

$$L(s) = \left(\frac{A_0}{1+sA_0/(2\pi\,\text{GBW})}\right)\left(\frac{sRC}{1+sRC}\right)$$

The loop gain has a zero at a frequency of 0, a pole at the frequency $f_{p1} = 100$ kHz and a pole at the frequency $f_{p2} = 1/(2\pi RC) = 0.99$ MHz. At the frequency $f = 100$ MHz, $A_v \sim 0$ dB and $|sRC/(1+sRC)| \sim 0$ dB, so $|L(s)| \sim 0$ dB. We may sketch a Bode plot of $L(jf)$ using a piecewise linear approximation as shown below. From the Bode plot, we estimate $\angle L(jf_t) \simeq -90°$ corresponding to a phase margin of PM = 90°.

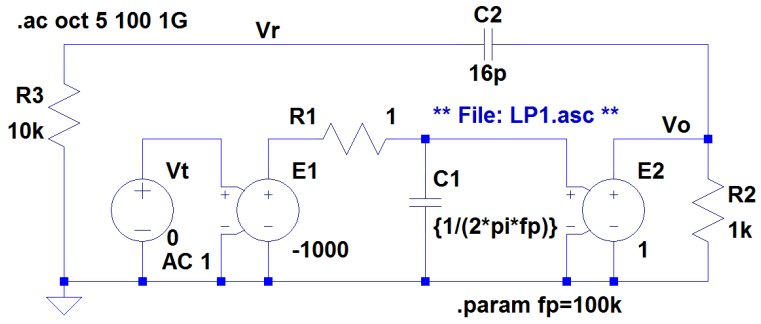
We may also calculate the phase margin using the unity-gain frequency $f_t = 100$ MHz for the loop gain. At $f = f_t = 100$ MHz, we find $\angle L(jf_t) = 90° - \arctan(f_t A_0/\text{GBW}) - \arctan(2\pi f_t RC) = 90° - \arctan 1000 - \arctan 100 = -89.37°$.

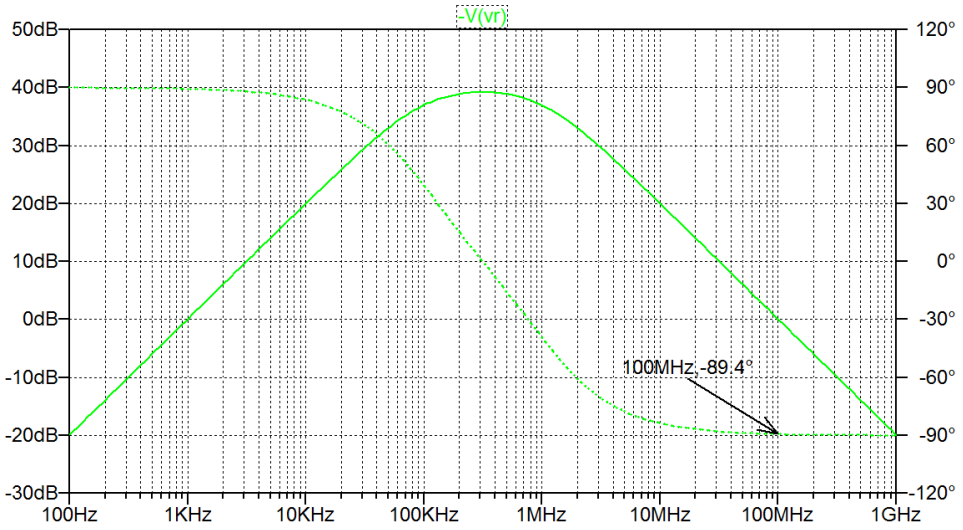
From this, we calculate a phase margin of PM $= 180° + \angle L(jf_t) = 90.63°$.



The loop gain and the phase margin may also be found using LTspice. The following figure is an LTspice schematic for finding the loop gain. The amplifier has been modeled by the filter block '`LP1.asc`' from Tutorial 5.3 in Bruun (2020). By using the gain value -1000 for the controlled voltage source '`E1`, the amplifier is specified to have an inverting low-frequency gain of 1000 V/V. The parameter '`fp`' sets the pole frequency to GBW$/A_0 = 100$ kHz.

Running a '.ac' simulation and plotting '`-V(vr)`', we find the magnitude and the phase of the loop gain. We see that $\angle L(jf) = -89.4°$ for $|L(jf)| = 1 \sim 0$ dB, corresponding to a phase margin of 90.6°.





Problem 6.9

Repeat Problem 6.8, assuming that the opamp has an additional pole at $f_{p2} = 100$ MHz. You may use LTspice to find the phase margin.

Solution:

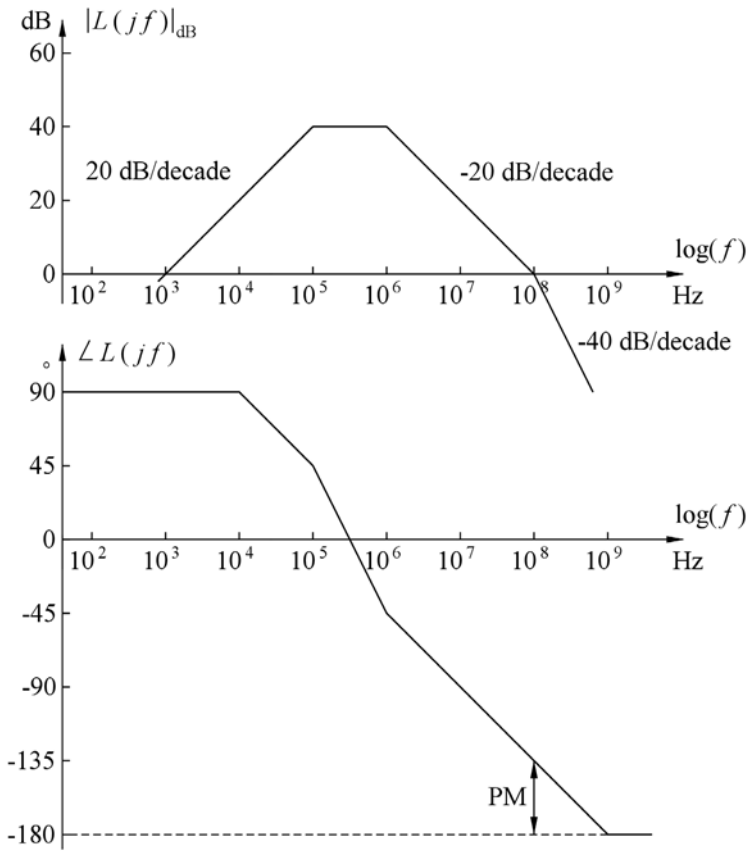
With an additional pole at the frequency $f_{p2} = 100$ MHz in A_v, we have

$$A_v(s) = \frac{A_0}{(1+s/\omega_{p1})(1+s/\omega_{p2})} = \frac{A_0}{(1+sA_0/(2\pi \text{GBW}))(1+s/(2\pi f_{p2}))}$$

resulting in

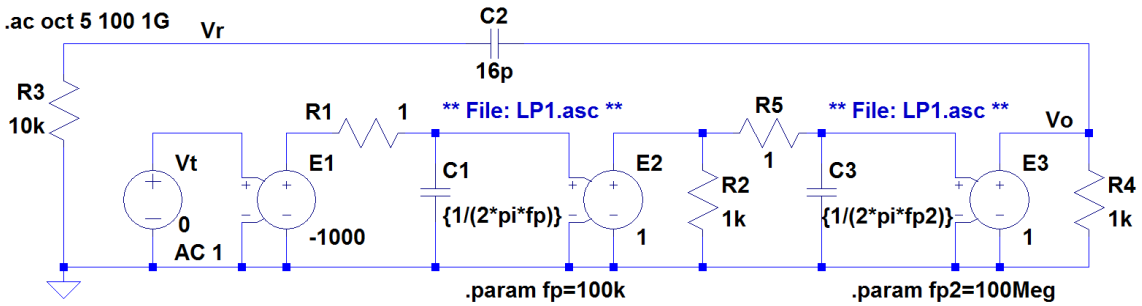
$$L(s) = \left(\frac{A_0}{(1+sA_0/(2\pi \text{GBW}))(1+s/(2\pi f_{p2}))}\right)\left(\frac{sRC}{1+sRC}\right)$$

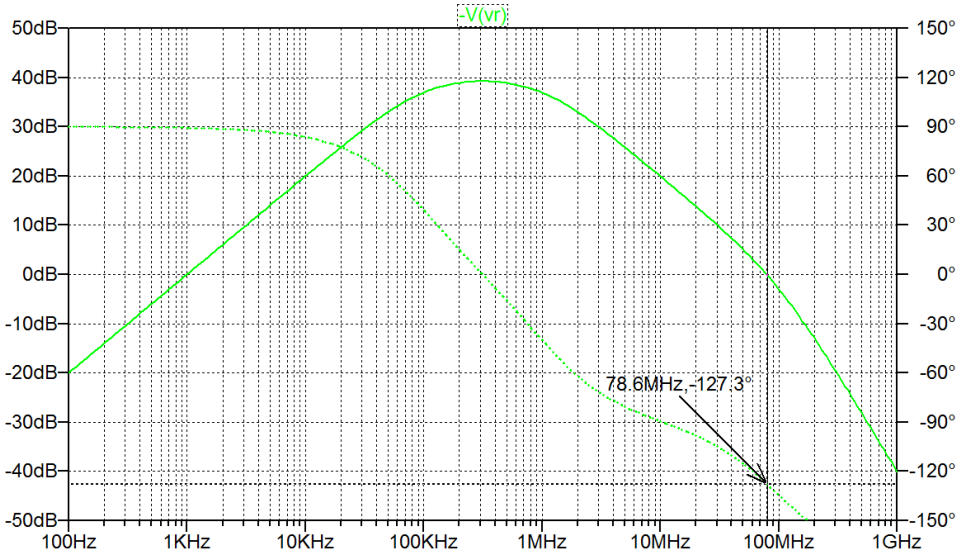
Using a piecewise linear approximation for the Bode plot of $L(jf)$, we arrive at the following plot. It is derived from the plot from Problem 6.8 by introducing an extra breakpoint at $f = 100$ MHz in the gain plot and the corresponding extra phase shift in the phase plot. Using the piecewise linear approximation, we may estimate the unity-gain frequency to be 100 MHz and the phase of $L(jf)$ to be $-135°$ at $f = 100$ MHz, corresponding to a phase margin of 45°. However, the piecewise linear approximation is not very accurate for finding the unity-gain frequency as we find f_t at the breakpoint between two line segments, i.e., at a frequency with maximum deviation from the linear approximation.



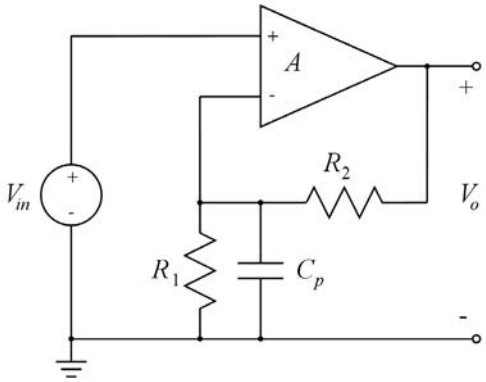
In order to find a more accurate result, we may use LTspice to simulate the loop gain. The following figure shows an LTspice schematic corresponding to the schematic for finding the loop gain. The LTspice schematic from Problem 6.8 has been modified by the insertion of an additional filter block for modeling the second pole with the frequency '`fp2=100Meg`' (Bruun 2020, Tutorial 5.3).

Running a '.ac' simulation and plotting '`-V(vr)`', we find the magnitude and the phase of the loop gain. We find a unity-gain frequency of 78.6 MHz and at this frequency, we find $\angle L(jf) = -127.3°$, corresponding to a phase margin of 52.7°.





Problem 6.10



The figure above shows a feedback amplifier using an opamp with infinite input resistance, an output resistance of 0, and a transfer function with a low-frequency gain of 200 V/V and a single pole at the frequency $f_{p1} = 270$ kHz. The feedback resistors are $R_1 = 50$ kΩ and $R_2 = 400$ kΩ. A parasitic capacitance $C_p = 0.6$ pF is also included as shown.

Sketch a Bode plot of the loop gain and estimate the phase margin. Verify your result using LTspice.

In order to increase the phase margin, a dominant-pole frequency compensation is applied. Find the new pole frequency f'_{p1}, so that a phase margin of 65.5° is obtained. Verify your result using LTspice.

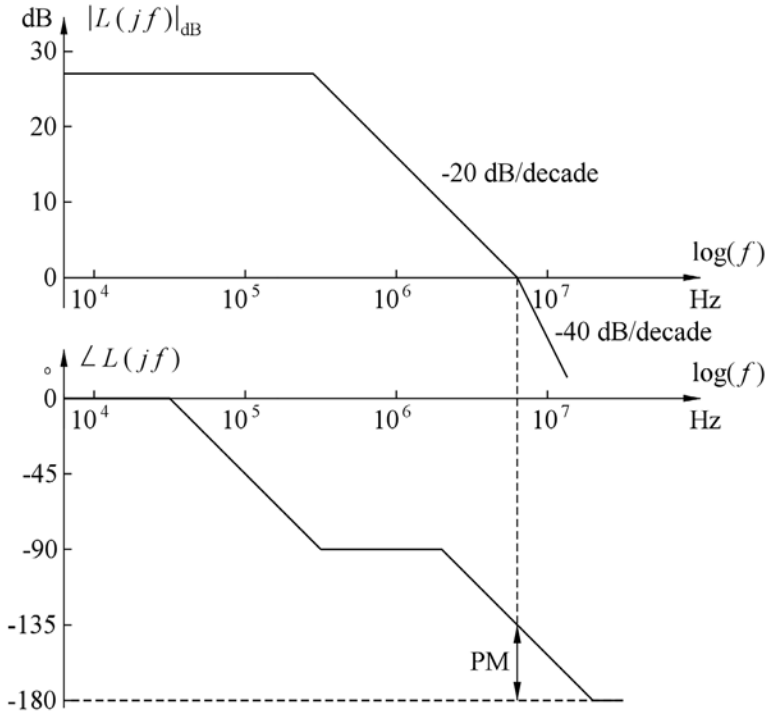
Solution:

The feedback amplifier uses series-shunt feedback with an open-loop gain of $A = \dfrac{A_0}{1 + jf/f_{p1}}$ where $A_0 = 200$ V/V is the low-frequency gain of the opamp.

The feedback factor is $\beta = \dfrac{R_1 \parallel (1/(j2\pi f C_p))}{R_2 + R_1 \parallel (1/(j2\pi f C_p))} = \left(\dfrac{R_1}{R_1 + R_2}\right)\left(\dfrac{1}{1 + j2\pi f (R_1 \parallel R_2) C_p}\right)$.

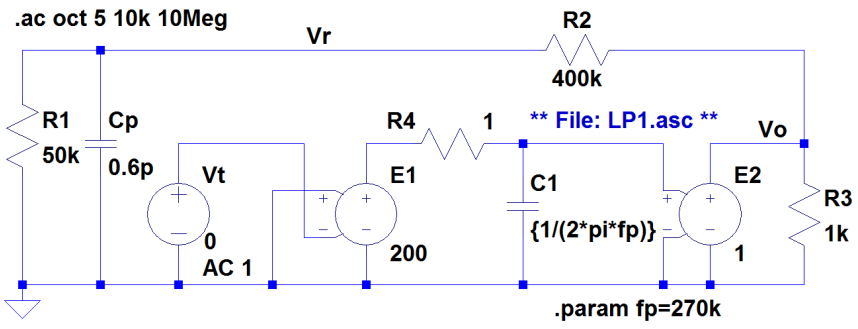
We find the low frequency value of the loop gain as $L_0 = A_0 R_1/(R_1 + R_2) = 22.22$ V/V ~ 26.9 dB, and we find that the loop gain has a pole at the frequency $f_{p1} = 270$ kHz and a pole at the frequency $f_{p2} = 1/(2\pi (R_1 \parallel R_2) C_p) = 5.97$ MHz.

We may sketch a Bode plot of $L(jf)$ using a piecewise linear approximation as shown in the following figure. From the Bode plot, we estimate $\angle L(jf_t) \simeq -135°$ corresponding to a phase margin of 45°. However, the piecewise linear approximation is not very accurate for finding the unity-gain frequency f_t for the loop gain as we find f_t at the breakpoint between two line segments, i.e., at a frequency with maximum deviation from the linear approximation.

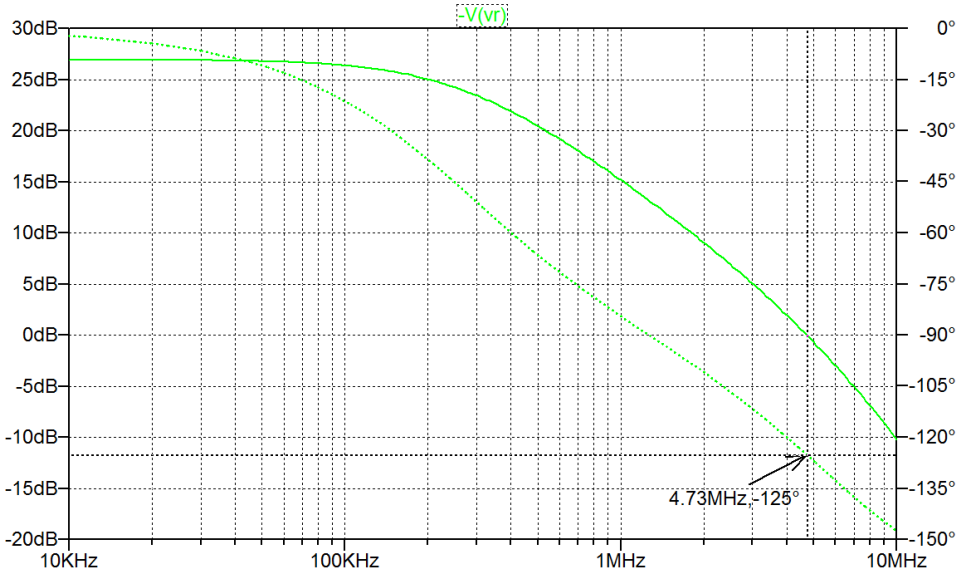


A better estimate can be found by noticing that the gain-bandwidth product $f_{tl} = L_0 f_{p1} = 5.99$ MHz $\simeq f_{p2}$. Using Fig. 6.35(a) in Bruun (2022), we find that for $f_{p2} = f_{tl}$, the phase margin is 52°.

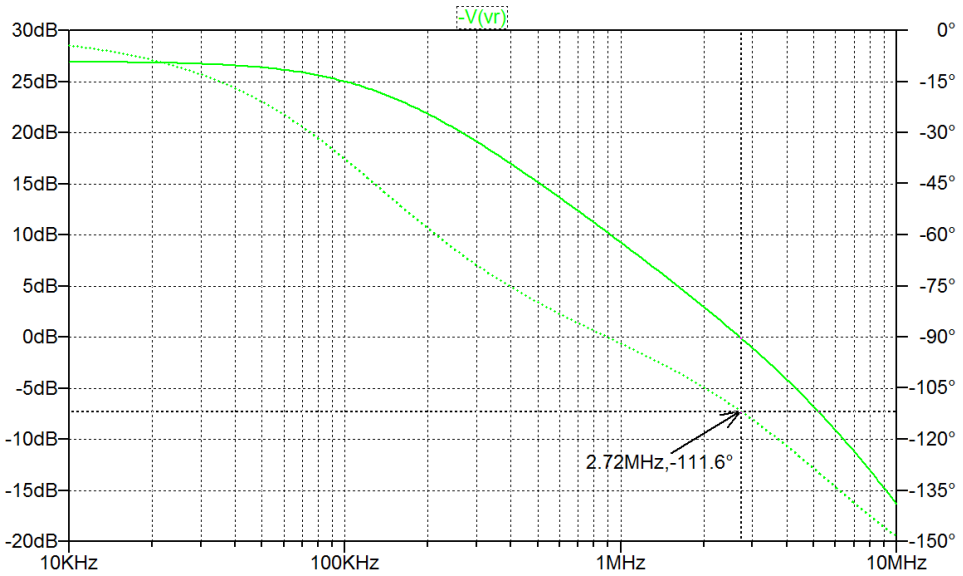
In order to find a more accurate result, we may use LTspice to simulate the loop gain. The following figure shows an LTspice schematic for finding the loop gain. The feedback loop has been broken at the inverting input of the opamp and a test voltage '`Vt`' has been applied to the inverting input while the noninverting input has been grounded, corresponding to a resetting of the input voltage V_{in}. The opamp has been modeled by the filter block '`LP1.asc`' from Tutorial 5.3 in Bruun (2020). By using the gain value 200 for the controlled voltage source '`E1`, the amplifier is specified to have a low-frequency gain of 200 V/V. The parameter '`fp`' sets the pole frequency to 270 kHz.



Running a '.ac' simulation and plotting '`-V(vr)`' we find the magnitude and the phase of the loop gain. We find a unity-gain frequency of 4.73 MHz and at this frequency, we find $\angle L(jf) = -125°$, corresponding to a phase margin of 55°. This is about 3° more than the estimate from Fig. 6.35(a) in Bruun (2022). The reason for this is that the phase shift from the first pole is less than 90° by the amount $\arctan(f_{p1}/f_t) = \arctan(0.27/4.73) \simeq 3°$.



For a second-order system with a phase margin of 65.5°, the ratio between the frequency of the second pole and the gain-bandwidth product of the loop gain should be $f_{p2}/f_{tl} = 2$ (Bruun 2022). The second pole frequency is $f = f_{p2} = 1/(2\pi(R_1 \parallel R_2)C_p) = 5.97$ MHz, so the pole in the opamp must be reduced such that $f'_{p1}L_0 = 5.97$ MHz$/2 = 2.98$ MHz, and with $L_0 = 22.22$ V/V, we find $f'_{p1} = 134$ kHz. Changing the parameter '`fp`' in the LTspice schematic to '`134k`' and running a new '.ac' simulation, we find the following loop gain.



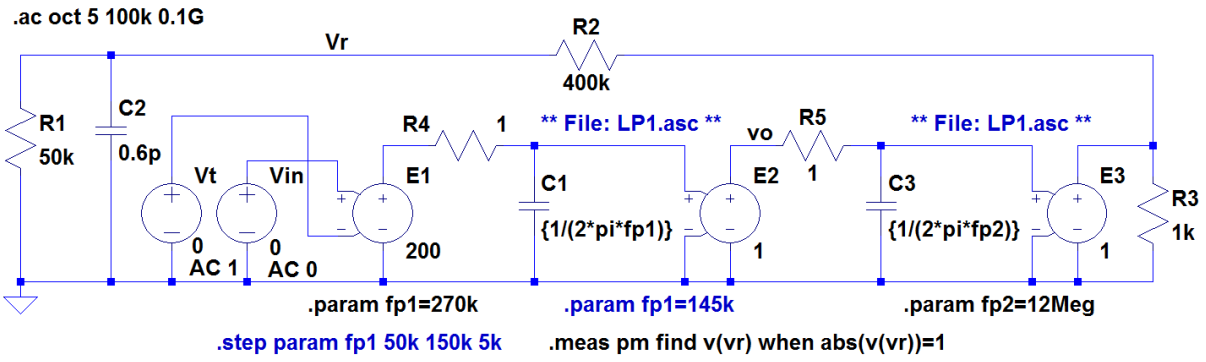
We find a unity-gain frequency of 2.72 MHz and at this frequency, we find $\angle L(jf) = -111.6°$, corresponding to a phase margin of 68.4°. This is about 2.9° more than requested. The reason for the additional phase margin is that the relation $f_{p2}/f_{tl} = 2$ is for a system where the first pole is at a frequency of 0, such that the phase shift caused by the first pole is −90°. With the first pole at 134 kHz, the phase shift at $f_t = 2.72$ MHz is $\angle L(jf_t) = -\arctan(2.72/0.134) = -87.1°$ corresponding to an extra phase margin of 2.9°. Thus, we may increase the frequency f'_{p1} slightly and still obtain a phase margin of 65.5°. A few iterations with LTspice shows that a phase margin of 65.5° is achieved with $f'_{p1} = 145$ kHz.

Problem 6.11

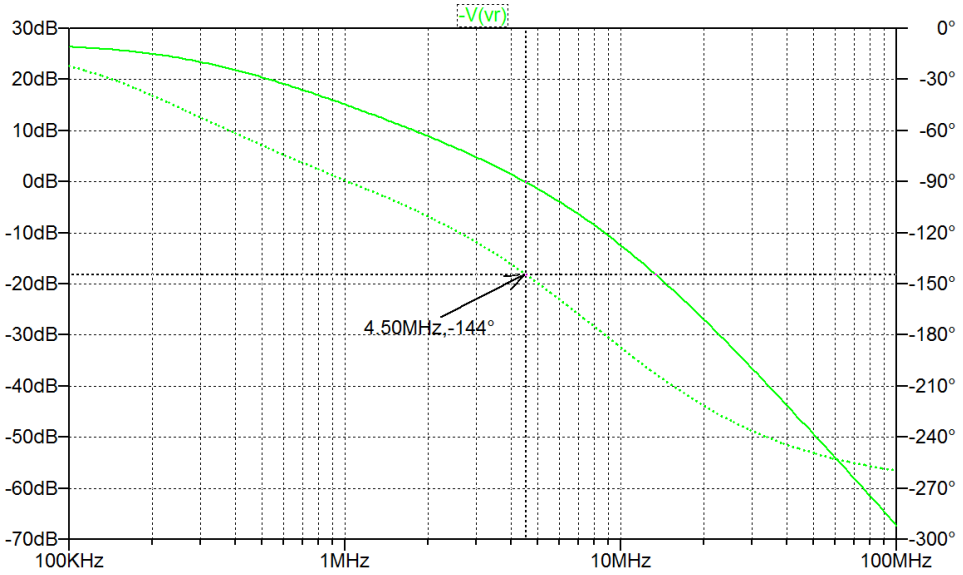
Assume now that the amplifier shown in Problem 6.10 has an additional pole at the frequency $f_{p2} =$ 12 MHz.
Find the phase margin when the dominant pole of the amplifier is located at $f_{p1} = 270$ kHz.
Find the phase margin when the dominant pole of the amplifier is located at the frequency f'_{p1} found in Problem 6.10 to give a phase margin of 65.5° for the single-pole amplifier.
Find the dominant-pole frequency required for a phase margin of 65.5° when using the two-pole amplifier with a dominant-pole compensation which leaves the frequency of the non-dominant pole unchanged at 12 MHz. You may use LTspice for solving this problem.

Solution:

For solving the problem, we modify the LTspice schematic from Problem 6.10 as shown below. An additional filter stage has been inserted and the parameter specification for '`fp1`' has been extended to include both the frequencies 270 kHz and 145 kHz (shown as a comment). Also a step directive for '`fp1`' has been inserted (shown as a comment) and a '.meas' directive for finding the phase margin has been included.

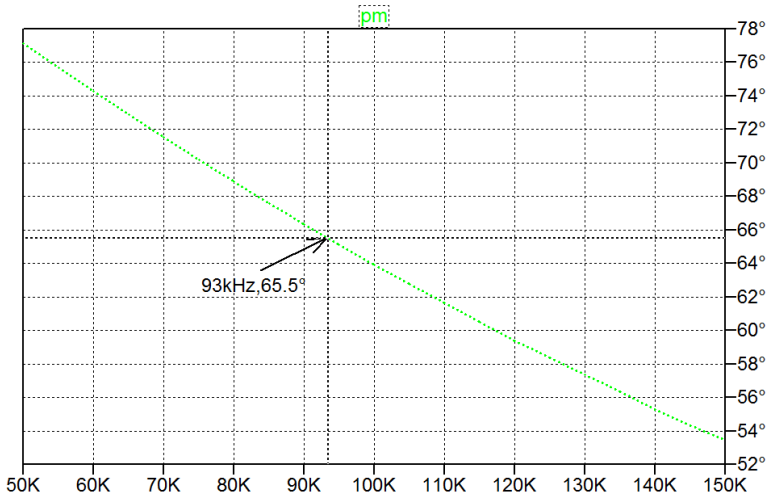


First we run a '.ac' simulation with $f_{p1} = 270$ kHz. Plotting '`-V(vr)`', we find the magnitude and the phase of the loop gain shown below. From the plot, we find a unity-gain frequency of $f_t = 4.50$ MHz and at this frequency, we find $\angle L(jf) = -144°$, corresponding to a phase margin of 36°. From the error log file, we also find the phase margin to be 36°. We notice that the loop gain has a gain-bandwidth product of $f_{tl} = f_{p1}A_0R_1/(R_1 + R_2) \simeq 6.0$ MHz, a second pole at the frequency $f_{p2} = 1/(2\pi(R_1 \parallel R_2)C_p) \simeq$ 6.0 MHz and a third pole at the frequency $f_{p3} = 12$ MHz. Thus, $f_{p2}/f_{tl} = 1$ and $f_{p3}/f_{tl} = 2$, and from Fig. 6.41 in Bruun (2022), we may estimate the phase margin to be approximately 33°. As for the circuit in Problem 6.10, an additional margin of 3° is found by the simulation because the phase shift from the first pole is less than 90° by the amount $\arctan(f_{p1}/f_t) = \arctan(0.27/4.73) \simeq 3°$.

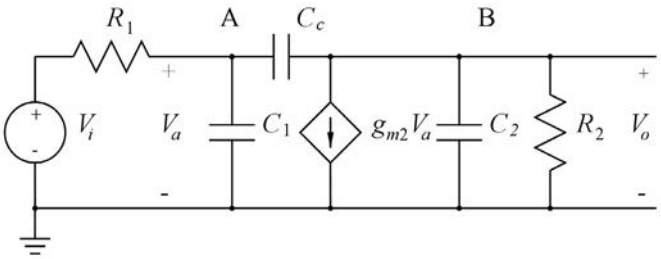


Repeating the simulation with $f_{p1} = 145$ kHz as found in Problem 6.10, we find a unity-gain frequency of $f_t = 2.84$ MHz and at this frequency, we find $\angle L(jf) = -126°$, corresponding to a phase margin of 54° as also found from the error log file. For $f_{p1} = 145$ kHz, we have $f_{tl} = f_{p1}A_0R_1/(R_1+R_2) = 3.22$ MHz, so $f_{p2}/f_{tl} = 1.86$ and $f_{p3}/f_{tl} = 3.72$. Using Fig. 6.41 in Bruun (2022), we may estimate the phase margin to be about 51°, and adding 3° from $\arctan(f_{p1}/f_t)$, we find a very good match to the simulated value.

For finding the value of f_{p1} required for a phase margin of 65.5°, we use the '.step' directive for f_{p1} shown as a comment in the LTspice schematic. From the error log file, we use a right-click to open a plot of the phase margin versus f_{p1}. The plot is shown below, and we find $f_{p1} = 93$ kHz for a phase margin of 65.5°. With $f_{p1} = 93$ kHz, we have $f_{tl} \simeq 2.0$ MHz, so $f_{p2}/f_{tl} = 3$ and $f_{p3}/f_{tl} = 6$, and from Fig. 6.41 in Bruun (2022), we may estimate the phase margin to be approximately 63°, and adding 3° from $\arctan(f_{p1}/f_t)$, again we find a very good match to the simulated value.



Problem 6.12



$R_1 = 200$ kΩ, $R_2 = 100$ kΩ, $C_1 = 0.16$ pF, $C_2 = 0.08$ pF, $C_c = 0.71$ pF and $g_{m2} = 0.1$ mA/V.

For the amplifier shown above, assume the device values listed with the figure. These values are the same as those used for the simulations in Figs. 6.57 and 6.58.
Use node equations for node A and node B to find exact values for the pole frequencies and the zero frequency of the amplifier and compare the calculated values to the simulated values and the values calculated when using the expressions given by Eqs. (6.54), (6.59), (6.60) and (6.62).

Solution:

In order to find poles and zeros for this configuration, we use node equations for the nodes A and B.

$$\begin{aligned} \text{Node A:} \quad (V_a - V_1)/R_1 + V_a\,sC_1 + (V_a - V_o)\,sC_c &= 0 \\ \text{Node B:} \quad (V_o - V_a)\,sC_c + g_{m2}V_a + V_o/R_2 + V_o\,sC_2 &= 0 \end{aligned}$$

Rearranging, we find

$$\begin{aligned} \text{Node A:} \quad V_a(1/R_1 + s(C_1 + C_C)) - V_o\,sC_c &= V_1/R_1 \\ \text{Node B:} \quad V_a(g_{m2} - sC_c) + V_o(1/R_2 + s(C_2 + C_c)) &= 0 \end{aligned}$$

From these equations, we find the transfer function

$$\frac{V_o}{V_1} = \frac{-(g_{m2} - sC_c)R_1}{(1/R_1 + s(C_1 + C_c))(1/R_2 + s(C_2 + C_c)) + sC_c(g_{m2} - sC_c)}$$

From the numerator, we identify a right-half-plane zero at the frequency

$$\omega_z = \frac{g_{m2}}{C_c}$$

For finding the poles, we must solve the equation

$$\begin{aligned} & (1/R_1 + s(C_1 + C_c))(1/R_2 + s(C_2 + C_c)) + sC_c(g_{m2} - sC_c) = 0 \\ \Rightarrow \quad & (C_1C_2 + C_1C_c + C_2C_c)s^2 + ((C_2 + C_c)/R_1 + (C_1 + C_c)/R_2 + g_{m2}C_c)s + 1/(R_1R_2) = 0 \end{aligned}$$

This is a quadratic equation with two solutions, $s = -\omega_{p1}$ and $s = -\omega_{p2}$ where we assume that $f_{p1} = \omega_{p1}/(2\pi)$ is the frequency of the dominant pole and $f_{p2} = \omega_{p2}/(2\pi)$ is the frequency of the non-dominant pole.

Introducing $A = C_1C_2 + C_1C_c + C_2C_c$, $B = (C_2 + C_c)/R_1 + (C_1 + C_c)/R_2 + g_{m2}C_c$ and $C = 1/(R_1R_2)$, we find the solutions

$$f_{p1} = \frac{B - \sqrt{(B^2 - 4AC)}}{2\pi 2A}$$
$$f_{p2} = \frac{B + \sqrt{(B^2 - 4AC)}}{2\pi 2A}$$

Inserting numerical values, we find $f_{p1} = 95.3$ kHz, $f_{p2} = 72.6$ MHz and $f_z = 22.4$ MHz. From the simulations shown in Figs. 6.57 and 6.58, we find $f_{p1} = 96$ kHz, $f_{p2} = 72.9$ MHz and $f_z = 22.5$ MHz, i.e., an almost perfect match.
Using Eqs. (6.62), (6.59) and (6.54), we find $f_{p1} = 100$ kHz, $f_{p2} = 61.7$ MHz and $f_z = 22.4$ MHz, i.e., a perfect match for f_z and a match within about 15% for the pole frequencies.
Using Eq. (6.60), we find $f_{p1} = 112$ kHz, i.e., a worse match than obtained by Eq. (6.62).

References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Bruun, E. 2020, *CMOS Integrated Circuit Simulation with LTspice*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-integrated-circuit-simulation-with-ltspice-ebook

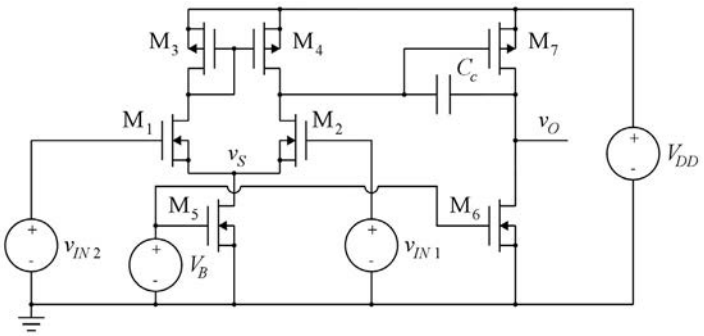
Chapter 7 – The Two-Stage Opamp

Multiple-choice test

1. Completed statements:

A-3:	The gain-bandwidth product of a Miller-compensated two-stage opamp is given by the ratio between the transconductance of the input transistors and the compensation capacitor.
B-9:	A Miller-compensated two-stage opamp has a right-half-plane zero at a frequency given by the ratio between the transconductance of the second-stage gain transistor and the compensation capacitor.
C-15:	The frequency of the right-half-plane zero in a Miller-compensated two-stage opamp may be pushed to a higher frequency relative to the gain-bandwidth product by increasing the transconductance of the second-stage gain transistor.
D-2:	When the compensation capacitor in a Miller-compensated two-stage opamp is increased, the phase margin is increased.
E-2:	When the feedback factor for an opamp with feedback is reduced, the phase margin is increased.
F-2:	When the channel-width-to-length ratio of the bias transistor providing the tail current to the input stage is decreased, the input voltage range is increased.
G-5:	When the load capacitor in a Miller-compensated two-stage opamp is increased, the phase margin is decreased.
H-5:	When the compensation capacitor in a Miller-compensated two-stage opamp is increased, the slew rate is decreased.
I-6:	The channel-width-to-length ratio for the transistors forming the active load to the differential input pair is designed from a scaling of the second-stage gain transistor and the bias currents in the input stage and the second stage.

2. The amplifier shown below has a supply voltage of $V_{DD} = 1.8$ V, and the absolute value of the overdrive voltage is 0.2 V for all transistors. All NMOS transistors have a threshold voltage of 0.40 V without bulk effect and all PMOS transistors have a threshold voltage of -0.42 V without bulk effect. The bias current in M_5 and M_6 is $I_{D5} = I_{D6} = 0.1$ mA.



The minimum value of the common-mode input voltage with all transistors in the active region is

A: 0.2 V

B: 0.6 V

C: 0.8 V

Solution:

The minimum common-mode input voltage is $v_{ICM\min} = v_{DS\,\mathrm{sat}5} + V_{GS1} = v_{DS\,\mathrm{sat}5} + V_{t1} + V_{DS\,\mathrm{sat}1} = 0.8$ V.

3. The bias voltage V_B for the amplifier shown above has a value of

A: 0.2 V

B: 0.6 V

C: 0.8 V

Solution:

The bias voltage V_B is $V_B = V_{GS5} = V_{t5} + V_{DS\,\mathrm{sat}5} = 0.6$ V.

4. The maximum value of the common-mode input voltage for the amplifier shown above with all transistors in the active region is

A: 1.58 V

B: 1.60 V

C: 1.81 V

Solution:

The maximum common-mode input voltage is
$v_{ICM\max} = V_{DD} - |V_{GS3}| - V_{DS\,\mathrm{sat}1} + V_{GS1} = V_{DD} - |V_{t3}| - |V_{DS\,\mathrm{sat}3}| + V_{t1} = 1.58$ V.

5. Assume now that M_1 and M_2 in the amplifier above has bulk connected to ground rather than to source, causing their threshold voltage to increase to 0.63 V. The maximum value of the common-mode input voltage for the amplifier shown above with all transistors in the active region is now

A: 1.58 V

B: 1.60 V

C: 1.81 V

Solution:

The maximum common-mode input voltage is increased by the increase in V_{t1}, i.e.,
$v_{ICM\max} = V_{DD} - |V_{GS3}| - V_{DS\,\mathrm{sat}1} + V_{GS1} = V_{DD} - |V_{t3}| - |V_{DS\,\mathrm{sat}3}| + V_{t1} = 1.81$ V.

6. In order to achieve a gain-bandwidth product of 20 MHz for the amplifier shown above, the capacitor C_c should have a value of approximately

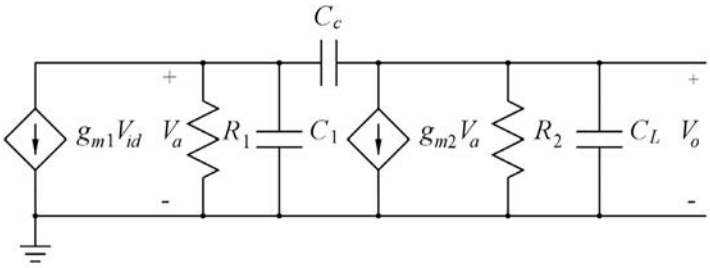
   A: 4 pF
   B: 8 pF
   C: 25 pF

Solution:

The gain-bandwidth product is approximately GBW $\simeq g_{m1}/(2\pi C_c)$ and $g_{m1} = 2I_{D1}/V_{DS\,\mathrm{sat1}} = I_{D5}/V_{DS\,\mathrm{sat1}}$ $= 0.5$ mA/V. From this, we find $C_c \simeq g_{m1}/(2\pi\,\mathrm{GBW}) = 4$ pF.

Problems

Problem 7.1



The amplifier shown above is to be used in a feedback amplifier with the feedback factor $\beta = 1$. The transfer function V_o/V_{id} where V_{id} is a differential input voltage has a zero at the frequency ω_z and a non-dominant pole at ω_{p2}, and the gain-bandwidth product is ω_{ta}. You may assume $g_{m1}R_1 \gg 1$ and $g_{m2}R_2 \gg 1$.

Find a relation between g_{m1} and g_{m2} so that $\omega_z \simeq 10\,\omega_{tl}$ where ω_{tl} is the gain-bandwidth product of the loop gain. Also find an expression for C_c as a function of g_{m1}, g_{m2}, C_1 and C_L so that $\omega_{p2} \simeq 2\,\omega_{tl}$.

Hint: Use Eq. (7.11).

With $g_{m1} = 0.5$ mA/V, $C_L = 5$ pF and $C_1 = 1.7$ pF, calculate g_{m2} and C_c so that $\omega_z \simeq 10\,\omega_{tl}$ and $\omega_{p2} \simeq 2\,\omega_{tl}$ and use LTspice to find phase margin and bandwidth for the feedback amplifier.

Solution:

Assuming $C_1 \ll C_c g_{m2} R_2$ and a dominant pole from the input node, we find using the Miller approximation

$$\omega_{p1} \simeq \frac{1}{R_1 C_c g_{m2} R_2}$$

and with the low-frequency gain $A_0 \simeq g_{m1}R_1 g_{m2}R_2$, this results in $\omega_{ta} \simeq g_{m1}/C_c$.

With $\beta = 1$, we find $\omega_{tl} = \beta\,\omega_{ta} \simeq g_{m1}/C_c$.

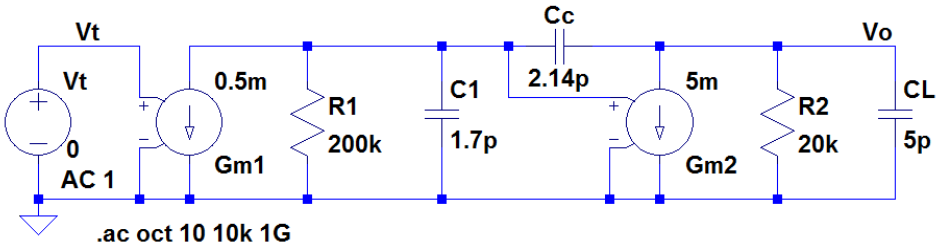
The zero caused by C_c is given by $\omega_z = g_{m2}/C_c$, compare to Eq. (6.54) in Bruun (2022). Thus,

$$\omega_z \simeq 10\,\omega_{tl} \Rightarrow \frac{g_{m2}}{C_c} \simeq 10\,\frac{g_{m1}}{C_c} \Rightarrow g_{m2} \simeq 10\,g_{m1}.$$

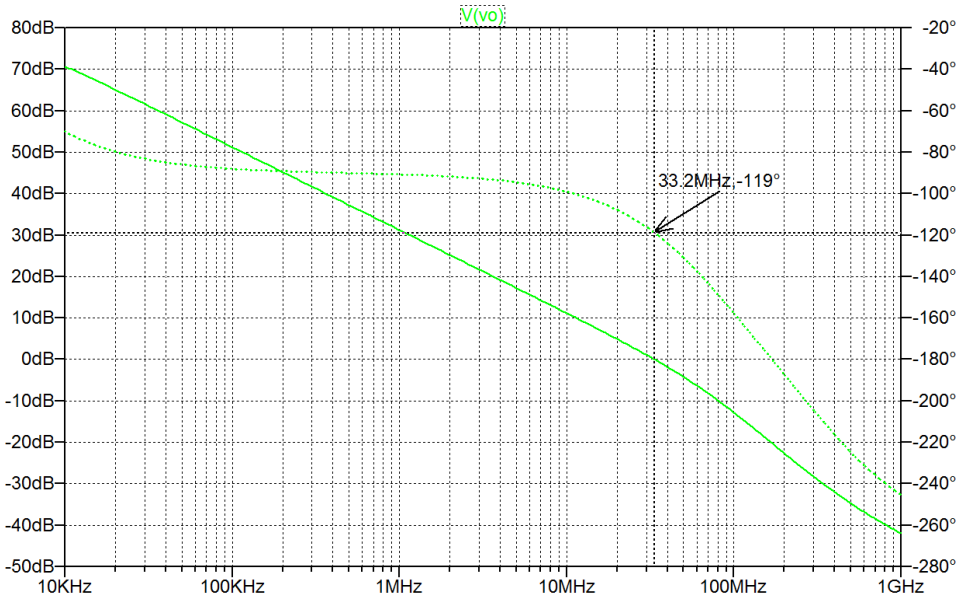
Using Eq. (7.11) from Bruun (2022) with $C_2 = C_L$, $\beta = 1$, $\omega_{p2} = 2\,\omega_{tl}$ and g_{m7} replaced by g_{m2}, we find

$$\begin{aligned}
\frac{C_c}{C_L} &= \frac{1+\frac{C_1}{C_L}+\sqrt{\left(1+\frac{C_1}{C_L}\right)^2+2\left(\frac{g_{m2}}{g_{m1}}\right)\left(\frac{C_1}{C_L}\right)}}{\left(\frac{g_{m2}}{g_{m1}}\right)} \\
\Rightarrow C_c &= \left(\frac{g_{m1}}{g_{m2}}\right)\left(C_1+C_L+\sqrt{(C_1+C_L)^2+2\left(\frac{g_{m2}}{g_{m1}}\right)C_1C_L}\right)
\end{aligned}$$

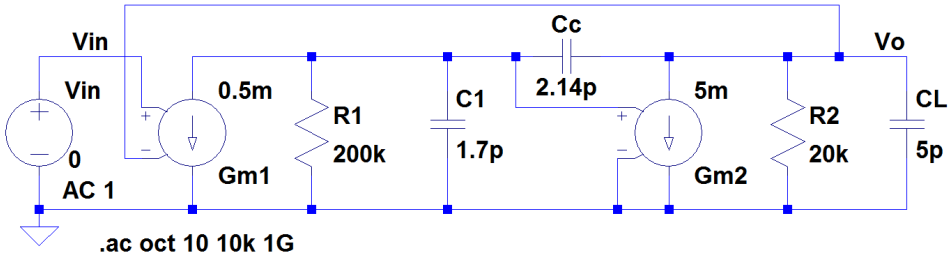
With $g_{m1} = 0.5$ mA/V, we find $g_{m2} = 10\,g_{m1} = 5.0$ mA/V. Using $C_L = 5$ pF and $C_1 = 1.7$ pF, we find $C_c = 2.14$ pF. These values are inserted in the LTspice schematic shown below. In order to fulfill $g_{m1}R_1 \gg 1$, we select $R_1 = 100/g_{m1} = 200$ kΩ, and in order to fulfill $g_{m2}R_2 \gg 1$, we select $R_2 = 100/g_{m2} = 20$ kΩ.

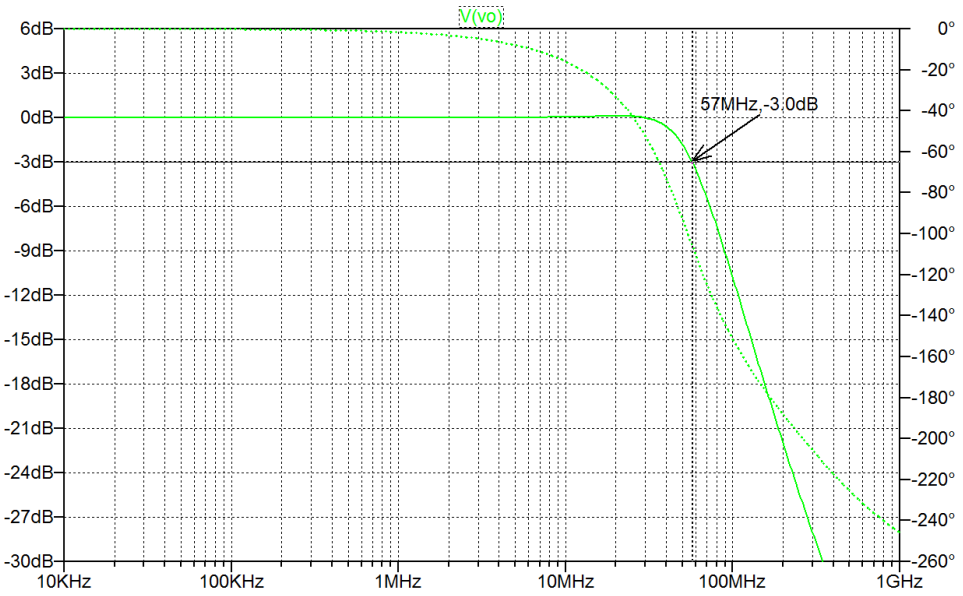


Running a '.ac' simulation results in the frequency response of the loop gain shown below from which we find a phase margin of 61°.



For finding the bandwidth of the feedback amplifier, we close the feedback loop as shown in the LTspice schematic below and run a new '.ac' simulation. From the '.ac' simulation, we find a bandwidth of 57 MHz.



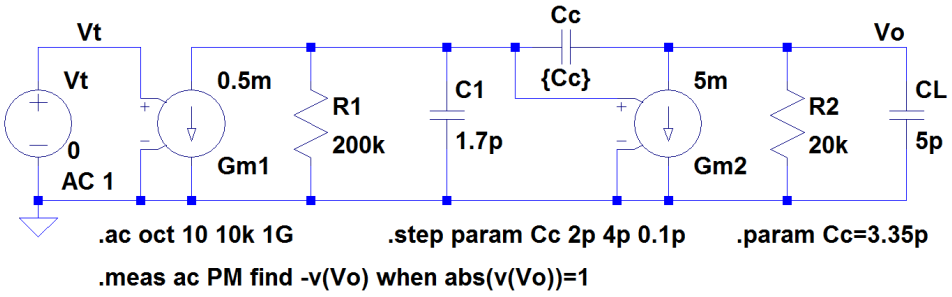


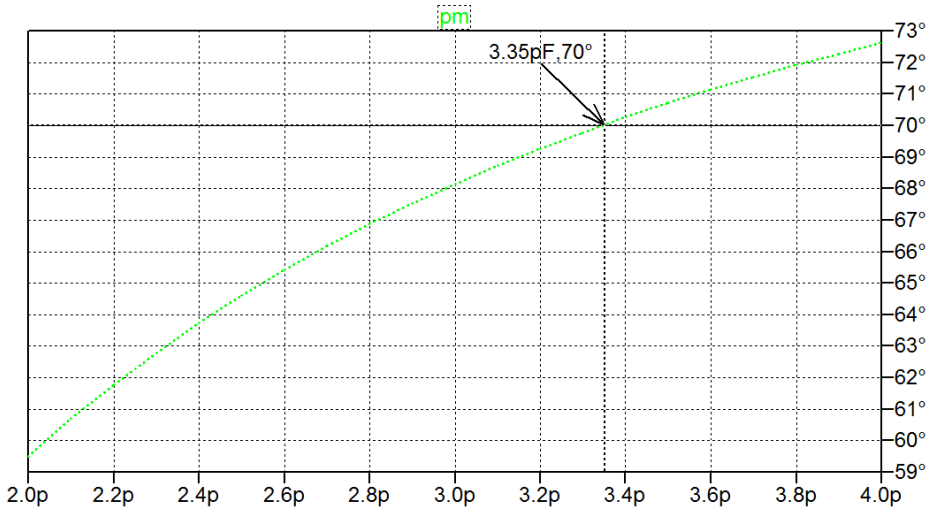
Problem 7.2

Redesign the circuit from Problem 7.1 to have a phase margin of 70° by increasing the value of C_c. Find the new value of C_c and find the bandwidth of the modified circuit.

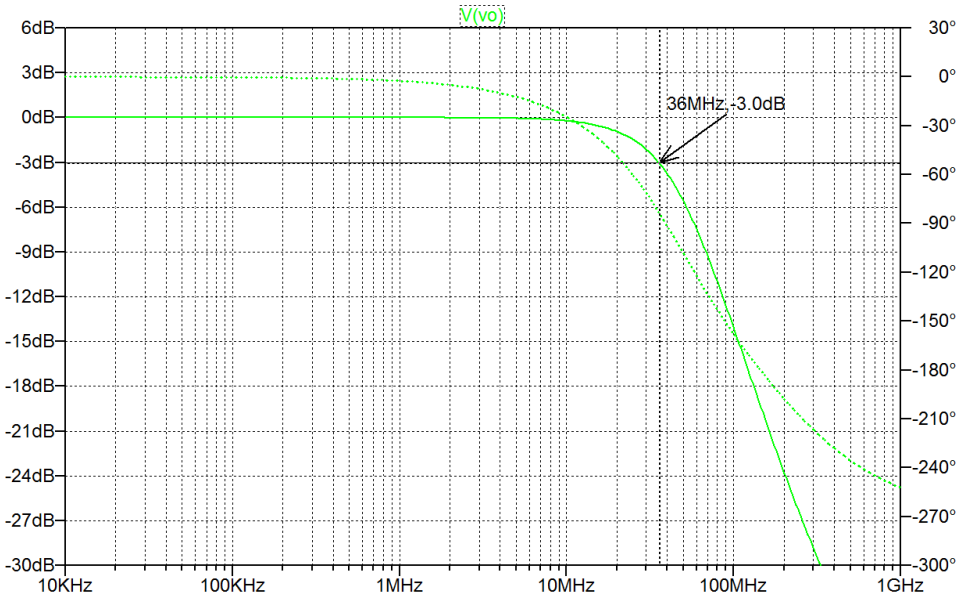
Solution:

An increase of the phase margin requires an increase of ω_{p2}/ω_{t1}. This may be achieved by an increase in C_c as seen from Eq. (7.10) in Bruun (2022). The value of C_c required for a phase margin of 70° may be found from an LTspice simulation where C_c is defined as a parameter stepped through a reasonable interval. Using a '.meas' directive, the phase margin may be calculated by LTspice for each value of C_c, compare to Bruun (2020, Tutorial 6.3). The calculated values of the phase margin are found in the error log file from a '.ac' simulation, and using a left-click on the mouse, you may plot the phase margin versus the capacitor C_c. The following figures show the LTspice schematic for the simulation and the plot of the phase margin versus the capacitor C_c. From the plot, we find $C_c = 3.35$ pF for a phase margin of 70°.





For finding the bandwidth, we close the feedback loop as shown in the LTspice schematic for Problem 7.1 and run a new '.ac' simulation. For this, the value of C_c is defined by a '.param' directive and the '.step' directive is deleted or changed into a comment. Shown below is the output plot from the '.ac' simulation. From the '.ac' simulation, we find a bandwidth of 36 MHz.

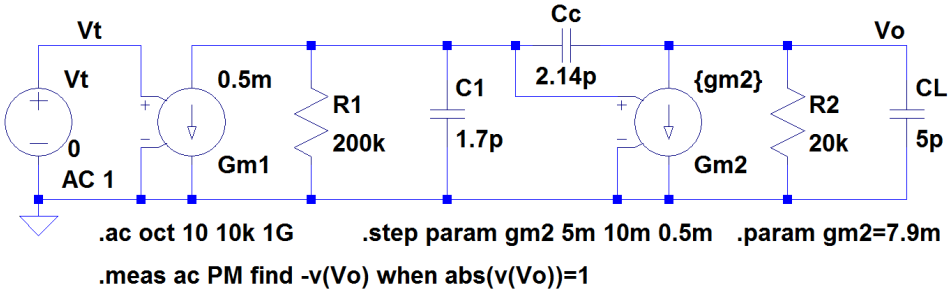


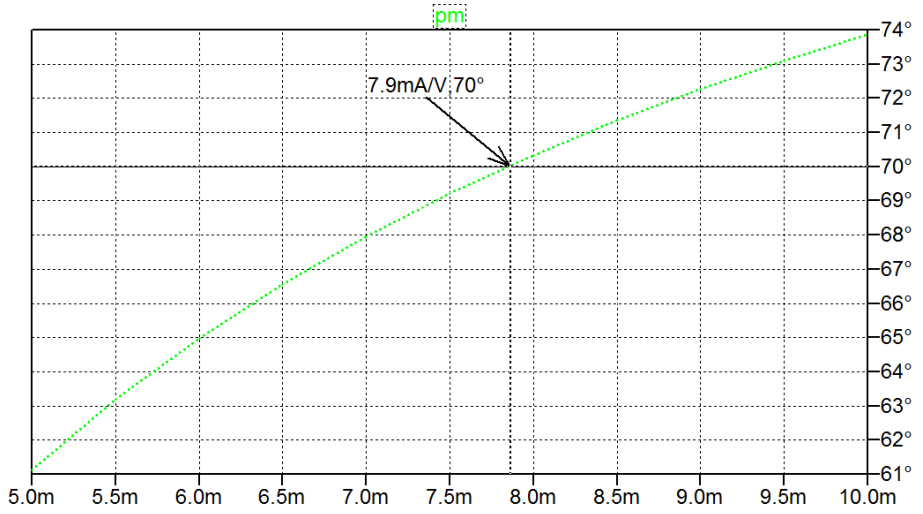
Problem 7.3

Redesign the circuit from Problem 7.1 to have a phase margin of 70° by increasing the value of g_{m2}. Find the new value of g_{m2} and find the bandwidth of the modified circuit.

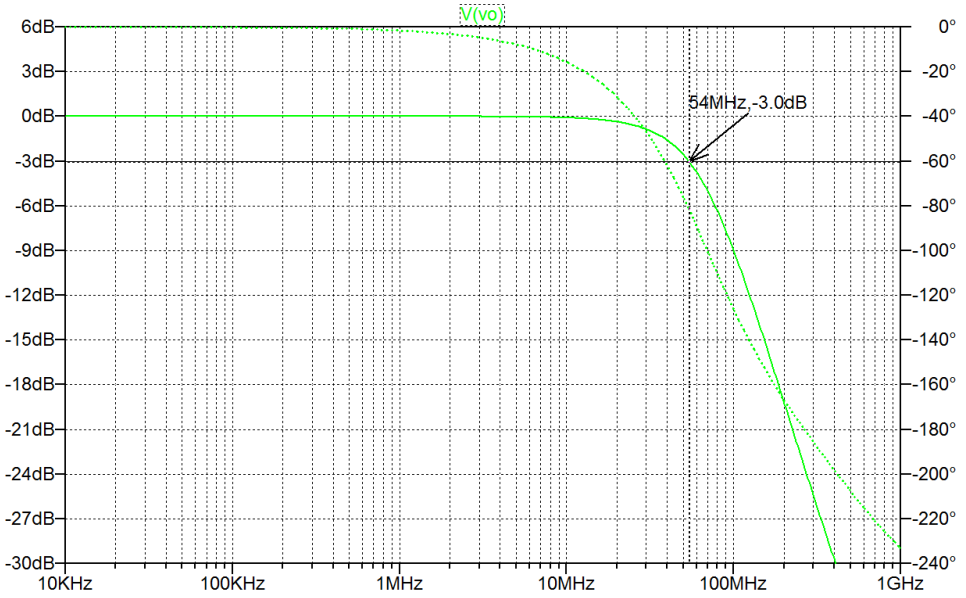
Solution:

An increase of the phase margin requires an increase of ω_{p2}/ω_{tl}. This may be achieved by an increase in g_{m2} as seen from Eq. (7.10) in Bruun (2022). The value of g_{m2} required for a phase margin of 70° may be found from an LTspice simulation where g_{m2} is defined as a parameter stepped through a reasonable interval. Using a '.meas' directive, the phase margin may be calculated by LTspice for each value of g_{m2}, compare to Bruun (2020, Tutorial 6.3). The calculated values of the phase margin are found in the error log file from a '.ac' simulation, and using a left-click on the mouse, you may plot the phase margin versus the transconductance g_{m2}. Shown below is the LTspice schematic for the simulation and the plot of the phase margin versus the transconductance g_{m2}. From the plot, we find $g_{m2} = 7.9$ mA/V for a phase margin of 70°.

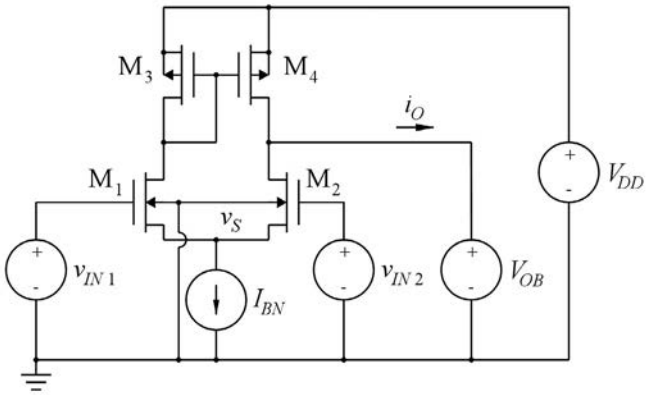




For finding the bandwidth, we close the feedback loop as shown in the LTspice schematic for Problem 7.1 and run a new '.ac' simulation. For this, the value of g_{m2} is defined by a '.param' directive and the '.step' directive is deleted or changed into a comment. The following figure shows the output plot from the '.ac' simulation. From the '.ac' simulation, we find a bandwidth of 54 MHz. We notice that the bandwidth is larger than the bandwidth found in Problem 7.2. This is achieved because ω_{tl} is not reduced by the increase of ω_{p2}/ω_{tl} as it is by the increase of C_c.



Problem 7.4

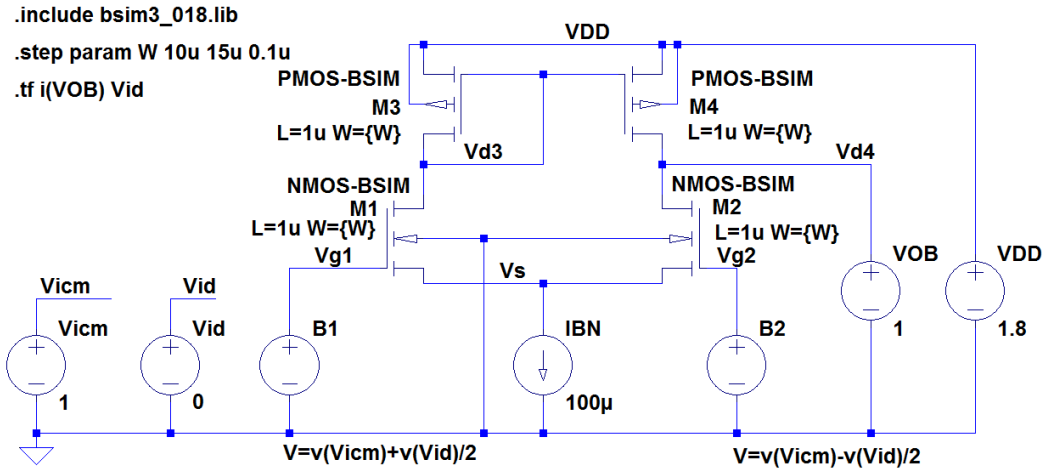


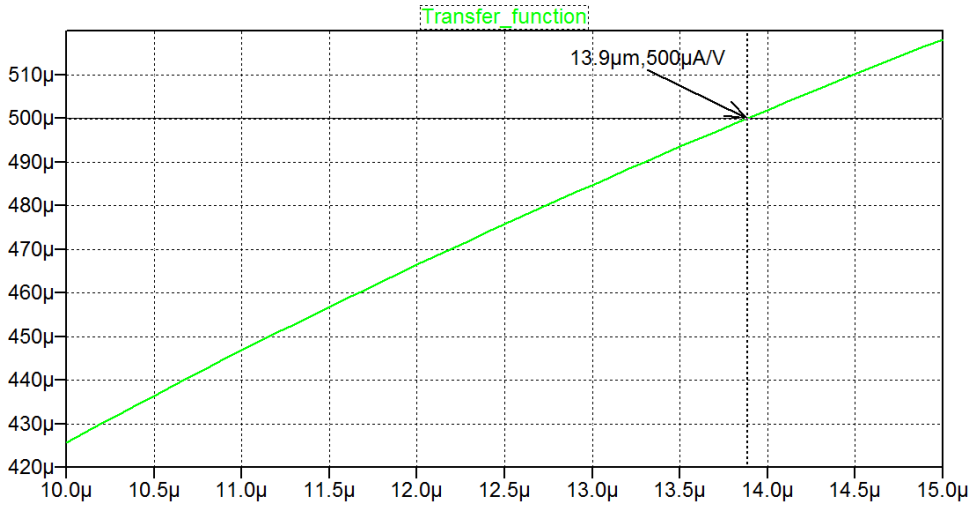
For the differential gain stage shown above, assume $V_{DD} = 1.8$ V, $V_{OB} = 1.0$ V and $I_{BN} = 0.1$ mA. Also, all transistors have a channel length of $L = 1$ µm and they all have the same channel width W.
Design the transistors M_1 and M_2 to provide a transconductance $g_m = i_o/v_{id} = 0.5$ mA/V where $v_{ID} = v_{IN1} - v_{IN2}$.
Assume a common-mode input voltage of 1 V and use the BSIM3 transistor models shown in Fig. 3.44.

For convenience, Fig. 3.44 is shown in the Appendix in this book.

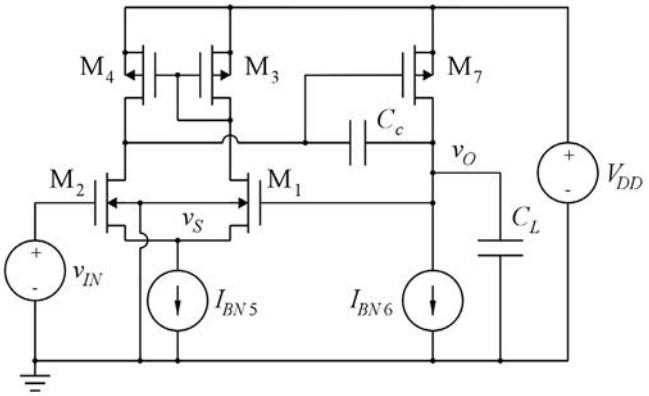
Solution:

Shown below is an LTspice schematic corresponding to Problem 7.4. The channel width W of the transistors has been defined as a parameter W which is stepped through a suitable interval of values. Using arbitrary behavioral voltage sources, the input voltages are modeled as the sum of a common-mode input voltage '`Vicm`' and a contribution from the differential input voltage '`Vid`'. The transconductance $g_m = i_o/v_{id}$ is found as the transfer function from a '.tf' simulation with '`i(VOB)`' as the output and the differential input voltage '`Vid`' as the input. From the '.tf' simulation, we may plot the transfer function versus the channel width W, and we find that $W = 13.9$ µm results in $g_m = 0.5$ mA/V.





Problem 7.5



Design a two-stage opamp with feedback as shown above. The load capacitor C_L has a value of 5 pF which is considered to be much larger than all transistor capacitances, except C_{gs7}. The bias value of the input voltage is 1 V and the supply voltage is $V_{DD} = 1.8$ V. Use the input stage designed in Problem 7.4, and design I_{BN6} and M_7 to provide a g_{m7} of 5 mA/V. The transistors are modeled by the BSIM3 transistor models shown in Fig. 3.44.

Estimate C_{gs7} using $C_{ox} = 8.5$ fF/(µm)^2.

Design C_c so that the non-dominant pole is at a frequency which is $\simeq 2\,\omega_{tl}$ where ω_{tl} is the gain-bandwidth product of the loop gain.

For convenience, Fig. 3.44 is shown in the Appendix in this book.

Solution:

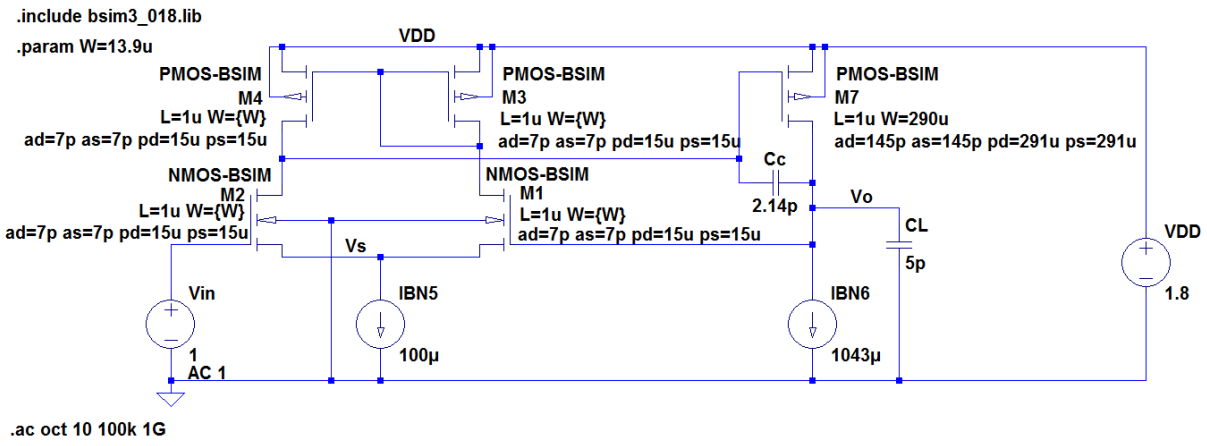
Running a '.op' simulation from the design from Problem 7.4 (using $W = 13.9$ µm), we find that the transconductance of M_3 and M_4 is 0.24 mA/V. Transistor M_7 has the same bias voltages as M_3 and M_4, so the transconductance and the bias current of M_7 scale proportionally with the channel width, hence $W_7 = (g_{m7}/g_{m3})W_3 = 290$ µm and $I_{BN6} = (W_7/W_3)I_{D3} = (W_7/W_3)I_{BN5}/2 = 1.043$ mA.
The gate-source capacitance C_{gs7} may be estimated from $C_{gs7} \simeq (2/3)C_{ox}W_7L_7 = 1.7$ pF.
From Eq. (7.11) in Bruun (2022), we find with $C_1 = C_{gs7} = 1.7$ pF, $C_2 = C_L = 5$ pF, $\beta = 1$ and $g_{m7}/g_{m1} = 10$ that $C_c = 2.14$ pF for $\omega_{p2}/\omega_{tl} \simeq 2$.

Problem 7.6

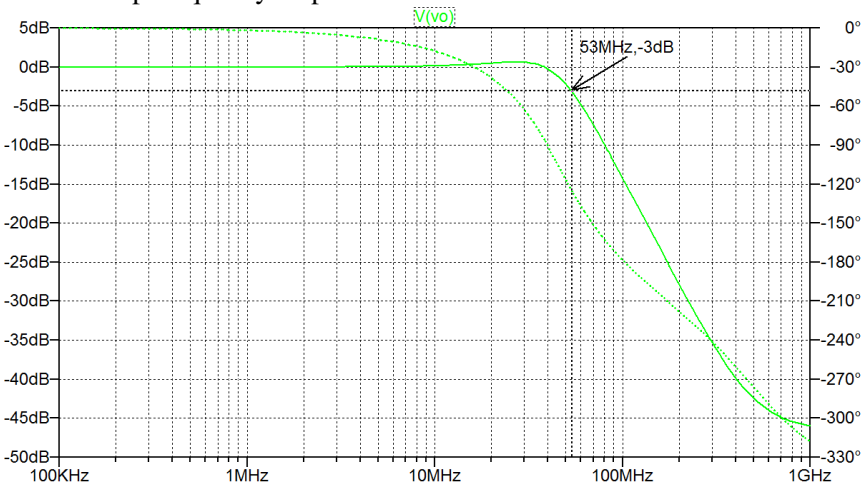
Use LTspice to simulate the circuit designed in Problem 7.5. Use drain areas and source areas of $(W \times 0.5$ µm) and drain perimeters and source perimeters of $(W + 1$ µm). Find the phase margin and the bandwidth for the amplifier.

Solution:

Shown here is the LTspice schematic corresponding to Problem 7.5 with the values of drain areas, source areas, drain perimeters and source perimeters as specified in the problem. Also, the value of C_c found in Problem 7.5 has been inserted. From the '.ac' simulation of the closed-loop gain, we find the closed-loop bandwidth of the amplifier to be 53 MHz.

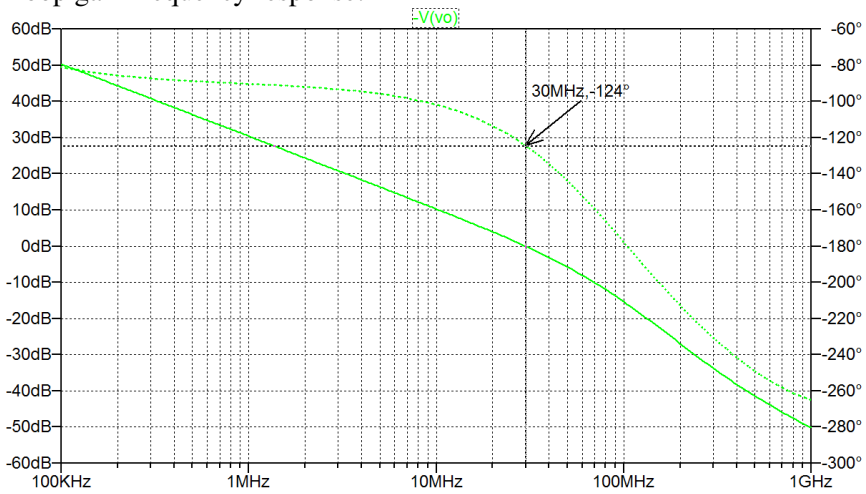


Closed-loop frequency response:



In order to find the phase margin, the feedback from the output to the gate of M_1 is broken and a test voltage V_t with a dc value of 1 and an ac amplitude of 1 is connected to the gate of M_1. Also, the ac value of '`Vin`' is changed to 0. The loop gain is found from a '.ac' simulation as '`-v(Vo)`' and the resulting plot is shown here. From the plot, we find a phase margin of 56°.

Loop gain frequency response:



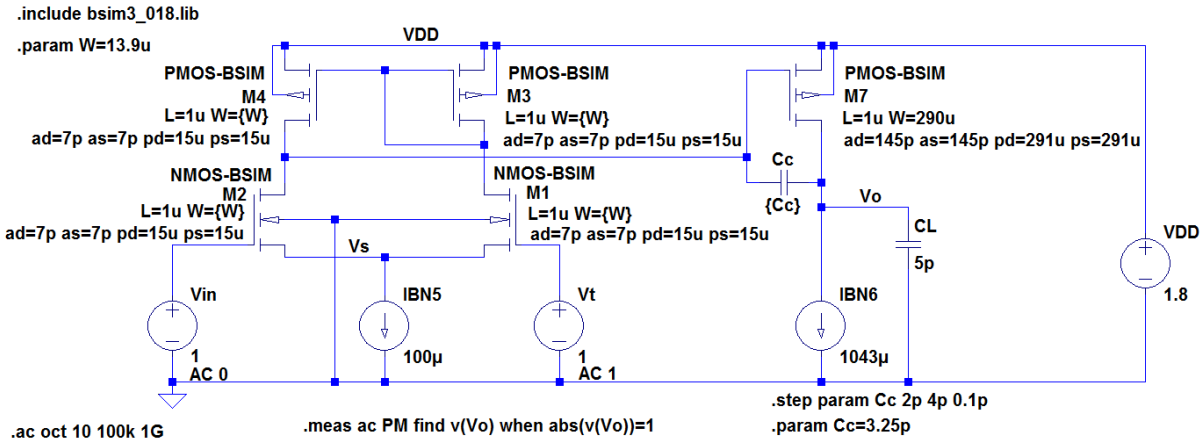
Problem 7.7

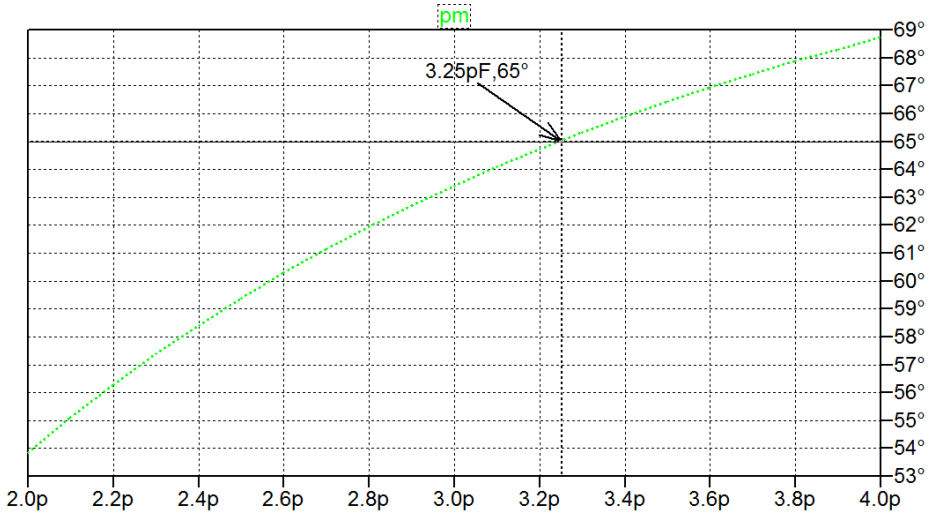
Suggest at least one modification to the circuit designed in Problem 7.5 in order to increase the phase margin to 65°.
Verify your suggestion using LTspice and find the resulting bandwidth.

Solution:

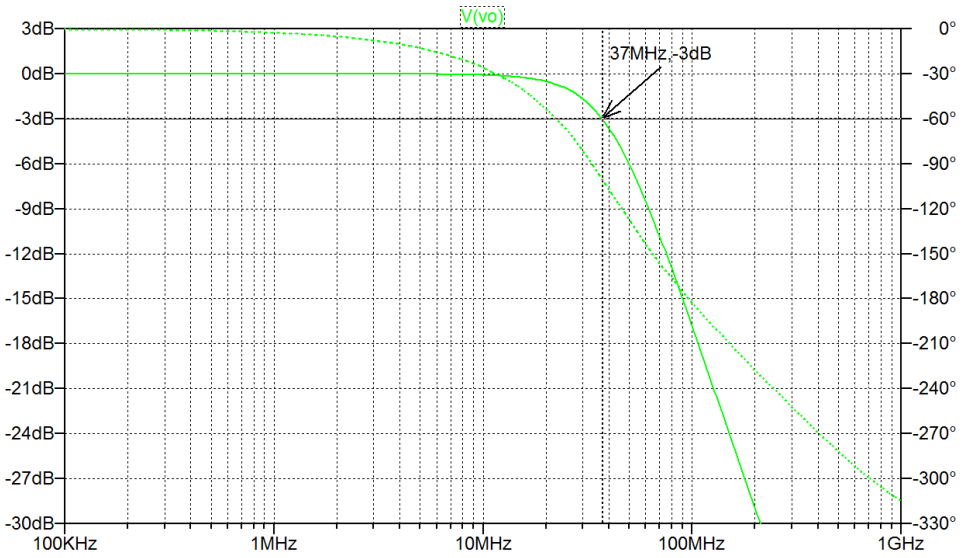
The phase margin may be increased by increasing the compensation capacitor C_c. According to Eq. (7.10) in Bruun (2022), this will increase ω_{p2}/ω_{t1}, thereby increasing the phase margin. Thus, we simulate the loop gain with C_c defined as a parameter and use a '.meas' directive to calculate the phase margin versus the value of C_c, compare to Bruun (2020, Tutorial 6.3). The calculated values of the phase margin are

found in the error log file from a '.ac' simulation, and using a left-click on the mouse, you may plot the phase margin versus the compensation capacitor C_c. Shown here is the LTspice schematic for the simulation and the plot of the phase margin versus the compensation capacitor C_c. From the plot, we find $C_c = 3.25$ pF for a phase margin of 65°.

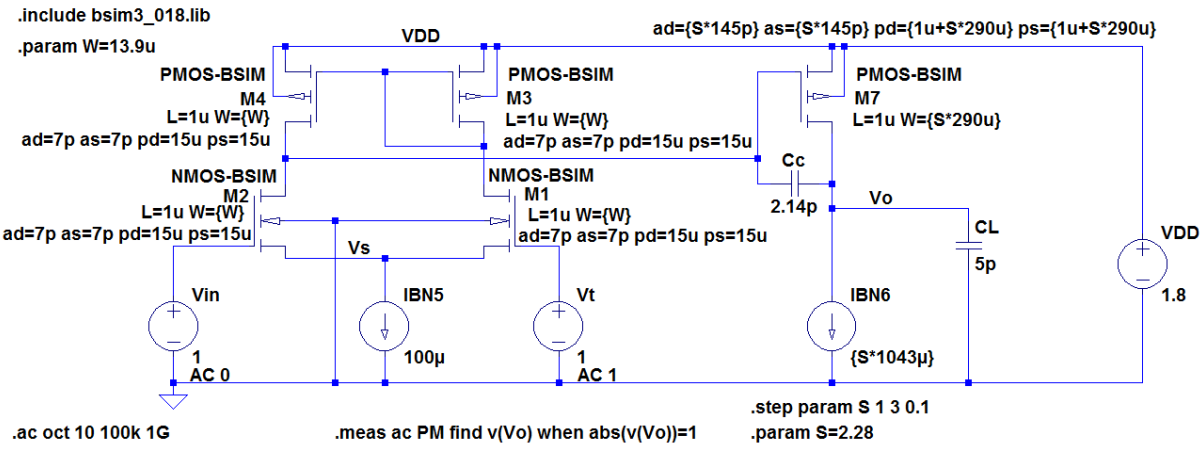


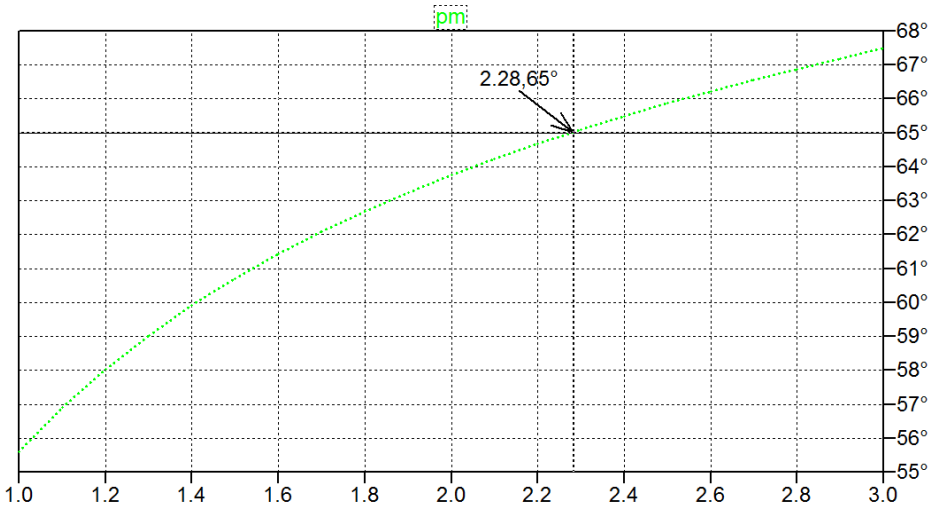


For finding the bandwidth, we close the feedback loop as shown in the LTspice schematic for Problem 7.6 and run a new '.ac' simulation. For this, the value of C_c is defined by a '.param' directive and the '.step' directive is deleted or changed into a comment. The following figure shows the output plot from the '.ac' simulation. From the '.ac' simulation, we find a bandwidth of 37 MHz.



Another way to increase the phase margin is to increase g_{m7}. This will increase both ω_z/ω_{tl} and ω_{p2}/ω_{tl}, see Eqs. (7.9) and (7.10) in Bruun (2022), thereby increasing the phase margin. The transconductance g_{m7} may be increased by increasing the bias current $I_{D7} = I_{BN6}$ and also increasing W_7 by the same factor so that the bias voltage V_{GS7} remains the same. We may define a scale factor 'S' as shown in the LTspice schematic below and step the scale factor through a suitable range, using a '.meas' directive to calculate the phase margin. From the error log file, we may plot the phase margin versus the scale factor. We find that a scale factor of 2.28 is required for a phase margin of 65°, corresponding to $W_7 = 661$ µm and $I_{BN6} = 2.38$ mA.

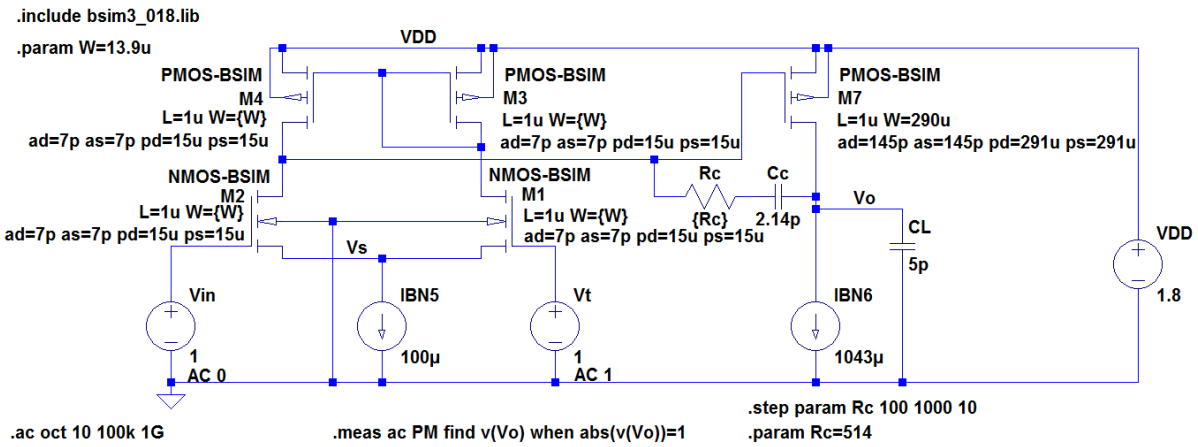


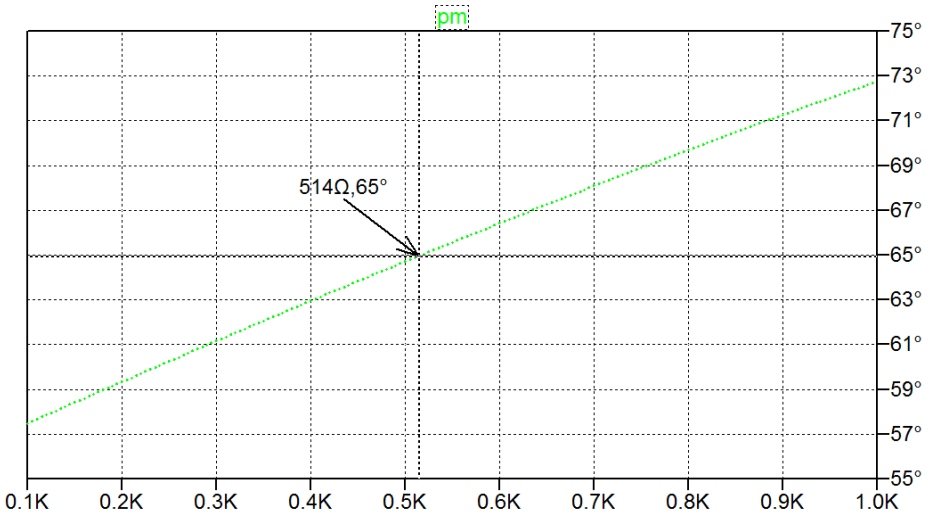


For finding the bandwidth, we close the feedback loop as shown in the LTspice schematic for Problem 7.6 and run a new '.ac' simulation. For this, the value of 'S' is defined by a '.param' directive and the '.step' directive is deleted or changed into a comment. From the '.ac' simulation, we find a bandwidth of 47 MHz.

Yet another way to increase the phase margin is to change the position of the zero in the loop gain by inserting a resistor R_c in series with C_c, see Eq. (6.61) in Bruun (2022).

Shown below is an LTspice schematic where the resistor R_c is stepped from 100 Ω to 1000 Ω. From the error log file, we may plot the phase margin versus R_c. We find that $R_c = 514$ Ω results in a phase margin of 65°.





For finding the bandwidth, we close the feedback loop as shown in the LTspice schematic for Problem 7.6 and run a new '.ac' simulation. For this, the value of R_c is defined by a '.param' directive and the '.step' directive is deleted or changed into a comment. From the '.ac' simulation, we find a bandwidth of 49 MHz.

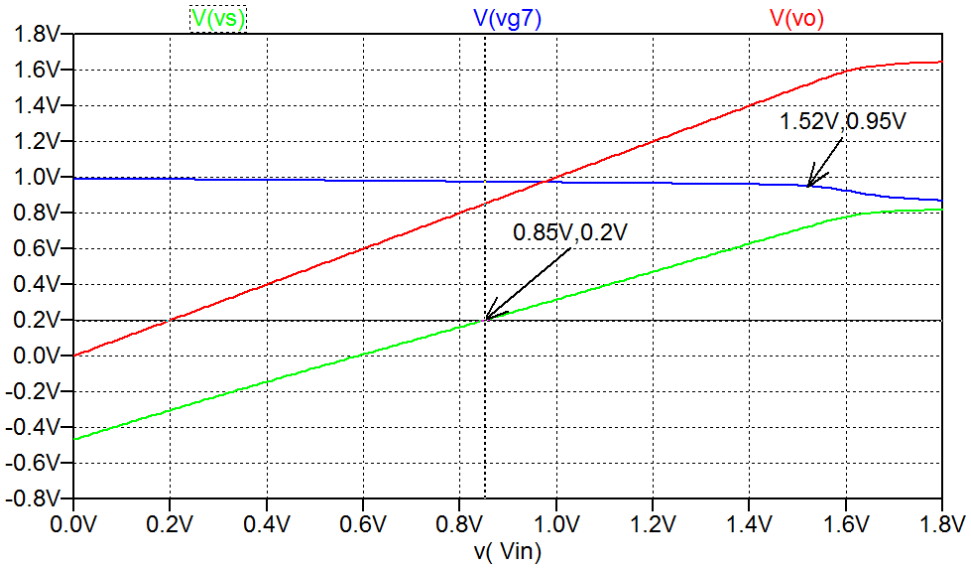
Problem 7.8

For the circuit designed in Problem 7.5, use LTspice to find the input voltage range for which all transistors operate in the active region. Assume that the voltage across the current sources I_{BN5} and I_{BN6} must be at least 0.2 V.

Solution:

For finding the input voltage range for the circuit derived in Problem 7.5, we use the LTspice schematic shown for Problem 7.6 and run a '.dc' simulation with '`Vin`' stepped from 0 V to 1.8 V. The lower limit is set by the requirement that 0.2 V is needed across the current source I_{BN5}, so from the simulation, we plot the source voltage V_S for M_1 and M_2. The upper limit is set by the requirement that M_7 should operate in the active region. This implies that the gate voltage for M_7 should remain almost constant with just a small, linear decrease of the voltage caused by the channel-length modulation. When M_7 enters the triode region for a high value of the input voltage and the output voltage, the absolute value of gate-source voltage for M_7 increases in order to maintain the same current in the transistor and this means that the gate voltage V_{G7} drops, so we plot the gate voltage V_{G7}.

The following figure shows the output plot from the simulation. Also shown in the plot is the output voltage V_O. From the plot, we find a minimum input voltage of 0.85 V and a maximum input voltage of about 1.52 V.



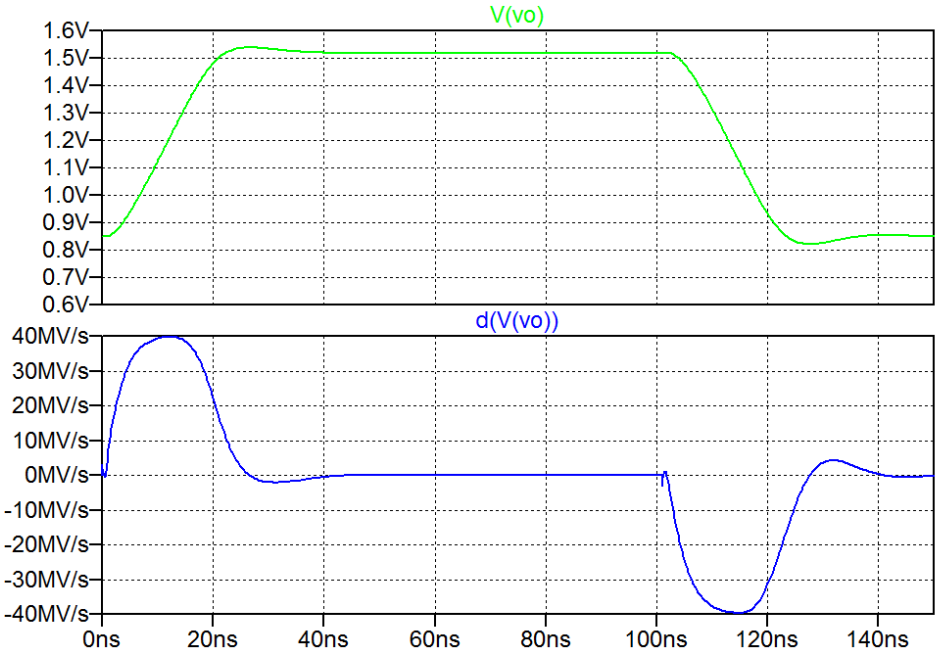
Problem 7.9

For the circuit designed in Problem 7.5, use LTspice to find the slew rate of the output voltage when applying an input voltage step with the maximum possible value within the input voltage range found in Problem 7.8.

Solution:

For finding the slew rate for the circuit designed in Problem 7.5, we use the LTspice schematic shown for Problem 7.6 and run a '.tran' simulation with '`Vin`' specified as a pulse,
'`PULSE(0.85 1.52 0 1n 1n 100n 200n 2)`'.

The following figure shows the output plot from the simulation. From the plot, we find a slew rate of approximately 40 V/μs for both a rising output signal and a falling output signal.



References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Bruun, E. 2017, *CMOS Integrated Circuit Simulation with LTspice*, bookboon.
Available from: http://bookboon.com/en/cmos-integrated-circuit-simulation-with-ltspice-ebook

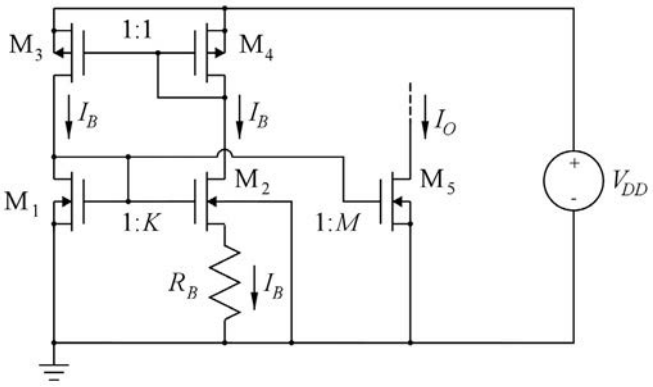
Chapter 8 – Bias Circuits, Bandgap References and Voltage Regulators

Multiple-choice test

1. Completed statements:

A-16:	The minimum voltage needed across the output transistor of a simple current mirror bias source is the transistor saturation voltage.
B-2:	The minimum voltage needed across the output transistors of a cascode current mirror bias source biased for low-voltage operation is the sum of two saturation voltages.
C-14:	The small-signal output resistance of a simple current mirror bias source is the small-signal output resistance of the transistor.
D-4:	The small-signal output resistance of a cascode current mirror bias source is approximately the product of a transistor intrinsic gain and a small-signal output resistance.
E-8:	In a MOS Widlar current source, the current is determined by a resistor and the difference between the gate-source voltages of two transistors biased with different current densities.
F-7:	A bandgap voltage reference obtains a very small temperature coefficient of the reference voltage by combining the voltage of a forward-biased diode and the voltage difference between two diodes which are forward biased with different current densities.
G-6:	The temperature coefficient of a voltage across a forward-biased diode is approximately -2 mV/K.
H-11:	When two identical diodes are forward-biased with different currents, the temperature coefficient of the voltage difference between the diodes is positive.
I-13:	In a low dropout voltage regulator, the pass transistor terminal connected to the output of the regulator is the drain.

2. For the bias circuit shown below, we assume that the transistors are modeled by the Shichman-Hodges model and that the channel-length modulation can be neglected.



The scaling ratio K between transistors M_1 and M_2 must be

A: smaller than 1
B: equal to 1
C: larger than 1

Solution:

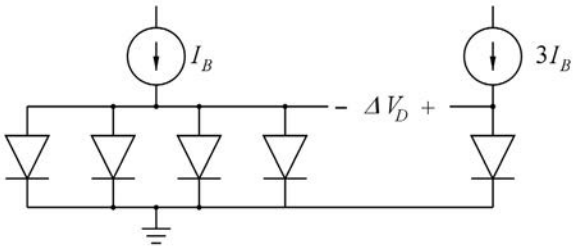
In order to have a voltage across R_B, the gate-source voltage for M_2 must be smaller than the the gate-source voltage for M_1. This implies $W_2/L_2 > W_1/L_1$, i.e., $K > 1$.

3. With $K = 4$ and $M = 3$ in the circuit above and an effective gate voltage of 0.4 V for M_1, the value of R_B required for $I_O = 0.3$ mA is
   A: 1 kΩ
   B: 2 kΩ
   C: 4 kΩ

Solution:

With $K = 4$, we find from the Shichman-Hodges transistor model that the effective gate voltage for M_2 is half the effective gate voltage for M_1, i.e., 0.2 V. This implies that the voltage V_B across R_B is $V_B = 0.2$ V. With a scaling factor $M = 3$ for M_3 and $I_{D5} = 0.3$ mA, we find $I_B = 0.1$ mA and $R_B = V_B/I_B = 2$ kΩ.

4. For the circuit shown below, we assume that the diodes are identical and that the relation between diode current I_D and diode voltage V_D is $I_D = I_S \exp(V_D/V_T)$ where I_S is the diode saturation current and V_T is the thermal voltage.



   At room temperature (27°C), the voltage ΔV_D is approximately
   A: 64 mV
   B: 36 mV
   C: 26 mV

Solution:

The current in the rightmost diode is 12 times the current in each of the other diodes. From Eq. (8.20) in Bruun (2022), we then find $\Delta V_D = (kT/q)\ln(12) \simeq 64$ mV at room temperature.

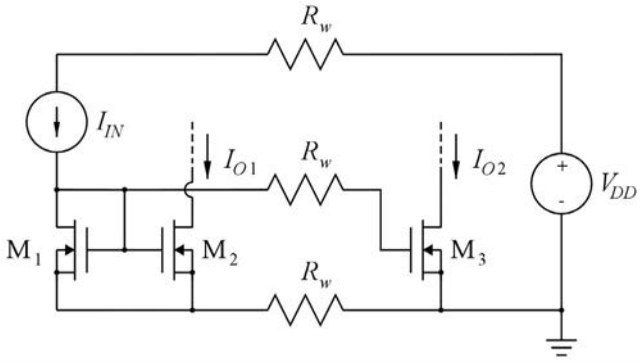
5. For the circuit above, the temperature coefficient $\partial \Delta V_D/\partial T$ is approximately
   A: 0.086 mV/K
   B: 0.119 mV/K
   C: 0.214 mV/K

Solution:

Using Eq. (8.21) in Bruun (2022), we find $\partial \Delta V_D/\partial T = 0.0861$ mV/K $\times \ln(12) \simeq 0.214$ mV/K.

Problems

Problem 8.1



The circuit shown above is used to mirror the current $I_{IN} = 90$ µA to the output currents I_{O1} and I_{O2}. M_1, M_2 and M_3 are identical with $V_{tn} = 0.40$ V, $\mu_n C_{ox} = 180$ µA/V^2 and $L = 1$ µm. The channel-length modulation can be neglected. Design M_1 to have an effective gate-source voltage of 200 mV.
The resistors R_w represent the wiring resistance of aluminum connections between M_3 and M_1 - M_2 which are located far away from M_3. Calculate R_w, assuming a wiring length of 2 mm, width of 1 µm and thickness of 0.25 µm. The resistivity of aluminum is $\rho = 2.7 \times 10^{-8}$ Ωm. Calculate the output currents I_{O1} and I_{O2}, assuming that all transistors are in the active region.

Solution:

For an effective gate voltage of $V_{\text{eff}} = V_{GS1} - V_{tn} = 200$ mV, we find from the Shichman-Hodges model

$$I_{D1} = I_{IN} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_{tn})^2 \;\Rightarrow W = L\frac{2I_{IN}}{\mu_n C_{ox}(V_{GS1} - V_{tn})^2} = 25\ \mu\text{m}$$

Thus, M_1, M_2 and M_3 have a channel length of $L = 1$ µm and a channel width of $W = 25$ µm.

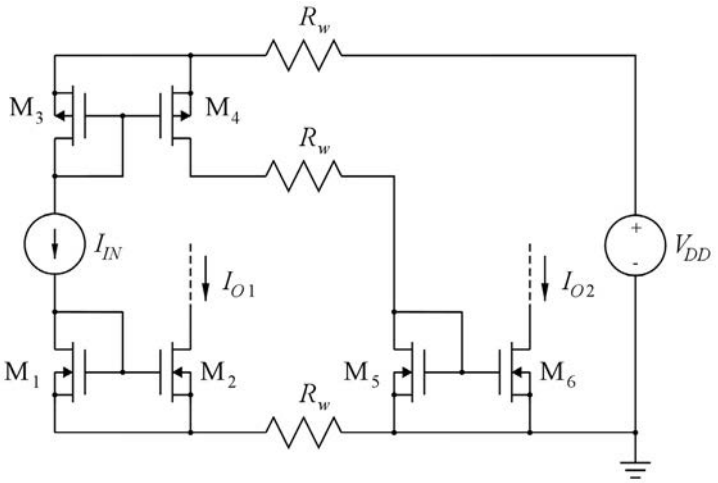
The resistor value R_w is given by $R_w = \rho L_w/(W_w t_w)$ where $\rho = 2.7 \times 10^{-8}$ Ωm is the resistivity of aluminum, $L_w = 2$ mm is the length of the wire, $W_w = 1$ µm is the width of the wire and $t_w = 0.25$ µm is the thickness of the wire. Inserting the numerical values, we find $R_w = 216\ \Omega$.

Since M_1 and M_2 have the same gate-source voltage and are both assumed to be in the active region, we find $I_{O1} = I_{D2} = I_{D1} = I_{IN} = 90$ µA.

Since the gate current to M_3 is 0, there is no voltage drop in the resistor R_w connected between the gate of M_1 and the gate of M_3, so $V_{G3} = V_{G1}$. The current in the resistor R_w connected between the source of M_1 and the source of M_3 is equal to $I_{D1} + I_{D2} = 2I_{IN}$. Thus $V_{S1} = 2I_{IN}R_w = 38.9$ mV and $V_{G1} = V_{G3} = V_{GS3} = V_{GS1} + V_{S1} = 638.9$ mV. From the Shichman-Hodges model, we find

$$I_{O2} = I_{D3} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS3} - V_{tn})^2 = \frac{1}{2}\mu_n C_{ox}(V_{GS1} + 2I_{IN}R_w - V_{tn})^2 = 128\ \mu\text{A}$$

Problem 8.2



The circuit shown above is used to mirror the current $I_{IN} = 90$ µA to the output currents I_{O1} and I_{O2}. The four NMOS transistors are identical and have $V_{tn} = 0.40$ V, $\mu_n C_{ox} = 180$ µA/V^2 and $L = 1$ µm. The two PMOS transistors are also identical and have $V_{tp} = -0.42$ V, $\mu_p C_{ox} = 45$ µA/V^2 and $L = 1$ µm. The channel-length modulation can be neglected for all transistors. Design M_1 and M_3 to have an absolute value of the effective gate-source voltage of 200 mV.
The wiring resistance is $R_w = 216\ \Omega$. Calculate the output currents I_{O1} and I_{O2}, assuming that all transistors are in the active region.
Verify your results from Problems 8.1 and 8.2 using LTspice simulation.

Solution:

For an effective gate voltage of $V_{\text{eff}} = V_{GS1} - V_{tn} = 200$ mV, we find from the Shichman-Hodges model

$$I_{D1} = I_{IN} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_{tn})^2 \quad \Rightarrow W = L\frac{2I_{IN}}{\mu_n C_{ox}(V_{GS1} - V_{tn})^2} = 25\ \mu\text{m}$$

Thus, M_1, M_2, M_5 and M_6 have a channel length of $L = 1$ µm and a channel width of $W = 25$ µm.

For the PMOS transistors M_3 and M_4, we find with $|V_{\text{eff}}| = 200$ mV:

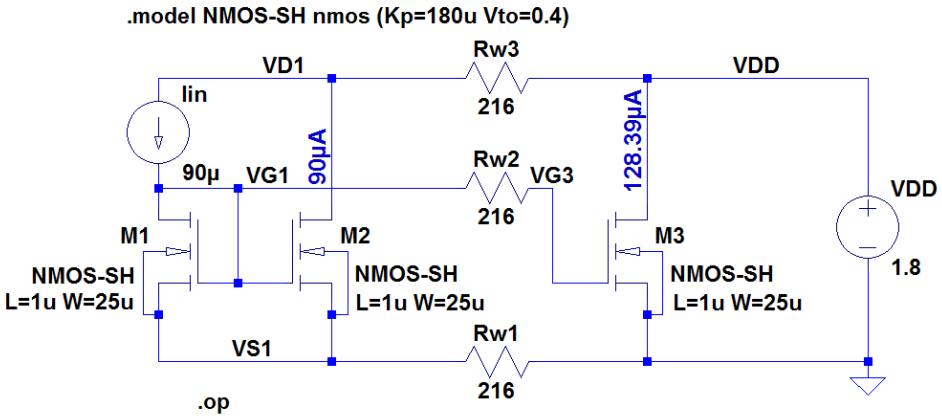
$$I_{D3} = I_{IN} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS3} - V_{tp})^2 \quad \Rightarrow W = L\frac{2I_{IN}}{\mu_p C_{ox}(V_{GS3} - V_{tp})^2} = 100\ \mu\text{m}$$

Since M_1 and M_2 have the same gate-source voltage and are both assumed to be in the active region, we find $I_{O1} = I_{D2} = I_{D1} = I_{IN} = 90$ µA.

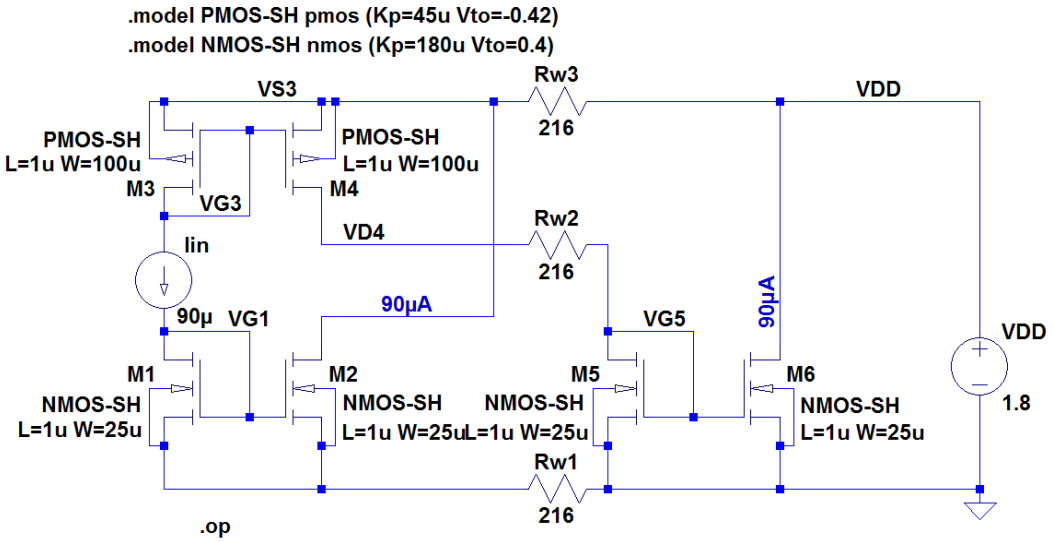
Since M_3 and M_4 have the same gate-source voltage and are both assumed to be in the active region, we find $I_{D4} = I_{D3} = I_{IN} = 90$ µA. The drain current of M_5 is identical to the drain current of M_4, so $I_{D5} = I_{IN} = 90$ µA.

Since M_5 and M_6 have the same gate-source voltage and are both assumed to be in the active region, we find $I_{O2} = I_{D6} = I_{D5} = I_{IN} = 90$ µA.

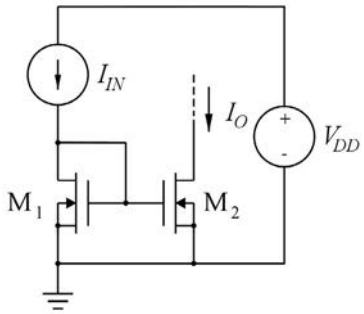
The results may be verified by LTspice. Shown below is an LTspice schematic corresponding to Problem 8.1 with the calculated values of the wiring resistances and the transistor dimensions inserted. From a '.op' simulation, the output currents I_{O1} and I_{O2} may be found from the output file as '`Id(M2)`' and '`Id(M3)`'. The simulation results confirm the calculated values.



Further, an LTspice schematic corresponding to Problem 8.2 is shown with the calculated values of the transistor dimensions inserted. From a '.op' simulation, the output currents I_{O1} and I_{O2} may be found from the output file as '`Id(M2)`' and '`Id(M6)`'. The simulation results confirm the calculated values.



Problem 8.3



The current mirror above consists of two NMOS transistors with $W/L = 25$, $\mu_n C_{ox} = 180\ \mu A/V^2$ and a nominal value of the threshold voltage V_{tn} of 400 mV. However, due to spread in the manufacturing process, V_{tn} may differ by 5 mV for the two transistors, i.e., $V_{tn1} = 400$ mV and $V_{tn2} = 400\ \text{mV} \pm 5$ mV. The channel-length modulation can be ignored and both transistors are in the active region.
Ideally, $I_O = I_{IN}$. However, the difference in V_{tn} causes a deviation from the ideal value of the output current. Calculate the maximum relative error in I_O for $I_{IN} = 100\ \mu A$. Repeat the calculation for $I_{IN} = 400\ \mu A$.

Solution:

For $I_{IN} = 100\ \mu A$, we find using the Shichman-Hodges model

$$V_{GS1} = V_{GS2} = V_{tn1} + \sqrt{\frac{2I_{IN}}{\mu_n C_{ox}(W/L)}} = 610.82\ \text{mV}.$$

For $V_{tn2} = 400\ \text{mV} + 5\ \text{mV} = 405\ \text{mV}$, we find $I_O = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GS2} - V_{tn2})^2 = 95.31\ \mu A$.

The relative mismatch is $(100 - 95.31)/100 = 0.0469 \sim 4.7\%$.

For $V_{tn2} = 400\ \text{mV} - 5\ \text{mV} = 395\ \text{mV}$, we find $I_O = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GS2} - V_{tn2})^2 = 104.80\ \mu A$.

The relative mismatch is $|100 - 104.80|/100 = 0.0480 \sim 4.8\%$.

Thus, the maximum relative error in I_O is 4.8%.

For $I_{IN} = 400\ \mu A$, we find using the Shichman-Hodges model

$$V_{GS1} = V_{GS2} = V_{tn1} + \sqrt{\frac{2I_{IN}}{\mu_n C_{ox}(W/L)}} = 821.64\ \text{mV}.$$

For $V_{tn2} = 400\ \text{mV} + 5\ \text{mV} = 405\ \text{mV}$, we find $I_O = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GS2} - V_{tn2})^2 = 390.57\ \mu A$.

The relative mismatch is $(400 - 390.57)/100 = 0.0236 \sim 2.4\%$.

For $V_{tn2} = 400\text{ mV} - 5\text{ mV} = 395\text{ mV}$, we find $I_O = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GS2} - V_{tn2})^2 = 409.54\ \mu\text{A}$.

The relative mismatch is $|400 - 409.54|/100 = 0.0239 \sim 2.4\%$.

Thus, the maximum relative error in I_O is 2.4%.

We may also use the Shichman-Hodges model to derive an analytical expression for the mismatch between I_{IN} and I_O. With $V_{GS2} = V_{GS1} = V_{IN}$ and $V_{tn2} = V_{tn1} + \Delta V_{tn}$, we find

$$\begin{aligned} I_O &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{IN} - V_{tn1} - \Delta V_{tn})^2 \\ &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[(V_{IN} - V_{tn1})^2 - 2\Delta V_{tn}(V_{IN} - V_{tn1}) + \Delta V_{tn1}^2] \\ &\simeq \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[(V_{IN} - V_{tn1})^2 - 2\Delta V_{tn}(V_{IN} - V_{tn1})] \\ &= I_{IN} - \mu_n C_{ox}\left(\frac{W}{L}\right)\Delta V_{tn}(V_{IN} - V_{tn1}) \end{aligned}$$

where we have used $I_{IN} = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{IN} - V_{tn1})^2$ and $\Delta V_{tn1} \ll V_{IN} - V_{tn1}$.

From this expression, we find

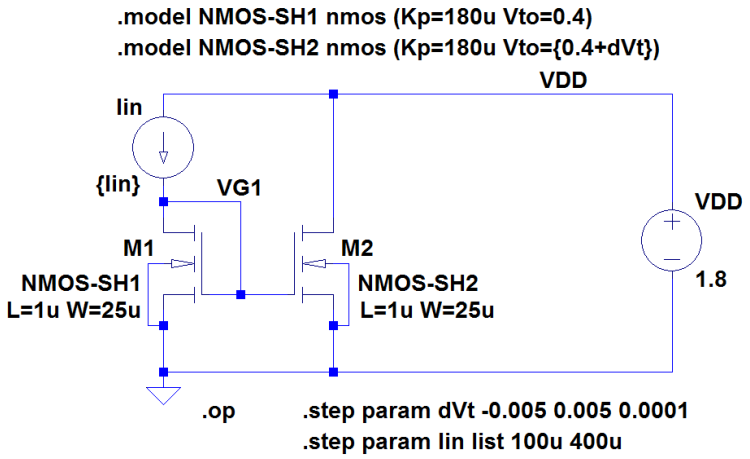
$$I_{IN} - I_O \simeq \mu_n C_{ox}\left(\frac{W}{L}\right)\Delta V_{tn}(V_{IN} - V_{tn1}) = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{IN} - V_{tn1})^2\left(\frac{2\Delta V_{tn}}{V_{IN} - V_{tn1}}\right) = I_{IN}\left(\frac{2\Delta V_{tn}}{V_{IN} - V_{tn1}}\right)$$

Using $V_{IN} - V_{tn1} = \sqrt{\frac{2I_{IN}}{\mu_n C_{ox}(W/L)}}$, we find the relative mismatch

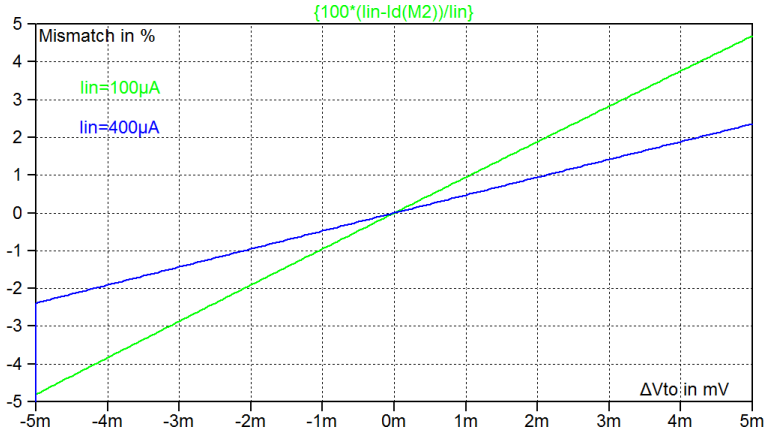
$$\frac{I_{IN} - I_O}{I_{IN}} = \frac{2\Delta V_{tn}}{\sqrt{2I_{IN}}}\sqrt{\mu_n C_{ox}(W/L)} = \left(\frac{\Delta V_{tn}}{\sqrt{I_{IN}}}\right)\sqrt{2\mu_n C_{ox}(W/L)}$$

From this expression, we see that the mismatch is proportional to ΔV_{tn} and inversely proportional to $\sqrt{I_{IN}}$. Inserting $\Delta V_{tn} = 5$ mV, we find a mismatch of 4.74% for $I_{IN} = 100\ \mu$A and 2.37% for $I_{IN} = 400\ \mu$A.

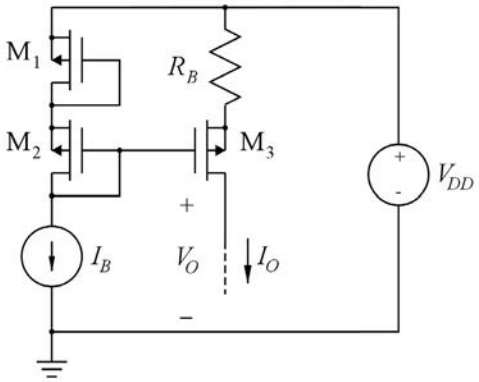
The analytical results may also be verified using LTspice. In the following schematic, the two transistors are defined by separate '.model' directives in order to define different threshold voltages. For transistor M_2, the threshold voltage is defined as '`0.4+dVt`' where the threshold voltage mismatch '`dVt`' is defined as a parameter which is stepped from -5 mV to $+5$ mV using a '.step' directive. Also the input current is stepped using a '.step' directive defining the values 100 µA and 400 µA.



From a '.op' simulation, we may plot the relative mismatch in % as '`{100*(Iin-Id(M2))/Iin}`' as shown below. The green trace is for $I_{IN} = 100$ µA and the blue trace is for $I_{IN} = 400$ µA.



Problem 8.4



The circuit shown above is used to generate a constant current I_O. All transistors are assumed to be identical with $\mu_p C_{ox} = 45$ µA/V^2, $V_{tp} = -0.42$ V and $W/L = 10$. The supply voltage is $V_{DD} = 1.8$ V.

The current I_B is $I_B = 9$ µA.
Calculate R_B so that $I_O = 100$ µA, assuming that all transistors are in the active region.
What is the maximum value of V_O for which M_3 is in the active region?

Solution:

Using a loop equation for the loop consisting of M_1, M_2, M_3 and R_B, we find that the voltage V_B across R_B is equal to $V_B = |V_{GS1}| + |V_{GS2}| - |V_{GS3}|$. With $I_{D1} = I_{D2} = I_B = 9$ µA, we find

$$|V_{GS1}| = |V_{GS2}| = |V_{tp}| + \sqrt{\frac{2I_B}{\mu_p C_{ox}(W/L)}} = 0.62 \text{ V}$$

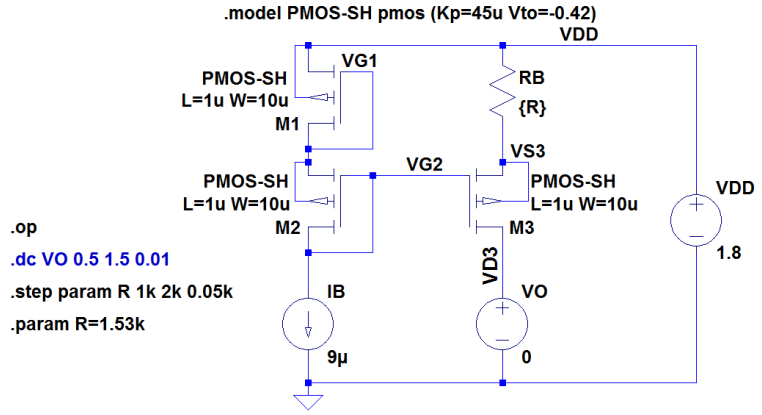
With $I_{D3} = I_O = 100$ µA, we find

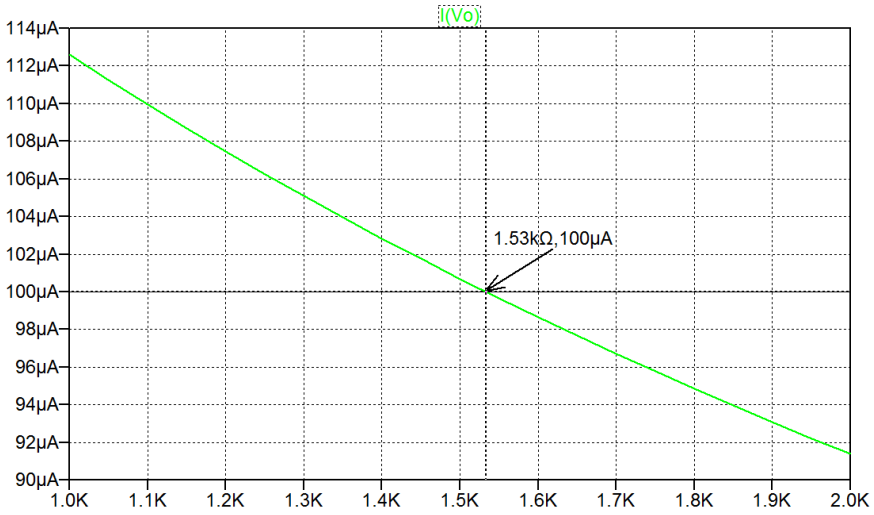
$$|V_{GS3}| = |V_{tp}| + \sqrt{\frac{2I_O}{\mu_p C_{ox}(W/L)}} = 1.087 \text{ V}$$

Thus, $V_B = 0.153$ V, resulting in $R_B = V_B/I_O = 1.53$ kΩ.

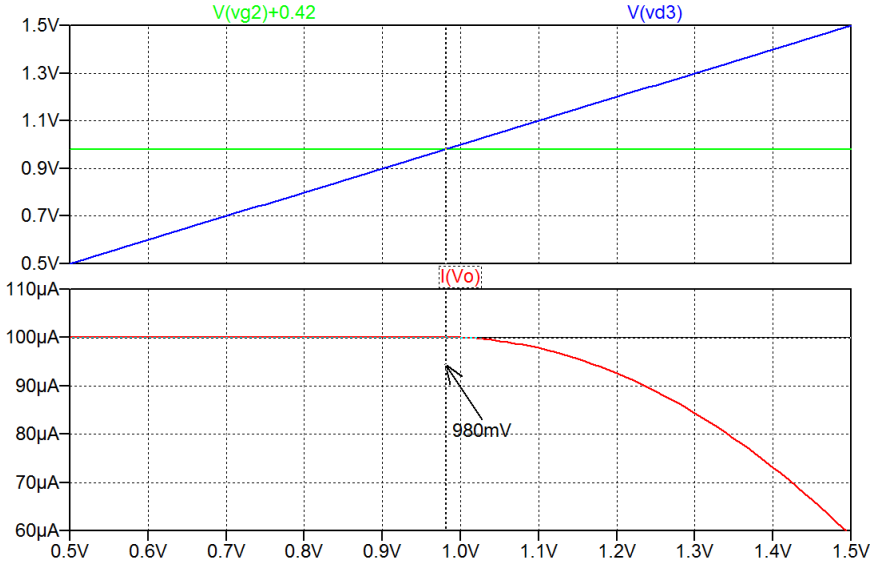
The maximum value of V_O is found from $|V_{DS3}| \geq |V_{GS3}| - |V_{tp}| \Rightarrow V_O \leq V_{G3} + |V_{tp}|$ where $V_{G3} = V_{G2} = V_{DD} - 2|V_{GS2}| = 0.56$ V. Thus, the maximum value of V_O is $V_{O\max} = 0.98$ V.

The problem may also be solved using LTspice. Shown below is an LTspice schematic corresponding to Problem 8.4. The value of R_B is defined as a parameter which is stepped through a suitable interval. From a '.op' simulation, we may show the output current '`I(Vo)`' as a function of the resistor R_B. From the plot, we find that $R_B = 1.53$ kΩ results in $I_O = 100$ µA as also found analytically.

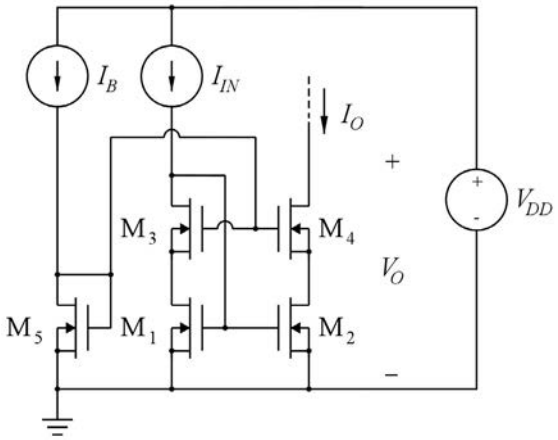




From a '.dc' simulation with a sweep of V_O (shown as a comment in the schematic) and with R_B defined by a '.param' directive, we may plot $V_O = V_{D3}$ and $V_{G2} + |V_{tp}| = V_{G2} + 0.42$ V as shown below. From the intersection between the two traces, we find $V_{O\max} = 0.98$ V. We may also plot I_O versus V_O as shown below. We see that the current I_O decreases when $V_O > V_{O\max}$ because M_3 is no longer in the active region but operates in the triode region.



Problem 8.5



The figure above shows a cascode current mirror biased for operation with a low output voltage and all transistors in the active region. All transistors have $\mu_n C_{ox} = 180$ µA/V^2 and $V_{tn} = 0.4$ V. The channel-length modulation and the body effect can be neglected. Transistors M_1 to M_4 are assumed to be identical with $W/L = 25$. The input current I_{IN} is 90 µA and also M_5 is biased by a current $I_B = 90$ µA.

Calculate W_5/L_5 so that the gate voltage for M_3, M_4 and M_5 equals $V_{GS3} + V_{DSsat1}$.

Find the minimum output voltage for which all transistors are in the active region.

Now assume that the channel-length modulation parameter is $\lambda = 0.1$ V^{-1} for all transistors. Use LTspice to adjust W_5/L_5 so that M_1 and M_2 remain in the active region and find the output resistance of the current mirror when the output voltage is $V_O = 0.9$ V.

Next, assume that M_3 and M_4 have their bulk connected to ground so that the bulk effect cannot be neglected. Use LTspice with the transistor model from Table 3.1 and a channel length of 1 μm to find the maximum value of W_5/L_5 ensuring that M_1 and M_2 are in the active region. Also find the minimum output voltage for which all transistors are in the active region and find the output resistance when the output voltage is $V_O = 0.9$ V.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

Since the four transistors M_1, M_2, M_3 and M_4 are identical and have the same bias current, they all have the same saturation voltage or effective gate voltage, i.e., $V_{DS\text{sat}1} = V_{DS\text{sat}2} = V_{DS\text{sat}3} = V_{DS\text{sat}4}$.

From $V_{GS5} = V_{GS3} + V_{DS\text{sat}1}$, we find $V_{GS5} = V_{tn} + V_{DS\text{sat}3} + V_{DS\text{sat}1} = V_{tn} + 2V_{DS\text{sat}1}$.

Combining this relation with $V_{GS5} = V_{tn} + V_{DS\text{sat}5}$, we find $V_{DS\text{sat}5} = 2V_{DS\text{sat}1}$.

From the Shichman-Hodges transistor model, we find with $I_{D5} = I_B = I_{IN} = I_{D1}$:

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W_5}{L_5}\right)(V_{DS\text{sat}5})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_5}{L_5}\right)(2V_{DS\text{sat}1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_1}{L_1}\right)(V_{DS\text{sat}1})^2$$

$$\Rightarrow \frac{W_5}{L_5} = \frac{W_1}{4L_1} = 6.25$$

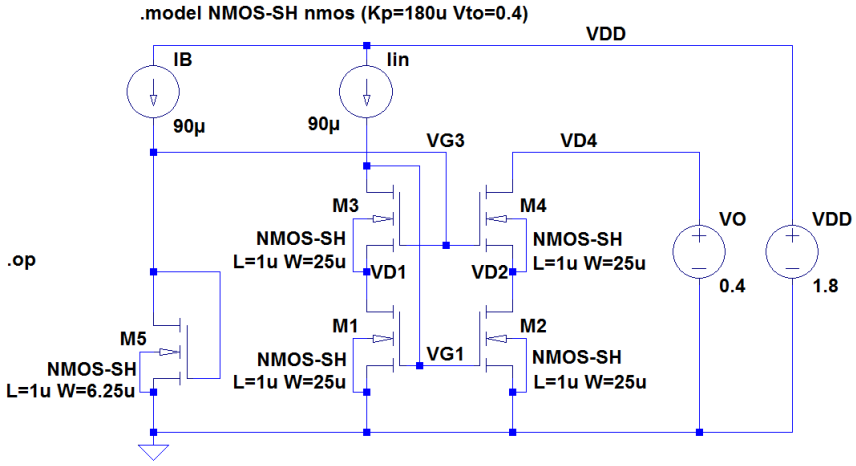
With $V_{G3} = V_{G4}$, we find the minimum output voltage with all transistors in the active region as $V_{O\min} = V_{D4\min} = V_{G4} - V_{tn} = V_{G3} - V_{tn} = V_{GS3} + V_{DS\text{sat}1} - V_{tn} = V_{GS1} + V_{DS\text{sat}1} - V_{tn} = 2V_{DS\text{sat}1}$.

The numerical value is found from $V_{DS\text{sat}1} = \sqrt{\dfrac{2I_{IN}}{\mu_n C_{ox}(W_1/L_1)}} = 200$ mV, resulting in a minimum output voltage of $V_{O\min} = 400$ mV.

With a channel-length modulation parameter $\lambda = 0.1\ \text{V}^{-1}$, we find the small-signal output resistance for each of the transistors as $r_{ds} \simeq 1/(\lambda I_D) = 111$ kΩ. Since M_4 operates as a cascode transistor for M_2, we find the output resistance of the cascode using Eq. (4.27) from Bruun (2022):

$$r_{out} \simeq g_{m4} r_{ds4} r_{ds2} = \left(\frac{2I_O}{V_{DS\text{sat}4}}\right)\left(\frac{1}{\lambda I_O}\right) r_{ds2} = \left(\frac{2}{\lambda V_{DS\text{sat}4}}\right) r_{ds2} = 11.1\ \text{MΩ}$$

The circuit may also be analyzed using LTspice. First, we simulate the circuit using the Shichman-Hodges model with $\lambda = 0$, i.e., without channel length modulation. The following figure shows an LTspice schematic with the output voltage set to $V_{O\min} = 400$ mV. For this circuit, we expect $V_{GS} = 600$ mV and $V_{DS} = V_{DS\text{sat}} = 200$ mV for M_1, M_2 and M_4, indicating that they are operating at the edge of the active region where $V_{DS} = V_{GS} - V_{tn}$. For M_3, we have $V_{D3} = V_{G1} = 600$ mV and $V_{S3} = V_{G4} - V_{GS3} = V_{DS\text{sat}1} = 200$ mV, so $V_{DS3} = 400$ mV.



From the output file, we may verify that all node voltages are as expected. From the error log file, we may find the drain-source voltages and the saturation voltages of each transistor to verify that all transistors are in the active region.

The following table shows the results from the error log file. We notice that all transistors have $V_{DS} \geq V_{DS\text{sat}}$. We also find the small-signal transconductance $g_{m4} = 0.9$ mA/V and we find that the output conductances are 0 as expected with the transistors in the active region. The non-zero but very small values for g_{ds1} and g_{ds2} appear because the transistors are operating at the edge of the active region.

Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m5          m3          m4          m1          m2
Model:      nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:       9.00e-05    9.00e-05    9.00e-05    9.00e-05    9.00e-05
Vgs:      8.00e-01    6.00e-01    6.00e-01    6.00e-01    6.00e-01
Vds:      8.00e-01    4.00e-01    2.00e-01    2.00e-01    2.00e-01
Vbs:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      4.00e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:    4.00e-01    2.00e-01    2.00e-01    2.00e-01    2.00e-01
Gm:       4.50e-04    9.00e-04    9.00e-04    9.00e-04    9.00e-04
Gds:      0.00e+00    0.00e+00    0.00e+00    1.00e-11    1.63e-10
```

Next, we modify the '.model' directive to '`.model NMOS-SH nmos (Kp=180u Vto=0.4 lambda=0.1)`' in order to include the channel-length modulation. We also change V_O from 0.4 V to 0.9 V in order to find the output resistance for $V_O = 0.9$ V. Running the '.op' simulation results in the error log file shown below. We notice that for M_1 and M_2, $V_{DS} < V_{DS\text{sat}}$, so they are not in the active region. We also see that g_{ds1} and g_{ds2} are significantly larger than g_{ds3} and g_{ds4}, also indicating that M_1 and M_2 operate in the triode region rather than in the active region.

Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m5          m3          m4          m1          m2
Model:      nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:       9.00e-05    9.00e-05    9.01e-05    9.00e-05    9.01e-05
Vgs:      7.85e-01    5.96e-01    5.93e-01    5.98e-01    5.98e-01
Vds:      7.85e-01    4.09e-01    7.08e-01    1.89e-01    1.92e-01
Vbs:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      4.00e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:    3.85e-01    1.96e-01    1.93e-01    1.98e-01    1.98e-01
Gm:       4.67e-04    9.18e-04    9.32e-04    8.67e-04    8.79e-04
Gds:      8.34e-06    8.65e-06    8.42e-06    5.11e-05    3.90e-05
```

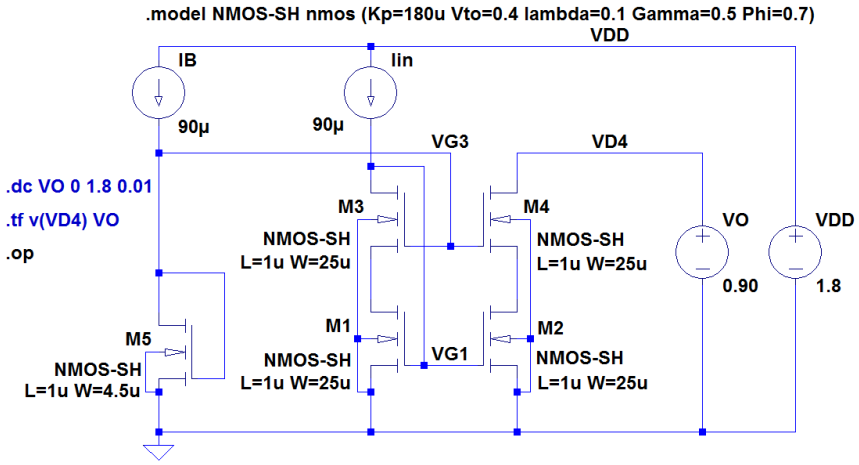
In order to bring M_1 and M_2 into the active region, we must increase V_{G3}, thereby increasing V_{D1} and V_{D2}. This can be achieved by reducing the channel width W_5. A few iterations show that with $W_5 = 5.9$ µm, M_1 and M_2 are in the active region and a '.op' simulation results in the error log file shown below.

Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m5          m3          m4          m1          m2
Model:         nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:            9.00e-05    9.00e-05    9.00e-05    9.00e-05    9.00e-05
Vgs:           7.96e-01    5.96e-01    5.93e-01    5.98e-01    5.98e-01
Vds:           7.96e-01    3.98e-01    6.97e-01    2.00e-01    2.03e-01
Vbs:           0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:           4.00e-01    4.00e-01    4.00e-01    4.00e-01    4.00e-01
Vdsat:         3.96e-01    1.96e-01    1.93e-01    1.98e-01    1.98e-01
Gm:            4.54e-04    9.18e-04    9.31e-04    9.09e-04    9.09e-04
Gds:           8.34e-06    8.66e-06    8.42e-06    8.82e-06    8.82e-06
```

From the error log file, we find $g_{m4} = 0.931$ mA/V, $g_{ds4} = 8.42$ µA/V and $g_{ds2} = 8.82$ µA/V, resulting in $r_{out} \simeq (g_{m4}/g_{ds4})(1/g_{ds2}) \simeq 12.5$ MΩ. Alternatively, the output resistance may be found from a '.tf' simulation with '`VO`' as the source and '`v(VD4)`' as the output. From this '.tf' simulation, the output resistance is found as the input impedance seen by '`VO`'. The value found by this simulation is 12.8 MΩ, i.e., very close to the calculated value.

Finally, we modify the LTspice schematic to include bulk effect for M_3 and M_4 as shown in the following schematic. Note that the bulk effect parameters are now included in the transistor model. With the bulk effect included, the threshold voltage is increased for M_3 and M_4, so a corresponding increase in $V_{G3} = V_{G4}$ is required in order to bring M_1 and M_2 into the active region. This can be achieved by reducing the channel width W_5 even further. A few iterations show that with $W_5 = 4.5$ µm, M_1 and M_2 are in the active region and a '.op' simulation results in the error log file shown below.



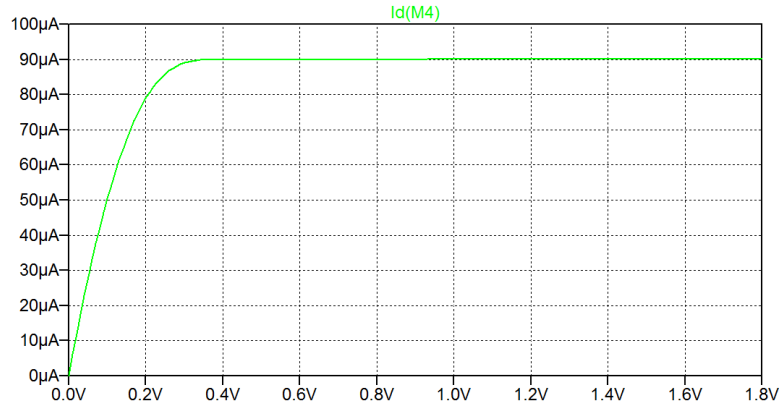
Error log file

```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m5          m3          m4          m1          m2
Model:         nmos-sh     nmos-sh     nmos-sh     nmos-sh     nmos-sh
Id:            9.00e-05    9.00e-05    9.00e-05    9.00e-05    9.00e-05
Vgs:           8.53e-01    6.52e-01    6.50e-01    5.98e-01    5.98e-01
Vds:           8.53e-01    3.98e-01    6.98e-01    2.00e-01    2.02e-01
Vbs:           0.00e+00   -2.00e-01   -2.02e-01    0.00e+00    0.00e+00
Vth:           4.00e-01    4.56e-01    4.57e-01    4.00e-01    4.00e-01
Vdsat:         4.53e-01    1.96e-01    1.93e-01    1.98e-01    1.98e-01
Gm:            3.98e-04    9.18e-04    9.31e-04    9.09e-04    9.09e-04
Gds:           8.29e-06    8.66e-06    8.41e-06    8.82e-06    8.82e-06
Gmb:           1.19e-04    2.42e-04    2.45e-04    2.72e-04    2.72e-04
```

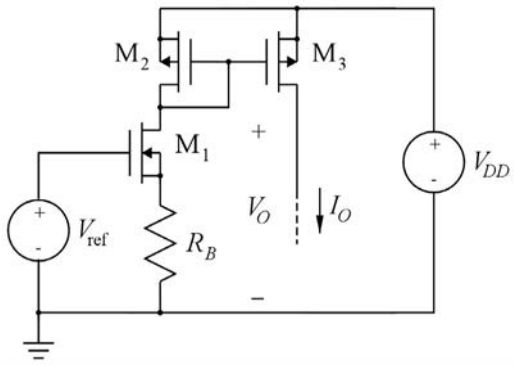
From the error log file, we find $g_{m4} = 0.931$ mA/V, $g_{mb4} = 0.245$ mA/V, $g_{ds4} = 8.41$ µA/V and $g_{ds2} = 8.82$ µA/V, resulting in $r_{out} \simeq [(g_{m4} + g_{mb4})]/g_{ds4})(1/g_{ds2}) \simeq 16$ MΩ. Alternatively, the output resistance may be found from a '.tf' simulation with '`VO`' as the source and '`v(VD4)`' as the output. From this '.tf' simulation, the output resistance is found as the input impedance seen by '`VO`'. The value found by this simulation is 16.1 MΩ, i.e., very close to the calculated value.

The minimum output voltage is found as $V_{O\min} = V_{DS\text{sat}2} + V_{DS\text{sat}4} = 391$ mV $\simeq 400$ mV where the values of the saturation voltages are taken from the error log file. We notice that the bulk effect does not influence the minimum output voltage as the transistor saturation voltages are not affected by the bulk effect. We may also verify the minimum output voltage by a '.op' simulation with '`VO`' swept from 0 to 1.8 V.

The plot from this simulation is shown below and we notice that the output current '`ID4`' drops for $V_O < 0.4$ V as expected.



Problem 8.6



The figure above shows a bias circuit which generates a constant bias current I_O from a bandgap reference voltage $V_{\text{ref}} = 1.25$ V. The supply voltage is $V_{DD} = 1.8$ V and the transistors have the following parameters: $\mu_n C_{ox} = 180$ µA/V^2 and $V_{tn} = 0.4$ V, $\mu_p C_{ox} = 45$ µA/V^2 and $V_{tp} = -0.42$ V.
The channel-length modulation and the body effect can be neglected. All transistors have $W/L = 25$.
Calculate the value of R_B so that the output current is $I_O = 90$ µA, assuming that all transistors are in the active region. Find the maximum output voltage for which all transistors are in the active region.

Now, assume that M_1 has its bulk connected to ground so that the bulk effect cannot be neglected. Also assume that the channel-length modulation must be included for all transistors. Use LTspice with the transistor models from Table 3.1 and a channel length of 1 µm to find a new value for R_B resulting in $I_O = 90$ µA when $V_O = 0.9$ V. Also find the output resistance of the current source when $V_O = 0.9$ V and find the maximum output voltage for which all transistors are in the active region.

For convenience, Table 3.1 is shown in the Appendix in this book.

Solution:

With identical transistors M_2 and M_3, we have $I_{D1} = I_{D2} = I_{D3} = I_O = 90$ µA. With $I_{D1} = 90$ µA, we find from the Shichman-Hodges model:

$$V_{GS1} = V_{tn} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W_1/L_1)}} = 0.6 \text{ V}$$

Using Kirchhoff's voltage law, we find the voltage V_B across R_B as $V_B = V_{\text{ref}} - V_{GS1} = 0.65$ V. Since the current through R_B is I_{D1}, we find from Ohm's law $R_B = V_B/I_{D1} = 7.22$ kΩ.

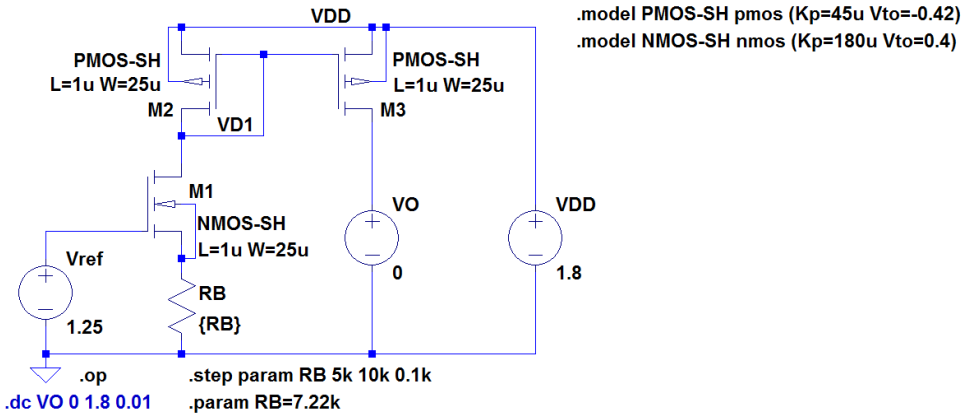
Transistor M_2 is diode-connected, i.e., $V_{D2} = V_{G2}$, so it is in the active region.

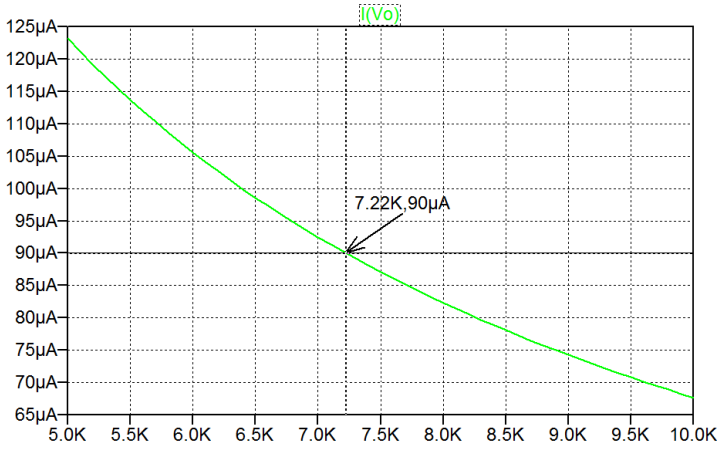
For M_1, $V_{G1} = V_{\text{ref}} = 1.25$ V and $V_{D1} = V_{DD} - |V_{GS2}| = V_{DD} - \left(|V_{tp}| + \sqrt{\frac{2I_{D2}}{\mu_p C_{ox}(W_2/L_2)}}\right) = 0.98$ V.

Thus, $V_{D1} > V_{G1} - V_{tn} = 0.85$ V, so M_1 is in the active region.

Transistor M_3 is in the active region for $V_O = V_{D3} \leq V_{G3} - V_{tp} = V_{D1} - V_{tp} = 0.98 \text{ V} - (-0.42 \text{ V}) = 1.4$ V.

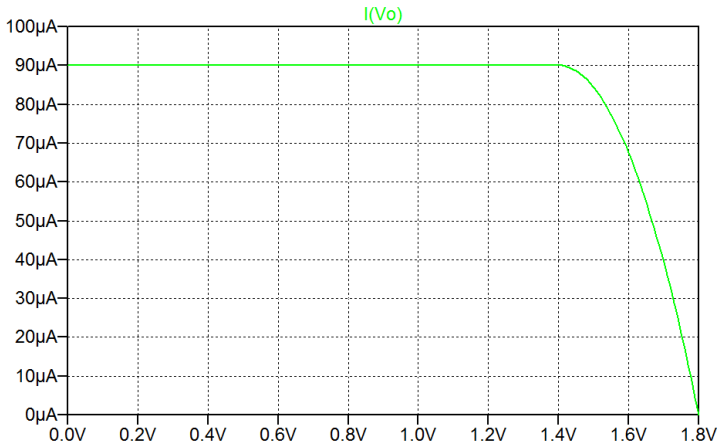
The problem may also be solved using LTspice. The following figure shows an LTspice schematic in which the value of R_B is defined as a parameter stepped through a suitable interval and with the output voltage defined as 0 V, ensuring that M_3 is in the active region. From a '.op' simulation, we may plot the output current versus R_B. From the plot, we find that $R_B = 7.22$ kΩ results in $I_O = 90$ µA.



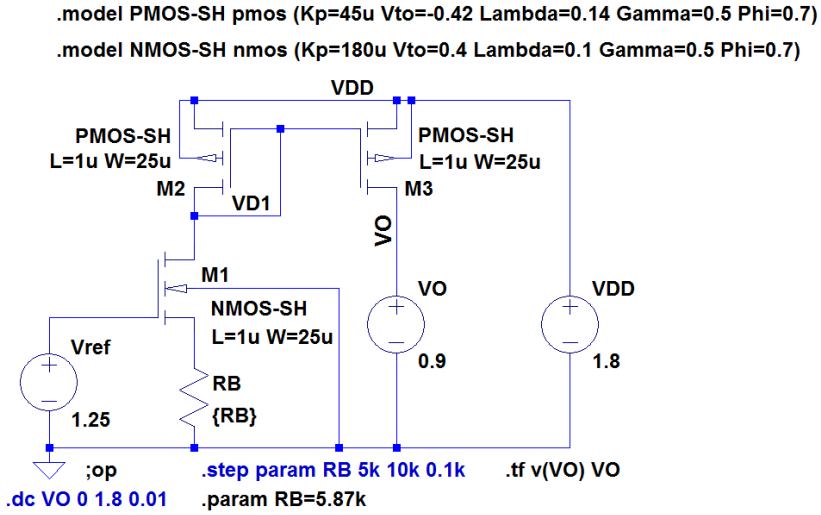


For finding the maximum output voltage, we run a '.dc' simulation with V_O as the source while defining $R_B = 7.22$ kΩ using a '.param' directive as shown in the LTspice schematic. For the '.dc' simulation, the '.step' directive must be changed into a comment.

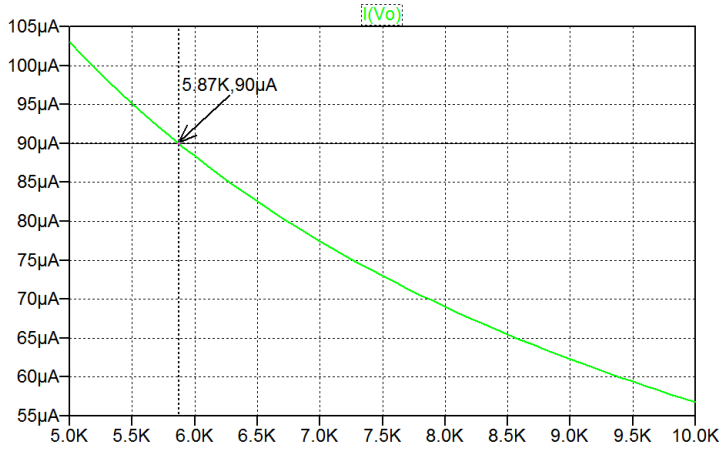
The resulting plot of I_O is shown below. We see that I_O is constant and equal to 90 µA for $V_O \leq 1.4$ V. For $V_O > 1.4$ V, the output current drops as M_3 enters the triode region.



When the bulk of M_1 is connected to ground and the channel-length modulation is also included, the LTspice schematic must be modified as shown in the following figure.

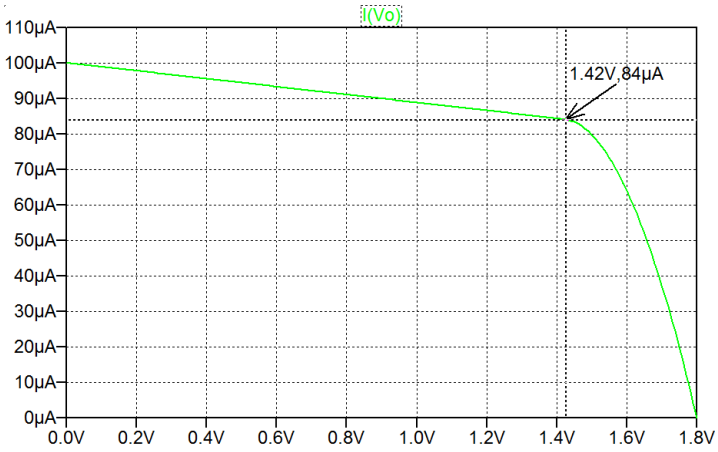


Running the same simulations as before, we find I_O versus R_B as shown in the figure below. We find $R_B = 5.87$ kΩ for $I_O = 90$ µA.

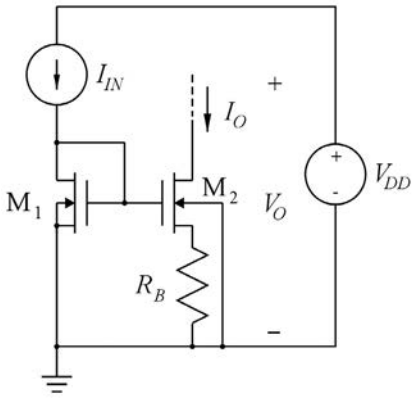


For finding the output resistance and the maximum output voltage, we notice that the output resistance of the current mirror M_2 - M_3 is the small-signal output resistance $r_{ds3} = 1/g_{ds3}$ of M_3 and that the maximum output voltage with all transistors in the active region is $V_{O\max} = V_{DD} - |V_{DSsat3}|$. Both g_{ds3} and V_{DSsat3} can be found from the error log file after a '.op' simulation. From the error log file, we find $g_{ds3} = 11.2$ µA/V and $V_{DSsat3} = -0.377$ V, resulting in an output resistance of 89.3 kΩ and a maximum output voltage of 1.42 V.

The output characteristics may also be illustrated by a'.dc' simulation with V_O as the source with $R_B = 5.87$ kΩ. This results in the following plot where we find $V_{O\max} = 1.42$ V. We note from the plot that I_O now depends on V_O, indicating that the current source has a finite output resistance. The output resistance may be found from the slope of I_O versus V_O or it may be found as the input impedance from a '.tf' simulation with '`v(VO)`' as the output and '`VO`' as the source. For both methods, we find an output resistance of 89.4 kΩ.



Problem 8.7



The figure above shows a Widlar current source used to generate a small dc output current I_O. Assume that M_1 and M_2 are two identical transistors with a channel length of 1 µm and a channel width of 5 µm and they have transistor parameters as specified in Table 3.1. The input current is $I_{IN} = 50$ µA and the supply voltage is $V_{DD} = 1.8$ V.
Use LTspice to find the value of R_B resulting in an output current $I_O = 5$ µA when $V_O = 0.9$ V.
From the LTspice simulation, find g_{m2}, g_{mb2} and r_{ds2} and calculate the small-signal output resistance, assuming an output voltage of $V_O = 0.9$ V. Also find the output resistance by an LTspice simulation.

For convenience, Table 3.1 is shown in the Appendix in this book.

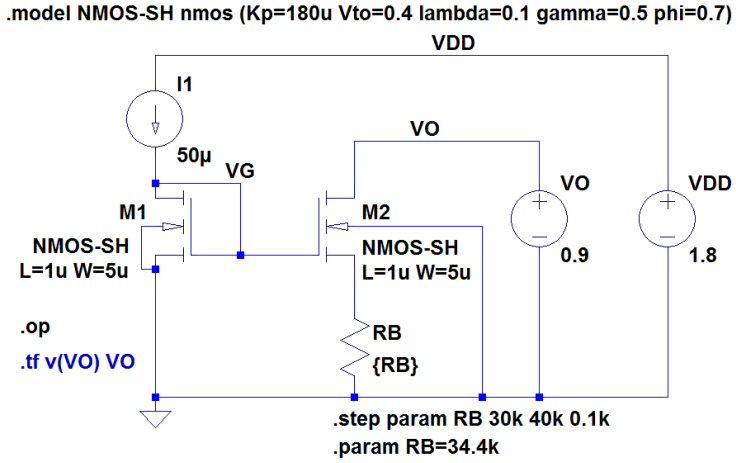
Solution:

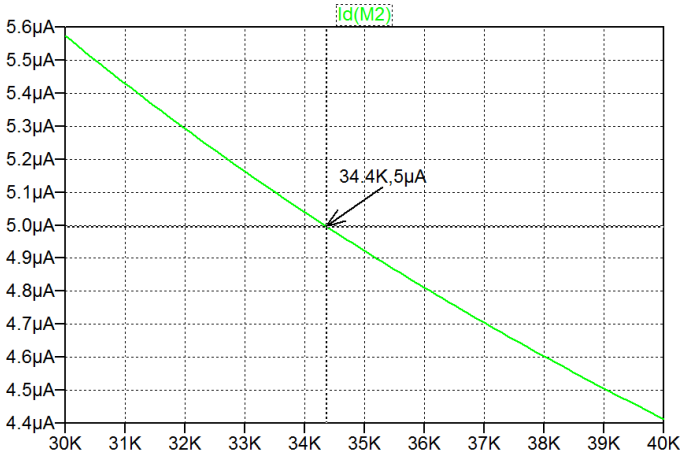
The following figure shows an LTspice schematic corresponding to Problem 8.7. The value of R_B is defined as a parameter and using a '.step' directive, R_B is swept through the range from 30 kΩ to 40 kΩ. From a '.op' simulation, the output current may be plotted as the drain current of M_2 versus the resistor value as shown in the following plot. From the plot, we find that $R_B = 34.4$ kΩ results in $I_O = 5$ µA with $V_O = 0.9$ V.

Running a '.op' simulation with R_B defined by a '.param' directive and the '.step' directive changed into a comment, we may find the transistor small-signal parameters from the error log file.
We find $g_{m2} = 98.2$ µA/V, $g_{mb2} = 26.3$ µA/V and $r_{ds2} = 1/g_{ds2} = (0.465\ \mu\text{A/V})^{-1} = 2.15$ MΩ.

The small-signal output resistance may be calculated using Eq. (4.25) from Bruun (2022):
$r_{out} \simeq r_{ds2} + (g_{m2} + g_{mb2}) r_{ds2} R_B = 11.4\ \text{M}\Omega$.

The output resistance may be found from a '.tf' simulation with '`VO`' as the source and '`v(VO)`' as the output. From this '.tf' simulation, the output resistance is found as the input impedance seen by '`VO`'. The value found by this simulation is 11.4 MΩ, i.e., the same as the calculated value.



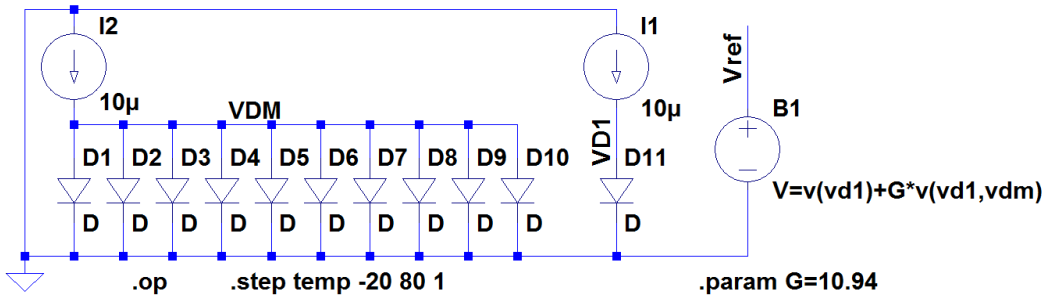


Problem 8.8

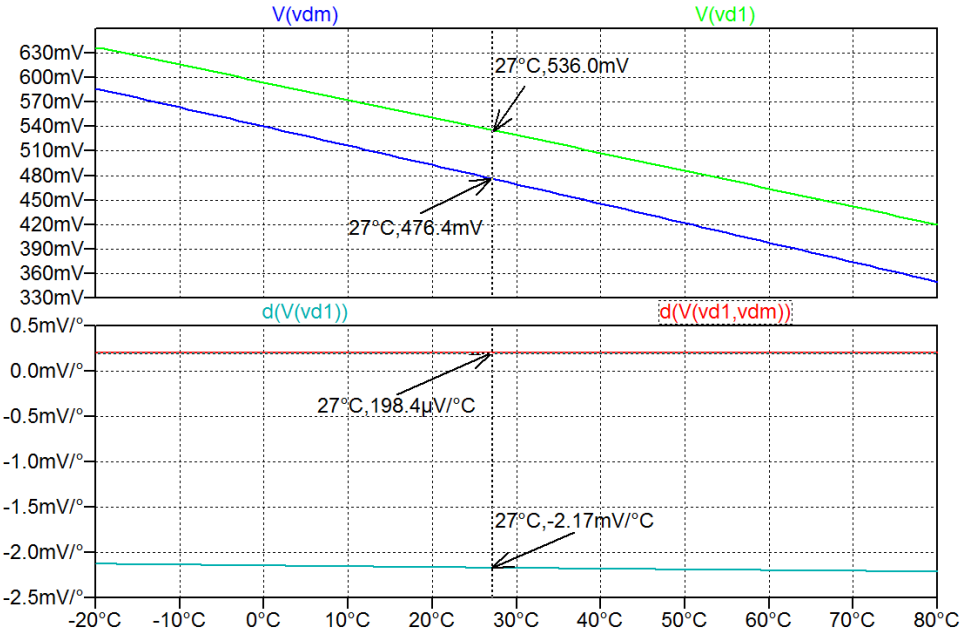
Using the LTspice default diode model, find the diode voltage V_{D1} and the temperature coefficient $\partial V_{D1}/\partial T$ for a single diode with $I_D = 10\ \mu\text{A}$ at room temperature, i.e., a temperature of 27°C. Also find the diode voltage V_{DM} for 10 parallel-connected diodes with a total current of 10 µA, and find the temperature coefficient of $V_{D1} - V_{DM}$ at room temperature.
For $V_{\text{ref}} = V_{D1} + G(V_{D1} - V_{DM})$, find G so that $\partial V_{\text{ref}}/\partial T = 0$ at room temperature and find the resulting value of V_{ref}.

Solution:

Shown in the following is an LTspice schematic with 10 parallel-connected diodes D_1 to D_{10} and a single diode D_{11}. The parallel-connected diodes are supplied by the 10 µA current source '`I2`' and the single diode D_{11} is supplied by the 10 µA current source '`I1`'. Also included is an arbitrary behavioral voltage source '`B1`' generating the reference voltage $V_{\text{ref}} = V_{D1} + G(V_{D1} - V_{DM})$ where G is defined as a parameter. For the initial simulation, G may be selected to a value of 10.



In order to find the diode voltages V_{D1} and V_{DM}, a '.op' simulation is run with the temperature stepped from -20°C to $+80$°C. From the simulation, we plot both the diode voltages V_{D1} and V_{DM} versus temperature and the temperature coefficients of V_{D1} and $(V_{D1} - V_{DM})$ as shown in the following figure.

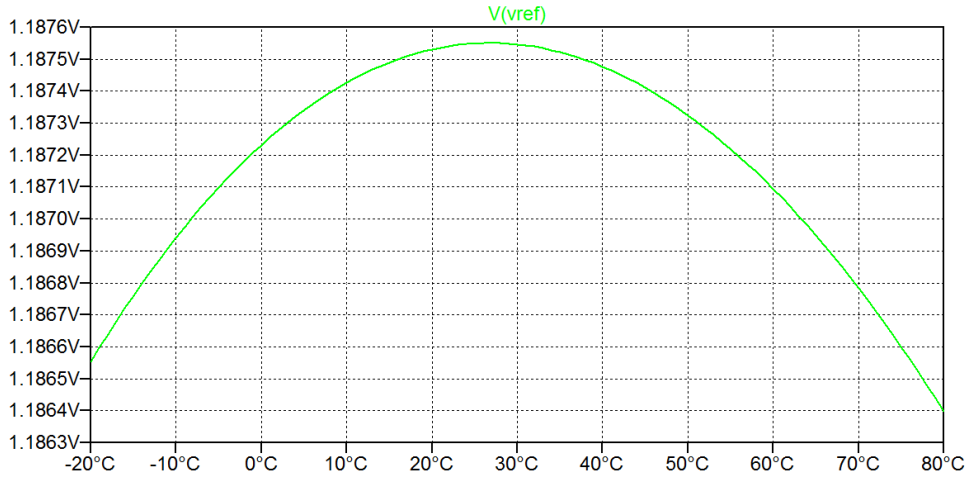


We find the diode voltages $V_{D1} = 536.0$ mV and $V_{DM} = 476.4$ mV and the temperature coefficients $\partial V_{D1}/\partial T = -2.17$ mV/°C and $\partial(V_{D1} - V_{DM})/\partial T = 0.1984$ mV/°C.

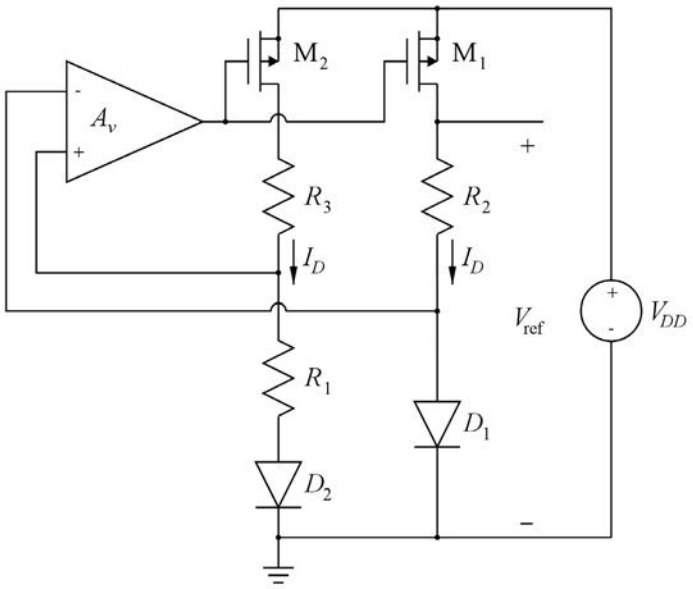
We may now calculate the parameter G from Eq. (8.24) in Bruun (2022):

$$G = -\frac{\partial V_D/\partial T}{\partial \Delta V_D/\partial T} = 10.94$$

Running a new '.op' simulation with $G = 10.94$, we find V_{ref} versus temperature as shown in the plot below. We find a reference voltage of $V_{\text{ref}} = 1.1876$ V $\simeq 1.19$ V at room temperature with a variation of less than 1.15 mV over the temperature range from -20°C to $+80$°C.



Problem 8.9



The figure above shows a bandgap reference circuit. An amplifier with the voltage gain A_v establishes a feedback loop controlling the current in the two identical PMOS transistors M_1 and M_2. The diode D_2 is composed of 10 parallel-connected diodes, each identical to diode D_1. The resistors are $R_1 = 6\ \text{k}\Omega$ and $R_2 = R_3 = 65\ \text{k}\Omega$, and the amplifier has a gain $A_v = 1000$ V/V. The supply voltage is $V_{DD} = 1.8$ V. For the transistors, assume a drain current $I_D = 10\ \mu\text{A}$ and an effective gate voltage $|V_{GS} - V_{tp}| = 0.2$ V. The transistors are in the active region and the channel-length modulation can be neglected.

Find an expression for the loop gain by breaking the loop at the output of the amplifier and applying a test voltage V_{test} to the gate of M_1 and M_2, resulting in a returned voltage V_r at the output of the amplifier. The diodes have identical small-signal resistances $r_{d1} = r_{d2} = V_T/I_D$ where V_T is the thermal voltage. Calculate the numerical value of the loop gain.

Find an expression for the small-signal gain $\partial V_{\text{ref}}/\partial V_{DD}$ and calculate the numerical value when the feedback loop is open and the dc value of V_{test} is applied to the gate of M_1 and M_2.

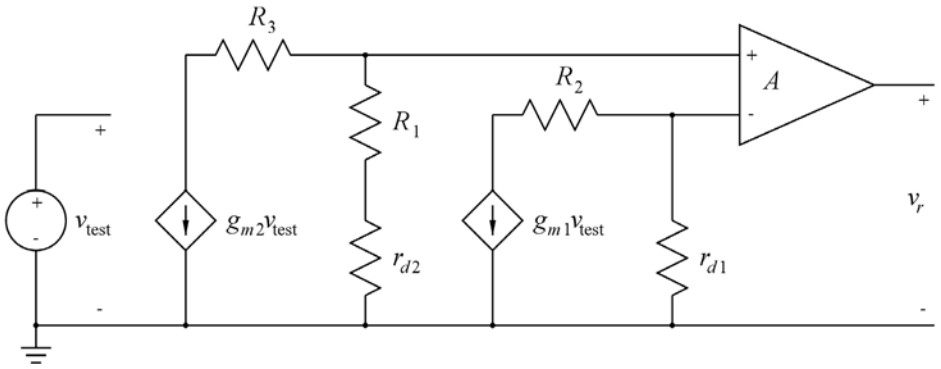
Find an expression for $\partial V_{\text{ref}}/\partial V_{DD}$ when the feedback loop is closed and calculate the numerical value.

Solution:

For finding the loop gain, we use the following small-signal diagram.
Using $g_{m1} = g_{m2} = g_m = 2I_D/|V_{GS} - V_{tp}|$ and $r_{d1} = r_{d2} = r_d$, we find

$$v_r = A(-g_{m2}v_{\text{test}}(R_1 + r_{d2}) - (-g_{m1}v_{\text{test}}r_{d1})) = -g_m R_1 A v_{\text{test}}$$

From this, we find the loop gain $L = -v_r/v_{\text{test}} = g_m R_1 A$. Inserting $g_m = 2I_D/|V_{GS} - V_{tp}| = 100$ µA/V, we find $L = 600$ V/V.



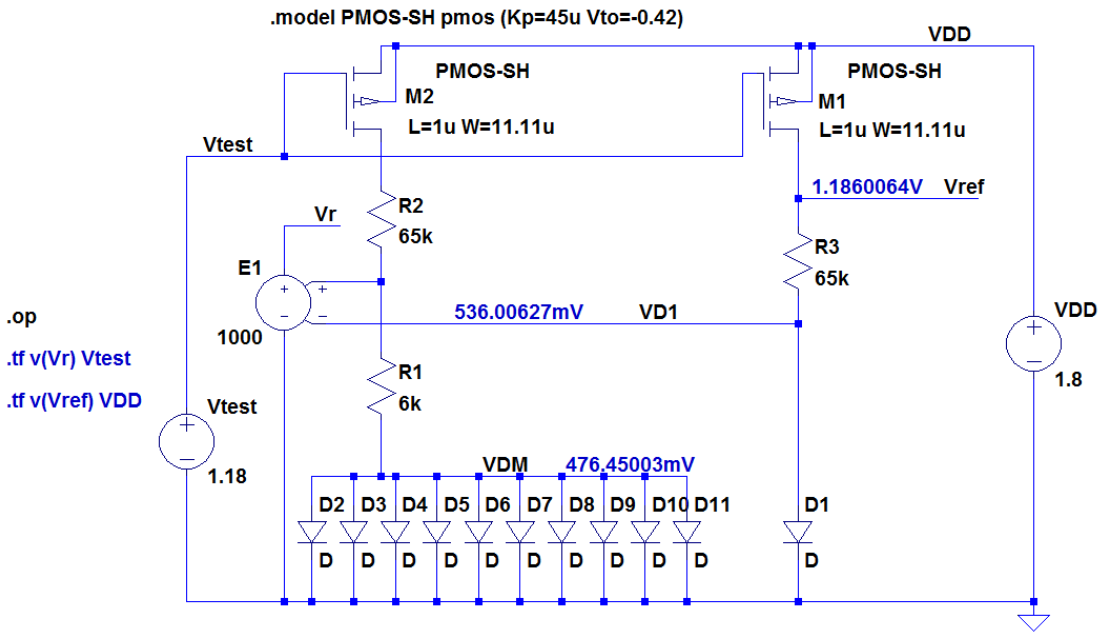
For finding the small-signal gain $\partial V_{\text{ref}}/\partial V_{DD}$ when the feedback loop is open, we notice that M_1 operates as a common-gate stage with a load of $(R_2 + r_{d1})$. Hence, the gain is $\partial V_{\text{ref}}/\partial V_{DD} = g_{m1}(R_2 + r_{d1})$, compare to Eq. (4.22) in Bruun (2022). Inserting $g_{m1} = 100$ µA/V and $r_{d1} = V_T/I_D = 2.6$ kΩ at room temperature, we find $\partial V_{\text{ref}}/\partial V_{DD} = 6.76$ V/V.

When the feedback loop is closed, the gain $\partial V_{\text{ref}}/\partial V_{DD}$ is reduced by a factor equal to the amount of feedback. With a loop gain much larger than 1, the amount of feedback is approximately equal to the loop gain, so $\partial V_{\text{ref}}/\partial V_{DD} \simeq ((R_2 + r_{d1})/R_1)/A = 11.3$ mV/V. The circuit may also be analyzed using LTspice. In order to design an LTspice schematic, we calculate the transistor dimensions for M_1 and M_2 using the Shichman-Hodges model with $\mu_p C_{ox} = 45$ µA/V^2, $V_{tp} = -0.42$ V and $L = 1$ µm. From this, we find

$$W = L\frac{2I_D}{\mu_p C_{ox}(V_{GS} - V_{tp})^2} = 11.11 \text{ µm}$$

For the diodes D_1 and D_2, we may just use the default LTspice diode with a single diode for D_1 and 10 parallel-connected diodes for D_2.

Shown below is the LTspice schematic with the feedback loop open and a test voltage v_{test} applied to the gate of M_1 and M_2. The test voltage has a dc value of $V_{DD} - |V_{GS1}| = V_{DD} - |V_{tp}| - |V_{GS} - V_{tp}| = 1.18$ V.



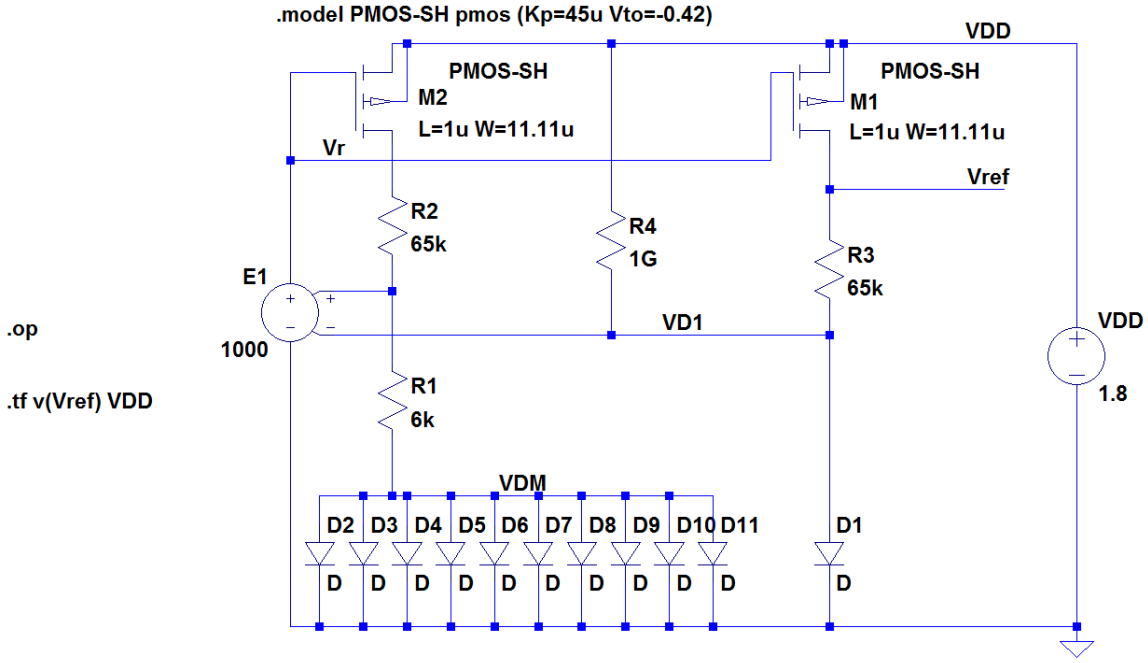
We may start by running a '.op' simulation in order to verify the bias point of the circuit. From the '.op' simulation, we find the diode voltages and the reference voltage indicated in the schematic. These voltages correspond very well to the voltages found in Problem 8.8. We also find the currents in the transistors and diodes to have the expected values.

Next, we may find the loop gain from a '.tf' simulation with '`Vtest`' as the source and '`v(Vr)`' as the output. The output file from the '.tf' simulation shows a gain of -599.94 V/V, i.e., a loop gain of $+599.94$ V/V, corresponding very well to the value calculated from the small-signal model used for the theoretical calculation.

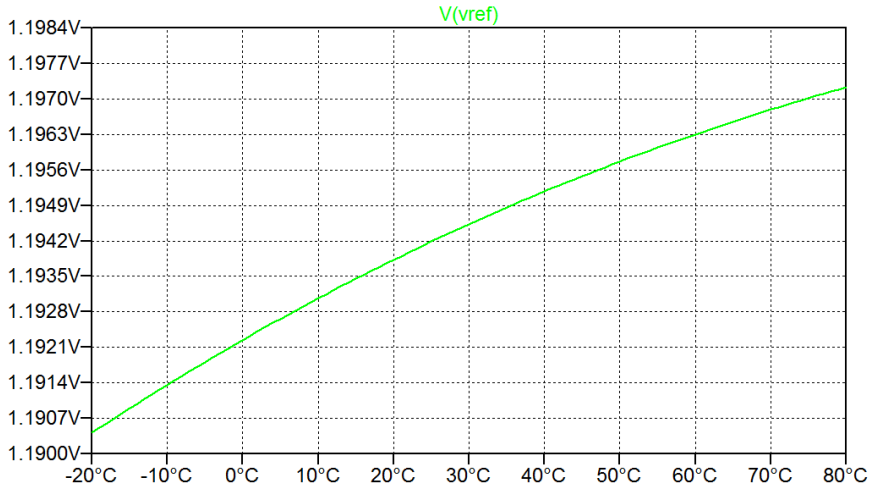
The gain $\partial V_{\text{ref}}/\partial V_{DD}$ with the feedback loop open is found from a '.tf' simulation with '`VDD`' as the source and '`v(Vref)`' as the output. We find a gain of 6.758 V/V, closely matching the value calculated from the small-signal model.

We may now delete the test voltage and close the feedback loop as shown in the following LTspice schematic. A '.op' simulation will show a bias point with an extremely small current in the transistors and diodes, so a start-up resistor R_4 must be added as shown below. The value of R_4 is large enough that it does not significantly influences the performance of the circuit but it ensures that the circuit finds a bias point with $I_D = 10$ µA.

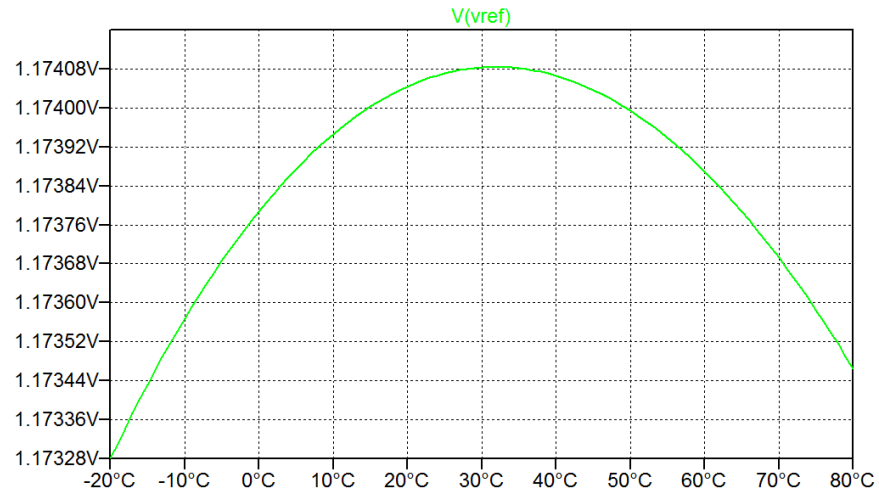
The gain $\partial V_{\text{ref}}/\partial V_{DD}$ with the feedback loop closed is found from a '.tf' simulation with '`VDD`' as the source and '`v(Vref)`' as the output. We find a gain of 0.0112712 V/V $\simeq$ 11.3 mV/V, closely matching the value calculated from the small-signal model.



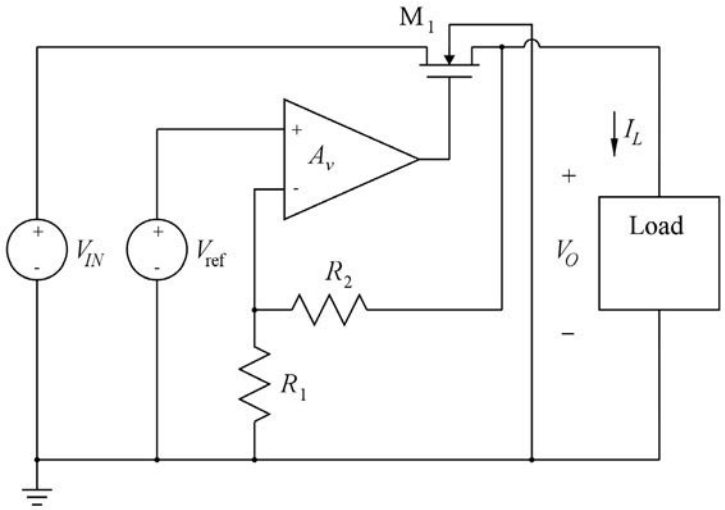
As an additional analysis, we may run a '.op' simulation with a sweep of the temperature using the directive '`.step temp -20 80 1`'. From this simulation, we may plot V_{ref} versus temperature. The resulting plot is shown in the following figure.



We notice a non-zero temperature coefficient at room temperature. The reason for this is that the gain factor for $\Delta V_D = V_{D1} - V_{DM}$ has not been optimized. Optimizing the gain as described in Chapter 8.3 in Bruun (2022), we find that the performance is improved if R_2 and R_3 are changed from 65 kΩ to 63 kΩ. A new simulation with this value for R_2 and R_3 results in the plot of V_{ref} versus temperature shown below.



Problem 8.10



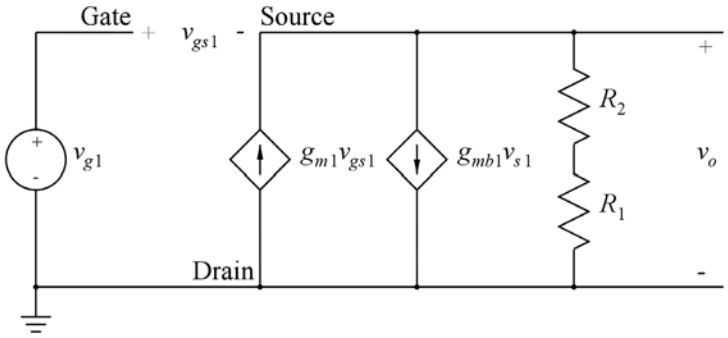
The figure above shows a voltage regulator with an NMOS pass transistor M_1. Assume that the channel-length modulation for M_1 can be neglected and that it has a gate transconductance of $g_{m1} = 100$ mA/V and a bulk transconductance of $g_{mb1} = 20$ mA/V. The resistors are $R_1 = 100$ kΩ and $R_2 = 20$ kΩ, i.e., both R_1 and R_2 are much larger than $1/g_{m1}$. The load can be modeled as a dc current source with a value of 10 mA and the amplifier has a gain of $A_v = 1000$ V/V.
Find an expression for the loop gain in the feedback loop controlling V_O, and find an expression for the load regulation $\partial V_O/\partial I_L$ and calculate the numerical results.

Solution:

Referring to general feedback theory (Bruun 2022, Chapter 6), the feedback loop consists of the voltage divider R_1 and R_2 as the β-circuit and the amplifier A, the transistor M_1 and the load as the A-circuit.

From the β-circuit, we find $\beta = R_1/(R_1+R_2) = 0.833$ V/V.

In the A-circuit, transistor M_1 is operating as a source follower loaded by R_1+R_2 from the β-circuit and by the small-signal resistance of the load. Since the load can be modeled as a dc current source, i.e., an infinite small-signal resistance, it presents no load to the source follower. A small-signal model of the source follower is shown below.



From a node equation at the output, we find $g_{m1}v_{gs1} = g_{mb1}v_{s1} + v_o/(R_1+R_2)$ and using $v_{s1} = v_o$ and $v_{gs1} = v_{g1} - v_o$, we find

$$g_{m1}(v_{g1}-v_o) = g_{mb1}v_o + v_o/(R_1+R_2) \;\Rightarrow\; \frac{v_o}{v_{g1}} = \frac{g_{m1}}{g_{m1}+g_{mb1}+1/(R_1+R_2)} \simeq \frac{g_{m1}}{g_{m1}+g_{mb1}} = 0.833 \text{ V/V}$$

where we have assumed $R_1+R_2 \gg 1/g_{m1}$.

Thus, the total loop gain is $L \simeq \beta A \left(\frac{g_{m1}}{g_{m1}+g_{mb1}}\right) = A \left(\frac{R_1}{R_1+R_2}\right)\left(\frac{g_{m1}}{g_{m1}+g_{mb1}}\right) = 694$ V/V.

The load regulation $\partial V_O/\partial I_L$ is found from the resistance to ground at the source of M_1. With the feedback loop open, this resistance is equal to R_1+R_2 in parallel with the output resistance of the source follower M_1. This output resistance is given by Eq. (4.18) in Bruun (2022), i.e., $r_{out} \simeq 1/(g_{m1}+g_{mb1})$. With $R_1+R_2 \gg 1/g_{m1}$, we may neglect R_1+R_2.

When the feedback loop is closed, the output resistance is reduced by a factor equal to the amount of feedback, i.e., $1+L$. Thus, with $L \gg 1$, we find

$$\begin{aligned}\frac{\partial V_O}{\partial I_L} &= -r_{outCL} \simeq -\left(\frac{1}{g_{m1}+g_{mb1}}\right)\left(\frac{1}{A_v(R_1/(R_1+R_2))(g_{m1}/(g_{m1}+g_{mb1}))}\right) \\ &= -\left(\frac{1}{A_v\, g_{m1}}\right)\left(1+\frac{R_2}{R_1}\right) = -12 \text{ mV/A}.\end{aligned}$$

The circuit may also be analyzed using LTspice. A simple approach for verifying the loop gain is to enter the small-signal model into LTspice and run a '.tf' simulation. However, here we show a more elaborate analysis performed from the circuit schematic shown in Problem 8.10. This provides a deeper insight into the operation of the circuit. For this analysis, we must first design the transistor M_1, and we must assume specific values of V_{ref}, V_{IN} and I_L.

Let us assume that V_{ref} is the output voltage of a bandgap reference circuit giving $V_{\text{ref}} = 1.25$ V. With a high loop gain, the output voltage V_O is $V_O = (1+R_2/R_1)V_{\text{ref}} = 1.5$ V.

For the transistor, we need some device parameters for the Shichman-Hodges model for LTspice. We may assume $V_{to} = 0.4$ V and $\mu_n C_{ox} = 180$ μA/V^2, corresponding to typical values for a 0.18 μm process. Neglecting the channel-length modulation, we have $\lambda = 0$. The body effect cannot be neglected since bulk and source are not connected. The parameters γ and $|2\Phi_F|$ may be found from Eq. (3.76) in Bruun (2022):

$$\frac{g_{mb}}{g_m} = \chi = \frac{\gamma}{2\sqrt{V_{SB}+|2\Phi_F|}}$$

Assuming $|2\Phi_F| = 0.7$ V and using $V_{SB} = V_O = 1.5$ V, we find with $g_{m1} = 100$ mA/V and $g_{mb1} = 20$ mA/V that $\gamma = 2\chi\sqrt{V_O + |2\Phi_F|} = 0.59\ \sqrt{\text{V}}$.

We may notice that $V_t = V_{to} + \gamma\left(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|}\right) = 0.78$ V. Thus, the amplifier A_v must be able to deliver an output voltage which is higher than $V_t + V_O = 2.28$ V. For delivering an output current of 10 mA, M_1 needs an effective gate voltage of $V_{\text{eff1}} = 2I_{D1}/g_{m1} = 0.2$ V, so the required output voltage from the amplifier is 2.48 V.

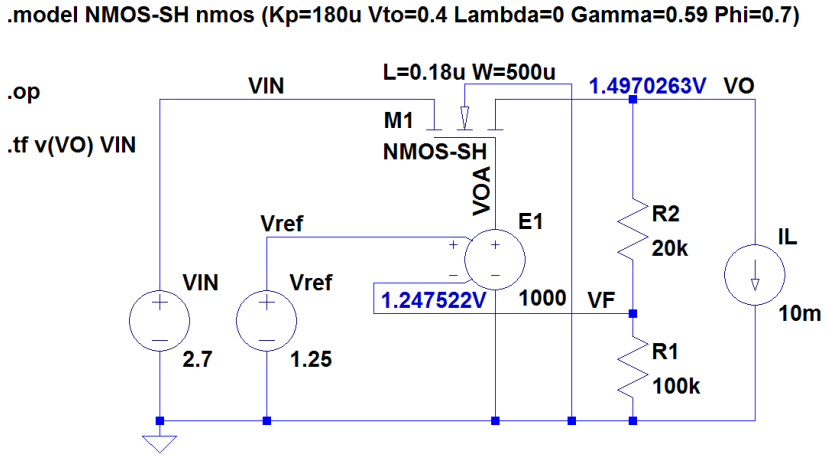
With $g_{m1} = 100$ mA/V and $V_{\text{eff1}} = 0.2$ V, we may use Eq. (3.70) from Bruun (2022) to find W_1/L_1:

$$\frac{W_1}{L_1} = \frac{g_{m1}}{\mu_n C_{ox} V_{\text{eff1}}} = 2778$$

Selecting $L_1 = 0.18$ µm, we find $W_1 = 500$ µm.

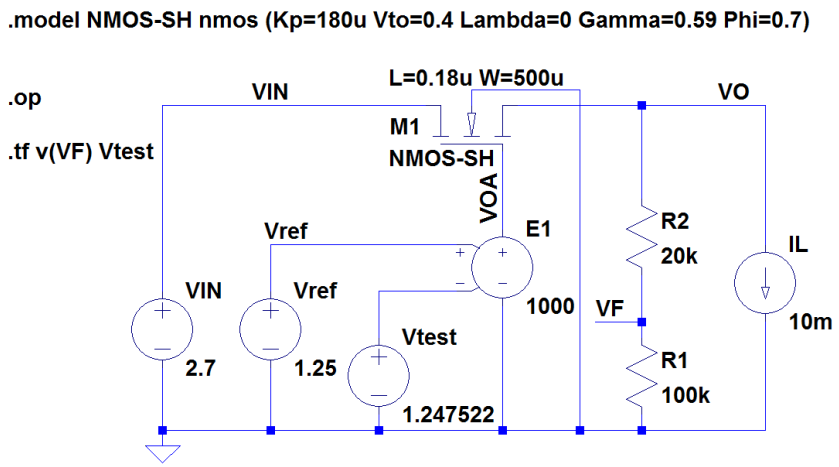
For the input voltage, we may select $V_{IN} = 2.7$ V, i.e., slightly higher than the required output voltage from the amplifier, and with the values of voltages, currents and transistor parameters calculated above, we arrive at the following LTspice schematic corresponding to Problem 8.10.

Running a '.op' simulation, we find the dc values of V_O and the feedback voltage V_F shown in the schematic. We also find the value of the output voltage of the amplifier to be 2.47804 V, i.e., voltage levels corresponding to the values calculated above. From the error log file, we find $g_{m1} = 100$ mA/V and $g_{mb1} = 19.9$ mA/V, i.e., values matching the specified values very closely. Also, we find $V_t = 0.781$ V, again matching the calculated value.

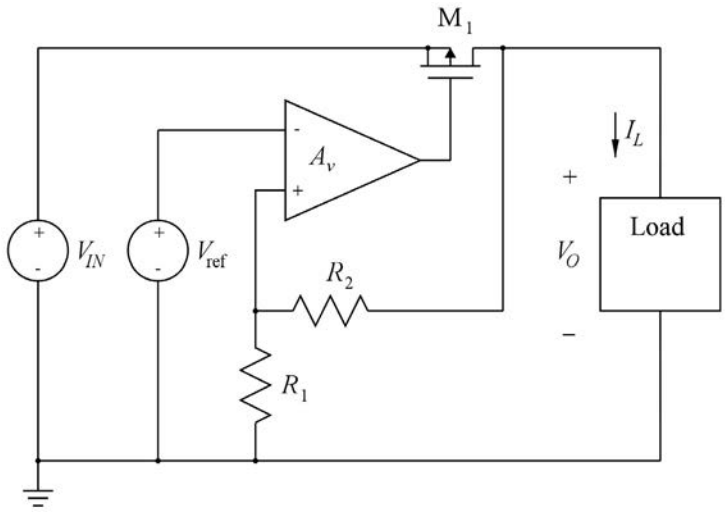


For finding the load regulation, we run a '.tf' simulation with '`v(VO)`' as the output and '`VIN`' as the input. From this simulation, the load regulation $\partial V_O/\partial I_L$ is found from the output impedance r_{outCL} at V_O as $\partial V_O/\partial I_L = -r_{outCL}$. We find $\partial V_O/\partial I_L = -11.98$ mV/A which closely matches the calculated value. The '.tf' simulation also shows a transfer function from V_{IN} to V_O of 1.198×10^{-14}, i.e., an almost perfect line regulation. However, this is an unrealistic result caused by neglecting the channel-length modulation. Changing the value of λ from 0 to $(0.10\ \mu\text{m/V})/0.18\ \mu\text{m} = 0.555\ \text{V}^{-1}$, we find a line regulation of about 0.031 mV/V which is still a very good line regulation.

In order to simulate the loop gain, the loop is broken at the inverting input to the controlled voltage source 'E1' and a test input voltage 'Vtest' is applied to the inverting input of 'E1' as shown below. This test voltage is given a dc value equal to the dc value found for 'VF' when simulating the circuit with the feedback loop closed. From a '.op' simulation, we may verify that the bias point for M_1 remains the same as when the feedback loop is closed and from a '.tf' simulation with 'v(VF)' as the output and 'Vtest' as the input, we find a small-signal gain $V_F/V_{\text{test}} = -694.961$ V/V. The loop gain L is equal to $-V_F/V_{\text{test}}$ (Bruun 2022), so the simulated value of the loop gain is $L = 695$ V/V, closely matching the calculated value.



Problem 8.11



The figure above shows a voltage regulator with a PMOS pass transistor M_1. The load is a dc current source with a value of 10 mA and the amplifier has a gain of $A_v = 1000$ V/V. The transistor has $\mu_p C_{ox}(W/L) = 500$ mA/V^2, $V_t = -0.42$ V and $\lambda = 0.7$ V^{-1}. The resistors are $R_1 = 100$ kΩ and $R_2 = 20$ kΩ. V_{ref} is a bandgap reference voltage with a value of 1.25 V and a line regulation of $\partial V_{\text{ref}}/\partial V_{IN} = 10$ mV/V. The input voltage V_{IN} has a nominal value of 1.8 V with a ripple of 0.2 V superimposed on the nominal value.

Find the nominal value of the regulated output voltage V_O and find the ripple on the output voltage. Also find the load regulation and the line regulation for the voltage regulator, including the bandgap reference circuit.

Solution:

Assuming a large loop gain, we find from Eq. (8.31) in Bruun (2022) $V_O = V_{\text{ref}}(1+R_2/R_1) = 1.5$ V.

The loop gain in the circuit is $L = A_v g_{m1}(r_{ds1} \parallel (R_1+R_2))R_1/(R_1+R_2)$ where g_{m1} is found from Eq. (3.66) and r_{ds1} is found from Eq. (3.68) in Bruun (2022). With $V_{IN} = 1.8$ V and $V_O = 1.5$ V, we find $|V_{DS1}| = 0.3$ V and inserting the numerical values, we find $g_{m1} = 110$ mA/V and $r_{ds1} = 173\ \Omega$, resulting in a loop gain $L \simeq 15860$. We notice that the loop gain is indeed $\gg 1$, so the approximation used for finding V_O is reasonable.

The load regulation $\partial V_O/\partial I_L$ is found from the output resistance as $\partial V_O/\partial I_L = -r_{out}$. Using Eq. (8.35) from Bruun (2022), we find

$$\frac{\partial V_O}{\partial I_L} \simeq -\left(\frac{1}{g_{m1}}\right)\left(\frac{1}{A_v}\right)\left(1+\frac{R_2}{R_1}\right) = -10.9\ \text{m}\Omega = -10.9\ \text{mV/A}$$

Using the superposition principle, the line regulation is found from the gain from V_{IN} to V_O via the bandgap reference voltage V_{ref} plus the gain from V_{IN} to V_O via the pass transistor. The gain from V_{IN} to V_{ref} is 10 mV/V, and the gain from V_{ref} to V_O is $(1+R_2/R_1) = 1.2$, implying that the gain from V_{IN} via the bandgap reference is 12 mV/V.

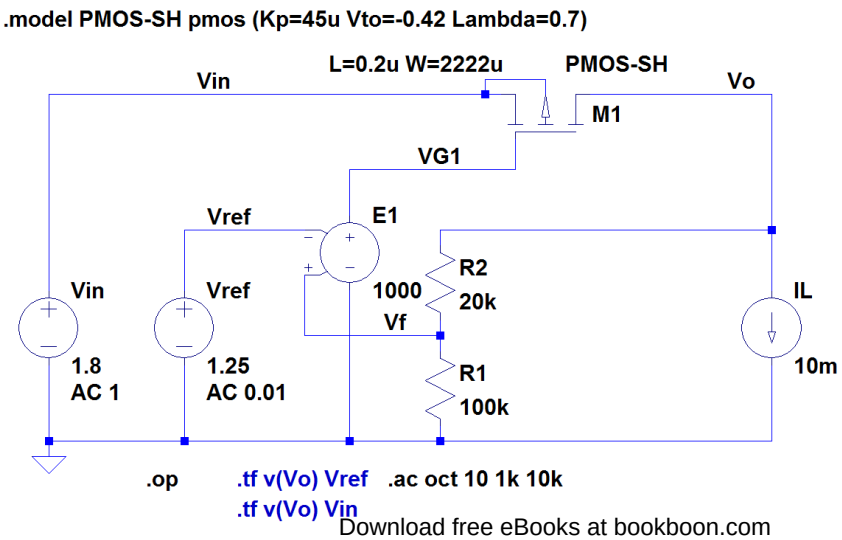
The gain from V_{IN} to V_O via the pass transistor is found using Eq. (8.34) from Bruun (2022), i.e.,

$$\frac{\partial V_O}{\partial V_{IN}} \simeq \left(\frac{1}{A_v}\right)\left(1+\frac{R_2}{R_1}\right) = 1.2\ \text{mV/V}$$

Thus, the total line regulation is $\partial V_O/\partial V_{IN} = 12\ \text{mV/V} + 1.2\ \text{mV/V} = 13.2$ mV/V.

With an input ripple of 0.2 V, this results in an output ripple of $0.2\ \text{V} \times 13.2\ \text{mV/V} = 2.64$ mV.

The circuit may also be analyzed using LTspice. The following figure shows an LTspice schematic corresponding to Problem 8.11. The transistor is modeled using '`Kp`' = 45 μA/V^2, corresponding to the Shichman-Hodges model parameters from Table 3.1 in Bruun (2022). With $\mu_p C_{ox}(W/L) = 500$ mA/V^2, we find $W/L = 11111$ and using $L = 0.2$ μm, corresponding to $\lambda = 0.7\ \text{V}^{-1}$, we find $W = 2222$ μm.

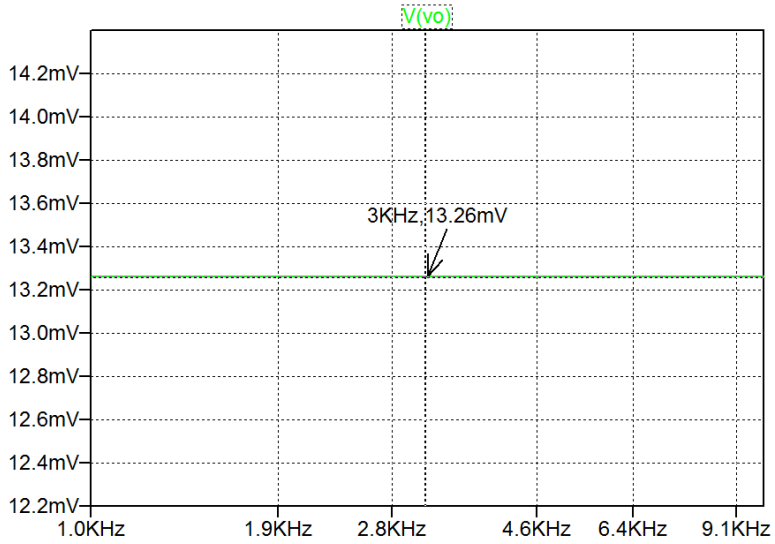


We may run a '.op' simulation to verify the bias point and the small-signal parameters calculated above. From the output file, we find $V_O = 1.5$ V, and from the error log file, we find $g_{m1} = 110$ mA/V and $g_{ds1} = 5.80$ mA/V, matching the calculated values.

For finding the load regulation, we may run a '.tf' simulation with '`v(Vo)`' as the output and '`Vin`' as the source. From the output file, we find an output resistance of 10.9 mΩ corresponding to a load regulation of $\partial V_O/\partial I_L = -10.9$ mV/A .

We also find a gain from V_{IN} to V_O of 1.26 mV/V, assuming a constant value of V_{ref}. Running another '.tf' simulation with '`v(Vo)`' as the output and '`Vref`' as the source, we find a gain from V_{ref} to V_O of 1.2 V/V and with a line regulation of 10 mV/V for the bandgap voltage, this results in a gain of 12 mV/V from V_{IN} to V_O via the bandgap reference voltage. Thus, the total gain from V_{IN} to V_O is 13.26 mV/V, i.e., a line regulation of 13.26 mV/V.

Alternatively, the line regulation may be found from a '.ac' simulation where the ac value of V_{IN} is specified to 1 and the ac value of V_{ref} is specified to 0.01, corresponding to a line regulation of the bandgap voltage of 0.01 V/V. Shown below is the plot from this simulation. Notice that a linear y-axis has been selected. We find the line regulation to be 13.26 mV/V as also found from the '.tf' simulations.



References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Appendix – Transistor Models

The parameters from Table 3.1 in Bruun (2022) are used in several problems. For convenience, Table 3.1 is shown below.

Parameter:	μC_{ox}	V_{to}	$\lambda^{'} = \lambda L$	γ	$\lvert 2\Phi_F \rvert$
NMOS:	180 µA/V^2	0.40 V	0.10 µm/V	0.5 $\sqrt{\text{V}}$	0.7 V
PMOS:	45 µA/V^2	−0.42 V	0.14 µm/V	0.5 $\sqrt{\text{V}}$	0.7 V

Table 3.1: Shichman-Hodges transistor parameters for a generic 0.18 µm CMOS process.

Also the BSIM3 transistor models from Fig. 3.44 in Bruun (2022) are used in some problems. For convenience, Fig. 3.44 is shown below.

Generic BSIM3 model for 0.18 µm CMOS process. Adapted from 'http://ptm.asu.edu/modelcard/180nm_bulk.txt '.

```
* Predictive Technology Model Beta Version
* 180nm NMOS SPICE Parametersv (normal one)
.model NMOS-BSIM NMOS
+Level=49
+Lint=4.e-08              Tox=4.e-09
+Vth0=0.3999              Rdsw=250
+Tref=27.0                version=3.1
+Xj=6.0000000E-08         Nch=5.9500000E+17
+lln=1.0000000            lwn=1.0000000          wln=0.00
+wwn=0.00                 ll=0.00
+lw=0.00                  lwl=0.00               wint=0.00
+wl=0.00                  ww=0.00                wwl=0.00
+Mobmod=1                 binunit=2
+Dwg=0.00                 Dwb=0.00
+K1=0.5613000             K2=1.0000000E-02
+K3=0.00                  Dvt0=8.0000000         Dvt1=0.7500000
+Dvt2=8.0000000E-03       Dvt0w=0.00             Dvt1w=0.00
+Dvt2w=0.00               Nlx=1.6500000E-07      W0=0.00
+K3b=0.00                 Ngate=5.0000000E+20
+Vsat=1.3800000E+05       Ua=-7.0000000E-10      Ub=3.5000000E-18
+Uc=-5.2500000E-11        Prwb=0.00
+Prwg=0.00                Wr=1.0000000           U0=3.5000000E-02
+A0=1.1000000             Keta=4.0000000E-02     A1=0.00
+A2=1.0000000             Ags=-1.0000000E-02     B0=0.00
+B1=0.00
+Voff=-0.12350000         NFactor=0.9000000      Cit=0.00
+Cdsc=0.00                Cdscb=0.00             Cdscd=0.00
+Eta0=0.2200000           Etab=0.00              Dsub=0.8000000
+Pclm=5.0000000E-02       Pdiblc1=1.2000000E-02  Pdiblc2=7.50E-03
+Pdiblcb=-1.3500000E-02   Drout=1.7999999E-02    Pscbe1=8.66E+08
+Pscbe2=1.0000000E-20     Pvag=-0.2800000        Delta=1.00E-02
+Alpha0=0.00              Beta0=30.0000000
+kt1=-0.3700000           kt2=-4.0000000E-02     At=5.5000000E+04
+Ute=-1.4800000           Ua1=9.5829000E-10      Ub1=-3.3473E-19
+Uc1=0.00                 Kt11=4.0000000E-09     Prt=0.00
+Cj=0.00365               Mj=0.54                Pb=0.982
+Cjsw=7.9E-10             Mjsw=0.31              Php=0.841
+JS=1.50E-08              JSW=2.50E-13
+N=1.0                    Xti=3.0                Cgdo=2.786E-10
+Cgso=2.786E-10           Cgbo=0.0E+00           Capmod= 2
+NQSMOD=0                 Elm=5                  Xpart=1
+Cgsl=1.6E-10             Cgdl=1.6E-10           Ckappa=2.886
+Cf=1.069e-10             Clc=0.0000001          Cle=0.6
+Dlc=4E-08                Dwc=0                  Vfbcv=-1
```

```
* Predictive Technology Model Beta Version
* 180nm PMOS SPICE Parametersv (normal one)
.model PMOS-BSIM PMOS
+Level=49
+Lint=3.e-08              Tox=4.2e-09
+Vth0=-0.42               Rdsw=450
+Tref=27.0                version=3.1
+Xj=7.0000000E-08         Nch=5.9200000E+17
+lln=1.0000000            lwn=1.0000000          wln=0.00
+wwn=0.00                 ll=0.00
+lw=0.00                  lwl=0.00               wint=0.00
+wl=0.00                  ww=0.00                wwl=0.00
+Mobmod= 1                binunit=2
+Dwg=0.00                 Dwb=0.00
+K1=0.5560000             K2=0.00
+K3=0.00                  Dvt0=11.2000000        Dvt1=0.7200000
+Dvt2=-1.0000000E-02       Dvt0w=0.00             Dvt1w=0.00
+Dvt2w=0.00               Nlx=9.5000000E-08      W0=0.00
+K3b=0.00                 Ngate=5.0000000E+20
+Vsat=1.0500000E+05       Ua=-1.2000000E-10      Ub=1.0000000E-18
+Uc=-2.9999999E-11        Prwb=0.00
+Prwg=0.00                Wr=1.0000000           U0=8.0000000E-03
+A0=2.1199999             Keta=2.9999999E-02     A1=0.00
+A2=0.4000000             Ags=-0.1000000         B0=0.00
+B1=0.00
+Voff=-6.40000000E-02      NFactor=1.4000000      Cit=0.00
+Cdsc=0.00                Cdscb=0.00             Cdscd=0.00
+Eta0=8.5000000           Etab=0.00              Dsub=2.8000000
+Pclm=2.0000000           Pdiblc1=0.1200000      Pdiblc2=8.00E-05
+Pdiblcb=0.1450000        Drout=5.0000000E-02    Pscbe1=1.00E-20
+Pscbe2=1.0000000E-20     Pvag=-6.0000000E-02    Delta=1.00E-02
+Alpha0=0.00              Beta0=30.0000000
+kt1=-0.3700000           kt2=-4.0000000E-02     At=5.5000000E+04
+Ute=-1.4800000           Ua1=9.5829000E-10      Ub1=-3.3473E-19
+Uc1=0.00                 Kt11=4.0000000E-09     Prt=0.00
+Cj=0.00138               Mj=1.05                Pb=1.24
+Cjsw=1.44E-09            Mjsw=0.43              Php=0.841
+JS=1.50E-08              JSW=2.50E-13
+N=1.0                    Xti=3.0                Cgdo=2.786E-10
+Cgso=2.786E-10           Cgbo=0.0E+00           Capmod=2
+NQSMOD=0                 Elm=5                  Xpart=1
+Cgsl=1.6E-10             Cgdl=1.6E-10           Ckappa=2.886
+Cf=1.058e-10             Clc=0.0000001          Cle=0.6
+Dlc=3E-08                Dwc=0                  Vfbcv=-1
```

Figure 3.44: Library file 'BSIM3_018.lib' with BSIM3 models for a generic 0.18 µm CMOS process, adapted from Predictive Technology Model Website (2011).

References

Bruun, E. 2022, *CMOS Analog IC Design: Fundamentals*, Third Edition, bookboon.
Available from: http://bookboon.com/en/cmos-analog-ic-design-fundamentals-ebook

Predictive Technology Model Website 2011. Retrieved from http://ptm.asu.edu/