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Analysis and Evaluation of 99% Efficient Step-up/down Converter based on Partial Power Processing

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***Abstract*—A step-up/and down converter based on partial power processing is proposed in this paper. With the same state equations, the step-up and step-down modes have the same small signal modelling. Therefore, a unified control strategy can be designed for both operating modes, achieving the auto-switching between two operating modes without requiring any additional control. The effect of the transformer's turn ratio on the current and voltage stresses is then analysed. The component stresses are reduced due to the decoupling of transformer. Moreover, the component stress factor method is implemented to evaluate the proposed step-up/down partial power converter. Compared with conventional step-up or step-down partial power converters, the proposed converter has the least component stress factor for a high voltage electrolysis system. In order to validate the proposed topology and modulation strategy, a 400 V prototype is implemented and experimentally evaluated. Measurement results confirm the high efficiency in the overall voltage range, and the maximum efficiency exceeds 99.5%.**

***Index Terms*—Partial power converter, step-up/down voltage regulation, small signal model, component stress factor, high efficiency.**

I. Introduction

RECENTLY, partial power processing (PPP) technology has presented significant advantages in power converter downsizing and efficiency improvement [1], [2]. Different from conventional full power converters (FPCs), a small portion of the power being processed by the partial power converter (PPC). In other word, the most considerable amount of energy flows directly from the source to the load without being processed, resulting in the reduced power rating of power electronic devices and systems [3]–[6]. Therefore, PPC has been an attractive solution in different applications, such as solar photovoltaic systems [7]–[14], energy storage systems (ESSs) [15], [16] and electric vehicle (EV) fast charging stations [17]–[19].

The PPC circuits contains the subcategories of series-connected PPC (S-PPC) and parallel-connected PPC (P-PPC). The P-PPCs are usually employed in PV module strings, also widely called as differential power processing, which achieve maximum power point tracking (MPPT) at fractional currents regulation [14].

S-PPC was first proposed for photovoltaic applications in the spacecraft applications [20]. S-PPCs achieve partial power processing by only regulating the difference between input and load voltage, namely one terminal of the S-PPC is connected in parallel with power source or load and another terminal is connected in series with the power source as well as the load. Consequently, the typical basic circuit connection architectures of S-PPCs based on unipolar dc-dc converter can be derived, as shown in Fig. 1, where consists of two main categories: step-up PPC (SU PPC) and step-down (SD PPC). The architectures shown in Fig. 1a and Fig. 1b are named SU-I and SU-II type PPC respectively, as the load voltage is to the sum of V_{in} plus V_c. In contrast, the load voltage in Fig. 1c and Fig. 1d is equal to the difference between V_{in} and V_c, resulting in a step-down regulation. The processed power by the converter in the typical PPCs are given in (1).

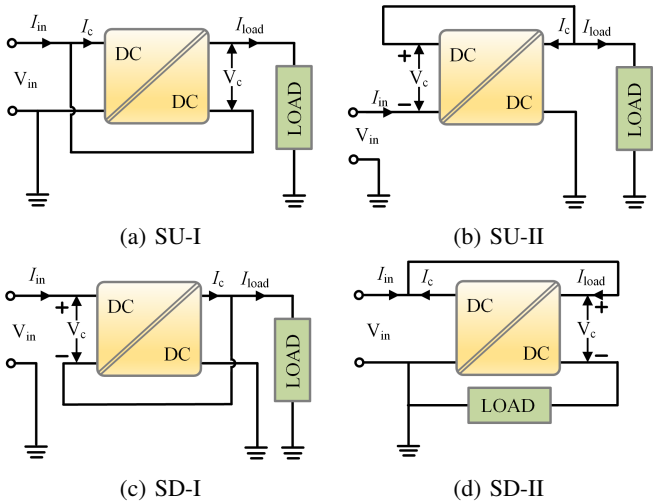


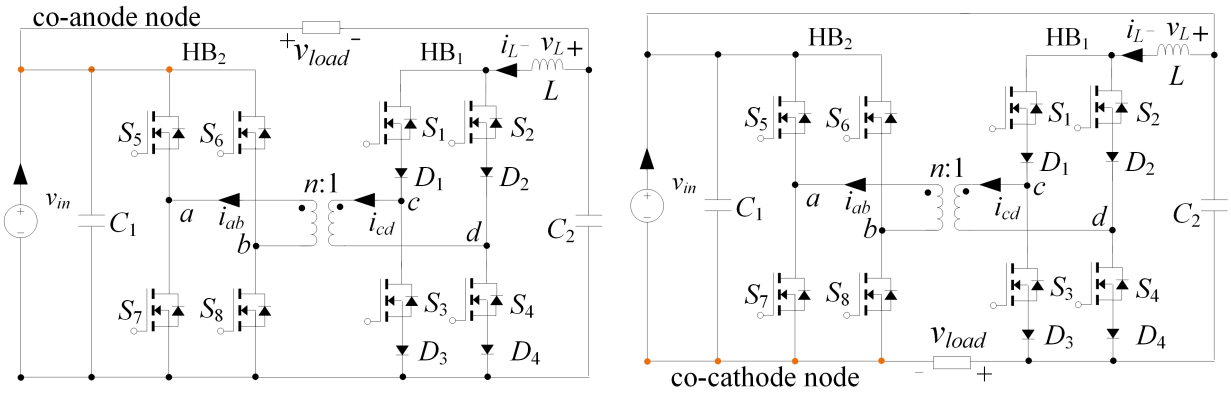
Fig. 1: Basic S-PPC architectures.

$$\begin{aligned} P_{c,SU-I} &= P_{c,SD-I} = |V_{in} - V_{load}| \cdot I_{load} \\ P_{c,SU-II} &= P_{c,SD-II} = |V_{in} - V_{load}| \cdot I_{in} \end{aligned} \tag{1}$$

It can be observed that $P_{c,SU-II}$ is larger than $V_{in} \cdot I_{in}$ when V_{load} is larger than $2V_{in}$, and $P_{c,SD-I}$ is larger than $V_{load} \cdot I_{load}$ when V_{load} is smaller than $0.5V_{in}$, namely SU-II and SD-I PPCs have the limited load voltage range of $V_{in} \sim V_{in}$ and $0.5V_{in} \sim V_{in}$ respectively.

Since I_{load} is smaller than I_{in} in SU PPCs and larger than I_{in} in SD PPCs, the processed power of SU-I and SD-II PPCs are smaller than that of SU-II and SD-I type, which consistent

(The corresponding author: Zhe Zhang)



(a) the co-anode configuration

(b) the co-cathode configuration

Fig. 2: Configurations of the proposed SUD PPC.

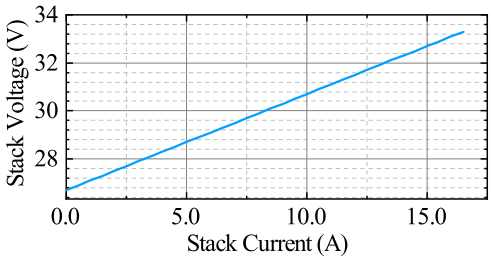


Fig. 3: SOEC stack voltage as a function of the current.

with the results obtained in [21] by Continuous Power Models (CPMs) and VA interpretation.

The partial processed power only evaluates the PPCs at architecture level. Therefore, the more accurate and comprehensive methods are necessary to the analysis of specific PPCs. To demonstrate the concept of PPP, the nonactive power was evaluated on a partial active power buck-boost converter in [22]. The comparative evaluation of PPCs for PV panel-integrated DCDC converter has been presented in [23] by using the component load factors (CLF) method. [24] presented a comparative analysis of the Isolated Full Bridge Boost (IFBB) topology and Active Bridge (DAB) topology for the SD-PPC application based on the method of component stress factor (CSF), and the results show that IFBB topology has the lower CSF. Moreover, an approach to extract state-space averaged equations and small-signal model (SSM) of PPC from the dynamic equations of the FPC is presented in [25].

On the other hand, SD-I and SD-II PPCs can be obtained by changing the polarity of V_c in SU-I and SU-II PPCs respectively. Consequently, the Step-up/down PPC configurations can be derived by replacing the unipolar converter with the bidirectional bipolar converter in SU-I and SU-II PPCs. The SUD PPC architecture based on SU-I PPC is preferred due to the lower processed power at SU mode [26], and is therefore analysed in detail in this paper. Compared with the SD and SU PPCs, SUD PPCs have more complicated modulation and control strategy due to the two operating modes. Therefore, the simply control strategy and nature mode switching modulation strategy are crucial to further enhance SUD PPC application prospects.

This paper proposes a high efficiency SUD PPC topology for a high voltage solid oxide electrolysis cells (SOEC) system. High temperature steam electrolysis based on SOEC is a promising way to produce hydrogen with high efficiency. Fig.3 shows the V-I profile of a typical SOEC stack, which can be seen as a voltage source connected with a resistor in series. Due to the low operating voltage of the individual stack, approximately 26.7 to 33.5 V, connecting multiple stacks in series to increase the voltage level is a trend to increase the power rating of SOEC systems. When the dc bus voltage is 400 V, the peak power of a 13-stack series SOEC system based on the given stack is 7.4 kW with the voltage range of 347.1 V to 435.5 V. Therefore, the efficient SUD PPC with the output voltage range of 350 to 435.5 V is designed for the high voltage SOEC system in this paper.

The rest of this paper is organized as follows. The operating principles of the proposed topology in both operating modes are expressed in details in Section II. According to the operating principles analysis, the small-signal model (SSM) is built and the two operating modes have the same SSM, resulting in the unified controller. The current and voltage stresses are analyzed to present the effects of the transformer's turn ratio in Section III. Then the approach of CSF is implemented to comparative evaluate the proposed topology and the conventional PPCs, and the results demonstrate the improvements resulting from the transformer. Section IV presents the experimental results of a 400 V prototype for the SOEC system to verify the feasibility and practicality of the topology and modulation strategy. Finally, Section V concludes this paper.

II. Operation Principle and Small Signal Analysis

A. System design and power analysis

Fig. 2 shows the two iso-structures of the proposed SUD PPC, which consists of one low-voltage H-bridge with D_{1-4} (HB_1), the high-voltage H-bridge (HB_2), the inductor L and

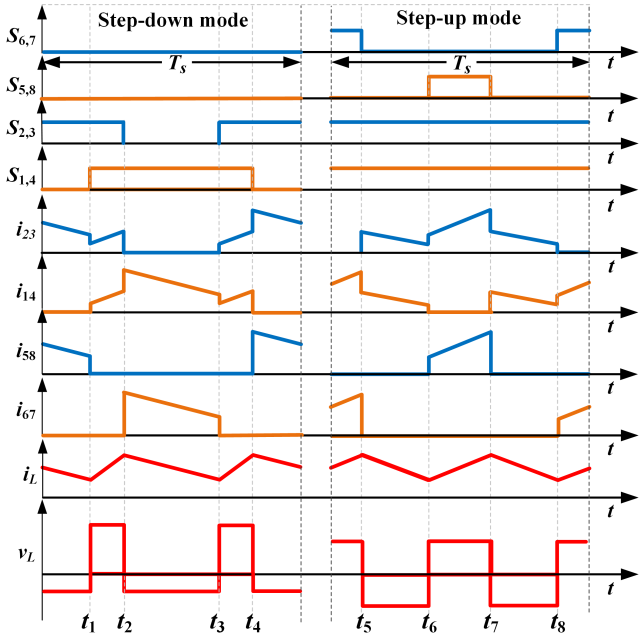


Fig. 4: Modulation signals and theoretical waveforms of the proposed topology.

a high-frequency transformer (HFT) with n turn ratio. The two iso-structures can be seen as the identical converter, only with different load positions, as they have the same topological characteristics, i.e. the same operation processes and voltage gain. In both H-bridge converters, the diagonal power switches have the same control signals. The control signals of $S_{1,4}$ and $S_{5,8}$ are 180 degrees lagged behind those of $S_{2,3}$ and $S_{6,7}$, respectively.

Defining d_s and d_q are the duty cycle for the S_{1-4} and S_{5-8}, respectively, the modulation signals are generated by comparing d_q and d_s with the carrier waves. Fig. 4 shows the Modulation signals and theoretical waveforms of the proposed converter in both SU and SD operating modes, where T_s is one completed switching period; $S_{1,4}$, $S_{2,3}$, $S_{5,8}$ and $S_{6,7}$ are modulation signals of the corresponding switches, respectively; i_{14}, i_{23}, i_{58} and i_{67} are currents pass though the corresponding switches, respectively; i_L and v_L are the current and voltage of the inductor, respectively. The operating principle of proposed topology is analyzed with the following assumptions.

1) Magnetizing inductance is assumed very large.
2) All the components are ideal and lossless.
3) Leakage inductance of the transformer is neglected.
4) The transient process of switching is very fast and neglected.

B. Step-down operating mode analysis

In the SD mode, S_{5-8} are always off-state, thereby HB_2 operates as the rectifier, which requires d_q to be always equal to 0. Fig. 5 shows the corresponding equivalent circuits during the first two intervals in Fig. 4 (t_1-t_2 and t_2-t_3). The operating process in each interval of the step-down operating mode is analyzed as follows.

1) State_SD1: t_1-t_2

In this subinterval, S_{1-4} are all on-state, the current across the inductor (i_L) uniform flows through both arms of HB_1, namely $i_{14} = i_{23} = 0.5 \times i_L$, as shown in Fig. 5 (a). Power is transferred from source directly to load. Since no power flows through the transformer and HB_2, the power processed by the converter can be seen as zero in this period. The inductor charges and i_L increases. The inductor voltage v_L is equal to the difference between input voltage v_{in} and load voltage v_{load}. The duration of this process is (d_s-0.5)×T_s. State equations for this subinterval are given by (2).

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = v_{in} - v_{load} \\ c_2\dfrac{\mathrm{d}v_{c2}}{\mathrm{d}t} = \dfrac{v_{load}}{R} - i_L \end{cases} \tag{2}$$

2) State_SD2: t_2-t_3

At t_2, S_2 and S_3 are turned off, i_{14} is increased from half of i_L to i_L, while i_{23} is decreased from half of i_L to zero. Therefore, the current in HB_2 flows through the anti-parallel diode of S_5 and S_8, as shown in Fig. 5 (b). v_{ab} and v_{cd} are v_{in} and v_{in}/n, respectively. The inductor discharges in this period, and i_L decreases. The duration of this process is (1-d_s)×T_s. State equations for this subinterval are given by (3).

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = \dfrac{(n-1)\ v_{in}}{n} - v_{load} \\ c_2\dfrac{\mathrm{d}v_{c2}}{\mathrm{d}t} = \dfrac{v_{load}}{R} - i_L \end{cases} \tag{3}$$

At t_3, S_2 and S_3 are turned on again. The operating state of this subinterval is the same as $State\_SD1$. At t_4, S_1 and S_4 are switched off, the current through i_{23} is increased from half of i_L to i_L while the current through the i_{14} is decreased from half of i_L to zero. Therefore, the 4th steady-steady operating process is symmetrical to the $State\_SD2$.

Consequently, the four operating states of the step-down mode are symmetrical. According to the analysis, the converter works as the isolated boost converter in SD mode. The following equation calculates the output voltage by applying volt-second balance to the inductor over one switching period where V_{in} and V_{load} are the DC components of v_{in} and v_{load}, respectively.

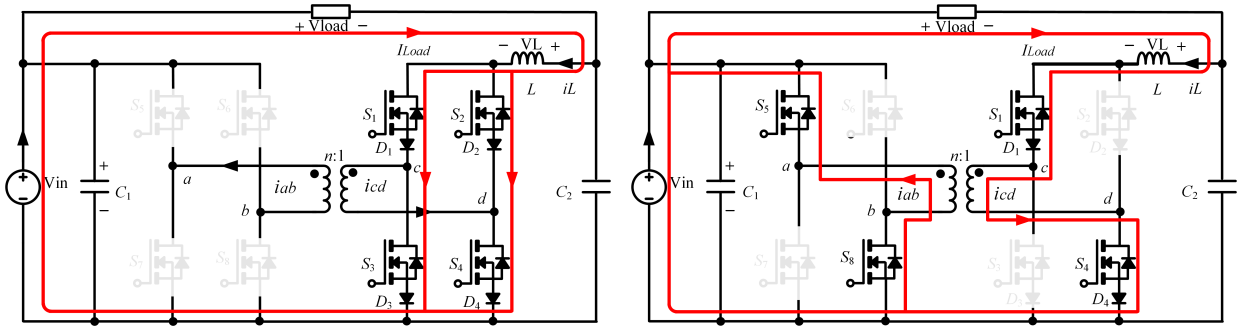
$$V_{load} = \frac{(n + 2d_s - 2)V_{in}}{n},\ 0.5 \le d_s \le 1 \tag{4}$$

C. Step-up operating mode analysis

To achieve the SU voltage regulation, D_{1-4} works as the rectifier to provide the negative voltage and S_{1-4} are always on-state, i.e. d_s is always equal to 1. The operating process in each interval of the step-up operating mode is analyzed as follows.

1) State_SU1: t_5-t_6

In this subinterval, the state of the switches is identical to that of $State\_SD2$. However, the inductor discharges and i_L decreases in this period. The duration of this process is $(0.5 - d_q)\times T_s$. The equations of this subinterval are the same as (2).



(a) Equivalent circuit of $State\_SD1$ (b) Equivalent circuit of $State\_SD2$

Fig. 5: Equivalent circuits of the former two operating states in SD mode.

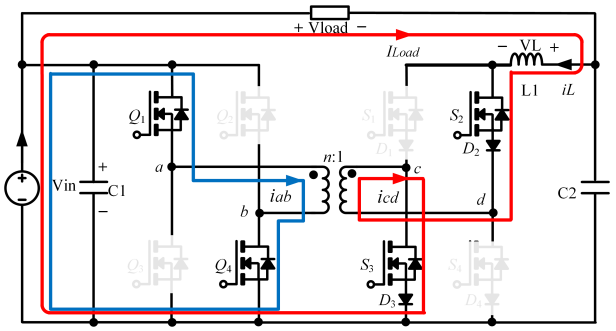


Fig. 6: Equivalent circuit during the interval of t_6-t_7 in Fig. 4.

2) $State\_SU2$: t_6-t_7

At t_6, S_5 and S_8 are switched on, v_{ab} and v_{cd} are equal to v_{in} and v_{in}/n, respectively. The positive v_{cd} blocks D_1 and D_4, thereby i_L only flows through $S_{2,3}$ and $D_{2,3}$ in HB_1. The duration of this process is $(d_q)\times T_s$. Equations of this subinterval are given by (5).

$$\begin{cases} L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = \dfrac{(n+1)\ v_{in}}{n} - v_{load} \\ C_2\dfrac{\mathrm{d}v_{c2}}{\mathrm{d}t} = \dfrac{v_{load}}{R} - i_L \end{cases} \tag{5}$$

At t_7, S_5 and S_8 are turned off, the operating state in this subinterval is identical as $State\_SU1$. At t_8, S_6 and S_7 are switched on, and i_L flows through $S_{1,3}$ and $D_{1,3}$ in HB_1 due to negative v_{cd}, i.e.$-v_{in}/n$. Therefore, the steady-steady operating process in this subinterval is symmetrical to that of $State\_SU2$. In SU mode, the proposed converter works as the inverting isolated buck converter with the input voltage of v_{in} and output voltage of v_{c2}. Applying volt-seconds principle again, the output voltage in step-up mode is obtained by (6).

$$V_{load} = \frac{(n+2d_q)V_{in}}{n},\ 0 \le d_q < 0.5 \tag{6}$$

D. The unified modulation strategy

According to (4) and (6), V_{load} at d_s=1 is equal to that at d_q=0, which is equal to V_{in}. Replacing d_s and d_q with the unified modulation ratio u, the one unified expression of V_{load} for both operating are derived by (7).

$$V_{load} = \frac{(n+2u-2)V_{in}}{n},\ 0.5 \le u < 1.5 \tag{7}$$

The expressions between u and d_s as well as d_q are given by (8) and (9), respectively. When u is smaller than 1 and larger than 0.5, d_q is always 0 and d_s = u, namely S_{5-8} are all switched off, the converter operates in SD mode. Conversely, when u is smaller than 1.5 and larger than 1, d_s is always 1 and d_s = u, namely S_{1-4} are all switched on, the converter operates in SU mode. The transition between the two modes occurs at $u = 1$.

$$d_s \begin{cases} = u & 0.5 \le u < 1 \\ = 1 & 1 \le u \le 1.5 \end{cases} \tag{8}$$

$$d_q \begin{cases} = 0 & 0.5 \le u < 1 \\ = u-1 & 1 \le u \le 1.5 \end{cases} \tag{9}$$

According to (7), Fig. 7 plots voltage gain, k, versus u with different n. The unified modulation strategy enables automatic switching between two operation modes without requiring any extra information, such as voltage direction and current direction, etc. Rearranging (7) results in the following equation.

$$u = \frac{nk-n}{2} + 1 \tag{10}$$

It can also be observed that n and k are inversely proportional for the specific duty ratio range. That is, the range of n decreases as voltage gain range increases.

For a given range of k and u, n should meet the following conditions.

$$n \le \begin{cases} \dfrac{2(u_{min}-1)}{k_{min}-1} & u_{min} < 1 \\ \dfrac{2(u_{max}-1)}{k_{max}-1} & u_{max} > 1 \end{cases} \tag{11}$$

To avoid the short circuit in HB_2 and open circuit in HB_1, the maximum and minimum limits of u are set to 1.4 and 0.6 respectively, i.e. $0.6 \le d_s \le 1$ and $0 \le d_q \le 0.4$. As a result, the maximum n of the SUD PPC in this system is 5.3, rounded down to 5.

Since all components are ideal and lossless, the processed power of the converter (P_c) can be obtained by (12).

$$\begin{aligned} P_c &= |V_{in} - V_{load}| \cdot I_{load} = |1-k| V_{in} \cdot I_{load} \\ &= \frac{|1-k|}{k} \cdot P_s \end{aligned} \tag{12}$$

where $P_s = V_{in} \cdot I_{in} = V_{load} \cdot I_{load}$.

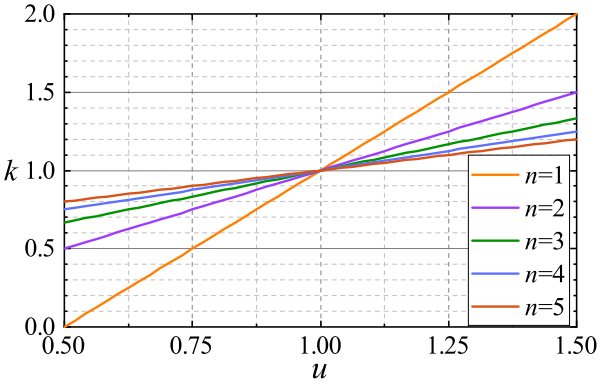


Fig. 7: gain versus u with different n.

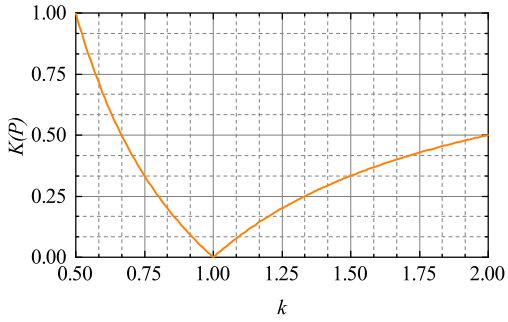


Fig. 8: Processed power versus k.

Fig. 8 plots the processed power ratio ($K(P)$) of the converter versus voltage gain. It can be seen that the proposed topology achieves partial power processing when voltage gain is larger than 0.5. At k = 1, $K(P)$ is equal to 0, meaning that no power is processed by the converter.

E. Small Signal Modeling

Based on the state equations for each interval of steady-state operation described above, both operating modes have the identical averaged state equations with the proposed modulation strategy, which are expressed by (13).

$$\begin{cases} L\dfrac{\mathrm{d}\langle i_L\rangle}{\mathrm{d}t} = \dfrac{(n+2u-2)}{n}\cdot\langle v_{in}\rangle - \langle v_{load}\rangle \\ C_2\dfrac{\mathrm{d}\langle v_{c2}\rangle}{\mathrm{d}t} = \dfrac{\langle v_{load}\rangle}{R} - \langle i_L\rangle \end{cases} \tag{13}$$

Since $v_{c2} = v_{in} - v_{load}$, (13) can be arranged in Laplace domain as

$$\begin{cases} Ls\langle i_L\rangle = \dfrac{(n+2u-2)}{n}\cdot\langle v_{in}\rangle - \langle v_{load}\rangle \\ (C_2 s + \dfrac{1}{R})\langle v_{load}\rangle = C_2 s\langle v_{in}\rangle + \langle i_L\rangle. \end{cases} \tag{14}$$

Introducing perturbation around the steady state value for the state variables and other quantities such that$\langle i_L\rangle = I_L + \widehat{i}_L, \langle v_{in}\rangle = V_{in} + \widehat{v}_{in}, \langle v_{load}\rangle = V_{load} + \widehat{v}_{load}, u = U + \widehat{u}$, then small signal AC model in matrix form is derived

$$\begin{bmatrix} \widehat{v}_{load} \\ \widehat{i}_L \end{bmatrix} = A \begin{bmatrix} A_{12} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} \widehat{v}_{in} \\ \widehat{u} \end{bmatrix} \tag{15}$$

TABLE I: Simulation System Specification

Symbol	Parameter	Value
V_{in}	Input voltage	400 V
L	Output inductor	15 μH
C_2	Output filter capacitor	10 μF
n	turn ratio	5:1
R	Load resistance	70 Ω
f_s	Switching frequency	100 kHz

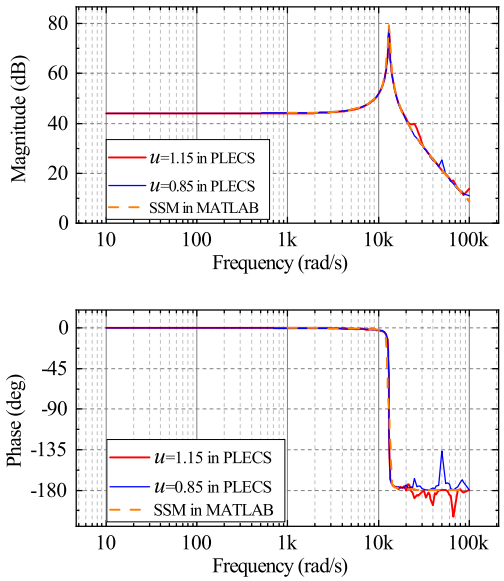


Fig. 9: Frequency response of the control-to-output voltage transfer function.

where

$$\begin{aligned} A &= \frac{1}{nLC_2Rs^2 + nLs + nR} \\ A_{11} &= (n + 2u - 2 + s^2LC_2)R \\ A_{12} &= 2RV_{in} \\ A_{21} &= \frac{A_{11}(1 + sC_2R)}{R} - AsC_2 \\ A_{22} &= 2(1 + sC_2R)V_{in}. \end{aligned} \tag{16}$$

Based on (16), the control-to-output transfer function can be obtained by setting $\widehat{v}_{in}$ = 0, which results in the following equation:

$$G_{vd} = \left.\frac{\widehat{v}_{load}}{\widehat{u}}\right|_{\widehat{v}_{in}=0} = \frac{2RV_{in}}{nLC_2Rs^2 + nLs + nR} \tag{17}$$

In order to verify the proposed SSM, a simulation has been built in PLECS and the system specifications are listed in Table I. The ac sweep analysis of the control-to-output transfer function has been analyzed in the cases of $u = 0.8$ (SD mode) and $u = 1.15$ (SU mode). The frequency response curves are plotted in Fig. 9, where the red and blue curves present the

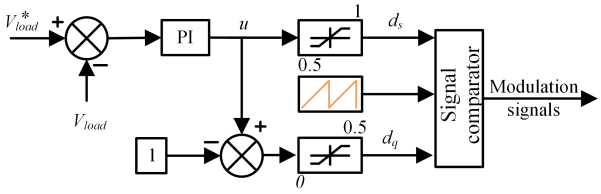


Fig. 10: Block diagram of the unified controller for two operating modes.

TABLE II: Main Specifications of the HV SOEC System

V_{in}	$V_{load,max}$	$P_{s,max}$	$P_{c,max}$	$I_{load,max}$
400 V	435.5 V	7.3 kW	0.6 kW	17 A

TABLE III: Component Voltage Stress with different n

n	V_{c1}	V_{S1-4}, V_{D1-4}	V_{S5-8}	V_{c2}
1	400 V	400 V	400 V	50 V
2	400 V	200 V	400 V	50 V
3	400 V	167 V	400 V	50 V
4	400 V	100 V	400 V	50 V
5	400 V	80 V	400 V	50 V

frequency response of SU mode and SD mode, respectively. Fig. 9 also plots the frequency response of control-to-output transfer function based on the SSM, indicated by orange dash. It can be seen that the PLECS simulation has the almost identical frequency response in SD mode (blue line) and SU mode (red line), which is consistent with the theoretical analysis (orange dash).

Consequently, a unified controller can be designed for the both operating modes without any other additional information, as shown in Fig. 10. When u is larger than 0.5 and smaller than 1, d_q equals to u and d_s still keeps 0 due to the lower limiter. When u is larger than 1, d_q equals to 1 due to the upper limiter and $d_s = u - 1$.

III. Evaluation of the Proposed SUD PPC

Table. II lists the main specifications of the high voltage SOEC system based on the proposed SUD PPC. According to (12), the peak value of P_c is only 0.6 kW, a reduction of more than 90% compared to total power. In addition to the reduced processed power, the PPC also has significantly advantage of the decoupling voltage and current stresses due to the transformer. To further assess the proposed SUD PPC topology, especially the effects of the transformer, the component stress analysis is carried out in this section. Then, the method of component stress factor is implemented to evaluate the proposed SUD PPC with other conventional unipolar PPCs.

TABLE IV: Peak Component Current with different n

n	I_H	I_{LS}	I_L	I_{C1}	I_{C2}
1	3.64 A	9.01 A	17.28 A	4.91 A	4.2 A
2	2.56 A	9.35 A	17.23 A	3.29 A	3.6 A
3	2.09 A	9.67 A	17.18 A	2.53 A	3.0 A
4	1.8 A	9.98 A	17.14 A	2.05 A	2.4 A
5	1.61 A	10.05 A	17.1 A	1.7 A	1.92 A

A. Component Voltage Stress

Neglecting the voltage ripple, the blocking voltages of the switches in HB_2 (V_{S5-8}) and input capacitor (V_{c1}) are not affected by transformer's turn ratio, which always equal to input voltage V_{in}.

In the low-voltage side, thanks to the partial power architecture, the voltage of output capacitor (V_{c2}) is equal to $|V_{in} - V_{load}|$ instead of V_{load} in conventional FPCs. Moreover, the blocking voltage of S_{1-4} and D_{1-4} is strongly influenced by the transformer's turn ratio, which equals to V_{in}/n.

Table.III shows the component voltage stress of the proposed system with different n. It is concluded that the proposed partial power topology significantly reduces the blocking voltage of the output capacitor. The blocking voltage of the semiconductors in low-voltage side can be reduced by increasing n. For the given system, the blocking voltage of the low-voltage semiconductor is smaller than 100 V when $n > 4$. Therefore, the 200 V semiconductors can be used in this 400 V SOEC system, leads to the further efficiency increasing and costs reducing.

B. Component Current Stress

In the proposed topology, the RMS value of load current (I_{load}) is expressed by (18).

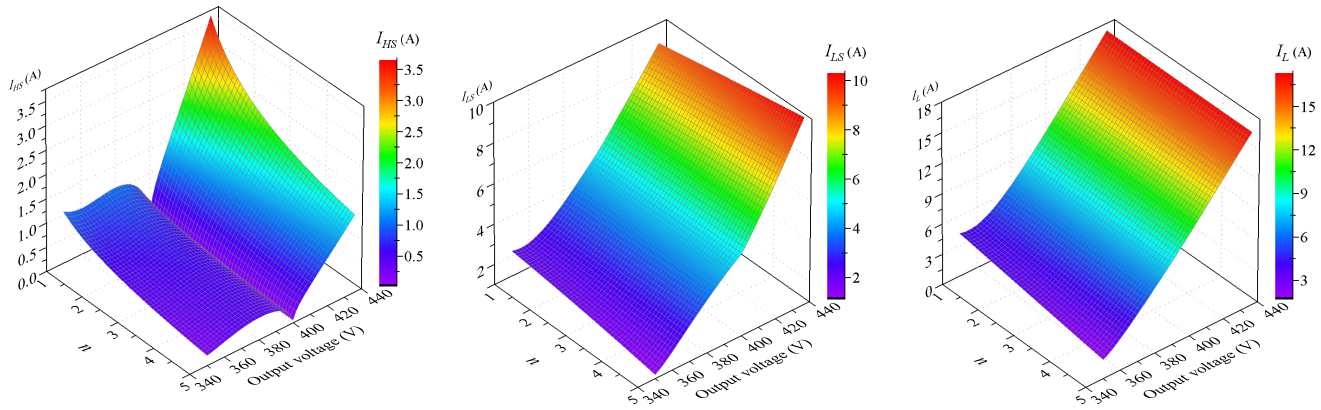
$$\begin{aligned} I_{load} &= I_L = \sqrt{I_{ave}^2 + \frac{\Delta I_L^2}{12}} \\ I_{ave} &= \frac{(n + 2u - 2)V_{in} - 347.1 \cdot n}{nR} \\ \Delta I_L &= \frac{(V_{in} - V_{load}) \cdot (0.5 - |1 - u|) \cdot T_s}{L} \end{aligned} \tag{18}$$

The RMS value of the current through the semiconductors on the low and high voltage side is given by (19) and (20) respectively.

$$I_{LS} = \sqrt{\frac{|1 - u| + 0.5}{2}} \cdot I_L \tag{19}$$

$$I_{HS} = \frac{\sqrt{|1 - u|}}{n} \cdot I_L \tag{20}$$

The current through the high and low voltage sides of the transformer is equal to $\sqrt{2}I_{HS}$ and $\sqrt{2}I_{HS}/n$, respectively.



(a) RMS value of I_{HS} versus n and output voltage.

(b) I_{LS} versus n and output voltage.

(c) I_L versus n and output voltage.

(d) I_{C1} versus n and output voltage.

(e) I_{C2} versus n and output voltage.

Fig. 11: RMS value of component current versus turn ratio and output voltage.

The RMS values of the current through input capacitor and output capacitor is given by (21) and (22), respectively.

$$I_{C1} = \begin{cases} \dfrac{\sqrt{-4u^2+6u-2}\cdot I_L}{n} & 0.5 \le u < 1 \\ \dfrac{\sqrt{-4u^2+10u-6}\cdot I_L}{n} & 1 \le u \le 1.5 \end{cases} \tag{21}$$

$$I_{C2} = \begin{cases} \dfrac{(2-2u)\cdot V_{in}\cdot(u-0.5)}{2\sqrt{3}Lf} & 0.5 \le u < 1 \\ \dfrac{(3-2u)\cdot V_{in}\cdot(u-1)}{2\sqrt{3}Lf} & 1 \le u \le 1.5 \end{cases} \tag{22}$$

Fig. 11 shows the RMS value of the component current as the function of the turn ratio and output voltage, respectively. The peak value of the component current with different n are listed at Table.IV. It can be observed that increasing n reduces the I_{HS}, I_{C1} and I_{C2} greatly. The minimum value of these currents occurs at $V_{load} = V_{in}$ and is zero. And the change in n results in the negligible changes in the peak value of I_{LS} and I_L. As a result the higher n has the potential to presents better performances due to the greatly reduced voltage stress of S_{1-4} and D_{1-4} and current stress of S_{5-8} and C_1.

C. Comparative Analysis based on CSF

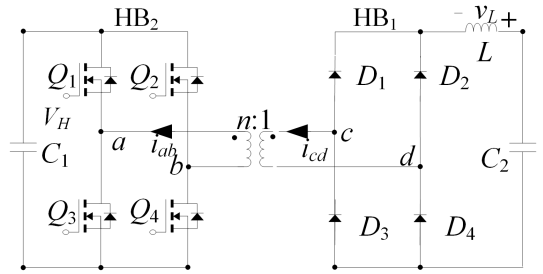
In order to give a quantitative measure for comparison with conventional unipolar PPCs, the CSF of the typical PPCs based on the isolated buck or boost converter shown in Fig.12, as well as the proposed SUD PPC are calculated. To simplify the calculations, the CSF method adopts the assumptions that the power losses in the converter are ignored and the same type components have the same weight factor [27]. The stress factor is calculated independently for each component: semiconductors (SCSF), capacitors (CCSF), and winding (WCSF), as shown in (23), (24) and (25), respectively,

$$SCSF = \sum_i^j \cdot \frac{V_{max\_i}^2 \cdot {I_{rms\_i}}^2}{{P_s}^2} \tag{23}$$

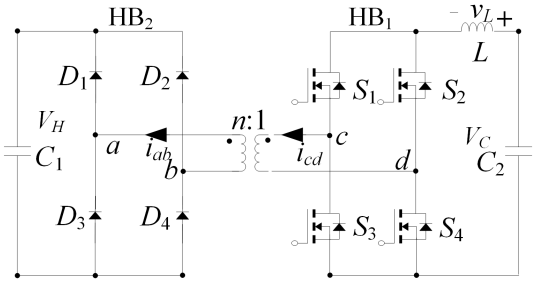
$$CCSF = \sum_i^j \cdot \frac{V_{max\_i}^2 \cdot {I_{rms\_i}}^2}{{P_s}^2} \tag{24}$$

$$WCSF = \sum_i^j \cdot \frac{V_{max\_avg\_i}^2 \cdot {I_{rms\_i}}^2}{{P_s}^2} \tag{25}$$

where $V_{max\_avg\_i} = D_i \cdot |V_i|$; I_{rms_i} and V_{max_i} are the peak RMS current and peak voltage of component i respectively; j is the number of same type components. In the proposed topology and the conventional SU/SD PPCs, j of capacitos and winding are 2 and 3 respectively and j of the semiconductors are 12 and 8, respectively.



(a) Isolated buck converter



(b) Isolated boost converter

Fig. 12: Isolated converter for conventional PPC configuration.

Both the proposed PPC and conventional unipolar PPCs are design for the given SOEC system with the same voltage range of 350 $\sim$ 435.5 V. Therefore, input voltage of the SU and SD PPCs are 350 and 435.5 V, respectively. V_{load} of the typical PPC based systems can be expressed by (26),

$$\begin{aligned} V_{load,SU-I} &= \frac{n+2d_q}{n}\cdot V_{in} \\ V_{load,SU-II} &= \frac{n}{n-2d_q}\cdot V_{in} \\ V_{load,SD-I} &= \frac{n+2d_s-2}{n}\cdot V_{in} \\ V_{load,SD-II} &= \frac{n}{n+2-2d_s}\cdot V_{in} \end{aligned} \tag{26}$$

where d_q and d_s are the duty ratio for SU and SD type PPCs respectively. Based on (26), the range of n of the typical PPCs are derived by (27).

$$\begin{aligned} n_{SU-I} &\le \frac{2d_q\cdot V_{in}}{V_{load,max}-V_{in}} \\ n_{SU-II} &\le \frac{2d_q\cdot V_{load,max}}{V_{load,max}-V_{in}} \\ n_{SD-I} &\le \frac{2(1-d_s)\cdot V_{in}}{V_{in}-V_{load,min}} \\ n_{SD-II} &\le \frac{2(1-d_s)\cdot V_{load,min}}{V_{in}-V_{load,min}} \end{aligned} \tag{27}$$

For SD PPCs V_{in} and $V_{load,max}$ are 350 V and 435.5 V, respectively, while for SU PPCs, V_{in} and $V_{load,min}$ are 435.5 V and 350 V, respectively. With the duty cycle limitation of $d_q \le 0.4$ and $d_s \ge 0.6$, the max turn ratio range of SU-I and SD-II is 2.72 and the max turn ratio of SU-II and SD-I is 3.72, rounded down to 2 and 3, respectively. Table.V shows component voltage stresses of the unipolar PPCs at their maximum n. Since the proposed SUD PPC can be seen as a combination of the SU-I and SD-I PPCs, SU-I and SD-I PPCs have the same expressions of the component current and voltage with the SU and SD modes of the proposed SUD PPC.

TABLE V: Component Voltage Stresses of the SU/SD PPCs

Type	SU-I	SU-II	SD-I	SD-II
V_{in}	350 V	350 V	435.5 V	435.5 V
$V_{S,D1-4}$	175 V	145.17 V	145.17 V	217.75 V
V_{S5-8}	350 V	435.5 V	435.5 V	435.5 V
V_{c1}	350 V	435.5 V	435.5 V	435.5 V
V_{c2}	85.5 V	85.5 V	85.5 V	85.5 V
n	2	3	3	2

In SD-II and SU-II PPCs, I_L equals I_{in}, thereby I_{LS} of the SD-II and SU-II PPCs is given by (28).

$$\begin{aligned} I_{LS,SD-II} &= \sqrt{\frac{1.5-d_s}{2}}\cdot I_L \\ I_{LS,SU-II} &= \sqrt{\frac{0.5-d_q}{2}}\cdot I_L \\ I_{ave} &= \frac{V_{load}-347.1}{R} \\ I_L &= \sqrt{(kI_{ave})^2+\frac{\Delta I_L^2}{12}} \end{aligned} \tag{28}$$

where ΔI_L in SD-II and SU-II PPCs is given by the following equations.

$$\begin{aligned} \Delta I_{L,SD-II} &= \frac{(V_{in}-V_{load})\cdot(d_s-0.5)\cdot T_s}{L} \\ \Delta I_{L,SU-II} &= \frac{(V_{load}-V_{in})\cdot(0.5-d_q)\cdot T_s}{L} \end{aligned} \tag{29}$$

Similarly, I_{HS} in SD-II and SU-II PPCs is given by (30).

$$\begin{aligned} I_{HS,SD-II} &= \frac{\sqrt{1-d_s}\cdot I_L}{n} \\ I_{HS,SU-II} &= \frac{\sqrt{d_q}\cdot I_L}{n} \end{aligned} \tag{30}$$

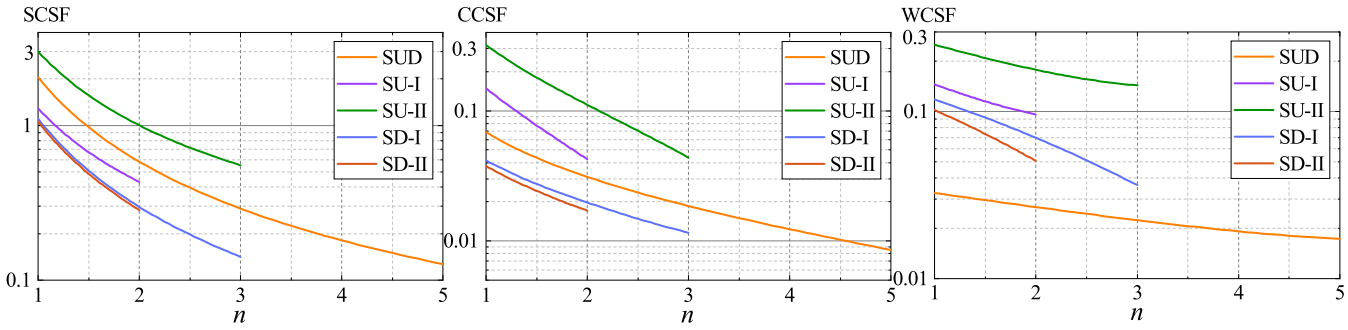
I_{C1} in SD-II and SU-II PPCs are given by (31).

$$\begin{aligned} I_{C1,SD-II} &= \frac{\sqrt{-4d_s^2+6d_s-2}}{n}\cdot I_L \\ I_{C1,SU-II} &= \frac{\sqrt{-4d_q^2+2d_q}}{n}\cdot I_L \end{aligned} \tag{31}$$

I_{C2} in the SD-II and SU-II PPCs is given by (32).

$$I_{C2} = \frac{\Delta I_L}{\sqrt{12}} \tag{32}$$

Applying (23), (24) and (25), the CSF of the typical SD/SU PPCs and the proposed SUD PPC are plotted in Fig. 13. It can be seen that a higher ratio presents the smaller CSF, both for the proposed SUD PPC and conventional SU/SD PPCs. Although the proposed SUD PPC has more low-voltage semiconductors, it has the minimum CSF due to the highest



(a) SCSF versus turn ratio (b) CCSF versus turn ratio (c) WCSF versus turn ratio

Fig. 13: CSF of different PPCs versus turn ratio.

turn ratio. In practice, the higher turn ratio means the lower voltage requirements for low-voltage side semiconductors and lower current requirements for high-voltage side semiconductors, resulting in the advantages in terms of cost, volume as well as efficiency.

IV. Experimental Results

A 400 V prototype with a 20:4 interleaved PCB transformer are shown in Fig. 14. Table.VI shows the specifications of main components. Since the 4-layer interleaved winding structure has a high coupling coefficient, the transformer's leakage inductance L_{leak} is only 3 μH, 0.1 % of L_m, suppressing the voltage oscillation caused by hard switching. Due to the partial power topology, the 100 V capacitor can be employed as the output capacitor, resulting in a smaller volume. Additionally, the blocking voltages of D_{1-4} and S_{1-4} are only 80 V as n = 5. Hence, the 200 V semiconductors, which are not available in other PPCs, are used in this 400 V system, thus reducing the drain-source on-resistance of the MOSFETs and the forward voltage of the diodes. The operating principle and modulation strategy are verified with a constant load. A fixed resistance load in series with a constant voltage (CV) electronic load simulates the electrolysis stacks to measure the efficiency of the SOEC system.

TABLE VI: Experimental System Specifications

Symbol	Parameter	value
C_1	Input capacitor	6.8 μF
C_2	Output capacitor	10 μF
S_{1-4}	Switches in HB_1	IRF200P223
D_{1-4}	Diodes in HB_1	V30200C
S_{5-8}	Switches in HB_2	IMW65R072M1H
f_{sw}	Switching frequency	100 kHz
L	Output inductor	15 μH
L_m	Magnetisation inductance of HFT	3 mH
L_{leak}	Leakage inductance of HFT	3 μH

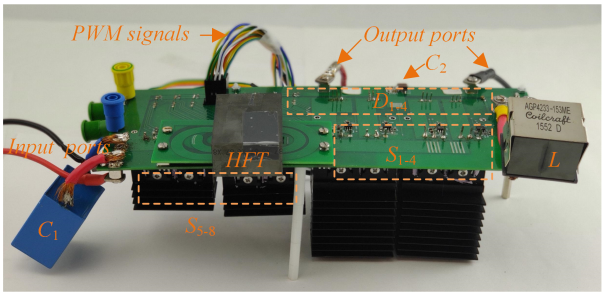


Fig. 14: Experimental prototype of the SUD PPC.

A. Experiments with the constant load

In this case, only a 70 Ω resistor is employed as the load. Fig. 15 and Fig. 16 show the steady-state experimental waveforms of SD and SU modes, respectively. In Fig. 15, V_{load} and P_s are 370 V and 1.9 kW, respectively. The polarities of v_{ab} and i_{ab} are reversed because the converter transfers power from low-voltage side to high-voltage side in this mode.

In Fig. 16, V_{load} and P_S are 426.7 V and 2.6 kW respectively. And the polarities of v_{ab} and i_{ab} are the same, because the converter transfers power from high-voltage side to low-voltage side. It can be seen that the experimental waveforms are identical with the theoretical analysis mentioned in Section.II.

Note that the voltage spike of V_L occurs when $S_{1,4}$ or $S_{2,3}$ are switched on. The combination of D_{1-4} and S_{1-4} can be seen as the unidirectional current switch. When a bottom switch (S_3 or S_4) is turned on, the charged stored in its parasitic capacitance redistributes to the diode above it because the switch itself is current unidirectional. The combined energy stored in the parasitic capacitance of S_{5-8} and of a top switch in HB_1 slowly dissipates until HB_2 changes to a $State\_SD1$. During this transition, v_{cd} is not zero due to the reflected voltage difference between ports a and b, resulting in the voltage spike in V_L. And replacing S_{1-4} and D_{1-4} with bidirectional switches can solve this issue.

Fig. 17 shows the transient-state waveforms of the operation mode switching as V_{load} steps up from 360 to 435 V. Under the proposed modulation strategy, the converter automatically implements the mode change from SD mode to SU mode. There is a gap where the transformer voltage and current is 0 when V_{load} approaches to V_{in}. It's because that the switching-off period of S_{1-4} or switching-on period of S_{5-8} is too short, as u is very close to 1.

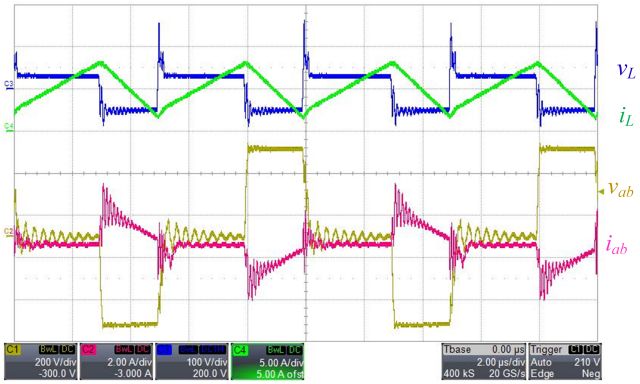


Fig. 15: Steady-state waveforms of SD mode.

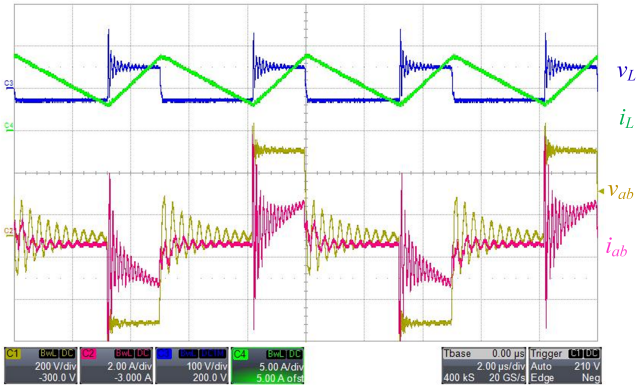


Fig. 16: Steady-state waveforms of SU mode.

Fig. 18 shows the transient-state waveforms of the operation mode switching as the input voltage steps down from 400 to 375 V, while V_{load} is fixed at 390 V. It can be seen that the converter smoothly changes the operating mode from SU mode to SD mode. Therefore, the proposed modulation strategy automatically achieves mode switching for both input and output voltages stepping.

B. Experiments with the constant load in series with CV electronic load

In this case, a 5.3 Ω resistor and a 347.1 V voltage load are connected in series to simulate the given SOEC stacks. Two 1mΩ current shunts are placed into the circuit to measure the input and load current, respectively. The voltages of the current shunt, V_{in} and V_{load} are measured by 34465A Digit Multimeters. Fig. 19 shows the experimental efficiency curve excluding the driving loss. The proposed prototype has the high efficiency in overall regulation range, exceeding 99% from 2 kw to 7 kW, with a peak efficiency of over 99.5% and a minimum efficiency of over 98.5 %. The peak efficiency occurs when u = 1. In this time, the theoretically load voltage should be equal to input voltage. However, in practice, V_{load} is little smaller than V_{in} due to the forward voltage of the diode and other conductive losses.

In SD mode, the conductive and switching losses of S_{1-4}

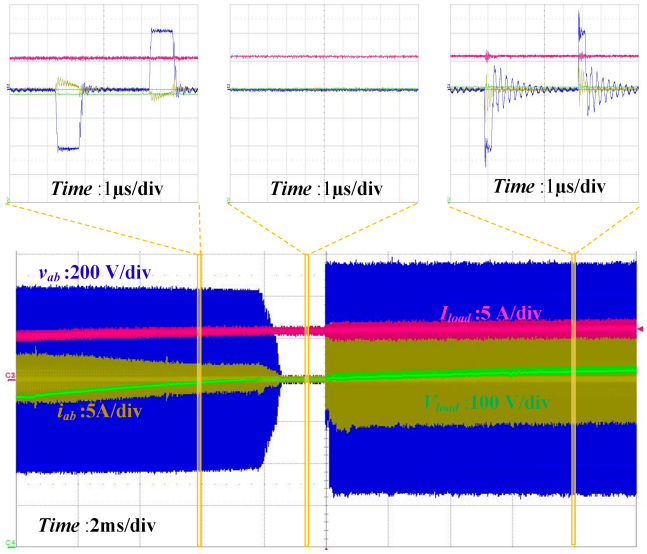


Fig. 17: Operation mode switching transient waveforms of output voltage step changes.

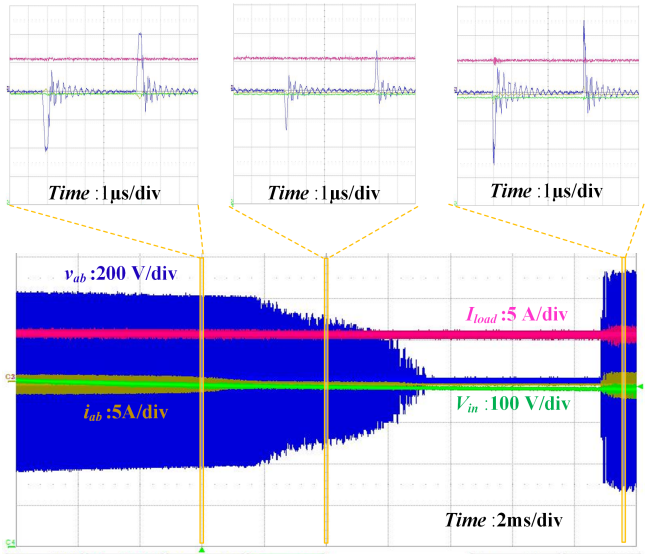


Fig. 18: Operation mode switching transient waveforms of input voltage step changes.

are given by the following equation.

$$\begin{aligned} P_{slc} =& 4I_{LS}^2 \cdot R_{dson} \\ P_{sls} =& 4f_{sw} \cdot \frac{V_{in}}{n} \cdot ((\frac{2I_{ave} - \Delta I_{load}}{2} \cdot t_{ri}) + \\ & (\frac{2I_{ave} + \Delta I_{load}}{4} \cdot t_{fa}) + \frac{Q_{oss}}{2}) \end{aligned} \tag{33}$$

where R_{dson} and Q_{oss} are the conductive resistance and output charge of the switch; t_{ri} and t_{fa} are the rise and fall times of the switch, respectively.

Since S_{5-8} keeps off in SD mode, the conductive and switching losses of S_{5-8} are given by the following equation.

$$\begin{aligned} P_{shc} =& 4 \cdot I_{LS} \cdot V_f \cdot |1 - u| \\ P_{shs} =& 4 \cdot f_{sw} \cdot \frac{V_{in}}{4} \cdot Q_{rr} \end{aligned} \tag{34}$$

where V_f and Q_{rr} are the forward voltage and the recovery energy of the body diode of S_{5-8}, respectively.

In SU mode, S_{1-4} keeps on, thereby S_{1-4} only have the conductive loss in SD mode. The switching and conductive losses of S_{5-8} are given by the following equation.

$$\begin{aligned} P_{shc} =& 4 \cdot I_{HS}^2 \cdot R_{dson} \\ P_{shs} =& 4 \cdot f_{sw} \cdot \frac{V_{in}}{4} \cdot ((\frac{2I_{ave} - \Delta I_{load}}{2n} \cdot t_{ri}) + \\ & (\frac{2I_{ave} + \Delta I_{load}}{2n} \cdot t_{fa}) + Q_{oss}) \end{aligned} \tag{35}$$

Since D_{1-4} is schottky rectifier, the switching loss is negligible. Therefore, the power loss of D_{1-4} is given by the following equation.

$$P_D = 4 \cdot 0.5 \cdot I_{load} \cdot V_D \tag{36}$$

where V_D is the forward voltage of D_{1-4}.

The inductor loss cab be calculated by (37).

$$P_L = I_{load,ac}^2 \cdot R_{Lac} + I_{load,dc}^2 \cdot R_{Ldc} \tag{37}$$

where $I_{load,ac}$ and $I_{load,dc}$ are the ac and dc components of I_{load}; R_{Lac} and R_{Ldc} are the ac and dc resistance of the inductor, respectively.

The transformer losses are split into two parts: core and winding losses, which are be calculated by (38) and (39) respectively.

$$P_{core} = P_v \cdot V_e \tag{38}$$

$$P_w = I_{ab}^2 \cdot R_{acH} + I_{cd}^2 \cdot R_{acL} \tag{39}$$

where R_{acH} and R_{acL} are the ac resistance of high and low voltage side of the transformer respectively.

After calculating ΔB by (40), the P_v can be obtained through the datasheet provided by manufacturer. [28]

$$\Delta B = \frac{V_{in} \cdot |1 - u| \cdot T_s}{2 \cdot n \cdot Ae} \tag{40}$$

At u=1, there is only the conductive loss. The actual conductive loss of 15.9 W is larger than the ideal conductive loss of 10.3 W due to the parasitic resistance. The parasitic resistance in this system can be obtained by dividing the difference between the two losses by the square of the load current, i.e., 0.06 Ω.

Based on the above power loss analysis, Fig. 20 shows the power losses breakdown of the maximum power. The total loss is 72.7 W. Thanks to the reduced I_{HS} and the using of low-voltage MOSFETs, the losses of the switches are small. The losses of S_{1-4} and S_{5-8} are 5.73 and 11.43 W, respectively. Parasitic resistor loss in this case is 17 W, which makes up a major part of P_{other}. The loss of the transformer is about 10.9 W. P_D is 32% of total losses, i.e. approximately 24 W. Therefore, replacing the diodes with the switches can further increase the efficiency.

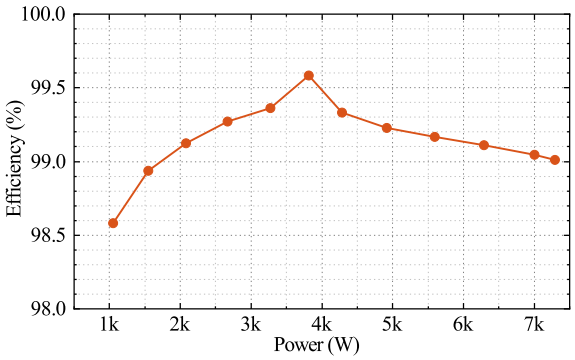


Fig. 19: Experimental efficiency curve.

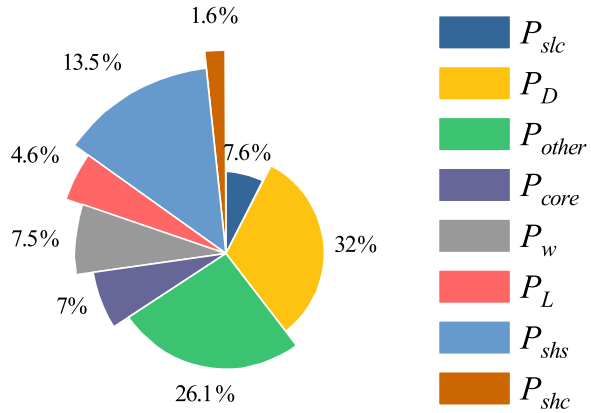


Fig. 20: Power losses breakdown at 7.3 kW.

V. Conclusion

This paper proposed a SUD PPC topology, which has the same SSM for both operating modes. Therefore, a unified modulation strategy is presented for SU and SD modes, resulting in the auto mode switching and control system simplification. Due to the decoupling of transformer, the current stress on high-voltage side components and voltage stress on low-voltage side components are reduced. The performance of the proposed PPC topology is evaluated by the method of CSF analysis. Compared with conventional PPCs, the proposed SUD PPC has the least CSFs with the highest turn ratio. Finally, the experimental results of the 400 V prototype verify the feasibility and practicality of the topology and modulation strategy. Since diode loss is the dominant loss, replacing the HB_1 with the bidirectional switches are critical to further improve the converter's performance, which is next research focus.

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